



# Network Reduction Algorithm for Developing Distribution Feeders for Real-time Simulators

## Preprint

Adarsh Nagarajan, Austin Nelson,  
Kumaraguru Prabakar, and Andy Hoke  
*National Renewable Energy Laboratory*

Marc Asano and Reid Ueda  
*Hawaiian Electric Company*

Shaili Nepal  
*South Dakota State University*

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# Network Reduction Algorithm for Developing Distribution Feeders for Real-time Simulators

Adarsh Nagarajan, Austin Nelson,  
Kumaraguru Prabakar, Andy Hoke  
National Renewable Energy  
Laboratory

Marc Asano, Reid Ueda  
Hawaiian Electric Company

Shaili Nepal  
South Dakota State University

**Abstract**—As advanced grid-support functions (AGF) become more widely used in grid-connected photovoltaic (PV) inverters, utilities are increasingly interested in their impacts when implemented in the field. These effects can be understood by modeling feeders in real-time simulators and test PV inverters using power hardware-in-the-loop (PHIL) techniques. This paper presents a novel feeder model reduction algorithm using a ruin & reconstruct methodology that enables large feeders to be solved and operated on real-time computing platforms. Two Hawaiian Electric feeder models in Synergi Electric’s load flow software were converted to reduced order models in OpenDSS, and subsequently implemented in the OPAL-RT real-time digital testing platform. Smart PV inverters were added to the real-time model with AGF responses modeled after characterizing commercially available hardware inverters. Finally, hardware inverters were tested in conjunction with the real-time model using PHIL techniques so that the effects of AGFs on the feeders could be analyzed.

**Index Terms**— advanced grid-support functions, power hardware-in-the-loop simulation, network reduction, real-time simulator, smart PV inverter

## I. INTRODUCTION

This paper proposes a novel way to develop reduced order equivalents of real-world distribution feeders for power hardware-in-the-loop (PHIL) experiments. PHIL simulations are receiving increased attention from utilities due to their ability to provide a window through which utilities can understand operational behavior of physical devices without causing power disturbance or outages. PHIL simulations run on real-time simulation platforms including, but not limited to, Real-Time Digital Simulator (RTDS) and OPAL-RT.

PHIL experiments are a hybrid utilizing a software simulation and physical hardware testing. Data exchanges occur at each transient time-step between simulation and hardware, and power is virtually exchanged with physical hardware, in contrast to control hardware-in-the-loop (CHIL) simulation, which involves only signal exchange. In contrast to CHIL, PHIL experiments require high power flows between the real component and the simulated electric circuit running on the simulator using PHIL techniques that are required to test power converters, generators, FACTS, etc. The physical equipment is interfaced to the simulator using voltage and power amplifiers that can generate and absorb power since the simulator works with low levels of voltage and current.

Utilities are increasingly interested in understanding the impacts of advanced inverter controls on real feeders, creating

a demand for accurate reduced order equivalents for real-world feeders. Since real-time simulators used for PHIL experiments often cannot solve a network model with several thousand nodes in real-time, a reduced-order model must be developed as a precursor to the PHIL simulation. The model reduction algorithm proposed in this paper develops a reduced-order equivalent representing the salient aspects of the original feeder. A typical distribution feeder with several thousand nodes was reduced to a model with only eight nodes using an iterative bottom-up approach, where the user chooses the nodes to be retained. The reduced-order equivalent model was validated for a range of loading conditions (100%, 75%, 50%, and 25% loads) to ensure that the reduced feeder accurately represented the original feeder for a wide range of operating scenarios.

Additionally, distribution-connected photovoltaic (PV) generators are typically distributed throughout a given feeder. With a goal to develop a distribution feeder model with geographically distributed PV throughout, the nearest retained node to each PV generator in the reduced feeder model was identified as part of the network reduction process. As a part of this effort, a methodology was developed to identify the nearest retained node (either the nearest upstream or downstream retained node) to which each PV generator needed to be connected. Simple PV generator models capable of advanced grid support functions (AGF) were aggregated into each node of the reduced order model. Representative PHIL experimental results performed in conjunction with the Hawaiian Electric Companies are presented with a variety of AGF enabled PV inverters and results are compared to the full feeder model simulation. Such experiments are a test platform for utilities to evaluate the effects of deploying AGFs in the field for large and complex feeders.

## II. BACKGROUND ON NETWORK REDUCTION

Studies on the topic of network reduction are old and frequently visited. Even though a detailed work on the reduction of a network was published in the year 1949 [1], the topic of network reduction has been revisited at regular intervals over time [2–4]. Most of these seminal reduction techniques are heuristic (experience-based) or semi-heuristic in nature. These methods have been developed for transmission systems with multiple, physically distant synchronous generators. However, this work concentrates on distribution systems and involves the modeling of large numbers of distributed PV generators.

Ischenko, Jokic, Myrzik, and Kling [5] provided an approach for dynamic reduction of the distribution networks

with wind systems and neglected the PV generators. Le, Tran, Devaux, Chilard, and Caire [6], in contrast, focused on the synchronous generators and disregarded the participation of the power electronics interfaced renewable sources for system studies.

A technique similar to the proposed technique was described by Oh [7], involving a network reduction algorithm based on the grouping of nodes. The distinction between the referred study and the current study is that the grouping in Oh’s study was decided based on congestion studies, whereas this work selects retained nodes based on user input and importance to the circuit (e.g. nodes with capacitors or regulators are retained).

In [8], a network-reduction technique was proposed using the minimum spanning tree (MST) algorithm. This algorithm identifies the nearest three-phase section for each load and PV generator, and focuses on retaining the three-phase laterals and not on reducing the feeder. A similar publication authored by Matthew Reno et.al. [9] is based on a load bus reduction formula, with the key assumption that all loads on the feeder are fixed current loads, which is atypical in real-world field applications.

When compared with all of the previous work in the area of research, this paper stands different in its approach as well as its application in that it can be used to reduce any given radial feeder model with any types of loads and PV. The real-time simulators used for the PHIL experiments cannot solve the entire network model with several thousand nodes in real-time, therefore a feeder model reduction technique has been developed, as described in the following section.

### III. PROPOSED NETWORK REDUCTION APPROACH

The proposed approach is based on the ruin and reconstruct principle. The approach based on ruin and reconstruction is conceptually simple but at the same time a powerful meta-heuristic technique for this application. The main components of this method are a ruin (mutation) procedure and a recreate (improvement) procedure. One way to develop a reduced network is based on destruction in which we start from a full network and remove the network components until we have the smallest possible feeder. However, this paper proposes a methodology based on the concept of injection. A reduced-order equivalent of the original feeder is developed by choosing the appropriate line lengths in order to match the voltages and sequence impedances at the retained nodes. The method of network reduction is summarized in Figure 1.

The model reduction process runs up to 50,000 Monte Carlo simulations, with varying line-lengths based on a Latin-Hypercube Sampling (LHS) random number generator. The network reduction algorithm is realized in Python programming language in conjunction with OpenDSS for performing distribution system power flow. Figure 2 shows a high-level view of the algorithm identifying the combination of line-lengths for all lines for which the voltage errors and sequence impedance errors are at a minimum.

The steps involved in developing the reduced network are listed below:

**Step 1: User-input** - User selects any specific buses that should remain in the reduced circuit. The algorithm automatically identifies additional buses of interest such as capacitors, voltage regulators, step transformers between buses of interest, and junctions required to maintain the topology in the reduced circuit. A baseline reduced circuit is generated consisting only of the retained nodes connected by lines whose length is determined in step 3. The line types are selected by identifying the most common line type in the feeder.

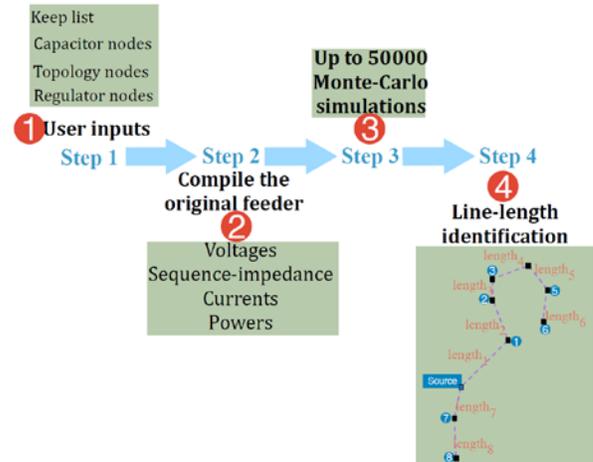


Figure 1. Outline of the network reduction process

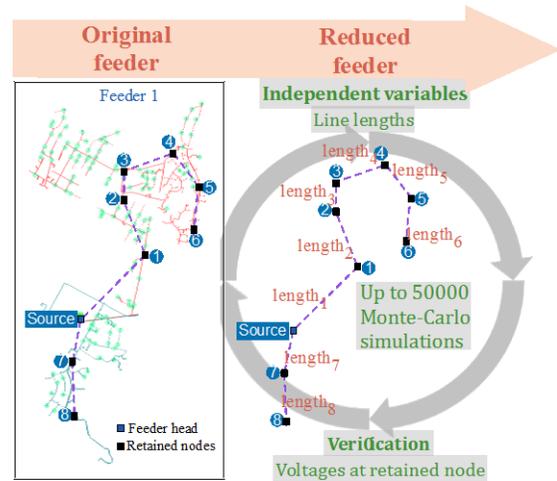


Figure 2. High-level view of the network reduction process demonstrating the node selection process

**Step 2: Original data capture** – Power-flow is performed on the original feeder to capture voltages, sequence impedances, and three-phase unbalanced active and reactive powers at the retained nodes. The aggregated unbalanced loads at retained nodes are calculated directly from the three-phase power flow.

**Step 3: Monte Carlo simulations** – A line-length identification algorithm runs up to 50,000 Monte Carlo simulations of the reduced feeder, with varying line-lengths based on an LHS random number generator. In other words, the line lengths are varied across a wide range, and the power flow is solved with each combination of line lengths.

**Step 4: Identify reduced feeder** – The algorithm chooses the appropriate combination of line lengths for which mini-

imum voltage errors and sequence impedance errors can be obtained across several circuit loading conditions.

#### IV. TEST FEEDER REDUCTION AND VALIDATION

The network reduction and modeling consisted of two stages as described below. Stage 1 consisted of developing a reduced feeder having eight nodes using the technique described above, starting from a full feeder containing  $\approx 3000$  nodes, and primarily modeled in the quasi-static domain. Stage 2 involved porting the previously-developed reduced network to a real-time simulator operating in the electromagnetic transient (EMT) domain. The accuracy of the reduced feeder model was verified by comparing them with the original model. In order to ensure that the reduced feeder was valid for a variety of operating conditions, the voltages were compared at a variety of load levels. This entire process was repeated for two Hawaiian Electric feeders, identified as Feeder 1 and Feeder 2.

The maximum number of retained nodes is determined by the desired time step of the real-time simulation. For an EMT simulation, the time step must be roughly two orders of magnitude faster than a 60 Hz period, thus the circuit must be simple enough that the real-time computer can solve it in that time step. For phasor domain real-time simulations, a time step on the order of 60 Hz or slower can be used, so a much higher number of nodes could be retained. EMT simulations were used in this work because sub-cycle effects were of interest; such effects would not be captured by a phasor-domain simulation.

##### A. Stage 1 – Network reduction in quasi-static analysis tool

The original feeder models were provided by the Hawaiian Electric in Synergi and were subsequently converted to OpenDSS. They were then reduced using the described reduction techniques. A visualization of the original models and retained nodes for the reduced models is shown in Figure 3. The summary of three-phase voltages at the retained nodes for both feeder models along with the error in voltages between the full Synergi model and the reduced OpenDSS model are tabulated in Table I.

The reduced Feeder 1 voltages when compared with the Synergi model had maximum error of 0.7%, as shown in Table I. Similarly, the reduced Feeder 2 voltages when compared with the original Synergi model had a maximum error of 0.6%.

TABLE I. MEAN AND MAXIMUM VOLTAGE ERRORS

Load Level (%)	Feeder 1		Feeder 2	
	Mean Error (%)	Max Error (%)	Mean Error (%)	Max Error (%)
50	0.25	0.4	0.15	0.29
75	0.382	0.6	0.24	0.52
100	0.51	0.7	0.3	0.6

##### B. Stage 2 – Reduced model development in real-time simulator

The reduced order OpenDSS model was subsequently transformed into a real-time model in OPAL-RT by creating an analogous model in Simulink using the SimPowerSystems toolbox. An eight node primary circuit was created by implementing an ideal voltage source with source impedance at the feeder head, and then placing  $RL$  equivalent line impedances between each of the primary nodes as well as real and reactive loads at each of the nodes.

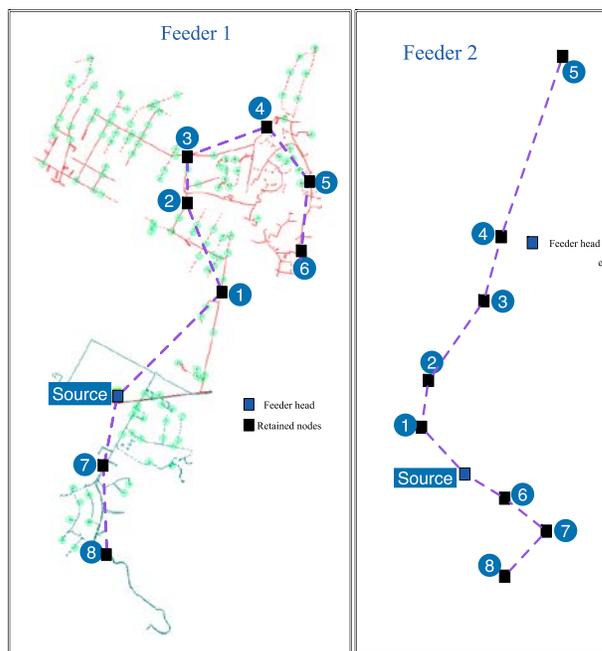


Figure 3. View of the original feeder with the nodes that were retained

Additionally, the real-time model contained modeled PV inverters at each of the primary nodes. The PV inverters were modeled as power-controlled current sources capable of various AGFs such as fixed power factor, volt-watt (V-W), voltage and frequency ride through, and power ramp rate control. Several commercially available PV inverters were experimentally characterized for their responses to abnormal grid conditions and dynamic behavior with these AGFs enabled. The modeled PV inverter dynamic responses were tuned to match the hardware inverter responses.

Each primary node contained four classes of inverters: 1) AGF-capable microinverters, 2) legacy microinverters, 3) AGF-capable string inverters, and 4) legacy string inverters (where “legacy” is used to describe inverters not capable of certain AGFs). The total power rating of each inverter type at each node was determined in conjunction with the utility, representing a combination of existing net energy metered (NEM) installations, NEM systems (with smart PV inverters) currently in the interconnection queue, projected future growth of Customer Grid Supply installations (with smart PV inverters), and a variety of legacy PV inverter retrofit scenarios. The total rating of each inverter type at each node represented an aggregation of all PV in a given section of the feeder, according to how the retained nodes were aggregated in the model reduction.

tion. Finally, detailed distribution feeder secondary circuit models provided by Hawaiian Electric were added to each model at one location in order to create an interconnection point between the test inverters and the medium voltage distribution network. Additional details of the inverter characterization tests and subsequent PHIL tests are found in [10].

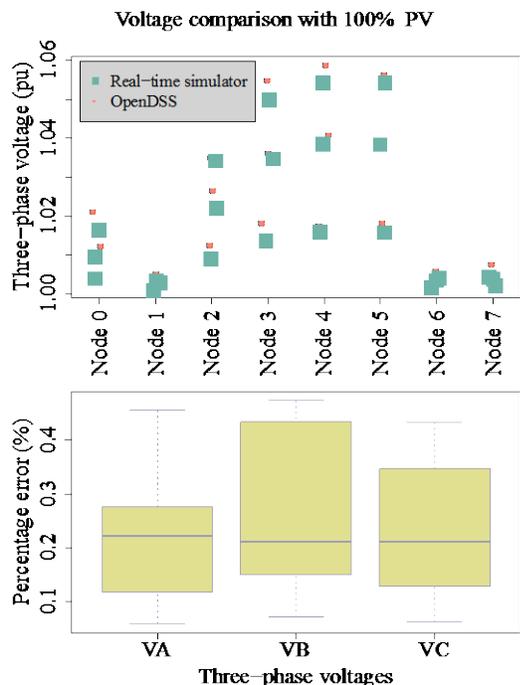


Figure 4. Voltages and errors at the retained nodes for the reduced order OpenDSS model and the real-time model for the 100 % scenario

The OpenDSS model and the real-time model are compared for several test cases in Table II. A summary of mean and maximum voltage errors for each phase and each PV rating scenario is shown in Table II. Figure 4 shows the error in phase voltages on the Feeder 1 model, with PV inverters operating at 100% of nominal output power. The loads were set to 86.6% of maximum daily load for this test case, and the feeder source voltage was set to 105% of nominal. The maximum error for any phase voltage and any of these PV rating scenarios was 0.50%, and the mean error was 0.26%, demonstrating good agreement in the primary node voltages after converting the quasi-static domain model to the real-time domain.

TABLE II. MEAN AND MAXIMUM PHASE VOLTAGE ERRORS FOR FEEDER 2 MODEL AT VARYING PV RATINGS

PV Rating (%)	Phase A		Phase B		Phase C	
	Mean Error (%)	Max Error (%)	Mean Error (%)	Max Error (%)	Mean Error (%)	Max Error (%)
0	0.23	0.39	0.27	0.50	0.33	0.48
50	0.29	0.47	0.25	0.40	0.27	0.48
100	0.22	0.46	0.27	0.47	0.23	0.43

## V. PHIL TESTING WITH REAL-TIME MODEL

The validated real-time model was subsequently used for hardware experiments using PHIL testing techniques. A block diagram for the test setup is shown in Figure 5, which shows a configuration for testing two different hardware PV inverters. Two points of interconnection were selected from the secondary circuit, which was connected to the primary through a step down transformer. The low-voltage grid signals were output from the real-time model interface and amplified through a controllable AC voltage source to create the 120/240V output signal to the inverters. The AC voltage source was a 45 kVA power supply with sourcing and sinking capability. The DC sides of the PV inverters under test were supplied from an appropriately-sized PV simulator, and the inverter output current was measured and fed back into the real-time model. Additional filtering and phase lag compensation techniques were employed in the model to preserve system stability and accuracy, as in [11].

The complete real-time model with hardware PV inverter setup was then used to test a wide range of AGFs and evaluate the effects of dispatching such functions on these feeders in the field. Specifically, different configuration scenarios of the V-W function with fixed power factor operation were studied to examine the effects on node voltages during dynamic changes in PV power output on the network. A comprehensive review of all test cases and the conclusions drawn in this study is provided in [10]. All PHIL tests were operated with time steps in the range of 180-260  $\mu$ s in the real-time model, depending on the complexity of the model and the test.

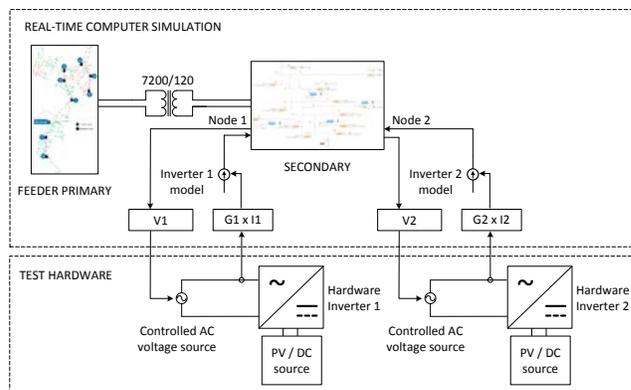


Figure 5. PHIL testing configuration for multi-inverter experiments

An example PHIL test result is shown in Figure 6. In this test case, all inverters were operating at 0.95 power factor (absorbing), and the V-W curve was set to begin linearly curtailing power at 106% of nominal voltage, reaching zero power at 110% of nominal voltage. A fast irradiance ramp (simulating clouds quickly clearing) was applied to both hardware and modeled inverters, changing from 200  $W/m^2$  to 1000  $W/m^2$  in 40 seconds. The rapid increase in PV output power, i.e. from 200  $W/m^2$  to 1000  $W/m^2$  in 40 seconds, caused voltage rise in the secondary circuit, thus triggering the V-W function. The V-W function reduced the PV active-power to bring back the voltage at point of common coupling back to within threshold. In this test, the hardware inverter settled out to 43% of rated power at  $\sim$ 107% of nominal voltage. Dashed lines in

Figure 6 represent voltages and aggregated inverter powers within the real-time simulation, and the solid lines represent the hardware inverter.

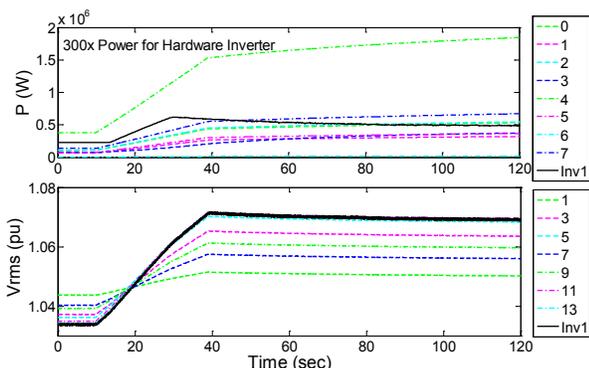


Figure 6. Sample PHIL test result showing effect of V-W function and 0.95 power factor on secondary voltages (Feeder 2 model)

One key advantage to the feeder reduction methods described in this paper is that feeder-level effects can be observed following transient-level real-time events. Additional tests in this study included voltage and frequency ride-through events, soft start ramp rate, and normal power ramp rates due to irradiance changes. Figure 7 shows an example of a low voltage ride-through event, where there was a rapid decrease in source voltage, forcing all modeled and hardware inverters to trip. In subsequent tests, the PV inverters were enabled to ride through the same event, and the difference in system level node voltages was analyzed.

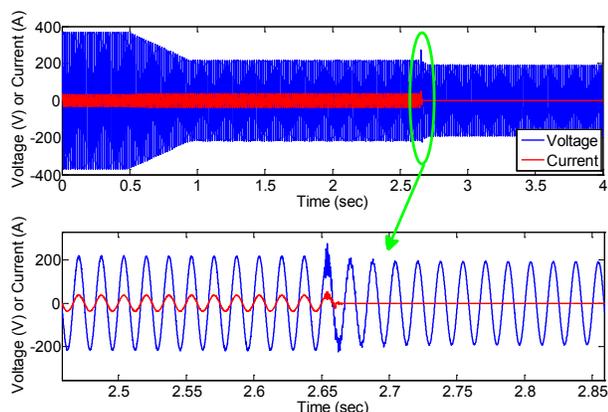


Figure 7. Low voltage ride through event showing hardware inverter tripping. Model reduction techniques provide a means to examine feeder-level effects of transient real-time events.

## CONCLUSIONS

A novel feeder network reduction algorithm based on ruin & reconstruct methods has been presented converting two Hawaiian Electric feeder models consisting of several thousand nodes into reduced order real-time models reduced to eight primary nodes. The network comparison between the full OpenDSS feeder models to the real-time model (Table II) yielded a maximum voltage error of 0.5%. The real-time mod-

el was subsequently used to evaluate the effect of various advanced grid support functions on the modeled feeders using power hardware-in-the-loop testing techniques. This feeder model reduction algorithm is a powerful tool to evaluate the benefits of the activation of various inverter grid support functions on large, complex, feeders with high penetrations of rooftop legacy PV that otherwise cannot be solved on a real-time test platform.

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