Inverter Anti-Islanding with Advanced Grid Support in Single- and Multi-Inverter Islands

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Mahalo to:

- **SolarCity – Frances Bell, Mike McCarty**
- **NREL – Austin Nelson, Brian Miller, Sudipta Chakraborty (PI)**
- **The Hawaiian Electric Companies:**
  - Marc Asano – Technical input
  - Earle Ifuku – SITWG lead
- **Department of Energy Solar Energy Technologies Program**
- **Northern Plains Power Technologies – Mike Ropp**

Overview

1. **Background**
2. **Single-inverter anti-island tests with grid support functions (GSFs) enabled**
   a) Test plan
   b) Test results
3. **Multi-inverter anti-islanding tests with GSFs enabled**
   a) Test plan
   b) Test results
4. **Conclusions**

Background

- **Island = portion of a circuit with DER and load that becomes disconnected from the rest of the grid**

NASA - http://earthobservatory.nasa.gov/IOTD/view.php?id=82975

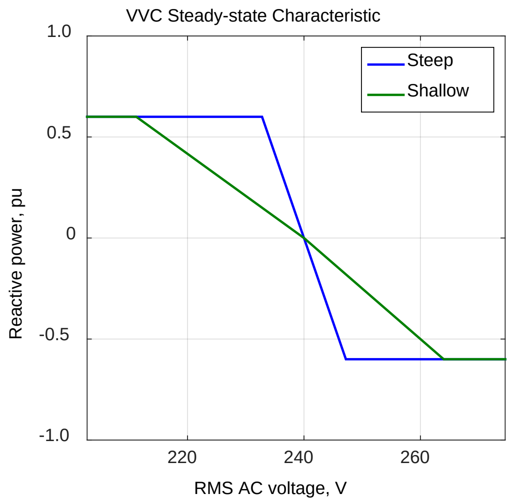
- **DERs must recognize when they are in an island and disconnect**
  - *Safety* – prevent contact with unexpectedly energized lines
  - *Protection* – prevent out-of-phase reclosure

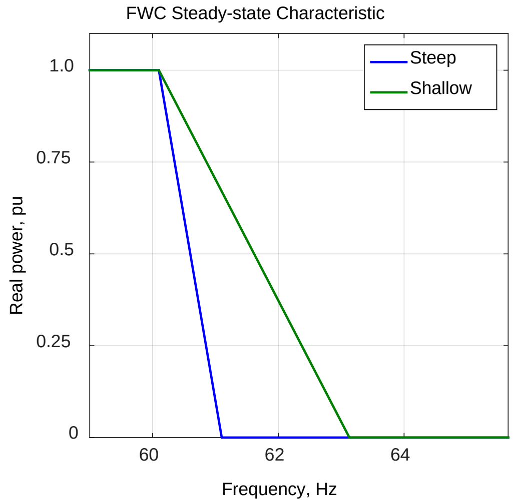
Background

- If generation and load are not matched (or close), island voltage goes out of range quickly (undervoltage or TrOV) and DERs disconnect
- If gen:load ≈ 1, island may persist
- IEEE 1547 requires DERs to disconnect within 2 seconds
- Most common method of unintentional island prevention:
  - Autonomous anti-islanding (AI) controls in the DER
  - All UL 1741-certified inverters contain such controls

Background

- **As DERs become a significant portion of total generation, they will be required to:**
  - Remain online during grid events
  - Help regulate grid voltage and frequency back towards nominal
- **These grid support function (<u>GSF) requirements</u> *may* make anti-islanding more difficult**
- **Islands with <u>multiple DERs</u> *may* also make anti-islanding more difficult**





This work

- **Experimentally create balanced islands with:**
  - GSFs enabled
  - 3 PV inverters *connected to different points* on the same circuit
- ***Can we create islands lasting more than IEEE allows?***
  - Balanced, resonant load → difficult for island detection
- **Test inverters from *3 different manufacturers***
- **Two phases:**
  1. Single-inverter islands: identify worst-case combinations of GSFs
  2. Multi-inverter islands: try various circuit topologies, interconnecting impedances, load locations, load tunings, inverter locations, GSF combinations

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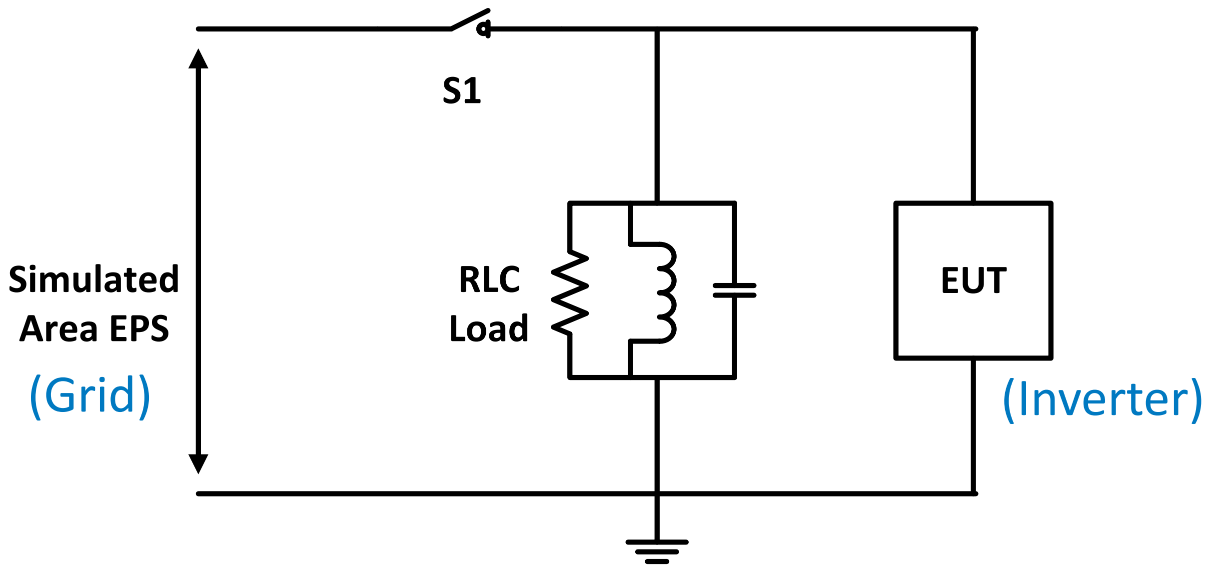
Island test overview

- **AI tests based on IEEE 1547.1 / UL 1741 test:**



Steps:

1. Carefully tune load P, Q so fundamental current in S1 is nearly zero and QF = 1.0
2. Open switch S1
3. Measure time until inverter disconnects

- **Balanced, resonant RLC load intentionally creates a stable, semi-self-sustaining island that is difficult to detect**
- **Inverter powered by PV simulator → constant, stable source**

Grid support functions

- **Conventional AI test does not include testing with GSFs enabled**
  - Upcoming UL 1741 SA does
- **GSFs used here:**
  - High/low voltage ride-through (VRT)
  - High/low frequency ride-through (VRT)
  - Volt-VAr control (VVC)
  - Frequency-Watt control (FWC)
- **Two settings tested for both VVC and FWC:**
  - Steep curve
  - Low-slope ("shallow") curve
- **Each GSF first verified to work properly**

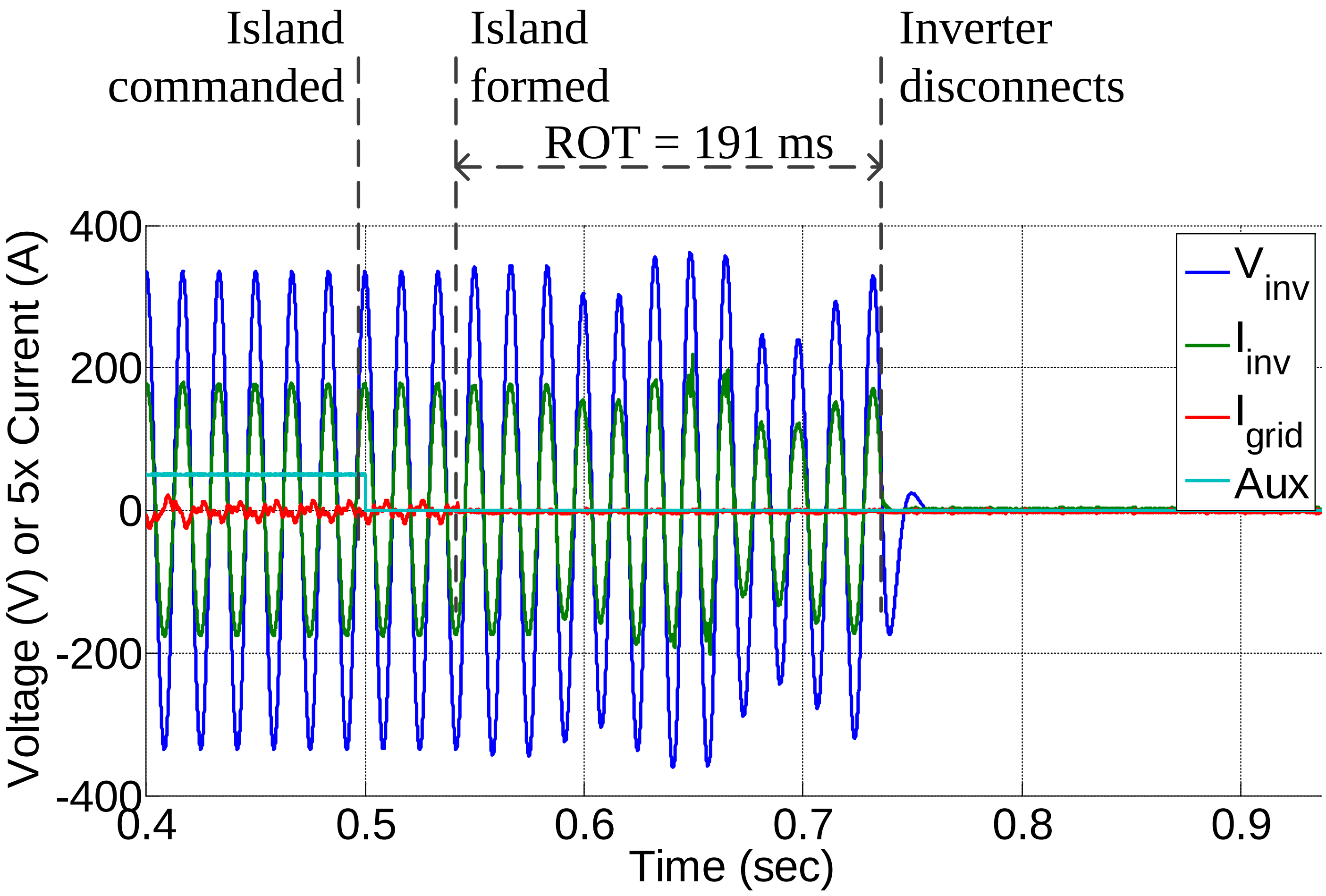
Grid support functions

- **10 GSF test cases:**

Test Case	Inverter Function Settings			
	VRT	**FRT**	**FWC**	**VVC**
1	OFF	OFF	OFF	OFF
2	ON	ON	OFF	OFF
3	ON	ON	OFF	SHALLOW
4	ON	ON	OFF	STEEP
5	ON	ON	SHALLOW	OFF
6	ON	ON	SHALLOW	SHALLOW
7	ON	ON	SHALLOW	STEEP
8	ON	ON	STEEP	OFF
9	ON	ON	STEEP	SHALLOW
10	ON	ON	STEEP	STEEP

- **Repeat each 5 times → 50 tests per inverter**

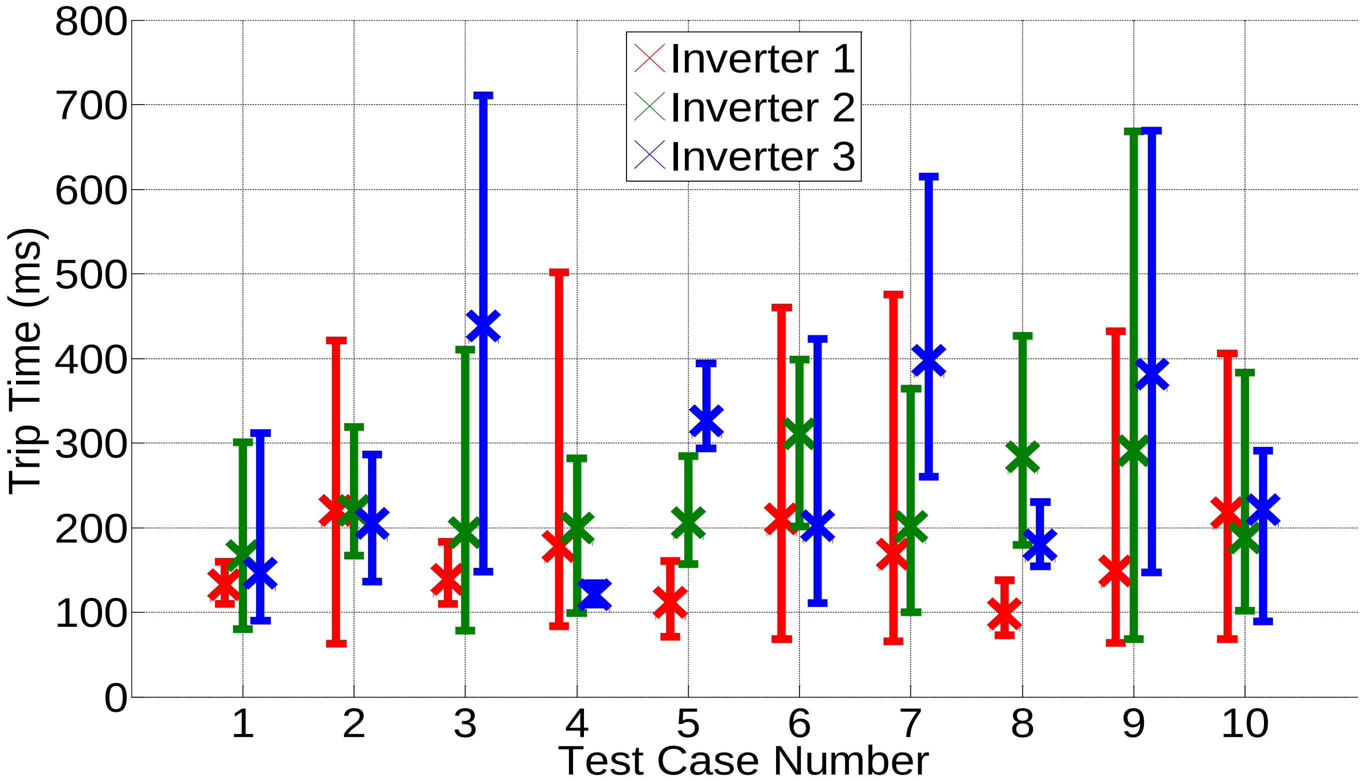
Interpreting AI test results:



ROT = run-on time (island duration)

Single-inverter Results

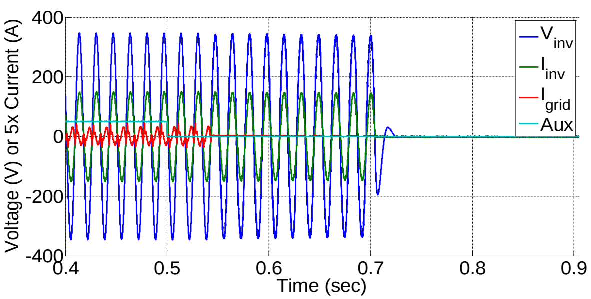
Maximum, mean, and minimum island ROT:

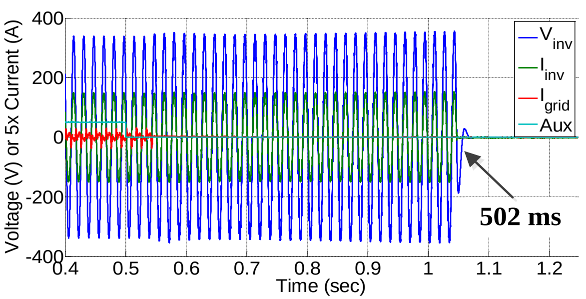


Maximum ROT is most important criterion

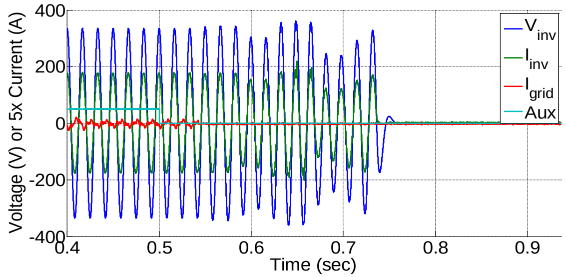
Typical and worst-case waveforms

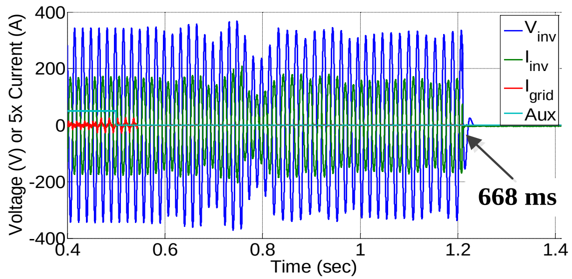
Inverter 1



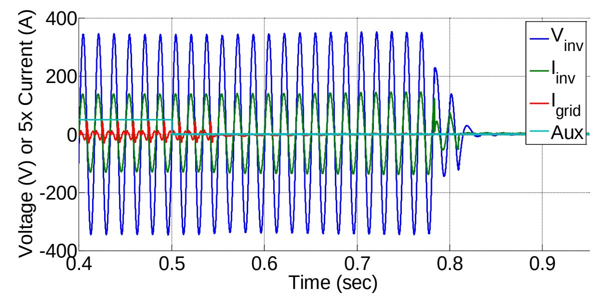


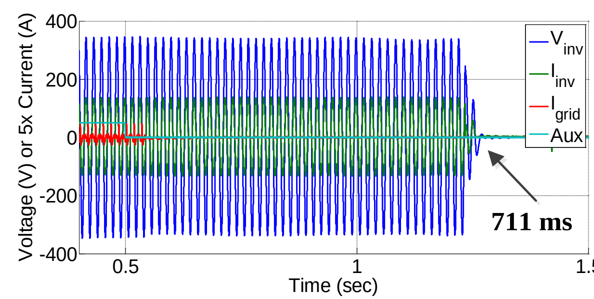
Inverter 2





Inverter 3





Linear regression analysis

- **Linear regression of all test data (>150 tests):**
  - o VRT and FRT considered as a single binary predictor, *VFRT*; 0=off.

$$ROT = 95 + 75 \cdot VFRT + 64 \cdot Inv2 + 99 \cdot Inv3 + \varepsilon \quad \text{[ms]}$$

  - o p-value = 0.0005
  - o RMS error = 133 ms
- **What does this tell us?**
  - ➢ Enabling VRT and FRT tends to extend ROT by 75 ms
  - ➢ Inverter 2 tends to run on 64 ms longer than Inverter 1
  - ➢ Inverter 3 tends to run on 99 ms longer than Inverter 1
  - ➢ Stochastic effects are larger than modeled effects
- **Additional regression models including VVC and FWC were not conclusive (high p-values)**

Single-inverter conclusions

- **All inverters passed all 50 tests well within required IEEE 1547 AI standard**
- **VRT and FRT lead to *slightly* longer islands**
- **Worst-case overall GSF configurations:**

Inverter	**Voltage ride-through**	**Frequency ride-through**	**Frequency-Watt**	**Volt-VAr**
1	ON	ON	OFF	HIGH
2	ON	ON	HIGH	LOW
3	ON	ON	OFF	LOW

- **Second worst-case GSF configurations:**

Inverter	**Voltage ride-through**	**Frequency ride-through**	**Frequency-Watt**	**Volt-VAr**
1	ON	ON	OFF	OFF
2	ON	ON	LOW	LOW
3	ON	ON	HIGH	LOW

- **Upcoming paper:** A. Nelson, A. Hoke, B. Miller, S. Chakraborty, F. Bell, M. McCarty, "Impacts of Inverter-based Advanced Grid Support Functions on Islanding Detection," 2016 *IEEE Innovative Smart Grid Technologies Conference (ISGT)*, 2016

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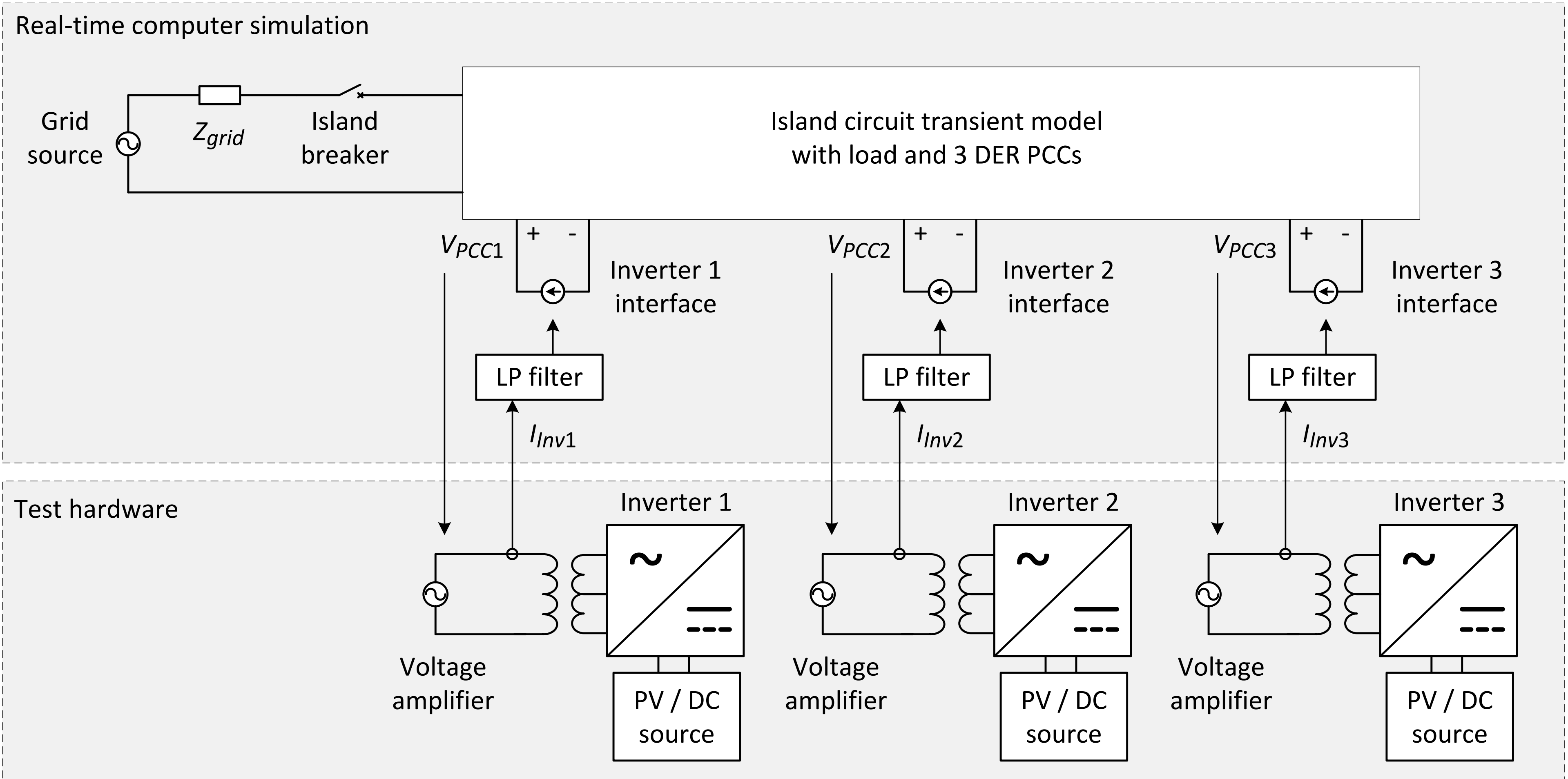
Multi-inverter, multi-PCC anti-islanding

- **Difficult to analytically predict worst-case circuit parameters for multi-inverter AI**
- **Instead, test a wide, representative variety of scenarios to find worst-case circuit parameters**
    - Vary topology, impedances, load location, short-circuit impedance, GSF settings, inverter locations
    - Too many parameters to test all combinations
- **Four-step plan**
    - First 3 steps find worst-case setting(s) of target parameters
    - 4^{th} step investigates worst-case settings in-depth
- **224 test total (plus extras)**

Step	Parameters Varied	Number of Tests	Number of Worst-Case Conditions Selected
1	Circuit topology and impedances	50	3
2	Load location relative to inverters	15	1
3	Short-circuit impedance of grid at island breaker	15	1
4	Inverter locations and GSF settings	144	NA

PHIL anti-island testing

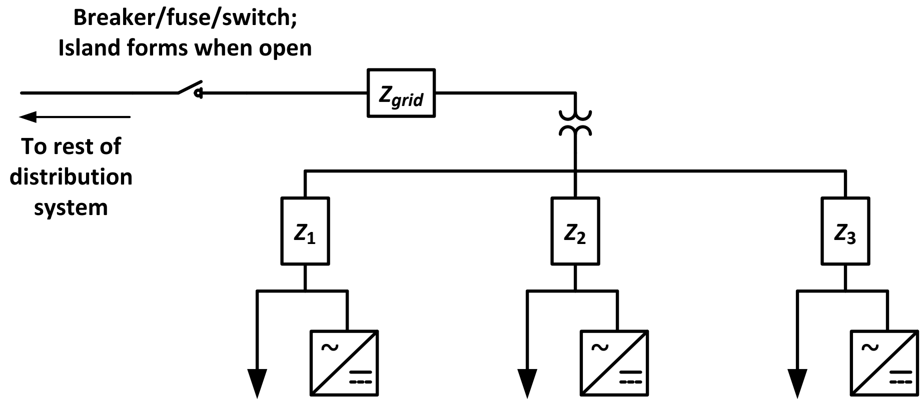
- Building a wide variety of test circuits is costly and time-consuming
- Instead, use power hardware-in-the-loop to create the island circuits (including the RLC load)
- Builds on past single-inverter PHIL AI testing, and multi-inverter GSF testing



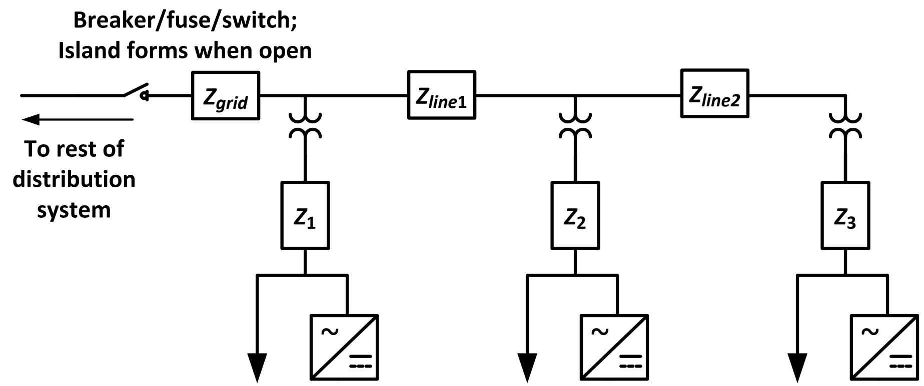
Step 1: Topologies

- Three island topologies
- Each LV line can be overhead or underground
- Service drops of 100', 200' and 300' considered
- 10 total circuits considered in Step 1
- Each circuit tested 5 times → 50 tests
- Worst-case circuit used for Steps 2 and 3
- Three worst cases used in Step 4

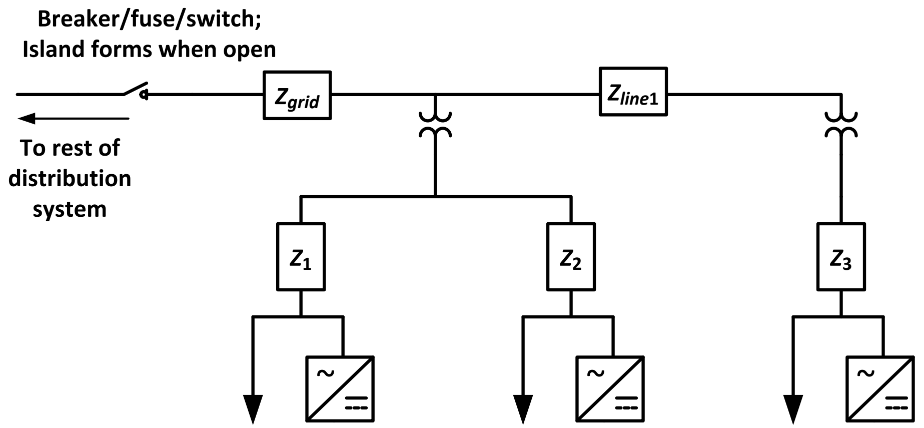
Topology 1:
Three inverters on same transformer



Topology 2:
Three inverters on three different transformers

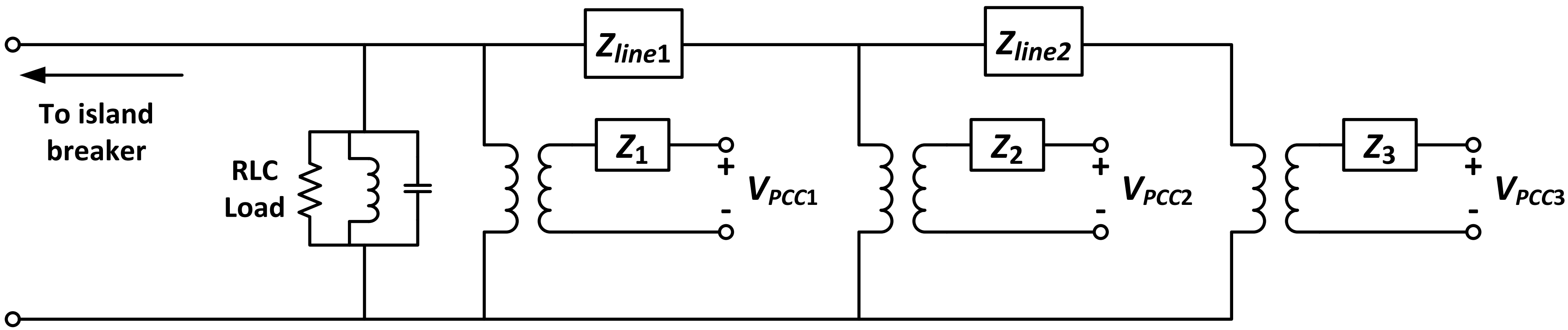


Topology 3:
Two inverters on one transformer and one on a second



Step 2: Load location

- **Three possible load locations considered:**
  1. Centralized load *near* island breaker
  2. Centralized load *far* from island breaker
  3. *Distributed* load at each inverter PCC
- **Each load location tested 5 times → 15 tests**
- **Worst-case load location used for Steps 3 and 4**
- **Example island circuit with load near breaker:**



Step 3: Short-circuit impedance

- **Some AI methods rely on changes in grid impedance to detect an island**
- **Range of impedances generated by analyzing the short-circuit impedances at all distribution transformer primary nodes in the IEEE 8500-node test feeder:**
  - Test cases: Maximum, median, minimum Z_{SC}
- **Each Z_{SC} tested 5 times → 15 tests**
- **Worst-case Z_{SC} used for Step 4**

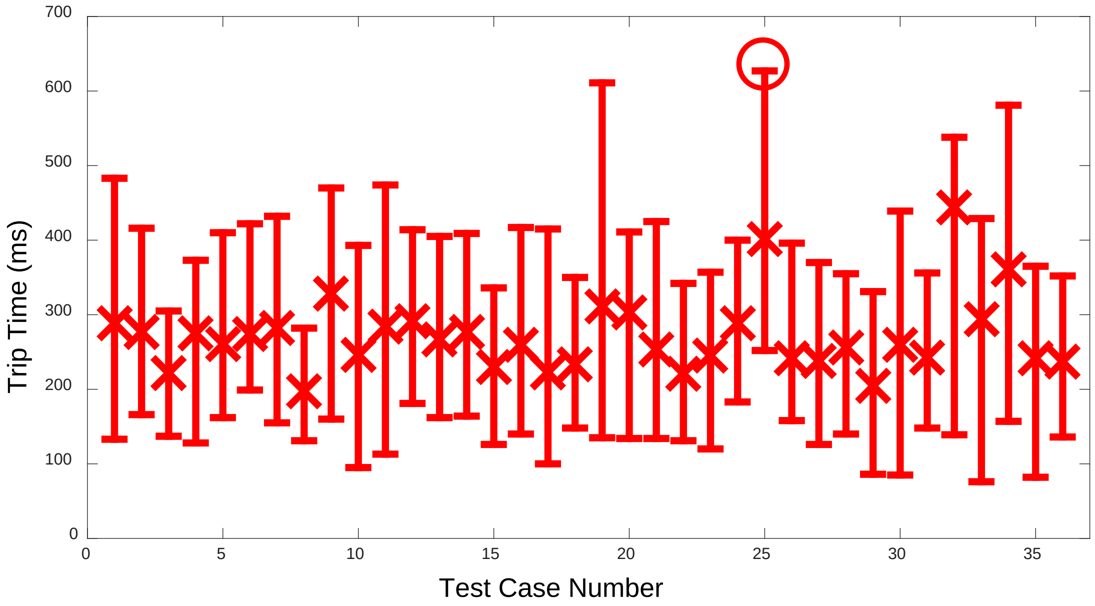
Impedance Z_{SC}	**R (Ω)**	**X (Ω)**
Minimum	0.00195	0.00334
Median	0.0198	0.0249
Maximum	0.0747	0.105

Step 4: Detailed AI investigation

- **All combinations of the following:**
  - The 2 worst-case inverter settings from the single-inverter tests
  - The 3 worst-case combinations of topology and impedances from Step 1
  - The single worst-case load location from Step 2
  - The single worst-case grid impedance from Step 3
  - All 3! = 6 permutations of inverter locations on the 3 PCCs in each test circuit.
- **2·3·1·1·6 = 36 test cases**
- **Each case repeated 4 times → 144 tests**

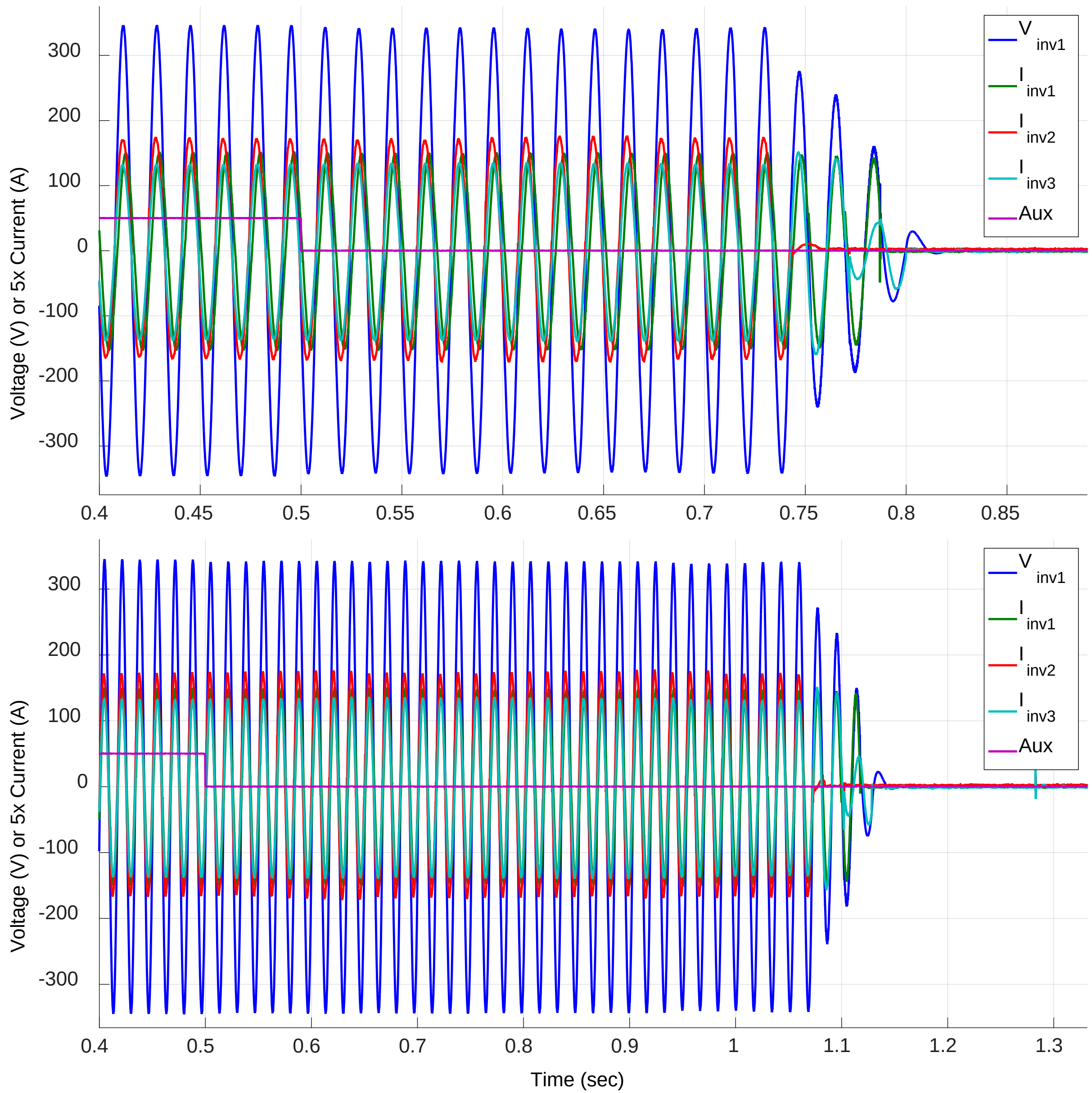
Step 4 Results

Maximum, mean, and minimum island ROT:



Test Case	Test Settings		
	Inverter GSF Configuration	Circuit #	Location Map
1	1	1	1
2	1	1	2
3	1	1	3
4	1	1	4
5	1	1	5
6	1	1	6
7	1	2	1
8	1	2	2
9	1	2	3
10	1	2	4
11	1	2	5
12	1	2	6
13	1	3	1
14	1	3	2
15	1	3	3
16	1	3	4
17	1	3	5
18	1	3	6
19	2	1	1
20	2	1	2
21	2	1	3
22	2	1	4
23	2	1	5
24	2	1	6
25	2	2	1
26	2	2	2
27	2	2	3
28	2	2	4
29	2	2	5
30	2	2	6
31	2	3	1
32	2	3	2
33	2	3	3
34	2	3	4
35	2	3	5
36	2	3	6

Step 4 Waveforms – Typical and worst-case



- **Worst-case: Case 25**
- **627 ms ROT (less than maximum from single-inverter tests)**

Linear regression analysis

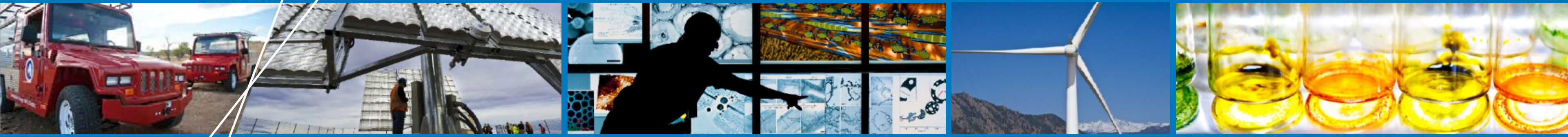
- **Linear regression of all multi-inverter test data (224 tests)**
- **Predictors considered:**
  - Grid support function configuration
  - Island circuit
  - Location of load relative to inverters
  - Grid short-circuit impedance at the island location
  - Inverter location map (i.e. which inverter is connected to which PCC)
- **Most models had high p-values**
- **One model with GSF setting as only predictor had reasonably low p-value:**

$$ROT = 297 + 27 \cdot GSF2 + \varepsilon \quad [\text{ms}]$$

  - p-value = 0.046
  - RMS error = 98 ms
  - $GSF2 = 0$ means worst-case GSF combo was active; $GSF2 = 1$ means 2nd worst-case was active
- **What does this tell us?**
  - ➢ The second-worst GSF function combination (from single-inverter tests) actually tended to run on 27 ms longer than the worst in multi-inverter tests
  - ➢ Stochastic effects are larger than modeled effects
  - ➢ No single circuit configuration stuck out as problematic

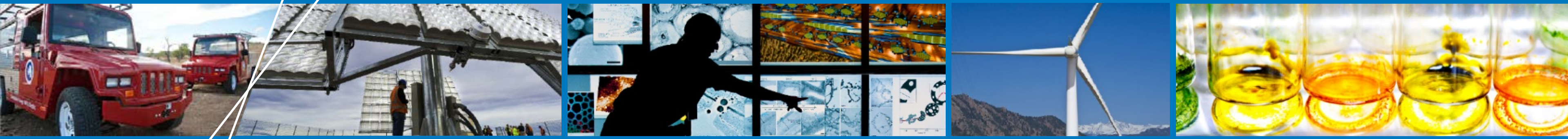
Conclusions

- **First known laboratory test of multi-inverter, multi-PCC anti-islanding**
    - Tests covered 49 unique field cases, each tested at least 4 times
    - In all 244 tests, maximum ROT was 632 ms (well below 2 s)
    - No single circuit configuration stuck out as problematic
- **Grid support functions increased island durations, but still well below the IEEE 1547 required limit**
    - True even in multi-inverter scenarios
    - Results will vary with other inverters, different numbers of inverters
- **NREL report: http://www.nrel.gov/docs/fy16osti/66732.pdf**



Thank you

Questions welcome



Extra slides

Test circuit topologies

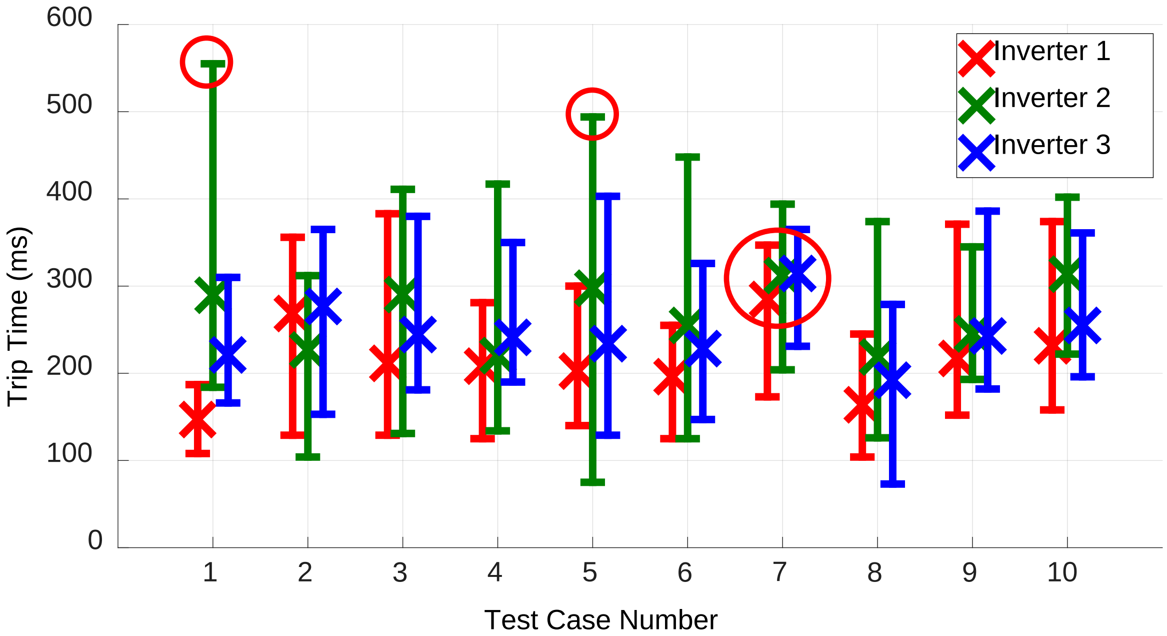
Test Case	Description	# of Transformers	# of Overhead Lines	# of Underground Lines
1	Three inverters on one transformer connected via underground lines	1	0	3
2	Three inverters on one transformer connected via overhead lines	1	3	0
3	Three inverters on three different transformers, connected via underground lines	3	0	3
4	Three inverters on three different transformers, connected via overhead lines	3	3	0
5	Two inverters connected to two different transformers via underground lines and one inverter connected to a third transformer via overhead lines	3	1	2
6	Two inverters connected to two different transformers via overhead lines and one inverter connected to a third transformer via underground lines	3	2	1
7	Three inverters connected to two different transformers via underground lines	2	0	3
8	Three inverters connected to two different transformers via overhead lines	2	3	0
9	Two inverters connected to one transformer via underground lines and one inverter connected to a second transformer via overhead lines	2	1	2
10	Two inverters connected to one transformer via overhead lines and one inverter connected to a second transformer via underground lines	2	2	1

Additional notes

- **PHIL model features to make the island more difficult to detect:**
  - RLC load continuously variable → better load balancing
  - Real-time display of circuit quality factor, including all physical and modeled circuit elements → better load tuning
  - Real-time display of island breaker P, Q visible to operator → can time island disconnection
- **PHIL setup validated by comparing single-inverter AI tests using hardware and to single-inverter tests using PHIL**

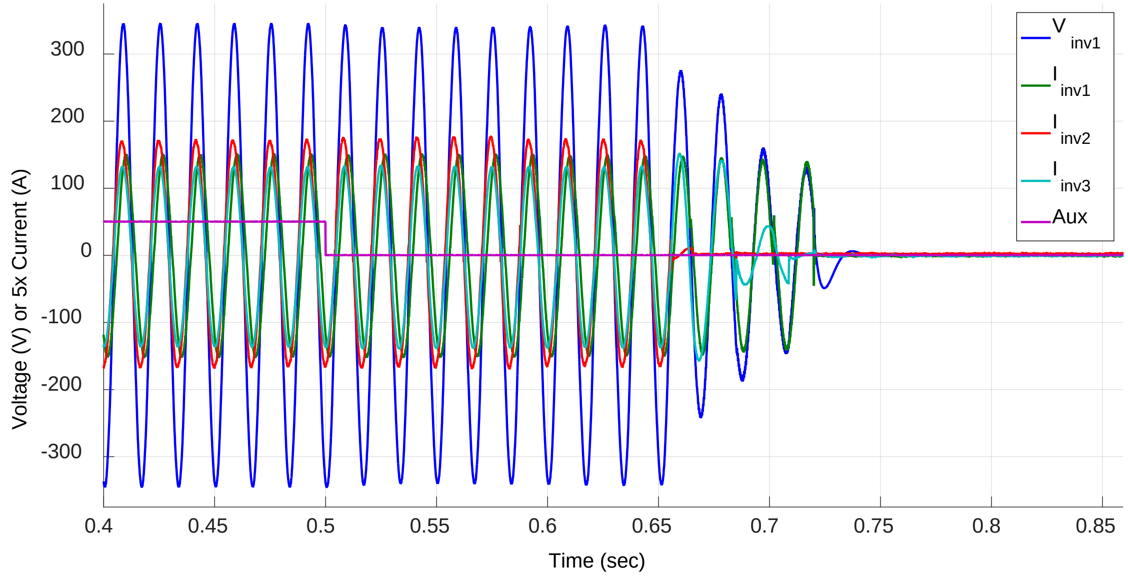
Step 1 Results

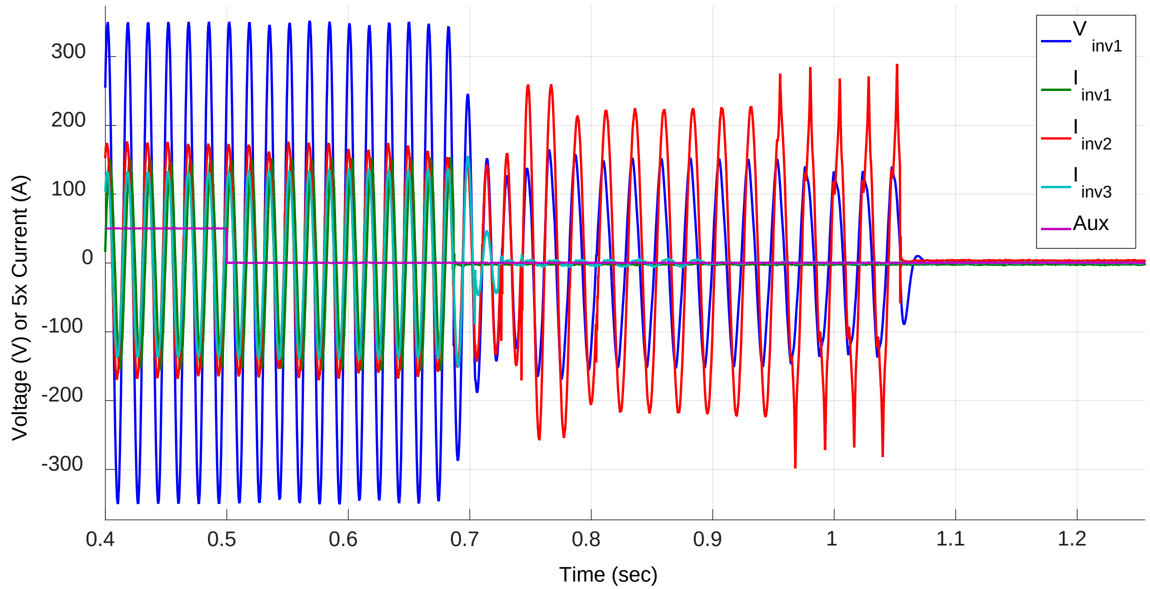
Maximum, mean, and minimum island ROT:



Test Case	Circuit Topology and Impedances		
	# Transformers	# Overhead Lines	# Underground Lines
1	1	0	3
2	1	3	0
3	3	0	3
4	3	3	0
5	3	1	2
6	3	2	1
7	2	0	3
8	2	3	0
9	2	1	2
10	2	2	1

Step 1 Waveforms – Typical and worst-case

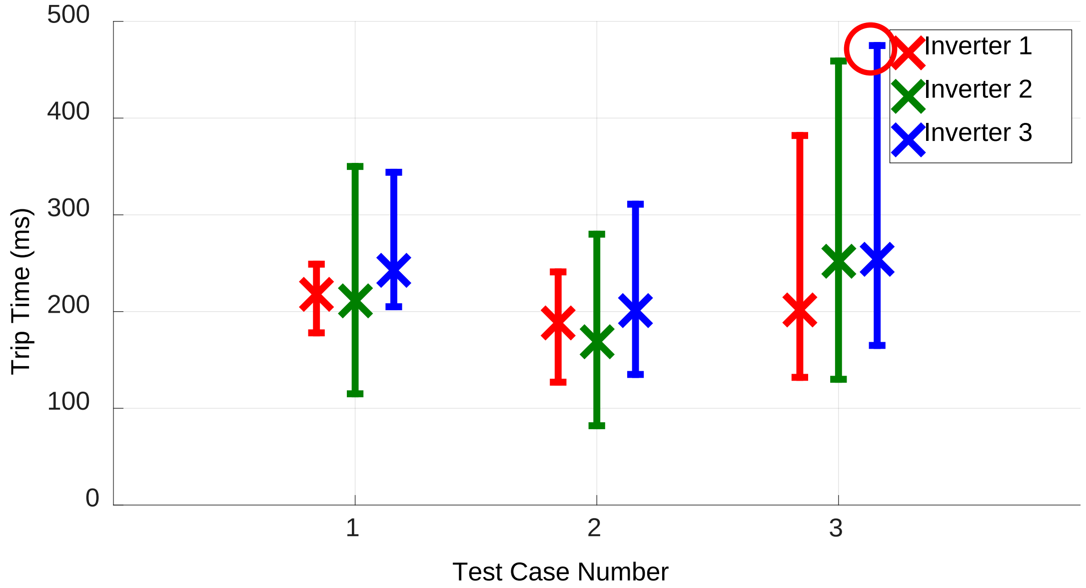




- **Worst-case: circuit 1, 555 ms ROT (shown)**
- **2nd worst: circuit 5**
- **3rd worst: circuit 7**

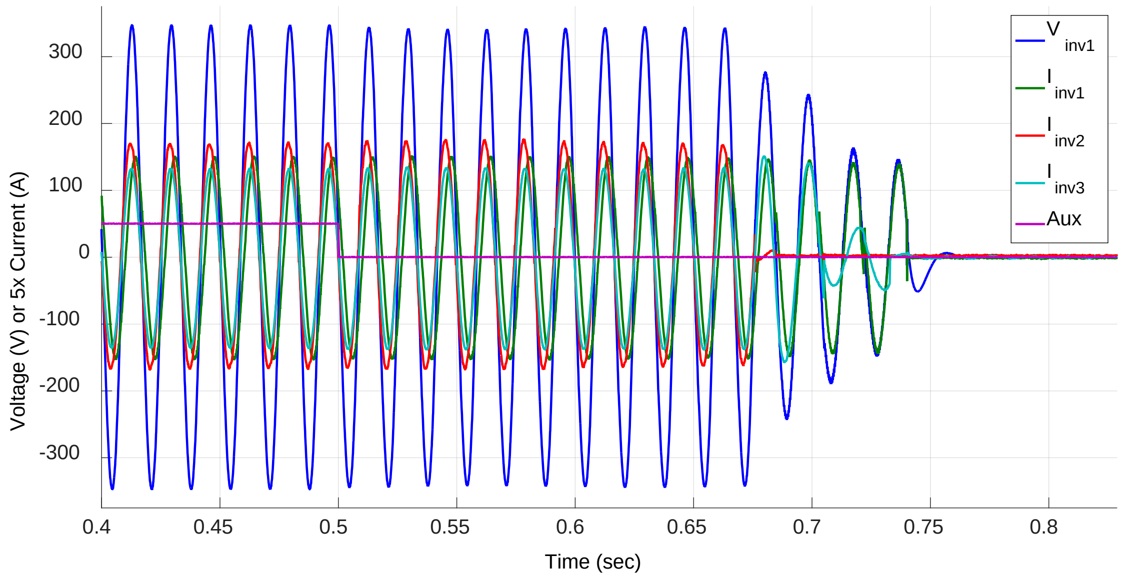
Step 2 Results

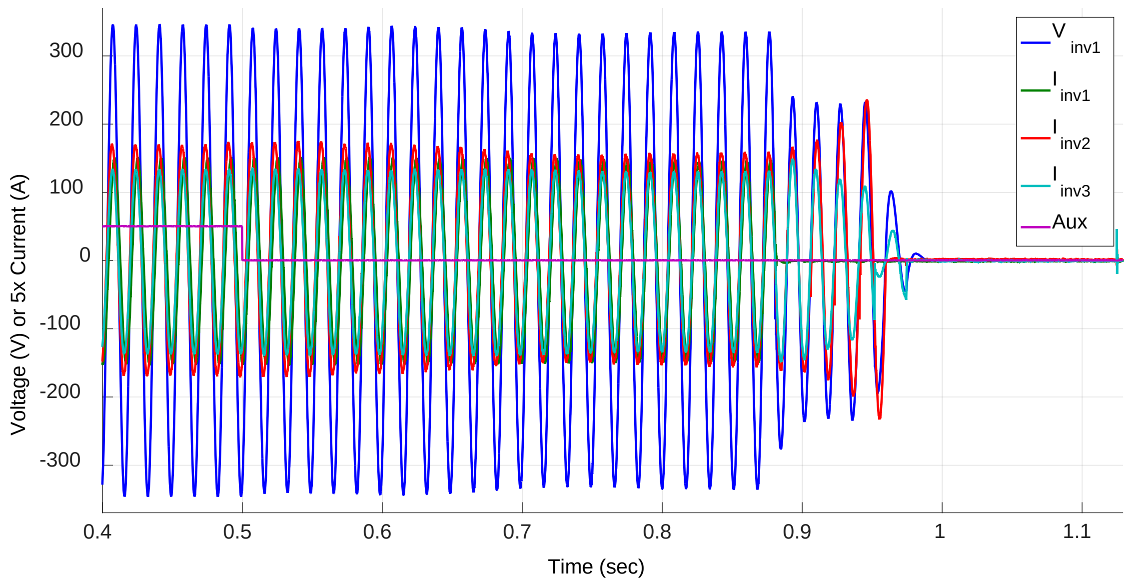
Maximum, mean, and minimum island ROT:



Test Case	Load Location
1	Load Distributed
2	Load Near Breaker
3	Load Far from Breaker

Step 2 Waveforms – Typical and worst-case

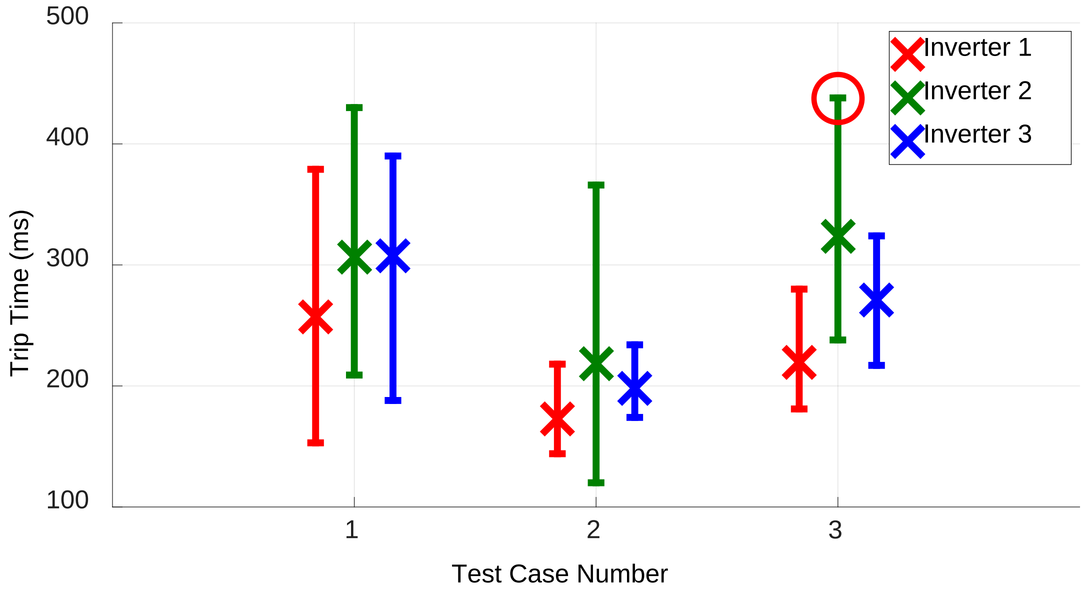




- **Worst-case: load far from breaker**
- **475 ms ROT**

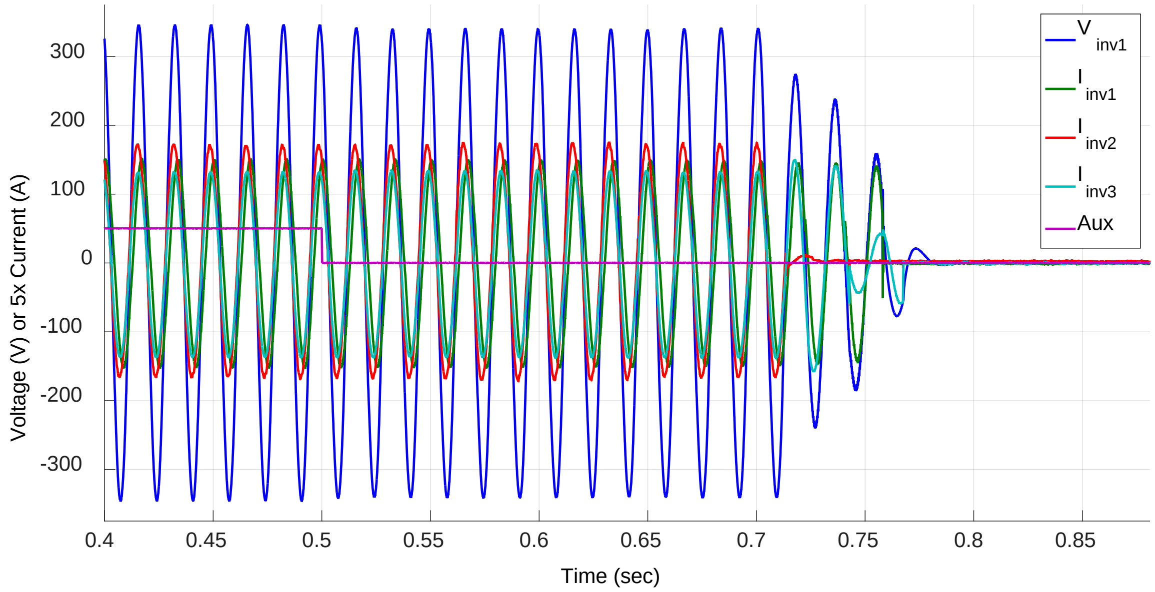
Step 3 Results

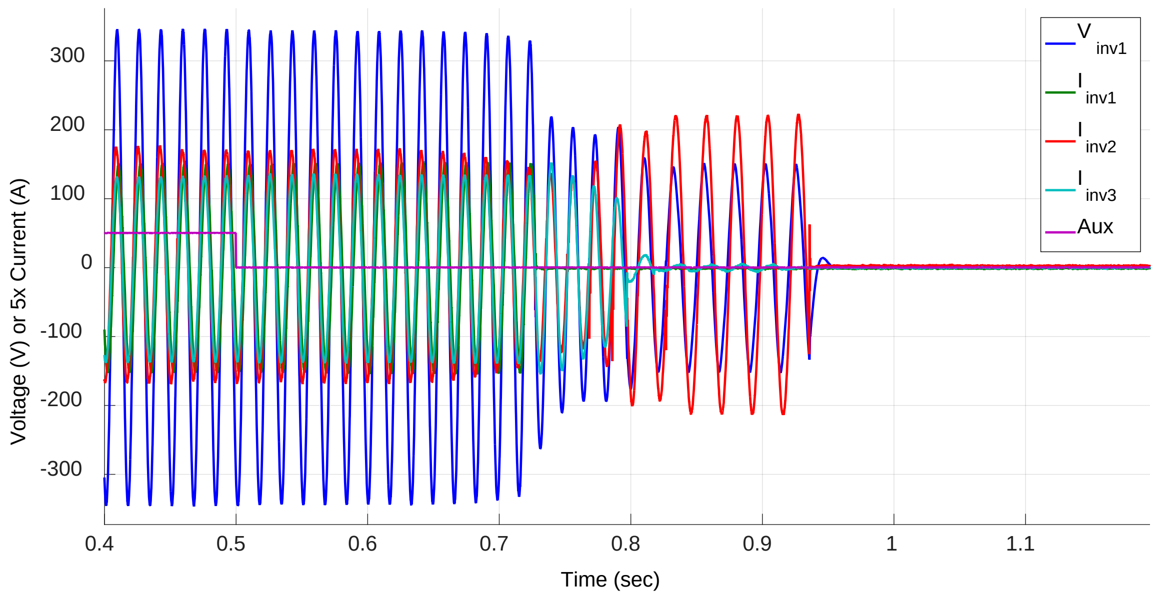
Maximum, mean, and minimum island ROT:



Test Case	Grid Impedance, Z_{SC}
1	Minimum
2	Median
3	Maximum

Step 3 Waveforms – Typical and worst-case

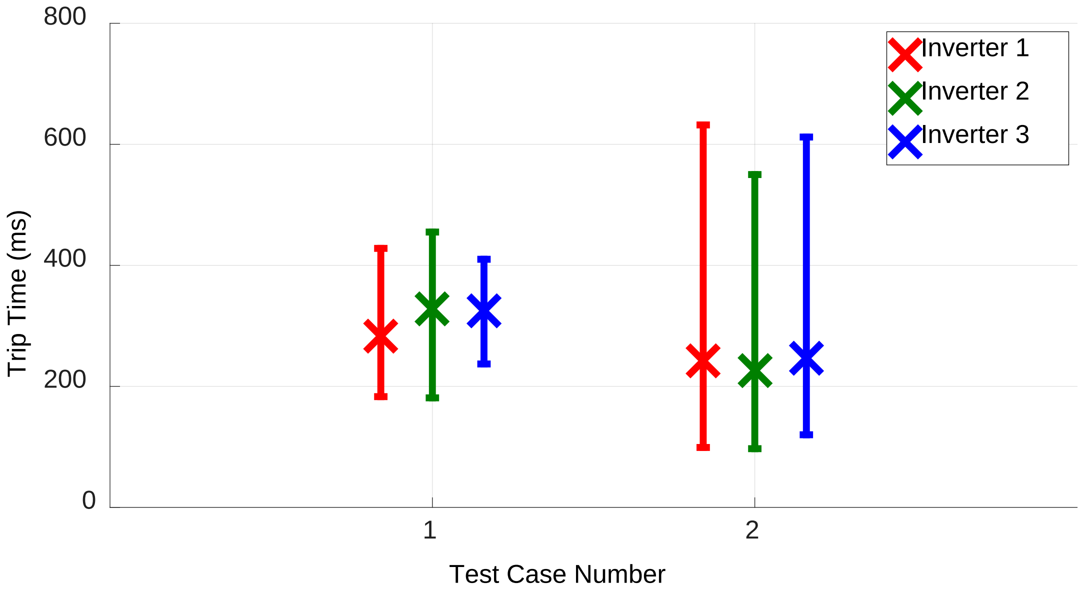




- **Worst-case: maximum Z_{SC}**
- **438 ms ROT**

Addition tests: Island timing

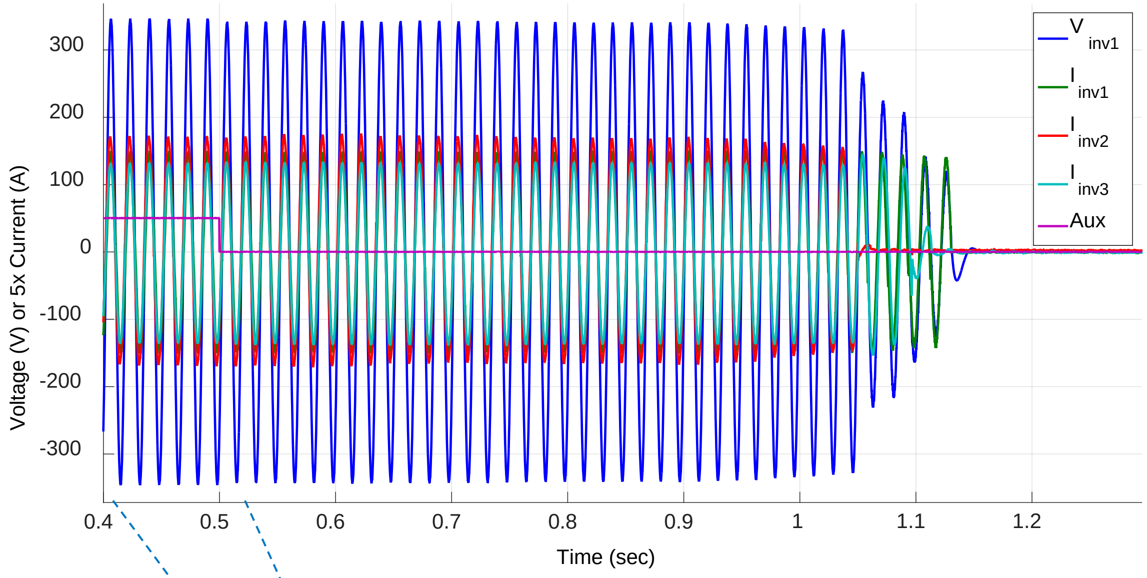
- Inverter 1 shifts output phase angle slightly to detect islands
- Causes periodic variations in Q, P
- Tests above were timed to start near zero-crossing of P and Q flowing through island breaker
- Additional 10 AI tests run to investigate effects of *randomized* island timing

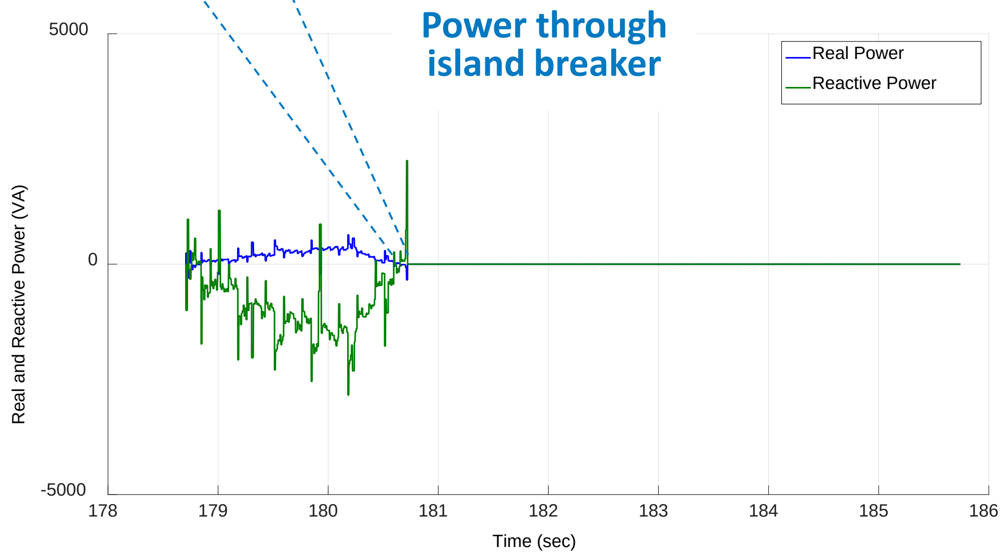


Test Case	Island disconnection timing
1	Timed Disconnection
2	Random Disconnection Time

- Result: Generally, randomized timing led to shorter ROT, but one randomized test had longer ROT. (See next slide)

Worst-case overall test

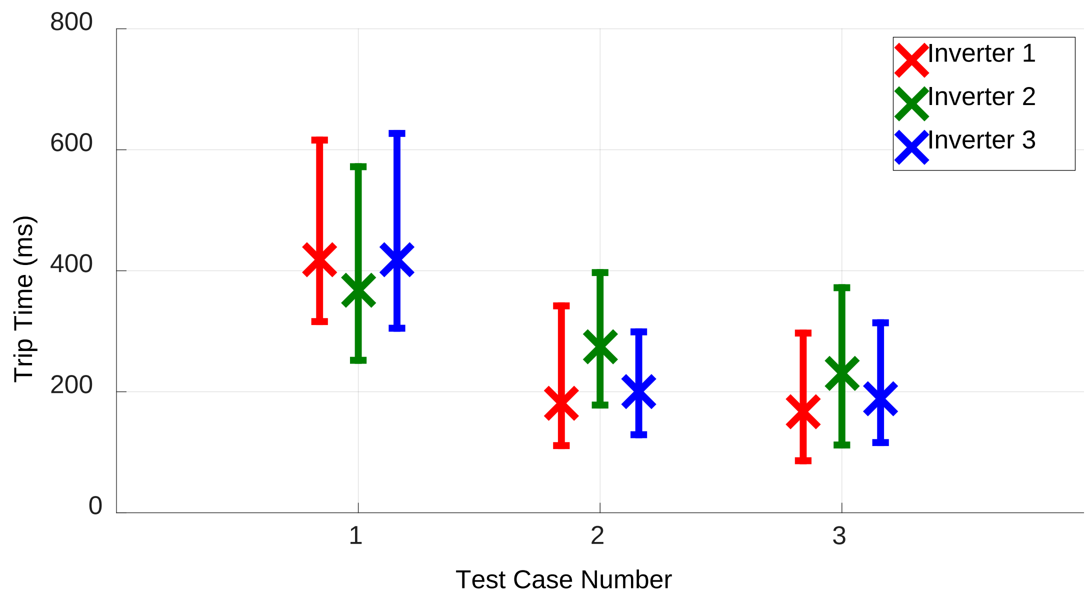




- **632 ms ROT**
- **By chance, the randomized disconnection occurred at the zero-crossing of P and Q flowing through the breaker**
  - So this test is effectively a timed-disconnection test
- **→ Increased confidence that Steps 1-4 capture worst-case island durations**

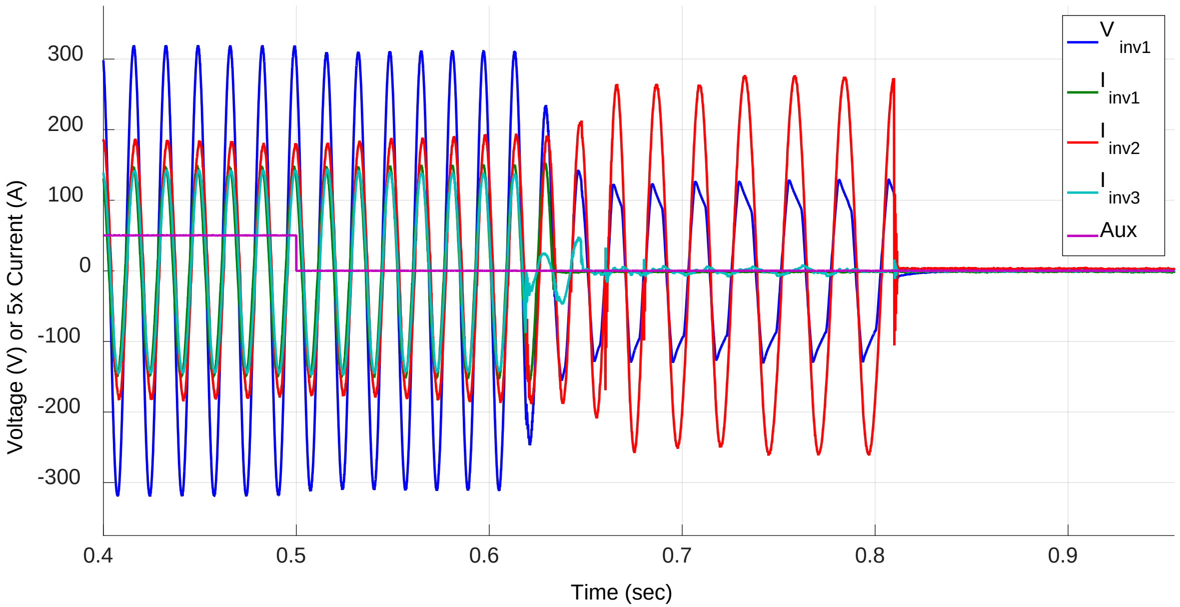
Addition tests: RL loads

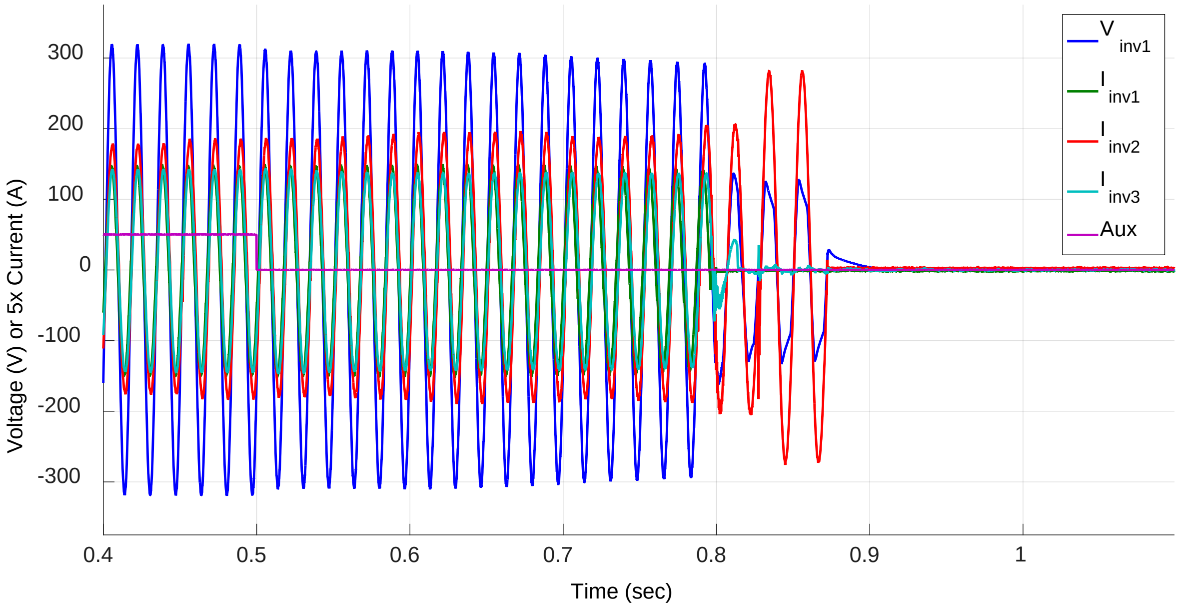
- **RL loads are more typical than RLC loads**
- **10 additional AI tests:**
  - o 5 tests with tuned RL load
  - o 5 tests with 10% detuned RL load
- **All used worst-case settings from Step 4**



Test Case	Test Settings
1	Tuned RLC (baseline)
2	Tuned RL Load
3	De-Tuned RL Load

RL Load Waveforms – Typical and worst-case





- **Worst-case: Tuned RL load**
- **397 ms ROT**