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Reliability of Emerging Bonded Interface Materials for Large-Area Attachments

Paul Paret, *Member, IEEE*, Douglas DeVoto, *Member, IEEE*, and Sreekant Narumanchi, *Member, IEEE*

Abstract—Conventional thermal interface materials (TIMs) such as greases, gels, and phase change materials pose bottlenecks to heat removal and have long caused reliability issues in automotive power electronics packages. Bonded interface materials (BIMs) with superior thermal performance have the potential to be a replacement to conventional TIMs. However, due to coefficient of thermal expansion mismatches between different components in a package and resultant thermomechanical stresses, fractures or delamination could occur, posing serious reliability concerns. These defects manifest themselves in increased thermal resistance in the package. In this paper, results for reliability evaluation of emerging bonded interface materials for large-area attachments in power electronics packaging are reported. Thermoplastic (polyamide) adhesive, with embedded near-vertical aligned carbon fibers, sintered silver, and conventional lead solder ($\text{Sn}_{63}\text{Pb}_{37}$) materials were bonded between 50.8 mm \times 50.8 mm cross-sectional footprint silicon nitride substrates and copper base plate samples, and were subjected to accelerated thermal cycling till failure or 2,500 cycles. Damage in the bonded interface materials was monitored every 100 cycles by scanning acoustic microscopy. Thermoplastic with embedded carbon fibers performed the best with no defects, whereas sintered silver and lead solder failed at 2,300 and 1,400 thermal cycles, respectively. Besides thermal cycling, additional lead solder samples were subjected to thermal shock and thermal cycling with extended dwell periods. A finite element method (FEM)-based model was developed to simulate the behavior of lead solder under thermomechanical loading. Strain energy density per cycle results were calculated from the FEM simulations. A predictive lifetime model was formulated for lead solder by correlating strain energy density results extracted from modeling with cycles-to-failure obtained from experimental accelerated tests. A power law based approach was used to formulate the predictive lifetime model.

Index Terms—bonded interface, cycles-to-failure, FEM modeling, lead solder, predictive lifetime, sintered silver, thermoplastic.

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I. INTRODUCTION

IN a power electronics module, a significant amount of heat is generated by the semiconductor device during its operation that needs to be removed to keep temperatures within limits. However, due to the asperities on the component surfaces in contact to each other, the air gaps that are formed between the surfaces [1, 2] can cause a large resistance to heat transfer, which in turn results in large increases in temperatures in the package. Bonded interface materials (BIMs) ensure an efficient path for heat transfer at the interfaces [3] by closing the air gaps. Hence, the semiconductor device is typically attached by a BIM such as solder to a metalized substrate. The substrate is composed of a ceramic bounded by copper layers on either side and provides electrical isolation. This substrate is then mounted onto a base plate or directly to a heat exchanger, typically made of copper or aluminum, via another large-area BIM. A cross-section of a typical power electronics package is shown in Fig. 1.

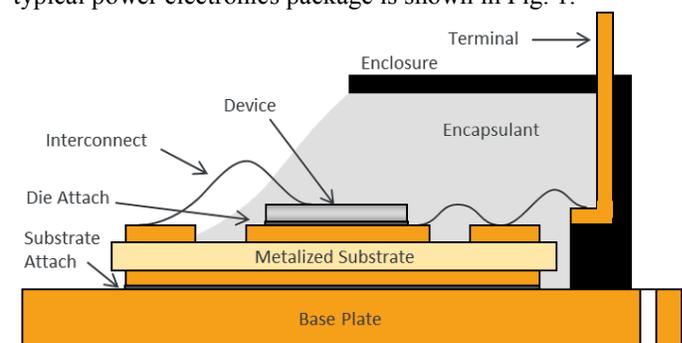


Fig. 1. A traditional power electronics package.

A power electronics package is subjected to significant temperature fluctuations in its operational environment. Because the different layers in a package are made up of different materials, a coefficient of thermal expansion (CTE) mismatch occurs between the adjacent layers. BIMs have significant thermomechanical fatigue induced in them resulting in crack initiation and propagation. Failure of BIMs due to thermomechanical fatigue in its operational environment is a major concern in the automotive industry. A reliable BIM layer is a critical enabler for low cost, lightweight, and high-performance power electronics packages. Lead solders had predominantly been used in the electronics packaging industry; however, the Restriction of Hazardous Substances Directive [4] in Europe mandated lead-

free attachments. The industry turned its attention to various Sn, Ag, and Cu (SAC) compositions as a suitable lead-free alternative, with Innolot ($\text{SnAg}_{3.8}\text{Cu}_{0.7}\text{Bi}_{3.0}\text{Sb}_{1.4}\text{Ni}_{0.2}$) proving to be a promising solution [5–6]. Because the melting point of SAC solders is higher than lead solders, it needs to be subjected to a higher reflow temperature during synthesis, resulting in increased costs. Also, performance and reliability under temperature cycling continue to be a concern with lead-free solders. To provide greater thermomechanical reliability under temperature cycling and to allow for higher temperature applications such as wide-band gap devices-based packaging, sintered silver has also emerged as a promising bonding solution in power electronics packages [7–8]. However, to reduce synthesis temperatures to below 300°C , up to 40 MPa of pressure must be applied to the package, causing a higher complexity in the production process and more stringent flatness specifications for the substrates. Hence, alternative bonding techniques are being developed to increase the thermomechanical reliability of the interface through the use of newer materials, such as thermoplastic with embedded micrometer-sized carbon fibers, nanospring-based materials, graphite solder, and carbon-nanotube-based BIMs. Little information is available on the thermal performance and reliability of large-area attaches based on the more recently developed thermoplastic materials and sintered silver.

Because BIMs are promising [9–12], work at the National Renewable Energy Laboratory (NREL) has focused on assessing their thermal performance and reliability on a large-area attachment. Conclusions on thermal performance and reliability from the present effort are intended to directly assist incorporation of these materials into automotive power electronics designs. This paper focuses on the reliability aspects of novel BIMs such as thermoplastic (polyamide) adhesive with embedded near-vertical-aligned carbon fibers (8- to 10- μm diameter), sintered silver based on micrometer-sized Ag particles, and $\text{Sn}_{63}\text{Pb}_{37}$ solder as a baseline for reference. We have outlined in detail the sample synthesis, initial characterization, accelerated testing, and experimental conclusions of all three selected BIMs. Modeling efforts were focused solely on lead solder, and the computed strain-energy density per cycle results are reported. A predictive lifetime model was formulated for lead solder by correlating the strain-energy density per cycle results with experimentally obtained cycles-to-failure based on a power law model.

II. SAMPLE SYNTHESIS

The sample assembly consists of a 5-mm-thick Cu base plate attached to a 0.72-mm-thick active metal bonded substrate (0.32-mm-thick silicon nitride (Si_3N_4) with 0.2-mm-thick Cu foil on either side of Si_3N_4 , 50.8 mm \times 50.8 mm cross-sectional area footprint) via the bonding material. Before assembly, the Cu metallization layers in the substrate were plated with 4 μm of electroless Ni-P, 1 μm of Pd, and 0.3 μm of Ag to improve adhesion with the bonding material. The Cu base plate was electroplated with 5 μm of Ag. An assembled sample is shown in Fig. 2. Four samples for each BIM were fabricated for accelerated testing.

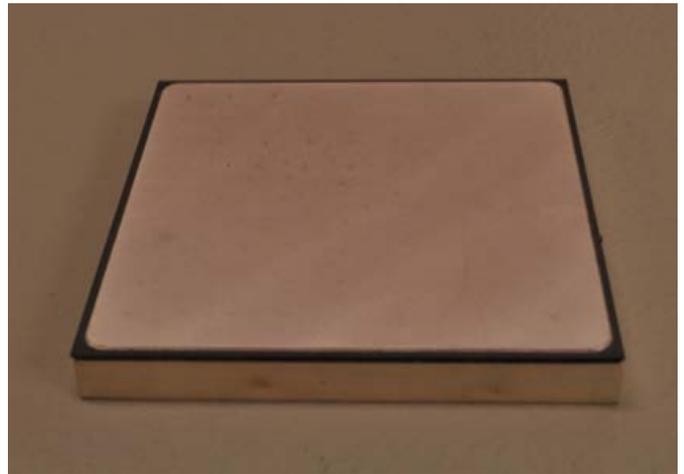


Fig. 2. Representative metalized substrate/base plate assembly.

A tabletop hot press was developed for synthesizing test samples requiring both temperature and pressure bonding parameters. Two hot plates were positioned, one on either side of the sample to be bonded, and were embedded with five 250-W cartridge heaters. Three heaters were inserted in the top hot plate and two in the bottom hot plate. A temperature controller adjusted the power of the heaters based on the temperature measurement by a thermocouple located in the bottom hot plate. The test sample and hot plates were placed between layers of mica and cold plates, and then inserted into an arbor press [13]. Glycol-water (1 to 1 ratio by volume) coolant was circulated within the cold plates to isolate the high bonding temperatures from the hydraulic piston and the fluid. A screw jack was also placed between the hydraulic piston and top cold plate to provide fine adjustment to the applied bonding pressure. The pressure of the hydraulic fluid was electronically monitored to determine the force applied to the sample under bonding.

The HM-2 material, manufactured by *btechcorp*, is a composite structure consisting of 8- to 10- μm -diameter carbon fibers embedded in a polyamide/thermoplastic adhesive at approximately 40 percent fill factor by volume. The HM-2 was placed between the substrate and base plate assembly and subjected to a pressure of 689.5 kPa and a temperature of 190°C . Once the temperature was reached, the assembly was allowed to cool to room temperature while the pressure was maintained.

Bonded interfaces based on sintered silver particles were synthesized by Semikron. Corners of the Si_3N_4 substrate were rounded off to match the 2-mm radius of the Cu layers. The sample assembly was placed in a hot press and raised to its processing temperature, after which pressure was applied.

As a baseline, a $\text{Sn}_{63}\text{Pb}_{37}$ bond was also synthesized between the substrate/base plate assembly. A 127- μm -thick stainless steel stencil with square openings of 9 mm \times 9 mm and 1-mm separation was used to apply solder evenly to the substrate and base plate surfaces. After the solder was applied, the assembled sample was placed in a vacuum solder reflow oven. The reflow profile ensured that flux was removed from the bond and that voiding remained less than 2 percent.

III. INITIAL CHARACTERIZATION

Degradation (e.g., cracks, voids, and delaminations) of the bonded interface can be non-destructively detected by acoustic microscopy. After defect initiation, the thermal and electrical performance of the sample assembly degrades. A C-mode scanning acoustic microscope (C-SAM) emits ultrasound waves with frequencies ranging from 5 MHz to 400 MHz into a sample immersed in water. The strength of the signal reflected back to the microscope's transducer from an interface within a sample depends on the relationship between the acoustic impedances of the two materials forming the interface. A crack, void, or delamination will create a solid-to-air interface, which will cause a strong reflection to be detected by the microscope's transducer. In this project, a transducer with a frequency of 50 MHz, a spot size of 0.073 mm, and a resolution of 0.052 mm was used for scanning. Samples were analyzed for their initial bonding condition and then subsequently tested at every 100 thermal cycles. Images showing the bonded interface within samples before accelerated thermal testing are shown in Fig. 3. The circular bands visible in each sample are artifacts of the C-SAM representing top surface curvatures induced during the synthesis process as two-dimensional images and are not indicators of bond quality. The small white patch seen in the first image indicates a void that was inherently formed in the solder sample during its reflow process. The $\text{Sn}_{63}\text{Pb}_{37}$ solder, *btechcorp* HM-2 thermoplastic, and sintered silver all exhibited uniform initial bonds between the base plate and substrate samples.

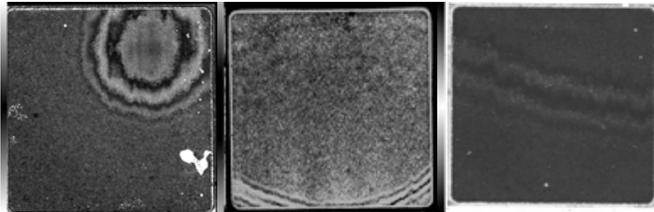


Fig. 3. C-SAM images showing initial bond quality in $\text{Sn}_{63}\text{Pb}_{37}$ solder (left), sintered silver (center), and *btechcorp* HM-2 (right).

In addition to acoustic microscopy, the electrical resistance of the Si_3N_4 insulation layer was measured. In a high potential test, a high voltage is applied to an electronic device's current-carrying components. The quality of the insulation in the device is determined by measuring the presence of a leakage current. Leakage current indicates that dielectric breakdown in the insulation layer has occurred. A dielectric resistance tester was previously constructed based on the high potential testing process to detect when a crack in the Si_3N_4 has developed. A custom fixture contacts the top and bottom sides of a test sample, and a test voltage of 2.0 kV is applied for 20 s, which is sufficient voltage to cause an arc in the air through a defect or crack in the 0.32-mm-thick Si_3N_4 layer. A measurable leakage current from an arc is an indication of any damage occurrence within the Si_3N_4 layer in the sample. The sample successfully passes the test if no current was measured over the analysis period. The results correlated with acoustic microscopy images, indicating that all initial samples

exhibited no defects within the Si_3N_4 layer.

CTE mismatches within the samples cause package deformation and stresses to build up in the Si_3N_4 layer during cool down from the synthesis temperature to room temperature. These stresses can be sufficient to cause crack initiation and propagation within the Si_3N_4 , leading to failure of the layer's electrical insulating properties. As a package cools from a stress-free temperature, the Cu base plate's higher CTE relative to the substrate and silicon die causes it to contract more and induce a bow into the package. Heating will conversely cause the base plate to expand more quickly than the rest of the package and create a bow in the opposite direction.

The high pressure and temperature synthesis requirements for sintered silver did not cause crack initiation within the Si_3N_4 substrate; however, package deformation was evident when samples were at room temperature. A laser profilometer was used to scan the top and bottom surfaces of sintered silver samples for accurate measurements of these deformations. The height variation across the sample was measured to be 166 μm , as shown in Fig. 4. Surface profile measurements were also taken for $\text{Sn}_{63}\text{Pb}_{37}$ solder and thermoplastic samples, but no significant package deformations were found.

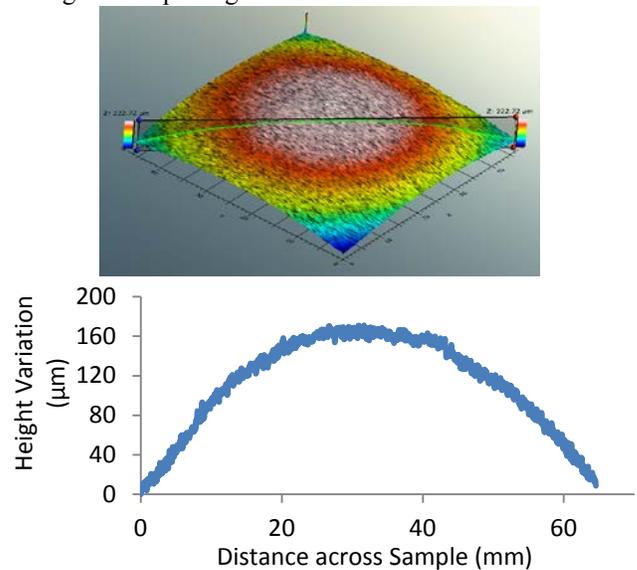


Fig. 4. Surface profile of sintered silver sample at room temperature.

IV. ACCELERATED THERMAL CYCLING

A thermal cycling profile of -40°C to 150°C was chosen based on Joint Electron Devices Engineering Council (JEDEC) standard number 22-A104D [14] to subject the samples to thermomechanical fatigue, eventually causing failure. The ramp rate was set at $5^\circ\text{C}/\text{min}$ and a dwell/soak time of 10 minutes at both temperature extremes was selected. A sufficiently low ramp rate avoids transient thermal gradients within the samples. All four samples of each BIM were subjected to the thermal cycle together in an environmental chamber. During thermal cycling, a container holding the samples shifted back and forth between a hot and a cold chamber. A built-in thermocouple measured the air

temperature inside the container during cycling. The actual temperatures set inside the hot and cold chamber were 165°C and -55°C, respectively, to allow enough time for the BIM sandwiched between the substrate and base plate to reach the desired temperature. Possible failure mechanisms included a substrate delamination, a cohesive fracture within the BIM, or an adhesive fracture between either the metalized substrate and BIM or the base plate and BIM. These different failure mechanisms would ultimately result in crack initiation and propagation. For power electronics packages, it has been generally accepted by the industry that BIMs will be considered to have failed after the induced cracks have propagated to 20 percent of the total interface attachment area [15]. Thermal cycling was performed on the samples until the average value of crack-percentage areas in the samples of each BIM met the failure criterion, or up to 2,500 cycles. C-SAM images of all samples undergoing thermal cycling were taken every 100 cycles to monitor crack initiation and propagation.

In addition to the four samples of each BIM, another set of eight samples of lead solder were fabricated. Four of these underwent a thermal shock test with the ramp rate set at 25°C/min, while other loading parameters stayed the same as the previously selected thermal cycle. Similarly, the remaining four samples were subjected to the original thermal cycling profile with ramp rate of 5°C/min, but this time, the dwell time was extended from 10 minutes to 30 minutes. The three selected loading profiles are listed in Table I. These two additional accelerated tests were conducted only on lead solder samples to understand and quantify the impact of variation in loading parameters on its deformation behavior, and also to build sufficient test cases to formulate a predictive lifetime model.

TABLE I
LOAD PROFILES

Type	Min. temperature (°C)	Max. temperature (°C)	Ramp rate (°C/min)	Dwell (min)
Thermal cycle	-40	150	5	10
Thermal shock	-40	150	25	10
Extended dwell	-40	150	5	30

V. THERMOMECHANICAL MODELING

The objective of thermomechanical modeling was to calculate the accumulated viscoplastic strain energy density per cycle in the solder joint using finite element method (FEM) analysis. Prior research [16] on lead solder characterization showed that the material is viscoplastic in nature. Strain energy density, the main output of interest, at a particular node in the FEM model is the time integral of the product of stresses and incremental strains in all six directions at that node. Modeling results were correlated with cycles-to-failure obtained from experimental accelerated tests to formulate a predictive lifetime model. ANSYS Mechanical was selected for the FEM analysis because of its established

accuracy by other researchers [17-20] in this field. The modeling analysis was conducted only for lead solder due to the lack of accurate stress-strain curves of sintered silver and thermoplastic adhesives at various temperatures and strain rates in the literature, which are required for extracting the constitutive model parameters.

In the lead solder modeling, material properties for the different components in the model, which included a Cu base plate, and Si₃N₄ substrate, were adopted from the literature [19]. The Anand constitutive model [21-22] was used to define the viscoplastic nature of the lead solder, while linear elastic properties were assigned to the base plate and substrate layers. The temperature dependence of elastic properties was also included to the extent possible. The material properties at room temperature of various layers in the test sample model are listed in Table II.

TABLE II
MATERIAL PROPERTIES AT ROOM TEMPERATURE

Material	Elastic Modulus (GPa)	Poisson's ratio	Coefficient of Thermal Expansion (x10 ⁻⁶ /°C)
Cu	113	0.34	16.5
Si ₃ N ₄	300	0.28	2.8
Sn ₆₃ Pb ₃₇	32	0.38	2.5

An ANSYS Parametric Design Language (APDL) code was developed that included model pre-processing, solver, and post-processing phases. A geometric model that matched the sample geometry used in experimental accelerated thermal cycling was created. Quarter symmetry of the sample was utilized in the modeling to save computational space and time, shown in Fig. 5.

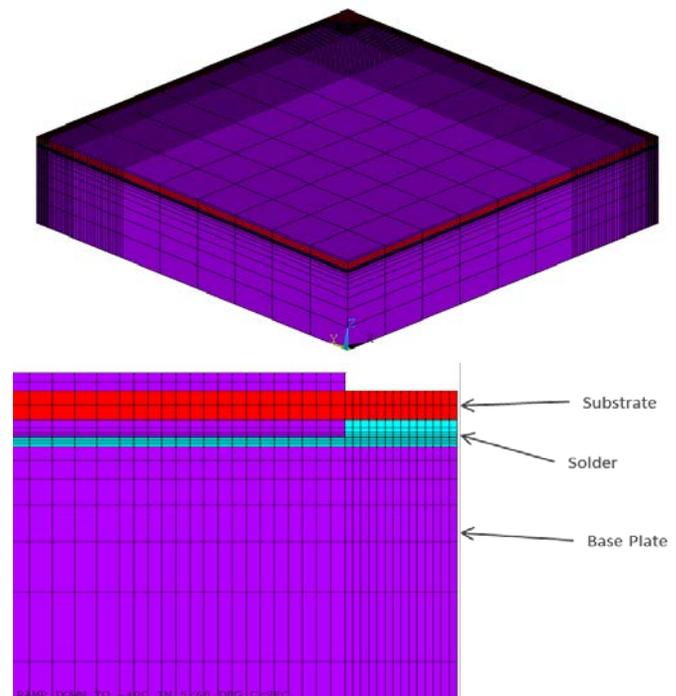


Fig. 5. Meshed model of the sample assembly in ANSYS.

SOLID185 element with a selective reduced integration technique [23] was used in ANSYS for meshing the entire sample geometry. The entire geometry was created in such a way that mapped meshing can be adopted to ensure the use of only hexahedral elements. Also, it gave an easy control over different features of meshing such as element sizing and edge sizing. An increased mesh density was used in the solder layer, particularly at the corner fillet region for accurate results. The element size was 0.4 mm and there were five element layers across the 0.1-mm thickness of the solder joint. The total mesh count was 65,528 elements and 70,461 nodes. The radius of the fillet was set at 2 mm.

Once the model was meshed, a fixed point load was applied to the center node in addition to the symmetry boundary conditions to prevent rigid body motion. Reference temperature was assigned to be 25°C. Three separate simulations - thermal cycling (ramp rate - 5°C/min, dwell time of 10 min), thermal shock (ramp rate - 25°C/min, dwell time of 10 min), and thermal cycling with extended dwell time (ramp rate - 5°C/min, dwell time of 30 min) were run. The load profile started at 25°C followed by a ramp-up to 150°C, and then the cycling loading initiated. Different phases in a load cycle included high temperature-dwell, ramp-down, low temperature-dwell, and ramp-up. Load cycles were repeated until the results converged. Also, a mesh-independence study was conducted to obtain a balance between accuracy and computational time. A simulation of the thermal cycling load profile with close to twice the element count yielded similar results, as shown in Table III. The numerical results presented in the following sections are accurate to within 1%. Also, different mesh layouts with refinements in the corner region were found to have minimal impact on these results.

TABLE III
MESH-INDEPENDENCE STUDY

Case no.	Element count	Percentage variation
1	114,364	-
2	65,528	1 %
3	44,052	1.8 %

VI. RESULTS AND DISCUSSION

A. Experimental Results

An open-source image analysis tool was used to measure the area-wise percentage of cracks/voids with respect to the total interface area in each C-SAM image. Cracks appear as a white patch in the image while a dark region denotes a firm, bonded material. Less than 2% by area of initial voids had already formed in lead solder samples during its synthesis while crack initiation occurred at around 300 cycles for sintered silver samples. No cracks or any defects were seen in thermoplastic BIM samples before thermal cycling. The lead solder samples were subjected to 1,400 thermal cycles, at which point the average value of crack-percentage areas, obtained from the C-SAM images of test samples, spread more than 20 percent of the total interface attachment area and were considered to be failed. Cycling continued for sintered silver and thermoplastic

samples, and it took 2,300 thermal cycles for the sintered silver samples to reach failure. However, no cracks were observed in the thermoplastic samples even after 2,500 cycles, as indicated by its C-SAM images. This result is similar to what is reported in [24] and confirms the significantly superior reliability of thermoplastic as compared to sintered silver and lead solder. Early failure of lead solder can be attributed to the high creep deformation in addition to plasticity in the specified temperature range. Sintered silver has a relatively high melting point as compared to solder and therefore, the amount of creep deformation can be considered as negligible. Also, the lower CTE mismatch of sintered silver with adjacent materials in the sample has played a role in improving its reliability over lead-based solder. As for the samples of thermoplastic with embedded carbon fibers, its anisotropic nature renders the estimation of causes of its excellent reliability - under a complex loading condition like thermal cycling - challenging and tedious. Further tests and detailed images from techniques like Scanning Electron Microscopy or Transmission Electron Microscopy may reveal more information on the thermomechanical behavior of thermoplastic BIM.

The C-SAM images of lead solder, sintered silver, and thermoplastic at certain intervals during the thermal cycling are shown in Figs. 6, 7, and 8, respectively. Only the top-right portions of lead solder and sintered silver C-SAM images are shown for clarity, even though these are not symmetric. The initiation of cracks at the corners of lead solder and sintered silver as indicated by the white regions, and its gradual ingress towards the inner dark regions with increasing number of thermal cycles is evident in these C-SAM images.

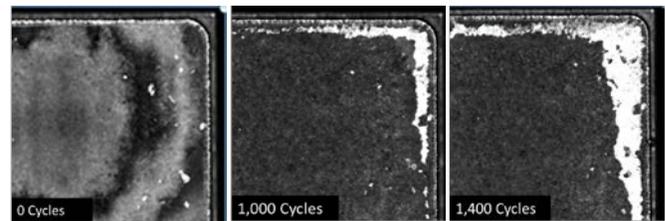


Fig. 6. C-SAM images of the top-right portion of lead solder at 0, 1,000, and 1,400 cycles.

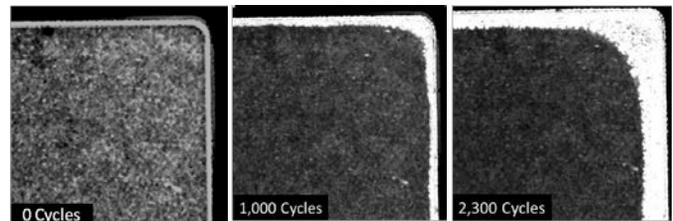


Fig. 7. C-SAM images of the top-right portion of sintered silver at 0, 1,000, and 2,300 cycles.

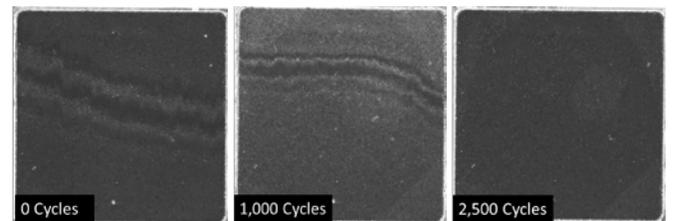


Fig. 8. C-SAM images of thermoplastic at 0, 1,000, and 2,500 cycles.

It is interesting to note that the crack propagation pattern in sintered silver takes more of a convex shape at the corner regions as opposed to the slightly patchy and sharp patterns in lead solder. In order to understand the causes of this difference in detail, a study of the deformation behavior of these materials at a microstructural length scale needs to be conducted. The material synthesis process could also have played a role in this observed behavior.

Fig. 9 summarizes the experimental observations made from C-SAM images of all samples that underwent the JEDEC 22-A104D thermal cycling. It shows the crack-area percentages recorded from C-SAM images plotted against the number of thermal cycles. The blue and violet family of curves represents the sintered silver and lead solder samples respectively. A sample with a crack-area percentage close to the average value in lead solder samples was picked out of the set at 1,000 cycles for cross-sectioning. For the sintered silver samples, there is a wider spread in the crack-area percentages at any given cycle than in the lead solder samples. Two different crack growth rates were observed in these samples, which possibly occurred due to minor variations in their synthesis process at Semikron. One of the samples with a higher crack growth rate, but closer to the average crack-area percentage, was arbitrarily chosen for cross-sectioning. The red line coincident with the X-axis denotes the thermoplastic adhesive samples that do not have any cracks or fractures. The red dashed line denotes 20% cracked area and is defined as the failure point in this project.

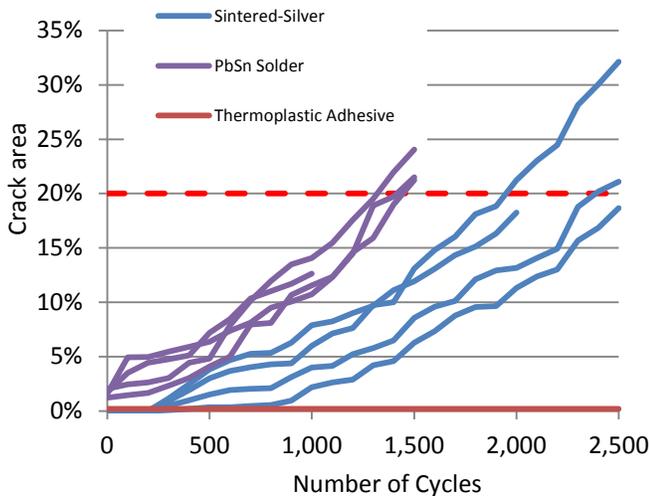


Fig. 9. Crack area versus number of cycles.

The samples picked out from each set for cross-sectioning were cut and polished along a diagonal to obtain a detailed view of the crack. A high-resolution digital microscope was used to take cross-sectional images, and cohesive fracture was observed in both BIMs, as shown in Fig. 10 and Fig. 11. Also, these figures demonstrate a solid contact between the BIM and the adjacent layers on its either side, which is generally considered to be an area prone to delamination.

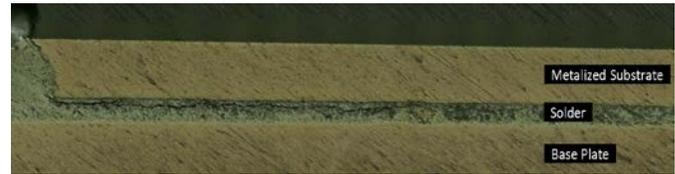


Fig. 10. Cross-sectional image of crack in the solder joint.

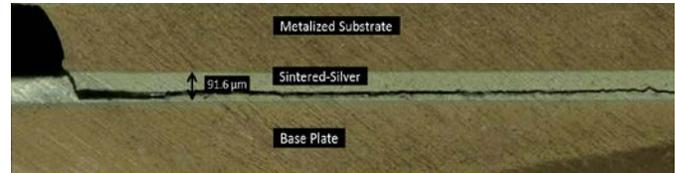


Fig. 11. Cross-sectional image of crack in the sintered silver joint.

C-SAM images were also taken every 100 cycles for the additional lead solder samples that were subjected to thermal shock and extended dwell tests. In both of these cases, the samples failed at 1,200 cycles, which indicates that thermal shock and extended dwell tests have similar effects on varying the deformation rate of lead solder under thermomechanical fatigue.

B. Modeling Results

In the FEM model of lead solder, the maximum value of strain energy density was found to be at the corner regions, specifically at the interface between bottom metallization of the substrate and the solder joint. The location of the maximum strain energy density values matches with the observation of crack initiation in the experimental samples, and is expected because stress concentration is higher at the corner regions. Fig. 12 shows a top view of the strain energy density contour plot on the solder layer, with the location of maximum value highlighted by a red box. To avoid singularity, a volume-averaged strain energy density [16], calculated at the entire corner fillet region was chosen as the output. Fig. 13 is an isometric view of the corner region of the solder joint.

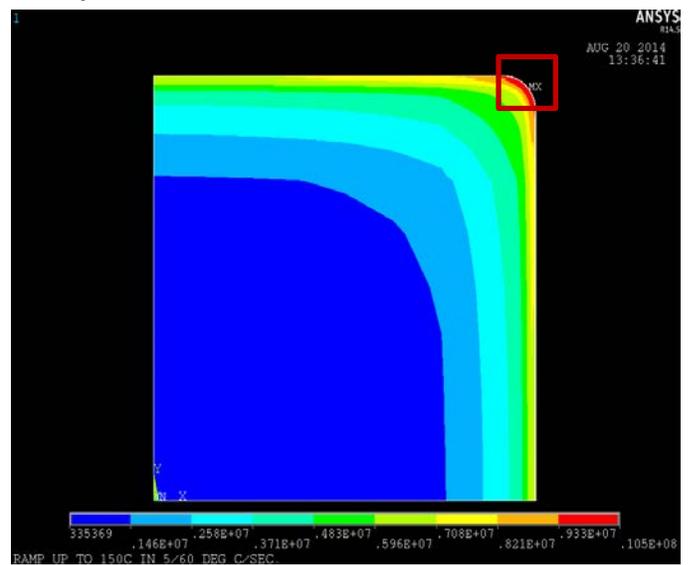


Fig. 12. Top-view of strain energy density contour plot on the lead solder layer.

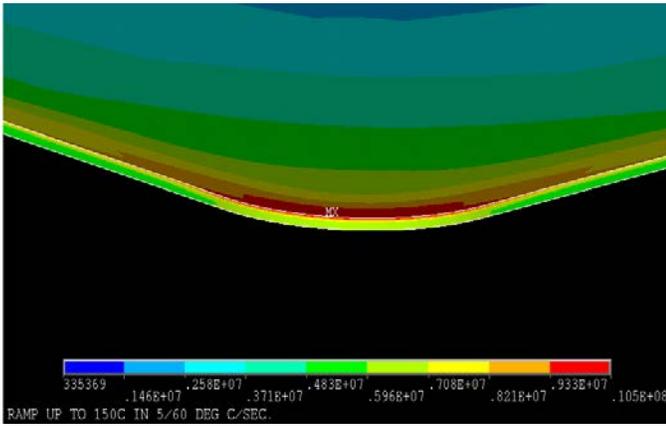


Fig. 13. Isometric view of strain energy density contour plot at the corner region. Maximum values of strain energy density occur at the top interface with the substrate metallization.

Volume-averaged strain energy density at the corner fillet regions for thermal cycling, thermal shock, and extended dwell tests are listed in Table IV.

Load profile	Volume-averaged strain energy density/cycle, ΔW (MPa)
Thermal cycling	1.36
Thermal shock	1.46
Extended dwell	1.51

The modeling results are fairly in agreement with experimentally obtained cycles-to-failure results for lead solder: the lower the strain energy density value, the higher the experimental cycles-to-failure. Comparing the strain energy density values of thermal shock and extended dwell profiles, it can be inferred that increasing the ramp rate to 25°C/min, or the dwell time to 30 minutes in the thermal cycling profile has more or less the same effect on thermomechanical fatigue of lead solder. Although the strain energy density output from the extended dwell profile is higher than that of the thermal shock, it is not enough higher to confirm a stronger degradation-inducing effect, as indicated by the similar cycles-to-failure results of the samples that were subjected to these profiles.

Taking the thermal cycling profile as a reference and analyzing the stresses and strains in all six directions, shear deformations, particularly in the out-of-plane directions, are found to contribute the most towards the strain energy density output. Shear stresses and inelastic shear strains at a node in the corner fillet region were extracted in one of the out-of-plane directions and were plotted against each other to obtain a hysteresis loop. Stress-strain plots help to understand the impact of each loading condition within a thermal cycle on the thermomechanical fatigue induced within the solder joint.

It is clear from Fig. 14 that maximum values of volume-averaged strain energy density per cycle occur during the ramping portions of the thermal cycle, due to the wider variations in stress and strain values, than during dwell times. For solders, it has been reported in the literature that creep

is time- and temperature-dependent plays a dominant role in the deformation process once the homologous temperature is above 0.5, which is the case even at -40°C. With the ramp rate at 5°C/min, the solder joint spends 38 minutes in each ramp load, which is considerably higher than the 10-minute dwell loads. Hence, it can be concluded that ramp loads cause a higher strain energy formation than dwell loads in a thermal cycle. This is confirmed by the analysis of hysteresis loop in Fig. 14, explained in the clockwise direction. At high dwell, strain increases to its maximum value with creep strain presumably being the dominant factor while a slight stress relaxation occurs. As the temperature cools down to -40°C during the ramp-down phase, stress begins to build up in the opposite direction combined with a reduction in the strain. The low-dwell phase contributes the least amount of strain energy density in the entire cycle, as little variation occurs to both stress and strain values. This is because at -40°C, creep deformation is the lowest in solder than at any other phase in the thermal cycle. Finally, during ramp up, stress relaxation occurs as temperature approaches 150°C, whereas strain begins to increase due to temperature-dependent creep effects. The stress values change in direction in accordance with the expansion and contraction of the solder joint under thermal cycling. Also, the magnitude of stresses and strains would vary depending on the location of the node in the corner fillet region but the trend observed in Fig. 14 would remain the same.

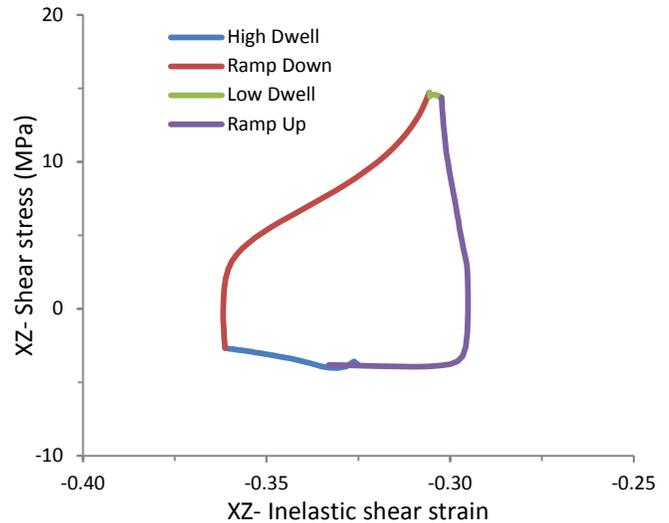


Fig. 14. Shear stress-shear strain hysteresis plot from thermal cycling profile.

Fig. 15 shows the variation of shear stresses and strains of all three load profiles in one graph. The thermal cycling profile is taken as a reference for ease of explanation. Comparing the hysteresis plot of thermal shock with thermal cycle, it can be seen that the loop has elongated a bit in the vertical axis, and shrunk in the horizontal direction. This change in shape of the loop is due to the higher ramp rate leading to a rapid variation of temperature, thereby inducing higher amounts of stresses in the solder joint. Strain values are understandably lower because the faster ramp rates do not allow for creep deformation to develop. As for extended

dwel, the maximum strain value has increased as compared to thermal cycling due to the extended dwell time allowing more creep to occur.

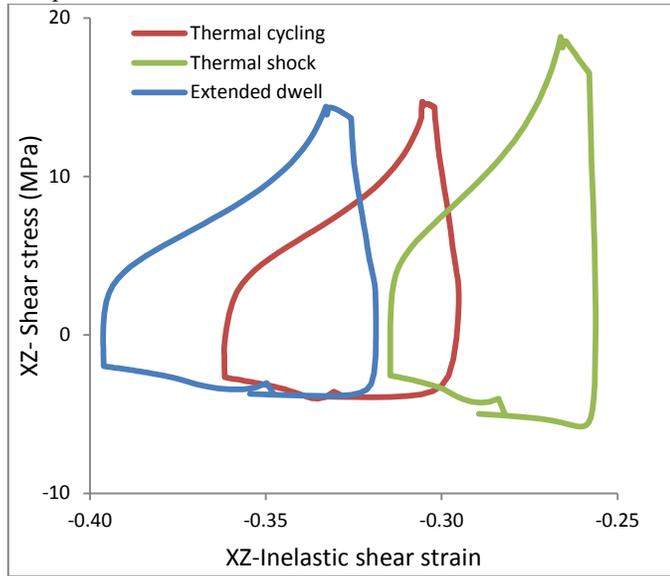


Fig. 15. Shear stress-shear strain hysteresis plots from all profiles.

C. Predictive Lifetime Model

Predictive lifetime models have been formulated in the past for eutectic lead solder in different types of packages such as ball grid array and chip scale packages. To the authors' knowledge, no models have been published for flat, large-area lead solder joints in the literature to date. For the same solder material and for a given failure mechanism, which is thermomechanical fatigue in this study, the geometry of the package has an impact on the predictive lifetime model. Furthermore, it can depend on the type of constitutive model, accuracy of FEM modeling results, and the failure criterion. In this study, based on recommendations from the automotive industry, the number of thermal cycles it took for the induced cracks in the joint to propagate to 20% of the total attachment area was chosen as the failure criterion. Table V lists the required results, obtained from experimental study and modeling analysis, to develop the predictive lifetime model. The volume-averaged strain energy density per cycle values are same as the ones in Table IV and the cycles-to-failure results were obtained for each of the loading profile based on the failure criterion mentioned above. A predictive lifetime model was formulated by correlating the experimentally obtained cycles-to-failure with the volume-averaged strain energy density per cycle results calculated from modeling.

TABLE V
EXPERIMENTAL AND MODELING RESULTS

Load Profile	Volume-averaged strain energy density/cycle, ΔW (MPa)	Cycles-to-failure (N_f)
Thermal cycling	1.36	1,400
Thermal shock	1.46	1,200
Extended dwell	1.51	1,200

In Fig. 16, the blue dotted line shows the results given in Table V. Taking a similar approach as in lifetime estimation models [25-32] of other electronics packages, the correlation between the cycles-to-failure and the modeling results is established using a power-law model, which serves as the predictive lifetime model.

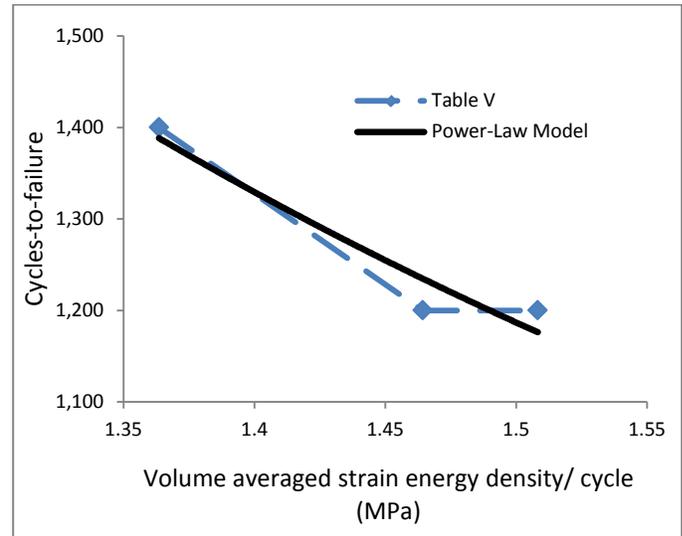


Fig. 16. Cycles-to-failure versus strain energy density plot.

The predictive lifetime model from Fig. 16 is:

$$N_f = 2312.5 (\Delta W)^{-1.645} \quad (1)$$

The model, shown in Eq. 1, has a similar format to that of other energy fatigue models [30], but the constants differ in magnitude due to a few different variations such as the constitutive model used, geometry of the package, and the failure criterion. Volume-averaged strain energy density per cycle was used as it captures both stress and strain information, and has been proven to be an accurate representation of the deformation behavior of solder joints [30]. Also, crack initiation and crack propagation were not considered separately in developing the model. The predictive lifetime model developed in this study encompasses variations in ramp rate and dwell time in a thermal cyclic load and can be used to estimate the cycles-to-failure of a flat lead solder ($\text{Sn}_{63}\text{Pb}_{37}$) interface attachment. Lack of sufficient test samples for accelerated testing meant a validation study could not be conducted to measure the accuracy of the proposed lifetime model with respect to parameter variations.

D. Effects of Variation in Geometry

A parametric study of the solder joint response to thermal cycling load profile, by varying the fillet radius and joint thickness separately while keeping all other dimensions the same, was also conducted. The results of the study are listed in Table VI and Table VII. In these tables, the volume-averaged strain energy density/cycle values were computed from modeling and the predicted cycles-to-failure results were obtained from Eq. 1.

TABLE VI
VARIATION OF FILLET RADIUS

Radius of the fillet at the corner (mm)	Volume-averaged strain energy density/cycle, ΔW (MPa)	Predicted cycles-to-failure
1.5	1.47	1,225
2	1.36	1,400
3	1.19	1,740

A fillet at the sharp corner region of the solder joint eases the effect of high stress concentration, thereby reducing the strain energy density. Consequently, the cycles-to-failure will increase. Therefore, higher the fillet radius, larger will be the cycles-to-failure. However, it is not recommended to design solder joints with very high fillet radius as it decreases the overall solder attach area. This would have a negative impact on the entire power module as heat dissipation gets constrained at the solder joint.

TABLE VII
VARIATION OF SOLDER JOINT THICKNESS

Solder Joint Thickness (mm)	Volume-averaged strain energy density/cycle, ΔW (MPa)	Predicted cycles-to-failure
0.05	2.65	465
0.1	1.36	1,400
0.15	0.93	2,600

From Table VII, it is evident that increasing the solder joint thickness lowers the strain energy density. As the thickness increases, the solder joint is better able to accommodate the CTE and stiffness mismatch that exists within the power module, and thus offer a higher resistance to fatigue. Nevertheless, it is preferable to have the joint layer as thin as possible because a thick solder joint offers higher resistance to heat dissipation. A balanced approach between thermal and thermomechanical perspectives needs to be adopted in choosing the thickness of the solder joint.

VII. CONCLUSIONS

A reliability evaluation study of emerging BIMs such as thermoplastic with embedded carbon fibers and sintered silver as compared to eutectic lead solder on a large-area attachment was conducted. Cross-sectional footprint samples of each BIM (50.8 mm \times 50.8 mm) were made and subjected to accelerated thermal cycling. Test results proved that no defects occurred in thermoplastic even after 2,500 cycles whereas sintered silver and lead solder samples failed at 2,300 and 1,400 cycles, respectively. Thermoplastic samples performed remarkably well considering that no signs of any failure were observed even after 2,500 cycles. However, the maximum operating temperature for thermoplastic is limited to around 170°C, which prevents it from being used in high-temperature packages. High-temperature packages, which utilize the superior conversion efficiency of wide-bandgap devices such as silicon carbide and gallium nitride, are currently being investigated by industries to bring down the overall cost of power electronics in electric traction drives. Materials that can

withstand the harsher environments of higher temperatures need to be developed and their reliability evaluated and demonstrated. Our future work will focus on improving the reliability of sintered silver by optimizing its processing conditions through a rigorous analysis of different bond pad designs to minimize the induced failure mechanisms.

The reliability of lead solder samples under varying conditions of thermal test profiles was studied. It was found that increasing the ramp rate from 5°C/min to 25°C/min or extending the dwell time from 10 minutes to 30 minutes for a given thermal cycle has more damaging but similar effects on the failure of lead solder. A power law-based predictive lifetime model was formulated for lead solder. Volume-averaged strain energy density per cycle results obtained from non-linear FEM modeling were correlated with experimentally obtained cycles-to-failure to develop the predictive lifetime model, which can potentially be a design tool for practicing engineers. Future steps in modeling will include, but not be limited to, developing crack initiation and propagation models based on fracture mechanics, study of dislocation dynamics that cause fracture, and incorporating geometric variations of BIMs, such as microstructural evolution during thermal cycling, into the FEM models.

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REFERENCES

- [1] M. M. Yovanovich and E. E. Marotta, "Thermal spreading and contact resistances," in *Heat Transfer Handbook*, A. Bejan and A.D. Kraus, Eds. Hoboken, New Jersey: Wiley, 2003, pp. 261–395.
- [2] R. Prasher, "Thermal interface materials: Historical perspective, status and future directions," *Proc. of the IEEE*, vol. 94, no. 8, pp. 1571–1586, Aug. 2006.
- [3] D. DeVoto, P. Paret, S. Narumanchi, and M. Mihalic, "Reliability of bonded interfaces for automotive power electronics," in *ASME InterPACK*, Burlingame, CA, 2013.
- [4] Official Journal of the European Union, 2003, "Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment." February 13, 2003.

- [5] S. Narumanchi, M. Mihalic, K. Kelly, and G. Eesley, "Thermal Interface Materials for Power Electronics Applications," NREL, Golden, CO, Tech. Rep. CP-540-44056, 2008.
- [6] R. Dudek, W. Faust, R. Ratchev, M. Roellig, H. Albrecht, and B. Michael, "Thermal test and field cycling induced degradation and its FE-based prediction for different SAC solders," in *IEEE ITherm*, Orlando, FL, 2008, pp. 668-675.
- [7] E. Schulze, C. Mertens, A. Lindemann, "Low temperature joining technique - a solution for automotive power electronics," in *Pow. Conv. Intell. Mot.*, Nuremberg, Germany, 2009.
- [8] E. Schulze, C. Mertens, A. Lindemann, "Pure low temperature joining technique power module for automotive production needs," in *Int. Conf. Integr. Pow. Electron. Sys.*, Nuremberg, Germany, 2010.
- [9] R. Chuang, C. Lee, "Silver-indium joints produced at low temperature for high temperature devices," *IEEE Trans. Compon. and Packag. Technol.*, vol. 25, no. 3, pp. 453-458, 2002.
- [10] R. Wu, P. McCluskey, "Reliability of indium solder for cold temperature packaging," in *ASME InterPACK*, Vancouver, BC, Canada, Jul. 2007.
- [11] T. Lei, J. Calatta, G-Q. Lu, X. Chen, S. Luo, "Low temperature sintering of nanoscale silver paste for attaching large-area (>100 mm²) chips," *IEEE Trans. Compon. Packag. Technol.*, vol. 33, no. 1, pp. 98-104, Mar. 2010.
- [12] D. DeVoto, P. Paret, M. Mihalic, S. Narumanchi, Avram Bar-Cohen, Kaiser Matin, "Thermal Performance and Reliability Characterization of Bonded Interface Materials (BIMs)," in *IEEE ITherm*, Orlando, FL, 2014.
- [13] Enerpac, "A, IP-series, arbor, c-clamp and bench frame presses." Available: <http://www.enerpac.com/en-us/industrial-tools-imperial/hydraulic-presses/a-ip-series-arbor-c-clamp-and-bench-frame-presses>.
- [14] JEDEC Standard Temperature Cycling, JESD22-A104D, March 2009.
- [15] Private communications.
- [16] P. Adams, "Thermal fatigue of solder joints in micro-electronic devices," M.S. thesis, Dept. Mech. Eng., MIT, Cambridge, MA, 1986.
- [17] R. Darveaux, "Effect of simulation methodology on solder joint crack growth correlation," *J. of Electron Packag.*, vol. 124, pp. 147-154, Jul. 2002.
- [18] B. Zahn, "Finite element based solder joint fatigue life predictions for a same die stacked chip scale ball grid array package," in *Int. Electron. Manuf. Technol. Symposium, 27th Annual IEEE/SEMI*, 2002, pp. 274-284.
- [19] G. Wang, Z. Cheng, K. Becker, J. Wilde, "Applying Anand model to represent the viscoplastic deformation behavior of solder alloys," *J. Electron Packag.*, vol. 123, pp. 247-253, Sep. 2001.
- [20] A. Yeo, C. Lee, J. Pang, "Flip chip solder joint reliability analysis using viscoplastic and elastic-plastic-creep constitutive models" *IEEE Trans. Compon. Packag. Tech.*, vol. 29, no. 2, pp. 355-363, Jun. 2006.
- [21] L. Anand, "Constitutive equations for hot working of metals," *Int. J. Plasticity*, vol. 29, no.2, pp. 213-231, 1985
- [22] S. Brown, K. Kim, and L. Anand, "An internal variable constitutive model for hot working of metals," *Int. J. Plasticity*, vol. 5, no. 2, pp. 95-130, 1989.
- [23] ANSYS Help, Release 15.0, ANSYS Inc., Canonsburg, PA, 2014.
- [24] Y. Yamada, "Power semiconductor module using a bonding film with anisotropic thermal conduction," *Microelectronics Reliability*, vol. 52, pp. 2443-2446, 2012.
- [25] X. Fan, M. Pei, and P. Bhatti, "Effect of finite element modeling techniques on solder joint fatigue life prediction of flip-chip BGA packages," in *IEEE Electron. Compon. Technol. Conf.*, San Diego, CA, 2006, pp. 972-980.
- [26] A. Schubert, R. Dudek, E. Auerswald, A. Gollhardt, B. Michel, and H. Reichl, "Fatigue life models for SnAgCu and SnPb solder joints evaluated by experiments and simulation," in *IEEE Electron. Compon. Technol. Conf.*, New Orleans, LA, 2003, pp. 603-610.
- [27] A. Dasgupta, C. Oyan, D. Barker, and M. Pecht, "Solder creep-fatigue analysis by an energy-partitioning approach," *Trans. of the ASME*, vol. 114, pp. 152-160, June 1992.
- [28] T. Dishongh, C. Basaran, A. Cartwright, Y. Zhao, and H. Liu, "Impact of temperature cycle profile on fatigue life of solder joints," *IEEE Trans. Adv. Packag.*, vol. 25, no. 3, pp. 433-438, Aug 2002.
- [29] X. Fan, G. Raiser, and V. Vasudevan, "Effects of dwell time and ramp rate on lead-free solder joints in FCBGA packages," in *IEEE Electron. Compon. Technol. Conf.*, Lake Buena Vista, FL, 2005, pp. 901-906.
- [30] W. Lee, L. Nguyen, and G. Selvaduray, "Solder joint fatigue models:

review and applicability to chip scale packages," *Microelectronics Reliability*, vol. 40, pp. 231-244, 2000.

- [31] A. Syed, "Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints," in *Proc. 54th Electron. Compon. Technol. Conf.*, 2004, vol. 1, pp. 737-746.
- [32] X. Liu and G-Q Lu, "Effects of solder joint shape and height on thermal fatigue lifetime," *IEEE Trans. Compon. Packag. Technol.*, vol. 26, no. 2, pp.455-464, Jun. 2003
- [33] N. Kawasaki, "Parametric study of thermal and chemical nonequilibrium nozzle flow," M.S. thesis, Dept. Electron. Eng., Osaka Univ., Osaka, Japan, 1993.



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