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A 2.3-MW Medium-Voltage, Three-Level Wind Energy Inverter Applying a Unique Bus Structure and 4.5-kV Si/SiC Hybrid Isolated Power Modules

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***Abstract*—A high-efficiency, 2.3-MW, medium-voltage, three-level inverter utilizing 4.5-kV Si/SiC (silicon carbide) hybrid modules for wind energy applications is discussed. The inverter addresses recent trends in siting the inverter within the base of multimegawatt turbine towers. A simplified split, three-layer laminated bus structure that maintains low parasitic inductances is introduced along with a low-voltage, high-current test method for determining these inductances. Feed-thru bushings, edge fill methods, and other design features of the laminated bus structure provide voltage isolation that is consistent with the 10.4-kV module isolation levels. Inverter efficiency improvement is a result of the (essential) elimination of the reverse recovery charge present in 4.5-kV Si PIN diodes, which can produce a significant reduction in diode turn-off losses as well as insulated-gate bipolar transistor (IGBT) turn-on losses. The hybrid modules are supplied in industry-standard 140 mm x 130 mm and 190 mm x 130 mm packages to demonstrate direct module substitution into existing inverter designs. A focus on laminated bus/capacitor-bank/module subassembly level switching performance is presented.**

Keywords—Wind turbine; wind energy; medium voltage; three-level inverter; silicon carbide; SiC; efficiency; barrier diode; laminated bus; parasitic inductances; logarithmic decrement method

I. INTRODUCTION

Wind turbine electrical architectures have historically been driven by multiple issues including: siting requirements (land use, aesthetics, and audible noise), evolving utility interconnect standards, turbine manufacturing efficiencies, growth in turbine ratings, and an ongoing need to reduce wind-generated cost of energy (COE). These issues are discussed in detail in [1], where the preferred architecture of Fig. 1 is presented. Key reasons for the architecture shown are threefold. First, placing the padmount transformer and converter within the base of the turbine tower is aesthetically appealing, making good use of external land area and eliminating high-frequency audible switching noise that is naturally tonal and violates many siting standards. Second, using a medium-voltage generator and converter minimizes the cross-sectional copper used in the pendant cables. Because these cables are long—80 to 100 meters in length—there is a significant copper cost reduction when moving from low-voltage (690 V AC) to medium-voltage (3.3 kV AC) systems. Third, the replacement of a doubly-fed, partially rated converter system with a fully rated converter system allows for new and future utility interconnect requirements to be met more easily as a result of completely decoupling the generator from the utility during symmetrical and asymmetrical fault conditions [2].

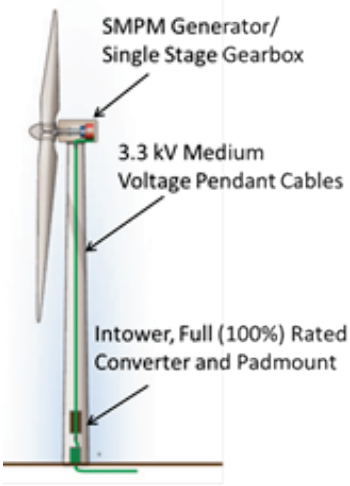

Fig. 1. Preferred wind turbine electrical architecture showing a medium-voltage fully rated converter, medium-voltage pendant cables, and converter with padmount transformer located within the base of the turbine tower.

To take advantage of the architectural features of Fig. 1, the thermal challenges associated with locating the power converter and padmount transformer within the turbine tower must be addressed. These challenges are severe, as air-exchange tower penetrations at the base must be kept to a minimum where the turbine's entire thrust loads are reacted by the tower. These loads are the largest at the base and penetrations need to be offset by the use of a thicker tower wall, leading to a significant capital cost increase. Note that the tower starts out as the most expensive component on the turbine assembly. The lack of air movement and thermal challenges associated with a fully rated converter within the tower is one reason for placing a premium on converter efficiency. A second reason for increasing converter efficiency is to improve turbine energy capture. The increased energy

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capture can be used, in part, to offset higher converter costs associated with increased efficiency and to improve COE. In [1], increased energy capture is monetized by using a turbine COE model, which is a typical method for ascribing incremental value to increased energy capture.

To achieve increased converter efficiency, a team of researchers applied a two-step approach. First, we substituted a medium-voltage, three-level neutral-point-clamped (NPC) inverter for the traditional low-voltage, two-level inverter. Next, we substituted a silicon carbide (SiC) junction barrier Schottky (JBS) diode for a Si PIN diode in the clamping location and main switch free-wheeling location of the NPC inverter. The JBS diode is a majority carrier device and essentially eliminates the reverse recovery current and switching losses typically associated with a PIN diode [3-4]. This substitution significantly reduces diode turn-off losses and IGBT turn-on losses, both of which will be quantified in this paper. It will be shown that inverter efficiency will be increased by 1.5%, or a 35-kW reduction of in-tower power dissipation, for a 2.3-MW turbine.

This paper begins with a discussion of the NPC inverter layout that includes a split, three-layer laminated bus structure. This split bus is simpler than other proposed NPC bus structures that utilize more layers [5-9]. We then show that the simplified bus remains effective at maintaining low parasitic inductances and resistances in both the long and short commutation paths. A low-voltage, high-current "ring" test is presented and used to quantify these parasitics by applying the logarithmic decrement method to the test results [10-11]. Next, we present the 4.5-kV Si/SiC power module, including the die layout, 10.4-kV isolation capabilities, and static and dynamic module characteristics. These characteristics are summarized in an inverter loss model that clearly shows the advantages of the JBS diode. All results were taken from a single-phase NPC inverter test fixture that represents real-world inverter subassembly construction, which was designed as part of a wind turbine drivetrain technology development program [12].

II. NPC Inverter Layout and Bus Characterization

A. Inverter Target Specifications and Layout Approach

A summary of the wind turbine inverter specifications is provided in Table I.

TABLE I. SALIENT INVERTER SPECIFICATIONS

1	Inverter Architecture	Three-level NPC
2	Inverter Power Rating	2.3 MW
3	Interconnect Voltage	3.3 kV
4	Rated Line Current	400 A
5	DC Bus Voltage	5 kV (+/- 2.5 kV)
6	IGBT/Diode Voltage Rating	4.5 kV
7	IGBT/Diode Current Rating	1200/800 A
8	Utility Power Factor	0.95L to 0.95C

The layout of a single phase of the NPC inverter is shown in Fig. 2a below. The layout was assembled and used as a test fixture for determining parasitic inductances and qualifying the Si/SiC module level static and dynamic characteristics. A picture of the assembled single phase layout is shown in Fig. 2b. The test fixture was also run with commercial Si modules for performance comparison purposes.

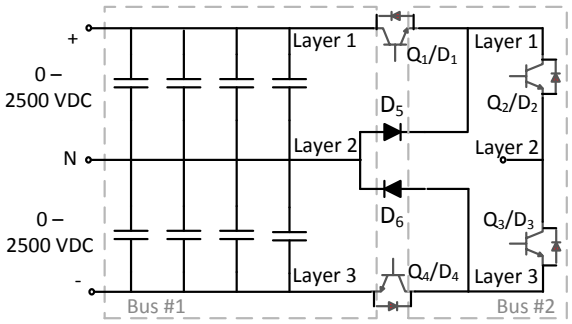


Fig. 2(a). NPC inverter schematic (emphasizing the "split" bus structure).

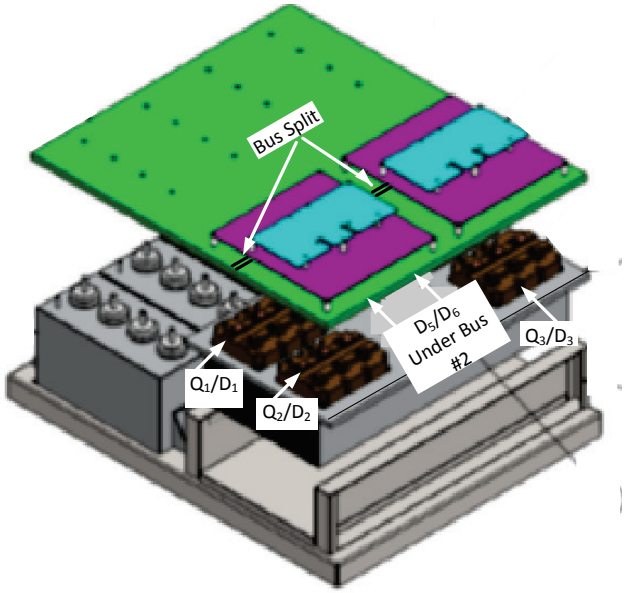


Fig. 2(b). Physical layout of a single phase of the NPC inverter. Main and auxiliary IGBT, clamping diodes, bus capacitor bank, and split bus structure correspond to Fig. 2(a).

Operation of the NPC inverter is well documented [13-14], and control of the parasitic inductances in the commutation loops is important in limiting device turn-off voltage transients. The two loops of interest in the NPC inverter include the "short" commutation loop including Q1 and D5, and the "long" commutation loop including D6, Q3, Q2, and Q1. These two loops are discussed in more detail in [15] and [16]. Laminated bus structures applying the concept of field-canceling currents are used to minimize inductances in both commutation paths. Also, notice in Fig. 2(a) that loops symmetric to those described above exist on the negative side of the bus, thus making it necessary to discuss and test only the positive loops.

Laminated bus structures for three-level NPC inverters are more complex than those used in two-level inverters. Examples of different bus structures are covered in [5-9]. These referenced structures use four and five layers and contain complicated cut-out features in an attempt to minimize stray parasitic bus inductances. The bus used in this inverter layout is unique because it uses a "split" bus, with two bus sections consisting of three layers each. Details of the layout are shown schematically in Fig. 2(a), with corresponding implementation details shown in Fig. 2(b). By splitting the bus, both structures are simplified by reducing the number of layers and eliminating cut-out features. The split bus has the added feature of being physically smaller and easier to handle. In Fig. 2(b), the clamping diodes D5 and D6 cannot be seen; however, it is important to note that they are located as close as possible to the main IGBTs, Q1 and Q4. This position helps minimize the inductance in the "short" commutation loop, where most of the switching events occur as a result of the inverter's high power factor. Locating the split between the collector-emitter (anode-cathode) has a minimal impact on total "short" commutation parasitic inductance as the module current flow in this region is vertical and through module Q1/D5. The modules use current canceling field concepts similar to the bus structure to keep module inductance low. No current flow exists in the bus structure between the collector and emitter terminal because of the vertical module current. Similar comments apply to the "long" commutation loop; however, there are two additional module inductances included in the loop. In the next section, the bus and module parasitic inductances will be quantified by means of a low-voltage, high-current "ring" test.

B. Bus Characterization and the Ring Test: An Overview

Approaches to quantifying bus inductance have been proposed in the literature [17-18]. In this paper, bus parasitic inductance and resistance are obtained by means of a "ring" test. The name is derived from a test response that consists of a ringing, lightly damped second-order RLC response. The test offers the following advantages over previous approaches:

- High operating voltage is not required, as the test can be performed at 10–20 V
- High current, i.e., hundreds to thousands of amps to include bus proximity effects
- Complex, single, dual-pulse switching regimes are not required
- It utilizes design bus capacitance necessary in quantifying commutation path parasitics (assumes amount of capacitance is known from other test)
- It provides a simple, effective approach to comparing competing bus layouts.

The test is setup by pre-charging the DC bus capacitors to the test level and then completing the commutation circuit by the closing a mechanical plate-switch at one of the power module locations in the commutation circuit. Other power modules beyond the plate-switch location, but in the commutation path, are replaced with a shorting plate with pre-determined inductance. The second-order response to closing the circuit is measured at a convenient point, for example, at the capacitor bank terminals. Measured frequency and magnitude information is then used in a logarithmic decrement calculation to determine parasitics R and L. Theoretical details for the test are provided below.

Fig. 3(a) is a schematic representation of the "short" commutation path in the NPC inverter. The schematic includes the capacitor bank C_+ with corresponding (assumed known) internal inductance and resistance L_{C+} and R_{C+}, respectively. Bus parasitics R_{B1} and L_{B1} represent the bus connection between the capacitor bank and the collector of the main IGBT, Q_1. R_{Q1} and L_{Q1} are main IGBT module parasitics, R_{B2} and L_{B2} are bus parasitics, L_{D5} and R_{D5} are clamping diode module parasitics, and R_{B6} and L_{B6} are final bus commutation circuit parasitics. These same parasitics are shown (but not designated) on the bus structure in Fig. 3(b). The clamping diode D_5 is replaced by a shorting plate spanning both of its module terminals. This plate and the corresponding parasitics are shown in red and to the right in Fig. 3(a) and as a white-dashed rectangle covering the diode terminals in Fig. 3(b). Similarly, a plate-switch spanning all three of the main IGBT terminals is shown in Fig. 3(a) and Fig. 3(b). This plate-switch is rigidly connected to the collector side of the module and is positioned just above the terminals of the emitter. The test is initiated by pressing the plate-switch down to the three emitter terminals to complete the commutation circuit. An oscillograph of the capacitor terminal voltage response is taken with the oscilloscope triggered by the plate-switch closure. An example response is shown in Fig. 5(b).

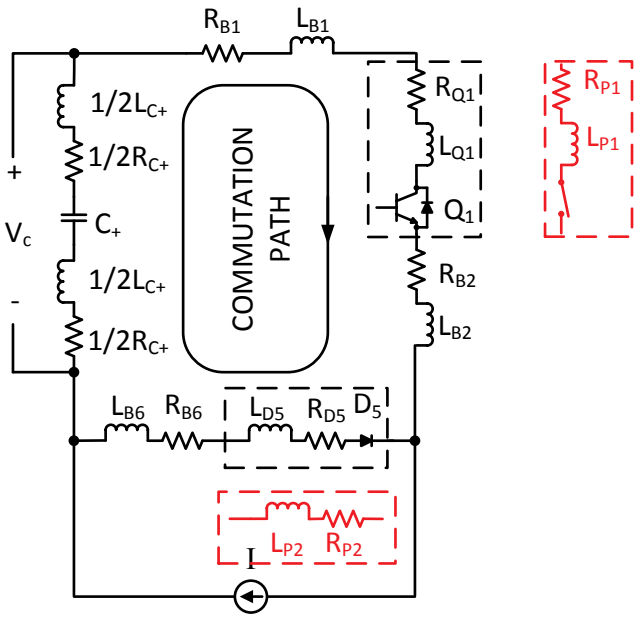


Fig. 3(a). Schematic representation of the "short" commutation circuit including parasitic elements. The diode shorting plate is indicated below D5 in red. The plate-switching element is located to the right of Q1. The output current is represented as I, a constant current over the commutation duration.

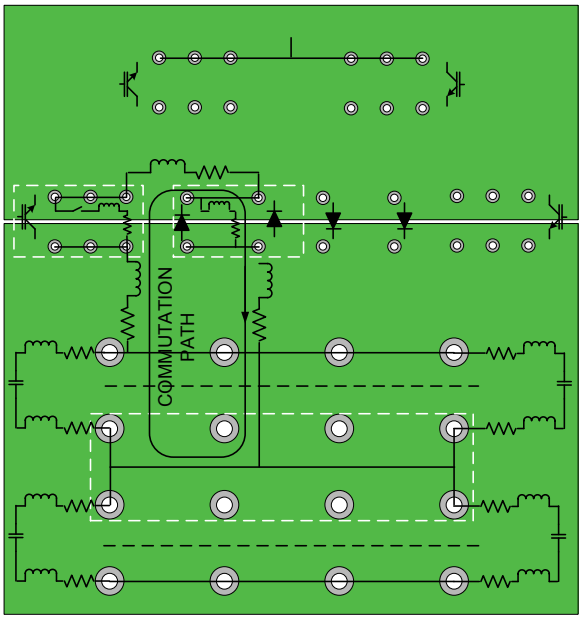
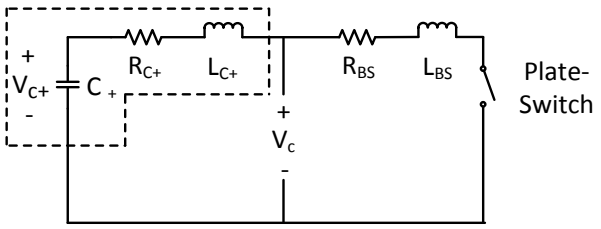


Fig. 3(b). A split bus with a "short" commutation path from Fig. 3(a) identified.

C. *Mathematical Details of the Ring Test*

The elements in the schematic of Fig. 3(a) are lumped together in the simplified circuit of Fig. 4. Note that the "BS" subscript notation is used to denote the bus "short" commutation path.



$R_{BS} = R_{B1} + R_{B2} + R_{B6} + R_{Q1} + R_{D5}$

$L_{BS} = L_{B1} + L_{B2} + L_{B6} + L_{Q1} + L_{D5}$

Fig. 4. Simplified commutation circuit showing capacitor bank and lumped parasitic resistances and inductances. Voltage measurement is at the capacitor terminals.

This simplified representation is recognized as a series RLC circuit described by the following circuital equation

$$L\frac{di(t)^2}{dt} + R\frac{di(t)}{dt} + \frac{1}{C}i(t) = 0 \qquad (1)$$

where $L = L_{BS} + L_{C+}$, $R = R_{BS} + R_{C+}$ and $C = C_{+}$. Initial conditions include

$$i(0) = 0, \frac{di(0)}{dt} = \frac{V}{L}; v_C(0) = V. \qquad (2)$$

Traditional second-order terms are formed such that

$$\alpha \equiv \frac{R}{2L};\ \omega_0 \equiv \frac{1}{\sqrt{1/LC}};\ \omega_D \equiv \sqrt{{\omega_0}^2 - \alpha^2}. \qquad (3)$$

A solution to equation (1) and its derivative is given by

$$i(t) = \frac{V}{L\omega_D} e^{-\alpha t} \sin(\omega_D t) \qquad (4)$$

$$\frac{di(t)}{dt} = \frac{V}{L\omega_D} e^{-\alpha t}(\omega_D \cos(\omega_D t) - \alpha \sin(\omega_D t). \qquad (5)$$

Voltage, v_c, at the measurement point, can be expressed as

$$v_c(t) = R_{BS} i(t) + L_{BS}\frac{di(t)}{dt}; t \geq 0 \qquad (6)$$

Substituting equations (3) and (4) into (6) gives the ring test measurement voltage as

$$v_c(t) = \frac{V}{L\omega_D} e^{-\alpha t}\{(R_{BS} - L_{BS}\,\alpha)\sin(\omega_D t) + L_{BS}\,\omega_D \cos(\omega_D t)\}. \qquad (7)$$

It is often the case that $L_{BS}\,\omega_D \gg (R_{BS} - L_{BS}\,\alpha)$, leading to the approximation

$$v_c(t) \approx \frac{V}{L\,\omega_D} e^{-\alpha t} L_{BS}\,\omega_D \cos(\omega_D t); t \geq 0. \qquad (8)$$

Fig. 5(a). Completed single phase test fixture as described in Fig. 2(b).

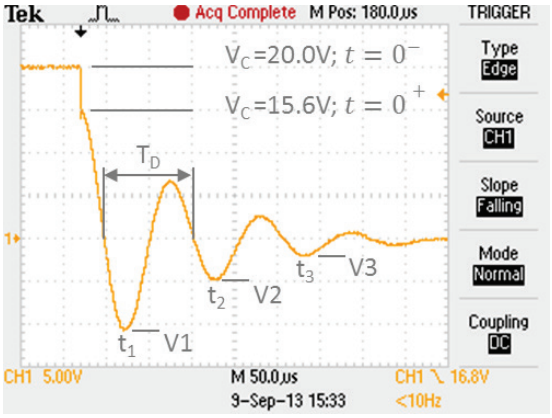


Fig. 5(b). "Short" commutation second-order response to the ring test.

At $t = 0^+$, there is an immediate drop in v_c

$$v_C(0^+) = V\,\frac{L_{BS}}{L} \tag{9}$$

which is a simple voltage division statement upon the plate-switch closure.

Capacitance C+ is known, as well as the capacitor parasitic elements R_C+ and L_C+. This information, together with the response in Fig. 5(b), overdetermines total parasitic elements as well as bus parasitic elements. One approach to obtaining parasitic elements starts by using equation (8), from which inductances can be determined

$$15.6\,V = 20\,V\,\frac{L_{BS}}{L} = 20\,V\,\frac{L_{BS}}{L} \rightarrow L = 110\,nH$$

$$L_{BS} = 85.8\,nH, L_{C+} = 24.2\,nH. \tag{11}$$

By applying the method of logarithmic decrement, [10-11], R can be obtained from the relationship in (3)

$$-\alpha\,T_D = -\frac{R}{2L}T_D = \ln\left(\frac{|V_2|}{|V_1|}\right) = \ln\left(\frac{4.9}{11.5}\right) \rightarrow$$

$$R = 3.43\,m\Omega, R_{BS} = 1.83\,m\Omega, R_{C+} = 1.6\,m\Omega. \tag{12}$$

For comparison purposes, the "long" commutation parasitics using the ring test approach were determined as $L = 192.2\,nH$, $L_{BL} = 168\,nH$, $R = 4.45\,m\Omega$, and $R_{BL} = 2.85\,m\Omega$.

III. The SiC Barrier Diode and Efficiency Improvements

A. Locating the SiC Barrier Diode in the NPC Inverter

Of the three diode locations in the positive portion of Fig 2(a)—D1, D2, and D5—the question remains of which Si PIN diodes should be replaced by SiC JBS diodes to effectively increase inverter efficiency. This question is answered in [1] and [4]. The former reference develops a simplified circuit of the NPC inverter operating at inverter unity power factor and shows that, under these conditions, only the clamping diode undergoes repetitive reverse recovery at the inverter switching frequency. In this specific case, there is no advantage in substituting JBS diodes for D1 and D2. Because the wind turbine inverter must operate over a nonunity power factor range as given in Table I, marginal additional benefits do accrue to substituting JBS diodes in the main and auxiliary locations. In the test fixture discussed in this work, all PIN diodes were substituted with SiC JBS diodes. The JBS module diode consists of twenty 4.5-kV, 40A, 8 mm x 10 mm SiC die. Each die has a 450-μm floating guard ring leaving 0.72 cm^2 of active area. The diode has a 1.1 Schottky junction voltage drop and exhibits a specific resistance of 51mΩ-cm^2. The die were processed on a 100-mm 4HN-SiC wafer.

The SiC diodes were placed in standard 130 mm x140 mm (clamping diode) and 140 mm x 190 mm (IGBT) industry-standard, 10.4-kV isolation voltage modules. The modules use a fluted case to increase creepage and clearance distances, a 1.0-mm ceramic substrate, special substrate coatings, and the control of sharp edges to meet the 10.4 kV requirements. Internal electrode layout uses current canceling techniques to minimize the module's internal inductances as discussed in the previous section. Fig. 6 shows the "fluted" IGBT module and the internal location of the SiC die for both the diode and the IGBT module.

Fig. 6(a). "Fluted" 10.4-kV isolated IGBT/SiC hybrid module [19].

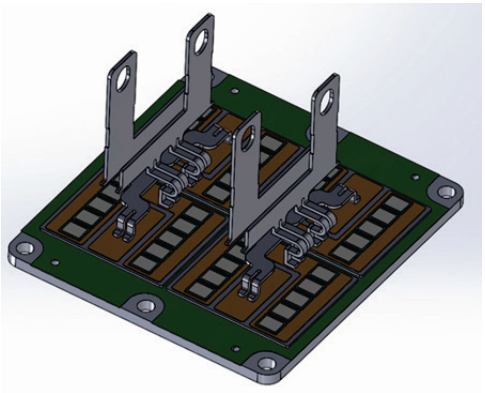


Fig. 6(b). Internal layout of the SiC diode module.

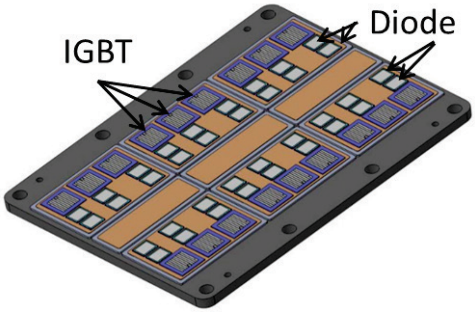


Fig. 6 (c) Internal layout of the IGBT/SiC hybrid module.

B. SiC Barrier Diode Static and Dynamic Characteristics

Forward conduction characteristics for the commercial Si PIN diode and hybrid SiC JBS diode are shown in Fig. 7. The forward characteristics were taken at the 40A die level and then scaled to the (quantity 20) module level for comparison against the Si diode. The higher forward voltage of the JBS diode will increase the diode conduction losses in the NPC inverter; however, it will be shown that the improvement in switching losses considerably offsets this small increase. One reason is when grouping the inverter's total conduction losses, the two IGBTs must be included, which is the same for both modules. The reverse characteristics shown are given at the die level and should be multiplied by a factor of 20 for comparison at the module level. When scaled for the 20 die, the SiC module has a lower reverse current by a factor of 15–20 at 25ºC. Furthermore, the JBS reverse current is independent of temperature, whereas the Si diode reverse current is strongly

influenced with temperature as a result of increased carrier concentration (i.e., current increases quickly with increasing temperature).

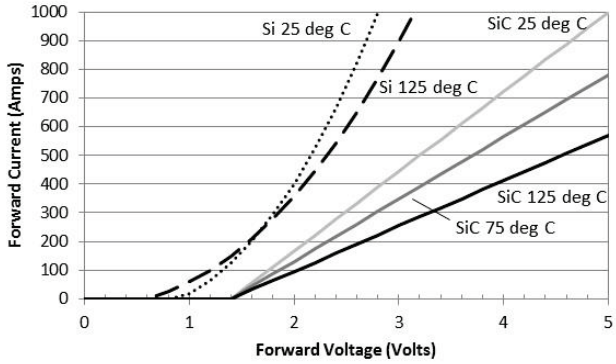


Fig. 7(a). Module-level forward conduction characteristics for the Si PIN and SiC JBS diodes.

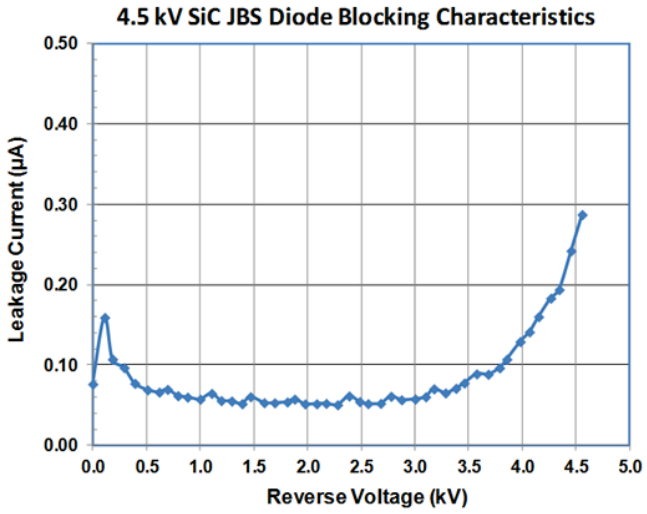


Fig. 7(b). JBS die-level reverse characteristics. Reverse current is independent of temperature and a factor of 15 lower than the published equivalent Si PIN diode module.

Switching performance of the 4.5-kV JBS diode is shown in Fig. 8 [3]. At the time of submission, switching performance at the module level had not been completed; however, the chip-level switching of an earlier 4.5-kV diode generation was completed, as shown. The switching waveforms are then used to summarize switching energies provided in Table II. The reverse recovery current and charge of the PIN diode is obvious in Fig. 8, and improvements because of the JBS diode are noticeable. It is important to also note that the reverse characteristics are nearly independent of forward current. Not shown is the fact that the reverse recovery characteristics are independent of temperature, unlike the PIN diode, which has a very strong temperature influence. This reduction in reverse recovery current causes a dramatic reduction of rectifier turn-off losses.

In addition, the diode reverse recovery characteristics have an impact on IGBT turn-on energy as this recovery current must be supplied by the IGBT during its turn-on transition. This effect can be seen in the IGBT turn-on waveforms in Fig 8(b). Table II summarizes the switching energy comparison in Fig. 8 of the Si PIN and SiC JBS diode working with the Si IGBT. The improvement provided by the JBS diode is apparent by focusing on the IGBT turn-on energy, $E_{SW\text{-}ON}$, and the diode turn-off energy, E_{REC}. The switching energies in Table II are used in a loss budget developed in the next section.

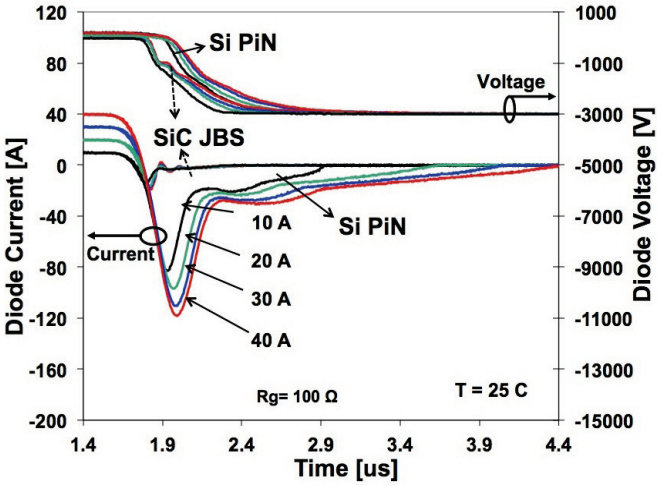


Fig. 8(a). Diode reverse recovery current and voltage for the Si PIN and SiC JBS diode at different die currents [3].

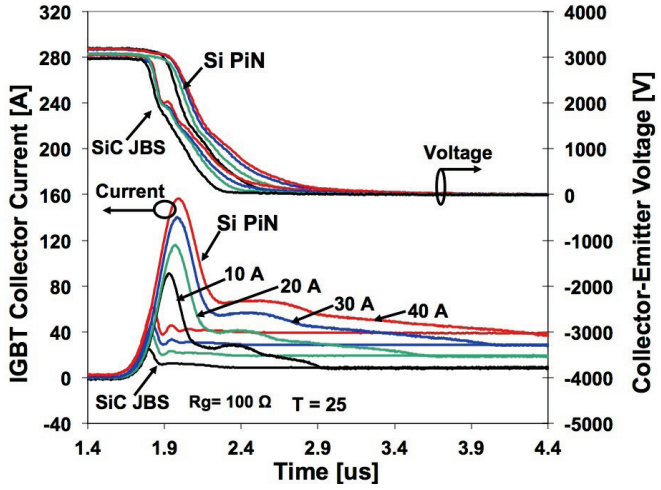


Fig. 8(b). IGBT collector current at turn-on. The presence of the diode reverse recovery current is noticeable in the IGBT collector current [3].

C. NPC Inverter Efficiency Model

As stated in the introduction, a principal objective of the inverter design is to substantially reduce the losses dissipated within the turbine tower. To summarize the advantages of the three-level NPC inverter with SiC diodes, the loss/efficiency model of [20] is used. In Fig. 9(a), the conduction losses and switching losses for the Si module and Si/SiC hybrid module are presented. Rated power in this plot corresponds to 2.3 MW, or a 400-A RMS line current. The AC line voltage is 3.3 kV with a 5-kV DC (± 2.5 kV DC) bus. The switching frequency was selected at 1.0 kHz. Losses are presented for one cell ($1/6^{th}$ of the total losses) of the NPC inverter.

TABLE II. SWITCHING ENERGIES FOR Si PIN AND SiC JBS DIODE

Current	Si IGBT with Si PIN Diode		Si IGBT with SiC Barrier Diode		Si PIN Diode	SiC Barrier Diode
	E_{SW-ON} (1)	E_{SW-OFF} (1)	E_{SW-ON} (1)	E_{SW-OFF} (1)	E_{REC} (2)	E_{REC} (1)
(Amps)	(Joules)	(Joules)	(Joules)	(Joules)	(Joules)	(Joules)
200	1.11	0.88	0.23	0.88	0.71	0.023
400	1.65	1.53	0.46	1.53	1.12	0.023
600	2.39	2.51	0.65	2.51	1.38	0.023
800	3.00	3.35	0.99	3.35	1.52	0.023
1200	4.65	4.81	1.42	4.81	1.64	0.023

(1) Data source [3]; (2) Data source is [21].

The conduction losses for the hybrid Si/SiC and Si modules nearly overlay each other, indicating that there is no significant penalty in the modestly higher forward-voltage level of the SiC diode. Any diode penalty is reduced by the fact that both inverter designs include two forward-conduction voltage drops of Si IGBTs, which dominate the total conduction losses. When comparing switching losses; however, there is a significant improvement when applying the SiC diode. At rated power, Fig. 9(a) shows a 2.1 kW improvement in switching losses at rated power for the single cell. When multiplied by six, the inverter realizes a 12.6 kW improvement in losses dissipated within the turbine tower—which is a significant improvement.

Fig 9(b) is a plot of the NPC inverter efficiency as a function of load. This figure includes losses associated with magnetics and other stray losses. An improvement of 1% is observed at 10% power and an improvement of 0.6% (12.6 kW total) is observed at 100% power. These results are presented for the line-side inverter only. In the case where a passive rectifier is used on the generator side, the line-side inverter efficiency dominates the total system efficiency. When an active rectifier is used, the losses are approximately double those in Fig. 9(a), resulting in a mathematical squaring of the Fig. 9(b) efficiencies for the entire converter. The advantages of the Si/SiC approach are amplified in the active rectifier case. Also shown in Fig. 9(b) are six measurements of a low-voltage, two-level inverter, which represents the current state of the art in wind energy inverters The hybrid-module-based, medium-voltage NPC inverter represents an approximate 1.5% improvement in line-side inverter efficiency over the two-level inverter. At 2.3 MW, this represents an approximate 34.5 kW improvement in power dissipation within the turbine tower.

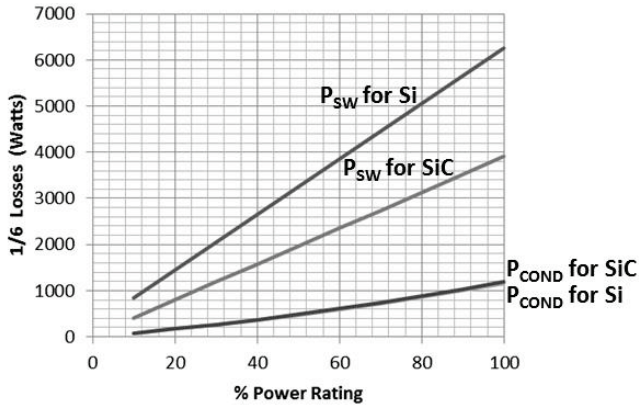


Fig. 9(a). Conduction and switching losses for one cell of the NPC inverter. Note that there is very little difference in conduction losses for the two modules. The conduction losses for the Si/SiC hybrid modules are marginally higher than for the Si modules.

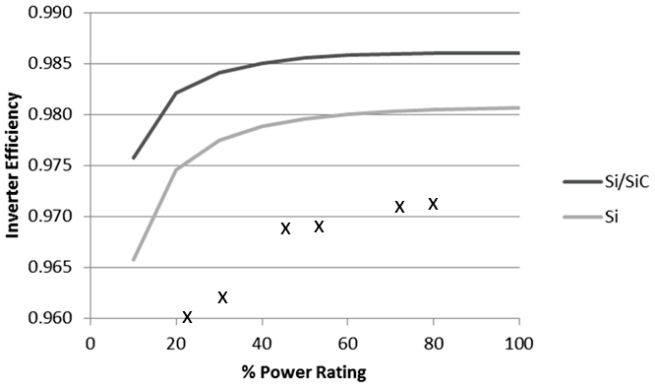


Fig. 9(b). Line-side inverter efficiency for the Si and Si/SiC hybrid modules. The six data points shown represent measured efficiency on an equivalently rated two-level, low-voltage inverter.

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