



# Beta Test Plan for Advanced Inverters Interconnecting Distributed Resources with Electric Power Systems

A. Hoke, S. Chakraborty, T. Basso,  
and M. Coddington  
*National Renewable Energy Laboratory*

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Prepared under Task No. DP12.2013

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## Executive Summary

An amendment to IEEE Std 1547 is under development to widen the range of grid voltage and frequency conditions under which distributed energy resources (DERs) may remain connected, and to allow DERs to actively contribute to voltage and frequency regulation. Collectively, these new DER features are known as advanced grid support features.

New test procedures are needed to verify the conformance of DER advanced interconnection systems to the requirements of the revised IEEE Std 1547 requirements, including advanced grid support features. In general, advanced grid support features may be interdependent, so these new test procedures should verify that interactions between features do not negatively affect grid safety, stability, or power quality. In addition, advanced grid support features operate on a range of time scales, from milliseconds to many minutes, so the new test protocols should also test DER dynamic responses. At the same time, the new test protocol should build upon the success of IEEE Std 1547 by preserving the characteristics of IEEE Std 1547.1 to the extent possible, including its balance between generality and prescriptiveness.

This document provides a preliminary (beta) test plan for grid interconnection systems of advanced inverter-based DERs. It follows the format and methodology approach established by IEEE Std 1547.1, while incorporating:

1. Upgraded tests for responses to abnormal voltage and frequency, including ride-through
2. A newly developed test for voltage regulation, including dynamic response testing
3. Modified tests for unintentional islanding, open phase, and harmonics to include testing with the advanced voltage and frequency response functions enabled.

These new tests are designed to verify that each grid support feature operates acceptably whether or not other grid support features are running simultaneously. The need to test various permutations of simultaneous features—and the large variety of new features—lead to a much larger number of tests compared to IEEE Std 1547.1. Hence, to prevent an unreasonable testing burden, this test plan reduces the number of repetitions of each test and selectively eliminates simultaneous testing of features that are very unlikely to interact, under the reasoning that a large number of slightly different tests provide acceptable assurance of field behavior.

It is important to note that this beta test plan addresses conformance of individual inverters to IEEE Std 1547a but does not address other issues that may arise with multiple inverters each performing multiple functions simultaneously on a complex power system with a variety of other control methods on potentially overlapping timescales. In addition, this test plan uses a conventional grid simulator that does not attempt to emulate the full dynamics of a real power system. Testing of multiple inverters, and testing in a power hardware-in-the-loop environment, are the subjects of ongoing and future research. Finally, this test plan attempts to strike a preliminary balance between testing enough to give acceptable confidence in the inverter's behavior and exhaustively testing every possible permutation of every variable. This balance will need to be refined through stakeholder agreement, preferably while incorporating statistical design of experiment methods where feasible.

Two advanced inverters, one single-phase and one three-phase, were tested under this beta test plan. These tests confirmed the importance of including tests for inverter dynamic response, which varies widely from one inverter to the next.

Notably, Amendment 1 to IEEE Std 1547 makes no explicit mention of settings to require DERs to ride through temporary voltage frequency deviations, but its language does allow usage of such settings. Neither inverter tested here incorporated explicit voltage or frequency ride-through settings. During abnormal voltage and frequency testing, both inverters were found to be highly accurate and consistent in their trip times and magnitudes. It is noted here that if full testing confirms the accuracy and consistency of trip times and magnitudes, then the separate settings for ride-through may not be necessary. Electric power system (EPS) and DER operators may then agree to the adequacy of a single setting that accurately configures trip time and magnitude for DER responding to abnormal conditions as well as for responding to a new requirement that it must stay connected.

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# 1 Introduction

With larger amounts of distributed energy resources (DERs) such as photovoltaic (PV) systems being deployed on electrical distribution systems, newer DER interconnection system (ICS) functions are being established to assist with electric power system (EPS) operation. In response to stakeholder demands to permit some of these advanced ICS functions, the Institute of Electrical and Electronics Engineers (IEEE) standards association has established an amendment to IEEE Std 1547-2003 (IEEE 2003). The amendment, IEEE Std 1547-Amendment 1 (abbreviated herein as 1547a), is focused on updates to voltage regulation, response to area EPS abnormal voltage and frequency conditions, and considering if other changes to IEEE Std 1547 are necessary in response to these updates.

This document introduces a preliminary (or beta) test plan for verifying conformance of ICSs to the modified interconnection requirements prescribed in IEEE Std 1547a (IEEE 2013). This beta test plan focuses on advanced inverter-based ICSs. Some initial test results from advanced inverter testing conducted at the National Renewable Energy Laboratory (NREL) are included in this document. It is expected that these initial tests will evolve along with the corresponding standards and will be further refined, validated, and harmonized to become precursors for future certification test procedures for ICSs.

Section 2 of this document describes a beta test plan for verifying conformance of ICSs to IEEE Std 1547a with a focus on advanced inverter-based ICSs. Type tests described in this document will ensure that the ICSs conform to the standard, enabling DERs to connect to the EPS safely and reliably. This test procedure does not cover all testing required for interconnection. It only covers the revised interconnection requirements specified in IEEE Std 1547a. In some cases, the test article (i.e., the inverter) will use information and communications technologies (ICT) for its operation and to provide advanced inverter functions. Testing of such ICT aspects of the interconnection is not included in this beta test plan.

This beta test plan was written before the first IEEE working group meeting to develop IEEE Std 1547.1-Amendment 1 (abbreviated herein as IEEE 1547.1a) was held. It is intended to support the IEEE working group development process and provide additional experience beyond strictly standards conformance testing, e.g., inverter characterization testing.

The test setup and the initial test results from advanced inverter testing using the beta test plan are included in Section 3.

The test plan in this document follows the outline and format of IEEE Std 1547.1 (IEEE 2005). The plan borrows extensively from the text of that document; some sentences and phrases from IEEE Std 1547.1 are used verbatim. For readability, the standard is not cited each time it is quoted. Rather, we note here that this document makes liberal use of wording borrowed from IEEE Std 1547.1. In this report, the term distributed energy resources (DER) is used instead of distributed resources (DR) as in the original IEEE 1547 documents.

*At various points in the test plan below, text boxes such as this one are inserted to elucidate the reasoning behind test design or to provide other auxiliary comments. These text boxes are not part of the test plan and are intended to aid understanding or expand on topics that arise in the plan.*

## 2 Beta Test Plan for Type Tests

Type tests are performed on a representative unit and may be conducted in the factory, at a testing laboratory, or on equipment in the field. Unless otherwise specified, equipment shall be installed per the manufacturer's specifications and operated under nominal operating conditions.

Several test procedures require the equipment under test (EUT) be operated at different discrete power levels (e.g., 33%, 66%, and 100% of rated power). Adjustments may be made to the EUT to achieve the discrete power levels, provided that these adjustments do not otherwise affect the performance of the EUT for the parameter under test. Alternatively, to accomplish testing at discrete power levels, the input source may be power limited to result in the desired EUT output power levels.

### 2.1 Test for Response to Abnormal Voltage Conditions

If the EUT senses voltage either at the point of common coupling (PCC) with the area EPS or at the point of DER connection, as specified in IEEE Std 1547, it may be tested at any convenient load level.

If the EUT senses voltage at a different point than the PCC with the area EPS or the point of DER connection, as specified in IEEE Std 1547, it shall be tested under load in conjunction with any external isolation transformer supplied or required by the EUT manufacturer.

These tests shall be performed at the terminals of the EUT.

Where appropriate, signal injection test methods may be used.

#### 2.1.1 Tests for Overvoltage and Undervoltage

*In contrast to IEEE Std 1547.1, this document includes a single test plan for both overvoltage and undervoltage.*

##### 2.1.1.1 Purpose

The purpose of this test is to verify that the DER interconnection component or system ceases to energize the area EPS as specified in IEEE Std 1547 (as amended) with respect to overvoltage and undervoltage conditions. For DERs with field-settable trip settings, this test also verifies that voltage trip settings can be modified (either remotely or locally as appropriate), and that the modified settings cause the DER to cease to energize the area EPS in response to voltage excursions. For DERs with voltage ride-through settings, this test verifies that the EUT remains connected to the EPS according to the ride-through settings.

### 2.1.1.2 Trip Magnitude

This series of tests verifies three EUT behaviors—one required behavior and two optional behaviors:

- a) Voltage trip magnitudes are in compliance with IEEE Std 1547a. This test is required.
- b) Adjustable voltage trip magnitudes and associated times behave as expected. This test shall only be conducted if the adjustable clearing voltages<sup>1</sup> are implemented in the EUT.
- c) Adjustable “must remain connected” voltage ride-through settings behave as expected. This test shall only be conducted if voltage ride-through settings are implemented in the EUT.

The required test for a) above is given in Section 2.1.1.2.1. A single test that verifies both b) and c) is given in Section 2.1.1.2.2.

#### 2.1.1.2.1 Clearing Magnitude Test Procedure—Required

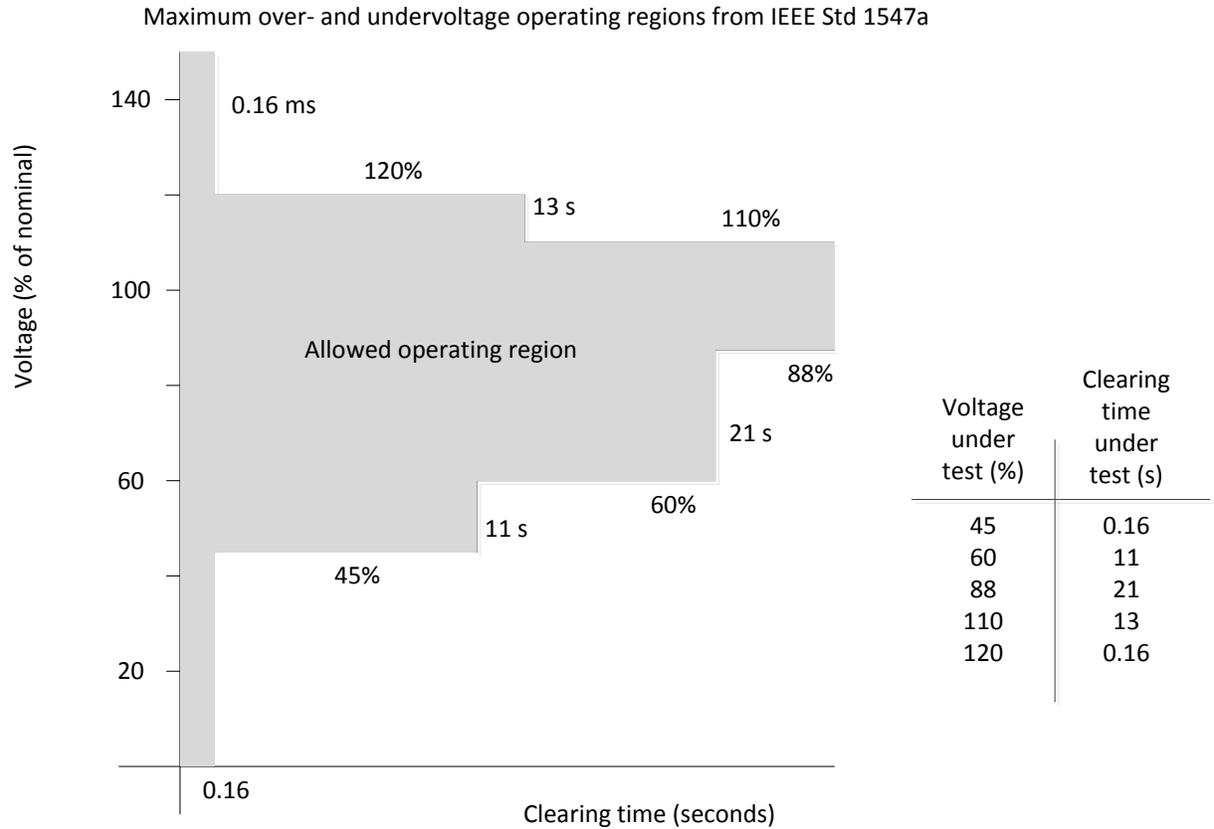
This procedure uses the ramp function defined in Annex A of IEEE Std 1547.1.

*The existing IEEE Std 1547.1 magnitude ramp function should work here. However, since many conventional inverters had only one trip time (and it was a very fast one), it is worth emphasizing in the new IEEE Std 1547.1a that the slope of the ramp function changes drastically when trip times go from 160 ms up to as high as 21 seconds (not to mention up to 300 seconds for frequency ramps). The ramp becomes so slow that each test ends up taking a very long time (for example, 20 minutes for voltage, or several hours for frequency). The time also depends on the manufacturer’s accuracy: the more accurate, the slower the ramp, and we can expect accuracies will get better as inverters improve. With multi-level curves, testers may also run into problems where it is difficult or impossible to get close enough to the trip magnitude to perform the ramp without causing a trip at a lower level. In summary, the existing ramp function is okay in general, but there will be situations where testers will need to make careful considerations and other situations where the ramp will need to be modified in a manner agreeable to the testing agency and the manufacturer.*

The EUT may have an array of clearing magnitude settings as a function of voltage, as shown in Figure Y0. This procedure verifies that clearing magnitude settings conform to IEEE Std 1547a, clause 4.2.3.

---

<sup>1</sup> “Clearing voltage” is synonymous with “voltage trip magnitude”.



**Figure Y0. Widest allowable voltage trip magnitudes and maximum clearing times from IEEE Std 1547a (as proposed, not to scale).**

- a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
- b) Set all source parameters to the nominal operating conditions for the EUT.
- c) Set all EUT parameters to the nominal operating settings (or verify that this is the case).
  - i. Verify that no clearing time and voltage setting can exceed the boundaries shown in Figure Y0 by attempting to modify the settings to exceed the boundaries.
  - ii. If the EUT will accept trip settings equal to the maximum time and voltage settings given in IEEE Std 1547a (and shown in Figure Y0), implement those settings. Otherwise, if the overvoltage clearing time settings are adjustable, set all voltage and time settings to values that best approximate the boundaries shown in Figure Y0.
- d) If the EUT is capable of confirming via communications that new trip settings have been entered, verify that the EUT communicates this correctly. *(Skip this step if not testing interactions with communications.)*
- e) Record applicable settings.

- f) Determine and record the *voltage under test* and the corresponding *clearing time under test*. The initial voltage under test is the lowest of the voltage settings recorded in step e). The clearing time under test is the clearing time associated with the voltage under test, as illustrated in Figure Y0.
- g) For single-phase units, adjust the source voltage to the holding point  $V_b$ , as defined in Annex A of IEEE Std 1547.1. Hold this voltage for time  $t_h$ ,<sup>2</sup> then initiate the voltage ramp with slope  $m$  as specified in Annex A of IEEE Std 1547.1. For multiphase units, perform this test on one phase while holding remaining phases at the nominal voltage.
- h) Record the trip magnitude.
- i) Repeat steps e) through h) seven times for a total of eight tests. Perform the eight tests under the settings given in Table Y0 (in any order).<sup>3</sup> If voltage ride-through and/or volt-VAR control is not available from the EUT, the test shall be repeated without it.

**Table Y0. EUT Settings for Clearing Voltage Magnitude Tests**

Test #	Voltage Ride-Through Setting <sup>4</sup>	Volt-VAR Setting
1-2	Off	Off
3-4	On – mfr default settings	Off
5-6	Off	On – mfr default volt-VAR settings
7-8	On – highest settings <sup>5</sup>	On – mfr default volt-VAR settings

*As shown in the above table, this test plan proposes testing each individual combination of settings only twice, as opposed to five times as in IEEE Std 1547.1. This is done to reduce the total number of tests required, which will still be much larger than the number required under IEEE Std 1547.1 due to the larger number of variations on each test.*

*The goal of tests 7 and 8 is to make sure that it is not possible to set the “must remain connected” boundary so high that it prevents clearing when the “must disconnect” boundary is crossed.*

- j) Repeat steps e) through i) for each of the clearing voltage settings, modifying the clearing time and voltage under test in step f).
- k) For multiphase units, repeat steps e) through j) for each phase individually and all phases simultaneously.
- l) If EUT parameters can be changed via more than one communications means, repeat steps c) through k) using each remaining communications means.<sup>6</sup> (*Skip this step if not testing interactions with communications.*)

<sup>2</sup> The variable  $t_h$  is at least two times the clearing time setting under test. This number may need to be adjusted to avoid conflict with other trip points.

<sup>3</sup> This step is not intended to verify voltage ride-through or volt-VAR functionality, but rather to verify that such functionality does not interfere with over/undervoltage disconnection.

<sup>4</sup> “Voltage ride-through setting” refers to a “must remain connected” boundary such as the one shown in Figure Y1 in Section 2.1.1.2.2.

<sup>5</sup> The highest voltage ride-through settings are those that come as close as the manufacturer will allow to the time and voltage trip settings in IEEE Std 1547a (Figure Y0).

<sup>6</sup> A communications means is defined here as a protocol stack, including physical layer.

**2.1.1.2.1.1 Requirements**

If used, the simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of clause 4.6.2 of IEEE Std 1547.1.

If in step k) of the procedure in Section 2.1.1.2.1 the simultaneous multiphase test results vary from the individual phase test results by more than the manufacturer’s specified accuracy, additional testing may be necessary to verify that the EUT is responding to phase to neutral magnitude changes instead of phase to phase magnitude changes.

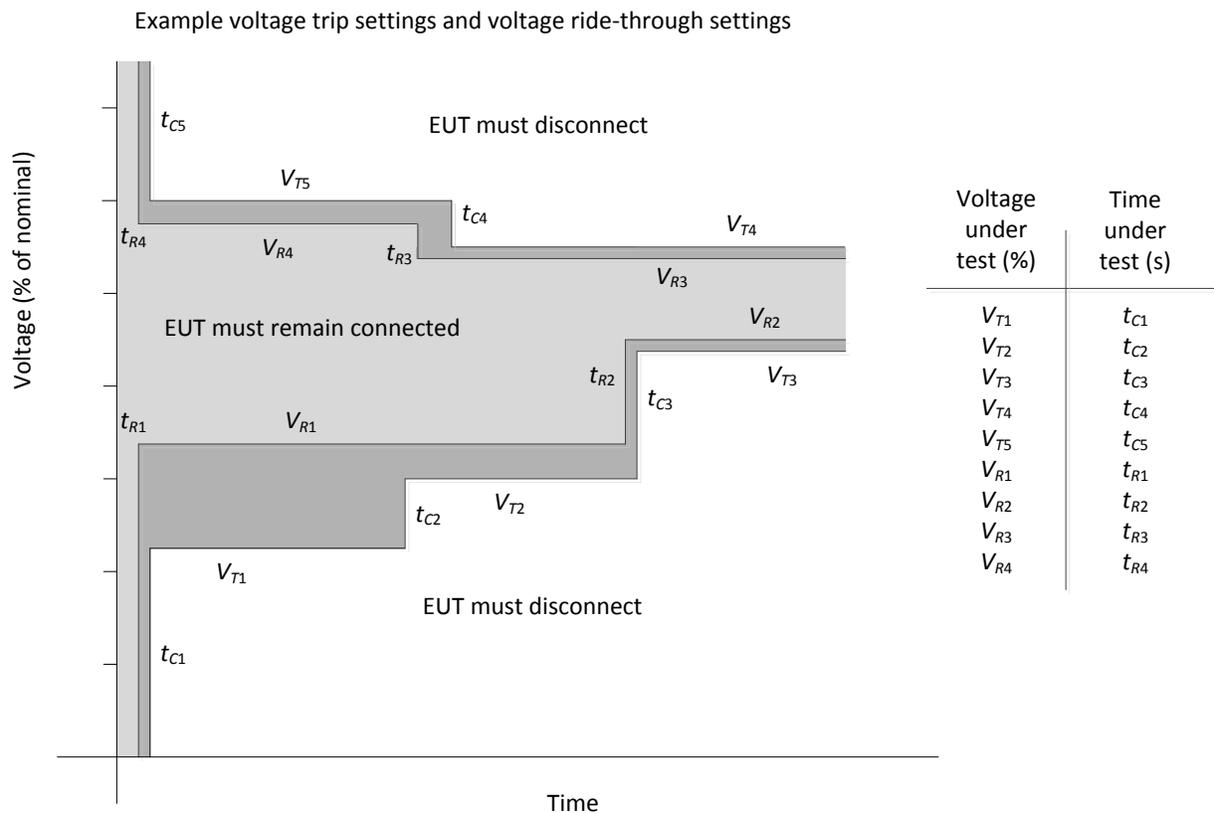
**2.1.1.2.1.2 Criteria**

The EUT shall be considered in compliance if all measured trip voltages are within the range specified in IEEE Std 1547a.

**2.1.1.2.2 Clearing Magnitude Test Procedure—Optional Functionality**

This procedure uses the ramp function defined in Annex A of IEEE Std 1547.1.

The EUT may have an array of voltage trip settings with associated clearing times and an array of ride-through (“must remain connected”) times as a function of voltage, as shown in Figure Y1. This procedure verifies that voltage trip and ride-through settings behave as expected.

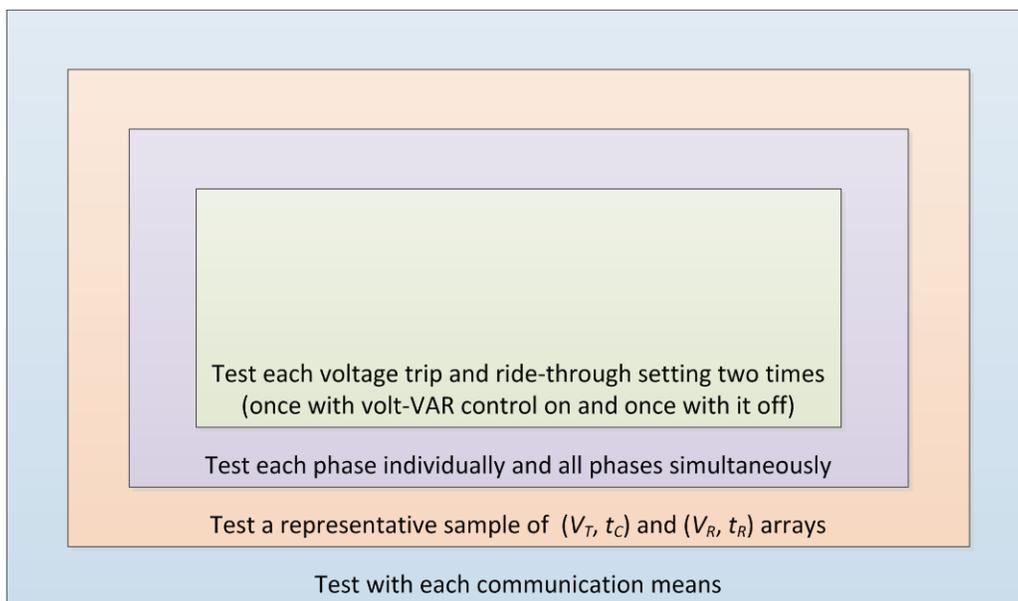


**Figure Y1. Voltage trip and ride-through settings. The number of settings may vary.**

The tests below assume voltage and time settings form step functions and are set using arrays of  $(V_T, t_C)$  and  $(V_R, t_R)$ <sup>7</sup> pairs as in Figure Y1. Alternative procedures for other types of voltage and time characteristics shall be agreed upon by the manufacturer and the testing agency.

*This test does not attempt to cover ride-through curves that are not step functions (or worse, are dynamic). These are allowed by IEEE Std 1547a, but writing a general test for them becomes complicated because the range of possible behaviors is very broad. One solution would be to instruct test labs and manufacturers to mutually agree on a new test when new behaviors are brought out. This would have the advantage of making the test plan adaptable and expandable.*

This procedure can be visualized as series of nested loops as illustrated in Figure Y2.



**Figure Y2. Visualization of voltage magnitude test iterations.**

*Testing of all permutations of trip settings, phases, ride-through settings, and arrays as shown in Figure Y2 will result in a very large number of tests. For example, a three-phase EUT with two overvoltage trip levels, two undervoltage trip levels, two overvoltage ride-through levels, and two undervoltage ride-through levels would require 192 tests. The number of repetitions of identical tests has been reduced relative to IEEE Std 1547.1 to reduce this number, under the logic that a large number of very similar tests provides at least as much confidence in an EUT's behavior as a smaller number of identical tests. It may be preferable to bring the total number of tests down even further through stakeholder agreement. This comment applies to all the test plans in this document.*

- a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
- b) Set all source parameters to the nominal operating conditions for the EUT.
- c) Set all EUT parameters to the nominal operating settings (or verify that this is the case).

<sup>7</sup>  $V_T$  is a voltage trip setting.  $t_C$  is a clearing time setting.  $V_R$  is a voltage ride-through setting.  $t_R$  is a voltage ride-through time.

- i. Set the  $(V_T, t_C)$  array defining the disconnect boundary to the manufacturer's default setting.
  - ii. Verify that the ride-through boundary cannot be set to exceed the *must disconnect* boundary by attempting to modify the settings to exceed it.
  - iii. Set the  $(V_R, t_R)$  array defining the ride-through boundary to the manufacturer's default setting.
- d) If the EUT is capable of confirming via communications that new trip settings have been entered, verify that the EUT communicates this correctly. (*Skip this step if not testing interactions with communications.*)
- e) Record applicable settings.
- f) Determine and record the *voltage under test* and corresponding *time under test*: The initial voltage under test is the lowest of the voltage trip settings and ride-through voltages recorded in step e). The time under test is the time associated with the voltage under test, as illustrated in Figure Y1.
- g) For multiphase units, this test shall be performed on one phase while holding remaining phases at the nominal voltage. Variables in this step are as defined in the ramp function in Annex A of IEEE Std 1547.1. Set the source voltage to a value corresponding to  $V_b$  and hold it there for time  $t_h$ . Ramp the source voltage up with slope  $m$  until the EUT trips.
- h) Record the trip magnitude.
- i) Repeat steps e) through h) once for a total of two tests. If the EUT can perform volt-VAR control, two of the tests should be done with volt-VAR running at the manufacturer's default settings.
- j) Repeat steps e) through i) for each of the voltage trip settings and ride-through voltage settings, modifying the time and voltage settings under test in step f).
- k) For multiphase units, repeat steps e) through j) for each phase individually and all phases simultaneously.
- l) Repeat steps c) through j) for five more pairs of voltage trip and ride-through arrays, for a total of six array pairs. The array pairs shall be as shown in Table Y1, but may need to be modified based on EUT constraints. Table Y1 uses three voltage trip arrays and three ride-through arrays (default, #1, and #2) that shall be chosen with the goal of covering a broad and representative sample of the possible array pairs in the EUT's capability range.

*Without knowledge of what settings each manufacturer allows, it is not possible to pre-specify test arrays, so it is left up to the tester to design the arrays. Alternatively, the test plan could specify arrays and note that they may need to be modified based on EUT capabilities.*

**Table Y1. Ride-Through and Disconnect Arrays for Optional Voltage Magnitude Test**

<b>Test #</b>	<b>Voltage Trip Array</b>	<b>Ride-Through Array</b>
1	Mfr default	Mfr default
2	Mfr default	As close as possible to disconnect array
3	Voltage trip array #1	Ride-through array #1
4	Voltage trip array #1	As close as possible to disconnect array
5	Voltage trip array #2	Ride-through array #2
6	Voltage trip array #2	As close as possible to disconnect array

*When the disconnect boundary is very close to the ride-through boundary, the allowable clearing magnitude range becomes very small. The even-numbered tests in this table test those cases.*

- m) If EUT parameters can be changed via more than one communications means, repeat steps c) through l) using each remaining communications means.<sup>8</sup> (*Skip this step if not testing interactions with communications.*)

#### **2.1.1.2.2.1 Requirements**

If used, the simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of clause 4.6.2 of IEEE Std 1547.1.

#### **2.1.1.2.2.2 Criteria**

The EUT shall be considered in compliance if the following two criteria are met:

- a) All measured trip voltages are as set during testing.
- b) The EUT remains connected up to all ride-through voltages set during testing.

Note that if a voltage ride-through setting is set to coincide with a voltage trip setting, the EUT must disconnect precisely at the voltage trip setting (within the manufacturer’s stated accuracy).

#### **2.1.1.3 Trip Time**

This series of tests verifies three EUT behaviors—one required behavior and two optional behaviors:

- a) Clearing times at various voltage levels are in compliance with IEEE Std 1547a. This test is required.
- b) Adjustable clearing times at various voltage levels behave as expected. This test shall only be conducted if the adjustable clearing times are implemented in the EUT.
- c) Adjustable “must remain connected” voltage ride-through settings behave as specified by the manufacturer. This test shall only be conducted if voltage ride-through settings are implemented in the EUT.

<sup>8</sup> See footnote 6.

The required test for a) above is given in Section 2.1.1.3.1. A single test that verifies both b) and c) is given in Section 2.1.1.3.2.

### 2.1.1.3.1 Clearing Time Test Procedure—Required

This procedure uses the step function defined in Annex A of IEEE Std 1547.1.

*The step function in Annex A of IEEE Std 1547.1 does not need to be modified. However, it would be helpful to draw a second version for ride-through tests when this test plan is updated.*

The EUT may have an array of clearing time settings as a function of voltage, as shown in Figure Y0. This procedure verifies that clearing time settings conform to IEEE Std 1547a, clause 4.2.3.

- a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
- b) Set all source parameters to the nominal operating conditions for the EUT.
- c) Set all EUT parameters to the nominal operating settings (or verify that this is the case).
  - i. Verify that no clearing time and voltage setting can exceed the boundaries shown in Figure Y0 by attempting to modify the settings to exceed the boundaries.
  - ii. If the EUT will accept trip settings equal to the maximum time and voltage settings given in IEEE Std 1547a (and shown in Figure Y0), implement those settings. Otherwise, if the voltage clearing time settings are adjustable, set all voltage and time settings to values that best approximate the boundaries shown in Figure Y0.
- d) If the EUT is capable of confirming via communications that new trip settings have been entered, verify that the EUT communicates this correctly. (*Skip this step if not testing interactions with communications.*)
- e) Record applicable settings.
- f) Determine and record the *clearing time under test* and corresponding *voltage under test*: The initial clearing time under test is the lowest of the clearing times recorded in step e). The voltage under test is the voltage at which the clearing time under test is active, as illustrated in Figure Y0.
- g) Set the source voltage to a value within 10% of, but not exceeding, the voltage setting under test. Hold the source at this setting for period  $t_h$ .<sup>9</sup> At the end of this period, step the source voltage to a value that exceeds the voltage setting under test by twice the manufacturer's stated accuracy. Hold this value until the unit trips. For multiphase units, this test may be performed on one phase only.
- h) Record the trip time.

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<sup>9</sup> See footnote 2.

- i) Repeat steps e) through h) seven times for a total of eight tests. Perform the eight tests under the settings given in Table X0 (in any order).<sup>10</sup> If voltage ride-through and/or volt- VAR control is not available from the EUT, the test shall be repeated without it.

**Table X0. EUT Settings for Clearing Time Tests**

Test #	Voltage Ride-Through Setting <sup>11</sup>	Volt-VAR Setting
1-2	Off	Off
3-4	On – mfr default settings	Off
5-6	Off	On – mfr default volt-VAR settings
7-8	On – highest settings <sup>12</sup>	On – mfr default volt-VAR settings

*The goal of tests 7 and 8 is to make sure that it is not possible to set the “must remain connected” boundary so high that it prevents clearing when the “must disconnect” boundary is crossed.*

- j) Repeat steps e) through i) for each of the clearing time settings, modifying the clearing time and voltage under test in step f).
- k) If EUT parameters can be changed via more than one communications means, repeat steps c) through j) using each remaining communications means.<sup>13</sup> (*Skip this step if not testing interactions with communications.*)

#### **2.1.1.3.1.1 Requirements**

If used, the simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of clause 4.6.2 of IEEE Std 1547.1.

#### **2.1.1.3.1.2 Criteria**

The EUT shall be considered in compliance if all measured trip times are within the appropriate clearing times for the voltage range specified in IEEE Std 1547a.

#### **2.1.1.3.2 Clearing Time Test Procedure—Optional Functionality**

This procedure uses two step functions defined in Annex A of IEEE Std 1547.1.

The EUT may have an array of clearing time settings as a function of voltage and an array of ride-through times as a function of voltage, as shown in Figure Y1. This procedure verifies that the EUT behaves as expected when clearing times and voltages are adjusted and ride-through times are implemented.

<sup>10</sup> This step is not intended to verify voltage ride-through or volt-VAR functionality, but rather to verify that such functionality does not interfere with overvoltage disconnection time.

<sup>11</sup> “Voltage ride-through setting” refers to a “must remain connected” boundary such as the one shown in Figure Y1 in Section 2.1.1.2.2.

<sup>12</sup> The highest voltage ride-through settings are the settings that come as close as the manufacturer will allow to the time and voltage trip settings in IEEE Std 1547a (Figure Y0).

<sup>13</sup> A communications means is defined here as a protocol stack, including physical layer.

The tests below assume voltage and time settings form step functions and are set using arrays of  $(V_T, t_C)$  and  $(V_R, t_R)$ <sup>14</sup> pairs as in Figure Y1. Alternative procedures for other types of voltage and time characteristics shall be agreed upon by the manufacturer and the testing agency.

This procedure can be visualized as series of nested loops as illustrated in Figure Y2.

- a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
- b) Set all source parameters to the nominal operating conditions for the EUT.
- c) Set all EUT parameters to the nominal operating settings (or verify that this is the case).
  - i. Set the  $(V_T, t_C)$  array defining the disconnect boundary to the manufacturer's default setting.
  - ii. Verify that the ride-through boundary cannot be set to exceed the *must disconnect* boundary by attempting to modify the settings to exceed it.
  - iii. Set the  $(V_R, t_R)$  array defining the ride-through boundary to the manufacturer's default setting.
- d) If the EUT is capable of confirming via communications that new trip settings have been entered, verify that the EUT communicates this correctly. (*Skip this step if not testing interactions with communications.*)
- e) Record applicable settings.
- f) Determine and record the *time under test* and corresponding *voltage under test*: The initial time under test is the lowest of the clearing times and ride-through times recorded in step e). The voltage under test is the voltage at which the time under test is active, as illustrated in Figure Y1.
- g) Set the source voltage to a value within 10% of, but not exceeding, the voltage under test. Hold the source at this setting for period  $t_h$ .<sup>15</sup> At the end of this period, step the source voltage to a value that exceeds the voltage under test by twice the manufacturer's stated accuracy. Hold this value until the unit trips. For multiphase units, this test may be performed on one phase only.
- h) Record the trip time.
- i) Set the source voltage to a value that is within the lowest ride-through voltage setting by twice the manufacturer's stated accuracy. Hold the source at this voltage for at least five minutes. Record whether the EUT disconnected.
- j) Repeat steps e) through i) one time for a total of two tests. If the EUT can perform volt-VAR control, one of the tests should be done with volt-VAR running at the manufacturer's default settings.

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<sup>14</sup> See footnote 7.

<sup>15</sup> See footnote 2.

- k) Repeat steps e) through j) for each of the clearing time settings and ride-through time settings, modifying the time and voltage settings under test in step f).
- l) Repeat steps c) through k) for five more pairs of  $(V_T, t_C)$  and  $(V_R, t_R)$  arrays, for a total of six array pairs. The array pairs shall be as shown in Table X1, but may need to be modified based on EUT constraints. Table X1 uses three voltage trip arrays and three ride-through arrays (default, #1, and #2) that shall be chosen with the goal of covering a broad and representative sample of the EUT capability range.

*Without knowledge of what settings each manufacturer allows, it is not possible to pre-specify test arrays, so it is left up to the tester to design the arrays. Alternatively, the test plan could specify arrays and note that they may need to be modified based on EUT capabilities.*

**Table X1. Ride-Through and Disconnect Arrays for Optional Clearing Time Test**

Test #	Voltage Trip Array	Ride-Through Array
1	Mfr default	Mfr default
2	Mfr default	As close as possible to disconnect array
3	Voltage trip array #1	Ride-through array #1
4	Voltage trip array #1	As close as possible to disconnect array
5	Voltage trip array #2	Ride-through array #2
6	Voltage trip array #2	As close as possible to disconnect array

*When the disconnect boundary is very close to the ride-through boundary, the allowable clearing time range becomes very small. The even-numbered tests in this table test those cases.*

- m) If EUT parameters can be changed via more than one communications means, repeat steps c) through l) using each remaining communications means.<sup>16</sup> *(Skip this step if not testing interactions with communications.)*

#### **2.1.1.3.2.1 Requirements**

If used, the simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of clause 4.6.2 of IEEE Std 1547.1.

#### **2.1.1.3.2.2 Criteria**

The EUT shall be considered in compliance if the following three criteria are met:

- a) All measured trip times are within the voltage-appropriate clearing times as set during testing.
- b) All measured trip times are greater than or equal to the voltage-appropriate ride-through times as set during testing.
- c) The EUT did not disconnect during step i).

<sup>16</sup> See footnote 6.

## 2.2 Test for Response to Abnormal Frequency Conditions

### 2.2.1 Test for Overfrequency and Underfrequency

*In contrast to IEEE Std 1547.1, this document includes a single test plan that covers both overfrequency and underfrequency conditions.*

#### 2.2.1.1 Purpose

The purpose of this test is to verify that the DER interconnection component or system ceases to energize the area EPS as specified in IEEE Std 1547a with respect to overfrequency and underfrequency conditions. For DERs with field-settable trip settings, this test also verifies that frequency trip settings can be modified (either remotely or locally as appropriate), and that the modified settings cause the DER to cease to energize the area EPS in response to frequency excursions. For DERs with frequency ride-through settings, this test verifies that the EUT remains connected to the EPS according to the ride-through settings.

#### 2.2.1.2 Trip Magnitude

This series of tests verifies two EUT behaviors—one required behavior and one optional behavior:

- a) Clearing frequency levels are in compliance with IEEE Std 1547a. This test is required and is given in Section 2.2.1.2.1.
- b) Adjustable “must remain connected” frequency ride-through settings behave as specified by the manufacturer. This test, given in Section 2.2.1.2.2, shall only be conducted if frequency ride-through settings are implemented in the EUT.

*The frequency test only covers one optional behavior, because under IEEE Std 1547a adjustable frequency trip settings are required (not optional) for all DERs. This is in contrast to voltage, where IEEE Std 1547a does not require adjustable trip settings for very small DERs.*

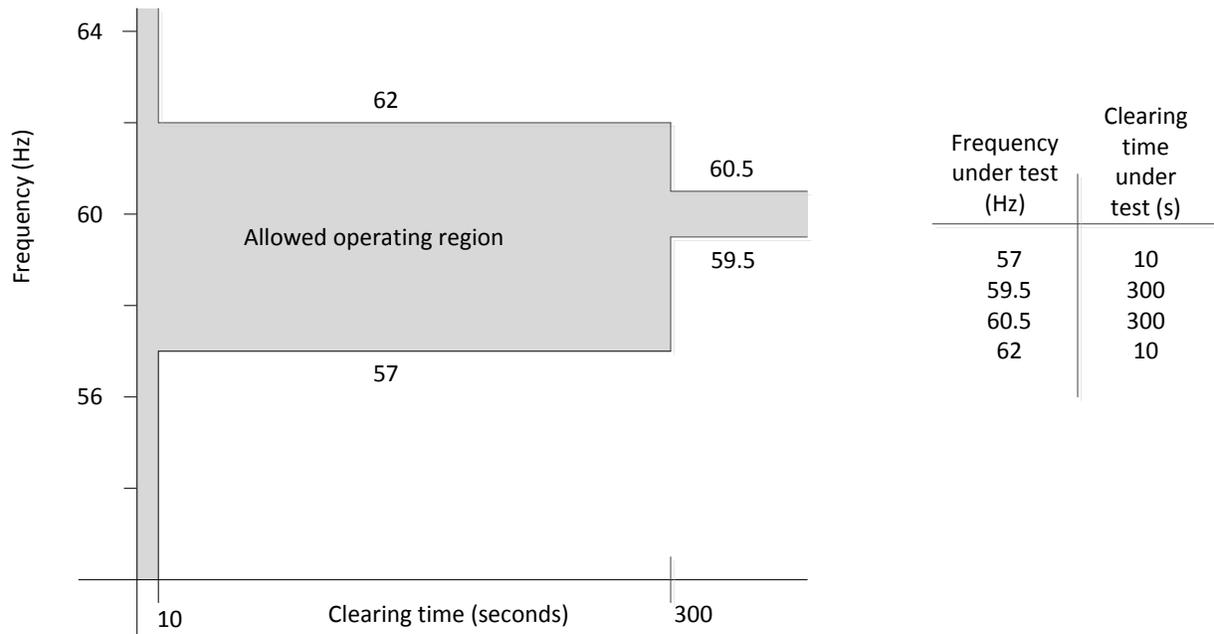
##### 2.2.1.2.1 Clearing Magnitude Test Procedure—Required

This procedure uses the ramp function defined in Annex A of IEEE Std 1547.1.

*The existing IEEE Std 1547.1 magnitude ramp function should work here. However, since most conventional inverters only have one trip time (and a very fast one), it is worth emphasizing in the new IEEE Std 1547.1a that the slope of the ramp function changes drastically when trip times go from 160 ms up to as high as 21 seconds (not to mention up to 300 seconds for frequency ramps). The ramp becomes so slow that each test ends up taking a very long time (for example, 20 minutes for voltage, or several hours for frequency). The time also depends on the manufacturer’s accuracy: the more accurate, the slower the ramp, and we can expect accuracies will get better as inverters improve. With multi-level curves, testers may also run into problems where it is difficult or impossible to get close enough to the trip magnitude to perform the ramp without causing a trip at a lower level. In summary, the ramp function is okay in general, but there will be situations where testers will need to make careful considerations and other situations where the ramp will need to be modified in a manner agreeable to the testing agency and the manufacturer.*

The EUT may have an array of clearing magnitude settings as a function of frequency, as shown in Figure F0. This procedure verifies that clearing magnitude settings conform to IEEE Std 1547a, clause 4.2.4.

Example of over- and underfrequency operating regions from IEEE Std 1547a

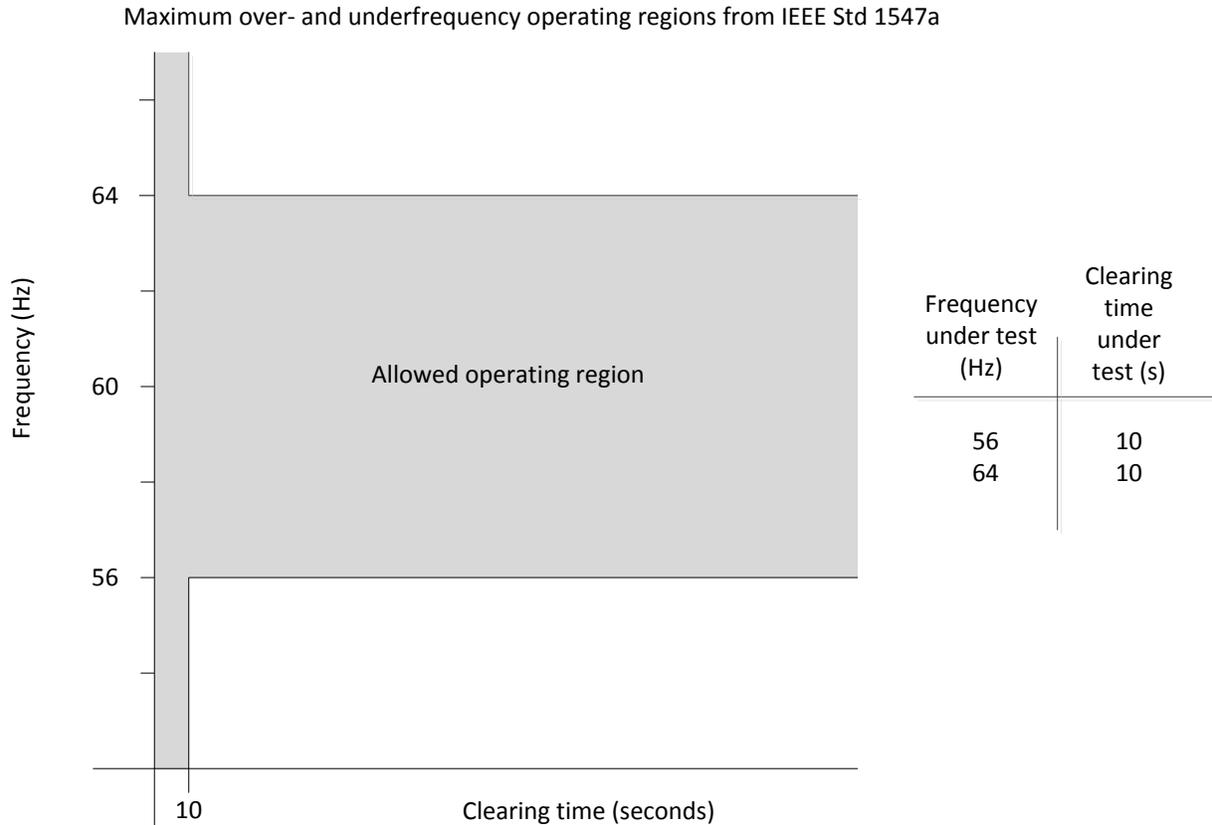


**Figure F0. Example of frequency trip magnitudes and clearing times from IEEE Std 1547a. This figure shows the *default trip frequencies* and their respective *maximum clearing times*.**

Figure F1 shows frequency trip settings with all times set to their maximum values and all magnitudes set to their extreme<sup>17</sup> values.

*Figure F0 shows **maximum** times and **default** frequencies. Figure F1 shows **maximum** times and **extreme** frequencies (which effectively means that there is only one frequency trip level since both overfrequency levels have a maximum of 64 Hz and both underfrequency levels have a minimum of 56 Hz). Two figures are shown because it is important to test the extrema for all settings, and it is also important to make clear that there are multiple levels.*

<sup>17</sup> For overfrequency settings, the extreme value is the maximum frequency allowed. For underfrequency settings, the extreme value is the minimum frequency allowed.



**Figure F1. Maximum frequency trip magnitudes and maximum clearing times from IEEE Std 1547a<sup>18</sup> range of adjustability.**

- a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
- b) Set all source parameters to the nominal operating conditions for the EUT.
- c) Set all EUT parameters to the nominal operating settings (or verify that this is the case).
  - i. Verify that no clearing time and frequency setting can exceed the maximum settings given in IEEE Std 1547.1 (shown in Figure F1) by attempting to modify the settings to exceed the boundaries.
  - ii. If the EUT will accept trip settings equal to the maximum time and frequency settings given in IEEE Std 1547a (and shown in Figure F1), implement those settings. Otherwise, set all frequency and time settings to values that best approximate the boundaries shown in Figure F1.

<sup>18</sup> Note that when both UF1 and UF2 (as defined in IEEE Std 1547a) are set to their respective maximum clearing times, UF2 effectively does not exist. The same is true for OF1 and OF2. This is why only one trip magnitude is visible in Figure F1.

- d) If the EUT is capable of confirming via communications that new trip settings have been entered, verify that the EUT communicates this correctly. *(Skip this step if not testing interactions with communications.)*
- e) Record applicable settings.
- f) Determine and record the *frequency under test* and the corresponding *clearing time under test*. The initial frequency under test is the lowest of the frequency settings recorded in step e). The clearing time under test is the clearing time associated with the frequency under test, as illustrated in Figures F0 and F1.
- g) Adjust the source frequency to the starting point  $f_b$ , as defined in Annex A of IEEE Std 1547.1. Hold this frequency for time  $t_h$ ,<sup>19</sup> then initiate the ramp as specified in Annex A of IEEE Std 1547.1.
- h) Record the trip frequency.
- i) Repeat steps e) through h) seven times for a total of eight tests. Perform the eight tests under the settings given in Table F0 (in any order).<sup>20</sup> If frequency ride-through and/or frequency response is not available from the EUT, the test shall be repeated without it.

**Table F0. EUT Settings for Clearing Frequency Magnitude Tests**

Test #	Frequency Ride-Through Setting <sup>21</sup>	Frequency Response Setting <sup>22</sup>
1-2	Off	Off
3-4	On – mfr default settings	Off
5-6	Off	On – mfr default frequency response settings
7-8	On – highest settings <sup>23</sup>	On – mfr default frequency response settings

*The goal of tests 7 and 8 is to make sure that it is not possible to set the “must remain connected” boundary so high that it prevents clearing when the “must disconnect” boundary is crossed.*

- j) Repeat steps e) through i) for each of the clearing frequency settings, modifying the clearing time and frequency under test in step f).
- k) If EUT parameters can be changed via more than one communications means, repeat steps c) through k) using each remaining communications means.<sup>24</sup> *(Skip this step if not testing interactions with communications.)*

<sup>19</sup> The variable  $t_h$  is at least two times the clearing time setting under test. This number may need to be adjusted to avoid conflict with other trip points.

<sup>20</sup> This step is not intended to verify frequency ride-through or frequency response functionality, but rather to verify that such functionality does not interfere with overfrequency disconnection.

<sup>21</sup> “Frequency ride-through setting” refers to a “must remain connected” boundary such as the one shown in Figure F3.

<sup>22</sup> A “frequency response setting” is a function that modifies DER output based on grid frequency, for example, high-frequency power curtailment.

<sup>23</sup> The highest frequency ride-through settings are those that come as close as the manufacturer will allow to the time and frequency trip settings in IEEE Std 1547a.

<sup>24</sup> A communications means is defined here as a protocol stack, including physical layer.

### 2.2.1.2.1.1 Requirements

If used, the simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of clause 4.6.2 of IEEE Std 1547.1.

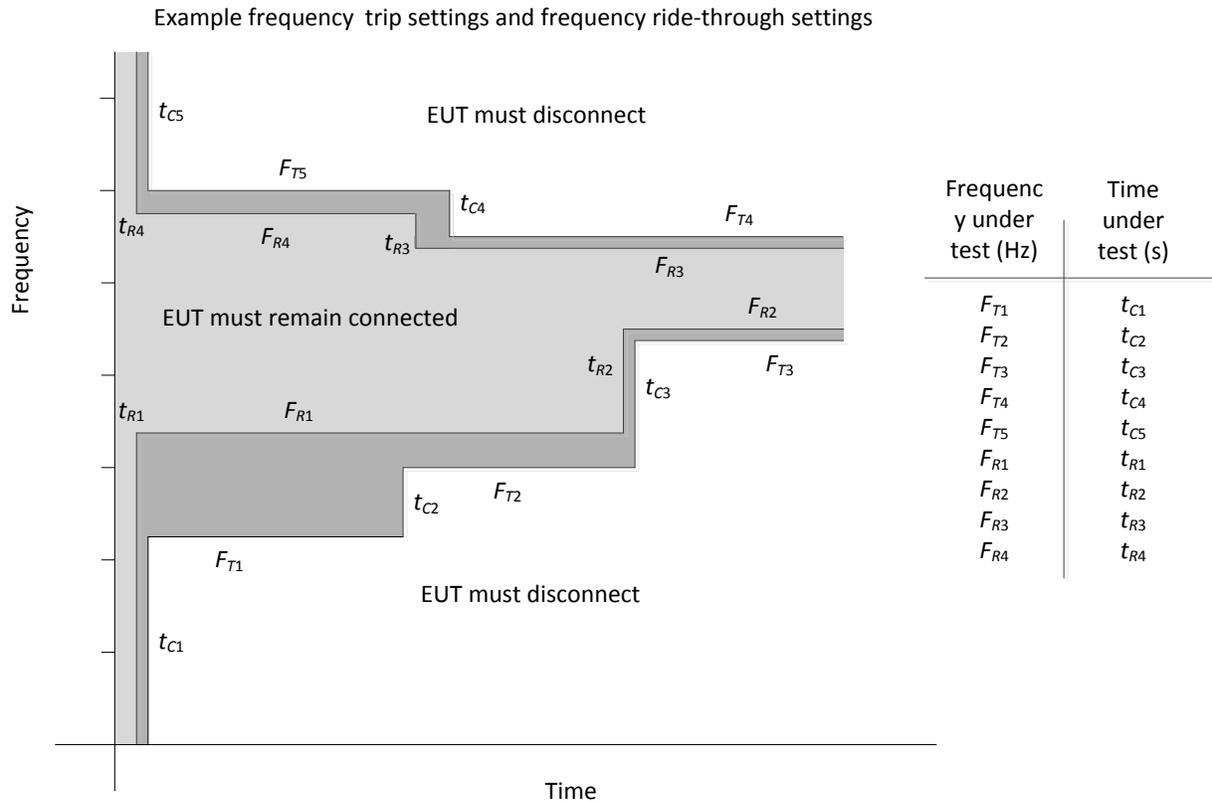
### 2.2.1.2.1.2 Criteria

The EUT shall be considered in compliance if all measured trip frequencies are within range specified in 1547a.

### 2.2.1.2.2 Clearing Magnitude Test Procedure—Optional Functionality

This procedure uses the ramp function defined in Annex A of IEEE Std 1547.1.

The EUT may have an array of frequency trip settings with associated clearing times and an array of ride-through times as a function of frequency, as shown in Figure F2. This procedure verifies that frequency trip and ride-through settings behave as specified by the manufacturer and conform to 1547a.



**Figure F2. Frequency trip and ride-through settings. The number of settings may vary.**

The tests below assume frequency and time settings form step functions and are set using arrays of  $(F_T, t_C)$  and  $(F_R, t_R)$ <sup>25</sup> pairs as shown in Figure F2. Alternative procedures for other types of frequency and time characteristics shall be agreed upon by the manufacturer and the testing agency.

*This test does not attempt to cover ride-through curves that are not step functions (or worse, are dynamic). These are allowed by IEEE Std 1547a, but writing a general test for them is complicated because the range of possible behaviors is very broad. One solution would be to instruct test labs and manufacturers to mutually agree on a new test when new behaviors are brought out. This would have the advantage of making the test plan adaptable and expandable, but it may not satisfy utilities because they would be out of the loop.*

- a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
- b) Set all source parameters to the nominal operating conditions for the EUT.
- c) Set all EUT parameters to the nominal operating settings (or verify that this is the case).
  - i. Set the  $(F_T, t_C)$  array defining the disconnect boundary to the manufacturer's default setting.
  - ii. Verify that the ride-through boundary cannot be set to exceed the *must disconnect* boundary by attempting to modify the settings to exceed it.
  - iii. Set the  $(F_R, t_R)$  array defining the ride-through boundary to the manufacturer's default setting.
- d) If the EUT is capable of confirming via communications that new trip settings have been entered, verify that the EUT communicates this correctly. (*Skip this step if not testing interactions with communications.*)
- e) Record applicable settings.
- f) Determine and record the *frequency under test* and corresponding *time under test*: The initial frequency under test is the lowest of the frequency trip settings and ride-through frequencies recorded in step e). The time under test is the time associated with the frequency under test, as illustrated in Figure F2.
- g) Variables in this step are as defined in the ramp function in Annex A of IEEE Std 1547.1. Set the source frequency to a value corresponding to  $p_b$  and hold it there for time  $t_h$ . Ramp the source frequency towards the frequency under test with slope  $m$  until the EUT trips.
- h) Record the trip magnitude.
- i) Repeat steps e) through h) once for a total of two tests. If the EUT can perform frequency response, one of the tests should be done with frequency response running at the manufacturer's default settings.

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<sup>25</sup>  $F_T$  is a frequency trip setting.  $t_C$  is a clearing time setting.  $F_R$  is a frequency ride-through setting.  $t_R$  is a frequency ride-through time.

- j) Repeat steps e) through i) for each of the frequency trip settings and ride-through settings, modifying the time and frequency settings under test in step f).
- k) Repeat steps c) through j) for five more pairs of frequency trip and ride-through arrays, for a total of six array pairs. The array pairs shall be as shown in Table F1, but may need to be modified based on EUT constraints. Table F1 uses three frequency trip arrays and three ride-through arrays (default, #1, and #2) that shall be chosen with the goal of covering a broad and representative sample of the EUT capability range.

*Without knowledge of what settings each manufacturer allows, it is not possible to pre-specify test arrays, so it is left up to the tester to design the arrays. Alternatively, the test plan could specify arrays and note that they may need to be modified based on EUT capabilities.*

**Table F1. Ride-Through and Disconnect Arrays for Optional Frequency Test**

Test #	Frequency Trip Array	Ride-Through Array
1	Mfr default	Mfr default
2	Mfr default	As close as possible to trip array
3	Frequency trip array #1	Ride-through array #1
4	Frequency trip array #1	As close as possible to trip array
5	Frequency trip array #2	Ride-through array #2
6	Frequency trip array #2	As close as possible to trip array

*When the disconnect boundary is very close to the ride-through boundary, the allowable clearing time range becomes very small. The even-numbered tests in this table test those cases.*

- l) If EUT parameters can be changed via more than one communications means, repeat steps c) through k) using each remaining communications means.<sup>26</sup> (Skip this step if not testing interactions with communications.)

**2.2.1.2.2.1 Requirements**

If used, the simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of clause 4.6.2 of IEEE Std 1547.1.

**2.2.1.2.2.2 Criteria**

The EUT shall be considered in compliance if the following two criteria are met:

- a) All measured trip frequencies are as set during testing.
- b) The EUT remains connected up to all ride-through frequencies set during testing.

Note that if a frequency ride-through setting is set to coincide with a frequency trip setting, the EUT must disconnect exactly at the frequency trip setting (within the manufacturer’s stated accuracy).

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<sup>26</sup> See footnote 6.

### 2.2.1.3 Trip Time

#### 2.2.1.3.1 Clearing Time Test Procedure—Required

This procedure uses the step function defined in Annex A of IEEE Std 1547.1.

*The existing IEEE Std 1547.1 magnitude ramp function should work here. However, because most conventional inverters only have one trip time (and a very fast one), it is worth emphasizing in the new IEEE Std 1547.1a that the slope of the ramp function changes drastically when trip times go from 160 ms up to as high as 21 seconds (not to mention up to 300 seconds for frequency ramps). The ramp becomes so slow that each test ends up taking a very long time (for example, 20 minutes for voltage, or several hours for frequency). The time also depends on the manufacturer's accuracy: the more accurate, the slower the ramp, and we can expect accuracies will get better as inverters improve. With multi-level curves, testers may also run into problems where it is difficult or impossible to get close enough to the trip magnitude to perform the ramp without causing a trip at a lower level. In summary, the ramp function is okay in general, but there will be situations where testers will need to make careful considerations and other situations where the ramp will need to be modified in a manner agreeable to the testing agency and the manufacturer.*

The EUT may have an array of clearing time settings as a function of frequency, as shown in Figure F0. This procedure verifies that no clearing time setting violates IEEE Std 1547a, clause 4.2.4.

- a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
- b) Set all source parameters to the nominal operating conditions for the EUT.
- c) Set all EUT parameters to the nominal operating settings (or verify that this is the case).
  - i. Verify that no clearing time and frequency setting can exceed maximum time and frequency settings given in IEEE Std 1547a (shown in Figure F1) by attempting to modify the settings to exceed the boundaries.
  - ii. If the EUT will accept trip settings equal to the maximum time and frequency settings shown in Figure F1, implement those settings. Otherwise, if the frequency clearing time settings are adjustable, set all frequency and time settings to values that best approximate the boundaries shown in Figure F1.
- d) If the EUT is capable of confirming via communications that new trip settings have been entered, verify that the EUT communicates this correctly. (*Skip this step if not testing interactions with communications.*)
- e) Record applicable settings.
- f) Determine and record the *clearing time under test* and corresponding *frequency under test*: The initial clearing time under test is the lowest of the clearing times recorded in step e). The frequency under test is the frequency at which the clearing time under test is active, as illustrated in Figure F0.
- g) Set the source frequency to a value within 1% of, but not exceeding, the frequency setting under test. Hold the source at this setting for period  $t_h$ .<sup>27</sup> At the end of this period, step the

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<sup>27</sup> See footnote 2.

source frequency to a value that exceeds the frequency setting under test by twice the manufacturer’s stated accuracy. Hold this value until the unit trips.

- h) Record the trip time.
- i) Repeat steps e) through h) seven times for a total of eight tests. Perform the eight tests under the settings given in Table F2 (in any order).<sup>28</sup> If frequency ride-through and/or frequency response is not available from the EUT, the test shall be repeated without it.

**Table F2. EUT Settings for Clearing Time Tests**

Test #	Frequency Ride-Through Setting <sup>29</sup>	Frequency Response Setting <sup>30</sup>
1-2	Off	Off
3-4	On – mfr default settings	Off
5-6	Off	On – mfr default frequency response settings
7-8	On – highest settings <sup>31</sup>	On – mfr default frequency response settings

*The goal of tests 7 and 8 is to make sure that it is not possible to set the “must remain connected” boundary so high that it prevents clearing when the “must disconnect” boundary is crossed.*

- j) Repeat steps e) through i) for each of the clearing time settings, modifying the clearing time and frequency under test in step f).
- k) If EUT parameters can be changed via more than one communications means, repeat steps c) through j) using each remaining communications means.<sup>32</sup> (*Skip this step if not testing interactions with communications.*)

**2.2.1.3.1.1 Requirements**

If used, the simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of 4.6.2 of IEEE Std 1547.1.

**2.2.1.3.1.2 Criteria**

The EUT shall be considered in compliance if all measured trip times are within the appropriate clearing times for the frequency range specified in IEEE Std 1547a.

**2.2.1.3.1.3 Comments**

For some EUT, the step size past the frequency trip limit should be as small as possible to reduce false results. Large frequency step changes can interfere with EUT phase lock loop operation.

<sup>28</sup> This step is not intended to verify frequency ride-through or frequency response functionality, but rather to verify that such functionality does not interfere with frequency trip time.

<sup>29</sup> “Frequency ride-through setting” refers to a “must remain connected” boundary such as the one shown in Figure F2 in Section 2.2.1.2.2.

<sup>30</sup> A “frequency response setting” is a function that modifies DER output based on grid frequency, for example, high-frequency power curtailment.

<sup>31</sup> The highest frequency ride-through settings are the settings that come as close as the manufacturer will allow to the time and frequency trip settings in IEEE Std 1547a.

<sup>32</sup> A *communications means* is defined here as a protocol stack, including physical layer.

### 2.2.1.3.2 Clearing Time Test Procedure—Optional Functionality

This procedure uses two step functions defined in Annex A of IEEE Std 1547.1.

The EUT may have an array of clearing time settings as a function of frequency and an array of ride-through times as a function of frequency, as shown in Figure F2. This procedure verifies that the EUT behaves as expected when clearing times and frequencies are adjusted and ride-through times are implemented.

The tests below assume frequency and time settings form step functions and are set using arrays of  $(F_T, t_C)$  and  $(F_R, t_R)$ <sup>33</sup> pairs as in Figure F2. Alternative procedures for other types of frequency and time characteristics shall be agreed upon by the manufacturer and the testing agency.

*This test does not attempt to cover ride-through curves that are not step functions (or worse, are dynamic). These are allowed by IEEE Std 1547a, but writing a general test for them is complicated because the range of possible behaviors is very broad. One solution would be to instruct test labs and manufacturers to mutually agree on a new test when new behaviors are brought out. This would have the advantage of making the test plan adaptable and expandable, but it may not satisfy utilities because they would be out of the loop.*

- a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
- b) Set all source parameters to the nominal operating conditions for the EUT.
- c) Set all EUT parameters to the nominal operating settings (or verify that this is the case).
  - i. Set the  $(F_T, t_C)$  array defining the disconnect boundary to the manufacturer's default setting.
  - ii. Verify that the ride-through boundary cannot be set to exceed the *must disconnect* boundary by attempting to modify the settings to exceed it.
  - iii. Set the  $(F_R, t_R)$  array defining the ride-through boundary to the manufacturer's default setting.
- d) If the EUT is capable of confirming via communications that new trip settings have been entered, verify that the EUT communicates this correctly. (*Skip this step if not testing interactions with communications.*)
- e) Record applicable settings.
- f) Determine and record the *time under test* and corresponding *frequency under test*: The initial time under test is the lowest of the clearing times and ride-through times recorded in step e). The frequency under test is the frequency at which the time under test is active, as illustrated in Figure F2.
- g) Set the source frequency to a value within 1% of, but not exceeding, the frequency under test. Hold the source at this setting for period  $t_h$ .<sup>34</sup> At the end of this period, step the

<sup>33</sup>  $F_T$  is a frequency trip setting.  $t_C$  is a clearing time setting.  $F_R$  is a frequency ride-through setting.  $t_R$  is a frequency ride-through time.

<sup>34</sup> See footnote 2.

source frequency to a value that exceeds the frequency under test by twice the manufacturer’s stated accuracy. Hold this value until the unit trips.

- h) Record the trip time.
- i) Set the source frequency to a value that is below the lowest ride-through frequency setting by twice the manufacturer’s stated accuracy. Hold the source at this frequency for at least five minutes. Record whether the EUT disconnected.
- j) Repeat steps e) through i) three times for a total of four tests. If the EUT can perform frequency response, two of the tests should be done with frequency response running at the manufacturer’s default settings.
- k) Repeat steps e) through j) for each of the clearing time settings and ride-through time settings, modifying the time and frequency settings under test in step f).
- l) Repeat steps c) through k) for five more pairs of  $(F_T, t_C)$  and  $(F_R, t_R)$  arrays, for a total of six array pairs. The array pairs shall be as shown in Table F3, but may need to be modified based on EUT constraints. Table F3 uses three frequency trip arrays and three ride-through arrays (default, #1, and #2) that shall be chosen with the goal of covering a broad and representative sample of the EUT capability range.

*Without knowledge of what settings each manufacturer allows, it is not possible to pre-specify test arrays, so it is left up to the tester to design the arrays. Alternatively, the test plan could specify arrays and note that they may need to be modified based on EUT capabilities.*

**Table F3. Ride-Through and Disconnect Arrays for Optional Clearing Time Test**

Test #	Frequency Trip Array	Ride-Through Array
1	Mfr default	Mfr default
2	Mfr default	As close as possible to trip array
3	Frequency trip array #1	Ride-through array #1
4	Frequency trip array #1	As close as possible to trip array
5	Frequency trip array #2	Ride-through array #2
6	Frequency trip array #2	As close as possible to trip array

*When the disconnect boundary is very close to ride-through boundary, the allowable clearing time range becomes very small. The even-numbered tests in this table test those cases.*

- m) If EUT parameters can be changed via more than one communications means, repeat steps c) through l) using each remaining communications means.<sup>35</sup> *(Skip this step if not testing interactions with communications.)*

### 2.2.1.3.2.1 Requirements

If used, the simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of clause 4.6.2 of IEEE Std 1547.1.

<sup>35</sup> See footnote 6.

### 2.2.1.3.2.2 Criteria

The EUT shall be considered in compliance if the following three criteria are met:

- c) All measured trip times are within the frequency-appropriate clearing times as set during testing.
- d) All measured trip times are greater than or equal to the frequency-appropriate ride-through times as set during testing.
- e) The EUT did not disconnect during step i).

### 2.2.1.3.2.3 Comments

For some EUT, the step size past the frequency trip limit should be as small as possible to reduce false results. Large frequency step changes can interfere with EUT phase lock loop operation.

## 2.3 Unintentional Islanding

The unintentional islanding test shall remain as in IEEE Std 1547.1, with one addition: At the end of subclause 5.7.1.2 (Procedure), two final steps should be added after step o). The added steps should read as follows:

- p) Repeat steps d) through o) three times with any reactive power modulation feature<sup>36</sup> activated, for a total of four sets of tests, including the test without reactive power modulation activated. The three sets of tests with reactive power modulation should be performed under the following conditions: 1) the manufacturer's default reactive power modulation settings, 2) the settings that result in the maximum range of reactive power export, and 3) the settings that result in the minimum nonzero range of reactive power export. During each of these three tests, all voltage trip settings and voltage ride-through settings should be configured to provide the maximum trip and ride-through times, the maximum overvoltage settings, and the minimum undervoltage settings.
- q) Repeat steps d) through p) three times with any real power modulation feature activated, for a total of four sets of tests. The three sets of tests with real power modulation activated should be performed under the following conditions: 1) the manufacturer's default real power modulation settings, 2) the settings that result in the maximum range of real power, and 3) the settings that result in the minimum nonzero range of real power. During each of these three tests, frequency trip settings shall be configured for maximum trip times, maximum overfrequency settings, and minimum underfrequency settings.

*The purpose of these two additional tests is to ensure that the EUT's island detection system continues to function appropriately in the presence of four advanced grid support features:*

1. *Wide voltage operating range (voltage ride-through)*
2. *Wide frequency operating range (frequency ride-through)*
3. *Voltage regulation (e.g., volt-VAR control)*
4. *Frequency response/regulation.*

<sup>36</sup> For the purposes of this test, any DER function that adjusts DER reactive power output, phase angle, or power factor based on voltage, frequency, or real power output shall be considered a "dynamic reactive power modulation feature" and shall be activated for the tests described here. If multiple features fitting this description exist, this step shall be repeated for each of the features, potentially increasing the number of repetitions in this step from four to seven, 10, or more.

## 2.4 Open Phase

*This test should be modified to include testing under each of the following conditions individually, under all of the following conditions simultaneously, and under the manufacturer's default settings:*

- *Frequency trip and ride-through settings set to their most permissive values (longest trip time(s), highest overfrequency setting(s), lowest underfrequency setting(s))*
- *Voltage trip and ride-through settings set to their most permissive values (longest trip time(s), highest overvoltage setting(s), lowest undervoltage setting(s))*
- *Volt-VAR settings set to provide maximum capacitive reactive power at lower voltages and maximum inductive reactive power at high voltages.*

## 2.5 Harmonics

*This test should be modified to include testing both with volt-VAR control off and with it on at various voltages. It should also be conducted both with frequency response control off and with it on.*

## 2.6 Test for Voltage Regulation through Volt-VAR Control

If the EUT senses voltage either at the point of common coupling (PCC) with the area EPS or at the point of DER connection as specified in IEEE Std 1547, it may be tested at any convenient load level.

If the EUT senses voltage at a different point than the PCC with the area EPS or the point of DER connection as specified in IEEE Std 1547, it shall be tested under load in conjunction with any external isolation transformer supplied or required by the EUT manufacturer.

These tests shall be performed at the terminals of the EUT. For multiphase EUT that produce only balanced reactive power, the voltage under consideration for these tests is the average of the line to neutral root mean square (RMS) voltages. For multiphase EUT capable of unbalanced reactive power, the test shall be modified in a manner agreed upon by the manufacturer and the tester.

Where appropriate, signal injection test methods may be used.

### 2.6.1 Purpose

The purpose of this test is to verify that the EUT provides voltage support by producing reactive power as specified by the manufacturer. If the EUT is not capable of modifying its power factor or reactive power output, this test shall not be performed.

### 2.6.2 Procedure

Multiple methods of reactive power support are possible. This test verifies only one category of methods: provision of reactive power as function of voltage based on a  $Q(V)^{37}$  characteristic as shown in Figures C1–C4.

*Additional tests should be developed to cover additional types of voltage regulation as necessary.*

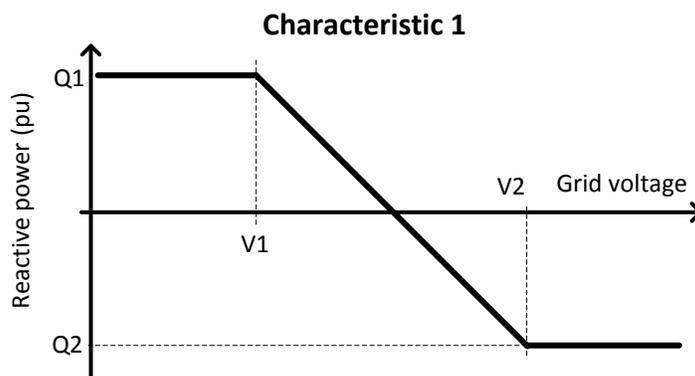
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<sup>37</sup> A  $Q(V)$  characteristic specifies EUT reactive power output ( $Q$ ) as a function of voltage ( $V$ ).

In this test procedure, maximum available reactive power is defined according to the EUT manufacturer's documentation. It may be a constant parameter, an adjustable parameter, or a function of instantaneous active power output. One definition may be specified for both capacitive and inductive reactive power, or two distinct definitions may be specified.<sup>38</sup>

This test uses several prescribed settings and test voltage profiles. If EUT parameters interfere with these settings and profiles, they shall be modified in a manner that is agreeable to the EUT manufacturer and the test lab. If the EUT includes parameters not tested in this procedure that may affect volt-VAR behavior, the test shall be modified in a manner that is agreeable to the EUT manufacturer and the test lab.

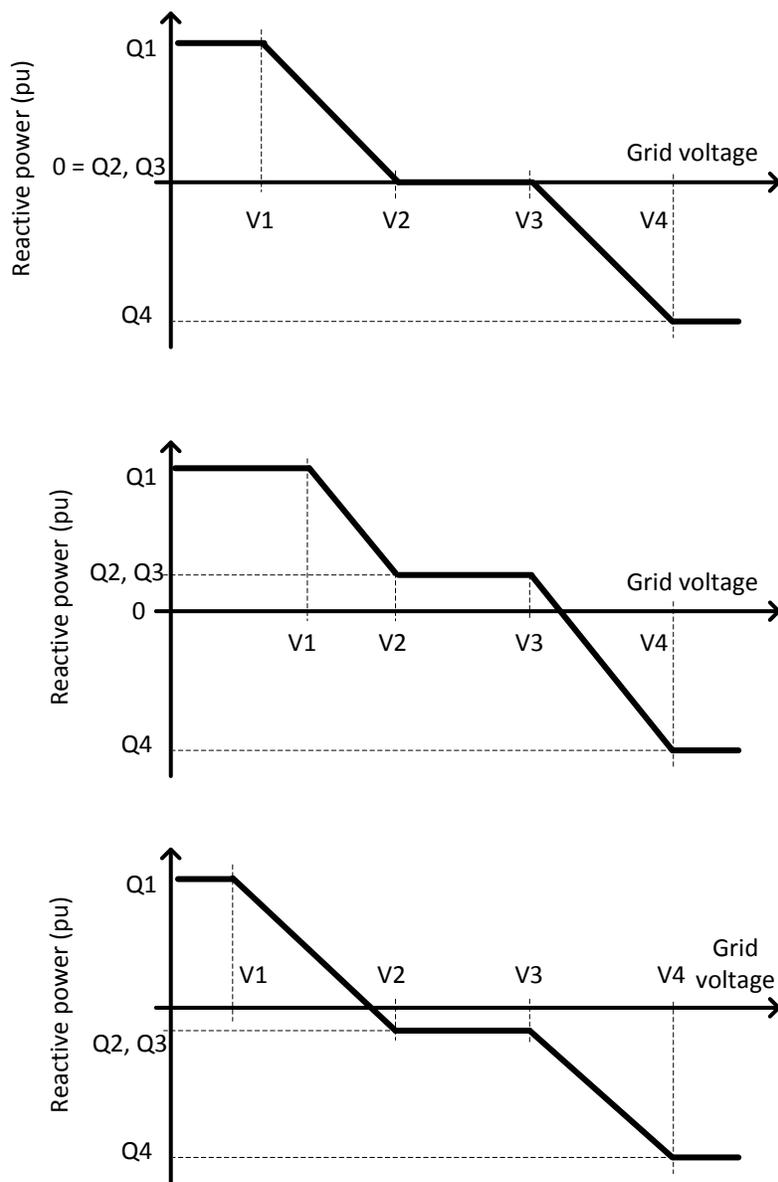
This test uses the four Q(V) characteristics shown in Figures C1–C4. Characteristic 1 is a simple droop slope. Characteristic 2 contains a range of voltages (dead-zone) for which reactive power is constant (often zero). Characteristic 3 exhibits hysteresis. Characteristic 4 exhibits both a dead zone and hysteresis.



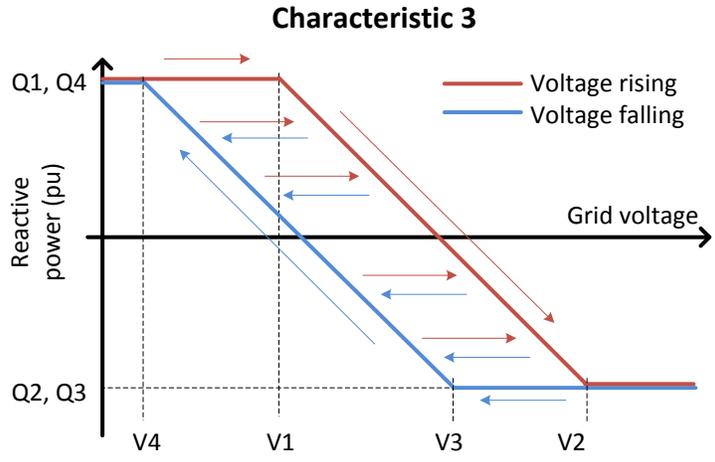
**Figure C1. Q(V) characteristic 1 for volt-VAR test: no hysteresis, no deadband. When inverter current lags voltage, the sign of Q is positive, as defined in footnote 37.**

<sup>38</sup> This document uses the generator reference frame when specifying active and reactive power (current is defined to be positive when leaving the DER) and the sign convention that lagging (inductive) reactive power produced has a positive sign. Lagging reactive power means that the current waveform lags the voltage waveform.

### Characteristic 2

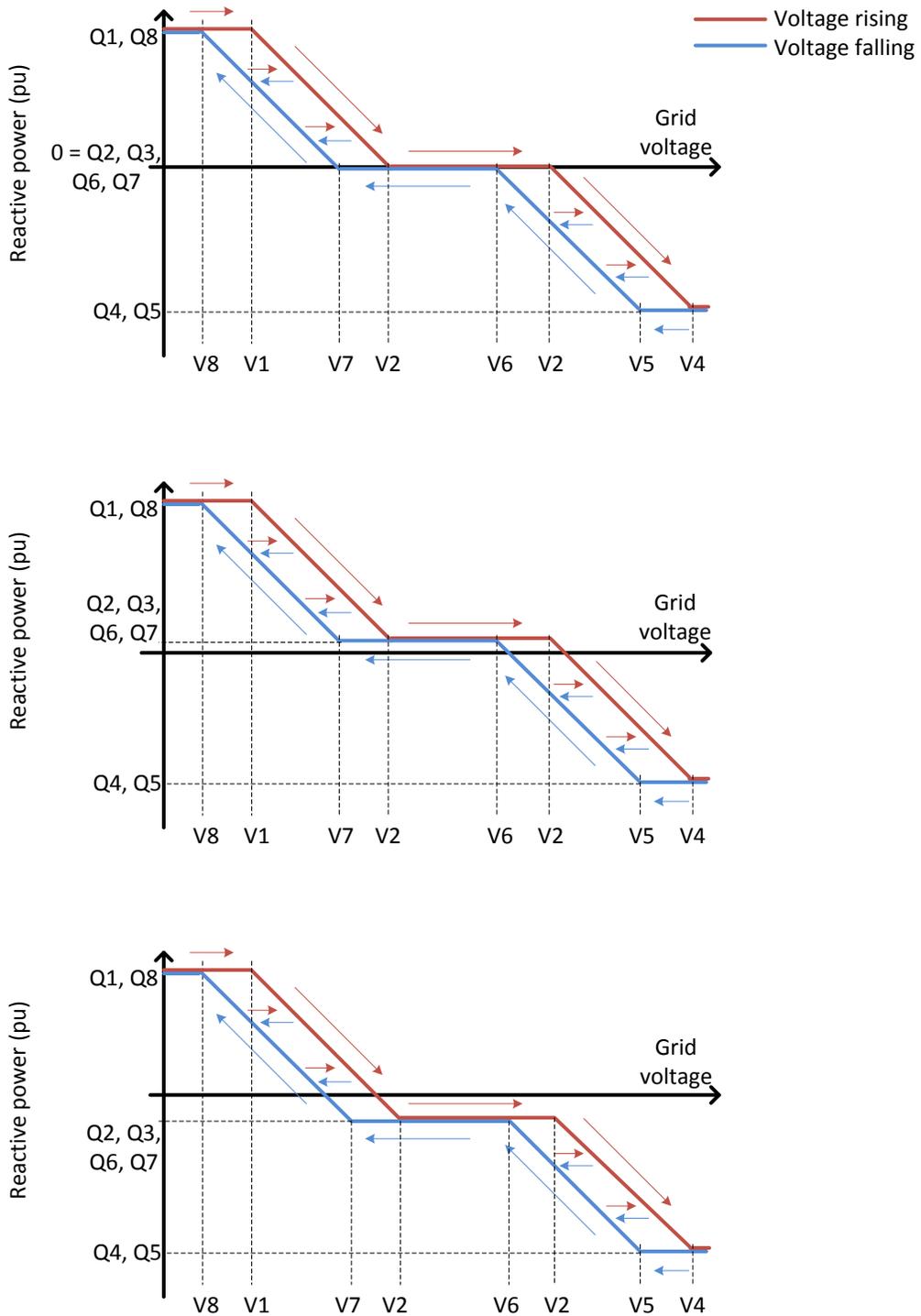


**Figure C2. Q(V) characteristic 2 for volt-VAR test: deadband, no hysteresis. Three versions are shown to clarify that in general the deadband may fall at nonzero Q. When inverter current lags voltage, the sign of Q is positive, as defined in footnote 37.**



**Figure C3. Q(V) characteristic 3 for volt-VAR test: hysteresis, no deadband. When inverter current lags voltage, the sign of Q is positive, as defined in footnote 37.**

### Characteristic 4



**Figure C4. Q(V) characteristic 4 for volt-VAR test: hysteresis and deadband. Three versions are shown to clarify that in general the deadband may fall at nonzero Q. When inverter current lags voltage, the sign of Q is positive, as defined in footnote 37.**

- a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
- b) Set all source parameters to the nominal operating conditions for the EUT.
- c) Set all EUT parameters to the nominal operating settings (or verify that this is the case). Set the EUT to provide reactive power according to Q(V) characteristic 1, with Q1 equal to the manufacturer's maximum capacitive reactive power, V1 equal to 92% of the nominal voltage, Q2 equal to the manufacturer's maximum inductive reactive power, and V2 equal to 108% of the nominal voltage. Turn off any volt-VAR timeout window function. If the volt-VAR function incorporates a maximum VAR ramp rate parameter, set it to the manufacturer's maximum setting. If the volt-VAR function has an *adjustment time* parameter specifying how quickly the inverter must track the Q(V) characteristic, set it to the fastest allowed time.

*Inverter manufacturers have different parameters affecting the rate of change of reactive power. It may be preferable to write this test in a more general manner to accommodate this variation.*

- d) Set all overvoltage settings and clearing times to their maximum values. Set all undervoltage settings to their minimum values, and set associated clearing times to their maximum values. Set all voltage ride-through settings as far from the nominal voltage as possible, and set all voltage ride-through times to their maximum values.<sup>39</sup>
- e) If the EUT is capable of confirming via communications that new volt-VAR settings have been entered, verify that the EUT communicates this correctly. (*Skip this step if not testing interactions with communications.*)
- f) Record applicable settings.
- g) Begin recording synchronized EUT reactive power output and voltage at a 10 Hz or greater sampling rate. Control the source to follow the voltage versus time (V(t)) profile shown in Figure V1. Ramp up the source voltage to 109% of its nominal value at a rate of 5 percentage points per minute or 50% of the maximum ramp rate, whichever is slower. Hold the source at that voltage for time  $t_h$ .<sup>40</sup> Ramp the source voltage back down to 90% of nominal at a rate of 5 percentage points per minute. Ramp the source voltage back up to nominal at a rate of 5 percentage points per minute. End recording of EUT reactive power output. During subsequent repetitions of this step, details will vary, following the appropriate figure (from Figure P1 through P16) for the characteristic under test and the test number, as specified in Tables C1–C4.
- h) If the EUT ceased exporting reactive power during step g) due to the timeout window setting, record the time that reactive power output ceased and repeat step g) with the timeout setting removed.
- i) Set source voltage to the nominal voltage for the EUT and hold until EUT output stabilizes. Begin recording EUT voltage and current at a sampling rate of at least 150 samples per line cycle. Step the source voltage to 110% of nominal in two line cycles or

<sup>39</sup> The intent of this step is to create as large an operating region as possible in both voltage and time dimensions to facilitate testing of volt-VAR functions.

<sup>40</sup> Time  $t_h$  shall be long enough for the reactive power output to stabilize.

less and hold until the EUT output stabilizes. Step the source voltage to 90% of nominal in two line cycles or less and hold until the EUT output stabilizes. Step the source voltage to 100% of nominal and hold until the EUT output stabilizes. Stop recording EUT voltage and current after the output stabilizes.

*This step is meant to verify EUT dynamic response.*

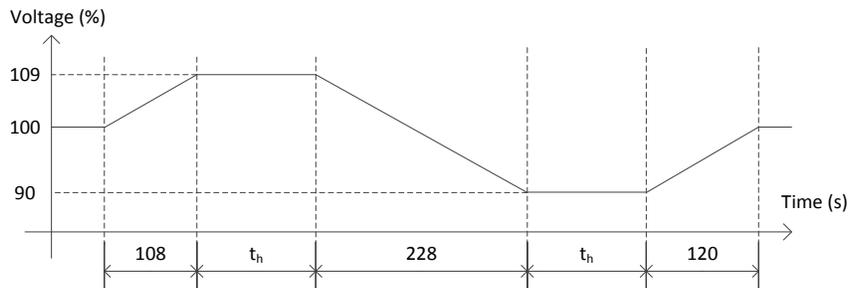
- j) Repeat steps f) through i) seven times for a total of eight tests, varying the V(t) profile and other test parameters as shown in the appropriate table selected from Tables C1 through C4. Qx and Vx parameters in Tables C1–C4 are as defined in Figures C1–C4.

*As currently designed, this test specifies voltage profiles in order to test each volt-VAR characteristic. There will be 16 figures to describe these V(t) test profiles for all four characteristics. Two of those figures are shown here for illustrative purposes. Alternatively, it may be preferable to allow manufacturers to specify voltage profiles for certification, perhaps in coordination with the tester.*

**Table C1. Volt-VAR Parameters for Characteristic 1**

Test #	V1 <sup>41</sup>	Q1 <sup>42</sup>	V2 <sup>41</sup>	Q2 <sup>42</sup>	Timeout (s)	Ramp Rate / Adjustment Time <sup>43</sup>	V(t) Test Profile Figure #
1-2	92	100	108	-100	None	Max / Min	P1
3-4	94	80	102	-80	300	Max / Min	P2
5-6	82	30	118	-50	0	Min / Max	P3
7-8	97	100	103	-100	Mfr min	Min / Max	P4

Tests 3 and 4 are designed to be asymmetrical with respect to voltage. Tests 5 and 6 are designed to be asymmetrical with respect to reactive power. If the EUT does not accept either or both types of V(Q) settings, the test shall be modified accordingly.

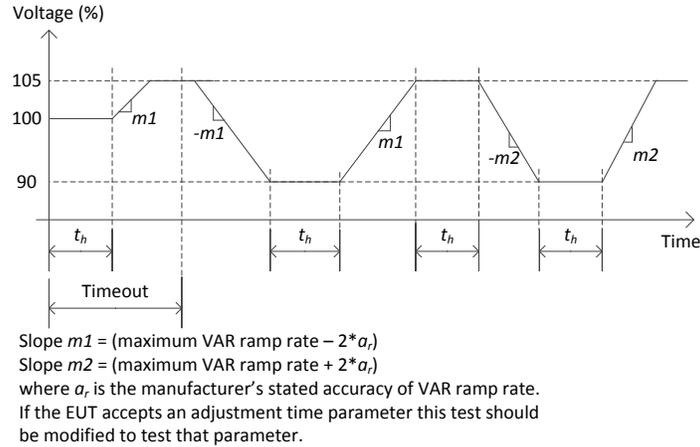


**Figure P1. Voltage versus time profile for Q(V) characteristic 1, tests 1 and 2.**

<sup>41</sup> As a percentage of nominal voltage.

<sup>42</sup> As a percentage of maximum reactive power. Positive sign signifies capacitive power; negative sign signifies inductive power.

<sup>43</sup> “Ramp rate” refers to the maximum absolute change in reactive power in percentage points per second. “Adjustment time” refers to the time between a change in voltage and the moment the reactive power settles to the corresponding level within the manufacturer’s stated accuracy of reactive power. In Tables V1–V4, both are specified with respect to the manufacturer’s stated range for the parameter. Because both ramp rate and adjustment time may affect the maximum rate at which a Q(V) setting can be tracked, this test assumes the EUT does not accept both parameters.



**Figure P2. Voltage versus time profile for Q(V) characteristic 1, tests 3 and 4.**

The idea behind the voltage profile in Figure P2 is to first test the timeout window, then per step h) go back and run the complete test profile, which is designed to test the inverter near its maximum VAR ramp rate.

Figures P1 and P2 show two of the 16 voltage profiles that should eventually be included. Alternatively, the test plan could require the manufacturer and/or the tester to specify the voltage profiles. In that case, the test plan may want to supply guidance.

**Table C2. Volt-VAR Parameters for Characteristic 2**

Test #	V1 <sup>44</sup>	Q1 <sub>45</sub>	V2 <sup>44</sup>	Q2 <sup>45</sup>	V3 <sup>44</sup>	Q3 <sup>45</sup>	V4 <sup>44</sup>	Q4 <sup>45</sup>	Timeout (s)	RR / AT <sup>46</sup>	V(t) Test Profile
1-2	92	100	99	0	101	0	108	-100	None	Max / Min	P5
3-4	94	80	96	0	99	0	102	-80	600	Max / Min	P6
5-6	82	30	97	10	103	10	118	-50	0	Min / Max	P7
7-8	97	100	99	0	101	0	103	-100	Mfr min	Min / Max	P8

Tests 3 and 4 are designed to have deadbands not centered on nominal voltage. Tests 5 and 6 are designed to have nonzero reactive power in the deadband. Not all inverters accept these types of Q(V) characteristics. For inverters that do not, the tester should design an alternative Q(V) curve.

<sup>44</sup> As a percentage of nominal voltage.

<sup>45</sup> As a percentage of maximum reactive power. Positive sign signifies capacitive power; negative sign signifies inductive power.

<sup>46</sup> RR (ramp rate) refers to the maximum absolute change in reactive power in percentage points per second. AT (adjustment time) refers to the time between a change in voltage and the moment the reactive power settles to the corresponding level within the manufacturer's stated accuracy of reactive power. In Tables V1–V4, both are specified with respect to the manufacturer's stated range for the parameter. Because both ramp rate and adjustment time may affect the maximum rate at which a Q(V) setting can be tracked, this test assumes the EUT does not accept both parameters.

**Table C3. Volt-VAR Parameters for Characteristic 3**

Test #	V1 <sup>47</sup>	Q1 <sup>48</sup>	V2 <sup>48</sup>	Q2 <sup>45</sup>	V3 <sup>47</sup>	Q3 <sup>45</sup>	V4 <sup>47</sup>	Q4 <sup>48</sup>	Timeout (s)	RR / AT <sup>49</sup>	V(t) Test Profile
1-2	99	100	108	-100	101	-100	92	100	None	Max / Min	P9
3-4	99	80	102	-80	96	-80	94	80	600	Max / Min	P10
5-6	90	30	108	-50	100	-50	82	30	0	Min / Max	P11
7-8	99	100	103	-100	101	-100	97	100	Mfr min	Min / Max	P12

*Tests 3 and 4 are designed to have hysteresis not centered on nominal voltage. Tests 5 and 6 are designed to have a Q(V) characteristic not centered around zero reactive power. Not all inverters accept these types of Q(V) characteristics. For inverters that do not, the tester should design an alternative Q(V) curve.*

**Table C4. Volt-VAR Parameters for Characteristic 4**

Test #	V1 <sup>50</sup>	Q1, Q8 <sup>51</sup>	V2 <sup>50</sup>	Q2, Q3, Q6, Q7 <sup>51</sup>	V3 <sup>50</sup>	Q4, Q5 <sup>51</sup>	V4 <sup>50</sup>	V5 <sup>50</sup>	V6 <sup>50</sup>	V7 <sup>50</sup>	V8 <sup>50</sup>	Timeout (s)	RR / AT <sup>52</sup>	V(t) Test Profile
1-2	92	100	97	0	108	-100	113	108	103	92	87	None	Max / Min	P13
3-4	92	80	96	0	102	-80	106	104	100	94	90	600	Max / Min	P14
5-6	91	30	96	-10	103	-50	108	102	97	90	85	0	Min / Max	P15
7-8	97	100	99	0	103	-100	105	103	101	97	95	Mfr min	Min / Max	P16

- k) Repeat steps c) through j) for each of the four Q(V) characteristics.
- l) If EUT parameters can be changed via more than one communications means, repeat steps c) through k) using each remaining communications means.<sup>53</sup> (*Skip this step if not testing interactions with communications.*)

<sup>47</sup> As a percentage of nominal voltage.

<sup>48</sup> As a percentage of maximum reactive power. Positive sign signifies capacitive power; negative sign signifies inductive power.

<sup>49</sup> RR (ramp rate) refers to the maximum absolute change in reactive power in percentage points per second. AT (adjustment time) refers to the time between a change in voltage and the moment the reactive power settles to the corresponding level within the manufacturer’s stated accuracy of reactive power. In Tables V1–V4, both are specified with respect to the manufacturer’s stated range for the parameter. Because both ramp rate and adjustment time may affect the maximum rate at which a Q(V) setting can be tracked, this test assumes the EUT does not accept both parameters.

<sup>50</sup> As a percentage of nominal voltage.

<sup>51</sup> As a percentage of maximum reactive power. Positive sign signifies capacitive power; negative sign signifies inductive power.

<sup>52</sup> RR (ramp rate) refers to the maximum absolute change in reactive power in percentage points per second. AT (adjustment time) refers to the time between a change in voltage and the moment the reactive power settles to the corresponding level within the manufacturer’s stated accuracy of reactive power. In Tables V1–V4, both are specified with respect to the manufacturer’s stated range for the parameter. Because both ramp rate and adjustment time may affect the maximum rate at which a Q(V) setting can be tracked, this test assumes the EUT does not accept both parameters.

<sup>53</sup> See footnote 6.

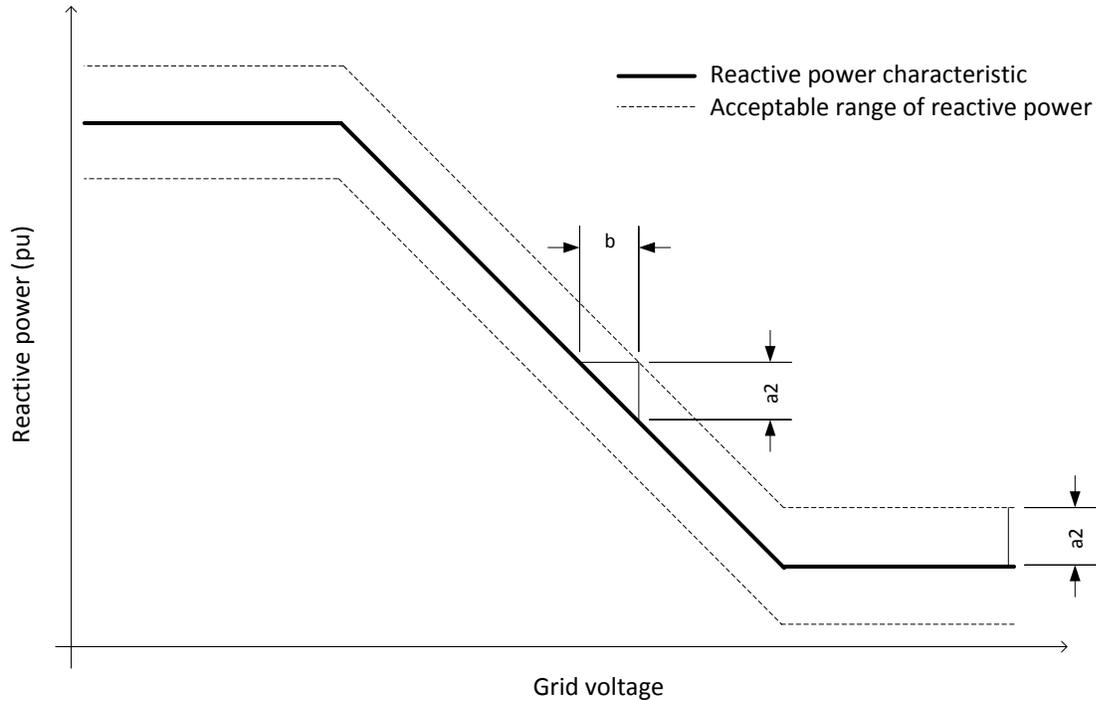
### **2.6.3 Requirements**

If used, the simulated area EPS shall meet the requirements of clause 4.6.1 of IEEE Std 1547.1. The measurement system shall meet the requirements of clause 4.6.2 of IEEE Std 1547.1.

### **2.6.4 Criteria**

The EUT shall be considered in compliance if all of the following criteria are true at all times during all tests:

- a) Reactive power output tracks the Q(V) characteristic within the accuracy defined in Figure V2, except when constrained by one of the following:
  - i. Reactive power ramp rate limit; this may be an adjustable EUT parameter or a fixed value defined by the manufacturer
  - ii. Q(V) adjustment time setting
  - iii. Timeout window.
- b) Reactive power does not change faster than the specified ramp rate, if applicable.
- c) Reactive power adjusts to appropriate settings in exactly the specified adjustment time within the manufacturer's stated accuracy, if applicable.
- d) Reactive power output ceases after the timeout window has passed, if applicable.
- e) Reactive power output following step changes in voltage conforms to the manufacturer's stated maximum rise time, settling time, overshoot values.



$$b = a1 + n$$

$n$  = maximum amplitude of noise on RMS voltage measurement

$a1$  = manufacturer's stated accuracy of voltage

$a2$  = manufacturer's stated accuracy of reactive power

**Figure V1. Acceptable range of measured reactive power, relative to a programmed  $Q(V)$  characteristic.**

*Testing described below found that the noise on the RMS voltage measurement was the dominant factor in producing measurements away from the commanded  $Q(V)$  characteristic. That is why this parameter is included in the test criteria. As in IEEE Std 1547.1, measurement accuracy must also be accounted for by the tester.*

## 2.7 Test for Frequency Response Capability

*Many advanced inverters can support grid frequency, typically by modulating power output in response to changes in frequency. A test for this behavior is not yet included here. Nevertheless, some preliminary test results for this function are included in this report.*

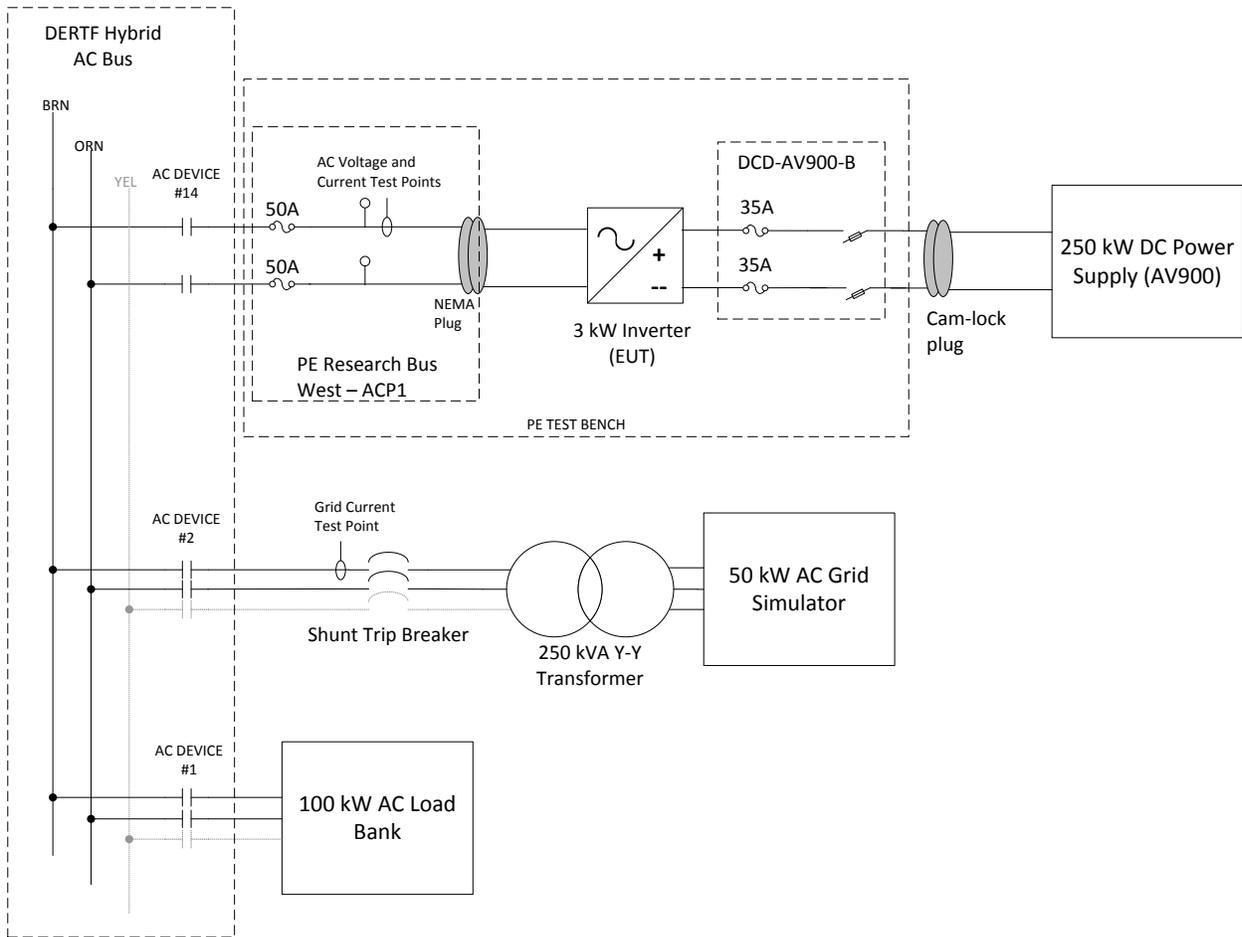
## 3 Test Results

Two DERs were tested at NREL in order to evaluate this preliminary test plan. One was a commercially available single-phase 3-kW advanced photovoltaic inverter. The other was a prototype 3-phase 50 kW inverter developed at NREL. A subset of the above tests was performed. A summary of the results of those tests is included here.

### 3.1 Single-Phase Inverter Tests

The single-phase 3-kW inverter was a commercially available string inverter that provides advanced grid support capabilities. These tests were performed before complete manufacturer documentation of the advanced features was available. Hence, the test results summarized below are preliminary only, and should not be taken as definitive. Features tested were multi-level voltage trip settings, multi-level frequency trip settings, anti-islanding, volt-VAR control (voltage regulation), and high-frequency power curtailment.

The test setup used is shown in Figure S0. A 50-kW Pacific Power programmable AC supply and a 100-kW AC load bank were used as the simulated EPS. A 250-kW AV900 DC power supply was used to power the inverter. The nominal grid voltage was 240 V AC, and the nominal DC voltage was 250 V DC. Communication between the inverter and a control PC was established through an RS-485 card in the inverter using inverter manufacturer's proprietary communication protocol. The communication appears to work well, but it is not fully supported or documented.



**Figure S0. Single-phase inverter test setup.**

It should be noted that these tests were performed in a research laboratory environment and not in a certified testing laboratory. While care was taken to achieve accurate and repeatable results, these results should not be interpreted as definitive or valid for any certification purpose.

The anti-islanding test was performed using a power hardware-in-the-loop (PHIL) method to simulate the resonant load condition required for this test (Lundstrom 2013). This method was very recently developed and would not yet be acceptable for certification purposes.

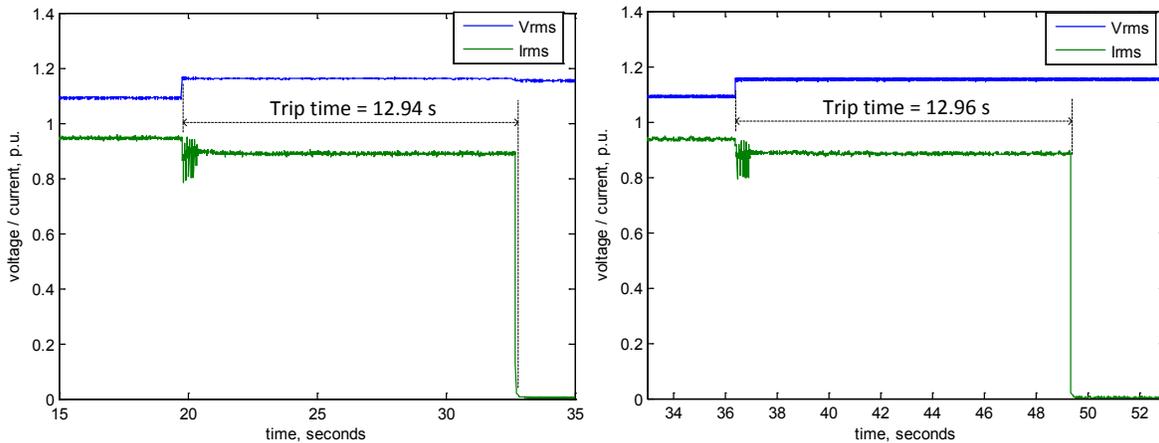
### 3.1.1 Abnormal Voltage Disconnection Test Results

The inverter includes two adjustable undervoltage and three adjustable overvoltage trip settings with adjustable clearing times. One of the overvoltage settings is intended for hardware protection rather than grid interconnection compliance and hence was not tested. Voltage time and magnitude tests were performed both with and without the volt-VAR function running to test for any interaction between the two functions.

Table S1 shows abnormal voltage trip times for each of the settings tested. Each test shown was performed once. The inverter passed all voltage trip time tests, both with volt-VAR running and without. Figure S1 shows plots of RMS inverter voltage and current during two typical trip time tests, both at the 110% voltage level, one without volt-VAR control running (left) and one with it running (right). No differences attributable to volt-VAR control were observed.

**Table S1. Voltage Trip Time Tests**

Volt-VAR Setting	Voltage Trip Setting (%)	Trip Time Setting (s)	Measured Trip Time (s)	Result
Off	60	0.16	0.13	Pass
	88	10	9.96	Pass
	110	13	12.94	Pass
	120	0.16	0.13	Pass
Q(V) Characteristic 2, Test 1-2 Settings	60	0.16	0.13	Pass
	88	10	9.96	Pass
	110	13	12.96	Pass
	120	0.16	0.13	Pass



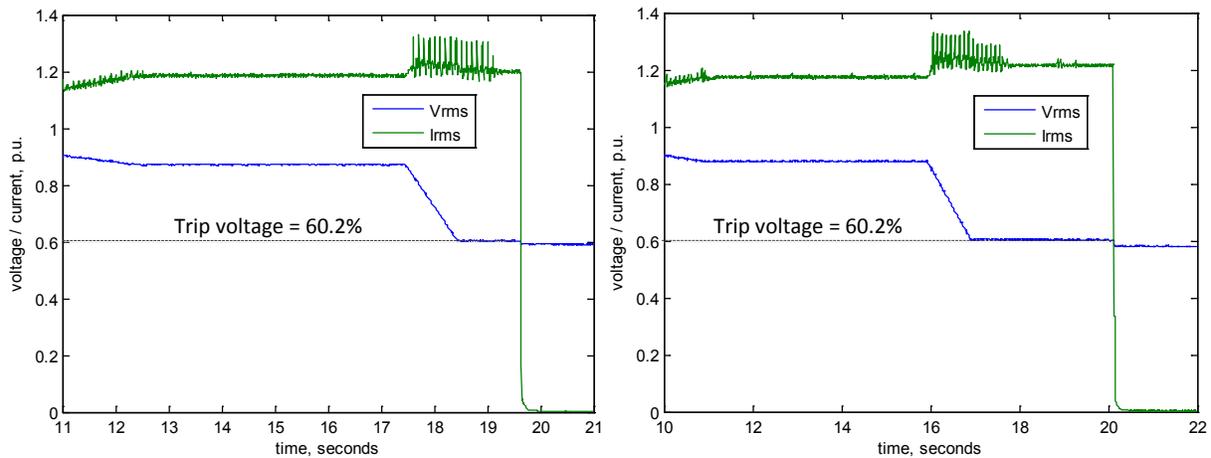
**Figure S1. Inverter RMS voltage and current during voltage time tests without (left) and with (right) volt-VAR running.**

Table S2 shows the results of voltage magnitude tests. Some tests were performed twice. The inverter passed all tests, with and without volt-VAR control running. Figure S2 shows inverter RMS current and voltage during two typical voltage magnitude tests, both with 60% voltage trip setting, one without volt-VAR running (left) and one with volt-VAR running (right). Note that the steep voltage ramp serves simply to adjust the voltage to  $V_b$ , the holding voltage; the test ramp occurs later and is nearly imperceptible on this scale.<sup>54</sup> No differences attributable to the presence of volt-VAR control were observed.

<sup>54</sup> Simply stepping the voltage to  $V_b$  can cause tripping due to the transient response. A similar ramp to get to  $V_b$  is used in subsequent tests as well. The exact method of getting to  $V_b$  can be determined by the tester.

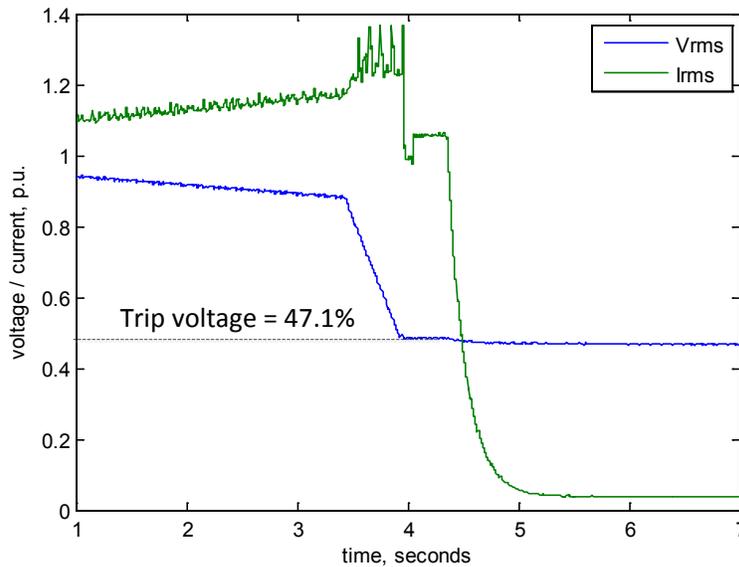
**Table S2. Voltage Trip Magnitude Tests**

Volt-VAR Setting	Voltage Trip Setting (%)	Trip Time Setting (s)	Measured Trip Voltage (%)	Result
Off	60	0.16	60.32	Pass
	60	0.16	60.2	Pass
	88	10	88.27	Pass
	110	13	109.56	Pass
	120	0.16	119.35	Pass
Q(V) Characteristic 2, Test 1-2 Settings	45	0.16	47.1	Pass*
	60	0.16	60.2	Pass
	60	0.16	60.2	Pass
	88	10	88.2	Pass
	110	13	109.6	Pass
	120	0.16	119.6	Pass



**Figure S2. Inverter RMS voltage and current during voltage magnitude tests without (left) and with (right) volt-VAR running.**

In all but one test, the inverter tripped within one-half percentage point of the designated trip voltage. The exception was the test at 45% voltage (marked by \*), where it tripped about two percentage points above the trip magnitude setting, still passing the test because it tripped above the setting rather than below it. A plot of RMS inverter voltage and current for this case is shown in Figure S3. Note that the current tails off somewhat slowly rather than dropping off abruptly as in Figure S2. In all other cases, the current dropped off abruptly. Further testing would be needed to determine why the 45% case was different. Nevertheless, the inverter passed this test.



**Figure S3. Inverter RMS voltage and current during an undervoltage magnitude test with a 45% trip setting. This result was unusual in that the current tailed off slowly.**

The volt-VAR function was not observed to affect the results of the voltage disconnect function tests.

The inverter does not provide voltage ride-through settings. However, during testing the inverter always tripped within 0.03 to 0.06 seconds (two to four line cycles) of the clearing time setting. Likewise, the trip magnitude was within one-half percentage point of the setting in all but one case (which would need to be investigated further to determine whether the anomaly was the fault of the inverter or of some other component of the test apparatus). Given these very accurate trip times, EPS and DER operators may feel that separate ride-through settings are not necessary because the inverter consistently remains connected until just before the clearing magnitude and time settings. For example, a trip setting of 10 seconds and 88% could be interpreted to include an implied ride-through setting of 9.4 seconds and 88.5%, assuming further testing confirms this observation.

### 3.1.2 Abnormal Frequency Disconnection Test Results

The inverter includes two adjustable overfrequency trip settings and two adjustable underfrequency trip settings, both with adjustable clearing times. These settings were tested both with and without the high-frequency power curtailment function running to test for any interaction between the two functions. (High-frequency power curtailment is a type of frequency response in which the inverter curtails active power at high frequencies in order to counteract the frequency rise.) These tests were also performed both with and without volt-VAR control running, although this is not required by the test plan.

Table S3 shows the results of frequency trip time tests. The inverter passed all tests.

It is interesting to note that in all cases, the inverter tripped when 90% of the clearing time had passed (minus one to four line cycles). This contrasts with the voltage time tests, where the

inverter always tripped at exactly the designated trip time (minus one to four line cycles). It appears the manufacturer may have intentionally built in a greater margin for error in the frequency trip setting. Nevertheless, the trip time appears to be very consistent once the 90% pattern is recognized.

**Table S3. Frequency Trip Time Tests**

Frequency Response Setting	Volt-VAR Setting	Frequency Trip Setting (Hz)	Trip Time Setting (s)	Measured Trip Time (s)	Result
Off	Q(V) Characteristic 2, <sup>55</sup> Test 1-2 Settings	56	10	8.99	Pass
		58	300	269.91	Pass
		62	90	80.96	Pass
		64	10	8.98	Pass
Off	Off	57	0.16	0.12	Pass
		60.5	0.16	0.11	Pass
		64	2	1.77	Pass
P(f) 20% Slope	Off	64	0.16	0.10	Pass
P(f) 40% Slope		56	0.16	0.12	Pass
P(f) 40% Slope		64	0.16	0.13	Pass

Table S4 shows the results of frequency trip magnitude tests. These tests were performed both with and without the high-frequency power curtailment function running. The manufacturer’s stated accuracy of frequency is not known, but assuming the manufacturer does not claim a frequency accuracy of less than 0.02 Hz, the inverter passed all tests.<sup>56</sup> It is worth noting, however, that in two of the four overfrequency tests (marked by \*) the inverter tripped just above the frequency trip setting, rather than just below it as expected. These tests were only performed once each, so these mildly anomalous results should not be taken to reflect poorly on the inverter. It is also possible that some systematic error in the test procedure or measurements led to these results; these tests would need to be repeated in a certified test lab for verification.

**Table S4. Frequency Trip Magnitude Tests**

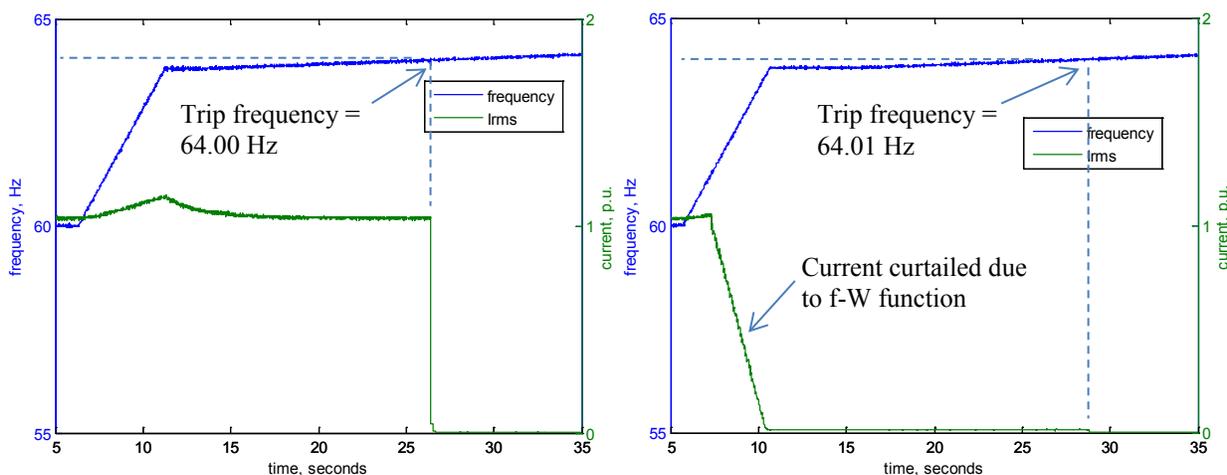
Frequency Response Setting	Volt-VAR Setting	Frequency Trip Setting (Hz)	Trip Time Setting (s)	Measured Trip Freq. (Hz)	Result
Off	Off	56	0.16	56.01	Pass
		58	10	58.00	Pass
		62	10	62.02	Pass*
		64	0.16	64.00	Pass
P(f) 20% Slope	Off	64	0.16	64.01	Pass*
P(f) 40% Slope		64	0.16	64.00	Pass

<sup>55</sup> Recall that under Q(V) characteristic 2, the inverter performs volt-VAR control following a Q(V) curve with a deadband.

<sup>56</sup> For the purposes of the magnitude ramps, the manufacturer’s accuracy of frequency was taken to be 0.01 Hz because this is the smallest frequency difference that the inverter registers when setting frequency parameters. However, this was not officially stated by the manufacturer.

Note that the trip times used for these tests are much shorter than the trip times used for the frequency time tests. This is because the slope of the frequency ramp function is inversely proportional to the trip time setting, so high trip times lead to very slow ramps and unreasonably long tests. For example, if the trip time is 300 seconds and the manufacturer's accuracy of frequency is 0.01 Hz, then the slope of the frequency ramp is  $(0.5 \cdot 0.01) / (2 \cdot 300) = 8.3 \times 10^{-6}$  Hz/s. At this rate, the ramp would require over 13 hours to change the frequency by 0.4 Hz. For this reason, smaller trip times were used. This should not affect the accuracy of the magnitude tests.

In one of the frequency trip magnitude tests, the high-frequency power curtailment function was tuned so that nearly zero current was flowing from the inverter when the frequency magnitude setting was reached. This was the test with P(f) slope of 20%. The frequency and RMS inverter current from this test are shown in Figure S4, along with a more typical magnitude test for comparison. Even when tuned in this manner, the high-frequency power curtailment function had no observable effect on the trip magnitude.<sup>57</sup> The same was true of all tests: no effect was observed when running frequency trip tests with high-frequency power curtailment on.



**Figure S4. Inverter RMS frequency and current during two overfrequency magnitude tests. On the left is a test without high-frequency power curtailment enabled. On the right is a test where high-frequency power curtailment is enabled and is tuned so the inverter output current is nearly zero when the trip frequency is reached. Note that the effect on the trip frequency was negligible. The rise in current during the frequency ramp in the test on the left is unexpected, and is due to the inverter absorbing reactive power. This behavior merits further investigation.**

As with voltage, the inverter does not provide an explicit frequency ride-through setting. However, the frequency trip times and magnitudes are very consistent, so it may be acceptable to EPS and EUT operators to interpret the frequency trip settings as containing implied frequency ride-through settings. For instance, a trip setting of 62 Hz and 10 seconds could be interpreted to imply a ride-through setting of 61.98 Hz and 8.94 seconds. It may in fact be preferable to have a single simple, reliable, and accurate group of settings for both frequency disconnection and frequency ride-through, rather than two independent groups of settings.

<sup>57</sup> The trip times for these two tests differ by 0.01 Hz, which is within the uncertainty margin of the measurement.

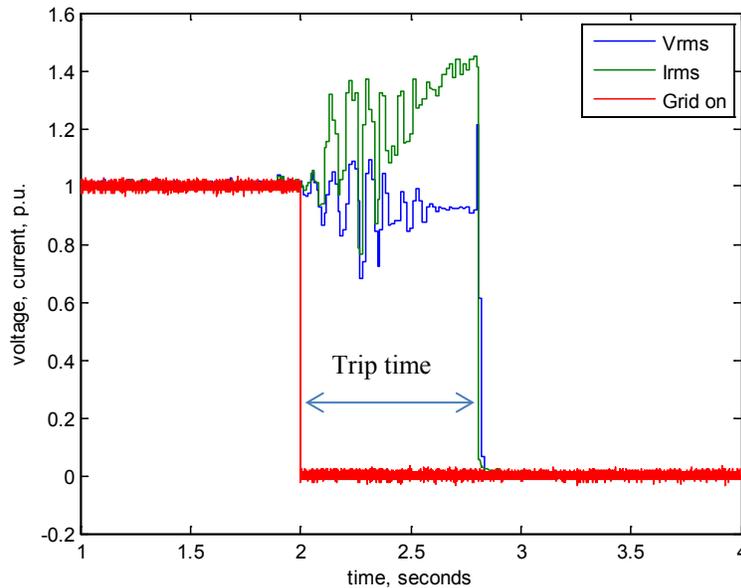
### 3.1.3 Unintentional Islanding Test Results

The inverter’s unintentional island disconnection feature was tested using a PHIL system to create a resonant island condition through real-time PHIL control of the grid simulator using the method described in Lundstrom (2013). Tests were conducted to confirm the inverter’s ability to disconnect upon the formation of an island while also performing various combinations of volt- VAR control, high-frequency power curtailment, and frequency and voltage ride-through. While explicit frequency and voltage ride-through settings are not available, the inverter does accept long voltage and frequency trip times, and consistently trips a small and predictable time margin before those trip times, as noted above. Therefore, for the purposes of the islanding tests, voltage and frequency trip parameters set to their maximum values were considered to be equivalent to voltage and frequency ride-through. Note that the tests presented here do not represent steps mentioned in the full anti-islanding test procedure as given in IEEE Std 1547.1.

Table A1 summarizes the results of the nine islanding tests performed. Some tests were repeated after re-tuning the simulated resonant load. The inverter passed all tests. Trip times, which must be under 2 seconds, varied from 0.174 seconds to 1.126 seconds. Much of the variation in trip time appeared to be due to how well the resonant circuit was tuned rather than which advanced inverter features were running. However, it does appear that the trip times are somewhat longer (but still within the acceptable range) when frequency ride-through is running. Further testing would be needed to confirm this. Figure A2 shows one example plot of RMS inverter voltage and current during an islanding test. A binary signal indicating whether the grid is present or islanded is also shown.

**Table A1. Islanding Tests**

<b>Voltage Ride-Through</b>	<b>Frequency Ride-Through</b>	<b>Volt-VAR Control</b>	<b>High-Frequency Power Curtailment</b>	<b>Measured Trip Time (s)</b>	<b>Result</b>
Off	Off	Off	Off	0.174	Pass
On	On	Off	Off	0.738	Pass
On	On	Off	Off	1.094	Pass
On	On	Off	Off	1.084	Pass
On	On	Off	Off	1.126	Pass
On	On	On	Off	0.679	Pass
On	On	On	Off	0.831	Pass
On	On	On	On	0.284	Pass
On	On	On	On	1.042	Pass



**Figure A1. Inverter RMS voltage and current during an islanding test with four advanced grid support features running: voltage ride-through, frequency ride-through, volt-VAR control, and high-frequency power curtailment. The trip time in this test is about 0.8 seconds.**

### 3.1.4 Volt-VAR Test Results

The inverter is capable of adjusting its reactive power output as a function of voltage (volt-VAR control). It can do so following a Q(V) characteristic with or without deadband or hysteresis, but the characteristic cannot have both deadband and hysteresis. Hence, it can perform characteristic 1 (no deadband or hysteresis), characteristic 2 (deadband), and characteristic 3 (hysteresis) as defined in the volt-VAR test section. Test results for these three characteristics are summarized below.

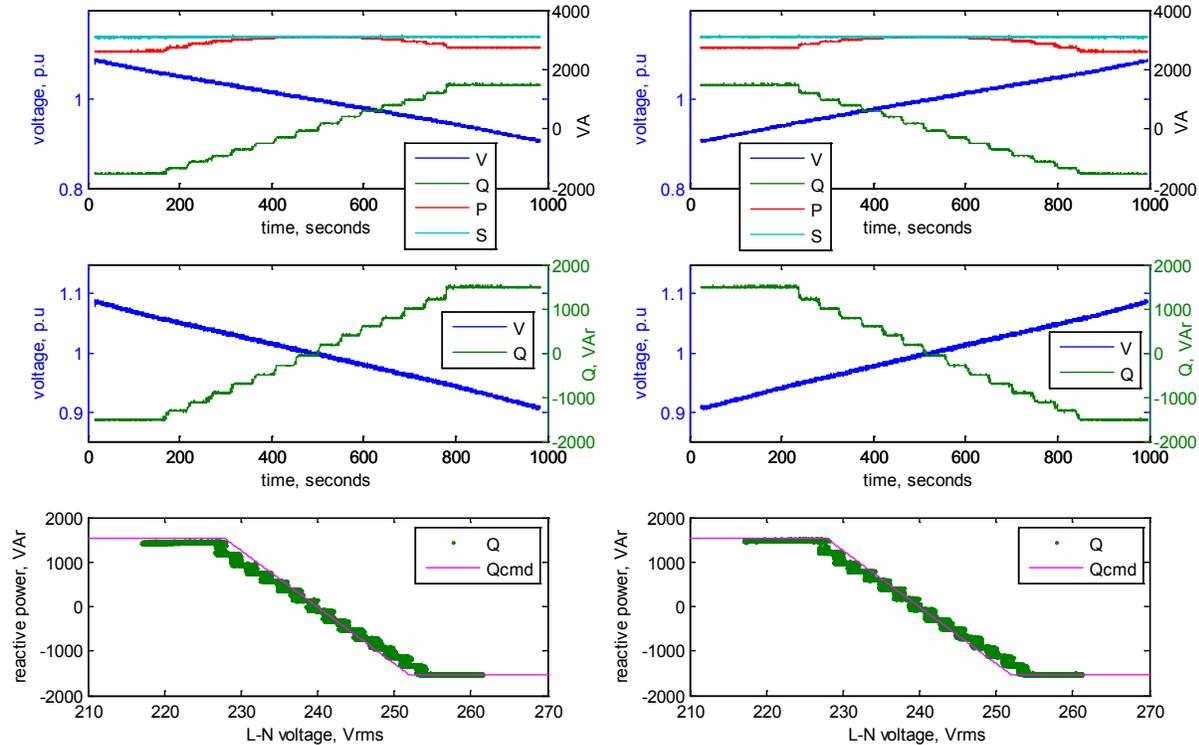
The volt-VAR control function is designed to have relatively slow dynamics; it accepts an *adjustment time* parameter in the range of 2 seconds to 100 seconds. This parameter defines how fast the reactive power reaches the commanded Q(V) characteristic after a change in voltage. Unless otherwise indicated, all of the tests below were performed with the volt-VAR adjustment time set to 2 seconds.

Recall that reactive power is defined here using the generator reference frame, with exportation of reactive power (i.e., inverter current lagging inverter voltage) corresponding to positive Q.

Plots of the results of Q(V) characteristic 1,<sup>58</sup> test 1, are shown in Figure S5. The test was divided into two segments because the measurement system's maximum time window is 1,000 seconds. The top plots show apparent and real power in addition to reactive power. Note that the inverter curtails active power in order to meet the V(Q) command without exceeding its apparent power limit. This is likely a reflection of internal inverter device current limits. Also note that the

<sup>58</sup> Q(V) characteristic 1 is a simple volt-VAR characteristic with no deadband or hysteresis, as shown in Figure C1.

reactive power forms a staircase function rather than a straight ramp. This is presumably because the inverter uses a discrete array (e.g., a lookup table) of reactive power setpoints internally, rather than a continuous Q(V) function.



**Figure S5. Inverter power and voltage during test 1 of volt-VAR characteristic 1. Qcmd is the Q(V) curve specified by the inverter settings.**

The bottom plots in Figure S5 show measured reactive power as a function of measured voltage, re-creating the Q(V) characteristic. The commanded Q(V) characteristic is shown for comparison. The slope of the measured characteristic visibly deviates from the commanded characteristic. The commanded slope of the Q(V) curve was -7.1, in units of (percentage of maximum real power setting)/(percent of nominal voltage)<sup>59</sup>, and the measured slope is -8.3, in the same units. Other volt-VAR tests for this inverter showed similar discrepancies. Possible explanations include:

- Misunderstanding of the volt-VAR parameters on the part of the test engineer due to lack of documentation
- Errors in the communication of parameters to the inverter, due to use of an unsupported communication protocol

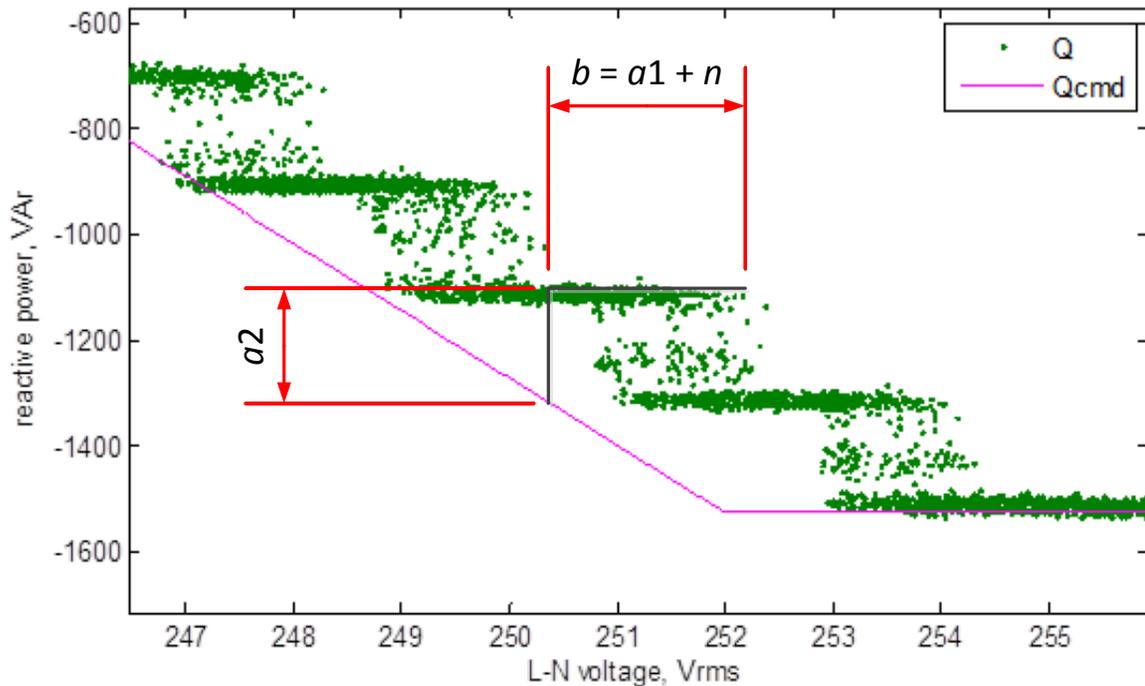
<sup>59</sup> These are the units used by the manufacturer to specify Q(V) slope.

- Unknown manufacturer’s accuracy of reactive power. It is possible that the inverter intentionally does not follow commanded  $Q(V)$  curves with great accuracy and that this is an entirely expected result. This appears to be the most likely explanation, for reasons discussed below.

Hence, it is not possible to say whether the inverter passed this test without more information.

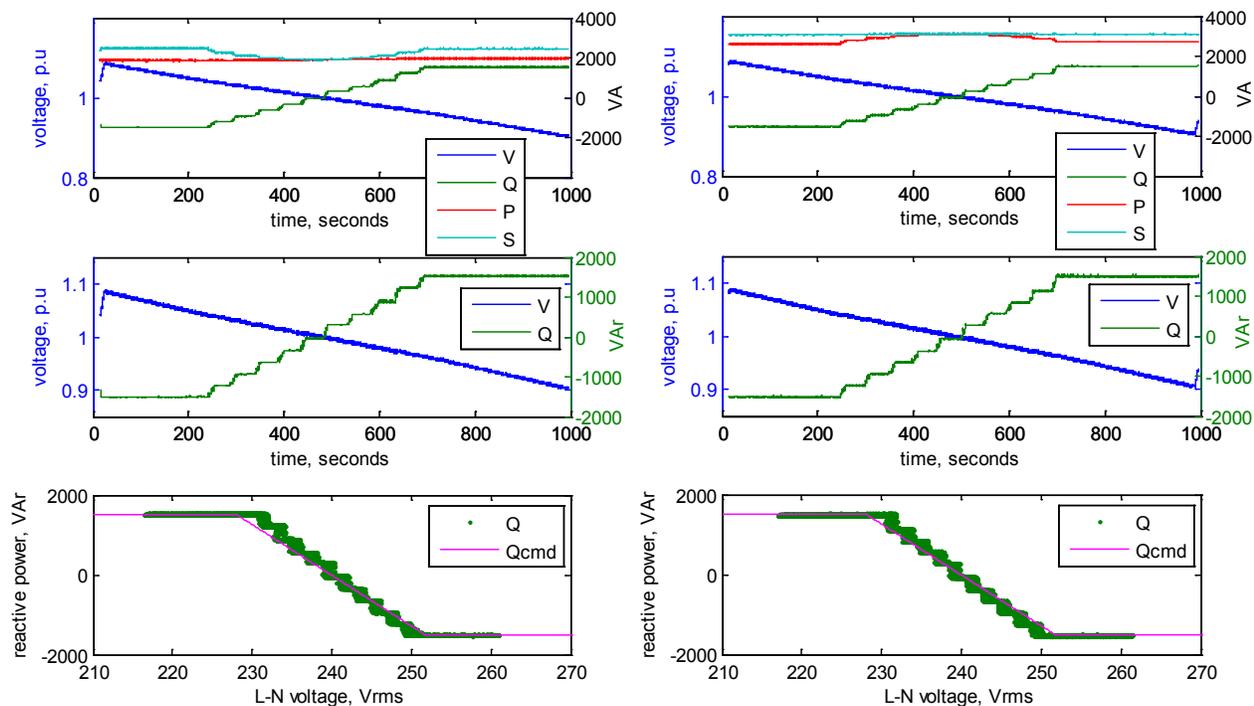
Figure S6 shows a close-up of part of the  $Q(V)$  characteristic from Figure S5. The figure is annotated to show how the manufacturer’s accuracy of voltage ( $a1$ ), the manufacturer’s accuracy of reactive power ( $a2$ ), and the amplitude of noise on the RMS voltage measurement ( $n$ ) can be used to determine whether a measured  $Q(V)$  plot meets the test criteria. Using  $a1 = 0.1$  V and  $n = 1.0$  V, the figure shows that  $a2$  would need to be roughly 200 VAR or more for the inverter to meet the criteria. This is simply for illustrative purposes; the manufacturer’s accuracies are not known.

It is worth noting that the noise on the RMS voltage can be a dominant factor in determining whether an EUT meets the test criteria. The approximately one volt of noise ( $n = 1$  V) present in this test is much larger than the accuracy of voltage parameter  $a1$  for most inverters.



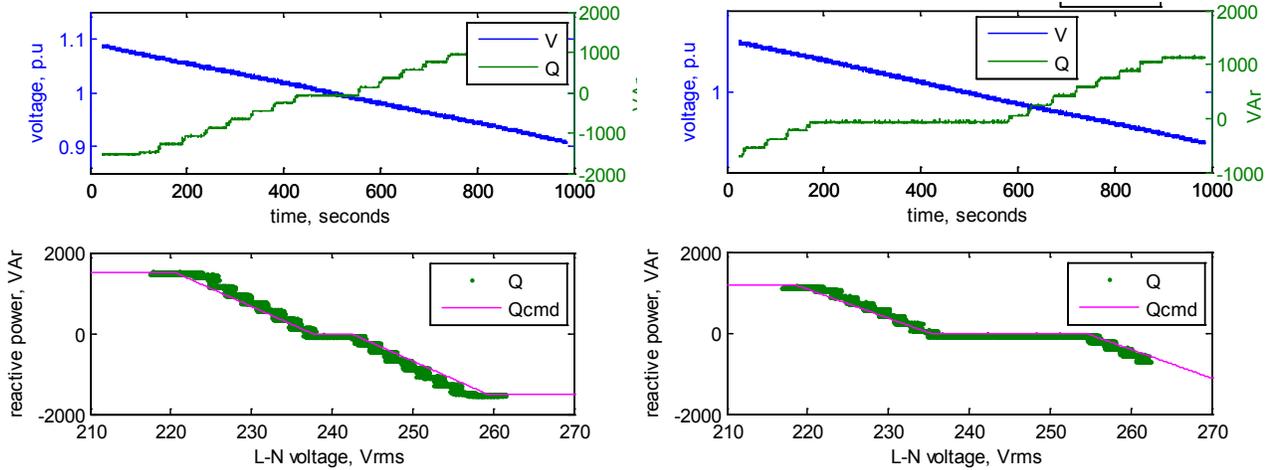
**Figure S6. Close-up of inverter voltage and reactive power during test 1 of volt-VAR characteristic 1, illustrating how the worst-case deviation between commanded and measured  $Q(V)$  can be used to evaluate whether an EUT meets the test criteria.**

Test 7 of characteristic 1 was also performed for this inverter. This test involves a steeper  $Q(V)$  slope. This test was performed both at full power and with the DC input power limited to 2 kW. The results of both tests are shown in Figure S7. In the input power-limited test, note that the real power does not need to curtail to make room for reactive power. This is as expected because apparent power is not constrained in this case. In both of these tests, the slope of the  $Q(V)$  characteristic is again slightly off from the commanded slope. Also note that in this case the measured  $Q(V)$  slope is steeper than the commanded slope, in contrast to Figure S5 where the commanded slope is steeper.



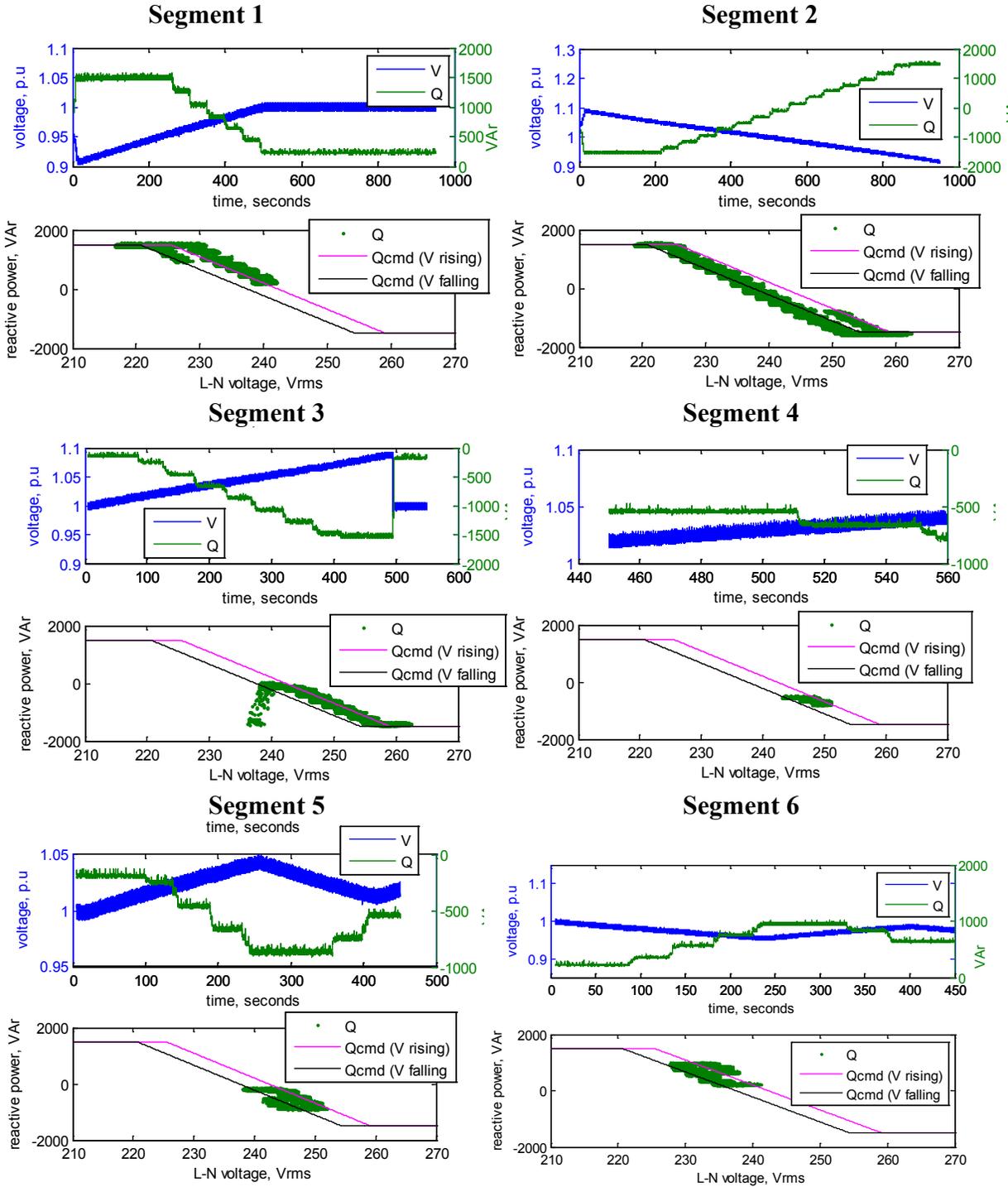
**Figure S7. Inverter voltage and reactive power during test 7 of volt-VAR characteristic 1. On the left is a test with DC input power limited to 2 kW. On the right is a test without DC power limited.**

$Q(V)$  characteristic 2 (deadband) was also tested. Figure S8 shows sample results of tests 1 and 3. The full results from these tests are not shown for brevity; they follow the same trends seen in the sample results. The measured results follow the  $Q(V)$  characteristic well in the deadband regions but deviate slightly when voltage goes away from nominal, as noted above. Test 3 was designed partly to test the inverter's ability to execute a  $Q(V)$  characteristic that is offset with respect to nominal voltage. The inverter does this successfully.



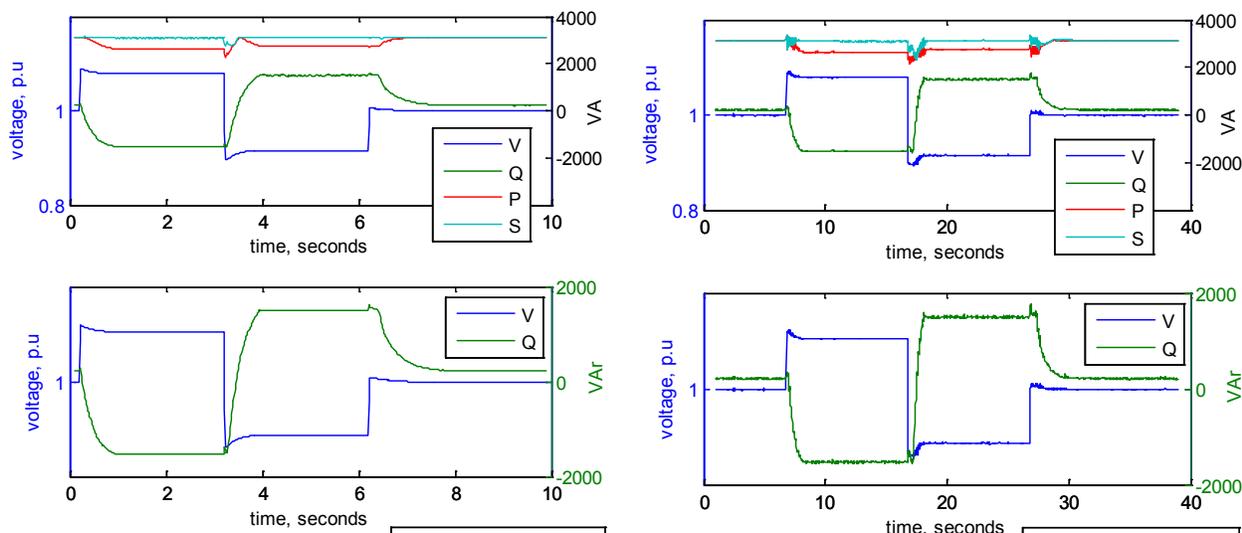
**Figure S8. Inverter voltage and reactive power during tests 1 (left) and 3 (right) of volt-VAR characteristic 2.**

Test 1 of characteristic 3 (hysteresis) is shown in Figure S9. These test results are broken into six segments for plotting purposes. The test included many changes in the direction of the voltage ramp to verify that the reactive power would correctly jump between the rising reactive power characteristic and the falling reactive power characteristic. Aside from the slight deviation from the commanded  $Q(V)$  characteristic at very high and low voltages (as seen in all tests), the reactive power tracks as expected. The reactive power consistently jumps to the appropriate part of the characteristic upon a change in voltage ramp direction. The off-characteristic part of segment 3 is due to a step change in voltage around 500 seconds, which is not part of the test.



**Figure S9. Inverter voltage and reactive power during test 1 of volt-VAR characteristic 3 (hysteresis). This test was divided into six segments so that the correlation between the time plots and Q(V) plots can be seen. Segments 3-6 show that when the direction of the voltage ramp changes at various points in the Q(V) ramp, the inverter correctly switches from the “rising” to the “falling” part of the characteristic (or vice versa).**

The inverter's dynamic response to voltage steps while programmed for Q(V) characteristic 3 (hysteresis) was also tested. Figure S10 shows results of two such tests: one with the reactive power adjustment time set to 2 seconds, and the other with the reactive power adjustment time set to 10 seconds. The reactive power actually adjusts to its Q(V) setpoint in less than half of the designated time in both cases. There is no overshoot or ringing of reactive power. Note that there is a small amount of overshoot in real power during the reactive power rise time. The inverter passes these tests.

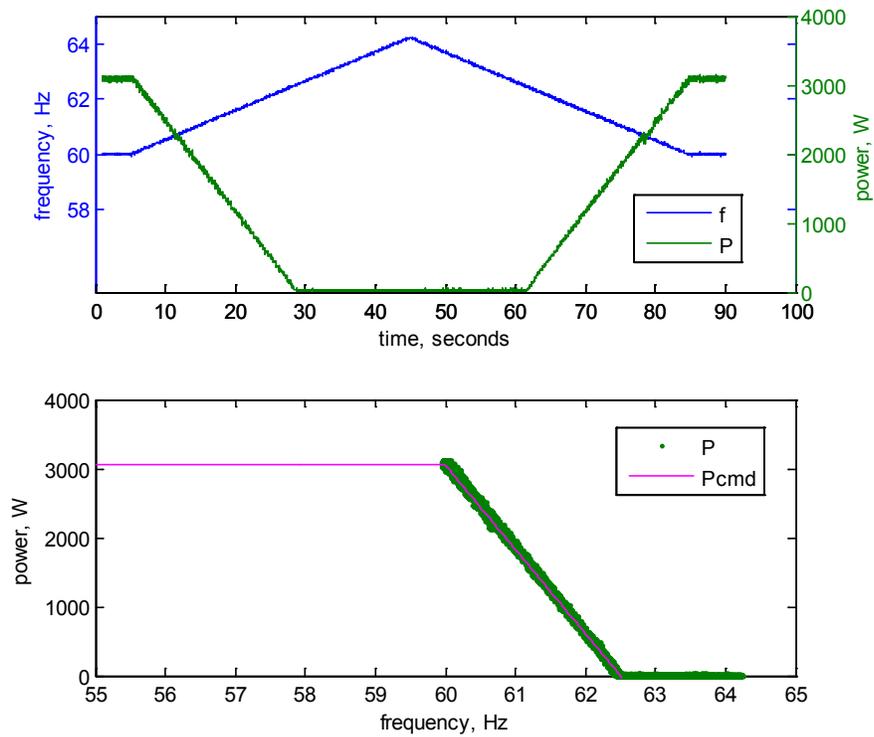


**Figure S10. Inverter voltage and reactive power during dynamic step response tests of volt-VAR characteristic 3. The result on the left was produced with the inverter programmed for a 2-second adjustment time, and the result on the right was produced with the inverter programmed for a 10-second adjustment time.**

### 3.1.5 Frequency-Watt Test Results

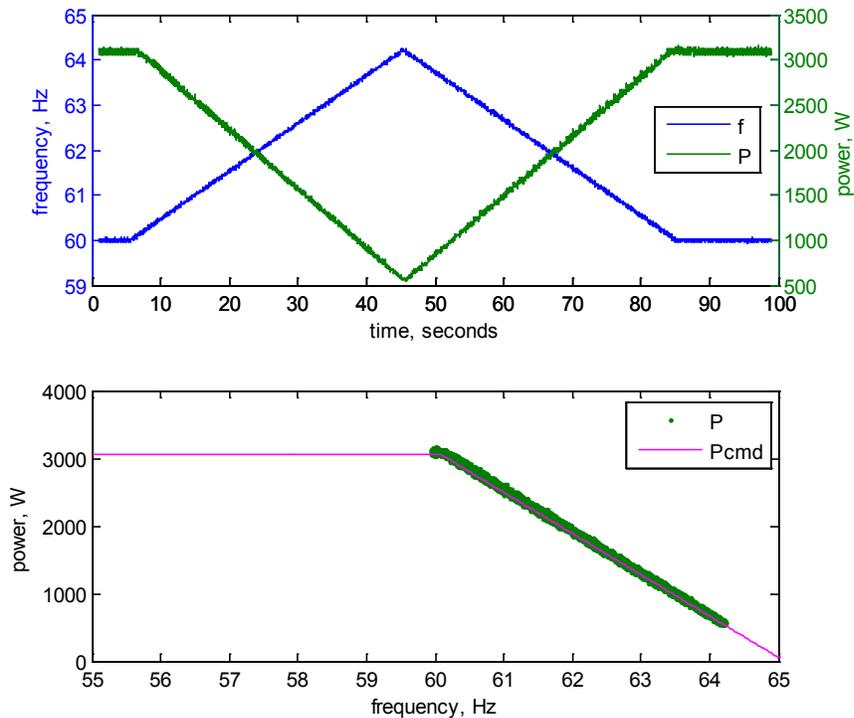
The inverter is capable of curtailing its output power at high frequency according to a programmed power versus frequency characteristic,  $P(f)$ . A test plan for this characteristic has not yet been developed, but some preliminary tests were performed to characterize this function.

Figure S11 shows plots of inverter power and frequency during a test where the inverter was commanded to curtail real power beginning at 60 Hz and at a slope of 40% of nominal power per Hz. The top plot shows power and frequency versus time, and the bottom plot shows the measured  $P(f)$  characteristic along with the commanded  $P(f)$  characteristic for comparison. The inverter tracks the  $P(f)$  command perfectly.



**Figure S11. Inverter real power and frequency during a test of high-frequency power curtailment.**

Figure S12 shows frequency and real power during at test where the inverter was commanded to begin curtailing power at 60.1 Hz at a rate of 20% per Hz. Again, the inverter tracked the characteristic perfectly.



**Figure S12. Inverter real power and frequency during a test of high-frequency power curtailment.**

Dynamic tests of high-frequency power curtailment were not performed. Future test plans should include dynamic tests of this function, as well as tests of  $P(f)$  characteristics that include hysteresis.

### 3.1.6 Summary of Single-Phase Inverter Test Results

The inverter performed well in all tests of voltage and frequency disconnection time and magnitude. Simultaneously performing volt-VAR control or high-frequency power curtailment does not affect the trip magnitude or time. Trip times and magnitudes are consistent enough that each trip setting can be interpreted to imply a corresponding ride-through setting, as noted above.

The inverter passed all islanding tests, regardless of which advanced grid support features were running simultaneously. However, some limited evidence suggests that the island trip times are longer when frequency trip settings allow wider ranges of frequencies. This requires further investigation.

The inverter also performed well in all tests of its volt-VAR function. However, the slope of the measured  $Q(V)$  characteristics consistently deviated from the commanded slope. Several possible reasons for this are noted above. Because the measured  $Q(V)$  slopes sometimes exceed and sometimes are less than the commanded slope, the most likely reason for the discrepancy is that the inverter internally uses low-resolution discrete values to set the  $Q(V)$  slope.<sup>60</sup> If this is

<sup>60</sup> For example, the  $Q(V)$  characteristic may be created using several scaled lookup tables.

the case, the internally created slope apparently has lower resolution than the slope parameter reported by the inverter via communications. This hypothesis could be tested through more thorough testing of the volt-VAR function. If it is indeed true, then the manufacturer's stated accuracy of reactive power will presumably take this into account, and the inverter will pass the tests.

Finally, the inverter performed well in all tests of high-frequency power curtailment.

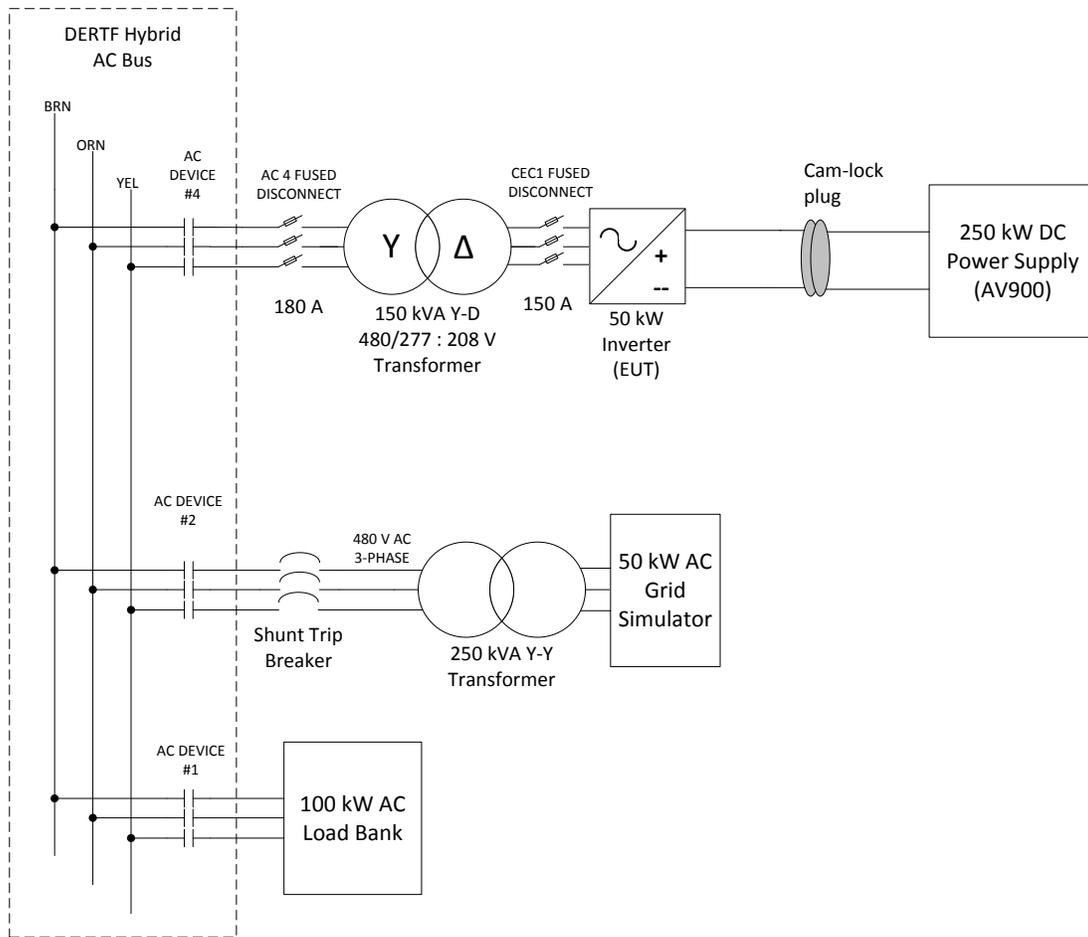
The reader should note that only a subset of the prescribed tests was performed, and tests were not repeated to a significant degree. Nevertheless, the inverter appears to perform well in all tests.

### **3.2 NREL Prototype Inverter Tests**

Several of the tests described here were also performed on a prototype inverter developed at NREL. The tests performed were for response to abnormal voltage, response to abnormal frequency, and volt-VAR control. These functions were very recently implemented in this inverter and had not been thoroughly tested before.

Figure N1 shows the electrical connections for the inverter test. The AV900 250-kW DC supply provided DC input power at 400 V to 500 V. A 50-kW Pacific Power programmable AC supply and a 100-kVA resistive-inductive load bank provided the simulated EPS. The inverter output was 208V line-line. There was no neutral. The inverter interfaced with the grid simulator at 480/277 V through the delta-wye transformer. The inverter was operated below 20 kVA during all tests due to an inoperative primary cooling system.

This prototype inverter controller accepts trip delay settings rather than trip time settings. Therefore, all the time tests were expected to exceed the time setting by at least one line cycle due to detection time, control action time, and other minor delays in the tripping process.



**Figure N1. Test setup for NREL prototype inverter.**

### 3.2.1 Abnormal Voltage Disconnection Test Results

The NREL inverter has two overvoltage settings and two undervoltage settings. These settings were tested at various levels both with and without volt-VAR control running. Overvoltage tests were only performed up to 112% due to the limitations of the grid simulator.

Table N1 summarizes the results of the voltage time tests. In all cases, the inverter tripped between 0.024 and 0.074 seconds after the commanded trip time, which is within the expected range given that the inverter accepts delay time settings rather than trip time settings. The inverter consistently tripped just after the commanded time with high accuracy for both long and short trip times. Performing volt-VAR control had no impact on trip time.

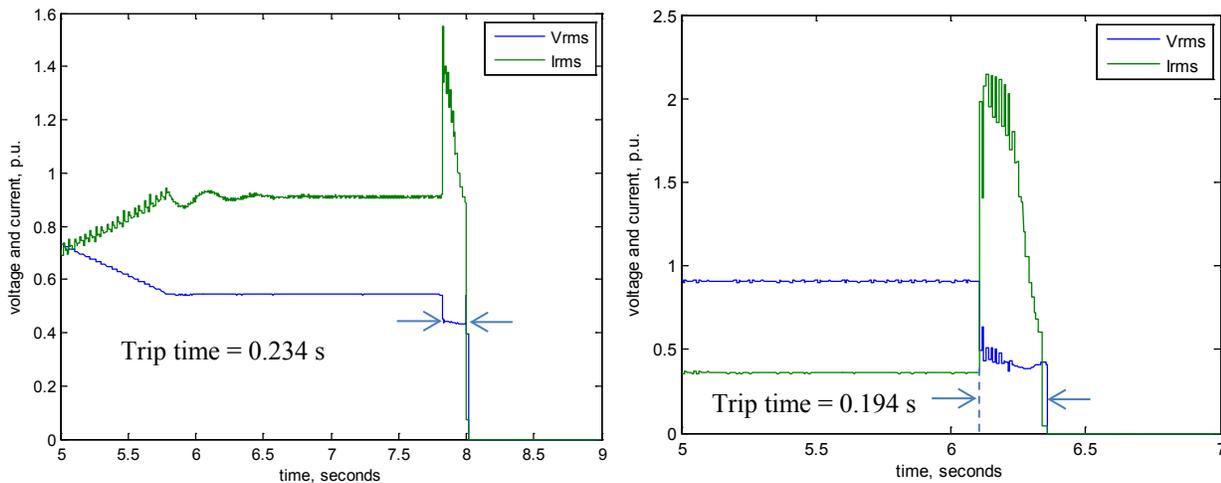
Figure N2 shows inverter RMS voltage and current for the two tests of the 45% voltage, 0.16 second trip setting, with and without volt-VAR running. The trip actually occurs slightly faster in the test with volt-VAR running. Note that the current spikes significantly following both voltage steps. This is allowed under the test criteria but may need to be remedied before operation in a real EPS.

Note that because voltage was measured on the inverter side of the inverter’s AC output contactor, measured voltage drops to zero immediately after the inverter disconnects during each test.

**Table N1. NREL Inverter Voltage Trip Time Tests**

Volt-VAR Setting	Voltage Trip Setting (%)	Trip Time Setting (s)	Measured Trip Time (s)	Result
Off	45	0.16	0.234	Pass*
	60	11	11.028	Pass*
	88	21	21.03	Pass*
	110	2	2.043	Pass*
	110	13	13.043	Pass*
	110	13	13.047	Pass*
	112	0.16	0.187	Pass*
Q(V) Characteristic 1, Test 1-2 Settings	45	0.16	0.194	Pass*
	60	11	11.024	Pass*
	88	21	21.03	Pass*
	110	13	13.048	Pass*
	120	0.16	0.19	Pass*

\*Trip timer needs adjustment for fixed delays



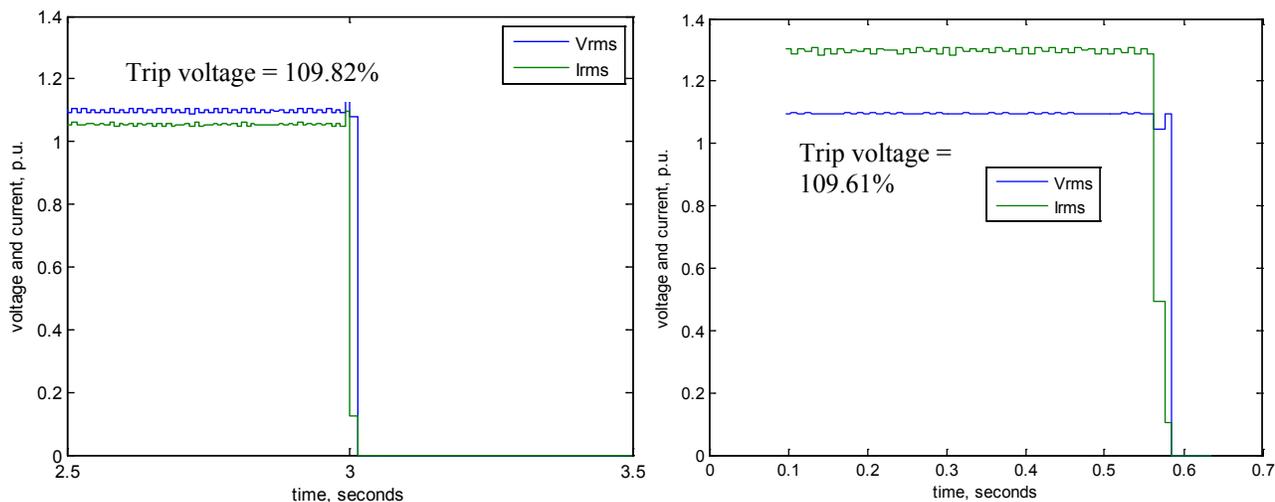
**Figure N2. NREL inverter voltage and current for two voltage trip time tests. On the left is the 45%, 0.16 second test without volt-VAR control running. On the right is the same test with volt-VAR running.**

Table N2 summarizes the voltage trip magnitude test results. Voltage magnitude tests were only performed for all phases simultaneously, not for each phase individually as would be required in a full test. This inverter’s accuracy of voltage was taken to be 1/32 V because that is the accuracy of the parameter used to store voltage trip settings, but in practice it may be larger due measurement uncertainty and other factors. This very high accuracy leads to very slow magnitude ramps. To counteract this, trip times were set at or below 2 seconds for these tests. This achieves a more reasonable ramp time without affecting the accuracy of the test.

The inverter passed all tests, consistently tripping before the trip voltage setting was reached by between 0.001 and 0.44 percentage points of nominal voltage. As with this inverter, such a level of consistency can be taken to imply that the voltage magnitude setting contains an implied voltage ride-through magnitude. No effect on the test result was observed when volt-VAR was running versus when it was not. Figure N3 shows inverter voltage and current during two representative magnitude tests.

**Table N2. NREL Inverter Voltage Trip Magnitude Tests**

Volt-VAR Setting	Voltage Trip Setting (%)	Trip Time Setting (s)	Measured Trip Time (s)	Result
Off	45	0.16	45.19	Pass
	60	2	60.14	Pass
	88	2	88.06	Pass
	110	2	109.82	Pass
	112	0.16	111.72	Pass
Q(V) Characteristic 1, Test 1-2 Settings	45	0.16	45.1	Pass
	60	2	60.001	Pass
	88	2	88.13	Pass
	110	2	109.61	Pass
	120	0.16	111.56	Pass



**Figure N3. NREL inverter voltage and current for two voltage trip magnitude tests. On the left is the 110%, 2-second test without volt-VAR control running. On the right is the same test with volt-VAR running.**

### 3.2.2 Abnormal Frequency Disconnection Test Results

The NREL inverter's frequency trip settings were also tested at various levels. This inverter currently does not include any frequency response function, so each frequency disconnection test was only performed without frequency response.

Table N3 shows the results of the frequency time tests. As with the voltage time tests, the inverter typically disconnected just after the commanded time had passed, in this case between 0 and 0.023 seconds later. Again, this is because the inverter uses a delay setting that does not account for various delays inherent to the trip function, rather than a true trip time setting.

**Table N3. NREL Inverter Frequency Trip Time Tests**

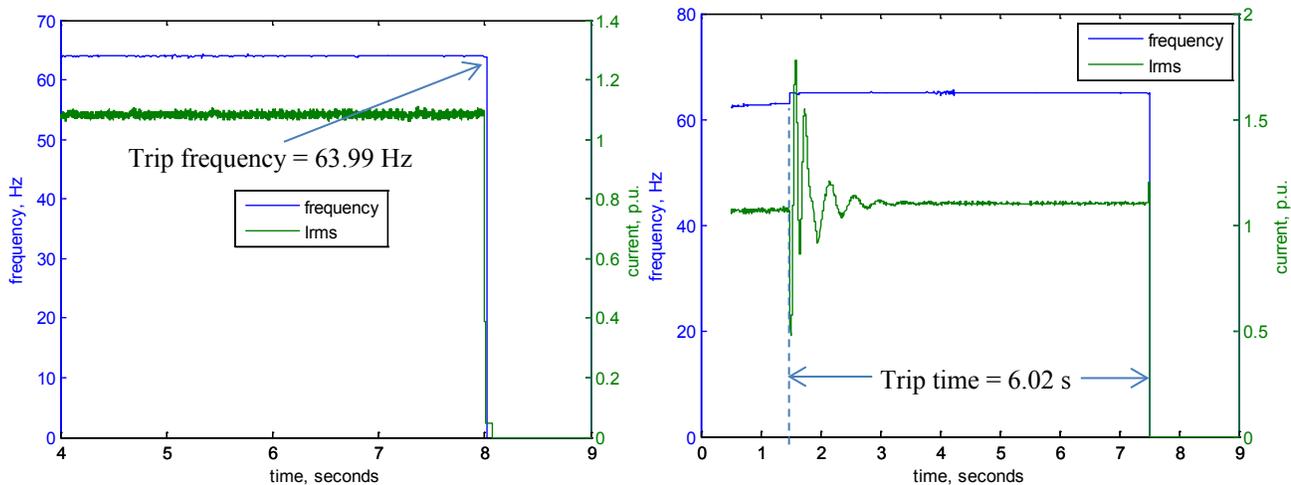
Trip Magnitude Setting (Hz)	Trip Time Setting (s)	Measured Trip Time (s)	Result
56	0.16	0.18	Pass*
56	6	6.021	Pass*
59.5	300	299.98	Pass
64	6	6.02	Pass*
64	0.16	0.183	Pass*
*Trip timer needs adjustment for fixed delays			

Table N4 shows the results of the frequency magnitude tests. The inverter consistently tripped at almost exactly the designated frequency. In three of the four tests, the measured trip frequency was just outside of the set limit, but still within the measurement accuracy of 0.01 Hz. The inverter passed these tests.

**Table N4. NREL Inverter Frequency Trip Magnitude Tests**

Trip Magnitude Setting (Hz)	Trip Time Setting (s)	Measured Trip Freq. (Hz)	Result
56	0.16	55.99	Pass
59.5	6	59.49	Pass
60.5	6	60.51	Pass
64	0.16	63.99	Pass

Figure N4 shows RMS inverter frequency and current for one frequency magnitude test (64 Hz, 0.16 seconds) and one frequency time test (64 Hz, 1 second). The inverter current exhibited significant ringing following the frequency step in the time test. For larger frequency steps, the inverter actually tripped offline due to its software overcurrent protection. This behavior is undesirable but does not constitute a failure of the test. However, it may need to be addressed before operating the inverter in practice, depending on the expected magnitude and slew rate of frequency changes in a real EPS.



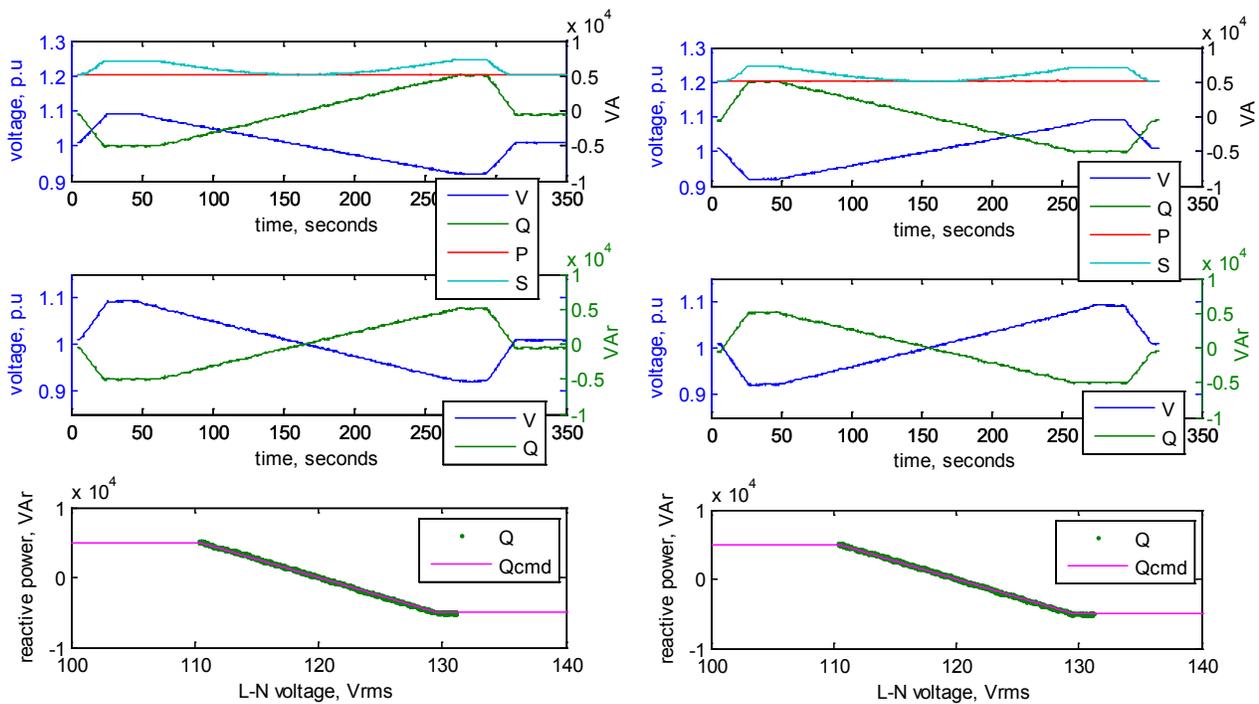
**Figure N4. NREL inverter frequency and current for a 64 Hz overfrequency magnitude test (left) and a 64 Hz, 6 second overfrequency time test (right). Note that while the inverter passes both tests, the current undergoes significant ringing following the frequency step in the time test.**

EPS and EUT operators may feel comfortable interpreting the frequency and voltage trip settings in the NREL inverter to include implied ride-through settings due to the high accuracy of the trip times and magnitudes.

### 3.2.3 Volt-VAR Test Results

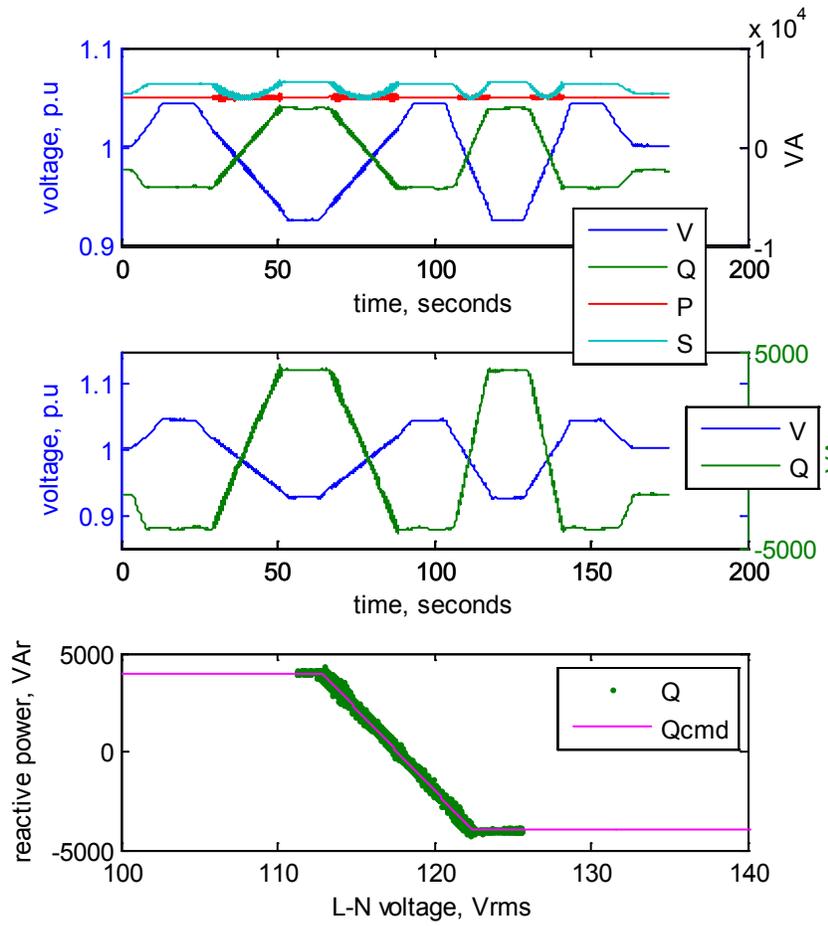
The NREL inverter can perform volt-VAR control according to characteristic 1 (no deadband, no hysteresis). This functionality was very recently implemented and had been only minimally tested before execution of the tests summarized below. Tests 1, 3, 5, and 7 for Q(V) characteristic 1 were performed. Unless otherwise noted, the maximum inverter power was set to 15 kW. This inverter does not include a volt-VAR response time setting.

Figure N5 shows inverter voltage and power during test 1, which was divided into two segments for measurement purposes. The reactive power tracks the commanded characteristic very well. Because this inverter was operating well below its rated power, real power remains constant during these tests, and apparent power increases as reactive power is exported or imported. Ideally, the test should have covered lower voltages as well to more thoroughly test the part of the characteristic where Q is constant and positive. The reactive power produced by the inverter created significant voltage differentials in the wires and transformer that are between the inverter and the grid simulator. This partially counteracted abnormal voltages produced by the grid simulator (as expected). The voltage commands sent to the grid simulator should be modified to better account for voltage drops and rises between the source and the inverter.

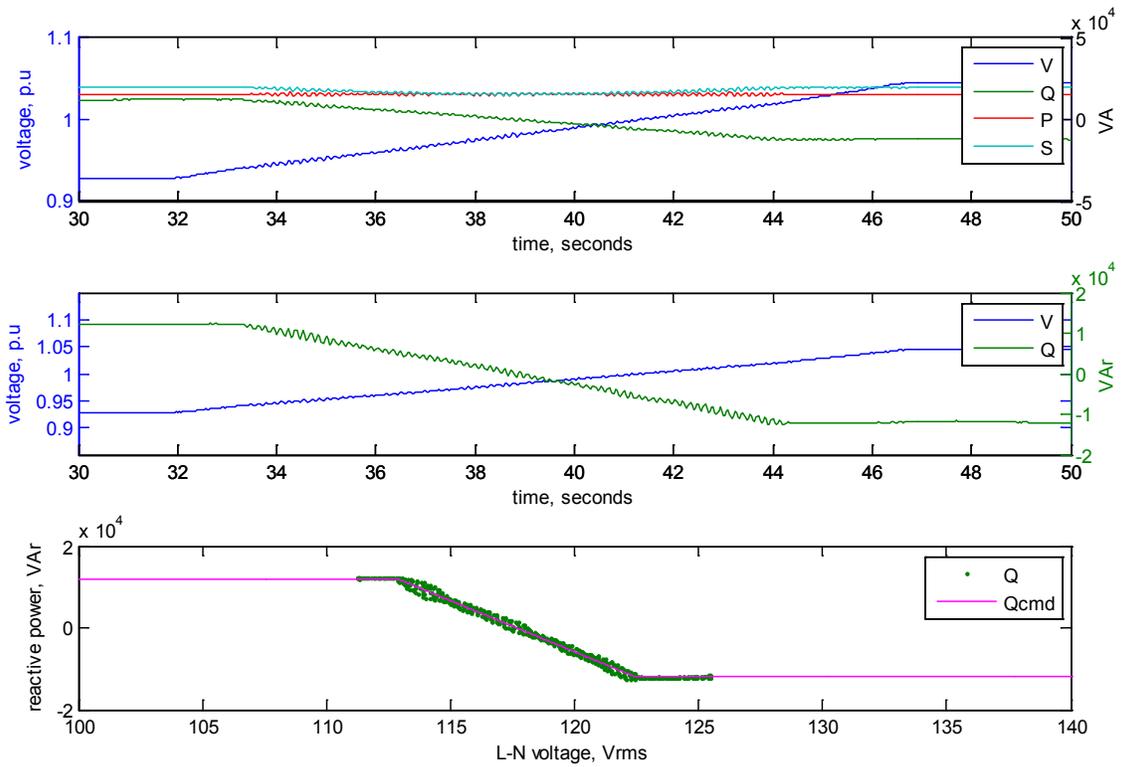


**Figure N5. NREL inverter voltage and power during volt-VAR test 1.**

Figures N6 and N7 show the results of test 3, which uses a Q(V) characteristic that is offset with respect to nominal voltage and has a somewhat steeper Q(V) slope than test 1. In Figure N6 the inverter appears to track the Q(V) characteristic very well. However, a closer view of part of the test in Figure N7 shows that reactive power is oscillating slightly when the voltage is changing. These oscillations seem to be a function of the slope of the Q(V) characteristic, with steeper slopes resulting in greater oscillation amplitudes.

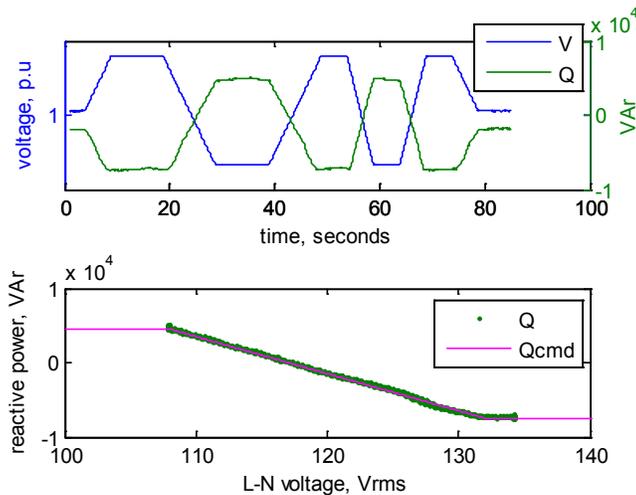


**Figure N6. NREL inverter voltage and power during volt-VAR test 3.**



**Figure N7. A closer view of NREL inverter voltage and power during one segment of volt-VAR test 3.**

Figure N8 shows test 5, which uses a  $Q(V)$  characteristic that is offset with respect to reactive power. The plots in Figure N8 appear to show very good tracking of the  $Q(V)$  characteristic, but a closer examination (not shown here) shows that reactive power is again oscillating slightly during times of changing voltage.

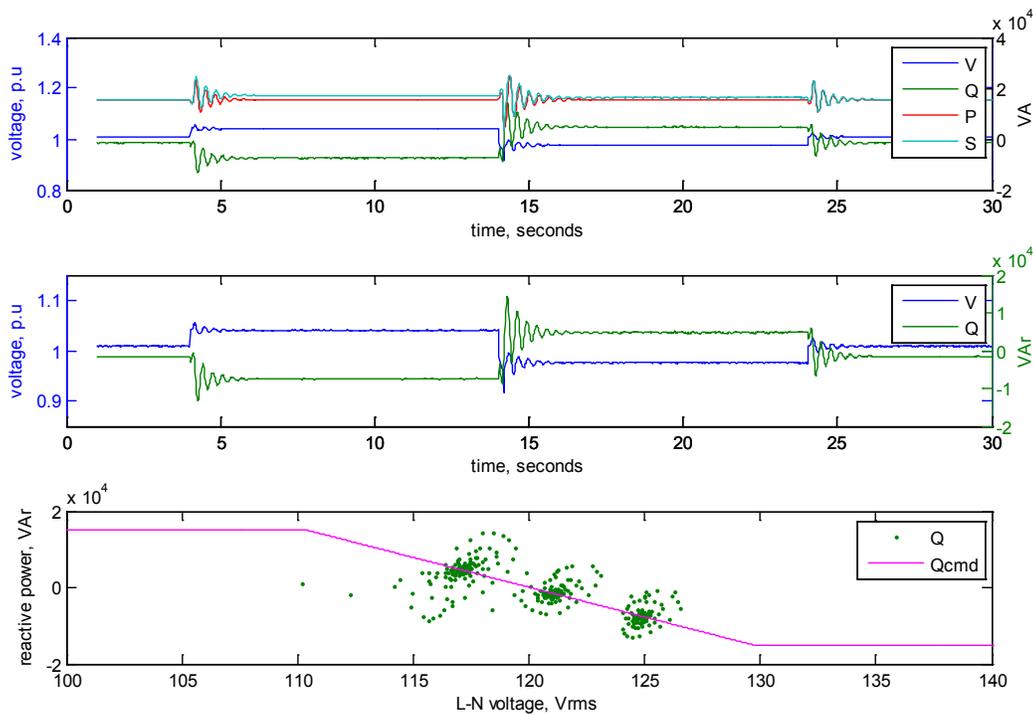


**Figure N8. NREL inverter voltage and reactive power during volt-VAR test 5.**

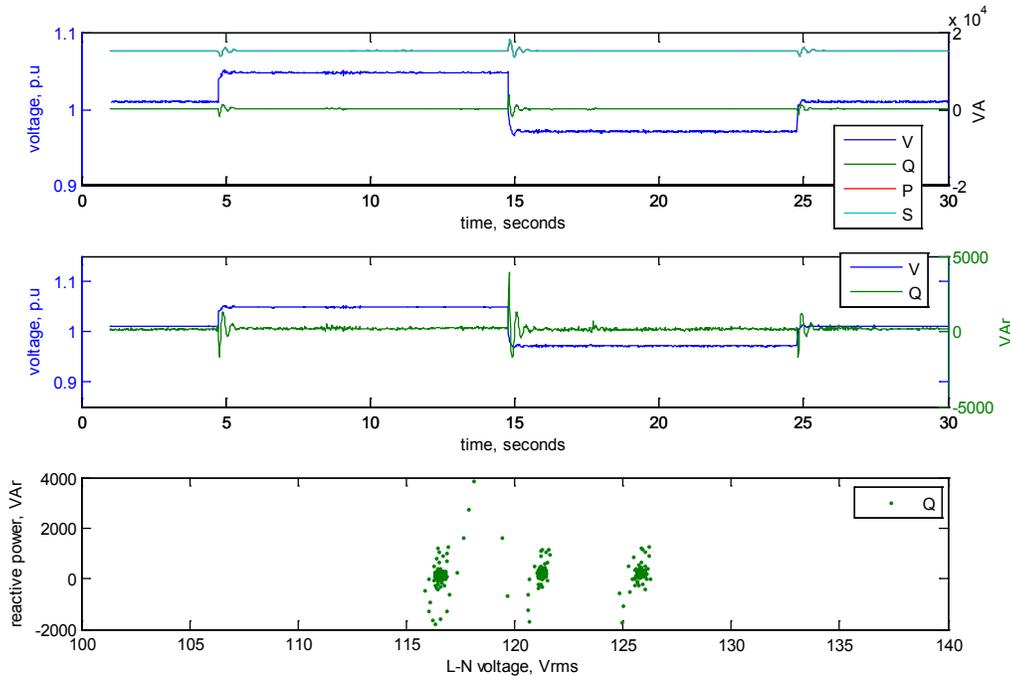
A final test using a still steeper  $Q(V)$  curve led to higher-amplitude oscillations that are not acceptable. The inverter's volt-VAR function needs to be designed to avoid such oscillations, either by placing limits on the slope of the programmed  $Q(V)$  characteristic or by altering the volt-VAR control code.

Figure N9 shows the results of a voltage step test performed with the inverter programmed for test 1 of characteristic 1. The reactive power shows significant ringing, but damps down to the desired value. This level of ringing and overshoot is probably too high to be acceptable. For comparison, Figure N10 shows the same voltage step test with volt-VAR turned off. From this comparison, it appears that roughly half of the ringing is still present without volt-VAR running.

Several other voltage step tests were performed and showed similar behavior. This inverter's volt-VAR response should have controls imposed to limit oscillations, for example, by restricting the ramp-rate or slowing the response time.



**Figure N9. NREL prototype inverter voltage and power during a volt-VAR step response test.**



**Figure N10. NREL prototype inverter voltage and power during a step response test without volt-VAR on.**

### 3.2.4 NREL Prototype Inverter Test Summary

The NREL inverter performed well in the voltage and frequency disconnection tests at all magnitudes and times tested. The disconnection times should be adjusted down by a few line cycles to account for delays in the disconnection process. The disconnection times and magnitudes consistently aligned with their commanded values. Therefore, it may not be necessary to implement separate voltage and frequency ride-through settings.

The volt-VAR function worked well with  $Q(V)$  characteristics having low slope, but displayed reactive power oscillations with higher slopes. The amplitude of the oscillations was small during most tests, but was dangerously large during for very steep  $Q(V)$  curves. The volt-VAR function also increases the magnitude of oscillations during voltage step tests. This is a prototype inverter, so it is expected that not all the algorithms and parameters are tuned to perfection, and the responses can be improved.

## 4 Conclusions

A preliminary (beta) test plan for advanced DER features has been described here along with the test results from applying that to two inverters. The test plan was written in anticipation of IEEE Std 1547a, follows the format and methodology successfully established by IEEE Std 1547.1, and can serve to provide feedback for the test procedures being proposed in the process of revising IEEE Std 1547.1a. As the 1547.1a development progresses, this beta test plan can also readily be revised to provide further insight. One focus of the test plan was to consider whether advanced grid support features might interfere with interconnection safety functions. The beta test plan is fairly general, and although the test for voltage regulation covers only a subset of the possible voltage regulation methods it addressed the most common ones. The voltage regulation tests given here provide an approach that can be extended to other voltage regulation methods.

Major components of this beta test plan include:

1. Upgraded tests for responses to abnormal voltage and frequency, including ride-through
2. A newly developed test for voltage regulation, including dynamic response testing
3. Suggested modifications for unintentional islanding, open phase, and harmonics tests to include testing while performing voltage and frequency response functions.

Testing for interactions between features greatly increases the number of tests required. The complexity of advanced grid support features (relative to conventional DER features) also increases the number of tests required. In order to reduce the total number of tests while still testing a broad range of features and interactions between features, this test plan reduces the number of repetitions of identical tests. Even so, the total number of test iterations required is significantly higher than in IEEE Std 1547.1. It may be preferable to reduce the total number of tests through the stakeholder agreement process.

The beta test plan was applied to two inverters and worked well for both. One conclusion that held true for both inverters is that explicit voltage and frequency ride-through settings may be unnecessary. The DERs tested adhered closely to programmed trip magnitudes and times, giving test personnel, EPS operators, and DER operators confidence that each voltage and frequency disconnection setting carries with it a high degree of confidence that the DER will trip very close to the setting in both magnitude and time. Additionally, DER manufacturers may define margins within which each DER will trip, giving further confidence and eliminating any need for testing separate ride-through settings.

Preliminary evidence was found that performing frequency ride-through (or having a wide band of operating frequencies) may prolong the trip time during anti-island tests. Preliminary evidence was also found that changes in grid frequency can elicit reactive power generation when volt-VAR control is enabled. Both of these findings merit further investigation.

This beta test plan requires significant future work to cover the maturing IEEE Std 1547.1 testing revisions being concurrently established. Also, extensions of this beta testing should be undertaken to address more in-depth performance characterization tests beyond strictly standards conformance tests. Example extensions of this beta test plan include the following:

- Tests for voltage and frequency ride-through curves that are not step functions (if implemented by manufacturers)
- Tests for frequency support/response functions
- Tests for other methods of voltage regulation not covered here
- Testing of advanced grid support features in an environment that simulates realistic power system dynamics (i.e., PHIL). This may lead to simpler realistic tests to support detailed impact studies in distribution circuits.
- Testing of multiple inverters with advanced features to study their dynamic interaction and performance.

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