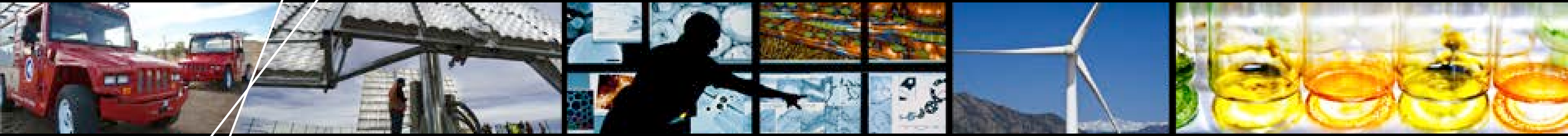
NREL
NATIONAL RENEWABLE ENERGY LABORATORY

A Manufacturing Cost Analysis Relevant to Single- and Dual-Junction Photovoltaic Cells Fabricated with III-Vs and III-Vs Grown on *Czochralski* Silicon



Michael Woodhouse
Alan Goodrich

Additional NREL Contributors:

Strategic Energy Analysis Center
Ted L. James
David Feldman
Robert Margolis

Hydrogen Technologies Center
(Photoelectrolysis Interest)
Todd Deutsch
Henning Doscher
John Turner

The National Center for Photovoltaics
Aaron Ptak
David Young
Scott Ward
Myles Steiner
Pauls Stradins
John Geisz
Daniel Friedman
Sarah Kurtz

Graphics and Communications
Alfred Hicks
Kendra Palmer
Nicole Harrison

September 30, 2013

Publication Number:
NREL/PR-6A20-60126
Contract Number:
NREL: DE-AC36-08GO28308

Analysis Disclaimer

DISCLAIMER AGREEMENT

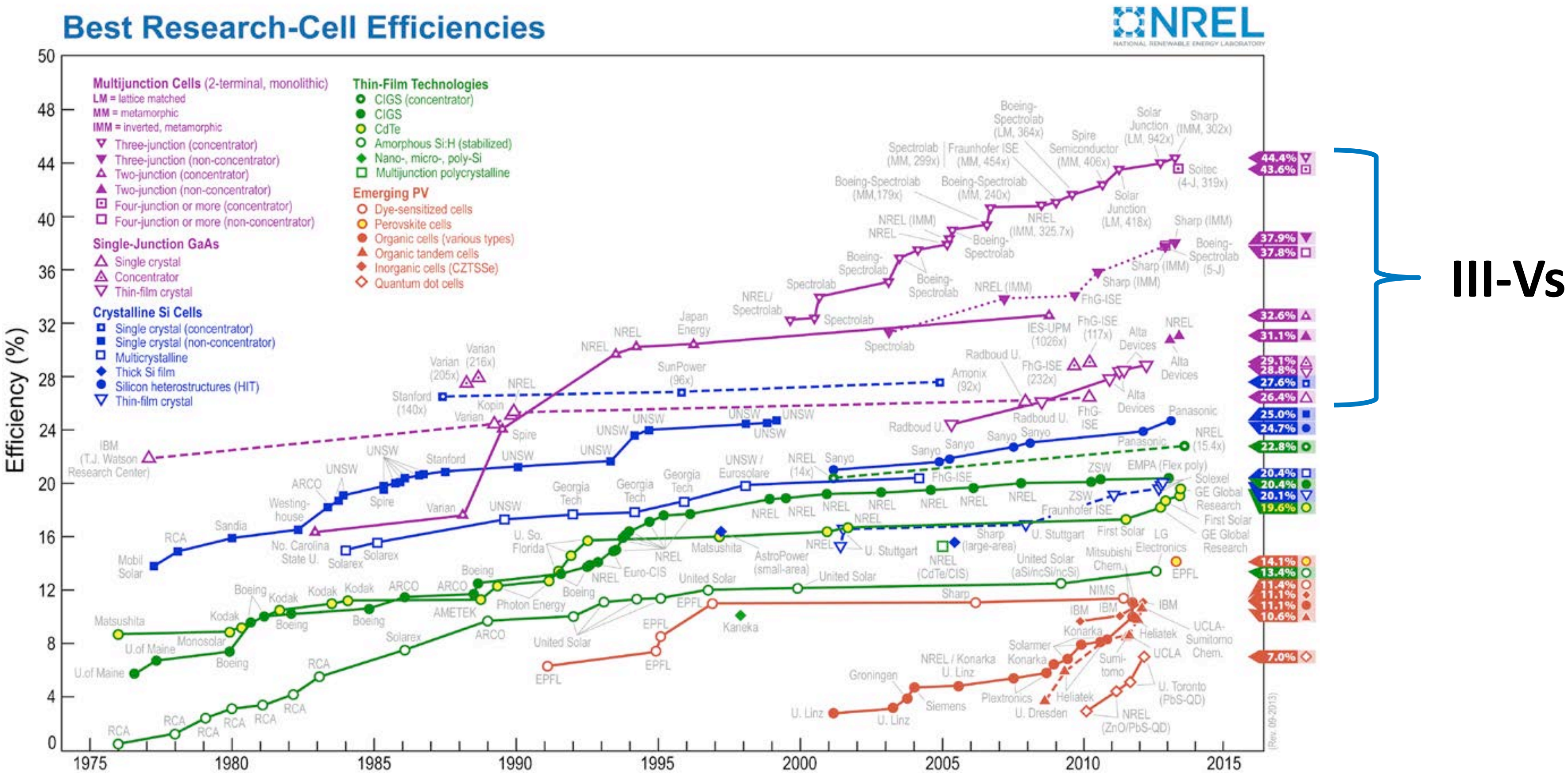
These manufacturing cost model results (“Data”) are provided by the National Renewable Energy Laboratory (“NREL”), which is operated by the Alliance for Sustainable Energy LLC (“Alliance”) for the U.S. Department of Energy (the “DOE”).

It is recognized that disclosure of these Data is provided under the following conditions and warnings: (1) these Data have been prepared for reference purposes only; (2) these Data consist of forecasts, estimates or assumptions made on a best-efforts basis, based upon present expectations; and (3) these Data were prepared with existing information and are subject to change without notice.

The names DOE/NREL/ALLIANCE shall not be used in any representation, advertising, publicity or other manner whatsoever to endorse or promote any entity that adopts or uses these Data. DOE/NREL/ALLIANCE shall not provide any support, consulting, training or assistance of any kind with regard to the use of these Data or any updates, revisions or new versions of these Data.

YOU AGREE TO INDEMNIFY DOE/NREL/ALLIANCE, AND ITS AFFILIATES, OFFICERS, AGENTS, AND EMPLOYEES AGAINST ANY CLAIM OR DEMAND, INCLUDING REASONABLE ATTORNEYS' FEES, RELATED TO YOUR USE, RELIANCE, OR ADOPTION OF THESE DATA FOR ANY PURPOSE WHATSOEVER. THESE DATA ARE PROVIDED BY DOE/NREL/ALLIANCE "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE EXPRESSLY DISCLAIMED. IN NO EVENT SHALL DOE/NREL/ALLIANCE BE LIABLE FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES WHATSOEVER, INCLUDING BUT NOT LIMITED TO CLAIMS ASSOCIATED WITH THE LOSS OF DATA OR PROFITS, WHICH MAY RESULT FROM AN ACTION IN CONTRACT, NEGLIGENCE OR OTHER TORTIOUS CLAIM THAT ARISES OUT OF OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THESE DATA.

Motivations and Objectives



- III-Vs continue to dominate PV—at least in terms of Research-Cell Efficiencies.
- This materials set has historically been limited by high manufacturing costs—so it would be beneficial to more accurately and fully understand the underlying factors behind this.
- Equally important, it would be good to understand some technology pathways to lower costs.

Efficiency Records Chart available at: http://www.nrel.gov/ncpv/images/efficiency_chart.jpg. The chart above was downloaded on 9/13/2013.

Page: 3

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:37 PM

The term 'III-Vs' refers to one or more of the group 13 elements on the periodic table (Boron, Aluminum, Gallium, Indium, Thallium, and Ununtrium) combining in some combination with one or more of the group 15 elements (Nitrogen, Phosphorous, Arsenic, Antimony, Bismuth, and Ununpentium). The nomenclature with the Roman Numerals III-V is actually historic, as the group numbering for those elements was formerly III (now group 13) and V (now group 15) under the old International Union of Pure and Applied Chemistry (IUPAC) nomenclature.

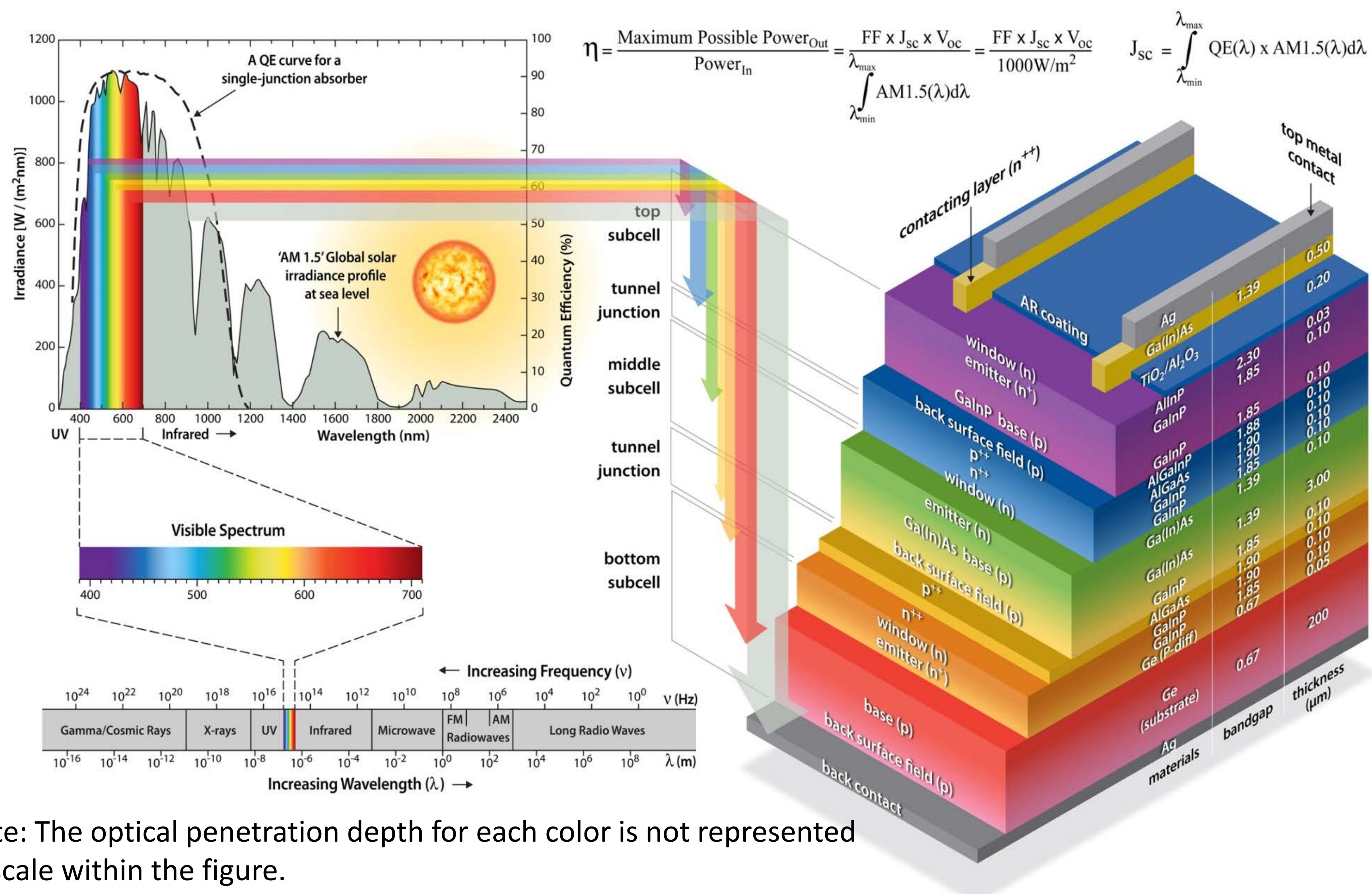
In this materials set, the Group 13-to-Group 15 atomic ratios total 1:1. Examples include GaAs, Ga0.5In0.5P, and GaAsxP(1-x).

Executive Summary

We examine the current, mid-term, and long-term manufacturing costs for III-Vs deposited by traditional Metal Organic Vapor Phase Epitaxy (MOVPE):

- Representative III-V photovoltaic devices and process flows are assembled after an extensive literature survey and after interviews with researchers and cells companies. Relevant materials suppliers and equipment vendors have also contributed to provide inputs for our manufacturing costs calculations.
- Step-by-step manufacturing cost calculations are shown for the case of single-junction GaAs cells. The model cells are envisioned to be made from thin solid film device layers. In what is esoterically called the 'epitaxial lift-off' (ELO) approach, the device layers are then released from the parent epitaxial substrate by selective etching of a sacrificial release layer (e.g., AlAs exposed to HF).
- The analysis is extended to the case of two dual-junction cell architectures: $GaAs_{0.75}P_{0.25}$ on *n*-type Czochralski (*Cz*) Si via MOVPE but without ELO, and $In_{0.5}Ga_{0.5}P$ on GaAs via ELO.
- With the traditional MOVPE approach for making the model cells—and with reasonable expectations for precursor utilizations, deposition rates, batch sizes, and parent epi-substrate allocations—the costs for these three cell types are calculated to be greater than $1.0/W at one-sun AM 1.5G.
- We highlight specific cost reduction pathways for novel III-V manufacturing processes to arrive at cell prices commensurate with the SunShot PV systems price goal of $1/W.

A Representative III-V Multi-junction Solar Cell



Note: The optical penetration depth for each color is not represented to scale within the figure.

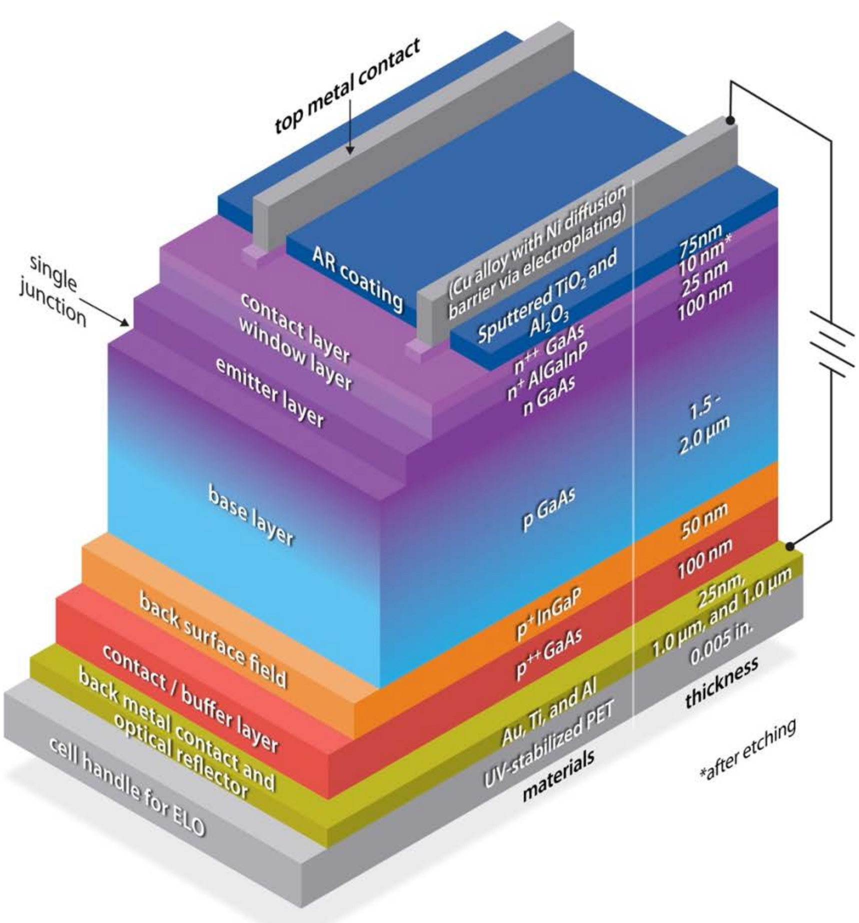
Figures adapted from Friedman, D.; Olson, J.; Kurtz, S. (2011). *High Efficiency III-V Multijunction Solar Cells, in Handbook of Photovoltaic Science and Engineering.* 2nd ed. West Sussex, UK: John Wiley and Sons.

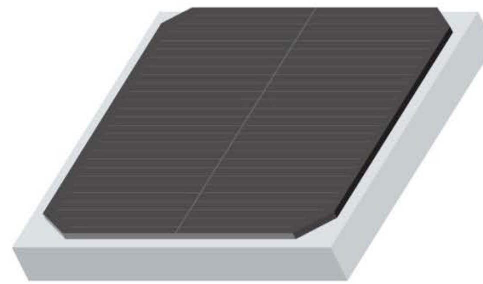
Page: 5

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:38 PM

The reader is encouraged to read the chapter cited for a great introduction to the concept of multi-junction PV cell architectures and device physics.

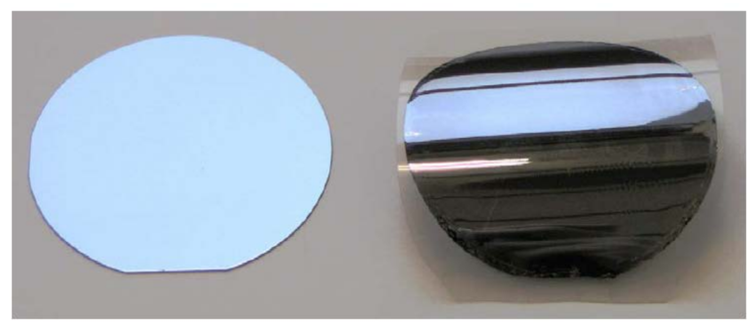
But First, the Single-junction Case: a Representative Single-Junction III-V Device that is Used for the Cost Model





133 cm² single junction GaAs solar cell on flexible handle.

Proof-of-concept within the published literature:



2” diameter single-junction GaAs on a flexible carrier (right). The solar cell was grown from (100) GaAs wafers with a misorientation of 2° towards [110] (left figure).

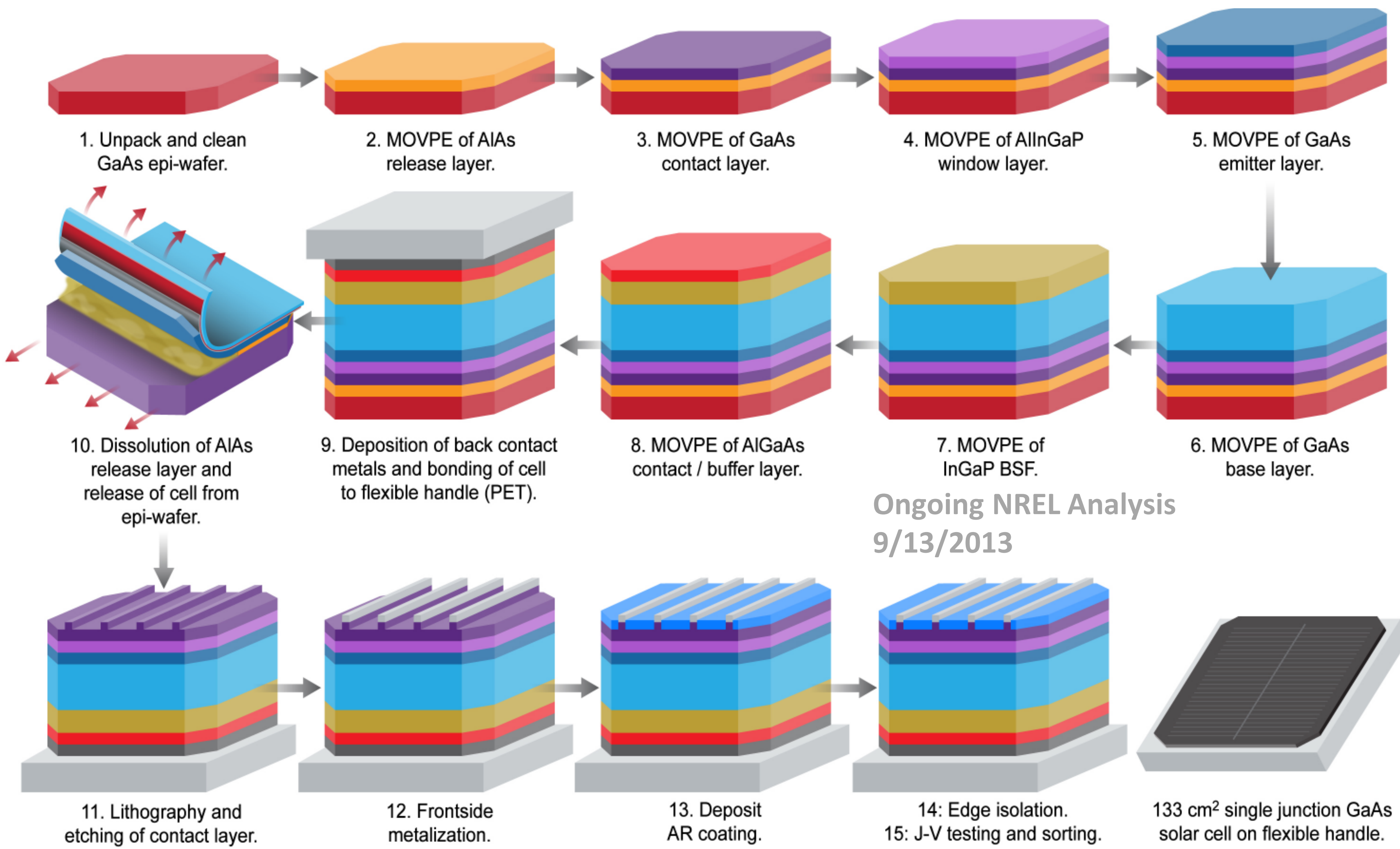
From Schermer, J.J.; Bauhuis, G.J.; Mulder, P.; Haverkamp, E.J.; van Deelen, J.; van Niftrik, A.T.J.; Larsen, P.K. (2006). “Photon confinement in high-efficiency, thin-fill III-V solar cells obtained by epitaxial lift-off.” *Thin Solid Films* 511-512; pp. 645-653.

Page: 6

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:38 PM

The model device that we use for our single-junction GaAs cost model is shown above and was conceived in consultation with NREL researchers (including those listed on the Title slide), industry collaborators, and after an extensive literature survey. The citation in the lower right provides an experimental demonstration of the epitaxial lift-off (ELO) approach to fabricating single-junction GaAs cells on a flexible carrier.

An Example Process Flow for Making Single-Junction III-V Devices by ELO



Page: 7

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:38 PM

The model process flow that we use for our single junction GaAs cost models is shown above, and was conceived in consultation with NREL researchers (including those listed on the Title slide), industry collaborators, and after an extensive literature survey.

Step 1: Unpack and Clean GaAs Parent Epi-Substrate—1

Current lowest found cost for GaAs parent epi-substrate: \$150 for a 6” diameter round wafer that is cut into a ‘pseudo-square’ shape (≈27% area loss).

Final Cell Area $= \pi(7.62\ \text{cm})^2 \times 0.73$

$= 133\ \text{cm}^2$

Cost = \$150/ 133 cm^2

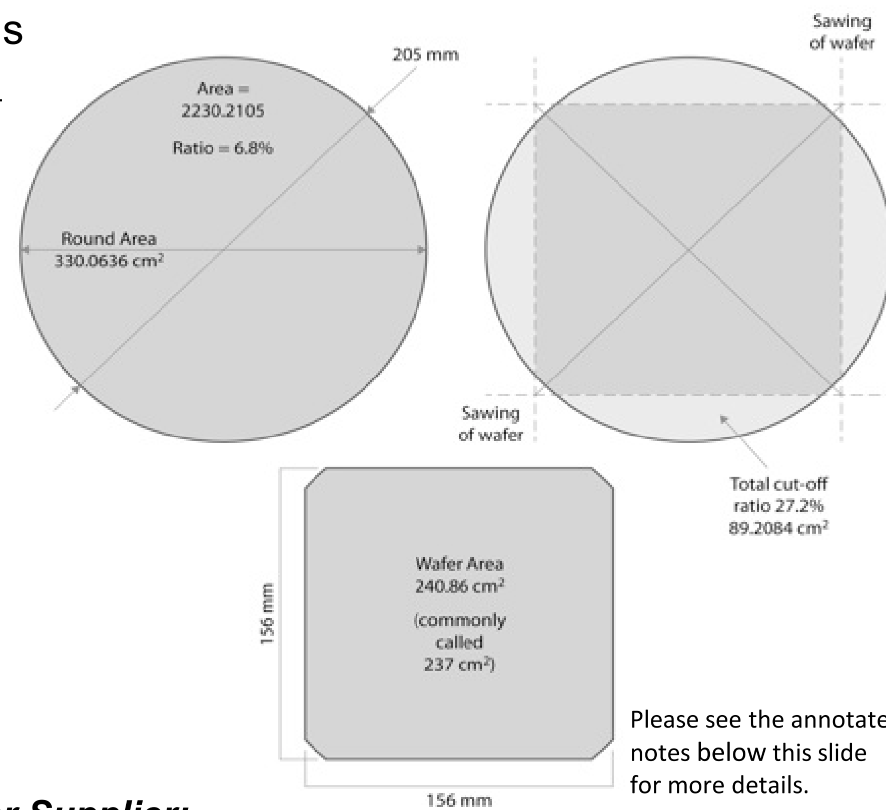
≈ \$11,300/ m^2

= \$4.0/ W @ η = 28%, 10 reuses

= \$0.81/ W @ η = 28%, 50 reuses

≈ \$0.081/ W @ η = 28%, 500 reuses

Wafering Geometry for 240 cm^2 Cz-Si Wafers



Please see the annotated notes below this slide for more details.

Additional Details About the Price Terms from the Wafer Supplier:

- The price shown is for **600 µm wafer thickness,** which is assumed to be necessary for handling and for potential material losses during each surface preparation.
- n-type doping (N_D $10^{18} – 10^{19}$), offcut 2° <100> in the <111> B direction.
- For the price shown, the purity requirements have been relaxed in order to make less expensive ‘Solar Grade’ wafers. The typical price for high purity wafers is probably more around \$180/wafer.
- The wafer price estimate includes the shaping of 6” round wafers into psuedo-square shapes (if requested).
- The price shown is a reasonable expectation for a **480,000 wafers per year contract level**. To satisfy such an order would require new scale-up of current GaAs wafer facilities. Therefore, a long-term supply contract would also be required.

Page: 8

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:44 PM

There is some debate as to what geometry is most appropriate for the parent epitaxial substrate when fabricating one-sun III-V solar cells. On the one hand, the shape might remain circular, as it originally is after the liquid-encapsulated Czochralski approach to making single crystal parents. But that would lead to significant 'dead areas' on a completed module; furthermore, if these cells might serve as drop-in replacements into incumbent cell and module assembly systems, there may be difficulties in transferring over circular wafers into the incumbent tabbing and stringing protocols. On the other hand, the shape can be made 'full-square' so that there would be essentially no dead zones on a completed module. But that leads to significant amounts of scrap losses when shaping the wafers from a full round Cz boule.

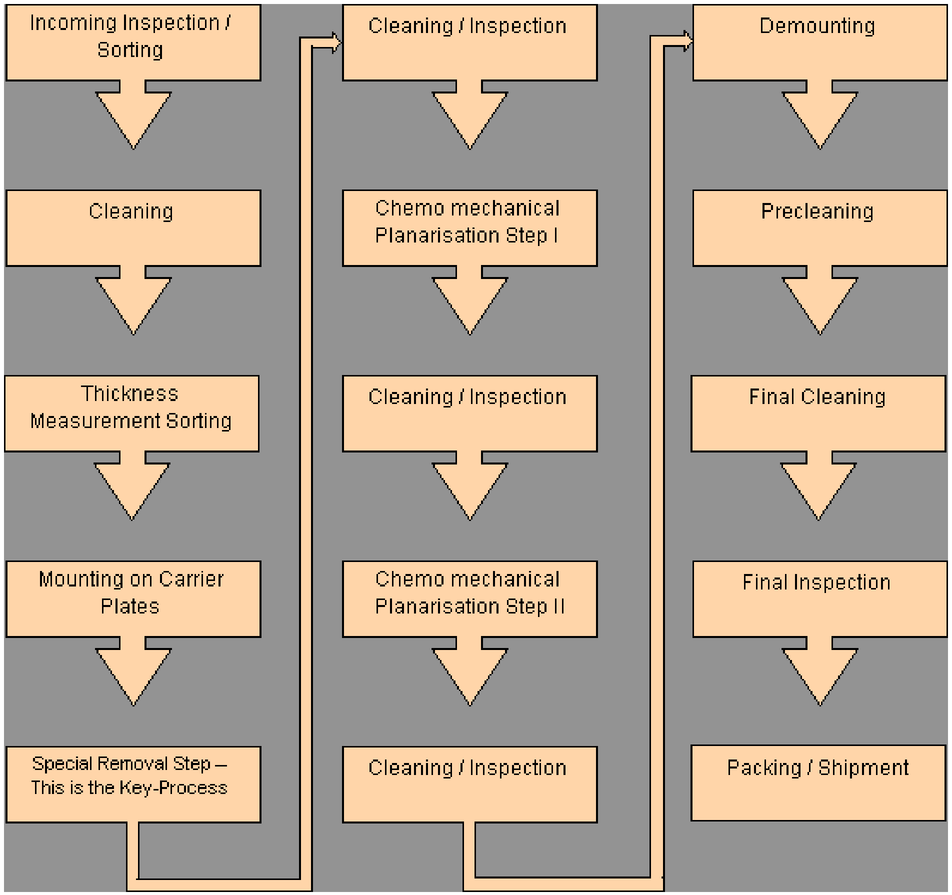
As there seems to be no clear guidance leading to a definitive answer to this quandary, we assume in this analysis that the answer may end up lying somewhere in between. As it is for high efficiency one-sun c-Si (which, in the case of monocrystalline Si also typically begins with full round Cz boules), we assume that the compromise between module dead area losses, wafer and cell equipment considerations, and material scrap losses during wafer forming might lead to the 'pseudo-square' shape for one-sun applications. The price quoted above is from a relevant wafer supplier and it would be the price for either full round wafers or for pseudo-square shaped wafers.

There may also be another argument that psuedo-square, and its associated 27% area loss, is not appropriate because the costs for the GaAs wafers are so much more than the costs for the Si wafers (on the order of 100 – 200X, depending upon volumes). But a counterpoint to that argument may be that the net cost actually depends upon the number of substrate reuses one can get from the GaAs parent epi-parent. In later slides, the reader can see that the one-sun cost allocation for the GaAs parent epi-substrate is actually calculated to be lower than the costs for a fixed Si wafer in the case that the III-V device layers are grown from a GaAs parent with ELO and with hundreds of growth cycles per parent epi-substrate.

For the case of heteroepitaxy and ELO from a c-Si wafer, our calculated costs for a 600 micron thick wafer are around \$95/m2 at an assumed polysilicon price of \$25/kg. : (1) The bandgaps of c-Si (1.2 eV) and GaAs (1.4 eV) are too similar to make an effective tandem junction device, but other III-Vs have a more appropriate bandgap around 1.8 eV.
(2) Cz-Si has served as a template for making GaAs ELO devices. There is, however, a compromise in material quality and yields in the ELO of III-Vs on c-Si approach.

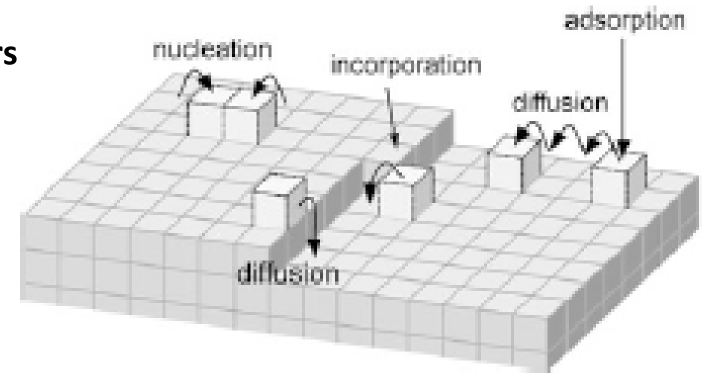
Step 1: Unpack and Clean GaAs Parent Epi-Substrate—2

Sample Process Flow for Chemical-Mechanical Polishing of GaAs Wafers



At much larger order volumes than typical for today, $8 - $12 per repolish might someday become possible for 6” diameter substrates. Please see the notes below this slide for m

The Chemical Mechanical Polishing (CMP) process flow is reproduced, with permission, from III-V reclaim (http://www.35reclaim.de/).



Schematic of atomistic rate processes in epitaxial growth. Figure from: Pohl, U.W. (2013). Atomistic Aspects of Epitaxial Layer Growth. In *Epitaxy of Semiconductors*. Berlin: Springer-Verlag.

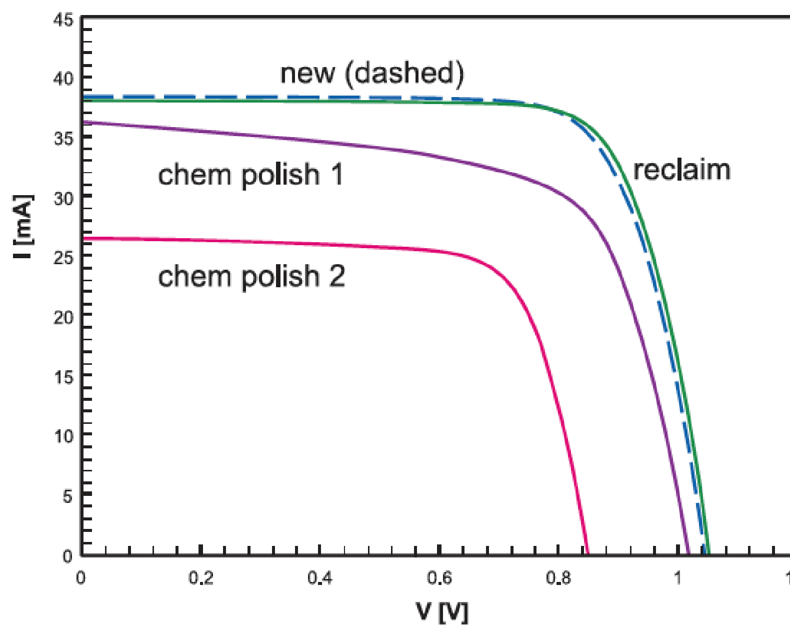


Figure from: Bauhuis, G.J.; Mulder, P.; Haverkamp, E.J.; Schermer, J.J.; Bongers, E.; Oomen, G.; Kostler, W.; Strobl, G. (2010). “Wafer Reuse for Repeated Growth of III-V Solar Cells.” *Progress in Photovoltaics* 18; pp. 155-159.

Page: 9

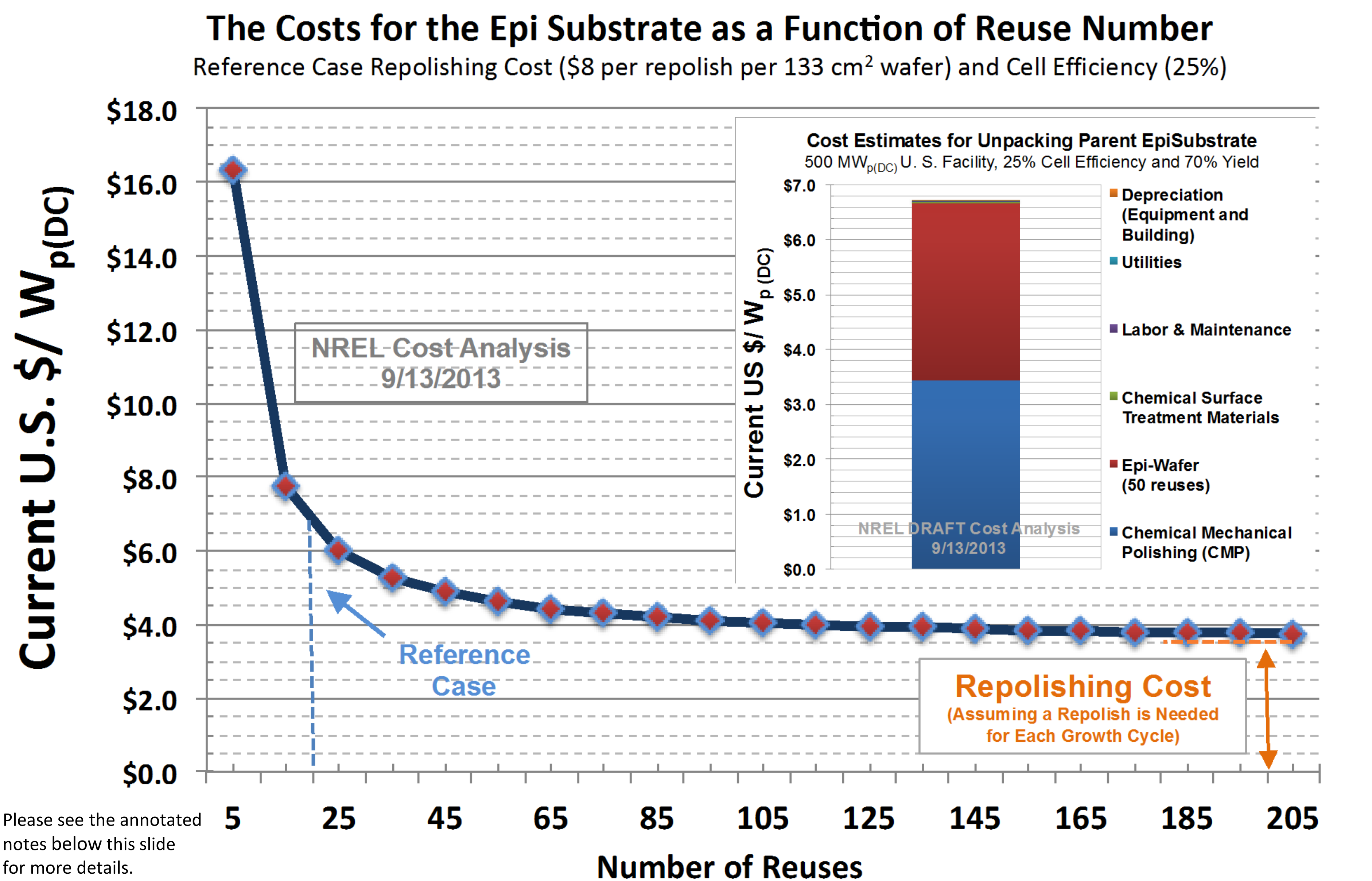
Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:44 PM

1. The reader is encouraged to read the references cited for a discussion of solid film III-V growth via MOVPE. The reference in the lower right gives an experimental demonstration of how the use, or non-use, of CMP can affect III-V solar cell device performance. There are other groups, however, that have demonstrated better success without CMP. Please see, for example:
(a) C-W Cheng, K-T Shiu, N Li, S-J Han, L Shi, and D Sadana (2013). 'Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics' Nature Communications 4; pp. 1577-1582. doi:10.1038/ncomms2583.
(b) K Lee, J D Zimmerman, X Xiao, K Sun, and S R Forrest (2012). 'Reuse of GaAs Substrates for epitaxial lift-off by employing protection layers' Journal of Applied Physics 111; pp. 033527-1. doi: 10.1063/1.3684555.

2. Because there currently doesn't seem to be a definitive answer to whether or not CMP is needed in commercial production, in this analysis we assume both a 'Reference Case' (where CMP is used between each growth cycle) and a 'Mid-Term Case' (where there is no CMP at all). Alternatively, a company or researcher may use CMP in-between so many growth cycles (e.g., a CMP after 5 or 10 growth cycles). In that case, our expectation would be that the costs scale down in proportion to the number of growth cycles between each CMP; and so the calculated costs would lie somewhere in-between the Reference and Mid-Term scenarios shown on slides 27 and 46.

Step 1: Unpack and Clean GaAs Parent Epi-Substrate—3

(The Reference Case Scenario in the Bar Chart Assumes 50 Reuses and 70% Yields)



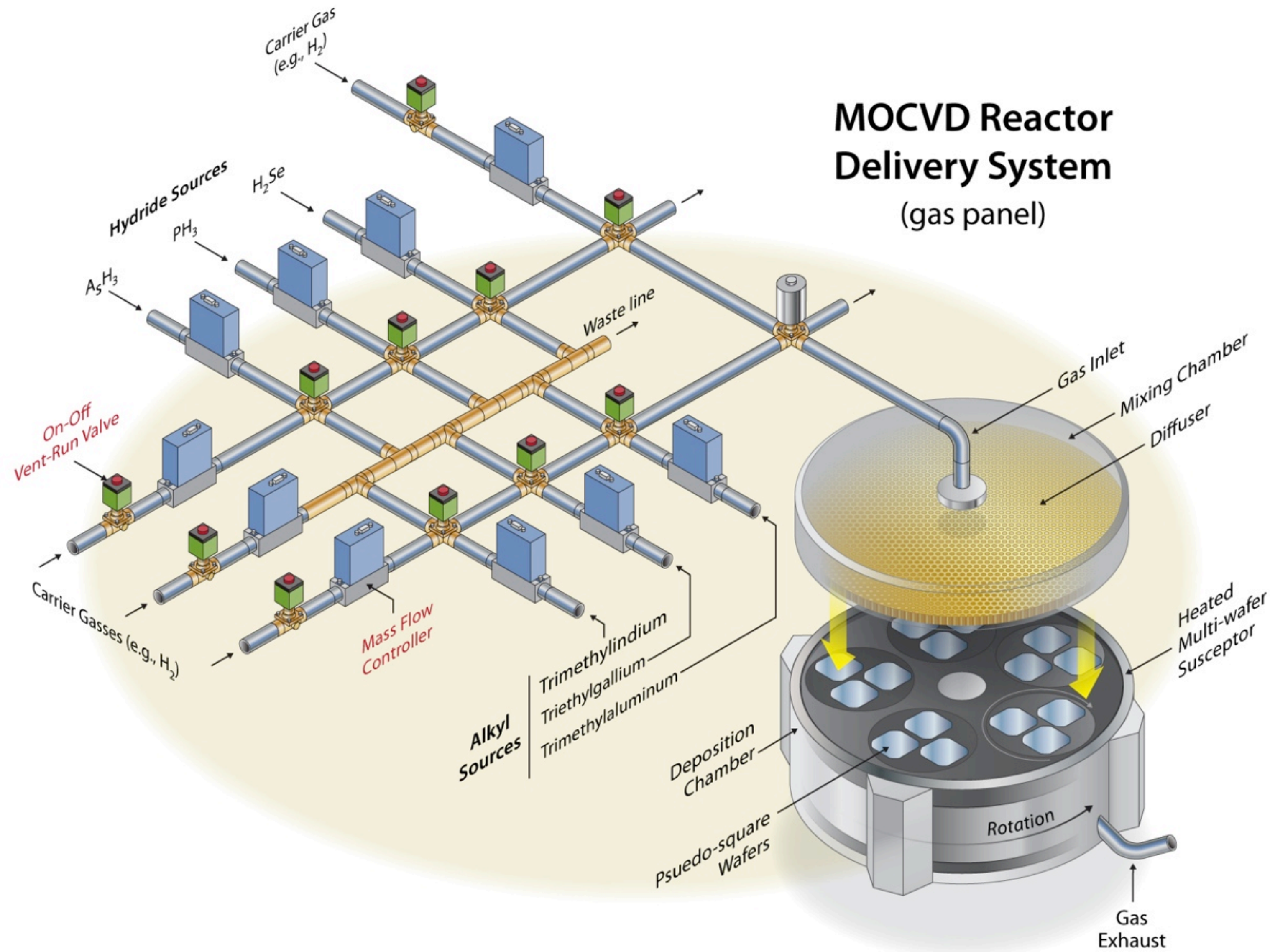
Please see the annotated notes below this slide for more details.

Page: 10

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:44 PM

1. The cost analysis represented on this slide shows the sensitivity of manufacturing costs to the number of substrate reuses and to a fixed CMP cost of $8/repolish. Note that the translated $3.4/W repolishing cost is based upon an assumption of a CMP step in-between each growth cycle and an assumption of 70% yields. Again, if there can be multiple growth cycles between each CMP, that cost will scale proportionally.
2. Also included in the bar chart are representative costs for visual inspection and microcrack detection of incoming wafers, which are based upon cost-of-ownership inputs borrowed from our c-Si PV manufacturing cost models. For a description of those costs, the reader is referred to: A Goodrich, P Hacke, Q Wang, B Sopori, R Margolis, T L James and M Woodhouse “A Wafer-Based Monocrystalline Silicon Photovoltaics Roadmap: Utilizing Known Technology Improvement Opportunities for Further Reductions in Manufacturing Costs.” (2013). Solar Energy Materials and Solar Cells 114; pp. 110–135.

The Model MOVPE Reactor



Today’s commercial reactors can accommodate 8 x 6” substrates or 15 x 4” substrates.

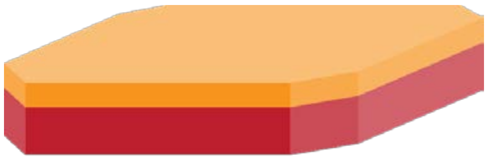
Page: 11

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:44 PM

1. This graphic represents our paradigm of a model solid film MOVPE reactor. The element III sources (Trimethylindium, or TMI, Trimethylgallium, or TMG, and Trimethylaluminum, or TMA); the element V sources (AsH3, PH3 and H2Se); and the H2 carrier gas feed into the reactor through mass flow controllers. There are also vent lines and valves to control the flow of precursors over the heated multi-wafer susceptor.
2. This reactor design leads to material utilizations that are lower than 100%. Efficient utilization of the precursors with today's MOVPE reactor designs might lead to around 30% atom-for-atom utilizations of the III sources, and around 20% atom-for-atom utilizations of the V sources. The unused precursors can be lost within the reactor, within the plumbing system itself, or they can be lost by venting through the waste line.

Step 2: MOVPE of AlAs Sacrificial Release Layer

$Al(CH_3)_3 + AsH_3 \longrightarrow$ AlAs + Byproducts
(e.g., CH_4)

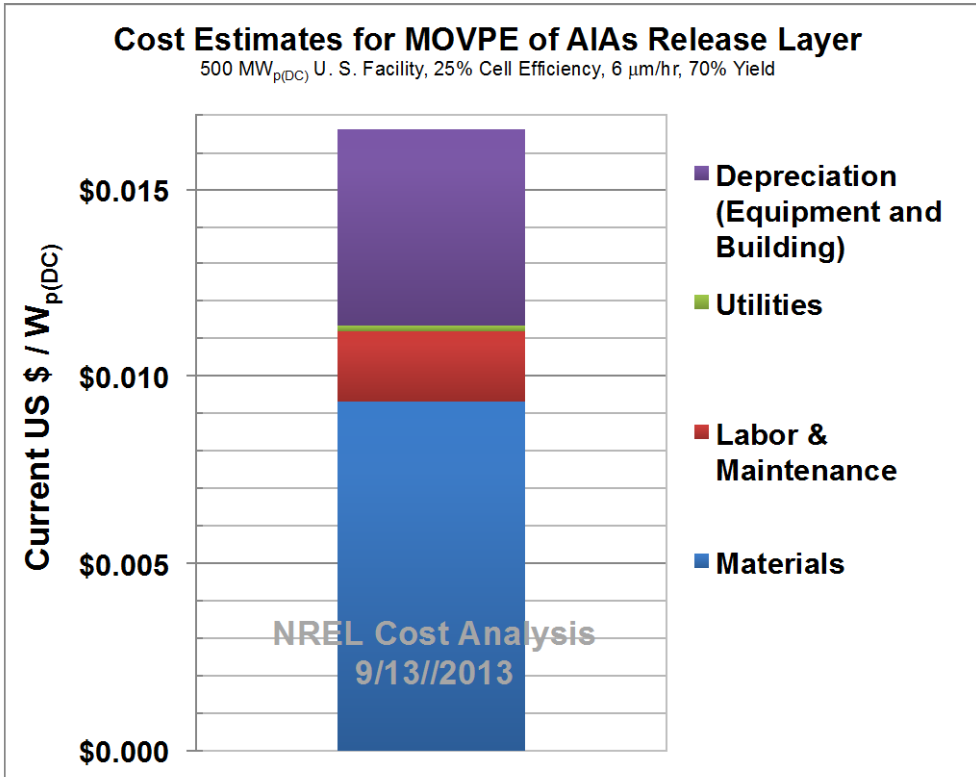


2. MOVPE of AlAs release layer.

AlAs film Thickness:	10.0	nm
AlAs Density:	3.7	g/cm^3

Precursor Gases	$Al(CH_3)_3$	AsH_3
Molecular Weight ($g\ mol^{-1}$)	144.17	77.94
Material Utilization (%)	30%	20%
Precursor Price ($/g)	$18.00	$0.44

Dopants	None	Carrier Gas(es)	H_2
Dopant Concentration (atoms cm^{-3})	0.E+00		
Price ($/ Standard L)	$0.00	Utilization	100%
Utilization	0%	Net loss per run	0%



Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $0.027/W

NOTE: Yields need to be considered. The assumption shown

Please see the annotated notes below this slide for more details.

Page: 12

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:45 PM

1. On this slide we show the relevant manufacturing cost model inputs and results for the second step of the process flow shown on Slide 7. The reader should be able to recreate the results within the bar chart by using the inputs given on this slide.

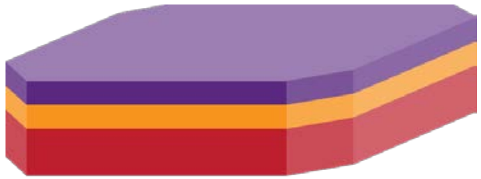
2. Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the EIA, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle and D. Shackelford. 'Do multinationals of domestic firms face higher effective tax rates?', National Bureau of Economic Research whitepaper, Cambridge, MA, 2009).

3. For the purposes of calculating the depreciation expense for steps 2 – 8 in the model process flow, it is important to note that MOVPE reactor dwell times for the temperature ramp up, pump down, and cleaning times need to be considered. For this accounting to not dwarf other details for the thinnest layers in the model device, these times are included in the Total Average Cycle Times (TACT) for the GaAs base layer step costs calculation only.

Step 3: MOVPE of n^{++} GaAs Contact Layer

$$Ga(CH_3)_3 + AsH_3 \longrightarrow GaAs + \text{Byproducts}$$

(e.g., CH_4)



3. MOVPE of GaAs contact layer.

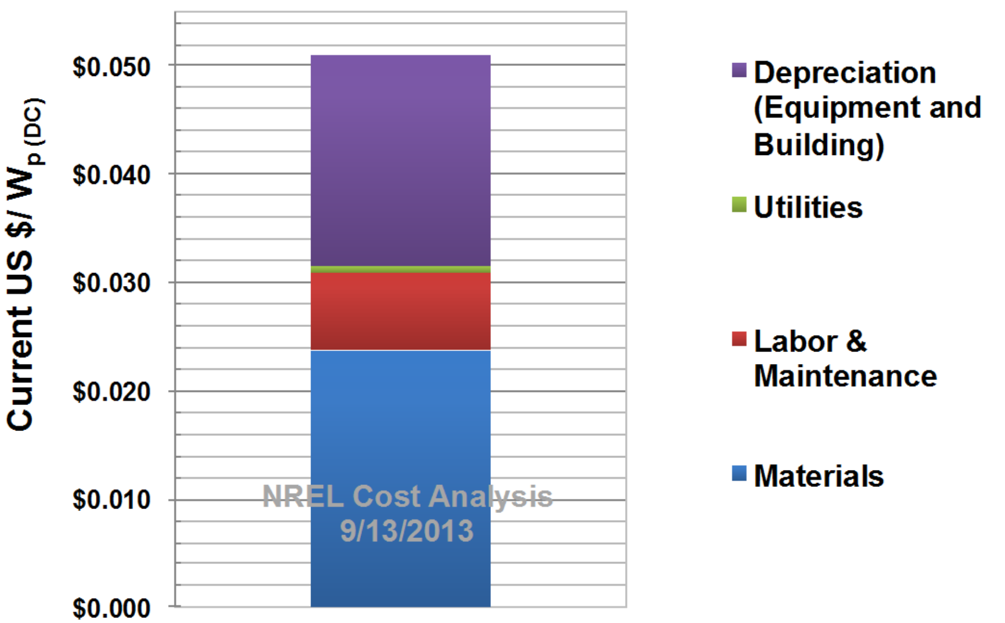
Precursor Gases	$Ga(CH_3)_3$	AsH_3
Molecular Weight (g mol^{-1})	114.82	77.94
Material Utilization (%)	30%	20%
Precursor Price ($/g)	$2.50	$0.44
Reclamation value of spent precursor ($/ g)	$0.00	$0.00

Dopants	SiH_4	Carrier Gas(es)	H_2
Dopant Concentration (atoms cm^{-3})	2.E+19		
Price ($/ Standard L)	$0.15	Utilization	100%
Utilization	5%	Net loss per run	0%

GaAs contact layer film Thickness:	0.100	microns
GaAs Density:	5.32	g/cc

Cost Estimates for n^{++} GaAs Front Contact Layer

500 $MW_{p(DC)}$ U. S. Facility, 25% Efficiency, 15 μm/hr, 70% Yield



Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $0.10/W

Please see the annotated notes below this slide for more details.

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:45 PM

1. On this slide we show the relevant manufacturing cost model inputs and results for the third step of the process flow shown on Slide 7. The reader should be able to recreate the results within the bar chart by using the inputs given on this slide.

2. Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the eia, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle, D. Shackelford, Do multinationals of domestic firms face higher effective tax rates?, National Bureau of Economic Research, Cambridge, MA, 2009).

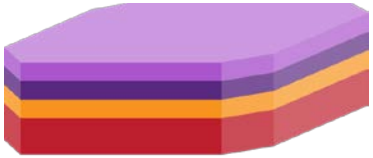
3. For the purposes of calculating the depreciation expense for steps 2 – 8 in the model process flow, it is important to note that MOVPE reactor dwell times for the temperature ramp up, pump down, and cleaning times need to be considered. For this accounting to not dwarf other details for the thinnest layers in the model device, these times are included in the Total Average Cycle Times (TACT) for the GaAs base layer step costs calculation only.

Step 4: MOVPE of n^+ AlInGaP Window Layer

$$x\mathrm{Al(CH_3)_3} + y\mathrm{In(CH_3)_3} + (1\text{-}x\text{-}y)\mathrm{Ga(CH_3)_3} + \mathrm{PH_3} \longrightarrow \mathrm{Al}_x\mathrm{In}_y\mathrm{Ga}_{1-x-y}\mathrm{P} + \text{Byproducts}$$

(e.g., CH_4)

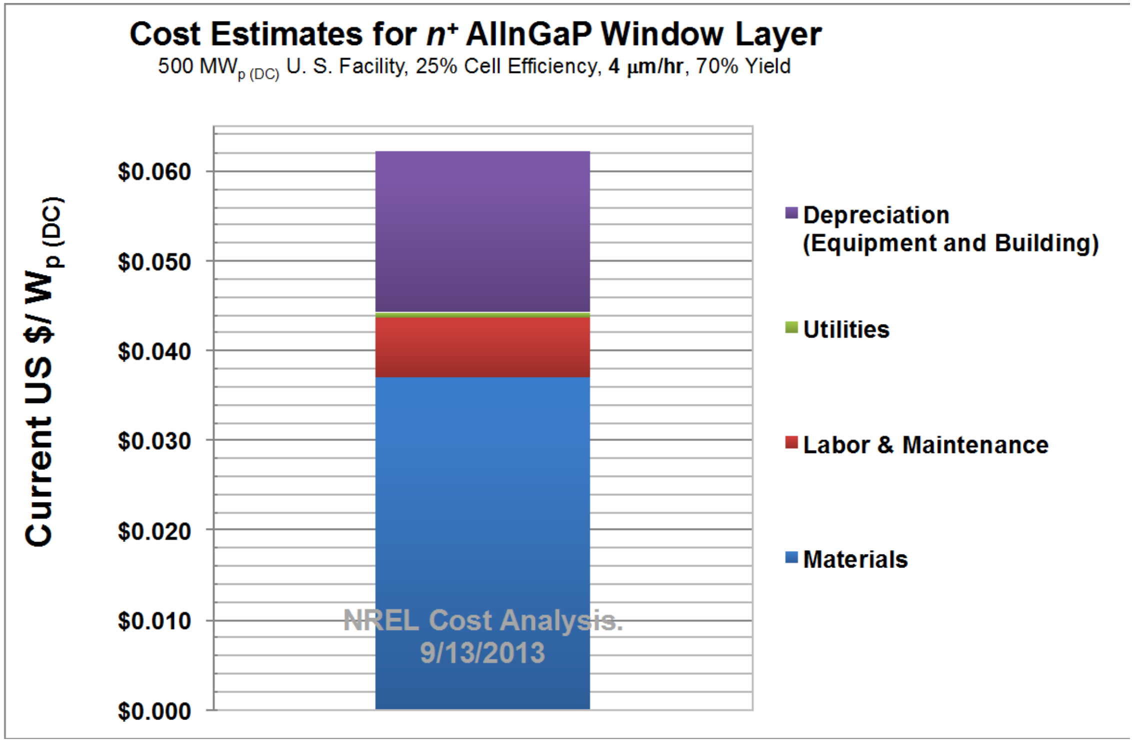
Precursor	$Al(CH_3)_3$	$In(CH_3)_3$	$Ga(CH_3)_3$	PH_3
Molar Reaction Coefficient (x, y, $1-x-y$)	0.02	0.48	0.5	1
Molecular Weight (g mol^{-1})	72.09	159.92	114.83	33.99
Material Utilization (%)	50%	50%	50%	30%
Precursor Price ($/g)	$18.00	$25.00	$2.00	$0.35
Reclamation value of spent precursor ($/ g)	$0.00	$0.00	$0.00	$0.00



4. MOVPE of AlInGaP window layer.

AlInGaP film Thickness:	25.0	nm
AlInGaP film Density:	4.48	g/cm^3

NOTE: In consideration of material quality issues, the assumed deposition rate for an AlInGaP layer (4 μm/hr) is much lower than for the GaAs layers (15 μm/hr).



Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $0.09/W

Please see the annotated notes below this slide for more details.

Page: 14

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:45 PM

1. On this slide we show the relevant manufacturing cost model inputs and results for the fourth step of the process flow shown on Slide 7. The reader should be able to recreate the results within the bar chart by using the inputs given on this slide.

2. Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the eia, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle, D. Shackelford, Do multinationals of domestic firms face higher effective tax rates?, National Bureau of Economic Research, Cambridge, MA, 2009).

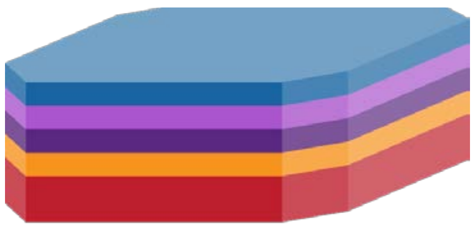
3. For the purposes of calculating the depreciation expense for steps 2 – 8 in the model process flow, it is important to note that MOVPE reactor dwell times for the temperature ramp up, pump down, and cleaning times need to be considered. For this accounting to not dwarf other details for the thinnest layers in the model device, these times are included in the Total Average Cycle Times (TACT) for the GaAs base layer step costs calculation only.

Step 5: MOVPE of *n* GaAs Emitter Layer

$Ga(CH_3)_3 + AsH_3 \longrightarrow$ GaAs + Byproducts

(e.g., CH_4)

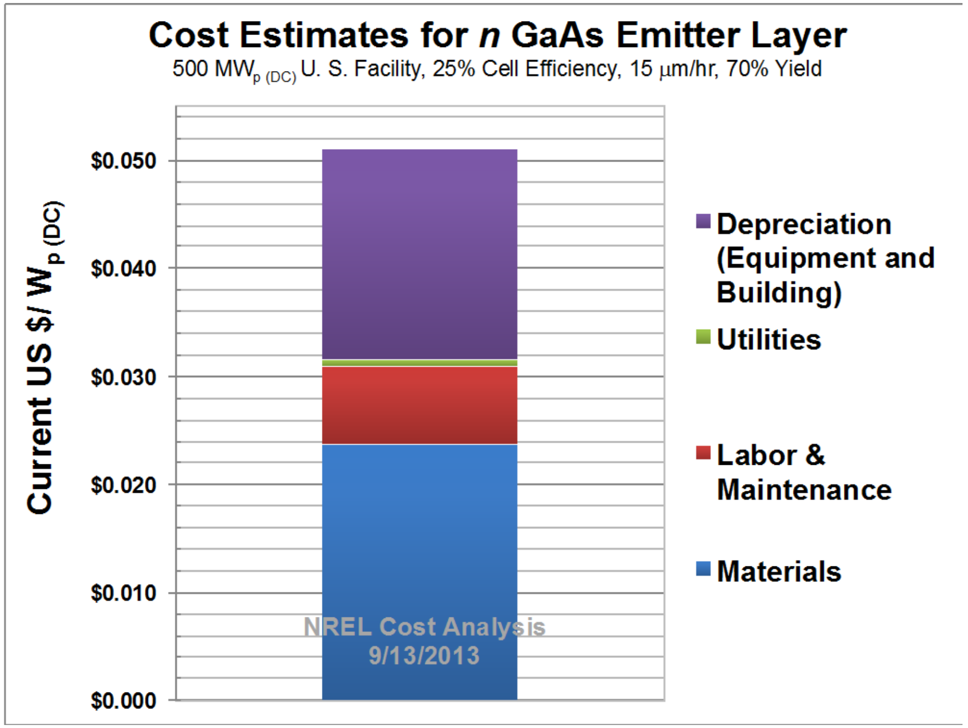
Precursor	$Ga(CH_3)_3$	AsH_3
Molecular Weight (g mol^{-1})	114.82	77.94
Material Utilization (%)	30%	20%
Precursor Price ($/g)	$2.50	$0.44
Reclamation value of spent precursor ($/ g)	$0.00	$0.00



5. MOVPE of GaAs emitter layer.

Dopants	SiH_4	Carrier Gas(es)	H_2
Dopant Concentration (atoms cm^{-3})	2.E+18		
Price ($/ Standard L)	$0.15	Utilization	100%
Utilization	5%	Net loss per run	0%

GaAs emitter film thickness:	0.100	microns
GaAs density:	5.32	g/cc



Please see the annotated notes below this slide for more details.

Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $0.10/W

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:46 PM

1. On this slide we show the relevant manufacturing cost model inputs and results for the fifth step of the process flow shown on Slide 7. The reader should be able to recreate the results within the bar chart by using the inputs given on this slide.

2. Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the eia, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle, D. Shackelford, Do multinationals of domestic firms face higher effective tax rates?, National Bureau of Economic Research, Cambridge, MA, 2009).

3. For the purposes of calculating the depreciation expense for steps 2 – 8 in the model process flow, it is important to note that MOVPE reactor dwell times for the temperature ramp up, pump down, and cleaning times need to be considered. For this accounting to not dwarf other details for the thinnest layers in the model device, these times are included in the Total Average Cycle Times (TACT) for the GaAs base layer step costs calculation only.

Step 6: MOVPE of *p* GaAs Base Layer

$$Ga(CH_3)_3 + AsH_3 \longrightarrow GaAs + Byproducts$$

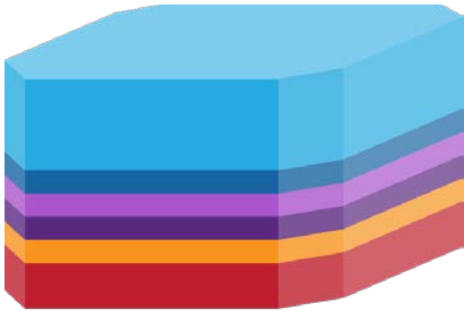
(e.g., CH_4)

GaAs base film Thickness:	2.50	microns
GaAs Density:	5.32	g/cc

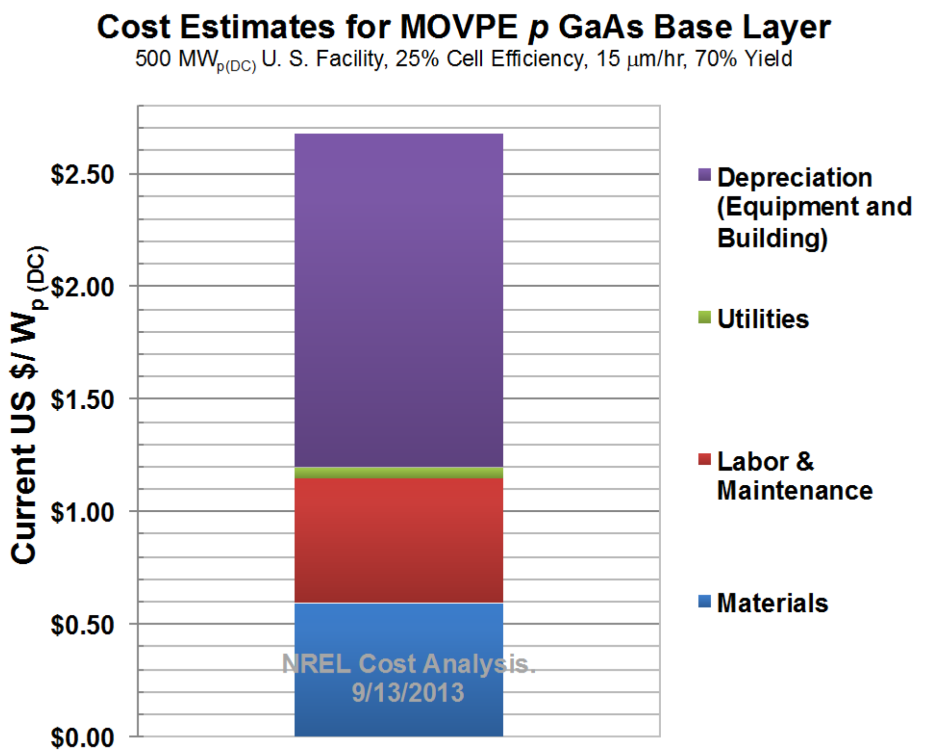
Precursor	$Ga(CH_3)_3$	AsH_3
Molecular Weight (g mol^{-1})	114.82	77.94
Material Utilization (%)	30%	20%
Precursor Price ($/g)	$2.50	$0.44
Reclamation value of spent precursor ($/ g)	$0.00	$0.00

Dopants	$Zn(C_2H_5)_2$	Carrier Gas(es)	H_2
Dopant Concentration (atoms cm^{-3})	1.E+17		
Price ($/ g)	$1.10	Utilization	100%
Utilization	5%	Net loss per run	0%

Batch Size	8.0	pieces per batch
Ramp (setup, heat) time	10.0	mins per batch
Deposition rate	15.00	µm per hour
Cleaning cycle time	1.5	hrs
Cleaning frequency	150.0	microns
Average cleaning time	1.5	mins per batch
Cool down (exit) time	10.0	mins per batch
Net TACT Time	31.5	mins per batch



6. MOVPE of GaAs base layer.



ALL temperature ramp up, pump down, and cleaning times for steps 2 – 8 are accounted for in this step of the process flow. For this reason, and because TMG is a relatively cheap III- source, the relative amount of depreciation and labor costs are higher in this MOVPE step than in others.

Please see the annotated notes below this slide for more details.

Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $7.50W

Page: 16

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:46 PM

1. On this slide we show the relevant manufacturing cost model inputs and results for the sixth step of the process flow shown on Slide 7. The reader should be able to recreate the results within the bar chart by using the inputs given on this slide.

2. Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the eia, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle, D. Shackelford, Do multinationals of domestic firms face higher effective tax rates?, National Bureau of Economic Research, Cambridge, MA, 2009).

3. For the purposes of calculating the depreciation expense for steps 2 – 8 in the model process flow, it is important to note that MOVPE reactor dwell times for the temperature ramp up, pump down, and cleaning times need to be considered. For this accounting to not dwarf other details for the thinnest layers in the model device, these times are included in the Total Average Cycle Times (TACT) for the GaAs base layer step costs calculation only.

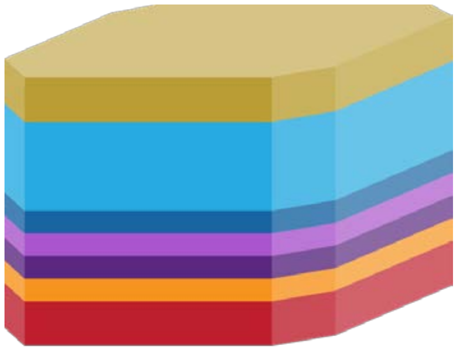
Step 7: MOVPE of p^+ InGaP BSF

$$x\mathrm{In(CH_3)_3} + (1\text{-}x)\mathrm{Ga(CH_3)_3} + \mathrm{PH_3} \longrightarrow \mathrm{In}_x\mathrm{Ga}_{1\text{-}x}\mathrm{P} + \text{Byproducts}$$

(e.g., CH_4)

Precursor	$In(CH_3)_3$	$Ga(CH_3)_3$	PH_3
Molar Reaction Coefficient (*x or 1-x*)	0.5	0.5	1
Molecular Weight (g mol^{-1})	159.92	114.83	33.99
Material Utilization (%)	50%	50%	30%
Precursor Price ($/g)	$25.00	$2.00	$0.35
Reclamation value of spent precursor ($/ g)	$0.00	$0.00	$0.00

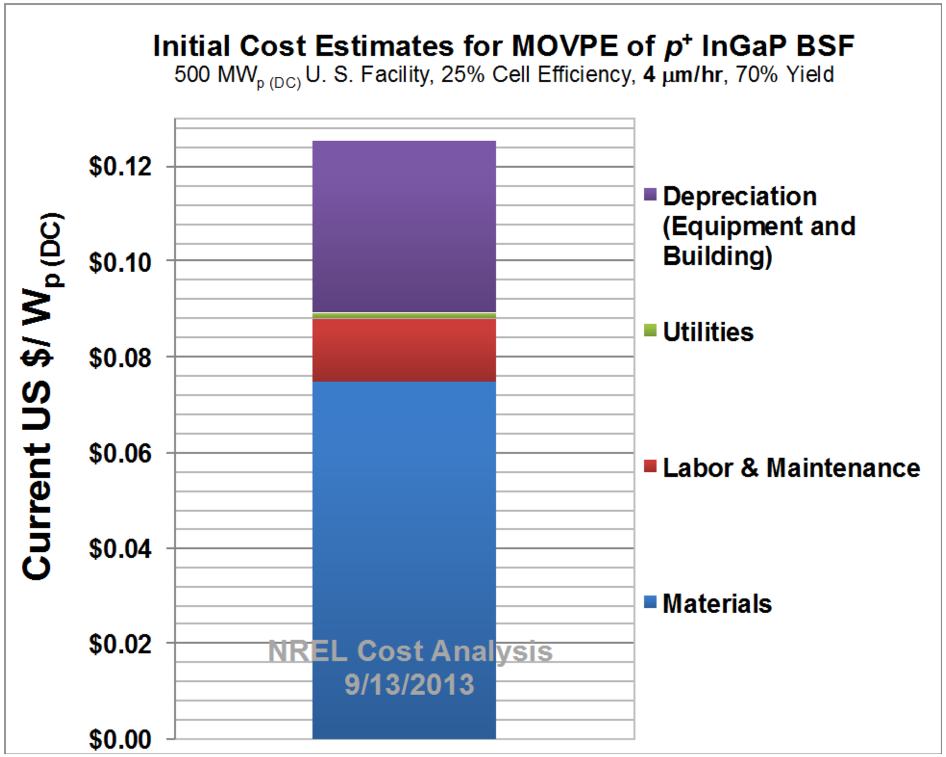
Dopants	$Zn(C_2H_5)_2$	Carrier Gas(es)	H_2
Dopant Concentration (atoms cm^{-3})	2.E+18		
Price ($/ g)	$1.10	Utilization	100%
Utilization	5%	Net loss per run	0%



7. MOVPE of InGaP BSF.

InGaP BSF film Thickness:	50.0	nm
InGaP film Density:	4.48	g/cm^3

Actual density may vary, and needs to be determined empirically.



NOTE: In consideration of material quality issues, the assumed deposition rate for the InGaP layer (4 µm/hr) is much lower than for the GaAs layers (15 µm/hr).

Please see the annotated notes below this slide for more details.

Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $0.18/W.

Page: 17

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:47 PM

1. On this slide we show the relevant manufacturing cost model inputs and results for the seventh step of the process flow shown on Slide 7. The reader should be able to recreate the results within the bar chart by using the inputs given on this slide.

2. Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the eia, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle, D. Shackelford, Do multinationals of domestic firms face higher effective tax rates?, National Bureau of Economic Research, Cambridge, MA, 2009).

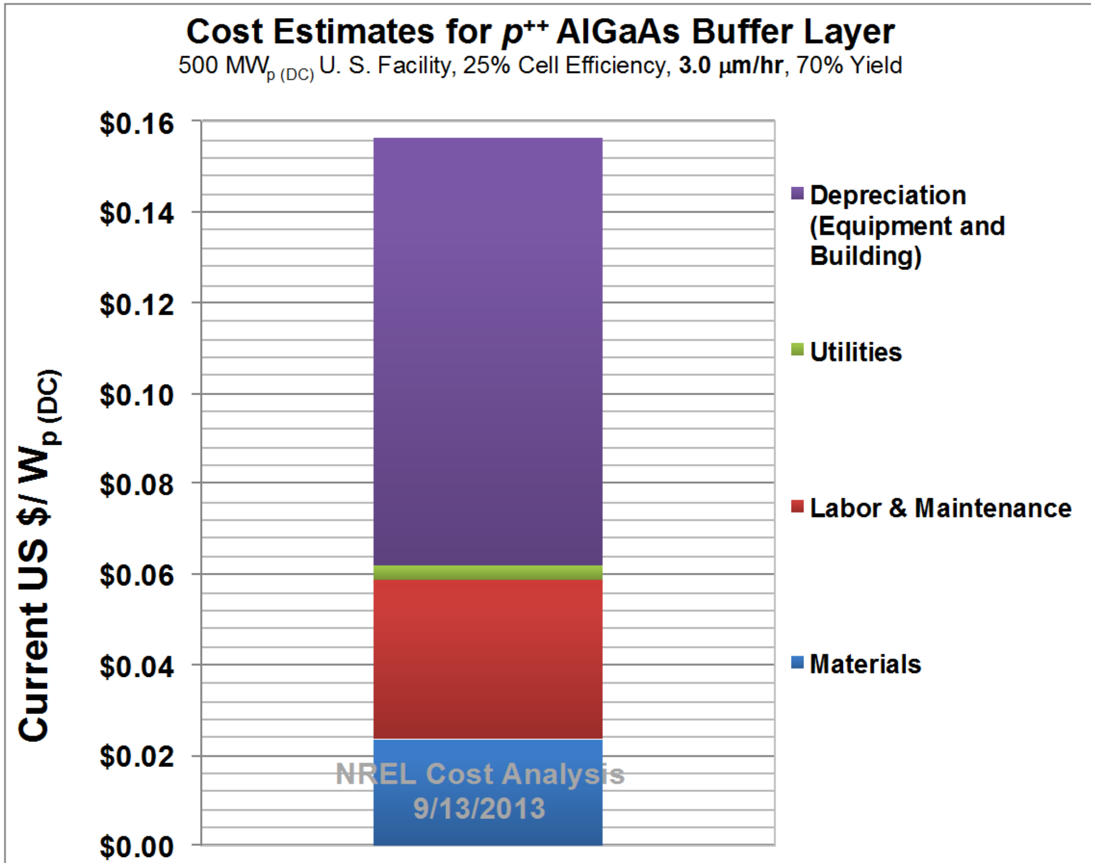
3. For the purposes of calculating the depreciation expense for steps 2 – 8 in the model process flow, it is important to note that MOVPE reactor dwell times for the temperature ramp up, pump down, and cleaning times need to be considered. For this accounting to not dwarf other details for the thinnest layers in the model device, these times are included in the Total Average Cycle Times (TACT) for the GaAs base layer step costs calculation only.

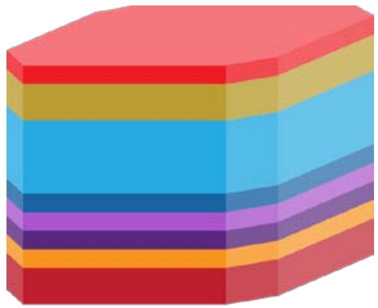
Step 8: MOVPE of p^{++} AlGaAs Contact/ Buffer Layer

$$x\mathrm{Al(CH_3)_3} + (1\text{-}x)\mathrm{Ga(CH_3)_3} + \mathrm{AsH_3} \longrightarrow \mathrm{Al}_x\mathrm{Ga}_{1\text{-}x}\mathrm{As} + \text{Byproducts}$$

(e.g., CH_4)

Precursor	$Al(CH_3)_3$	$Ga(CH_3)_3$	AsH_3
Molar Reaction Coefficient (x, $1\text{-}x$)	0.05	0.95	1
Molecular Weight (g mol^{-1})	72.09	114.82	77.94
Material Utilization (%)	30%	30%	20%
Precursor Price (\$/g)	\$18.00	\$2.50	\$0.44
Reclamation value of spent precursor (\$/ g)	\$0.00	\$0.00	\$0.00





8. MOVPE of AlGaAs contact / buffer layer.

AlGaAs contact layer thickness:	100	nm
AlGaAs Density:	4.52	g/cm^3

Actual density may vary, and needs to be determined empirically.

NOTE: In consideration of material quality issues, the assumed deposition rate for an AlGaAs layer (3.0 μm/hr) is much lower than for the GaAs layers (15 μm/hr).

Please see the annotated notes below this slide for more details.

Calculated CapEx in Depreciation for this step (500 MW scale of purchase): \$0.48/W

Page: 18

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:47 PM

1. On this slide we show the relevant manufacturing cost model inputs and results for the eighth step of the process flow shown on Slide 7. The reader should be able to recreate the results within the bar chart by using the inputs given on this slide.

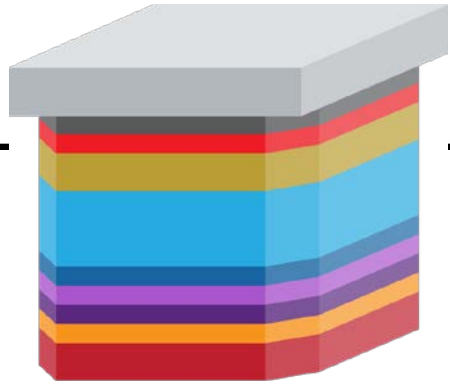
2. Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the eia, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle, D. Shackelford, Do multinationals of domestic firms face higher effective tax rates?, National Bureau of Economic Research, Cambridge, MA, 2009).

3. For the purposes of calculating the depreciation expense for steps 2 – 8 in the model process flow, it is important to note that MOVPE reactor dwell times for the temperature ramp up, pump down, and cleaning times need to be considered. For this accounting to not dwarf other details for the thinnest layers in the model device, these times are included in the Total Average Cycle Times (TACT) for the GaAs base layer step costs calculation only.

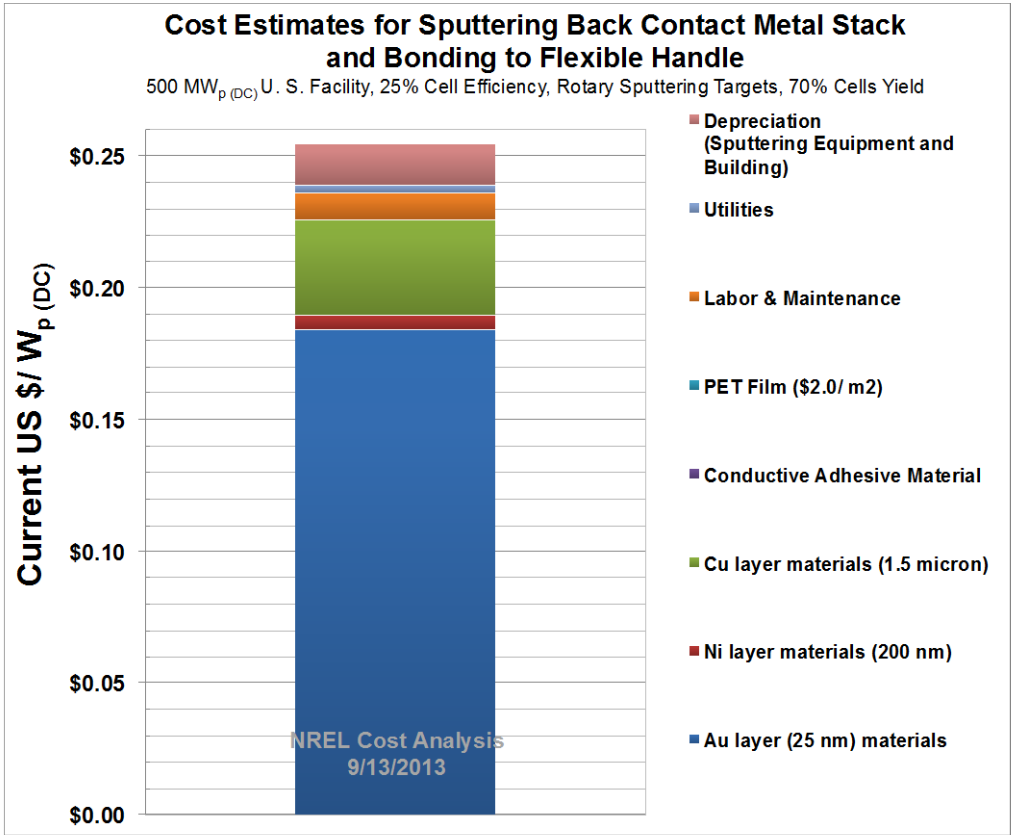
Step 9: Deposition of Back Contact Metals and Bonding of Cell to Flexible Handle (e.g., PET)

Au Density	19.3	g/cc
Dynamic Deposition Rate	145.0	nm m/min
Target Count	2	per machine
Au Target Price	$56.00	/ gram
Au Recycling value	$53.00	/gram
Au Rotary Target Utilization	80.0%	
Au Thickness	0.025	microns
Overall Substrate Collection Efficiency	59.5%	
Ni Density	8.9	g/cc
Dynamic Deposition Rate	145.0	nm m/min
Target Count	2	per machine
Ni Target Price	$0.36	/gram
Ni Recycling value	$0.00	/gram
Ni Rotary Target Utilization	80.0%	
Ni Thickness	0.2	microns
Overall Substrate Collection Efficiency	59.5%	
Cu Density	9.0	g/cc
Dynamic Deposition Rate	145.0	nm m/min
Target Count	2	per machine
Cu Target Price	$0.32	/gram
Cu Disposal value	$0.00	/gram
Cu Rotary Target Utilization	80.0%	
Cu Thickness	1.5	microns
Overall Substrate Collection Efficiency	59.5%	

The material utilizations shown are assumed for the case that rotatable sputtering targets would be utilized.



9. Deposition of back contact metals and bonding of cell to flexible handle (PET).



Please see the annotated notes below this slide for more details.

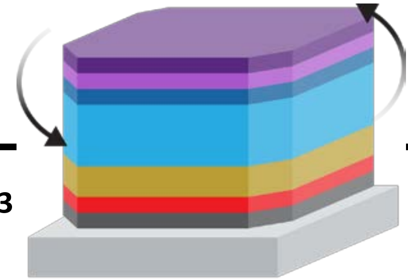
Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $0.04/W

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:47 PM

On this slide we show the relevant manufacturing cost model inputs and results for the ninth step of the process flow shown on Slide 7. The reader should be able to recreate the results within the bar chart by using the inputs given on this slide.

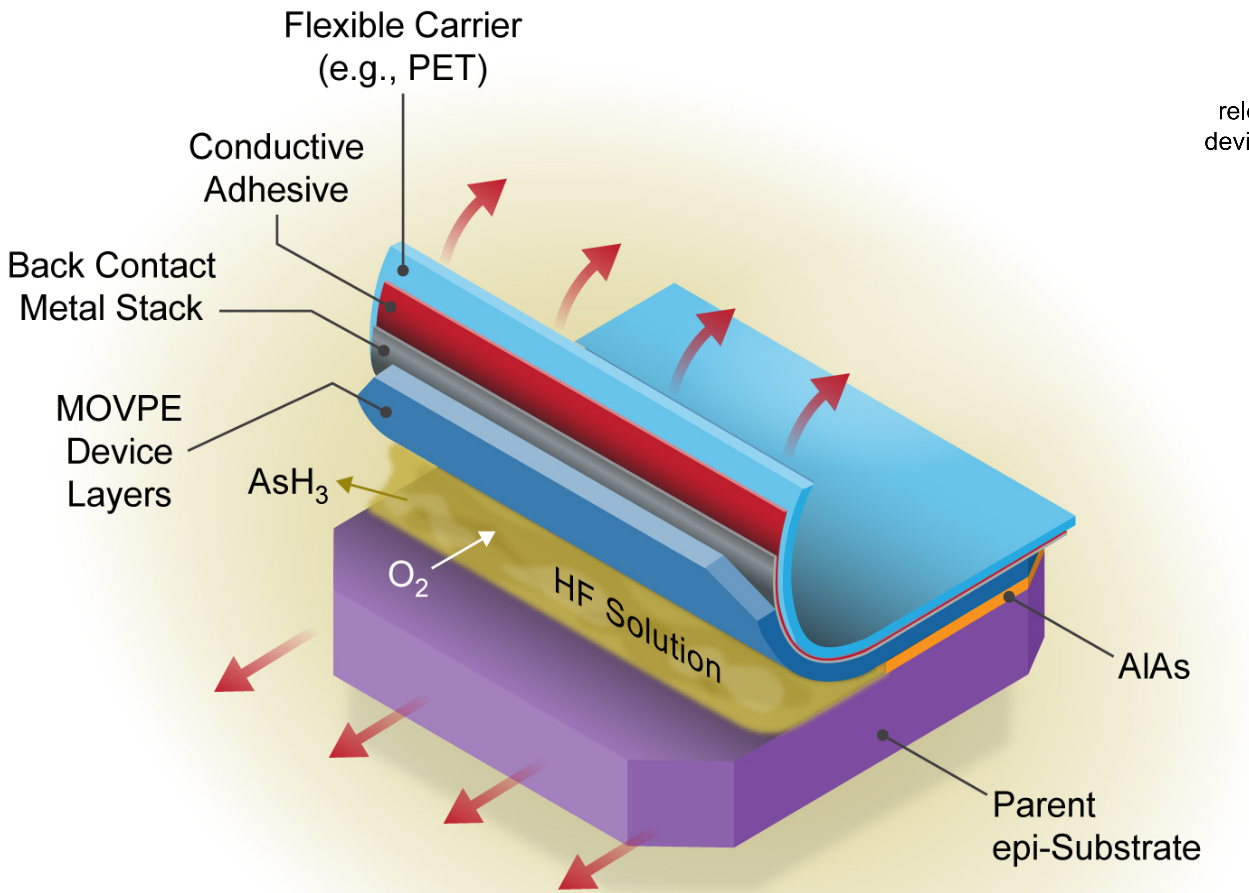
Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the eia, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle, D. Shackelford, Do multinationals of domestic firms face higher effective tax rates?, National Bureau of Economic Research, Cambridge, MA, 2009).

Step 10: Dissolution of AlAs Release Layer, and Release of MOVPE Device Layers from Parent Epi-Substrate (ELO Step)



10. Dissolution of AlAs release layer and release of MOVPE device layers from parent epi-substrate

$$AlAs + 3HF + 6H_2O \xleftrightarrow{O_2} AsH_3 + [AlF_n(H_2O)_{6-n}]^{(3-n)+} + (3-n)F^- + nH_2O \qquad n=0,1,2 \text{ or } 3$$



Lateral etch rates up to around 30 mm/ hr have been demonstrated.*

For 3" of etching, this would equate to AlAs etch times on the order of 2.5 hours.

* For example, see Schermer, J.J.; Bauhuis, G.J.; Mulder, P.; Haverkamp, E.J.; van Deelen, J.; van Niftrik, A.T.J.; Larsen, P.K. (2006). "Photon confinement in high-efficiency, thin-fill III-V solar cells obtained by epitaxial lift-off." *Thin Solid Films* 511-512; pp. 645-653.

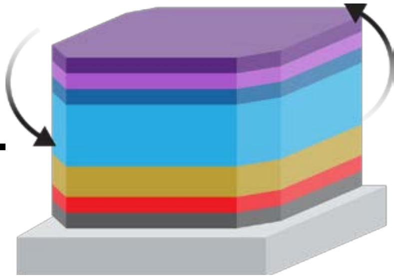
Page: 20

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:48 PM

1. Please see the given citation for an experimental demonstration of the ELO process, and for a brief description of the reaction mechanism for dissolving AlAs in HF with mechanical force and in the presence of air.

2. For more experimental details underlying the chemical mechanism for selective etching of this particular sacrificial release layer, please also see: M M A J Voncken, J J Schermer, A T J Van Niftrik, G J Bauhuis, P Mulder, P K Larsen, T P J Peters, B de Bruin, A Klassen, and J J Kelly 'Etching AlAs with HF for epitaxial lift-off applications', Journal of the Electrochemical Society 151 (2004) G347-G352.

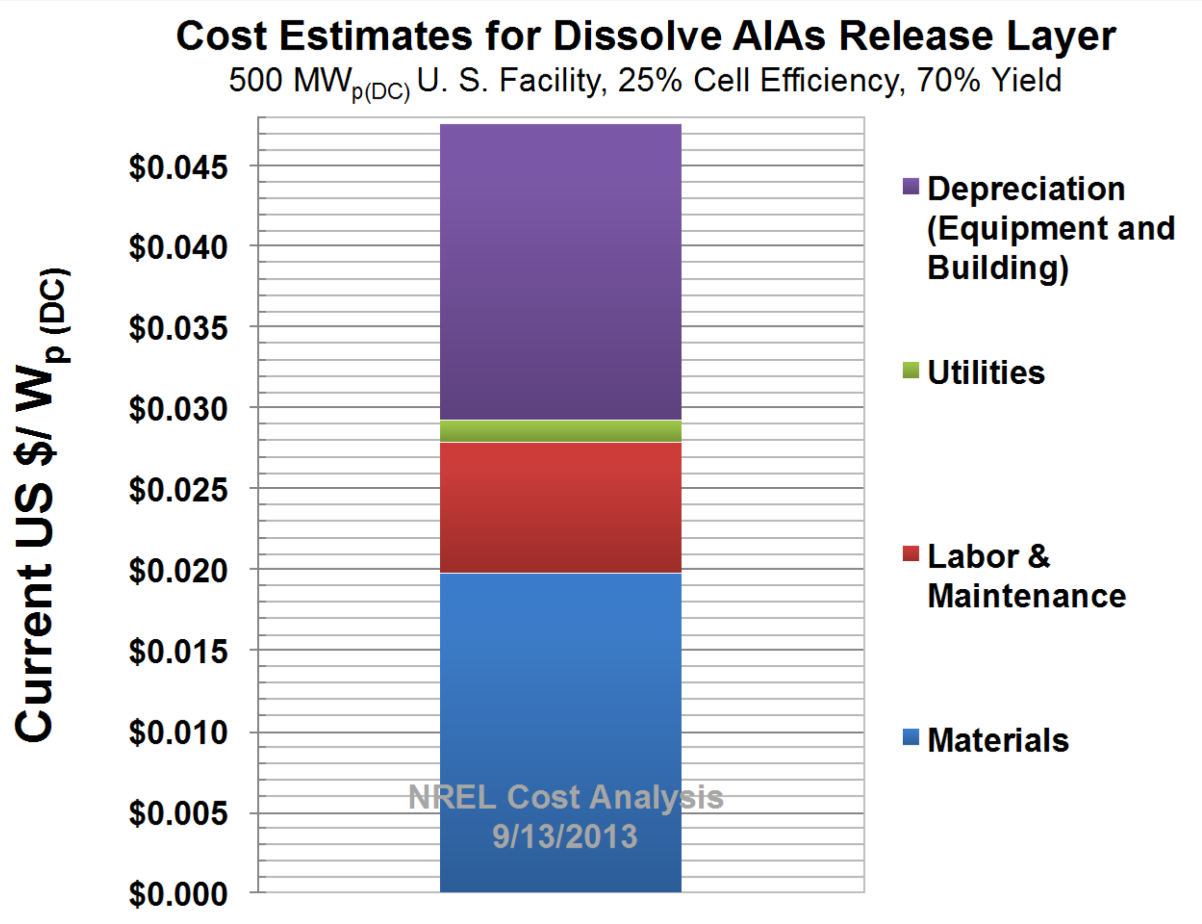
Step 10: Dissolution of AlAs Release Layer, and Release of MOVPE Device Layers from Parent Epi-Substrate (ELO Step)



10. Dissolution of AlAs release layer and release of MOVPE device layers from parent epi-substrate

The capital equipment, labor costs, etc. for a specific ELO process have not been included, primarily because the equipment for this step is not yet commercially available. The cost estimates shown, therefore, are only a proxy, which we have based upon the in-line wet bench chemical treatment used in c-Si surface texturing.

The cells may also need to be 'diced' into smaller areas.



Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $0.092/W

Please see the annotated notes below this slide for more details.

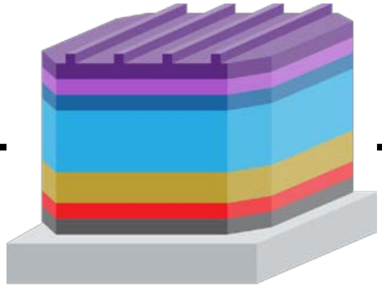
Page: 21

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:48 PM

On this slide we show the relevant manufacturing cost model inputs and results for the tenth step of the process flow shown on Slide 7. The materials costs for this step are based upon wet-bench chemistry borrowed from c-Si manufacturing cost models (with the surface texturing process serving as a proxy).

Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the eia, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle, D. Shackelford, Do multinationals of domestic firms face higher effective tax rates?, National Bureau of Economic Research, Cambridge, MA, 2009).

Step 11: Etching of n^{++} GaAs Contact Layer

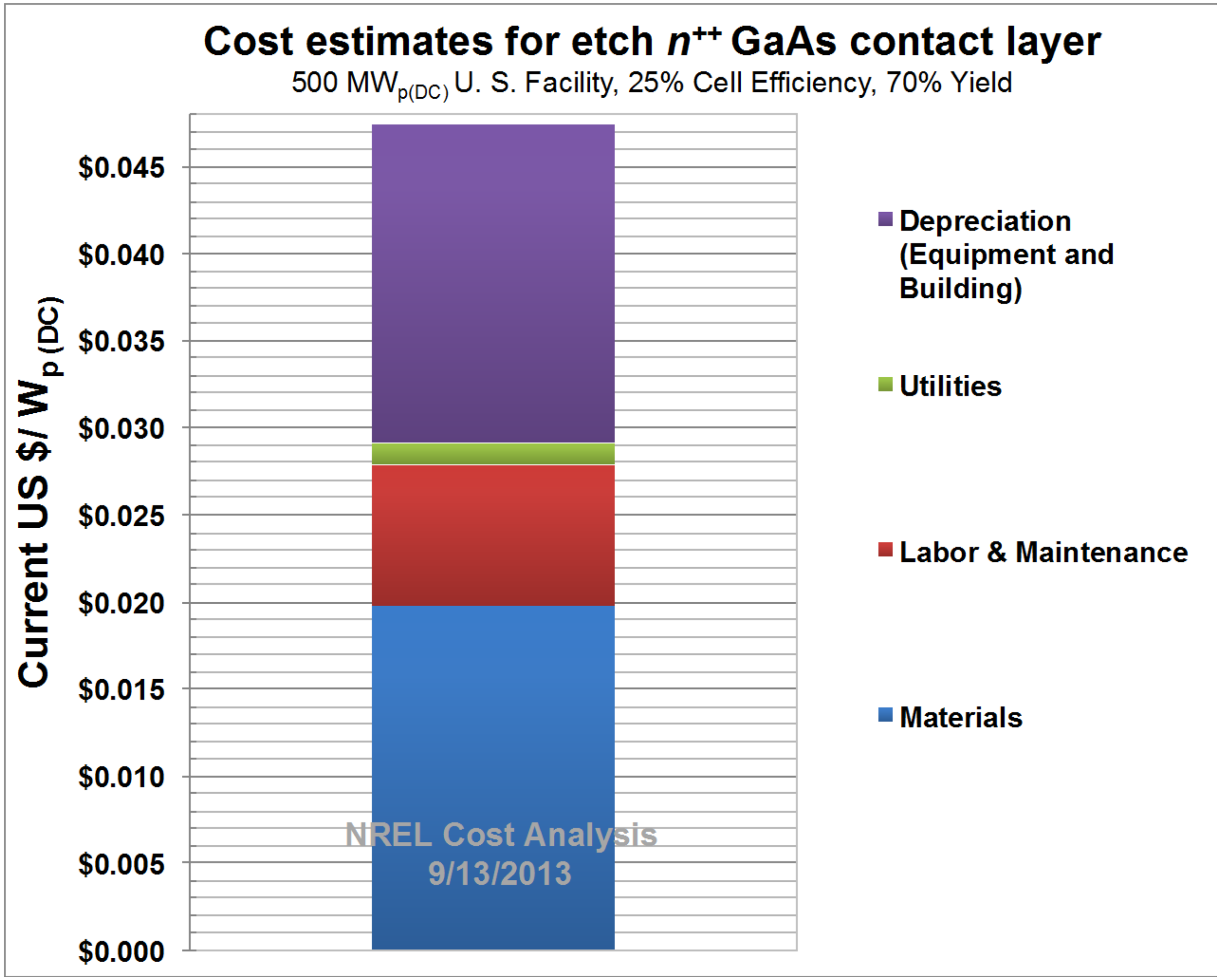


11. Etching of contact layer.

- Cost of ownership estimates are again based upon a proxy borrowed from the in-line wet bench chemical treatment used in c-Si surface texturing.
- One may also need to consider the need for lithography in this etching step, which is not included in these cost estimates.

Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $0.092/W

Please see the annotated notes below this slide for more details.



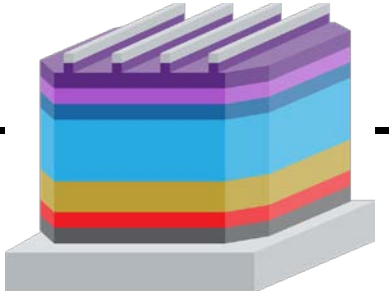
Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:48 PM

On this slide we show the relevant manufacturing cost model inputs and results for the eleventh step of the process flow shown on Slide 7. The materials costs for this step are based upon wet-bench chemistry borrowed from c-Si manufacturing cost models (with the surface texturing process serving as a proxy).

Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the eia, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle, D. Shackelford, Do multinationals of domestic firms face higher effective tax rates?, National Bureau of Economic Research, Cambridge, MA, 2009).

Step 12: Frontside Metallization

(Electroplating of Cu Alloy with Ni Diffusion Barrier)



12. Frontside metallization.

Frontside metal plating recipe:

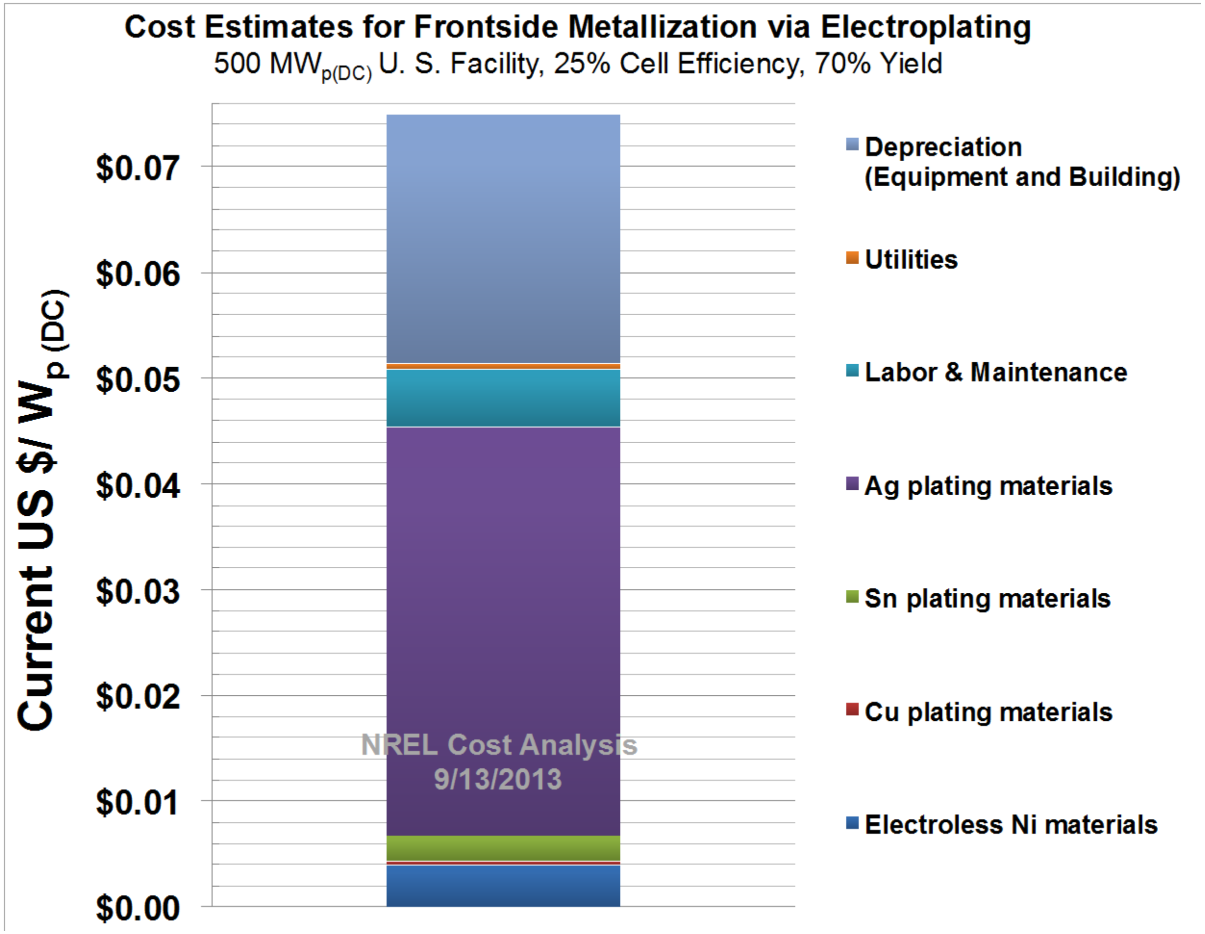
(1) Electroless Ni diffusion barrier
Width: 5.0 µm, Height: 1.0 µm

(2) Electroplated Cu
Width: 40. µm, Height: 3.0 µm

(3) Electroplated Sn
Width: 40. µm, Height 3.0 µm

(4) Electroplated Ag
Width: 40. µm, Height: 8.0 µm

For a description of this frontside metallization approach, please see:
"A Wafer-Based Monocrystalline Silicon Photovoltaics Roadmap: Utilizing Known Technology Improvement Opportunities for Further Reductions in Manufacturing Costs." (2013). *Solar Energy Materials and Solar Cells* 114; pp. 110–135.



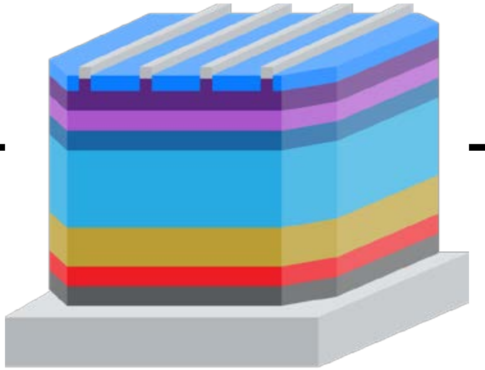
Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $0.12/W

Page: 23

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:49 PM

These frontside metallization costs are also borrowed from our c-Si manufacturing cost models. For a more complete description, the reader is referred to: A Goodrich, P Hacke, Q Wang, B Sopori, R Margolis, T L James and M Woodhouse. “A Wafer-Based Monocrystalline Silicon Photovoltaics Roadmap: Utilizing Known Technology Improvement Opportunities for Further Reductions in Manufacturing Costs.” (2013). Solar Energy Materials and Solar Cells 114; pp. 110–135.

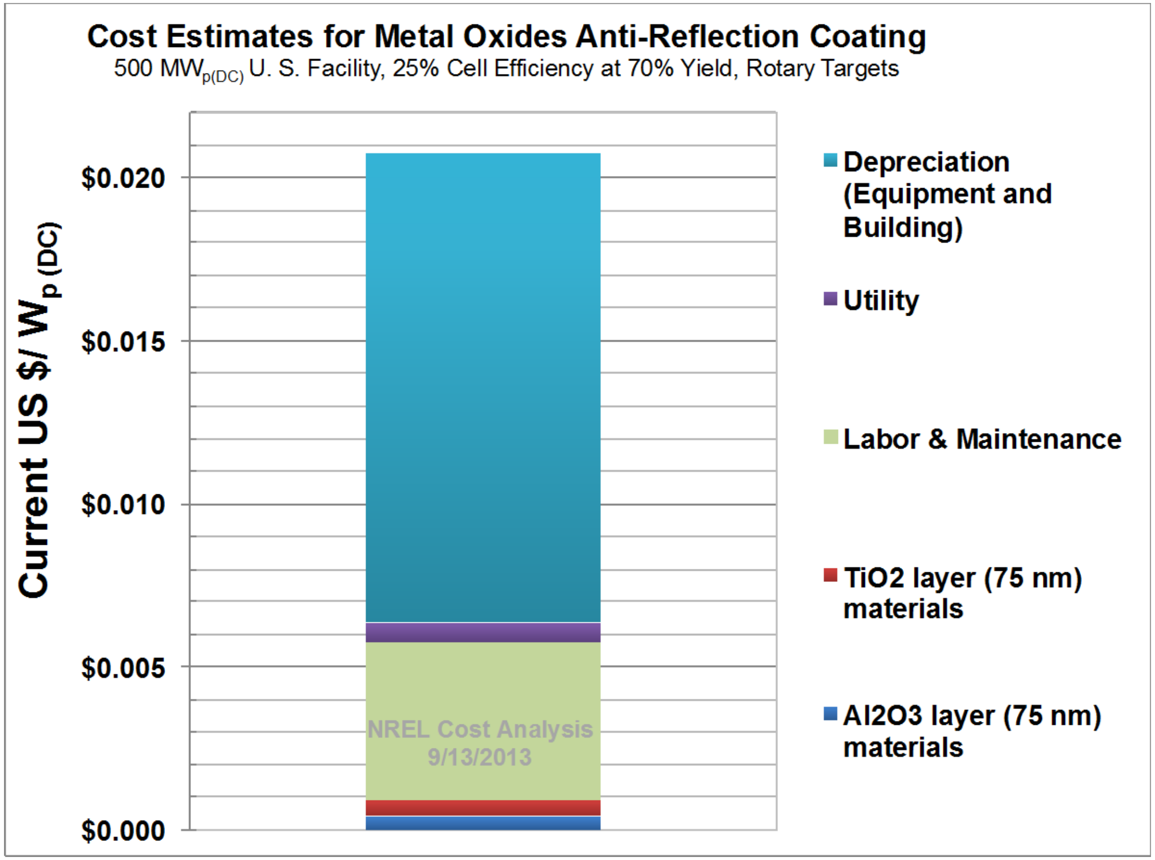
Step 13: Deposit AR Coating



13. Deposit AR coating.

Al_2O_3 Density	3.95	g/cc
Dynamic Deposition Rate	145.0	nm m/min
Target Count	2.0	per machine
Al_2O_3 Target Price	$0.168	/gram
Al_2O_3 Recycling value	$0.00	/gram
Al_2O_3 Target Utilization	80.0%	
Al_2O_3 Thickness	75	nm
Substrate Collection Efficiency	59.5%	
TiO_2 Density	4.27	g/cc
Dynamic Deposition Rate	100.0	nm m/min
Target Count	2.0	per machine
TiO_2 Target Price	$0.190	/gram
TiO_2 Recycling value	$0.00	/gram
TiO_2 Target Utilization	80.0%	
TiO_2 Thickness	75	nm
Substrate Collection Efficiency	59.5%	

The material utilizations are relevant to rotatable sputtering targets.



Please see the annotated notes below this slide for more details.

Calculated CapEx in Depreciation for this step (500 MW scale of purchase): $0.045/W

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:49 PM

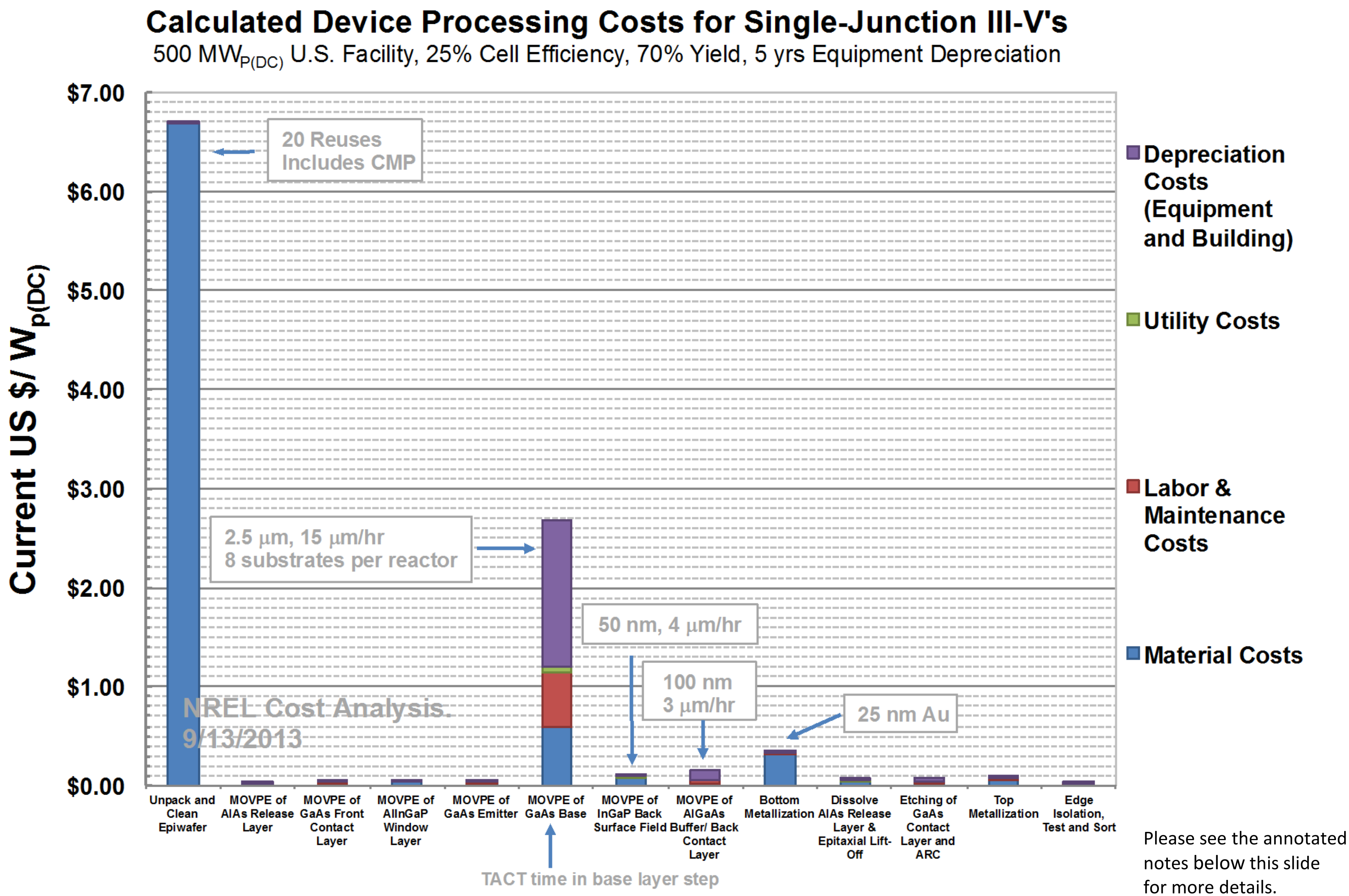
On this slide we show the relevant manufacturing cost model inputs and results for the thirteenth step of the process flow shown on Slide 7. The reader should be able to recreate the results within the bar chart by using the inputs given on this slide.

Other key input assumptions for a U.S.-based manufacturing costs calculation include:
(a) 0.25 laborers per reactor and 1:0.35 Direct:Indirect labor ratio. For wages we assume $12.05 /hr unskilled labor rate, $17.56/hr skilled labor rate, and 55% benefits on wages (based upon data from the U.S. Bureau of Labor Statistics, which is available online at: http://www.bls.gov/ncs/ect/home.html).
(b) 350 working days per year and 24 working hours per day
(c) Electricity price of $0.07/kWh (based upon the most recent industrial average electricity price from the eia, which is available online at: http://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a)
(d) Class 1000 cleanroom cost of $500/m2 (based upon input provided by an industry collaborator).
(e) An average effective corporate tax rate of 28% (based upon S. Markle, D. Shackelford, Do multinationals of domestic firms face higher effective tax rates?, National Bureau of Economic Research, Cambridge, MA, 2009).

In the bar chart shown above, the reader may notice relatively high calculated costs for Depreciation, Labor, and Maintenance relative to Materials. This result stems from the assumption of very thin layers for the AR coating, thus giving very low materials costs; and also after accounting for sputtering chamber pump down and venting and maintenance times in the total average cycle times for the sputtering equipment. The result is relatively higher costs for depreciation and maintenance relative to materials.

Cost Summary, by Step, for the Reference Case.

(20 substrate reusages, precursor utilizations of 30% for the III- source and 20% for the V- source, 15 μm/hr GaAs, 70% effective cell yield)



Please see the annotated notes below this slide for more details.

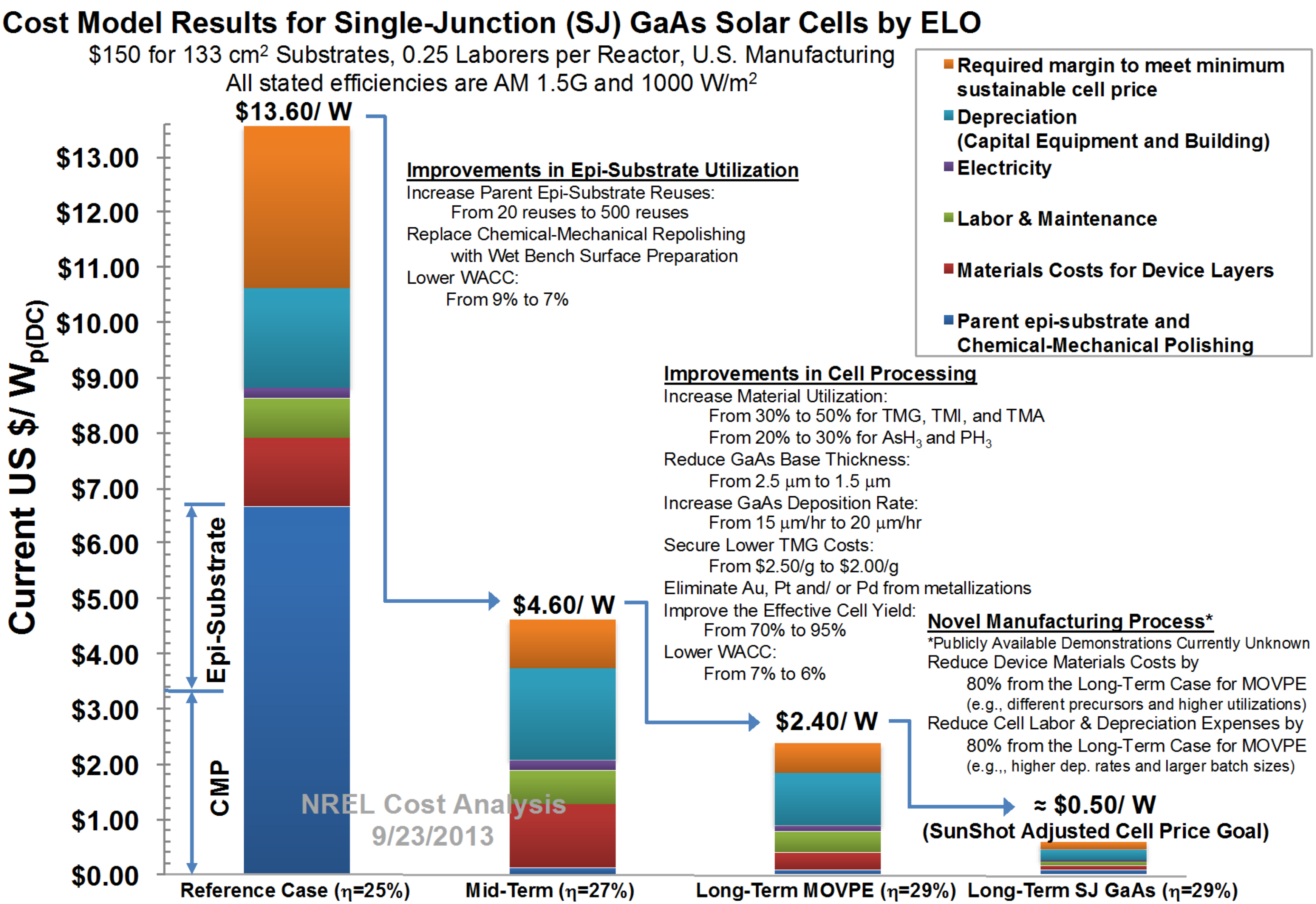
Page: 26

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:50 PM

This slide shows the costs for each step in the 'Reference Case' scenario for single-junction GaAs.

For steps 2-8 of the model process flow, the times for MOVPE reactor chamber atmosphere preparation, temperature ramp up, temperature ramp down, and maintenance are all included in the GaAs base layer step only. Please see slide 16 for the specific times assumed. Of course, the total calculated depreciation expense for the GaAs base layer step also depends upon the deposition rate and thickness. The total average cycle time (TACT) is, therefore, highest in that step and is inclusive of more factors than what is included in steps 2 -- 5, 7 and 8 of the model process flow.

Technology Roadmap Simulations for Single-Junction III-V's (GaAs Base)



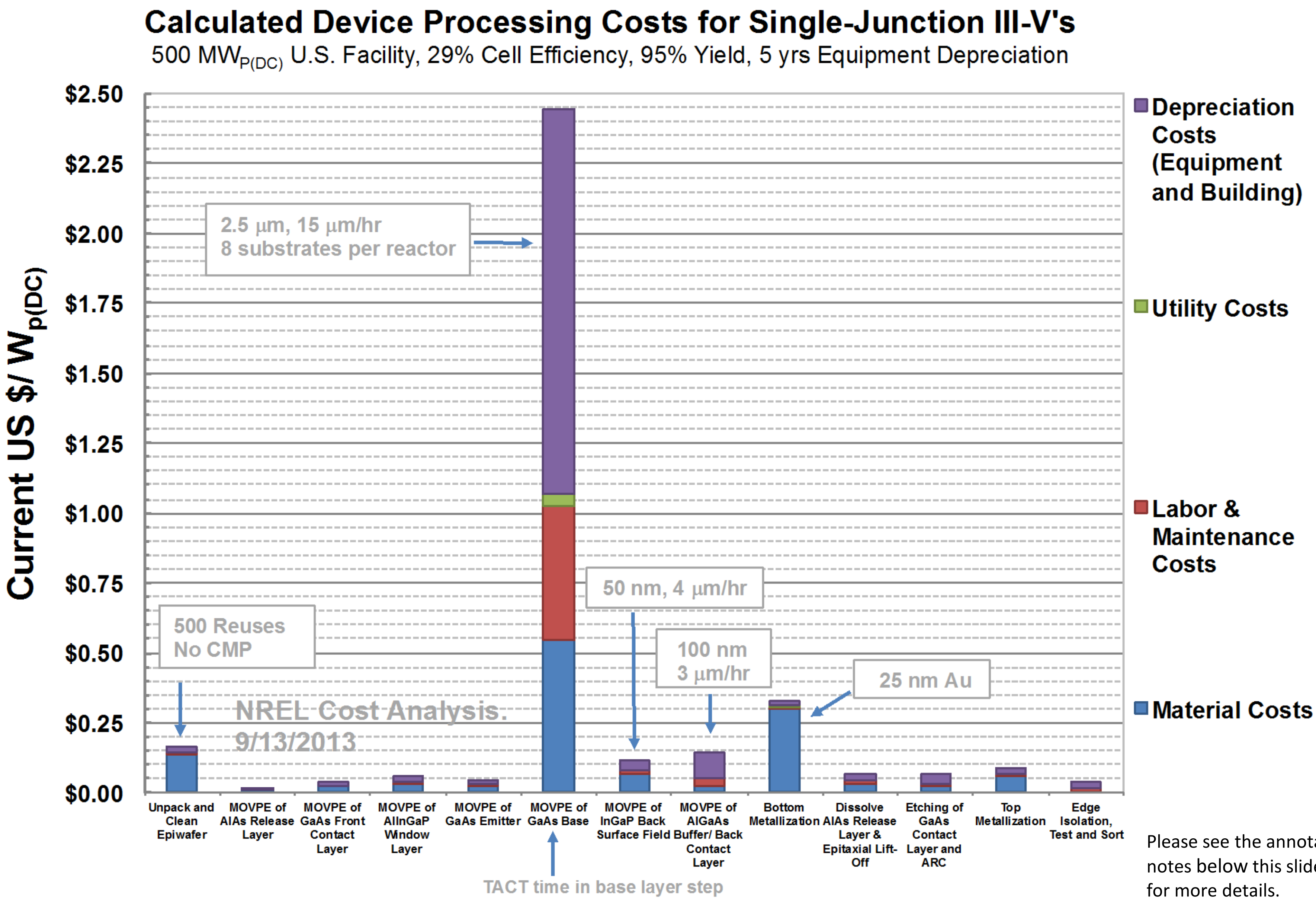
Page: 27

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:50 PM

This slide again shows the sum of costs for the 'Reference Case' scenario, and also highlights select technology pathways to lower manufacturing costs from that scenario. In the Mid-Term and Long-Term cases, we highlight what are currently believed to be practically achievable targets in cell processing—based upon numerous conversations with NREL researchers and industry collaborators—for solid III-V films deposited by MOVPE.

Cost Summary, by Step, in the Mid-Term Single-Junction Case

(500 epi- parent substrate reusages; precursor utilizations of 30% for the III- source and 20% for the V- source; 20 µm/hr GaAs)



Please see the annotated notes below this slide for more details.

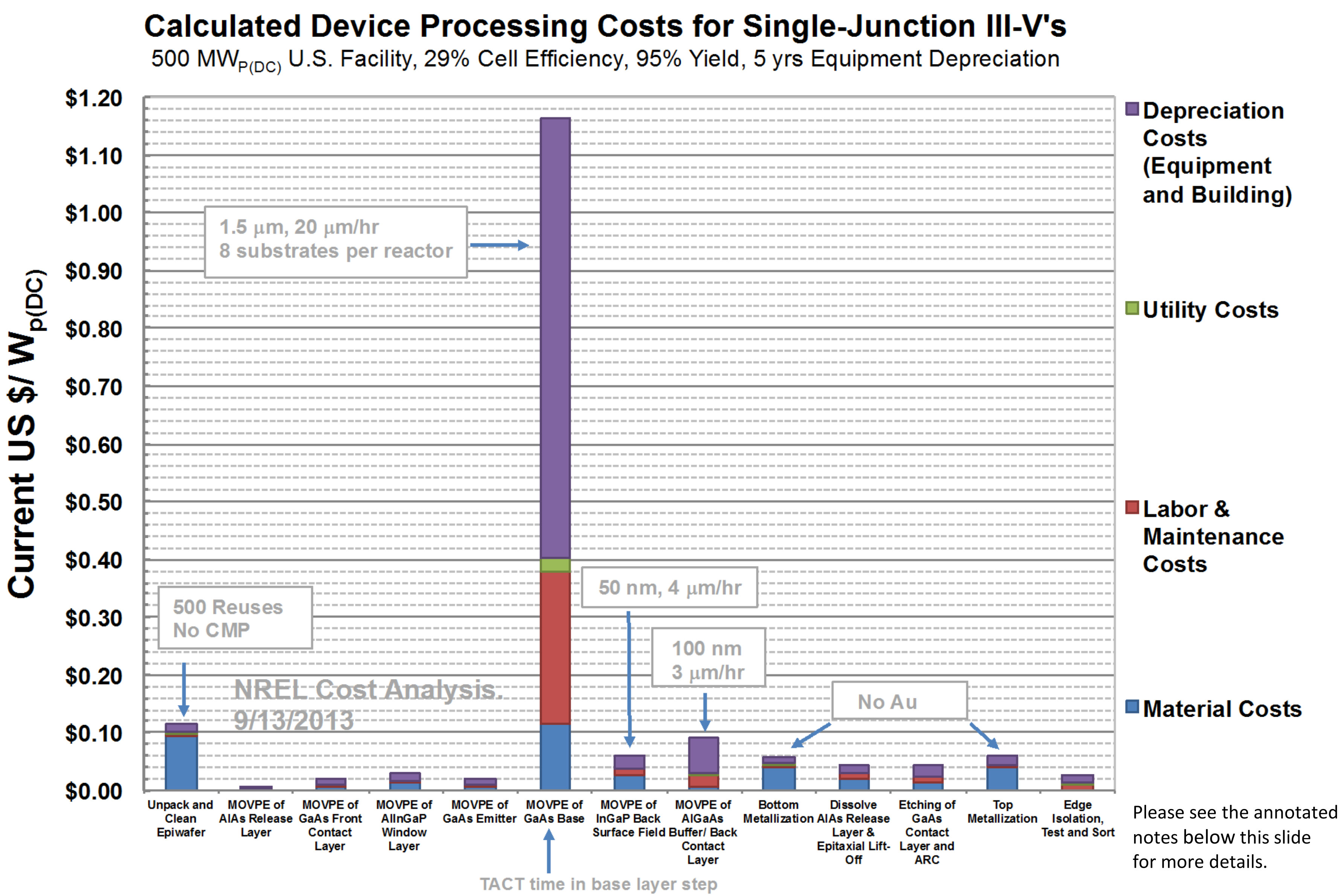
Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:51 PM

This slide shows the costs for each step of the process flow shown on slide 7 under the ‘Mid-Term’ technology scenario.

For steps 2-8 of the model process flow (slide 7), the times for MOVPE reactor chamber atmosphere preparation, temperature ramp up, temperature ramp down, and maintenance are all included in the GaAs base layer step only. Please see slide 16 for the specific times assumed. Of course, the total calculated depreciation expense for the GaAs base layer step also depends upon the deposition rate and thickness. The total average cycle time (TACT) is, therefore, highest in that step and is inclusive of more factors than what is included in steps 2 -- 5, 7 and 8 of the model process flow.

Cost Summary, by Step, in the Long-Term Single-Junction MOVPE Case

(500 epi- parent substrate reusages; precursor utilizations of 50% for the III- source and 30% for the V- source; 20 µm/hr GaAs)



Please see the annotated notes below this slide for more details.

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:51 PM

This slide shows the costs for each step of the process flow shown on slide 7 under the 'Long-Term' technology scenario.

For steps 2-8 of the model process flow (slide 7), the times for MOVPE reactor chamber atmosphere preparation, temperature ramp up, temperature ramp down, and maintenance are all included in the GaAs base layer step only. Please see slide 16 for the specific times assumed. Of course, the total calculated depreciation expense for the GaAs base layer step also depends upon the deposition rate and thickness. The total average cycle time (TACT) is, therefore, highest in that step and is inclusive of more factors than what is included in steps 2 -- 5, 7 and 8 of the model process flow.

Final Considerations for III-V Cells Serving Directly as Drop-In Replacements for c-Si Cells (Without Optical Concentration).

Balance of Materials Costs for Single-Junction GaAs Cells Serving as Drop-In Replacements into 2.26 m^2 c-Si designed modules (η=29%)	
Material	**Cost Assumptions**
Long-term cell prices	≈$0.50/$W_p$
Stringing and tabbing ribbons, metal solder and bus bars	$2.5/module
J-box containing the bypass diodes	$4.5/module
J-box sealant, bonding tape or edge seal, printed module sticker label and bus bar covers	$1.5/module
Aluminum frame	$20/module
EVA (2 sheets needed)	$3.50/$m^2$ for each sheet
Bottom-side film or glass	$6 /$m^2$
Premium Front Glass: 4.0 mm, low [Fe], tempered, with AR coating	$16/$m^2$
Total estimated module materials costs	**≈ $0.60/$W_{p(DC)}$**

Page: 30

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:51 PM

This slide represents typical balance-of-module materials costs if such cells were to serve as drop-in replacements into existing c-Si manufacturing. It does not include the depreciation, labor, etc. expenses for module assembly. For those costs, the reader is referred to: A Goodrich, P Hacke, Q Wang, B Sopori, R Margolis, T L James and M Woodhouse “A Wafer-Based Monocrystalline Silicon Photovoltaics Roadmap: Utilizing Known Technology Improvement Opportunities for Further Reductions in Manufacturing Costs.” (2013). Solar Energy Materials and Solar Cells 114; pp. 110–135.

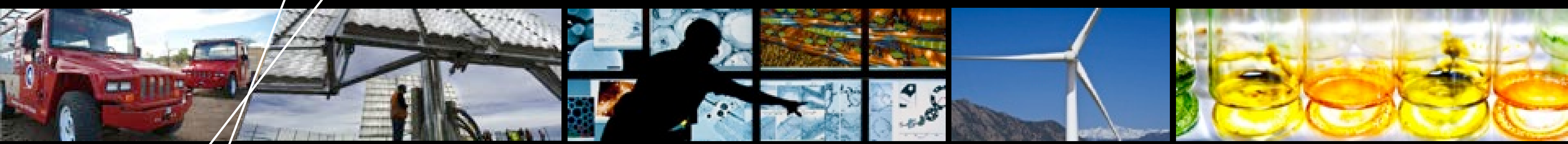
While being a simplification from a levelized-cost-of-energy (LCOE) metric, the the U.S. Department of Energy’s ‘SunShot’ goal is broadly defined as $1/W installed utility-scale PV system prices or $1.5/W installed residential-scale PV system prices. As a first-order approximation, using incumbent technologies already in mass production the model PV systems might then be comprised of circa 20% efficient modules having a price of $0.50/W—thus leaving an allowed budget for balance-of-systems of around $0.50/W for utility-scale systems or around $1.0/W for residential systems.

If higher than 20% efficiency modules were to be deployed, however, then lower balance-of-systems costs can be expected if the mounting configuration, labor requirements, land area, etc., are the same. For the case of 29% modules versus 20% modules, under this assumption of constancy we estimate a balance-of-systems price savings of around $0.10/W for the higher efficiency modules--thus leading to a module price that could hypothetically be $0.10/W higher and still reaching the $1/W system price goal.* Given the typical balance-of-module materials shown above, the ‘SunShot adjusted cell price’ goal shown in slide 27 is calculated to reach this hypothetical $0.60/W module price target.

*For a rationale of these cost-efficiency adjustments, please see: A Goodrich, T James, and M Woodhouse, ‘Residential, Commercial, and Utility-Scale Photovoltaic System Prices in the United States: Current Drivers and Cost Reduction Opportunities’ (2012). Available online at: http://www.nrel.gov/docs/fy12osti/53347.pdf.

NREL
NATIONAL RENEWABLE ENERGY LABORATORY

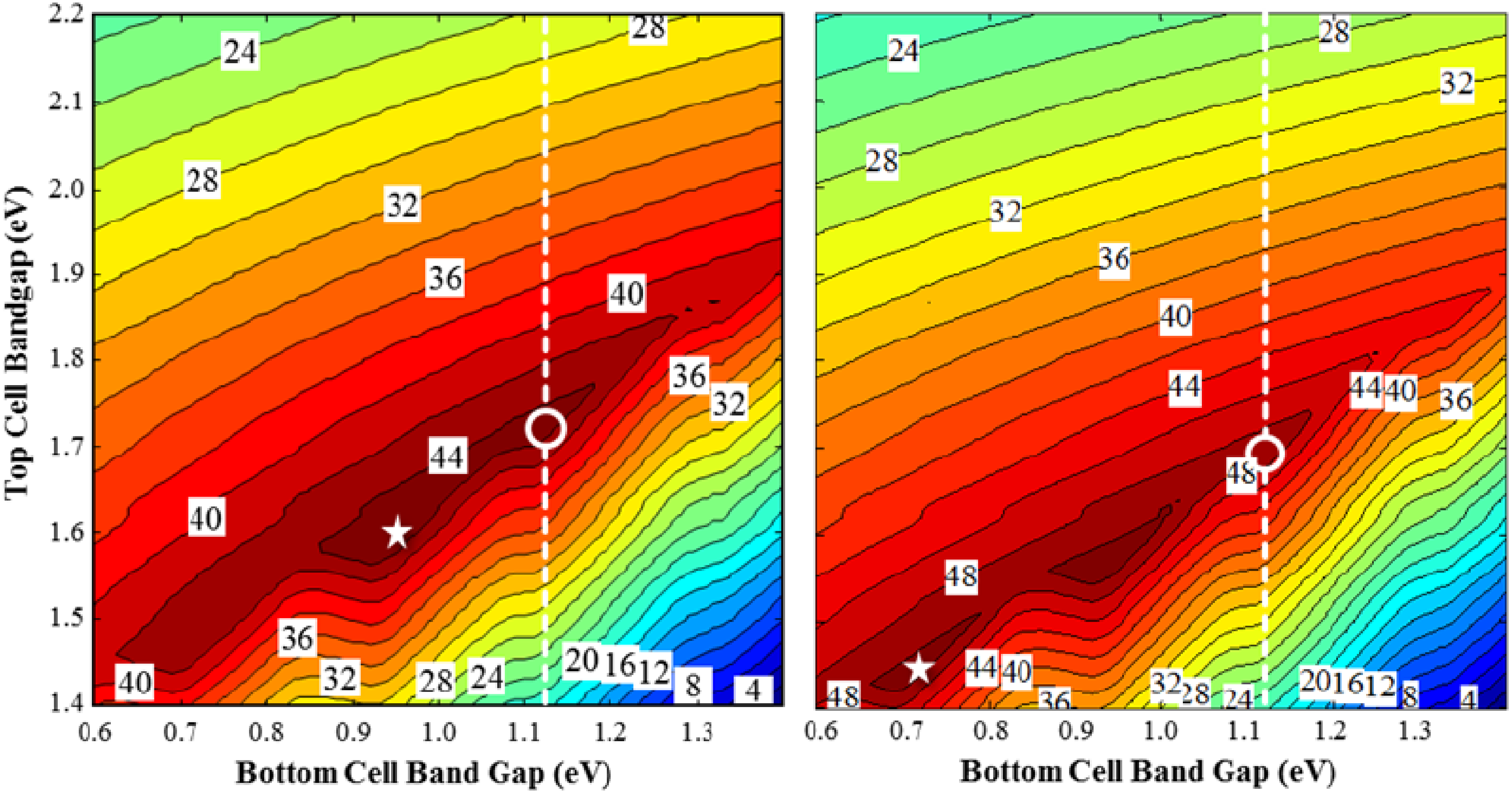
Two Cases for Dual-Junction Solar Cells



(1) III-V Top Cells via MOVPE on *Czochralski*-Grown Silicon Bottom Cells

(2) $In_{0.5}Ga_{0.5}P$ Top Cells on GaAs Bottom Cells via MOVPE & ELO

What Are the Desirable Properties for a Dual-Junction Solar Cell?



(Left) AM 1.5G, and (Right) 100 x AM1.5D dual-junction solar cell efficiency contours in the Shockley-Queisser limit. The dashed line with a circle represents a fixed Si bottom cell and the associated local maximum in efficiency.

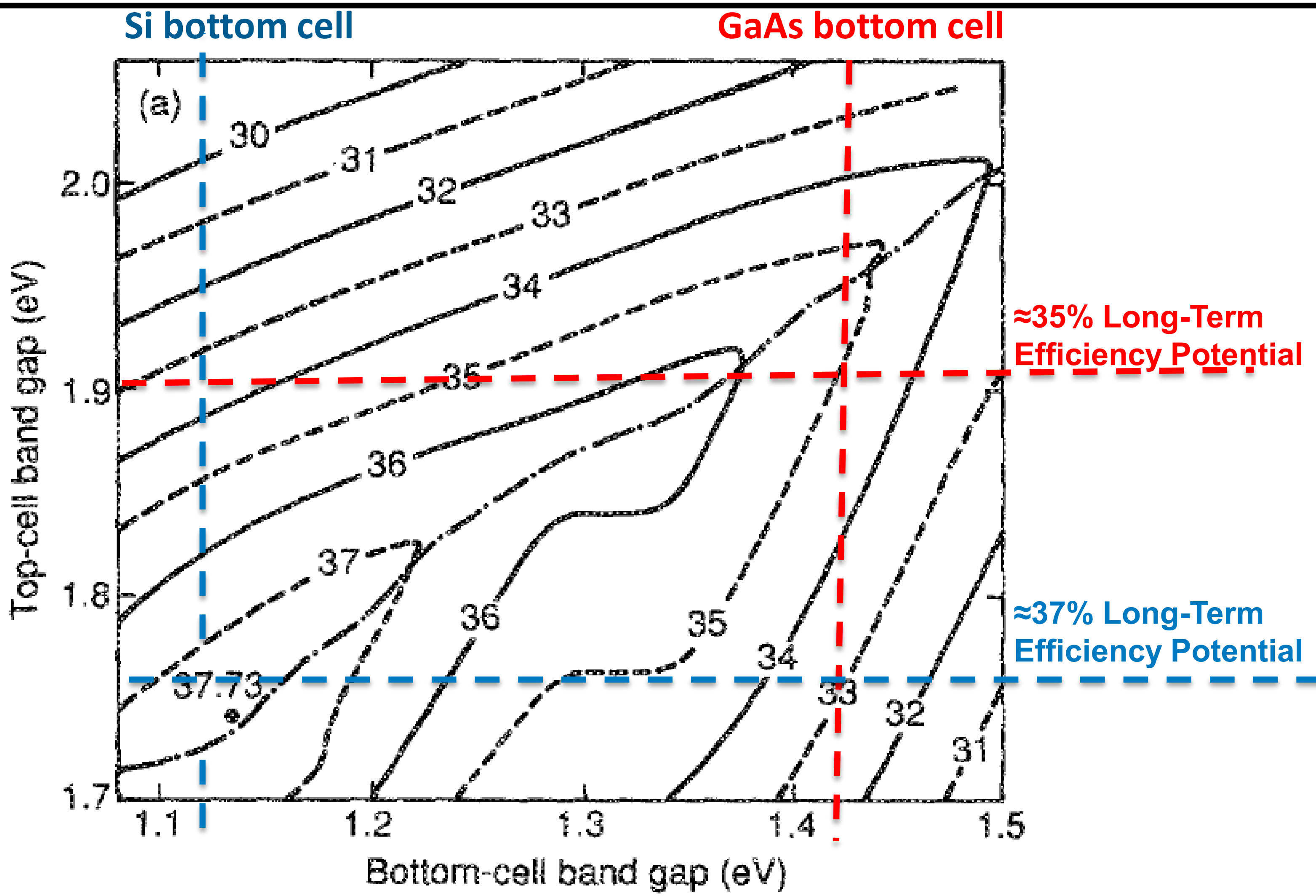
From Grassman, T.J.; Carlin, J.A.; Ratcliff, C.; Chmielewski, D.J.; Ringel, S.A. (2013). "Epitaxially-Grown Metamorphic GaAsP/Si Dual-Junction Solar Cells." *Proceedings of the IEEE PVSC.*

Page: 32

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:52 PM

This slide represents an analysis of maximum possible efficiencies for dual-junction solar cells made from top and bottom cells having different bandgaps. The reader is referred to the reference cited for more details.

What Are the Desirable Properties for a Dual-Junction Solar Cell?



Isoefficiency plots for two-junction, series connected tandem structures under AM 1.5G one-sun illumination. In this analysis, reasonable values for J_o, μ, τ, etc. are incorporated into the efficiency projections (not just Shockley-Quiesser).

From "Modeling of two-junction, series-connected tandem solar cells using topcell thickness as an adjustable parameter" Sarah Kurtz, P Faine, and Jerry Olson *Journal of Applied Physics* **68** 1890 (1990); doi:10.1063/1.347177.

Page: 33

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:52 PM

This slide represents the more practically achievable efficiencies for dual-junction solar cells made from top and bottom cells having different bandgaps. Please see the reference cited for more details.

But III-Vs on Si is Not a New Idea

14.5% conversion efficiency GaAs solar cell fabricated on Si substrates

Yoshio Itoh, Takashi Nishioka, Akio Yamamoto, and Masafumi Yamaguchi
NTT Electrical Communications Laboratories, Tokai, Ibaraki 319–11, Japan

(Received 15 July 1986; accepted for publication 14 October 1986)

AlGaAs-GaAs heteroface p^+-p-n solar cells have been fabricated directly on Si substrates using metalorganic chemical vapor deposition. GaAs on Si solar cell efficiency as high as exceeding 14.5% at AM1.5 was obtained by cleaning the substrate surface and repeating GaAs film growth interruption. This value is the highest ever reported for GaAs solar cells on Si substrates. Defects, which could not be observed in homoepitaxially grown GaAs film, were observed in the heteroepitaxial GaAs films through electron beam induced current image. Relatively low conversion efficiency of the GaAs cell on Si compared to the GaAs can be attributed to these defects.

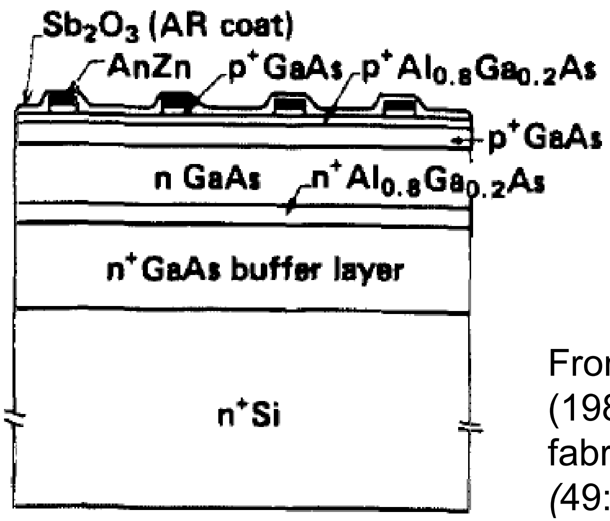


FIG. 1. Solar cell structure.

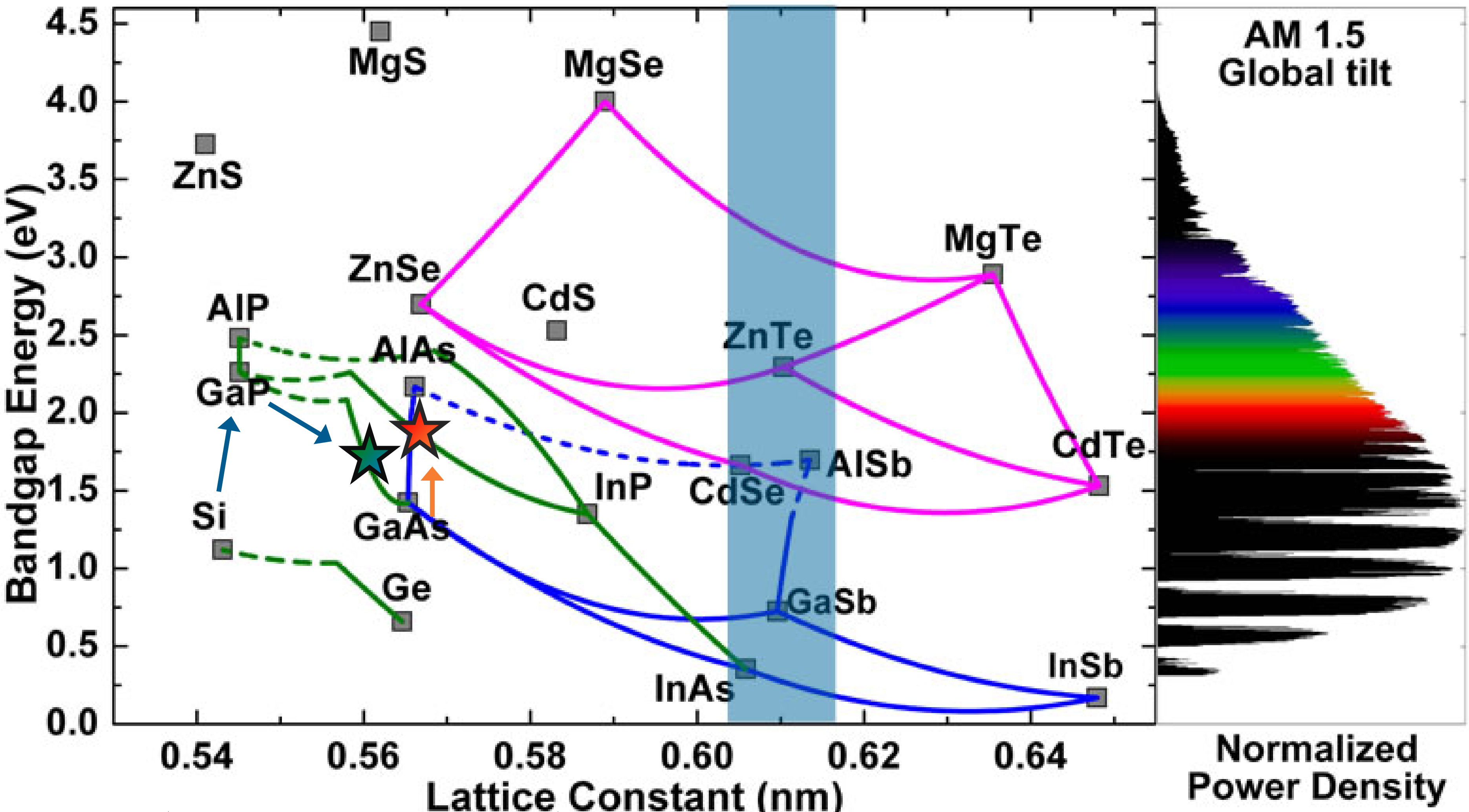
From Itoh, Y.; Nishioka, T.; Yamamoto, A.; Yamaguchi, M. (1986). "14.5% conversion efficiency GaAs solar cell fabricated on Si substrates." *Applied Physics Letters* (49:1614); doi 10.1063/1.97245.

Page: 34

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:52 PM

Please see the given reference for an early account of the defects arising from hetero-epitaxial growth of III-Vs.

What Are the Desirable Properties for a Dual-Junction Solar Cell?



$GaAs_{0.75}P_{0.25}$ $In_{0.5}Ga_{0.5}P$

Please see the annotated notes below this slide for more details.

Page: 35

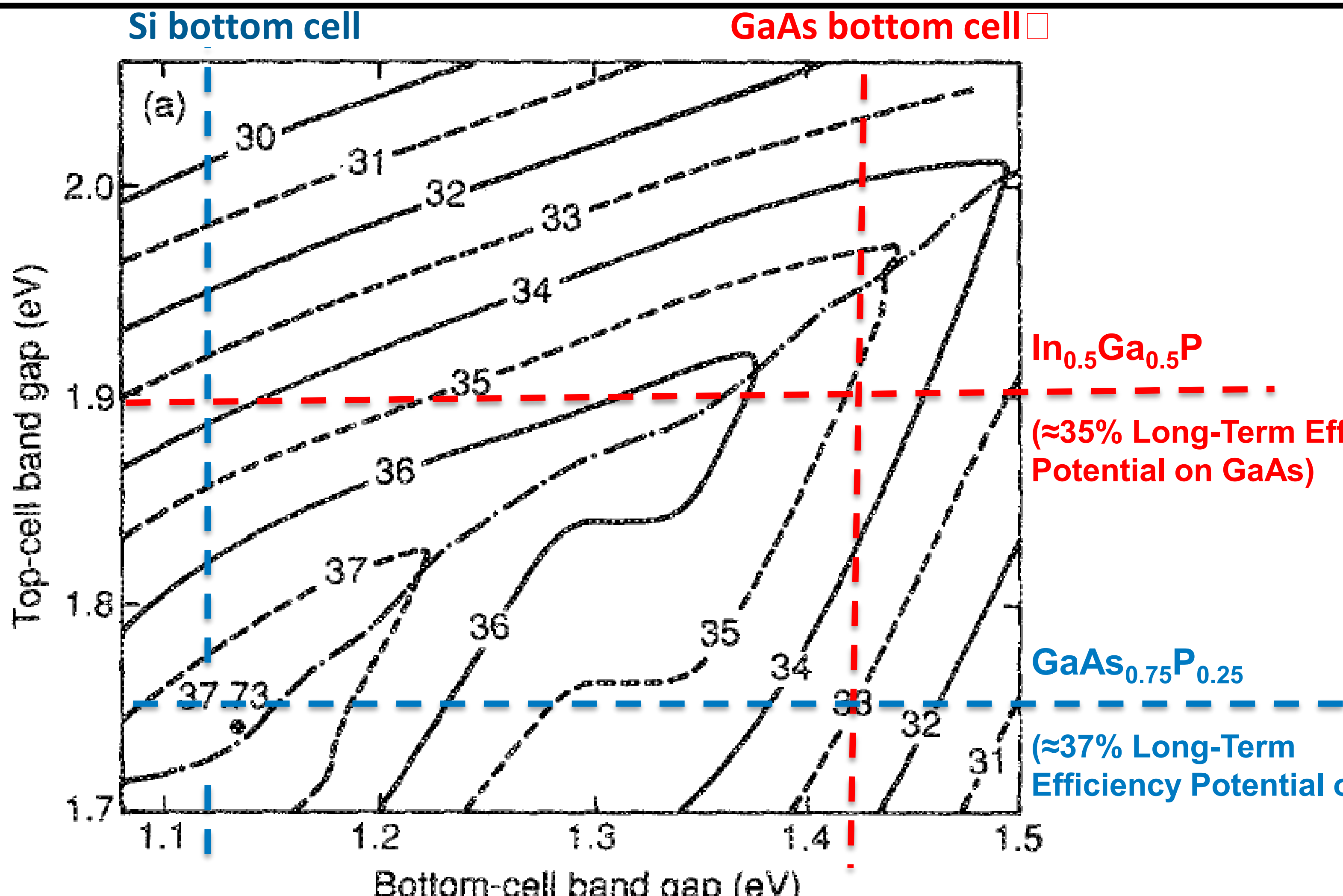
Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:52 PM

This slide ties together slides 32, 33 and 34. The goal is to optimize the top and bottom cell bandgaps with respect to cell efficiencies (slides 32 and 33), while also trying to match the lattice constant of the top and bottom cells in order to minimize defects (slide 34).

(1) For III-Vs on Si, the goal is to deposit a top cell with a bandgap of around 1.75 eV that is closely matched to the lattice constant of Si. An example material might be $GaAs_{0.75}P_{0.25}$.

(2) For an all III-V's device with a GaAs bottom cell, the goal is to deposit a top cell with a bandgap of around 1.9 eV that is closely matched to the lattice constant of GaAs. An example material might be $In_{0.5}Ga_{0.5}P$.

What Are the Desirable Properties for a Dual-Junction Solar Cell?



Isoefficiency plots for two-junction, series connected tandem structures under AM 1.5G one-sun illumination. In this analysis, reasonable values for J_o, μ, τ, etc. are incorporated into the efficiency projections (not just Shockley-Quiesser).

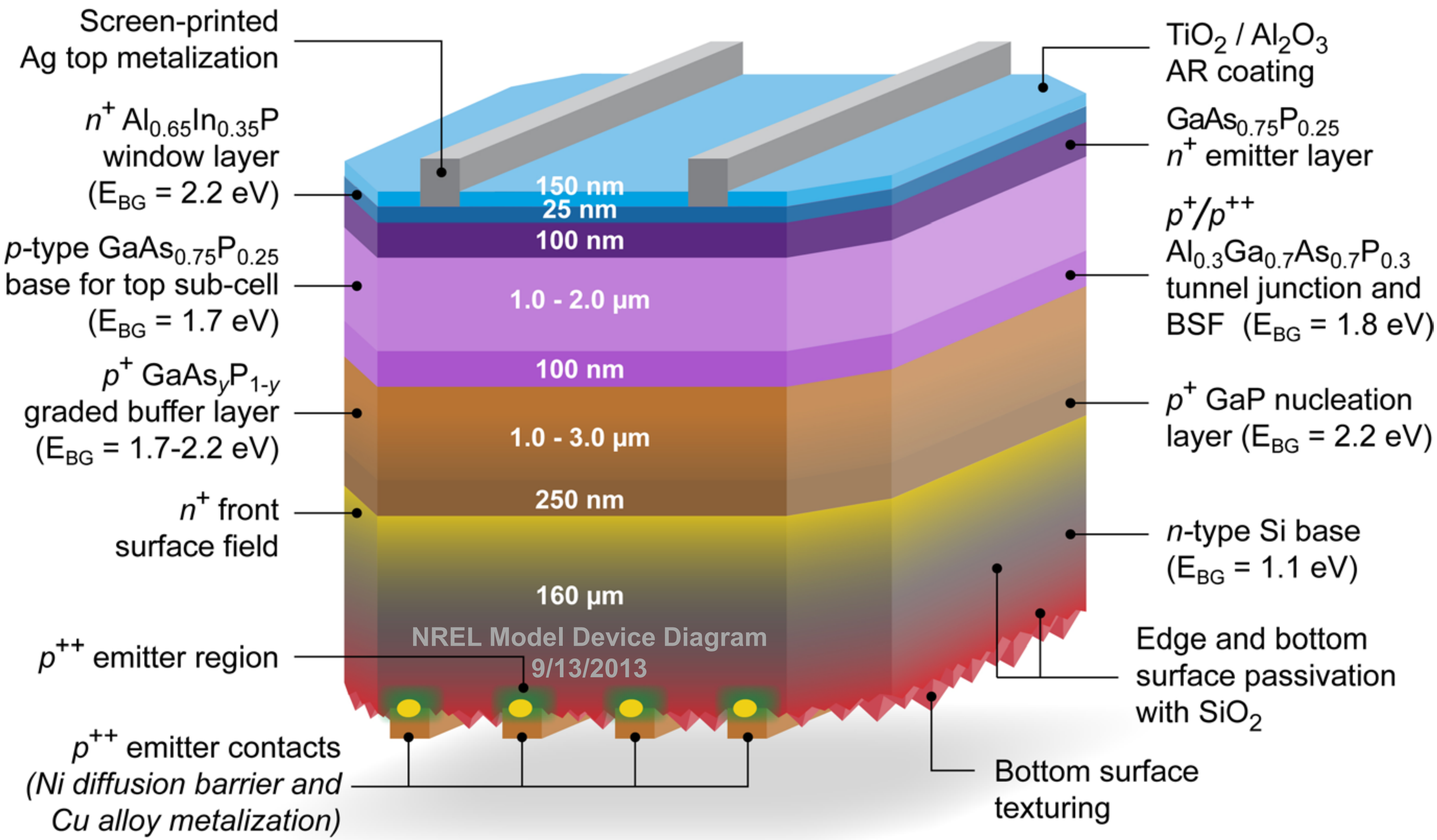
From "Modeling of two-junction, series-connected tandem solar cells using topcell thickness as an adjustable parameter" Sarah Kurtz, P Faine, and Jerry Olson *Journal of Applied Physics* **68** 1890 (1990); doi:10.1063/1.347177.

Page: 36

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:53 PM

This is a reproduction of slide 33 but with the material sets identified on slide 35 included.

Representative III-V's on *Cz*-Si Solar Cell



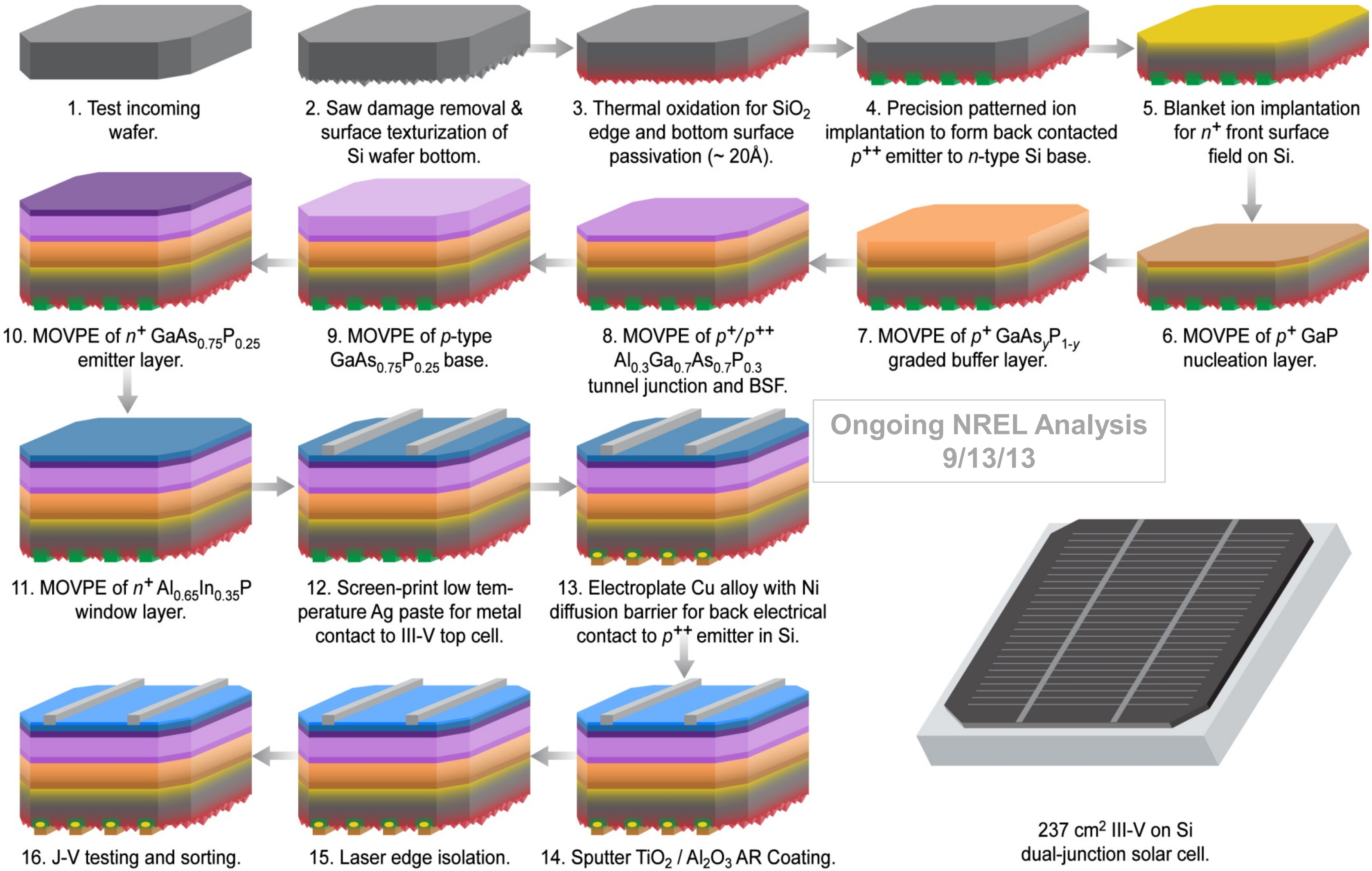
Device concept inspired by "Epitaxially-Grown Metamorphic GaAsP/Si Dual-Junction Solar Cells" from
T J Grassman, J A Carlin, C Ratcliff, D J Chmielewski, and S A Ringel *Proceedings of the IEEE PVSC* (2013).

Page: 37

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:53 PM

The model device that we use for our III-Vs on Si cost model was conceived in consultation with NREL researchers (including those listed on the Title slide), industry collaborators, and after an extensive literature survey. The given citation provides an experimental demonstration of the model device.

A Representative Process Flow for Making Such a Device



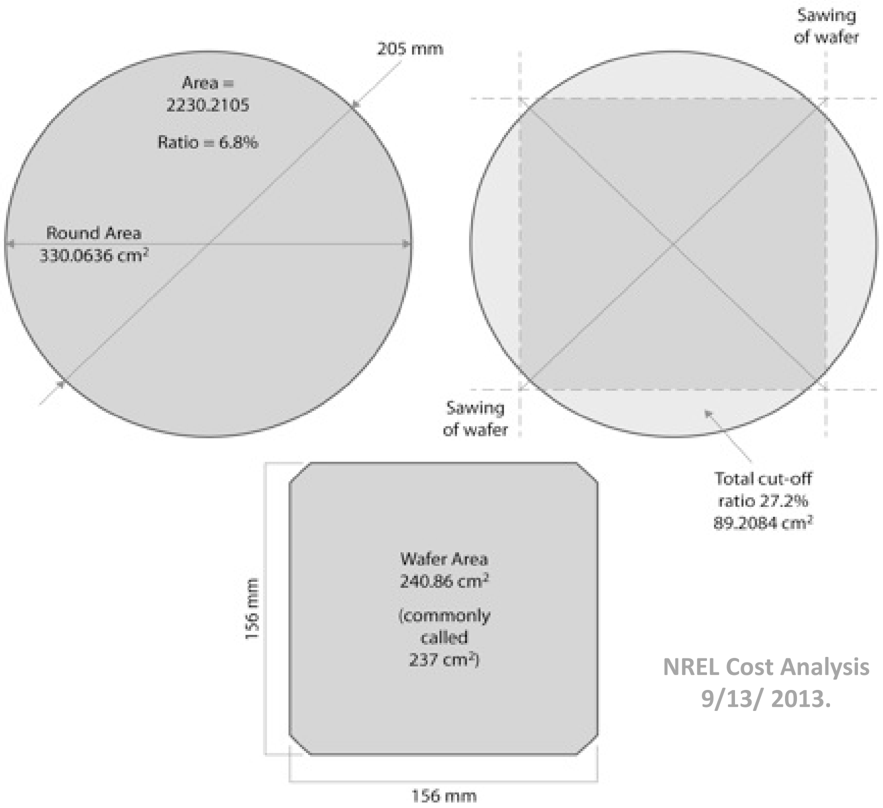
Page: 38

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:54 PM

The model process flow that we use for our cost models was conceived in consultation with NREL researchers (including those listed on the Title slide), industry collaborators, and after an extensive literature survey.

Step 1: Test Incoming Wafer

Wafer Geometry from c-Si



Estimated cost for a 160. μm thick, 237 cm² *Cz* Si wafer at $23/ kg polysilicon with diamond-wire sawing

= $43/ m² = $1.0/ wafer

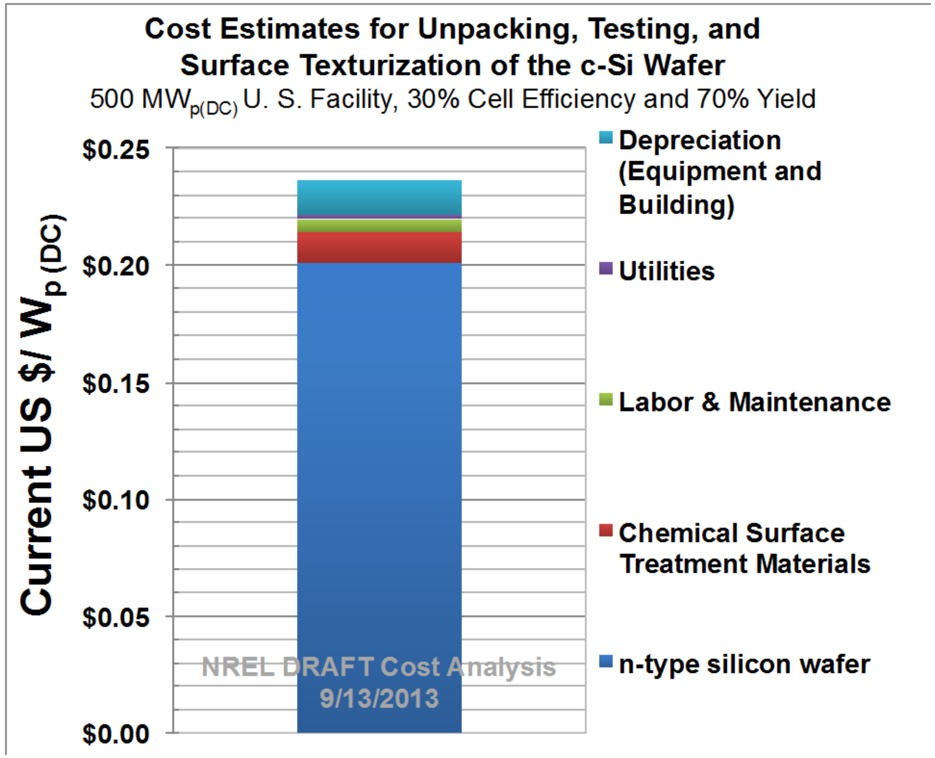
= $0.14/ W @ η = 30% with 100% yield

= $0.20/ W @ η = 30% with 70% yield.

Estimated cost for an 80. μm thick, 155 cm² *Cz* Si wafer at $23/ kg polysilicon with diamond-wire sawing and kerf recycling

= $22/ m² = $0.34/ wafer

= $0.073/ W @ η = 30% with 100% yield.



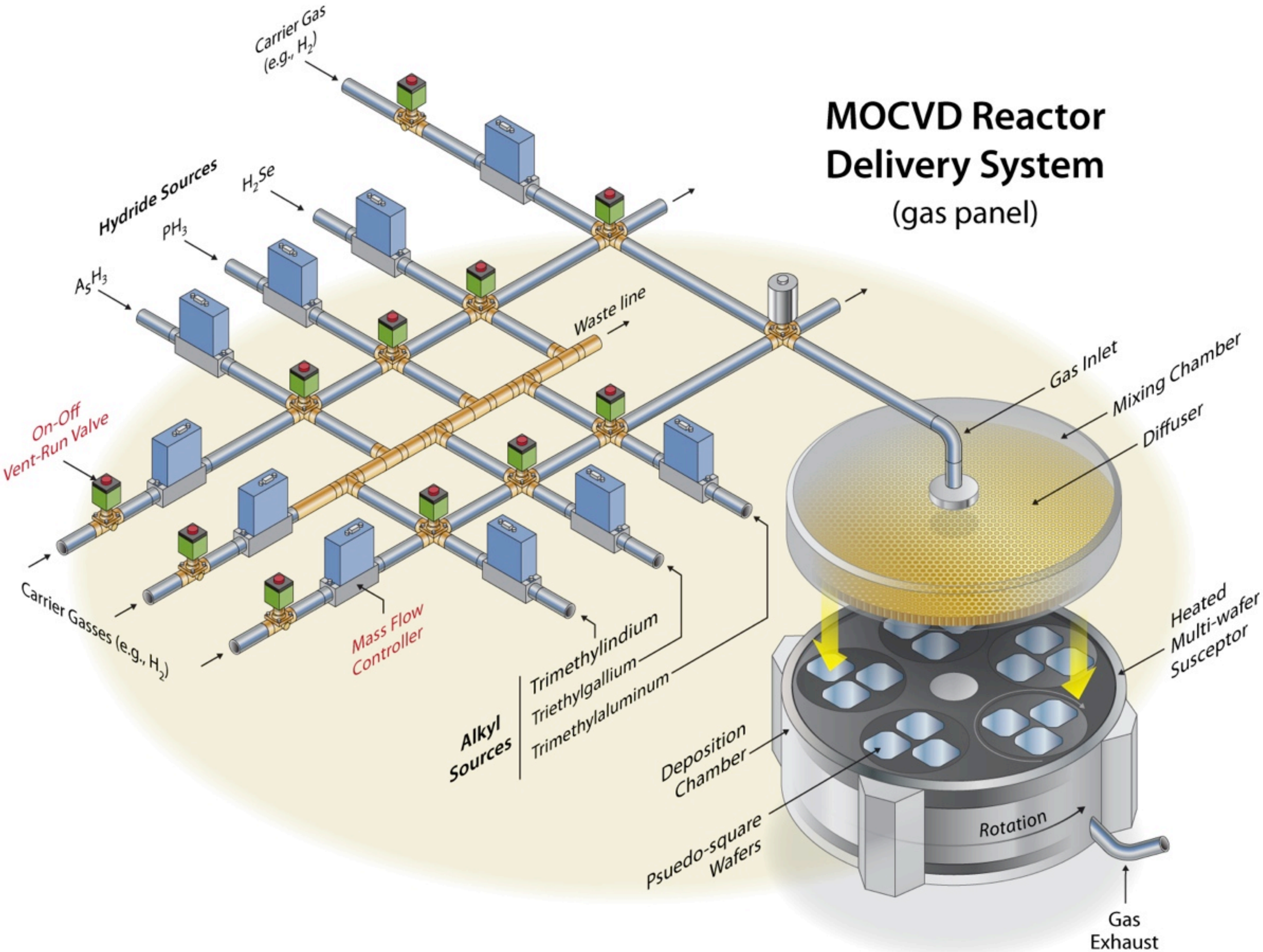
For a description of c-Si wafer prices, please see:
"A Wafer-Based Monocrystalline Silicon Photovoltaics Roadmap: Utilizing Known Technology Improvement Opportunities for Further Reductions in Manufacturing Costs." (2013). *Solar Energy Materials and Solar Cells* 114; pp. 110–135.

Page: 39

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:54 PM

Please see the given citation for a description of c-Si wafering. The wafer cost allocation is calculated in a manner similar to slide 8.

The Model MOVPE Reactor



Today's commercial reactors can accommodate 8 x 6" substrates or 15 x 4" substrates.

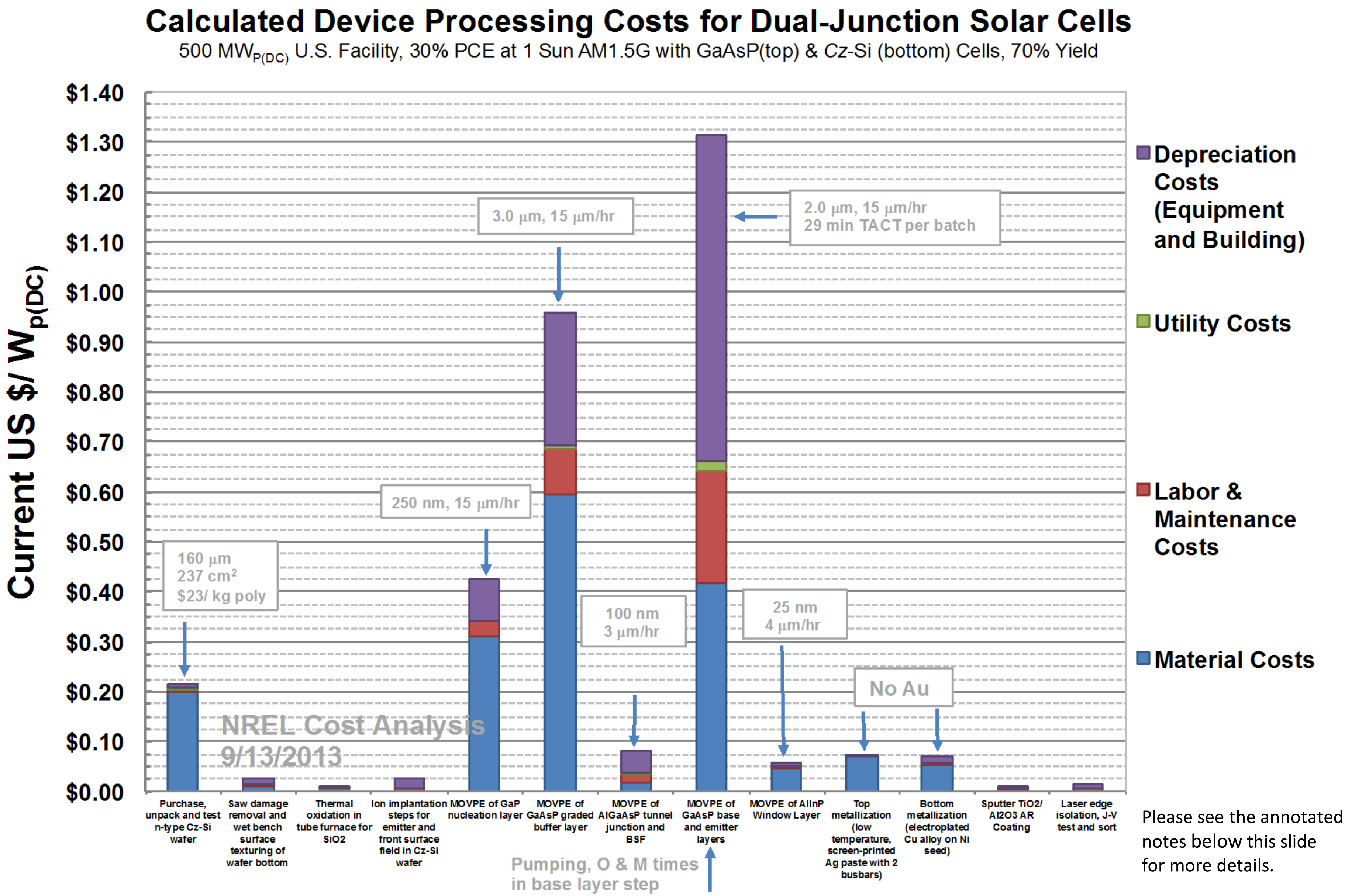
Page: 40

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:54 PM

1. This graphic represents our paradigm of a model solid film MOVPE reactor. The element III sources (Trimethylindium, or TMI, Trimethylgallium, or TMG, and Trimethylaluminum, or TMA), the element V sources (AsH3, PH3 and H2Se), and the H2 carrier gas feed into the reactor through mass flow controllers. There are also vent lines and valves to control the flow of precursors over the heated multi-wafer susceptor.
2. This reactor design leads to material utilizations that are lower than 100%. Efficient utilization of the precursors with today's MOVPE reactor designs might lead to around 30% atom-for-atom utilizations of the III sources, and around 20% atom-for-atom utilizations of the V sources. The unused precursors can be lost within the reactor, within the plumbing system itself, or they are vented through the waste line.

Cost Summary, by Step, for the Reference Case.

(Precursor utilizations of 30% for the III- source and 20% for the V- source)



Please see the annotated notes below this slide for more details.

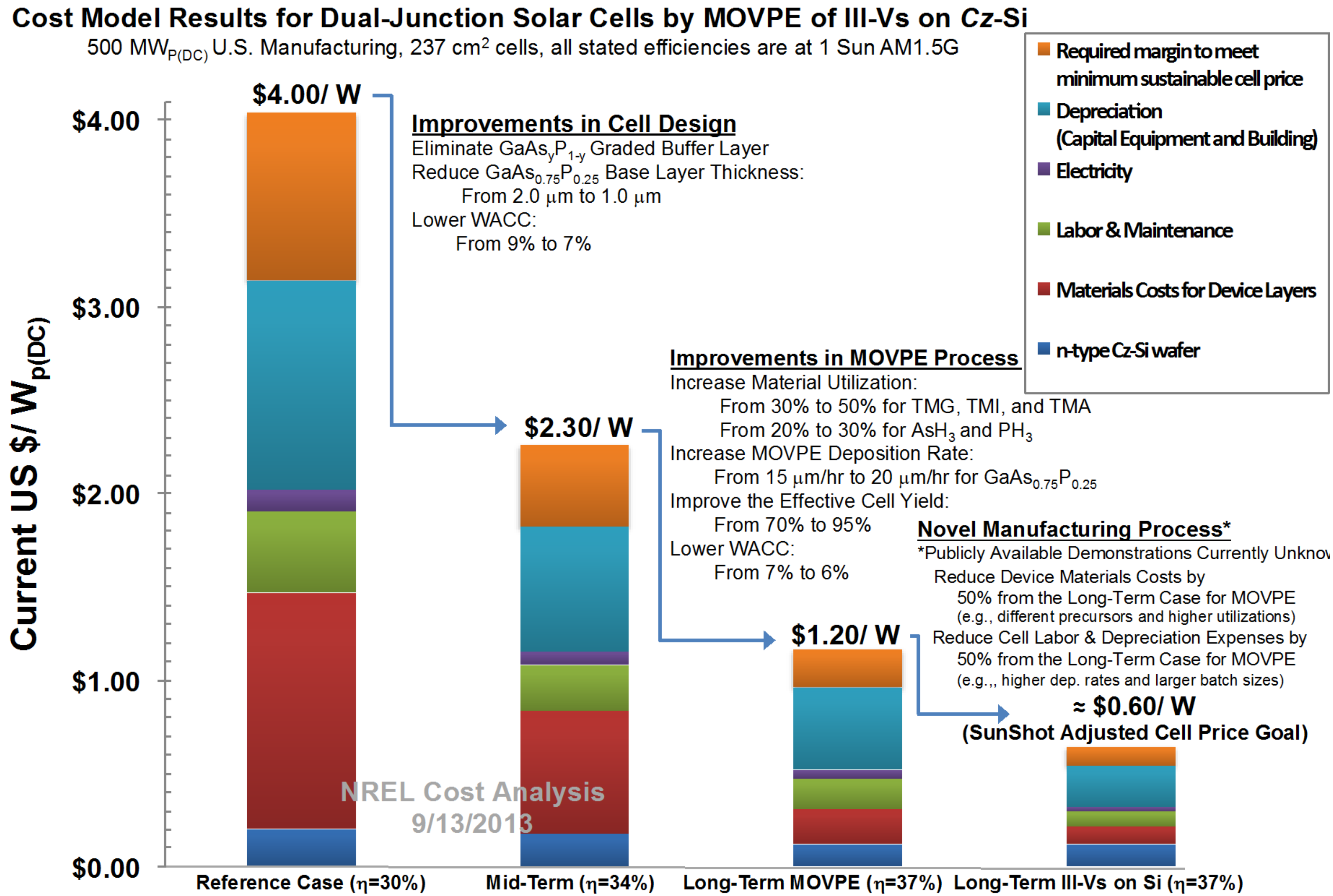
Page: 41

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:54 PM

This slide shows the costs for each step in the 'Reference Case' scenario of GaAsP on Cz-Si dual-junction PV cells. Key input parameters for each step are indicated on the figure, and can be compared to analogous layers represented on slides 12 – 23 (do note the differences in layer thicknesses and cell efficiency, which affect the cost calculations at each step).

For steps 6 -- 11 of the model III-Vs on Si process flow (slide 38), the times for MOVPE reactor chamber atmosphere preparation, temperature ramp up, temperature ramp down, and maintenance are all included in the GaAs base layer step only. Please see slide 16 for the specific times assumed. Of course, the total calculated depreciation expense for the GaAs base layer step also depends upon the deposition rate and thickness. The total average cycle time (TACT) is, therefore, highest in that step and is inclusive of more factors than what is included in steps 6 -- 8, 10 and 11 of the model process flow.

Technology Roadmap Simulations for Dual-Junction $GaAs_{0.75}P_{0.25}$ on *Cz*-Si Cells

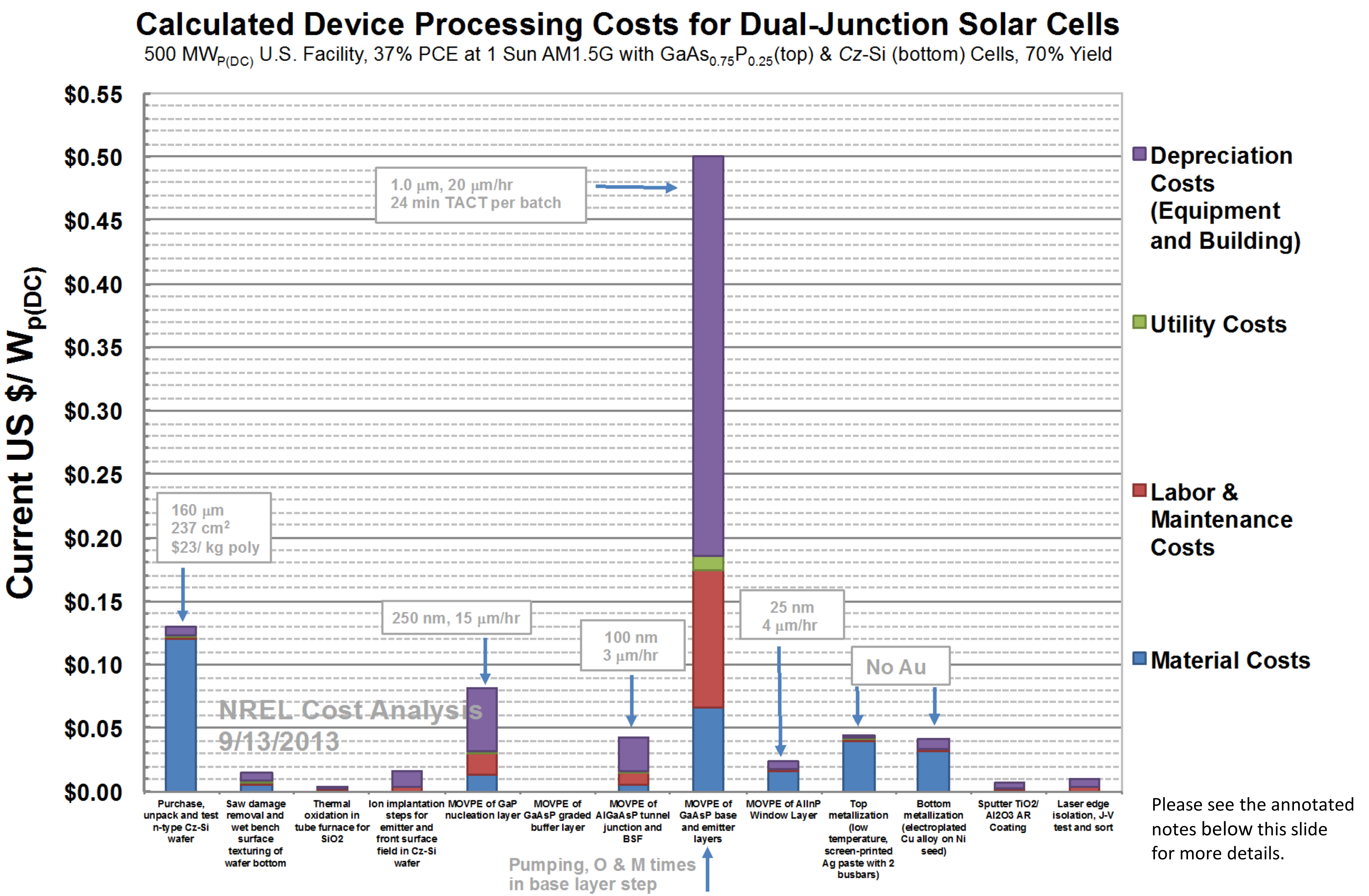


Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:55 PM

This slide again shows the sum of costs for the 'Reference Case' scenario of GaAsP on Cz-Si, and also highlights select technology pathways to lower manufacturing costs from that scenario. In the Mid-Term and Long-Term cases, we highlight what are currently believed to be practically achievable targets—based upon numerous conversations with NREL researchers and industry collaborators—for solid III-V films deposited by MOVPE.

Cost Summary, by Step, in the Long-Term Case

(Precursor utilizations of 80% for the III- source and 30% for the V- source, 80 μm *Cz* wafer)



Please see the annotated notes below this slide for more details.

Page: 44

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:55 PM

This slide shows the costs for each step of the process flow shown on slide 38 under the ‘Long-Term’ MOVPE technology scenario.

For steps 6 -- 11 of the model III-Vs on Si process flow (slide 38), the times for MOVPE reactor chamber atmosphere preparation, temperature ramp up, temperature ramp down, and maintenance are all included in the GaAs base layer step only. Please see slide 16 for the specific times assumed. Of course, the total calculated depreciation expense for the GaAs base layer step also depends upon the deposition rate and thickness. The total average cycle time (TACT) is, therefore, highest in that step and is inclusive of more factors than what is included in steps 6 -- 8, 10 and 11 of the model process flow.

Final Considerations for III-V Cells Directly Serving as Drop-in Replacements for c-Si Cells (Without Optical Concentration)

Balance of Materials Costs for Dual-Junction GaAsP on Cz-Si Cells Serving as Drop-In Replacements into 2.26 m^2 c-Si designed modules (η=37%)	
Material	**Cost Assumptions**
Long-term cell prices	≈$0.60/$W_p$
Stringing and tabbing ribbons, metal solder and bus bars	$2.5/module
J-box containing the bypass diodes	$4.5/module
J-box sealant, bonding tape or edge seal, printed module sticker label and bus bar covers	$1.5/module
Aluminum frame	$20/module
EVA (2 sheets needed)	$3.50/$m^2$ for each sheet
Bottom-side film or glass	$6 /$m^2$
Premium Front Glass: 4.0 mm, low [Fe], tempered, with AR coating	$16/$m^2$
Total estimated module materials costs	**≈ $0.70/$W_{p(DC)}$**

Page: 45

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:56 PM

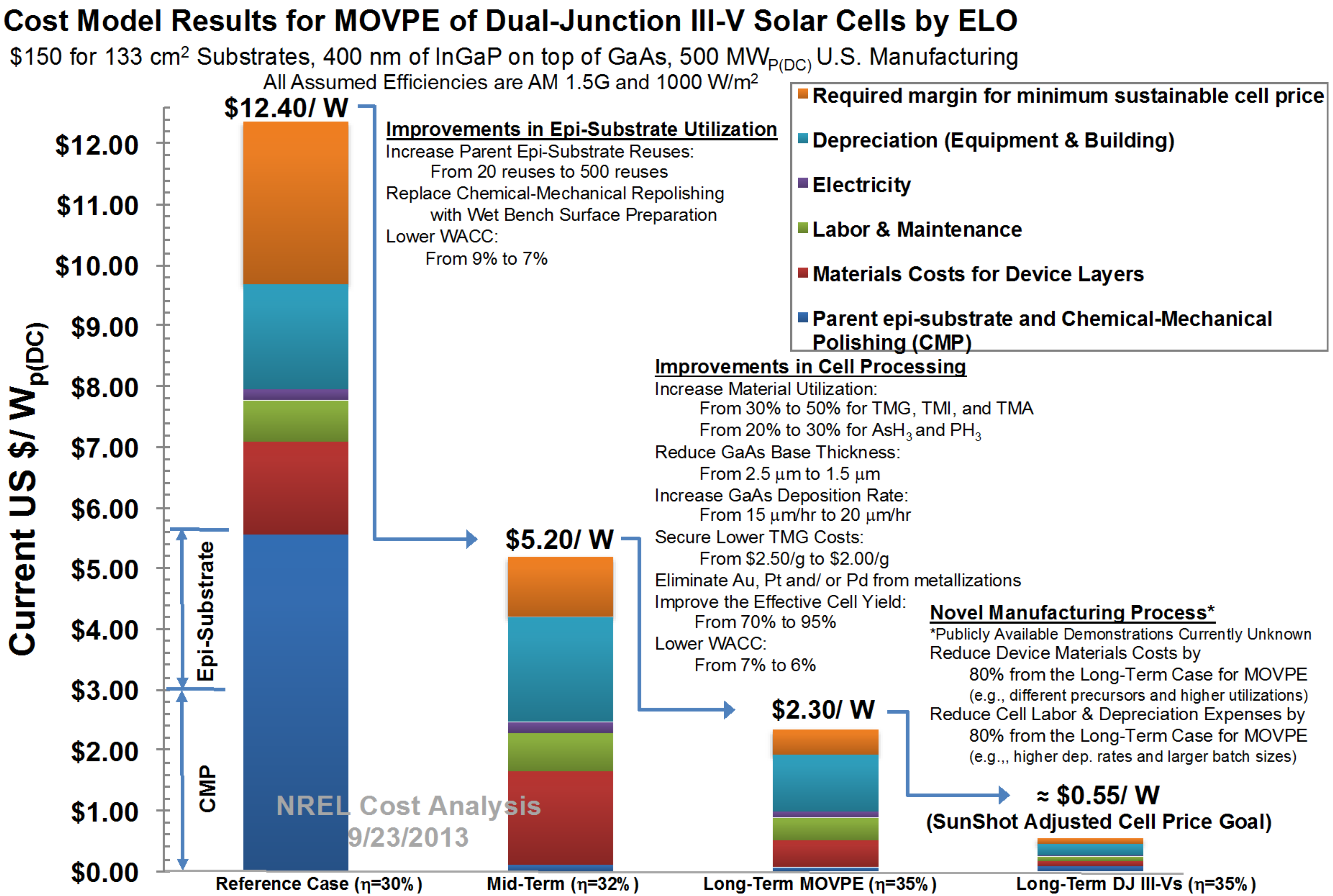
This slide represents typical balance-of-module materials costs if such cells were to serve as drop-in replacements into existing c-Si manufacturing. It does not include the depreciation, labor, etc. expenses for module assembly. For those costs, the reader is referred to: A Goodrich, P Hacke, Q Wang, B Sopori, R Margolis, T L James and M Woodhouse "A Wafer-Based Monocrystalline Silicon Photovoltaics Roadmap: Utilizing Known Technology Improvement Opportunities for Further Reductions in Manufacturing Costs." (2013). Solar Energy Materials and Solar Cells 114; pp. 110–135.

While being a simplification from a levelized-cost-of-energy (LCOE) metric, the the U.S. Department of Energy's 'SunShot' goal is broadly defined as $1/W installed utility-scale PV system prices or $1.5/W installed residential-scale PV system prices. As a first-order approximation, using incumbent technologies already in mass production the model PV systems might then be comprised of circa 20% efficient modules having a price of $0.50/W—thus leaving an allowed budget for balance-of-systems of around $0.50/W for utility-scale systems or around $1.0/W for residential systems.

If higher than 20% efficiency modules were to be deployed, however, then lower balance-of-systems costs can be expected if the mounting configuration, labor requirements, land area, etc., are the same. For the case of 37% modules versus 20% modules, under this assumption of constancy we estimate a balance-of-systems price savings of around $0.20/W for the higher efficiency modules--thus leading to a module price that could hypothetically be $0.20/W higher and still reaching the $1/W system price goal.* Given the typical balance-of-module materials shown above, the 'SunShot adjusted cell price' goal shown in slide 43 is calculated to reach this hypothetical $0.70/W module price target.

*For a rationale of these cost-efficiency adjustments, please see: A Goodrich, T James, and M Woodhouse, 'Residential, Commercial, and Utility-Scale Photovoltaic System Prices in the United States: Current Drivers and Cost Reduction Opportunities' (2012). Available online at: http://www.nrel.gov/docs/fy12osti/53347.pdf.

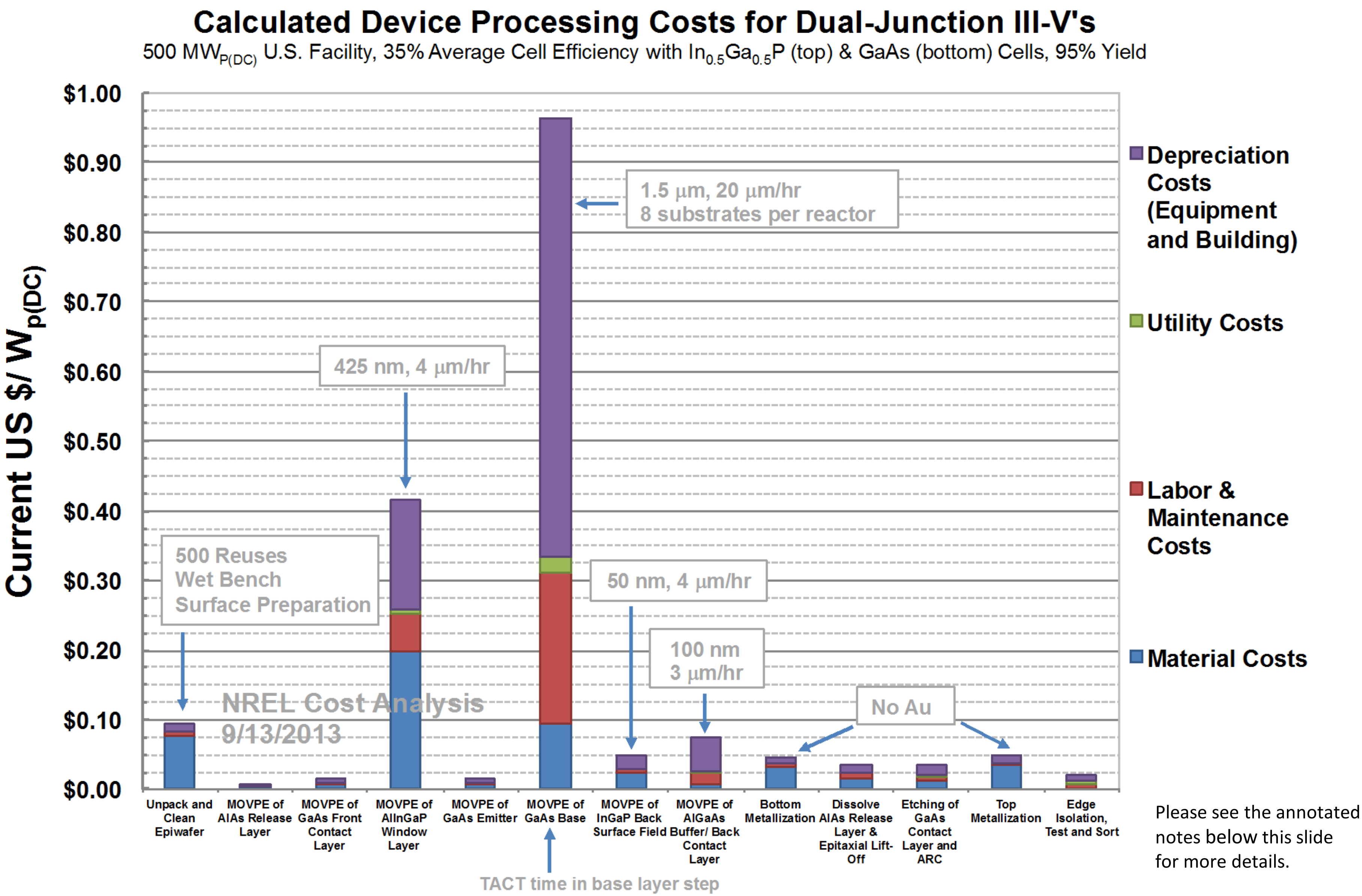
Technology Roadmap Simulations for Dual-Junction III-Vs ($In_{0.5}Ga_{0.5}P$ on GaAs)



Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:56 PM

This slide shows the sum of costs for the 'Reference Case' scenario of InGaP on GaAs and also highlights select technology pathways to lower manufacturing costs from that scenario. In the Mid-Term and Long-Term cases, we highlight what are currently believed to be practically achievable targets—based upon numerous conversations with NREL researchers and industry collaborators—for solid III-V films deposited by MOVPE.

Cost Summary, by Step, in the Long-Term Dual-Junction MOVPE Case



Please see the annotated notes below this slide for more details.

Page: 47

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:56 PM

This slide shows the costs for each step of the process flow shown on slide 7 under the 'Long-Term' MOVPE technology scenario. The difference between this slide and slide 29 is that we assume a 425 nm thick InGaP top cell.

For steps 2-8 of the model process flow (slide 7), the times for MOVPE reactor chamber atmosphere preparation, temperature ramp up, temperature ramp down, and maintenance are all included in the GaAs base layer step only. Please see slide 16 for the specific times assumed. Of course, the total calculated depreciation expense for the GaAs base layer step also depends upon the deposition rate and thickness. The total average cycle time (TACT) is, therefore, highest in that step and is inclusive of more factors than what is included in steps 2 -- 5, 7 and 8 of the model process flow.

Final Considerations for III-V Cells Directly Serving as Drop-in Replacements for c-Si Cells (Without Optical Concentration)

Balance of Materials Costs for Dual-Junction InGaP on GaAs Cells Serving as Drop-In Replacements into 2.26 m^2 c-Si designed modules (η=35%)	
Material	**Cost Assumptions**
Long-term cell prices	$\approx\$0.55/W_p$
Stringing and tabbing ribbons, metal solder and bus bars	\$2.5/module
J-box containing the bypass diodes	\$4.5/module
J-box sealant, bonding tape or edge seal, printed module sticker label and bus bar covers	\$1.5/module
Aluminum frame	\$20/module
EVA (2 sheets needed)	$\$3.50/m^2$ for each sheet
Bottom-side film or glass	$\$6\ /m^2$
Premium Front Glass: 4.0 mm, low [Fe], tempered, with AR coating	$\$16/m^2$
Total estimated module materials costs	$\approx \mathbf{\$0.65/W_{p(DC)}}$

Page: 48

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:57 PM

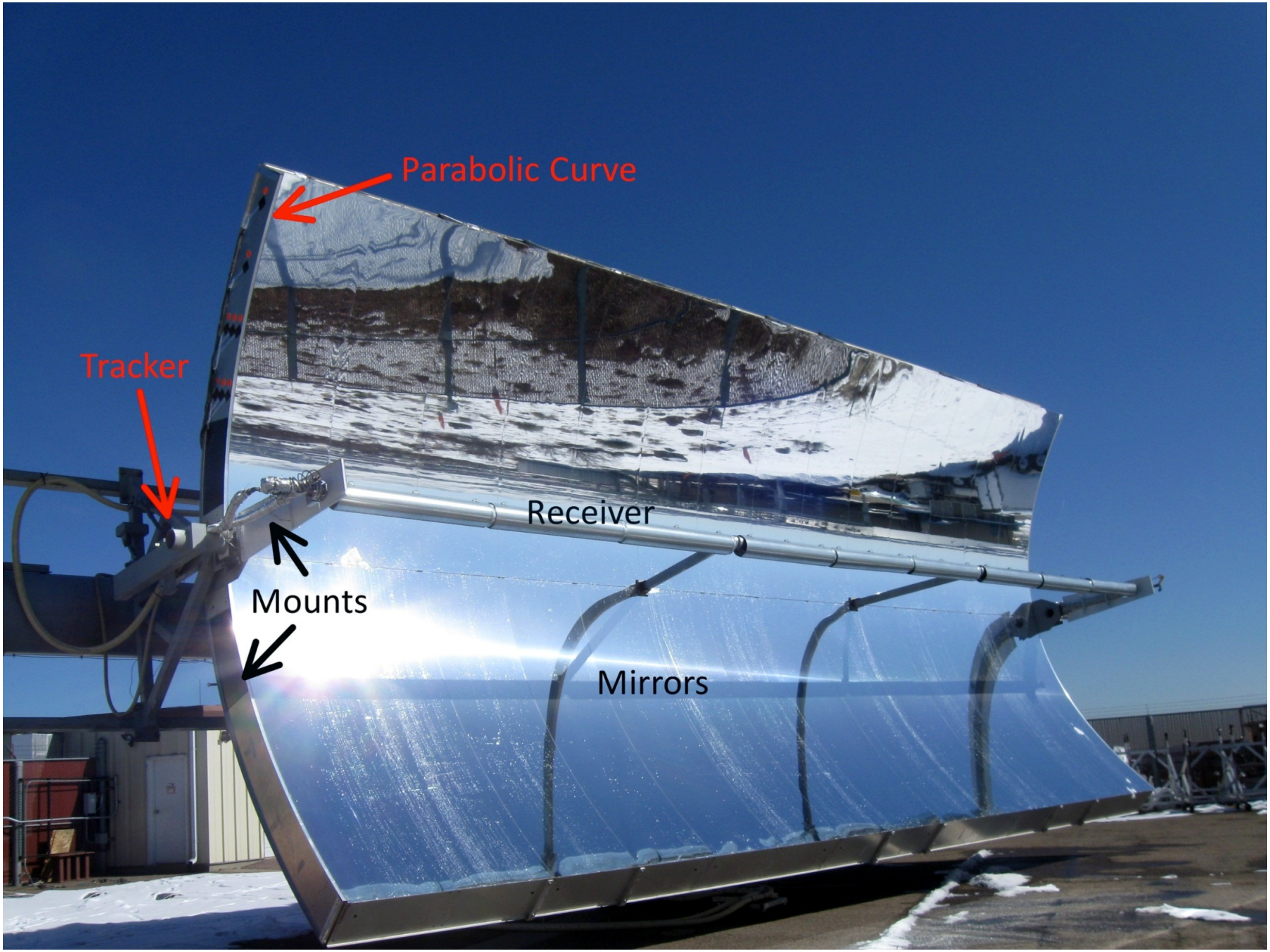
This slide represents typical balance-of-module materials costs if such cells were to serve as drop-in replacements into existing c-Si manufacturing. It does not include the depreciation, labor, etc. expenses for module assembly. For those costs, the reader is referred to: A Goodrich, P Hacke, Q Wang, B Sopori, R Margolis, T L James and M Woodhouse "A Wafer-Based Monocrystalline Silicon Photovoltaics Roadmap: Utilizing Known Technology Improvement Opportunities for Further Reductions in Manufacturing Costs." (2013). Solar Energy Materials and Solar Cells 114; pp. 110–135.

While being a simplification from a levelized-cost-of-energy (LCOE) metric, the the U.S. Department of Energy's 'SunShot' goal is broadly defined as $1/W installed utility-scale PV system prices or $1.5/W installed residential-scale PV system prices. As a first-order approximation, using incumbent technologies already in mass production the model PV systems might then be comprised of circa 20% efficient modules having a price of $0.50/W—thus leaving an allowed budget for balance-of-systems of around $0.50/W for utility-scale systems or around $1.0/W for residential systems.

If higher than 20% efficiency modules were to be deployed, however, then lower balance-of-systems costs can be expected if the mounting configuration, labor requirements, land area, etc., are the same. For the case of 35% modules versus 20% modules, under this assumption of constancy we calculate a balance-of-systems price savings of around $0.15/W for the higher efficiency modules--thus leading to a module price that could hypothetically be $0.15/W higher and still reaching the $1/W system price goal.* Given the typical balance-of-module materials shown above, the 'SunShot adjusted cell price' goal shown in slide 46 is calculated to reach this hypothetical $0.65/W module price target.

*For a rationale of these cost-efficiency adjustments, please see: A Goodrich, T James, and M Woodhouse, 'Residential, Commercial, and Utility-Scale Photovoltaic System Prices in the United States: Current Drivers and Cost Reduction Opportunities' (2012). Available online at: http://www.nrel.gov/docs/fy12osti/53347.pdf.

The Possibility of Lower Module Costs By Concentrating Optics Needs to be Considered: The Case for Low-Concentration PV (LCPV) with Linear Reflective Troughs



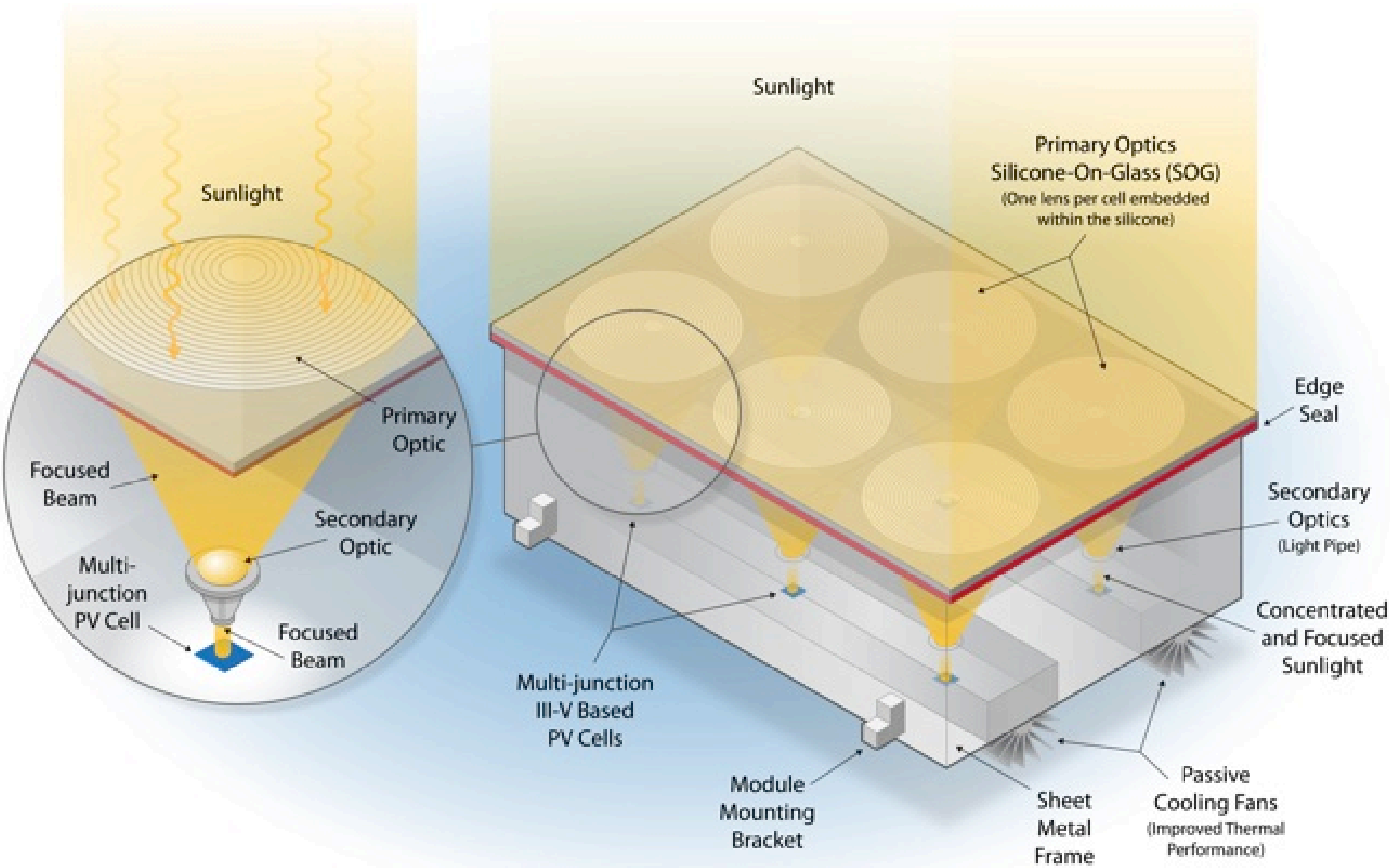
NREL Stock Photo (available online at: http://images.nrel.gov/albums.php?albumId=207403) modified by Greg Smestad

Page: 49

Author: Presenter Subject: Presentation Notes Date: 3/6/2014 3:28:57 PM

This photo is from the NREL stock photo library: http://images.nrel.gov/albums.php?albumId=207403.

The Possibility of Lower Module Costs By Employing Concentrating Optics Needs to be Considered: The Case for High-Concentration PV (HCPV) With the Fresnel Lens Box



Source of Figure: NREL

Page: 50

Author: Presenter   Subject: Presentation Notes   Date: 3/6/2014 3:28:57 PM

Stay tuned for our upcoming HCPV costs analysis!