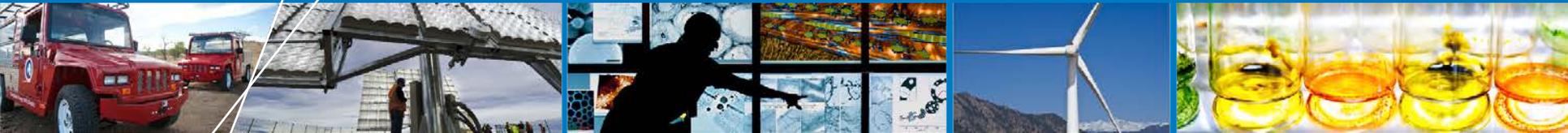


# Results of IEC 62804 *draft* round robin testing



**Peter Hacke and Kent Terwilliger**  
NREL, USA

**Simon Koch, Thomas Weber, and Juliane Berghold**  
PI-Berlin, DE

**Stephan Hoffmann, and Michael Koehl**  
Fraunhofer ISE, DE

**Sascha Dietrich and Matthias Ebert**  
Fraunhofer CSP, DE

**Gerhard Mathiak**  
TÜV Rheinland, DE

NREL/PR-5200-60493  
September 2013

# Abstract

---

Three crystalline silicon module designs were distributed in five replicas each to five laboratories for testing according to the IEC 62804 (Committee Draft) system voltage durability qualification test for crystalline silicon photovoltaic (PV) modules. The stress tests were performed in environmental chambers at 60°C, 85% relative humidity, 96 h, and with module nameplate system voltage applied to the cells (two modules in each polarity and one control). Results from the module designs tested indicate the test protocol is able to discern susceptibility to potential-induced degradation according to the pass/fail criteria with acceptable consistency from lab to lab. In the analysis of variance of the results, 6% could be attributed to the laboratory influence, 34%, the module design, and 60%, variability in test results within a given design.

# Introduction

- **Testing was performed according to IEC 62804 draft “SYSTEM VOLTAGE DURABILITY QUALIFICATION TEST FOR CRYSTALLINE SILICON MODULES.” The motivation was to:**
  - See if the specified sample size (2 modules per polarity) is adequate considering variations that might exist in shipping modules
  - See if possible lab to lab variation in stress levels overly influences results
- **Modules were chosen to be near the pass/fail limit vis-à-vis the 60°C/85%RH/-1000 V 96h stress condition to attempt to get useful statistics (without ‘censoring’). Said another way, we *could* have chosen modules that do not degrade at all, and modules that degrade an extreme amount, and shown how well the test differentiates the two, but such results would be less useful.**

| Participants |                |
|--------------|----------------|
| Lab #        | Lab name       |
| 1            | NREL           |
| 2            | Fraunhofer ISE |
| 3            | TÜV Rheinland  |
| 4            | Fraunhofer CSP |
| 5            | PI Berlin      |

# Experiment

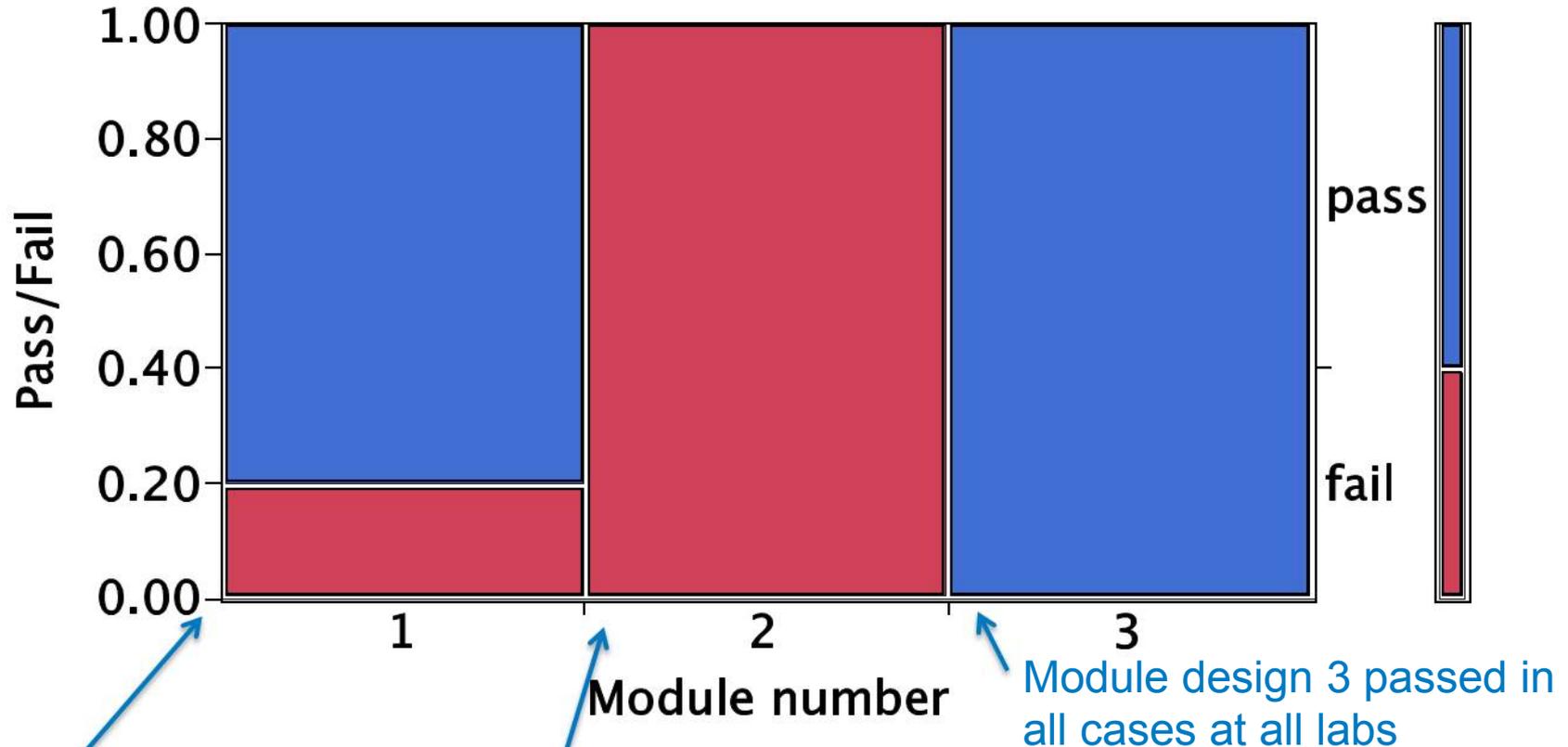
- **Highlights of round-robin test procedure based on IEC 62804 draft:**
  - Modules leads are shorted and connected to high voltage, module frames grounded (method per Hacke *et. al*, PVSC 37, Seattle, 2011)
  - Neither *in-situ* nor *ex-situ* I-V measurements are performed on the module over the course of the 96 h test
  - Leakage current from the active layer/cells to ground may optionally be measured during the testing (most labs did not report)
  - Open market modules with near-sequential serial numbers chosen (but not necessarily currently shipping), not specially designed modules
  - Electroluminescence measurements are carried out before and after the test
  - Modules tested in both polarities (2 each), although testing labs may instead choose to use the modules listed for test in the known stable polarity for outdoor tests instead
- **Stress conditions**
  - Chamber air temperature  $60\text{ }^{\circ}\text{C} \pm 2^{\circ}\text{C}$
  - Chamber relative humidity  $85\% \pm 5\% \text{ RH}$
  - Test duration 96 h
  - Voltage: module nameplate rated system voltage (1000 V), 2 for each polarity, 1 module supplied for control, voltage applied during ramps
  - Pass criterion: <5% power degradation (both modules of a tested polarity) and visual inspection pass

# Experiment

- **Modules with Al frames and polymeric backsheets were selected:**
- **Module 1**
  - 230 W class mc-Si module design (15.6 cm x 15.6 cm cell)
  - Susceptible to degradation with cell circuit in negative voltage bias
  - Manufactured from 2011 onward
  - Based on previously published reports of PID tests under different conditions, the module was expected to show a PID signal, but less than 5% degradation in negative bias is expected.
- **Module 2**
  - a 170 W class mc-Si module design (72 12.5 cm x 12.5 cm cells)
  - Susceptible to degradation with cell circuit in negative voltage bias
  - Manufactured in 2008 or 2009
  - Expected to show PID in negative based on data obtained at NREL under different conditions, but significant scatter in the data had been expected due to poorer process control and increased variability in the cells made during this period and as evidenced in prior EL imaging.
- **Module 3**
  - 235 W class c-Si module, 12.5 cm x 12.5 cm cells
  - Susceptible to degradation with cell circuit in positive voltage bias
  - Manufactured in 2012
  - Expected to show significantly less than 5% degradation based on NREL pre-tests

# Overview of pass/fail results of three different module designs tested at 5 labs – results of their susceptible polarity

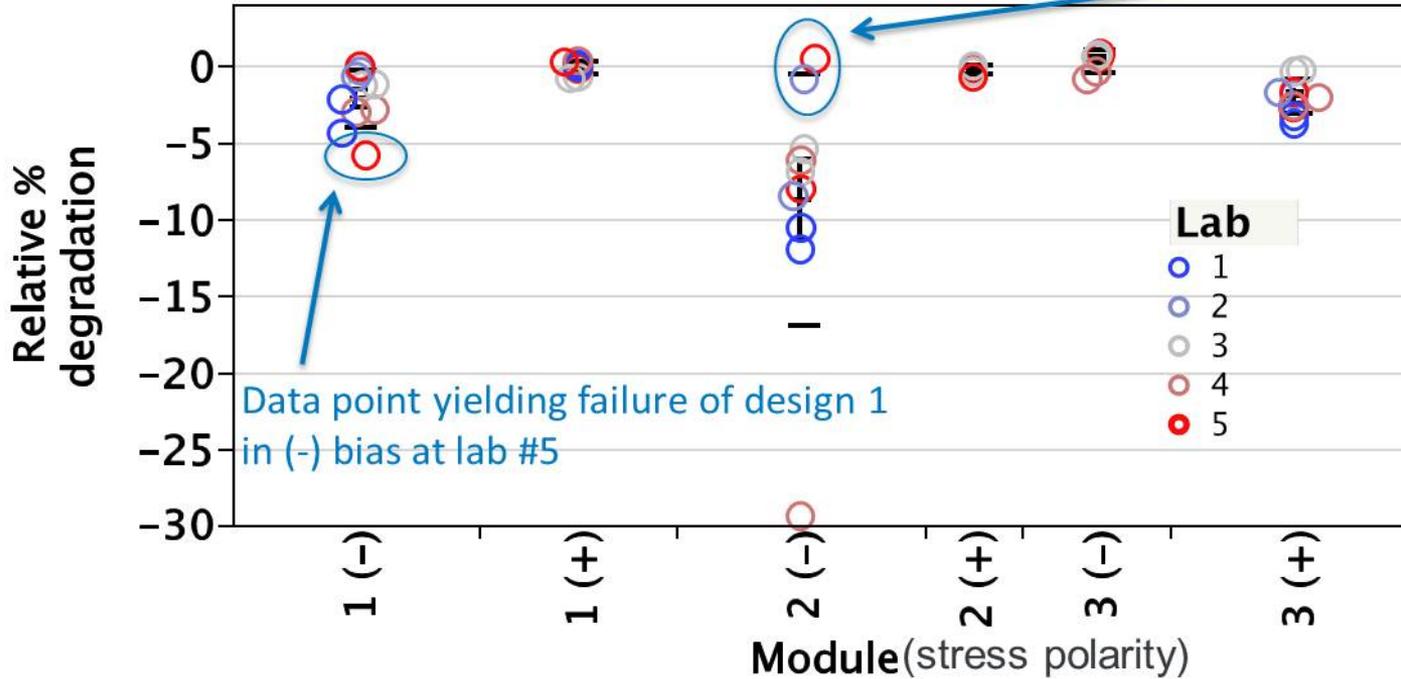
**Pass/fail condition:** If 1 or 2 modules tested in a polarity fail ( $P_{\max}$  drop > 5%), that design is considered failed in that polarity at the given test lab



Module design 1 failed in the (-) polarity test at one of the five labs when one of the two replicas tested there failed.

Module design 2 failed in the (-) polarity test at all five labs when at least one of the two modules tested failed at each lab

# Mean degradation and standard deviation of degradation in both polarities

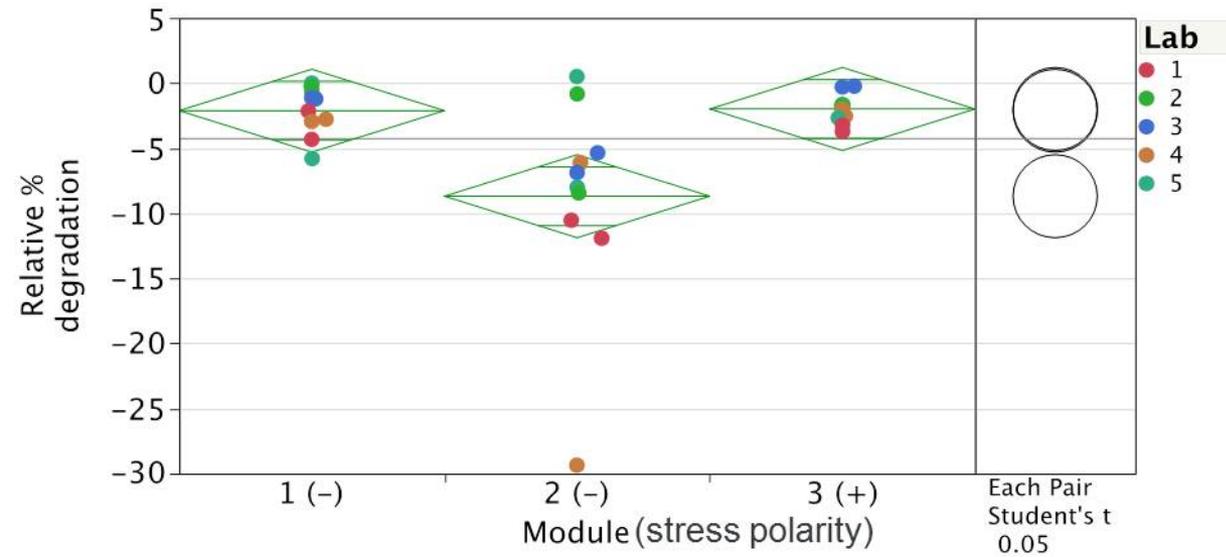


As anticipated, design 2 exhibited the greatest mean degradation and standard deviation in the susceptible polarity.

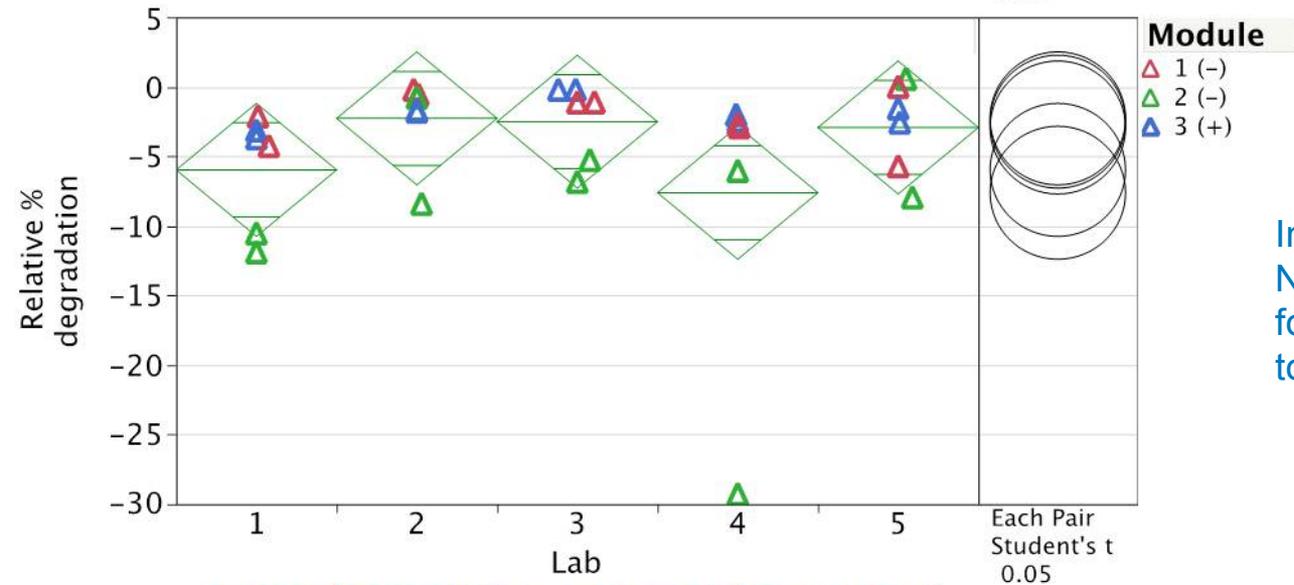
What is the probability of both those 2 modules that degraded less than 5% arriving at one lab, and thus passing the stress test in the (-) polarity at that one lab? ... There are 45 different combinations when the number of samples is 10 with 2 samples in each combination. The probability of those two ending up at one lab for a false pass is 1/45 (2.22%).

| Level | Number | Mean  | Std Dev |
|-------|--------|-------|---------|
| 1 (-) | 10     | -2.12 | 1.87    |
| 1 (+) | 8      | -0.10 | 0.43    |
| 2 (-) | 10     | -8.70 | 8.22    |
| 2 (+) | 4      | -0.29 | 0.32    |
| 3 (-) | 6      | 0.30  | 0.68    |
| 3 (+) | 10     | -1.99 | 1.13    |

# Relative percent degradation by module design and lab



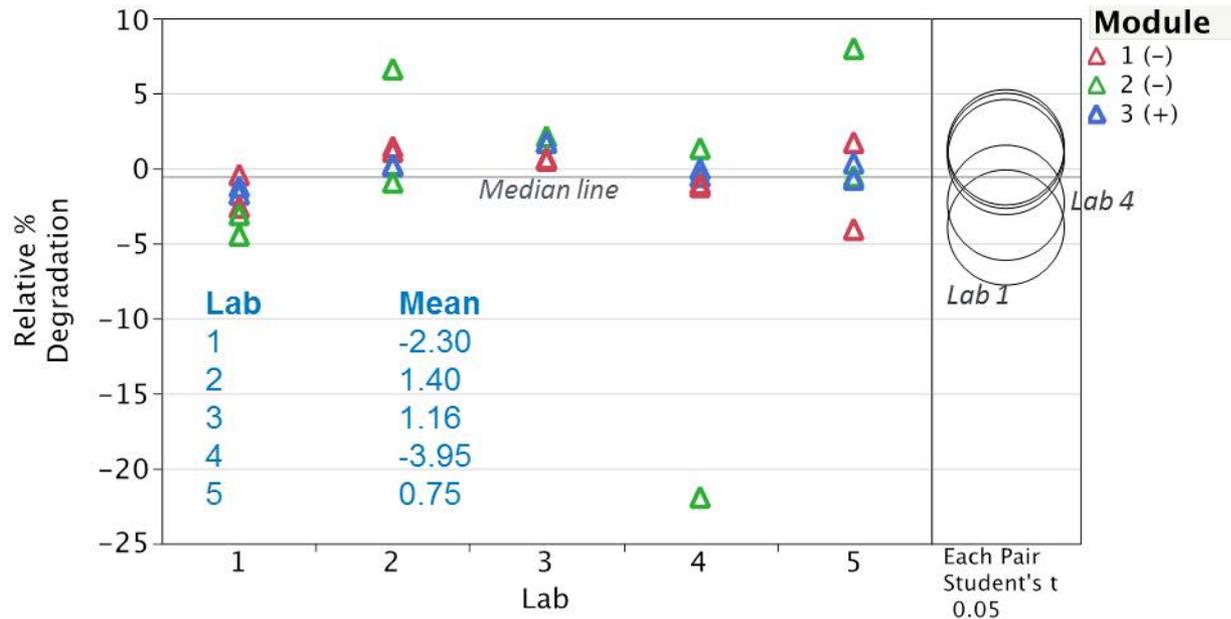
Influence of module design:  
A statistically significant difference in mean degradation of design 2, the failing module, can be seen



Influence of Lab:  
No statistically significant difference found; however, labs 1 & 4 appear to be more severe

Means diamonds for  $\alpha = .05$  confidence interval

# Examination of lab-to-lab variability

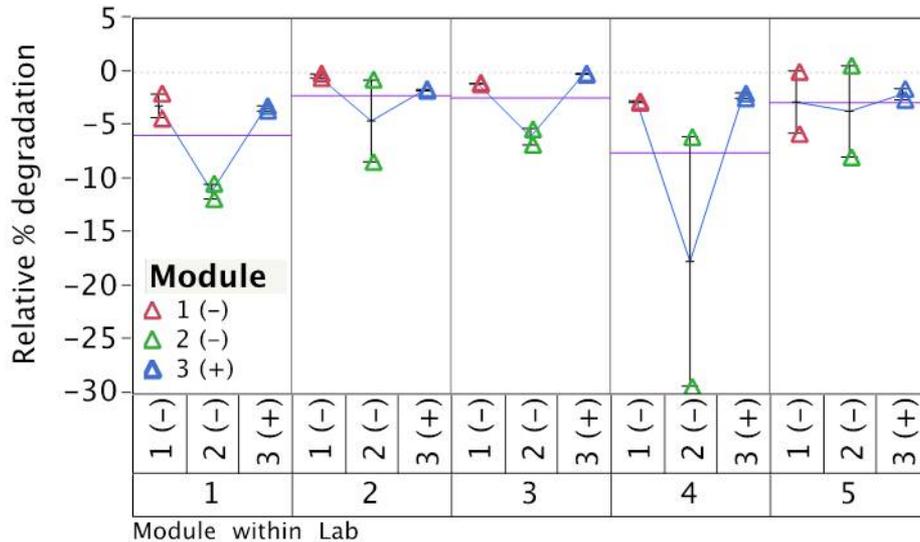


Subtracting median degradation for each module type in this analysis failed to show a statistical significance in difference between labs.

Degradation may be more pronounced in labs 1 and 4. More uniformity in the results from lab to lab may be obtained by:

- Tightening of the temperature and relative humidity tolerances
- Application of voltage bias stress after modules have reached equilibrium conditions in the environmental chamber

# What extent did the possible varying severity of the test labs influence outcomes?

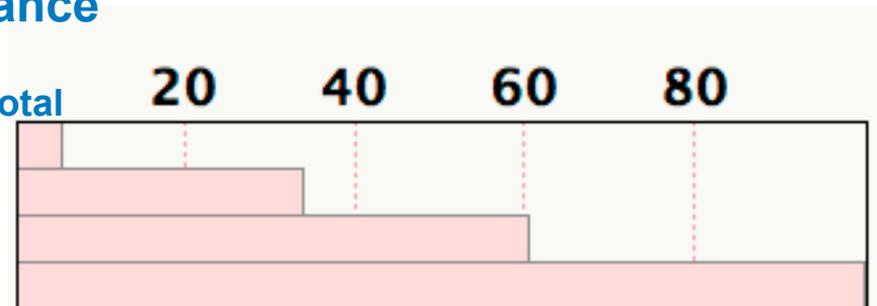


Module degradation [susceptible bias only] viewed as a function of lab to determine if any labs are more severe than others.

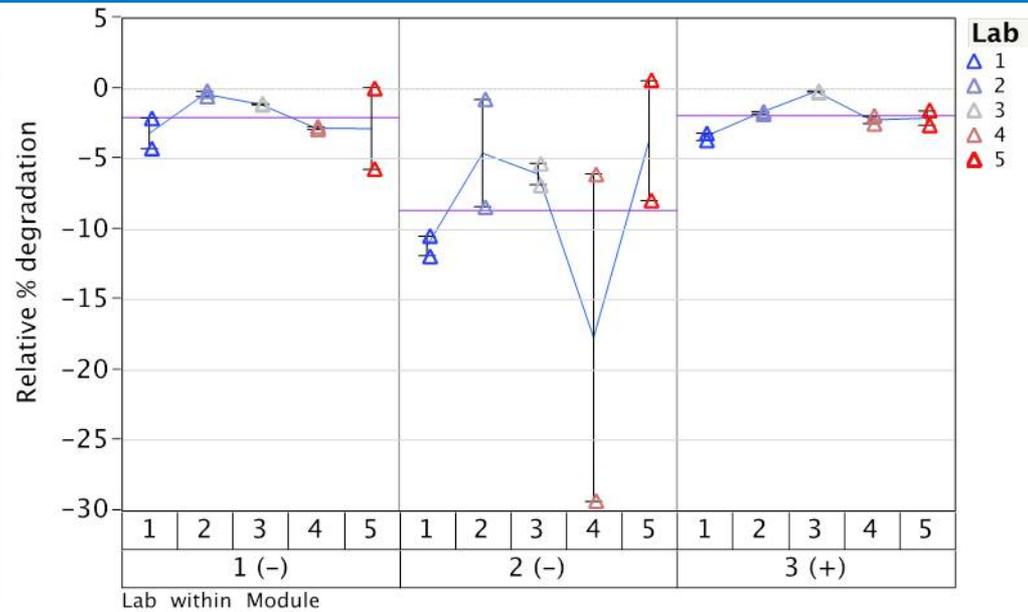
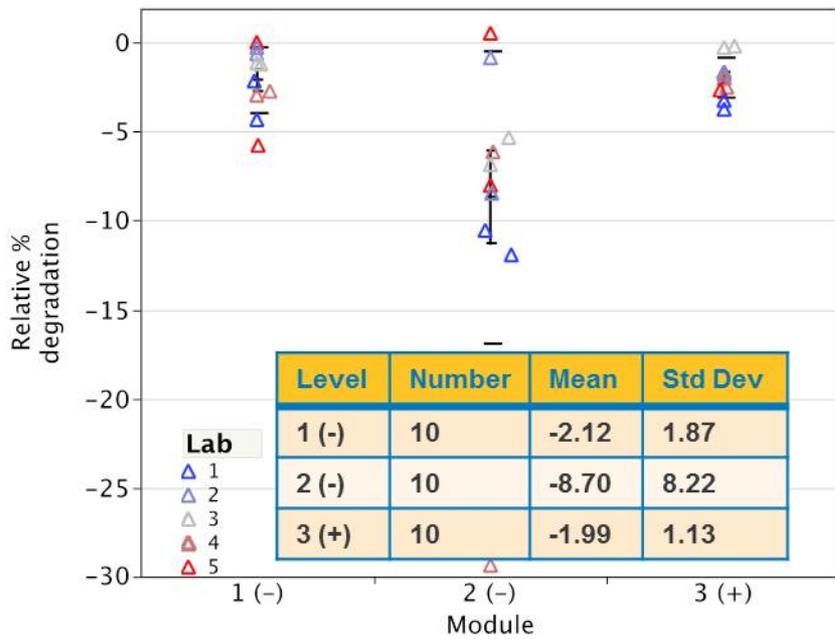
The analysis shows that the choice of lab was the least influential component of the variation, the type of module was the next important factor, but variation of results *within* a given module type (residual) was the most influential.

## Analysis of Variance

| Component       | Var Component | % of Total |
|-----------------|---------------|------------|
| Lab             | 2.03          | 5.5        |
| Module          | 12.47         | 33.8       |
| Within/Residual | 22.34         | 60.6       |
| Total           | 36.83         | 100.0      |



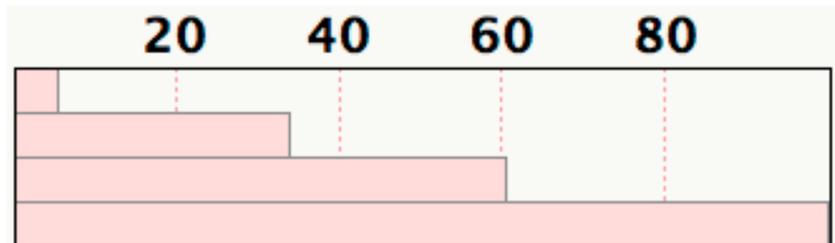
# Distinguishing variability within design versus within lab



- Variability within lab, such as gradients in the chamber, would add randomness to all designs equally; however, equal variability between designs was not found – standard deviation varies significantly between design. Design 2, an older module type with less highly regulated process control, showed extreme variability; design 3, the least variability.
- Variability within (60.6%) a given module design at a given lab is therefore largely attributed to variability within the design.

## Analysis of Variance

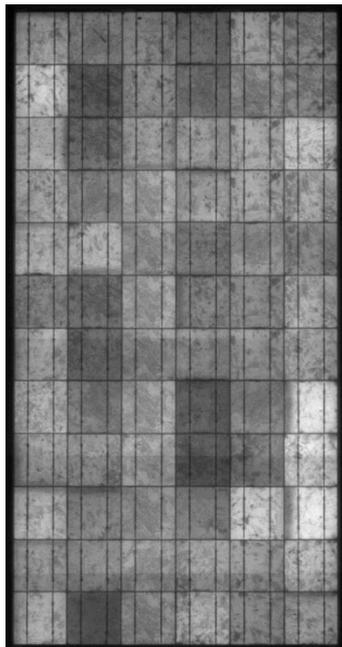
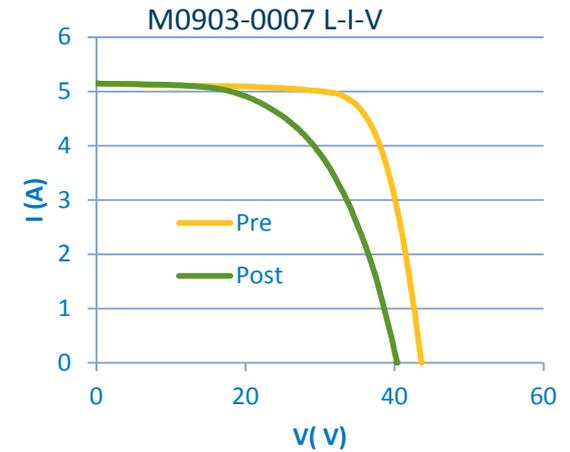
| Component       | Var Component | % of Total |
|-----------------|---------------|------------|
| Lab             | 2.03          | 5.5        |
| Module          | 12.47         | 33.8       |
| Within/Residual | 22.34         | 60.6       |
| Total           | 36.83         | 100.0      |



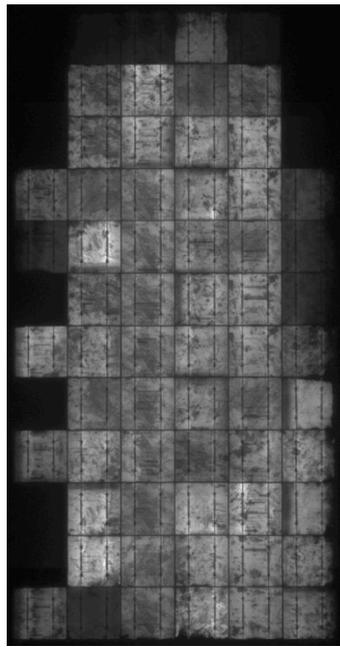
# Results of module design 2 from lab 4

| NREL ID    | Round | Sequence | Voc (V) | Isc (A) | FF (%) | Vmax (V) | I <sub>max</sub> (A) | P <sub>max</sub> (W) | P <sub>max</sub> change (%) |
|------------|-------|----------|---------|---------|--------|----------|----------------------|----------------------|-----------------------------|
| M0903-0007 | 0     | -1000V   | 43.59   | 5.14    | 74.03  | 34.97    | 4.74                 | 165.80               |                             |
| M0903-0007 | 96hr  | -1000V   | 40.32   | 5.15    | 56.41  | 28.2     | 4.15                 | 117.13               | -29.36                      |
| M0903-0014 | 0     | -1000V   | 43.57   | 5.17    | 73.14  | 34.64    | 4.76                 | 164.92               |                             |
| M0903-0014 | 96hr  | -1000V   | 43.43   | 5.19    | 68.71  | 34.42    | 4.5                  | 154.82               | -6.12                       |

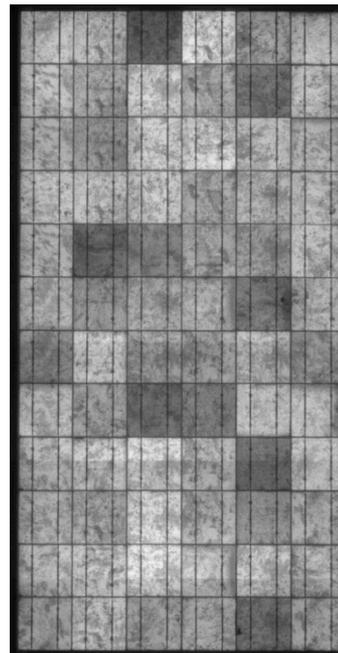
## Potential-induced degradation in the most degraded module design



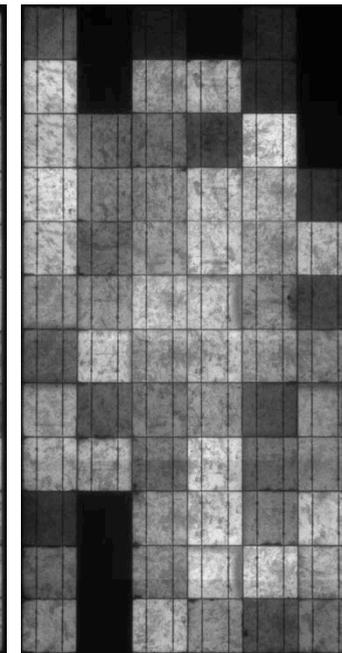
EL: M0903-0007, pre



EL: M0903-0007, post



EL: M0903-0014, pre



EL: M0914-0014, post

Images/Data:  
Sascha Dietrich  
Fraunhofer CSP

# Lessons learned during testing

- **Startup-sequence as written (simultaneous ramp up of T and RH) can lead to excess humidity on module surfaces because they are cooler.**
  - Solution is to ramp temperature, and then ramp humidity when module temperature is reached.
  - Monitoring of leakage current, relative humidity, and temperature of each module will be implemented as a record of stability
- **Sensitivity to temperature and relative humidity; possible solutions:**
  - Reduce T limits from  $\pm 2^{\circ}\text{C}$  to  $\pm 1^{\circ}\text{C}$
  - Reduce RH limits from  $\pm 5\%$  to  $\pm 3.5\%$
  - Monitor each module T, leakage current, and system RH during test

# Conclusions

- 3 module designs completed testing at 5 labs for system voltage durability
- The test was able to statistically significantly discern between the module designs for potential-induced degradation
- Potential-induced degradation was confirmed in the modules (EL & LIV characterization)
- lab to lab variability was the least influential variable, but its effect can be seen
- The test (per IEC 62804 draft) appears successful with respect to the scope of this round robin with results of the three modules analyzed
  - Consistent pass/fail results, except for one design with mean degradation -2.12% relative that failed at one lab. The largest variability is attributed to variability within the module design.
- Areas for improvement identified, including need to minimize non-equilibrium moisture on start-up, better system monitoring, and tighter testing limits on T and RH