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Technology Development for High-Efficiency Solar Cells and Modules Using Thin (<80 µm) Single-Crystal Silicon Wafers Produced by Epitaxy

June 11, 2011 — April 30, 2013

T.S. Ravi
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Santa Clara, California

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Subcontract Report
NREL/SR-5200-58593
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Executive Summary

The objective of this 18-month program was to demonstrate the viability of high-efficiency thin (less than 80 μm) monocrystalline silicon (Si) solar cells and modules with a low-cost epitaxial growth process.

The program was in two phases with goals that were progressively designed to show the commercial viability of the Crystal Solar approach. Phase I focused on showing the basic feasibility of in-house-developed equipment for the porous Si creation and the epitaxial growth, and on demonstrating full-size cells that exceeded 15% in efficiency.

Phase II was focused on further improvement of the equipment productivity and the cell efficiency and demonstrating the pathway to industrialization of this process. Crystal Solar demonstrated a batch of 24 wafers and a growth rate of >4 microns/minute using the production version of our epitaxial reactor. Furthermore, working with Prof. Rohatgi of Georgia Tech, we were able to demonstrate close to 17% efficiency on cells made with this epitaxial reactor. One deliverable was to demonstrate substrate reuse >50 times, followed by making epitaxial cells from successive peels. In the past, Crystal Solar has demonstrated that substrates can be reused >50 times without loss in the epitaxial quality as evidenced by the lifetime. However, we were not able to demonstrate five subsequent cells before the program's end due to constraints in the cycle times involved with substrate reclaim within the current operating capacity at Crystal Solar and with our processing partners.

Another important objective of the program was to show a plan for a 100-megawatt (MW) factory using Crystal Solar's gas-to-module approach using the best cost numbers as measured using our in-house epitaxial reactor and anodic etcher as well as cost estimates from various equipment and chemical and materials vendors. Crystal Solar demonstrated that a cost of <$0.50/watt is feasible for a 100-MW line with a capital cost of ~$0.70/watt.

In summary, while one of the deliverables was not met due to the timing of the program, we believe that all of the factors required to enable industrialization of the epitaxial approach were demonstrated.

Table of Contents

Introduction

Crystalline Si has continued to lead the market in the worldwide adoption of solar energy with over 85% market share. Much of this growth has happened in the last few years since the photovoltaic (PV) modules have dropped in price to below $1/watt due to massive vertical integration driven largely by Chinese manufacturers. Although this growth has been impressive, the cost of making these panels has not scaled down, thus resulting in significantly reduced gross margins and in many cases a net loss for the manufacturers. It is also clear that even with massive vertical integration with Si cell and module manufacturing, within one company the cost of making a panel has only leveled off to about $0.60/watt, well short of the <$0.50/watt numbers suggested by the U.S. Department of Energy (DOE) for true grid parity. What is needed is a completely different approach to manufacturing the Si, which still constitutes the single largest cost factor in the solar module.

Although kerfless approaches like implant-based cleaving and epitaxial thin Si on porous Si have been suggested in the past as ways to reduce the consumption and cost of the Si in the panel, to date there exists no production-proven way to use these approaches cost-effectively to make a kerfless module. Furthermore, since many of these approaches also use thin Si (less than 70 microns thick), a further barrier exists in terms of handling the thin Si all the way through cell creation and module formation.

Crystal Solar has addressed both these issues, first by developing the world's first production-worthy high-throughput solar epitaxial reactor and using this reactor to demonstrate thin cells and modules with high yield. The following pages document the results generated during the 18-month NREL SunShot program, starting with the porous Si creation and all the way to module formation. A significant part of the work had to do with showing the true cost of the process and planning of the commercialization of this technology.

We have demonstrated not only the manufacturing viability of the epi-based kerfless process using in-house-developed epitaxial reactors, but we have also shown that this approach can indeed bring the overall PV module costs down to <0.50/watt.

Phase I Deliverables Summary

Phase I			
Deliverable	**Criteria and Deliverable**	**Date**	**Crystal Solar Notes**
D1	3.1.2.1 – D1: NREL monitors Crystal Solar's three epitaxial Si depositions and the observed samples will be shipped to NREL to verify that these three <80-µm epi-Si wafers were grown at a rate of >3 µm/minute with uniformity better than 80%.	D1: M2	Completed successfully: Crystal Solar demonstrated average growth rate of 3.1 microns/min in their prototype epitaxial reactor.
D2	3.1.2.3 – D2: Four thin (<80 µm) free-standing gettered epitaxial Si wafers (~100 cm^2) will be submitted to NREL to verify that they exhibit resistivity ~1 Ohm-cm and minority carrier lifetimes >10 µ-sec. In addition, four <80-µm-thick 2-cm x 2-cm wafers will be submitted to NREL to verify BSRV of <1000 cm/s.	D2: M4	Completed successfully: NREL measured >10 microseconds average on the shipped thin epitaxial wafers.
D3	3.1.3.1 – D3: Deliver three 125 mm x 125 mm thin (<80 µm) epitaxial Si solar cells, bonded to glass, with 15% efficiency to NREL for I-V and DIV characterization and spectral response measurements.	D3: M6	Completed successfully although delayed by 3 months: NREL measured >15.2% efficiency on each of the wafers submitted for this purpose.

D4 **Reclaim Demonstration**	3.1.4.3 – D4: Deliver five 125 mm x 125 mm (<80 µm) epitaxial Si cells with efficiency >15% with all cells fabricated from and lifted off of a single Si substrate.	D4: M8	Completed successfully.
D5 **Module Fabrication**	3.1.4.5 – D5: Deliver four mini-modules (260 mm X 260 mm in size) to NREL composed of four (125 mm X 125 mm) thin (<80 µm) epitaxial Si cells for I-V characterization. The mini modules must exhibit a module efficiency of 13%.	D5: M8	Completed with average efficiency >13%.
D6 **Reclaim Demonstration**	3.1.4.6 – D6: Deliver 20 successfully released thin (<80 µm) epitaxial Si samples (>1 cm^2 in area) substrates from a single Si substrate that exhibit <15% degradation in lifetime (from 10 µ-sec) over twenty reuses.	D6: M9	Completed successfully: NREL measured minority carrier lifetimes for 20 epitaxial Si substrates.
D7 **Epitaxial Tool Throughput Demonstration**	3.1.5 – D7: Deliver a report that documents production operation of two epitaxial chambers and associated cool-down chamber and susceptor handling robotics. Demonstrate a per-chamber tool throughput of 25 wafers per hour (3 µm/min dep rate; 80-µm-thick epi) and document throughput, yield, and TAKT time.	D7: M9	Completed successfully: NREL observed tool productivity and measured thickness uniformity.

D8 **Manufacturing Flow and Capex Analysis**	3.1.6 – D8: Deliver a report that documents a detailed cost model of the manufacturing process flow that includes tool throughput, yield, consumable costs, optimal number of Si wafer reuses, optimal cell and module efficiency, and demonstrate factory capex costs of <$1/Wp for 100 MW/year capacity.	D8: M9	Completed successfully: A factory report was generated using commercially available cell and module equipment.

Phase II Deliverables Summary

D9 **Epitaxial Reactor and Process Development**	3.2.2.1 – D9: Report documenting three epitaxial Si depositions of 24 wafers/batch using the Rev 3.0 tool. 24 samples from a single batch will be shipped to NREL and random sampling will be used to verify thickness uniformity of >90% based on FTIR mapping. The report shall also include in-house FTIR results for all three epi-Si depositions that confirm thickness uniformity of >90% and a deposition rate of >4 μm/min.	D9: M10	Completed successfully: NREL observed epitaxial equipment and deposition rates and with FTIR mapping verified thickness nonuniformity of <10%.
D10 **Solar Cell Fabrication**	3.2.3.1 – D10: Deliver three 125 mm x 125 mm thin (<80 μm) epitaxial Si solar cells with 17% efficiency to NREL for I-V and DIV characterization and spectral response measurements and report documentation for this task.	D10: M14	Completed successfully: Verified >16.7% at NREL (which is within the 3% error margin).
D11 **Cell Efficiency with Reclaim**	3.2.4 – D11: Deliver to NREL five thin (<80 μm) epitaxial Si solar cells (125 mm x 125 mm) fabricated with epi-Si wafers grown on the same Si substrate after 50 reuses. The five deliverable cells will be fabricated from reuses 51-55 (from a single Si substrate) with three of the five cells exhibiting at least 16% efficiency.	D11 M19	Did not complete; although we were able to demonstrate 50 reuses of the substrate, we couldn't make the cells in time before the program ended.

D12 **Module Fabrication**	3.2.5.4 – D12: Deliver to NREL four mini-modules (260 mm x 260 mm in size) composed of four thin (<80 μm) epitaxial Si cells for I-V characterization and reliability tests. The mini-modules must exhibit a module efficiency of 14%.	D12: M8	Completed successfully: NREL measured 14% efficiency on Crystal Solar sub modules.
D13 **Module Testing**	3.2.5.5 – D13: Deliver modules for testing. NREL shall conduct 1,000 hours of damp heat testing on the modules in accordance with IEC 61215. Two of the modules must exhibit less than a 10% drop in maximum power (Pmax) (compared to initial LIV results) after 500 hours of damp heat testing (85C/85RH).	D13: M6	Partially successful: one of the modules passed with 10% degradation after 500 hours of damp heat testing.
D14 **Cost Modeling and Factory Planning**	3.2.6 – D14: Provide a D14 deliverable report that documents the development of a detailed cost model with individual demonstrated parameters (e.g., epi deposition rate, yield, consumables costs, optimal number of Si wafer reuses, capex, cell and module efficiency, TAKT time) coupled with capex model developed in Phase 1 to demonstrate <$1/Wp manufacturing cost when scaled to volume. A report will be provided in the D14 deliverable report.	D14: M18	Completed successfully: A comprehensive cost analysis and factory modeling was done for Crystal Solar's "gas to module" process. The results were discussed in terms of total capital expenditures, as well as all-in module costs. A baseline scenario demonstrated a production capital cost of $77M (including one-time expenditures related to gas handling and facilitization), thereby demonstrating significantly less than $1/W (as originally targeted in the original proposal to DOE by Crystal Solar). A total cost of $0.45/W was also modeled. Both of the above metrics allow Crystal Solar to achieve DOE module cost targets of $0.50/W.

Tasks 1 and 7: Porous Si Process and Tool Development

The objective was to further develop anodic etching technology for the fabrication of porous Si layers on large-area single-crystal Si substrates for subsequent epitaxial deposition.

Figure 1 shows a cross-section of a representative porous Si layer. The key challenge here was to get a uniform thickness. We achieved this by carefully engineering the field around the substrate wafer in an anodic etch cell. The thickness uniformity from the center to the edge as measured by SEM cross-section is shown in Figure 2.

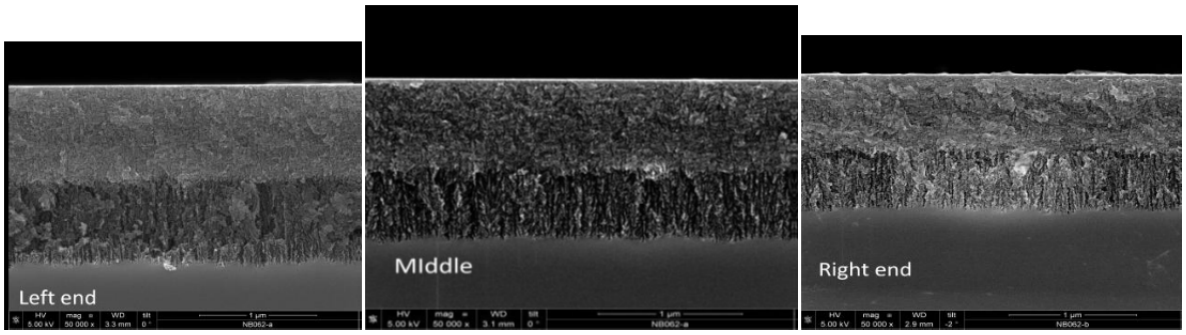


Figure 1. Representative SEM cross-section of anodically etched wafers.

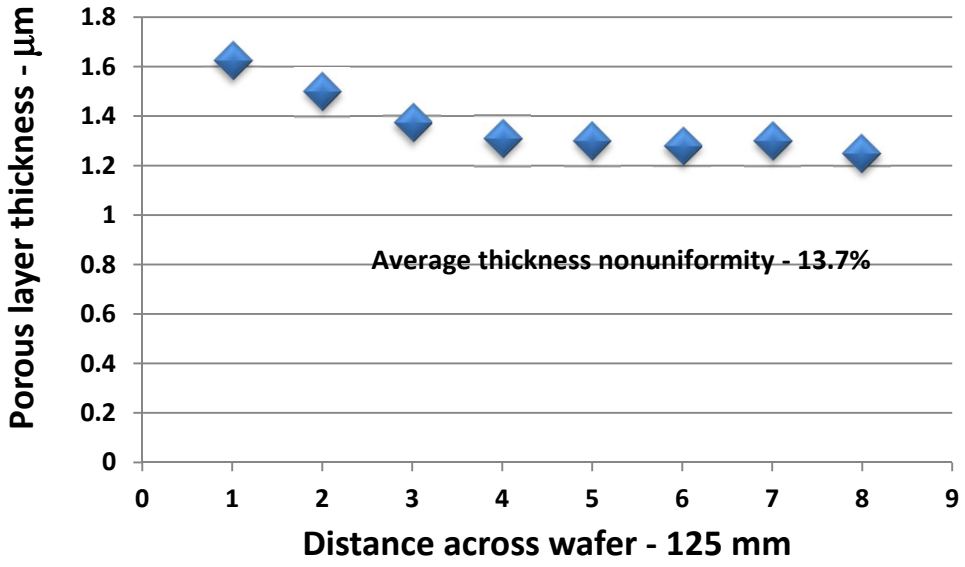


Figure 2. Thickness variation from center to edge showing an average nonuniformity of 13.7%.

Figure 3. Production anodic etch reactor and 10-wafer batch loading system.

By the end of Phase II we had developed a multi-wafer batch anodic etcher. Figure 3 shows the system in the Crystal Solar lab along with a 10-wafer vacuum chuck for holding the substrates. We have successfully tested this, and Figure 4 shows the visual appearance uniformity within a batch of 10 wafers. Having a batch of at least 10 wafers enables throughputs of greater than 200 wph, thus qualifying for our production use.

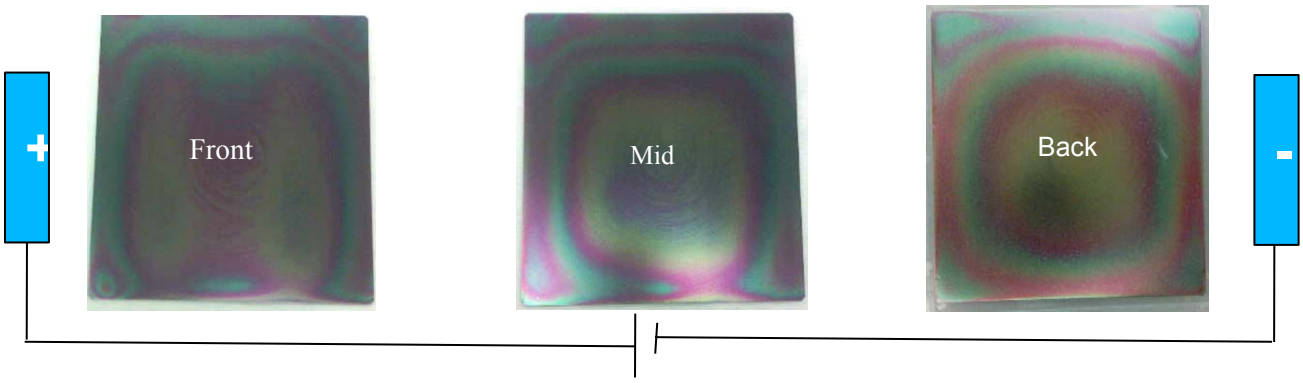


Figure 4. Visual appearance of anodic etched wafers in a batch showing uniformity from wafer to wafer.

Tasks 2, 5, and 8: Epitaxial Reactor Hardware, Process Development, and Throughput

Crystal Solar was founded on the basis of developing a high-throughput epitaxial reactor for solar applications. Our approach is based on high-temperature CVD of trichlorosilane to Si in a mini batch reactor. Figure 5 shows our prototype reactor. It is a manually loaded reactor with an eight-wafer batch. During Phase I we had a target growth rate of 3 microns/minute and a target nonunformity of 20%. We exceeded these requirements by a wide margin. Figure 6 shows the average growth rate and thickness nonuniformity from this prototype reactor.

Figure 5. Crystal Solar experimental prototype epitaxial reactor.

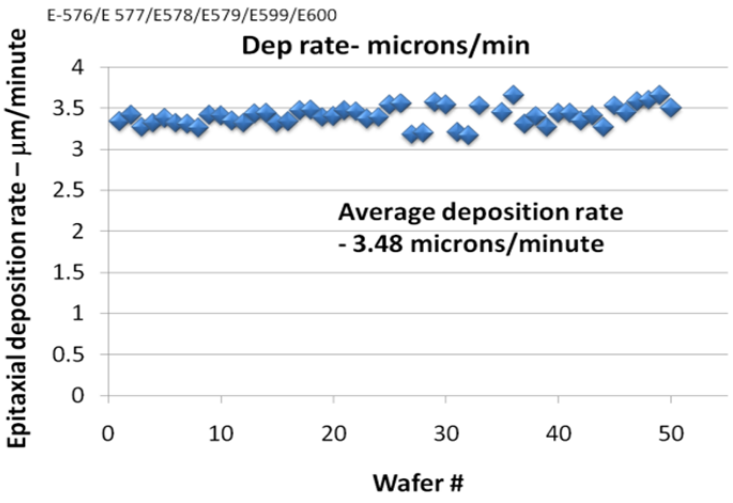


Figure 6. Growth rate for three consequent runs in Crystal Solar prototype epi reactor with <10% nonuniformity.

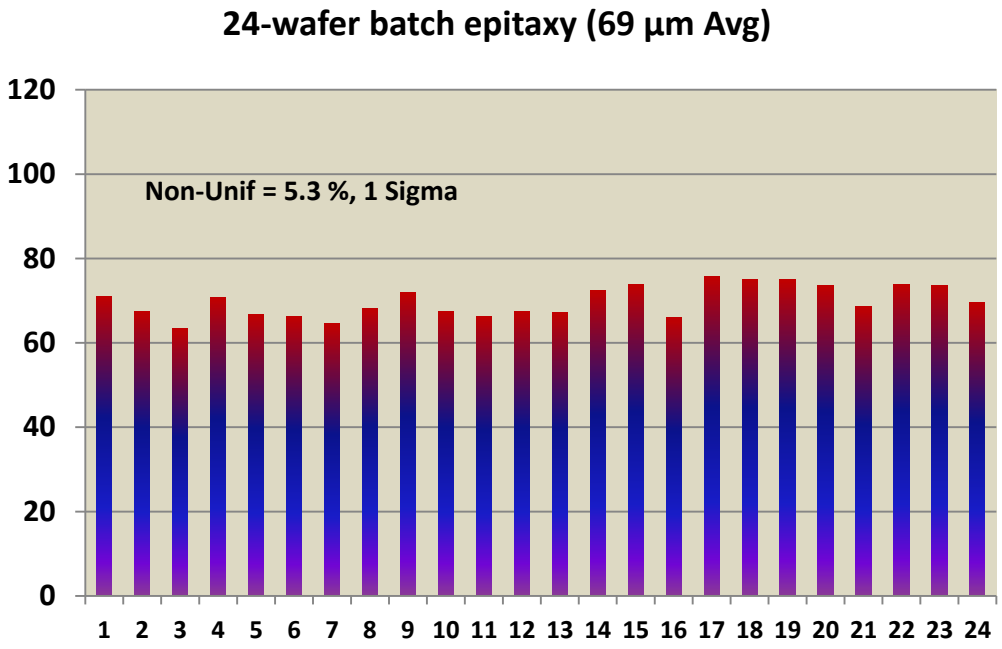
In Phase II, we not only had to demonstrate >4 microns/min deposition rate but also a thickness nonuniformity of better than 10%. In addition we had to show that the epi wafer was of high quality.

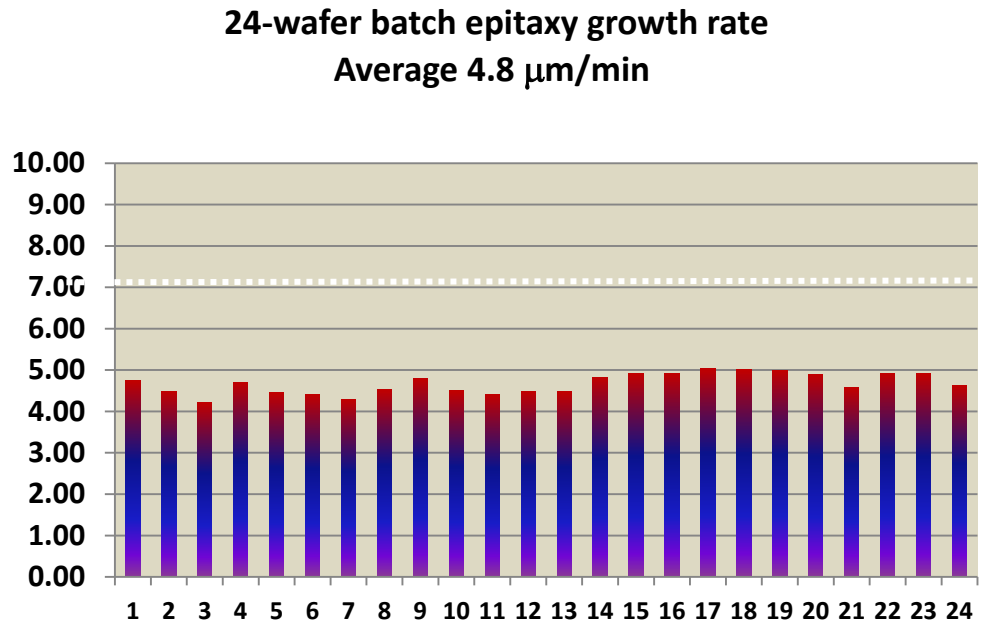
Figure 7 shows the Crystal Solar pilot epi reactor with automatic loading and unloading of the substrates.

Figure 7. Crystal Solar production epi reactor with automatic loading and unloading.

We were able to exceed both the growth rate and uniformity targets. Using the 24-wafer batch we were able to demonstrate a throughput of >30 wph/chamber, exceeding the target set by the program.

Figures 8 and 9 show the thickness and the growth rate of a 24-wafer batch.





Figures 8 and 9. Thickness and growth rate variations of Crystal Solar's 24-wafer batch epi reactor.

Epi Quality: The production system has shown consistently good-quality epi for P-type and N-type wafers. Figure 10 shows the average lifetime of P-type and N-type wafers during several epitaxial runs, showing the consistent quality of our epitaxial films.

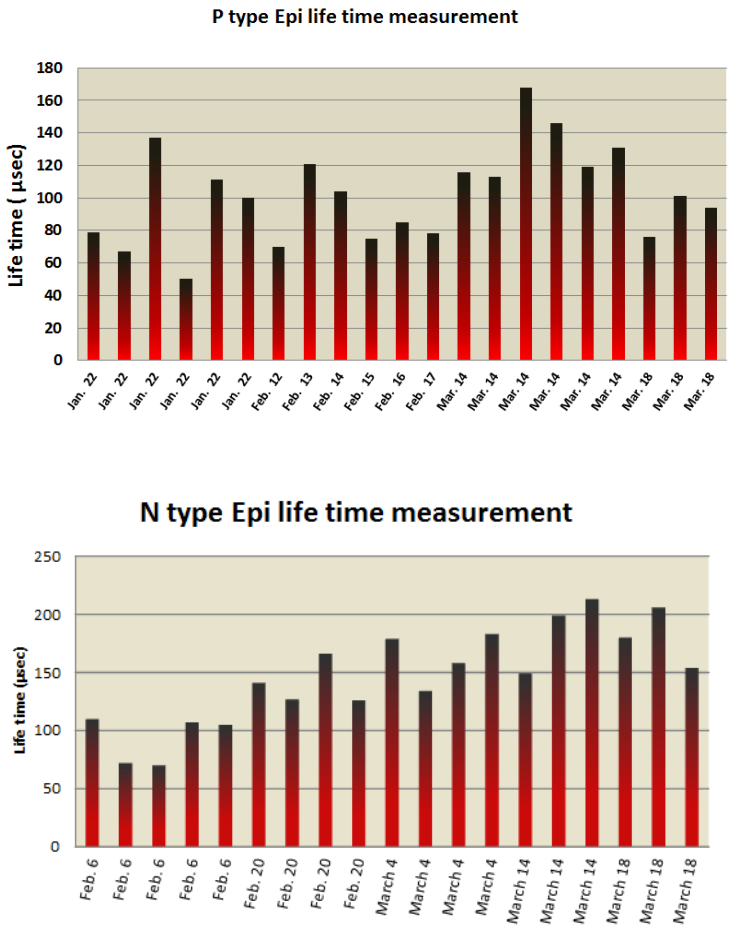


Figure 10. Epi quality from run to run with P-type (top chart) and N-type (bottom chart) epi.

Epi Reactor Throughput: With the production reactor we were able to verify the target throughput. Figure 11 shows the the timing diagram of our epi reactor with a 24-wafer batch. This was done in the presence of the NREL program monitor. The total cycle time for a batch of 24 wafers is about 55 minutes, which trnaslates to a throughput of >300 wph.

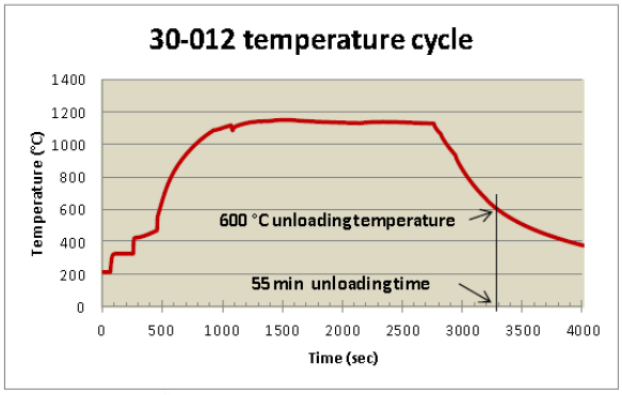


Figure 11. Timing diagram for a 24-wafer epi batch, total cycle time <55 m (verified by NREL).

Tasks 3 and 5: Thin Si Solar Cell Fabrication

Crystal Solar has developed a simple screen-printed Ag process for thin Si solar cell fabrication in collaboration with Prof. Rohatgi's group at Georgia Tech. By optimizing the various steps of texture etching, diffusion, nitride antireflective coating, and screen printing, we were able to demonstrate with the prototype epi reactor efficiencies under glass of around 15.5%. One of the limitations was that the prototype epi reactor produced lower lifetime due to lack of automation in loading and unloading samples, which resulted in contamination of the reactor.

During Phase II of the program we were able to increase the wafer size to 125 mm x 125 mm and along with significantly better material (see previous section) from the production epi reactor (with automatic loading) we were able to demonstrate the efficiency close to 17%, the original target. Figure 12 shows an NREL-measured I-V curve for a 16.7% thin epi cell measured under glass. The cell itself is shown in Figure 13 with the measurement tabs sticking out. We believe that taking into account transmission losses (of around 9%) this is equivalent to ~18.3% absolute cell efficiency.

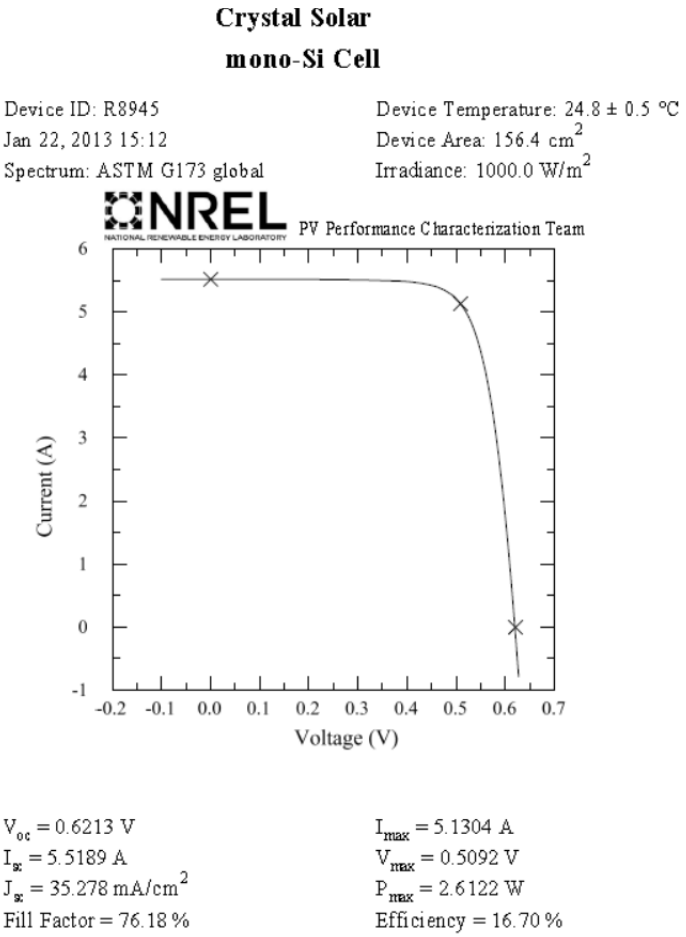


Figure 12. Epi thin Si cell measured under glass.

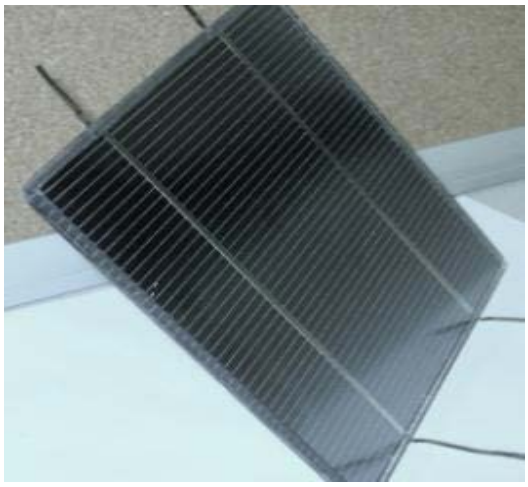


Figure 13. Epi thin silicon cell attached to glass.

The IQE analysis of the cell is shown in Figure 14. Based on this, it is expected that further improvements can be made with better emitter passivation, backside passivation, and light trapping. The backside passivation is also critical for high V_{oc} and different passivation materials are currently being investigated at Crystal Solar.

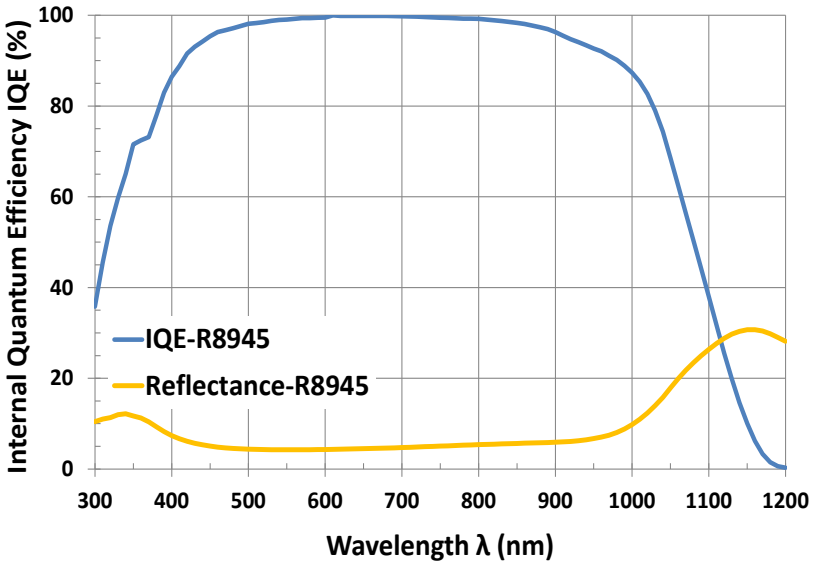


Figure 14. IQE analysis of the cell shown in Figure 13.

Cell efficiency as a function of bulk lifetime was further modeled using PC-1D to demonstrate the pathway to achieve efficiency >19% for a 50-µm-thick Si solar cell. Crystal Solar has consistently demonstrated high lifetime, as shown in Figure 10. According to the modeling results, the lifetime achieved at Crystal Solar is no longer the limiting factor of the efficiency. Further increases in efficiency will depend on improvement of the front surface passivation, back surface passivation, light trapping, and tabbing techniques, as indicated in Figure 15.

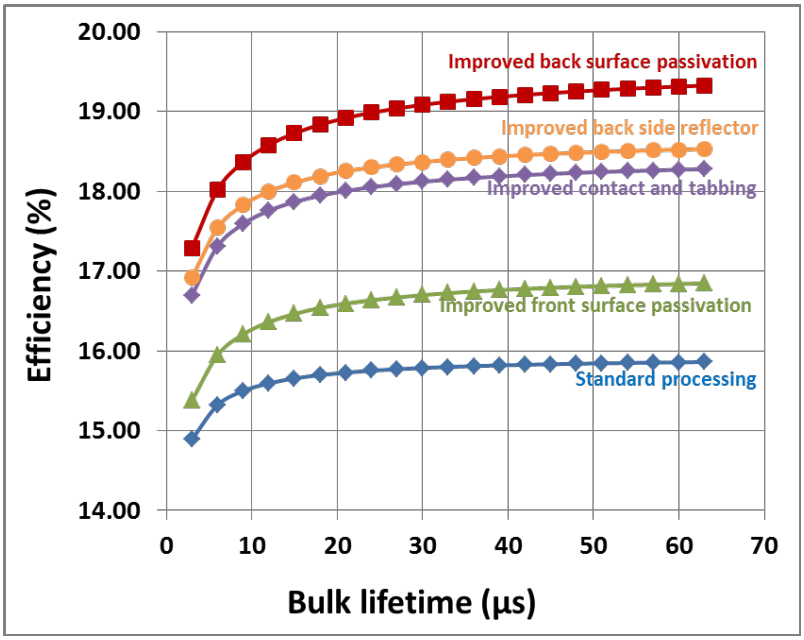


Figure 15. PC-1D modeling: efficiency as a function of bulk lifetime.

Tasks 4 and 11: Module Fabrication and Testing

Crystal Solar has made multiple 2 x 2 and larger-size modules using 125 mm x 125 mm cells. Our module-making process involves transferring our thin epi to glass using the encapsulant and then metallizing the back side of the solar cells to make contacts. Figure 16 shows the NREL I-V test for one of the thin Si modules showing a 14% module efficiency. Figure 17 shows a 24-cell (105 mm x 105 mm) module with a 35W output and an aperture area efficiency of ~ 14.4%.

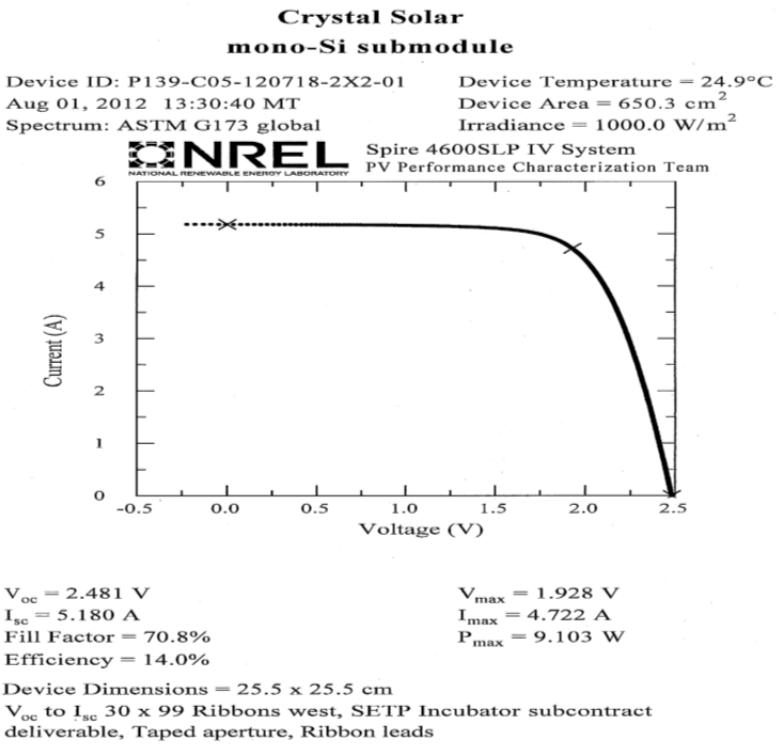


Figure 16. I-V curve of a 2 x 2 module made showing 14% efficiency.

Figure 17. A larger module (24 wafers, 38W) using Crystal Solar epi thin Si cells.

A Crystal Solar Technology Concept Module (>15% efficiency) was displayed at the Solar Power International Conference and at the EUPVSEC in 2012. Figure 18 shows the module. This is the first example of commercial-scale modules fabricated with our epitaxial Si technology.

Figure 18. *Epi Thin-Silicon* concept module.

Module testing: We have obtained preliminary data from NREL on the HAST testing and were able to show that we can pass the 500-hour damp heat test with a maximum of 10% degradation in power. Figure 19 shows the dual-cell module that was tested at NREL, and Figure 20 shows the before and after I-V curves. As can be seen the degradation is ~10%. We are continuing these tests internally with larger modules.

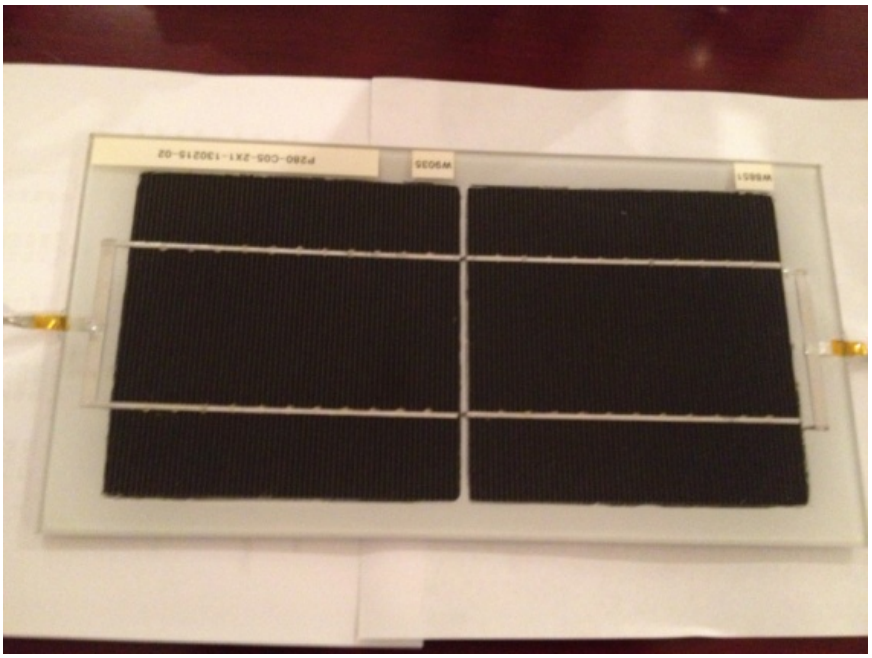
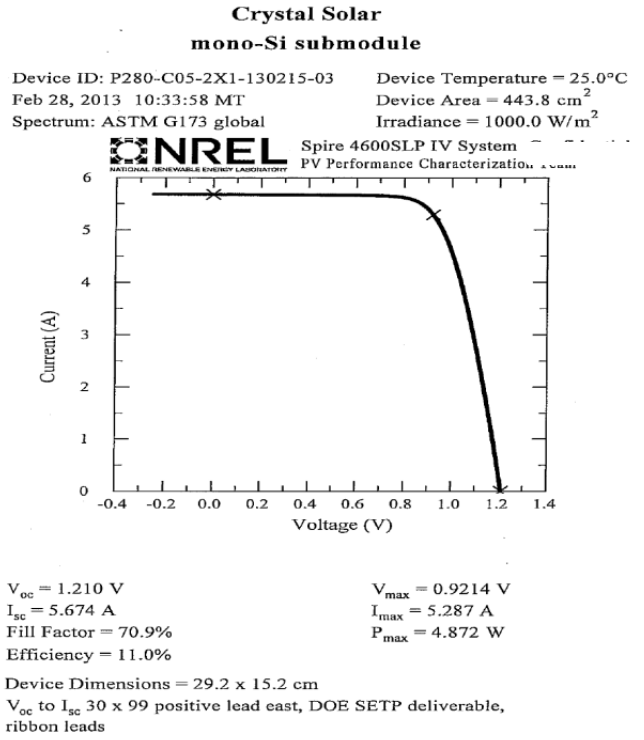


Figure 19. Two-cell submodule tested at NREL.



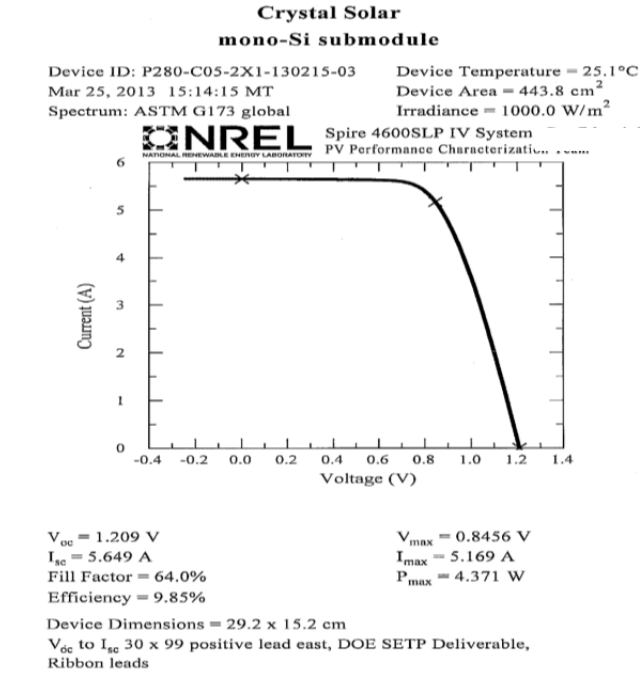


Figure 20. I-V curves before and after 500 hours of damp heat test at NREL showing ~10% degradation in power.

Task 10: Scale Up Simulation

Substrate reclaim is key to achieving low cost. Our cost models indicate that a minimum of 50 reuses are needed to achieve cost goals with the *Epi Thin-Silicon* lift-off approach. Crystal Solar has developed a simple reclaim process that involves using low-cost chemicals to reclaim the surface. Using this approach we have shown over 50 reclaims with a baseline lifetime of >10 microseconds using the prototype epitaxial reactor.

Figure 21 shows the deviation from the baseline lifetime based on this approach showing no trend in lifetime after 50 reuses.

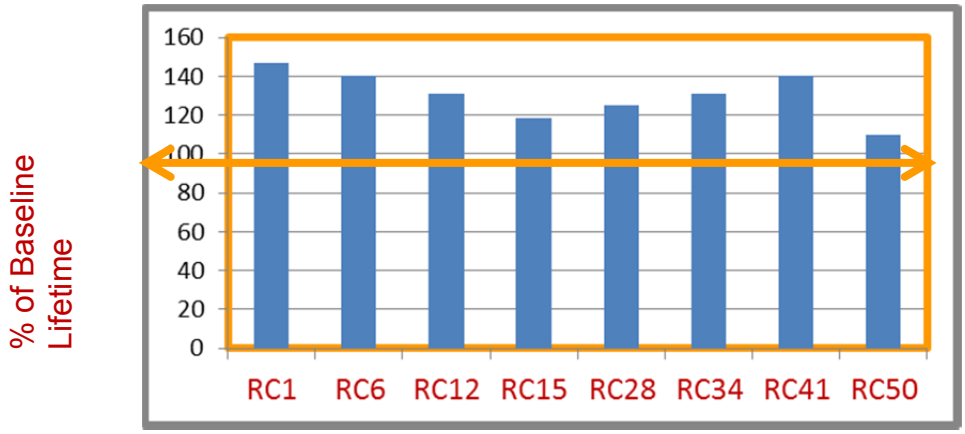


Figure 21. Lifetime as a function of number of reuses; baseline lifetime is 10 µs.

We had launched a similar reclaim experiment using the production epi reactor with the goal that after 50 reclaims five cells would be made in succession. Unfortunately, by the end of the program we couldn't complete this milestone. We had however shown some data in Phase I that showed no degradation (or correlation) in the efficiency numbers with subsequent reclaims. This is shown in Figure 22.

Substrate use	Voc-mV	Isc-mA/cm2	FF-%	Efficiency%
New wafer (Use 1)	605	31.0	73.7	13.8
Use 2	605	31.6	72.8	13.9
Use 3	621	34.1	75.9	16.1

Figure 22. Data on efficiency versus substrate reuse.

Tasks 6 and 12: Manufacturing Flow, Capex Analysis, Cost Modeling, and Factory Planning

We developed an integrated process flow for manufacturing thin Si modules starting with trichlorosilane gas. The major benefit of this approach comes with the avoidance of expensive poly-Si, ingoting, and wafering of Si, and it enables vertical integration on a much smaller scale. Crystal Solar's high-throughput epi reactor has enabled this.

The factory layout is quite flexible and can be adapted to fit into an existing structure. For this design, a circular flow was utilized. The cell-fab area occupies the largest percentage of the factory, and the flow of this section generally proceeds from left to right down the length of the building. The wafer-fab area is located below on the left side of the cell-fab, and the module-fab area is below on the right side.

The footprint of the 100-MW integrated plant is compact and highly suitable for modular expansion. The total fab area is 170 x 55 m^2, which is approximately 100,000 ft^2. Allowing for additional non-fab space for logistics, gas/chemical handling, and storage, the entire facility can be housed in a space of ~250,000 ft^2. Figure 23 shows the layout of a 100-MW factory that was developed as part of this deliverable.

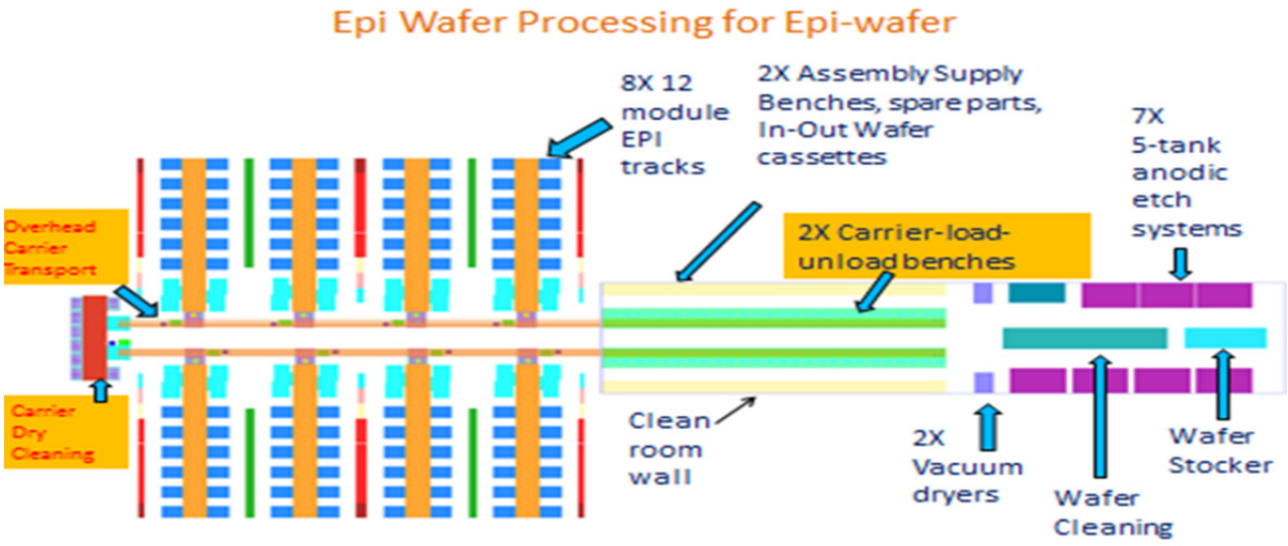


Figure 23. Layout of 100-MW fab for epi reactors with porous Si. Note that only eight epi reactors are needed for a 100-MW line.

	Equip Capex
	($)
Wafer	$40,929,536
Cell	$24,619,265
Module	$4,751,400
Sum	**$70,300,201**

All-in Module Cost Summary					
	Depreciation	**Consumables**	**Labor**	**Rent**	**All-in-cost**
	($/W)	**($/W)**	**($/W)**	**($/W)**	**($/W)**
Wafer	$ 0.044	$ 0.105	$ 0.006	$ 0.004	$ 0.159
Cell	$ 0.028	$ 0.113	$ 0.007	$ 0.007	$ 0.155
Module	$ 0.006	$ 0.118	$ 0.005	$ 0.004	$ 0.133
Sum	**$ 0.077**	**$ 0.337**	**$ 0.018**	**$ 0.015**	**$ 0.446**

Figure 24. Capex and cost/watt for a 100-MW, 50-micron-thick epi integrated module line.

Figure 24 shows the capex and the total cost for a 100-MW line based on the detailed analysis of Crystal Solar's process flow and all the equipment necessary for cell and module manufacturing. The total cost of the module is <$0.45/watt with a capex of $0.77/watt.

In comparison, a typical Crystalline Si line including the Poly has a capex of $1.50/watt with the best cost numbers for the module around $0.60/watt. This shows the potential of the epitaxial kerfless approach.

Thin-Epitaxial-Wafer-Based Heterojunction Cell Development at NREL (NREL PI: Dr. Qi Wang)

This work was done jointly with Dr. Qi Wang and is based on work done by Dr. Wang on P-type HIT cells. For standard HIT cell fabrication, the thin epi wafer was extracted from the substrate and processed as a thin wafer. While this proved difficult, Dr. Wang was able to make a few cells, and Figure 25 shows the best results to date.

Sample	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
T4810A	631	31.45	77.2	15.3
T4810B	637	31.83	75.8	15.4

Figure 25. HIT cells fabricated by Dr. Qi Wang (NREL) on Crystal Solar 50-micron epi.

As can be seen, while the V_{oc} and FF are reasonable, the J_{sc} is quite low, and we attribute that to the poor lifetime of the epi (this was from our prototype epi reactor). In addition, these were free-standing samples, and as such, the yields were quite low and the actual area of the samples was less than 10 cm^2.

In the second phase of this program, to be able to handle large-area cells, Crystal Solar developed an approach where the front side of the epi wafer is processed like a typical HIT cell and the back side processed using Crystal Solar's baseline approach of P++ Epitaxial BSF and backside aluminum deposition for metal contacts with the thin cell attached to a glass handle.

As shown schematically in Figure 26, this structure represents a hybrid heterojunction-homojunction device (patented by Crystal Solar).

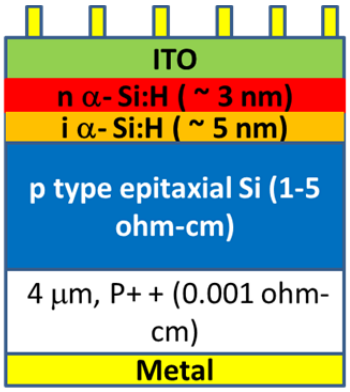


Figure 26. Concept for a heterojunction-homojunction hybrid cell.

The HIT part of the cell was completed at NREL under Dr. Qi Wang's supervision whereas the back side was completed at Crystal Solar.

Results and Prospects: Figure 27 shows the best effort to date on this hybrid cell. The results look quite promising, and although we couldn't reach the very high efficiencies we achieved with the homojunction cell, we believe that the basic process flow works.

In analyzing this we concluded that the main issue was a lack of effective passivation of the front side, followed by a lower fill factor due to front contact issues, and in general, the low lifetime of the epi that contributed to the low current.

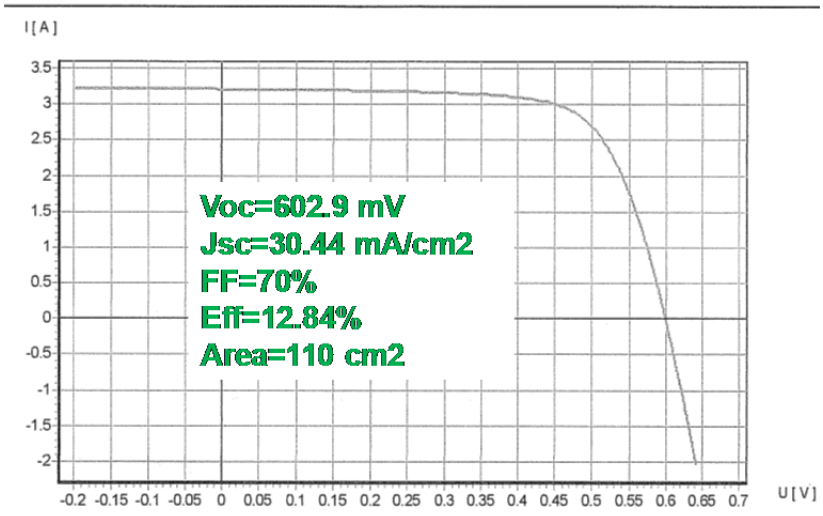


Figure 27. I-V curve of the first heterojunction/homojunction thin epi cell.

We believe that this is an attractive approach since it eliminates all of the high-temperature steps that can potentially affect the yield of the thin Si processing. We therefore plan to continue this work internally at Crystal Solar.

Summary

Crystal Solar's direct epi-wafer technology has the ability to radically change the Si PV landscape by allowing smaller-scale wafer (or integrated wafer+cell+module) plants that can be operated with sustained technical and cost advantages—rather than the huge scale and monolithic integration required by conventional Si PV.

We have not only demonstrated a high-throughput, low-COO epitaxial reactor but also high-efficiency cells and modules with less than 80-micron-thick Si. In addition, we have shown a path to commercialization with a projected cost less than $0.50/watt by using standard cell and module equipment for the processing of the thin Si cells and modules.

Future Work

Based on the work done within this program we expect over the next 12 months to focus on the following towards a commercialization path for epi-based thin Si cells and modules.

1. Demonstrate >19% cell efficiency using further innovations in the cell-making process
2. Build several KWs of large-area thin Si modules to test for various standards certifications
3. Build a pilot factory to demonstrate 25 MW for gas-to-module with an industrial partner
4. Further develop advanced cell concepts such as HIT, IBC, and PERC cells with thin epitaxial Si.

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