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Final Technical Progress Report: High-Efficiency Low-Cost Thin-Film GaAs Photovoltaic Module Development Program

July 14, 2010 — January 13, 2012

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Alta Devices, Inc.
Santa Clara, California

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NREL/SR-5200-54398
March 2012

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Executive Summary

Alta Devices has successfully completed all milestones and deliverables established as part of the NREL PV incubator program. During the 18 months of this program, Alta has proven all key processes required to commercialize its solar module product. The incubator focus was on back end process steps directed at conversion of Alta's high quality solar film into high efficiency 1-sun PV modules. This report will describe all program deliverables and the work behind each accomplishment.

Unless otherwise noted, all photos in this document are property of the authors.

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Scope of Work

Following the primary objective of the NREL/DOE PV technology incubator program, Alta Devices committed to develop and refine the processes required for demonstration of manufacturability of thin-film GaAs PV modules. Having completed each milestone successfully, a pathway to pilot production was defined and key technology risks were reduced. Alta has developed all backend process steps and improved each component of its module production to deliver the highest efficiency of any single junction PV technology. As the incubator program reaches its end, Alta continues the scale-up of its production line, with the ultimate goal of reaching grid-parity while delivering the highest efficiency PV product.

The two phases of this incubator program were defined as follows:

- Phase I: define and develop the processes required to convert Alta's solar film into cells and to assemble cells into modules
- Phase II: refine each process step in order to improve the conversion efficiency of Alta's modules

The processes included in this scope of work correspond to several cell formation steps (front metallization, back via formation, anti-reflection coating, and cell separation) and module production (matrix assembly and module encapsulation.) These steps start with fully defined solar thin films, and continue with deposition of exposed front contacts, opening of back contact vias, depositing anti-reflection coatings, separating the films into individual cells, forming electrically and mechanically interconnected matrices, and using standard techniques to encapsulate them into modules. To each step were assigned multiple deliverables for both program phases, with the goal of identifying primary and backup process options, evaluating risks, and developing optimal processes.

The program deliverables will be described in the next section along with the results obtained for each. The subsequent section will describe the trajectory of defining and optimizing processes to enable each deliverable. Finally, the appendix at the end will contain the measurements performed by NREL to validate success of each deliverable.

Deliverables & Results

There were a total of 14 deliverables equally distributed into two phases. Every deliverable was submitted on schedule and measured by members of the NREL technical team before approval. Below is a description of each deliverable and the results obtained by Alta.

Phase I

Phase I deliverables were aimed at accelerating process definitions to enable cell definition and module production. Through these deliverables Alta demonstrated < 150 μm front metal line-widths to reduce top shading losses, back via contact drilling with minimal efficiency losses, AR coating with > 35% current boost, cell separation free of cracks, matrix and module assemblies with less than 5% voltage loss relative to that of control cells, and large modules with > 14% efficiency.

The following table outlines each deliverable, its goal, and the results approved by NREL.

Task	Deliverable	Process	Goal	Result
1	D-1	Front metal contact	< 150 μm	Achieved ✓
1	D-2	Back via contact	< 5% efficiency loss	Achieved ✓
2	D-3	AR coating	> 35% boost	Achieved ✓
3	D-4	Cell separation	< 2 mm cracks	Achieved ✓
3	D-5	4-cell matrix assembly	< 5% Voc loss	Achieved ✓
3	D-6	4-cell mini-module	< 5% Voc loss	Achieved ✓
4	D-7	Module	> 0.08 m^2, > 14% efficiency	Achieved ✓

Phase II

In Phase II, the activities were focused on refining each step to improve process control and performance at the module level. The front metal line width was further reduced, the AR coating performance was optimized through appropriate metrology, the cell separation process was developed to minimize losses, and the matrix assembly process was refined to enable substantially higher efficiency.

The following table contains all Phase II deliverables along with its goals and Alta's results. The final deliverable (D-14) is still undergoing tests at NREL.

Task	Deliverable	Process	Goal	Result
5	D-8	Front metal contact	< 100 μm	Achieved ✓
6	D-9	AR coating	> 37% boost	Achieved ✓
7	D-10	Cell separation	< 5% efficiency loss	Achieved ✓
7	D-11	4-cell matrix assembly	< 3% Voc loss	Achieved ✓
7	D-12	8-cell module assembly	< 3% Voc loss	Achieved ✓
8	D-13	Mini-module	> 0.02 m^2, > 16% efficiency	Achieved ✓
8	D-14	Large-area module	> 0.125 m^2, > 20% efficiency	Achieved ✓

Detailed Work

In this section we will describe the work behind Phase I and Phase II deliverables in some detail. Most of the activities in each process involved running feasibility tests, designing experiments to verify process windows, and finally process development and optimization. For the past 18 months, Alta developed a back end process flow which is now being implemented into a first pilot production line.

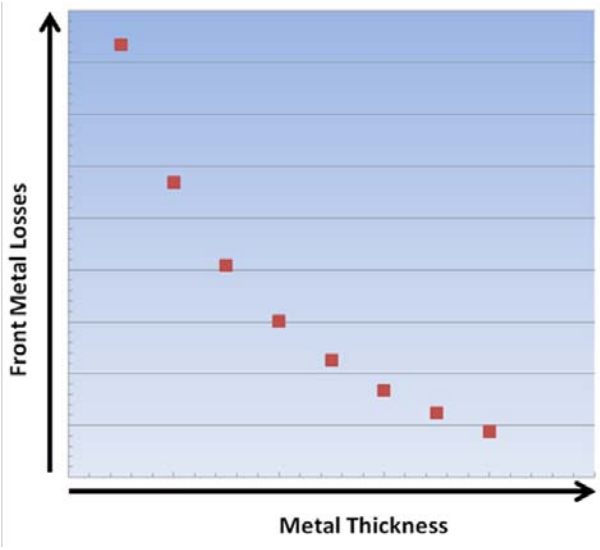
Front Metal

Alta's PV incubator program scope of work starts after the thin GaAs film is applied to a plastic carrier. The first subsequent step is the definition of front contact metallization. Because Alta's cells have low emitter sheet resistance, a front metal grid is more optimal for charge extraction than traditional thin film solutions like TCO (transparent conductive oxide.) The roadmap to improve the front metal process includes a focus on cost and manufacturability.

Our front metal design optimizes for the following parameters:

- Finger width which affects shading
- Metal-semiconductor contact resistance which affects cell performance
- Metal bulk resistance which affects cell performance
- Metal surface quality which affects interconnect resistance and module performance

First and foremost, it's important to reduce the metal line width in order to minimize shading losses without relying on expensive technologies. Metal prevents light from reaching the cell and thus causes a direct loss mechanism. At the same time, our process of choice should minimize resistive losses by increasing metal thickness, should have good adhesion and electrical contact to GaAs, and should not degrade the semiconductor surface.



To the left is a graph showing the dependence of front contact losses on the metal thickness. The detailed numbers depend on exact device and cell designs, but in general, thicker metal is favorable. Electroplating through patterned resist is a process that can deliver narrow line width and thick metal. Prior to plating, Alta utilized a lift-off metallization process, which addresses the narrow line width requirement, but is limited to very small thicknesses.

Because of the limited scalability of lift-off techniques and the high efficiency losses due to the resistance of thin metal lines, we focused our attention on electroplating. Process development included work on several fronts: the plating chemistry itself, the resist choice, and the optimization of expose and develop steps. In Phase I, we demonstrated process feasibility and delivered features below 150 μm in width (deliverable D-1.) In Phase II, Alta's baseline was converted to plating and both patterning and plating steps were optimized to deliver < 100 μm feature sizes (deliverable D-8.) Due to widespread adoption in the PCB industry, plating tools have proven to be scalable at a low cost, thus complying with Alta's primary requirements.

Work is ongoing to maintain process reproducibility of metal pattern geometry and contact resistance. Key metrology steps were introduced in the line to enable process control. For example, contact resistance is measured using Transmission Line Method (TLM) patterns and feature sizes are monitored using an inline profilometer. Moving forward, focus will be on accelerating a path to shading reduction, yield improvement, and process repeatability as we scale to higher volume production.

Via Formation

Contacts to both top and bottom of the solar cells are needed for module interconnect. As described above, the front contact is defined by plated metallization. The back metal, in turn, is covered with a back polymer (plastic) carrier film. Access to the back metal is obtained by carefully removing the plastic materials and forming vias without damaging the metal and solar films.

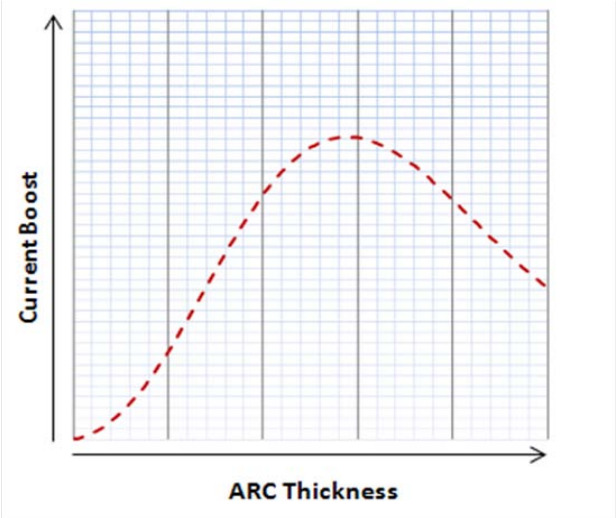
While several methods exist for drilling vias, we focused our attention on the most promising technique from a performance and scalability point of view: laser ablation. Lasers are fast and low cost, and provide a very stable process as a result of the physics of laser ablation. The interaction between laser radiation and a multitude of materials is well-understood, and we take advantage of existing platforms to enable our via formation technology. The process consists of ablating small vias through the polyethylene terephthalate (PET) support film and exposing the back metal, which proved to be a high-yield step, providing clear, precisely defined vias. As a result, well-established laser systems can be used in our manufacturing line.

Alta's via formation process does not cause any measureable degradation to the solar cells. Deliverable D-2 showed that the difference in efficiency for cells with and without back vias is negligible (within the measurement uncertainty.) Detailed characterization showed that the vias are clear and do not add any series resistance due to the interconnect process.

Anti-Reflection Coating

One of the top loss mechanisms in solar cells is light reflection at the surface. Because the short-circuit current is proportional to the light intensity, excessive surface reflection directly impacts solar cell efficiency. The difference in refractive index between the semiconductor surface and glass is the reason for these losses, and thin layers with the appropriate refractive index can be deposited in order to minimize reflection. Alta's anti-reflection coating (ARC) consists of dielectric oxide materials (e.g. TiO_x and SiO_x.)

Our ARC deposition process utilizes an in-house sputter tool which produces high optical quality films. The performance obtained from this process matches our optical models in performance. Altogether, the thickness, refractive index, and number of layers impact the final performance with the main performance indicator being the short-circuit current (Isc.) Measurements of Isc before and after ARC deposition are representative of the amount of light reaching the solar cell junction. The graph on the left shows how current boost (defined as Isc post-ARC minus Isc pre-ARC) depends on the ARC thickness.



The ARC deliverables were structured to show incremental improvements in this process. Deliverable D-3 in Phase I corresponded to >35% current increase due to ARC. Our process delivered 37%. In Phase II, Deliverable D-9 focused on achieving a current boost higher than 37% relative to devices without ARC. With improvements on metrology and process control, our samples showed > 39% current improvements.

Today, our main focus is quality control and fine tuning of performance parameters. Control of the thickness to a few nanometers was obtained through implementation of:

- Ellipsometry measurements that provide high resolution characterization of thickness and refractive index
- Sputter tool control of chamber base pressure, O_2 back pressure, power delivered to the targets, and speed of deposition process. These were implemented to improve run-to-run repeatability
- Reflection measurements to further characterize the optical properties of the deposited thin films

To enable this development, we hired a dedicated sputter engineer as well as an ARC process engineer who were instrumental in achieving the optical performance demonstrated here. Because ARC is a process responsible for such a large portion of our module performance, we will continue to make improvements to the tool and process as we build our first manufacturing line.

Cell Separation

In order to optimize for module output and binning strategy, we partition our solar films to define individual cells. The process by which we separate these films has evolved from mechanical blades to laser beams. Our goal was to develop a process that mitigates reliability failure mechanisms (such as cracks) or performance degradation. As such, we divided Phase I and Phase II deliverable into a mechanical evaluation of the process (deliverable D-4) and electrical performance characterization (deliverable D-10.)

In Phase I we compared a laser separation process with various mechanical processes. In total, we evaluated over five different mechanical processes and found that cracks are ubiquitous. Standard wafer cutting techniques such as dicing and cleaving are not optimal for Alta's films. The laser separation process showed excellent edge quality and provided a manufacturable path forward. The image shown in the Appendix, Phase I is an example of edge quality achieved by laser processes. Utilizing a laser tool, deliverable D-4 was met with samples separated without any visible cracks.

A dedicated laser engineer was hired and local laser application labs were utilized to develop a high performance laser separation process. One additional advantage of laser systems is dynamic alignment through the use of machine vision and the ability to deflect the laser beam using galvo mirrors. Additionally, galvos are known for their high speed, which enables high throughput processes, an important attribute for high-volume solar manufacturing. Today, we run a laser separation baseline and have accumulated data to show the superior performance of laser systems. No measurable degradation is seen with this process, as proved with deliverable D-10.

Matrix and Module

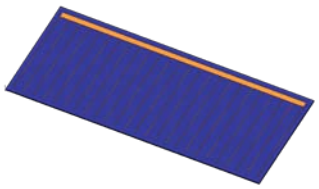
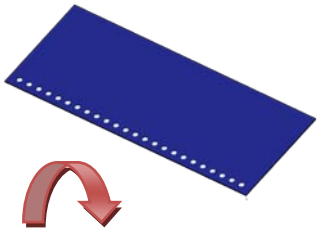
A substantial portion of the PV incubator program was dedicated to matrix and module process development. Several deliverables were defined in phases I and II to address the following topics:

- Cell-to-matrix losses due to interconnect and matrix assembly process (deliverables D-5 and D-11)
- Matrix-to-module losses due to encapsulation process (deliverables D-6 and D-12)
- Improvements on both processes to demonstrate higher efficiency, larger area modules (deliverables D-7, D-13, and D-14)

The work leading up to each deliverable consisted in various cycles of learning, starting with smaller assemblies and evolving to larger area modules in combination with detailed failure analysis and characterization. As part of our interconnect process development, we established calibrated solar simulators capable of handling larger area matrices and modules. The collaboration with NREL's measurement team was instrumental to help us calibrate our own test results. Other characterization methods such as electroluminescence, photoluminescence, and thermal imaging were implemented as well.

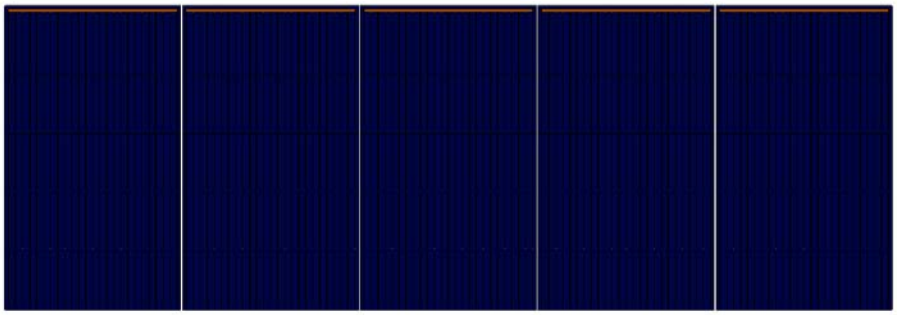
Schematic drawings will follow to describe our shingle matrix assembly approach. The basic idea is to interconnect the top contact of cell 1 to the bottom contact through the back vias in cell 2 using conductive epoxy. A 2-cell series string is depicted below. The assembly process starts with a separated cell which is precisely positioned on the assembly fixture. A second cell gets conductive epoxy dispensed into each of the vias on the back side. The second cell is subsequently placed over the first cell such with good enough alignment such that all vias of cell 2 land on the front metal busbar of cell 1. The process is repeated until a full matrix is built, and copper ribbons are attached to the positive and negative ends for interconnect leads. The final assembly step consists of a

thermal cure to set the epoxy and make it conductive. This cure is a standard process for conductive adhesives.

Cell 1 – Front Metal	Cell 2 – Back vias with ECA	2-cell shingled matrix
		

The matrices can then be transported to a vacuum press laminator where they are sandwiched between glass, encapsulant, and back sheet. Alta's flat plate encapsulation leverages on well-developed materials and process platforms to take full advantage of existing technologies. We use standard low-iron PV glass, standard PV encapsulants and Tedlar back sheets. No special process or material sets are required.

Modules of a variety of sizes and interconnect designs have been produced in this way. As incubator milestones and deliverables, we have built small coupons (2-, 4-, and 8-cell matrices and modules) as well as 0.02 m^2, 0.08 m^2, and 0.125 m^2 modules. We have also demonstrated series strings, series-parallel, and crosstie interconnect schemes. An inherent advantage of our matrix assembly process is the output and geometry flexibility which enables any interconnect design. The number of series and parallel connections can be tuned in to optimize for size, geometry, and power output. Below is a CAD design representing a 5x5 matrix, ribbons not shown (for illustrative purposes only.)



Our goal during the PV incubator program was to demonstrate high efficiency module production with our unique thin-film GaAs solar cells. We progressed from 18%-20% in Phase I to over 22% in Phase II. Though not a direct deliverable for this program, it is worth noting that using the same processes we broke the 1-sun world record by demonstrating 23.5% module efficiency, a result recently confirmed by NREL.

We have optimized specific process steps to enable high efficiency matrix assembly. Cell layout and alignment are done using prototype assembly fixtures and vacuum chucks. Our first generation of tooling has enabled the results in this report. We are developing a

second generation matrix assembly tool which will improve upon the current alignment scheme and will allow for more flexibility in the matrix interconnect design.

To evaluate interconnect performance, we characterized both the voltage and efficiency of matrices and modules and compared them to control samples. In Phase I, we delivered matrices and modules with less than 5% voltage degradation relative to control cells (deliverables D-5 and D-6.) In Phase II, the specification was reduced to < 3% (deliverables D-11 and D-12.) In order to achieve these results, we optimized the assembly process to minimize any damage to the cells. The interconnect materials were carefully selected to minimize series resistance and withstand the encapsulation process. Once optimized with small coupons, we employed the same processes to develop larger area modules (deliverable D-7 in Phase I and deliverables D-13 and D-14 in Phase II.)

During Phase II, we also started aggressively testing our modules for reliability and getting outdoor performance data. So far, the results have been excellent, and we will start engaging with NREL for further performance validation of our technology. In the future, we will focus on further optimizing interconnect and assembly processes to incrementally improve module efficiency.

Final Remarks

The PV technology incubator program has been extremely valuable for Alta as we transition from R&D to Pilot manufacturing. All of the activities associated with our deliverables helped us refine the process steps directed at high efficiency and scalable module production. As a result of how the deliverables were structured, we progressed at a fast rate to put in place all components of a back end production line. We met every deliverable and exceeded expectations by breaking 1-sun module record efficiency for all single-junction PV technologies with our thin-film GaAs solar panel.

As we exit the program, we lay out the foundation necessary to ramp up back end manufacturing equipment and processes. The steps involved in the conversion of Alta's solar film into high efficiency modules were all part of this engagement with NREL and the Department of Energy. NREL was particularly helpful in improving our measurement and characterization techniques. Through specific deliverables, Alta demonstrated both feasibility and high performance for each step in a manufacturing flow that is geared towards high-volume production of thin-film GaAs solar panels.

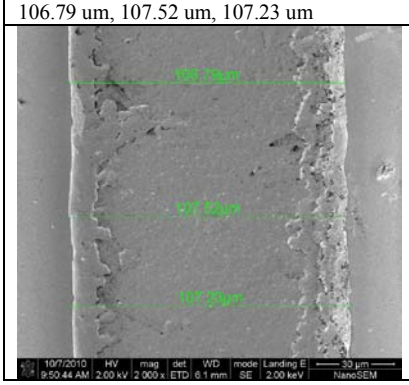
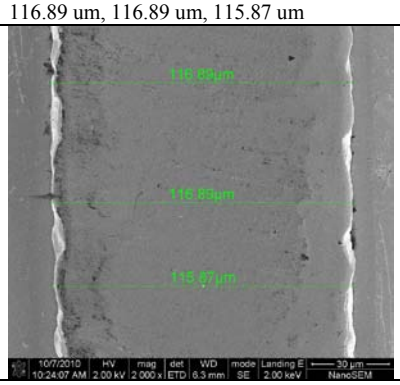
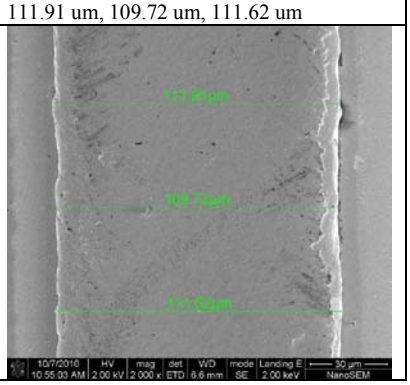
Acknowledgements

We acknowledge support by the Department of Energy, the National Renewable Energy Laboratory, and the contract funding which made this program possible.

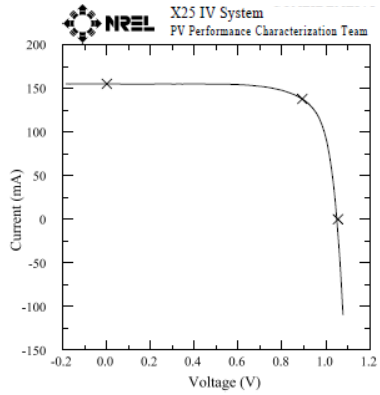
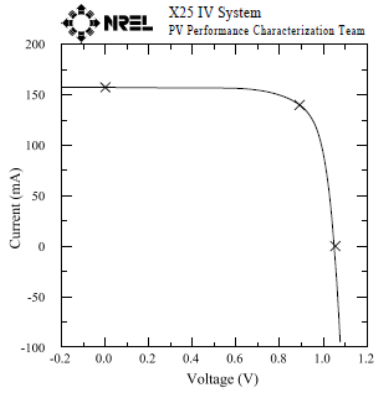
Appendix: Deliverable Results as Measured by NREL

Phase I

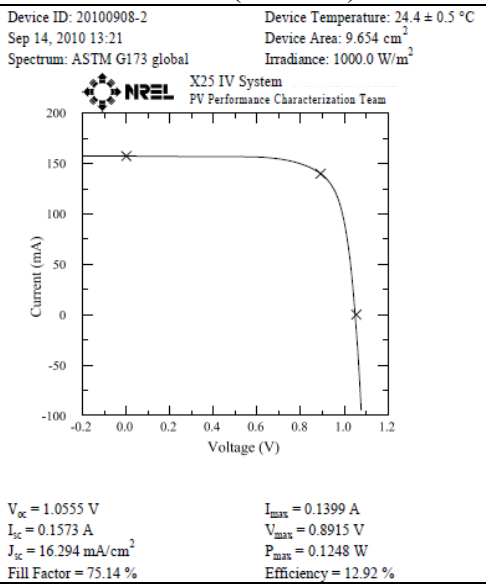
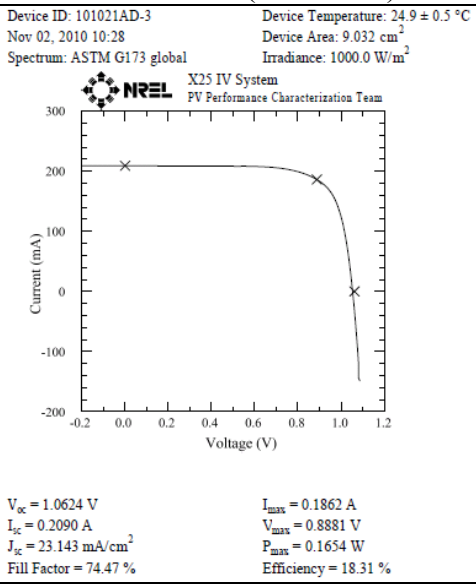
Deliverable D-1: Front metal line width < 150 μm

Labels: 106.79 um, 107.52 um, 107.23 um	Labels: 116.89 um, 116.89 um, 115.87 um	Labels: 111.91 um, 109.72 um, 111.62 um
		

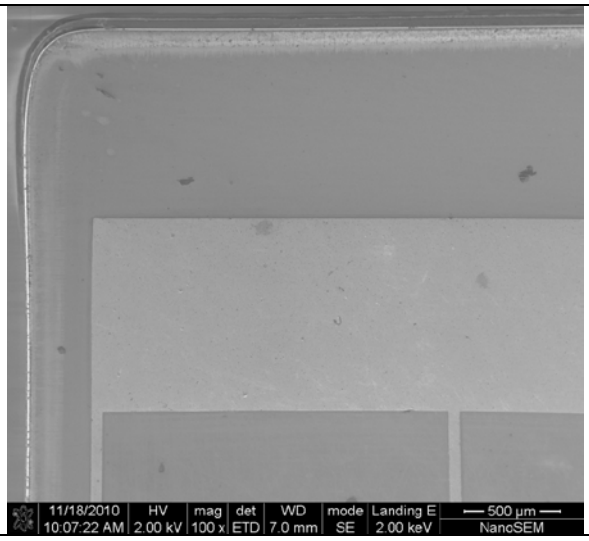
Deliverable D-2: Back via contact with < 5% efficiency loss

Control (no back via)	Deliverable (with back via)
Device ID: 20100908-4 Sep 14, 2010 13:41 Spectrum: ASTM G173 global Device Temperature: 24.6 ± 0.5 °C Device Area: 9.656 cm^2 Irradiance: 1000.0 W/m^2  V_{oc} = 1.0562 V I_{sc} = 0.1553 A J_{sc} = 16.081 mA/cm^2 Fill Factor = 75.12 % I_{max} = 0.1381 A V_{max} = 0.8924 V P_{max} = 0.1232 W Efficiency = 12.76 %	Device ID: 20100908-2 Sep 14, 2010 13:21 Spectrum: ASTM G173 global Device Temperature: 24.4 ± 0.5 °C Device Area: 9.654 cm^2 Irradiance: 1000.0 W/m^2  V_{oc} = 1.0555 V I_{sc} = 0.1573 A J_{sc} = 16.294 mA/cm^2 Fill Factor = 75.14 % I_{max} = 0.1399 A V_{max} = 0.8915 V P_{max} = 0.1248 W Efficiency = 12.92 %

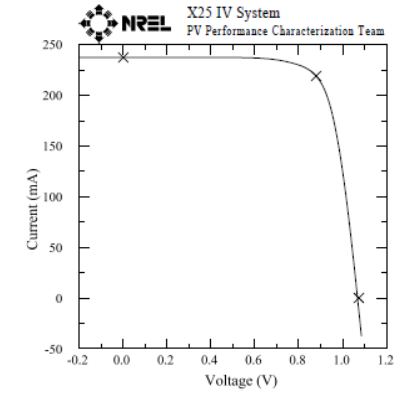
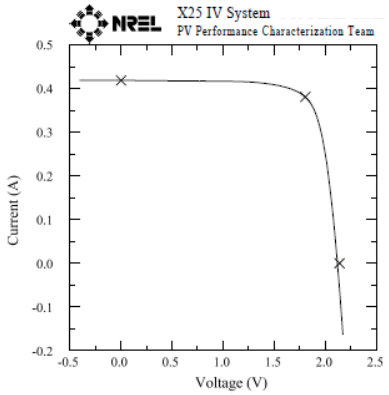
Deliverable D-3: Anti-reflection coating with > 35% current boost

Control (no ARC)	Deliverable (with ARC)
	

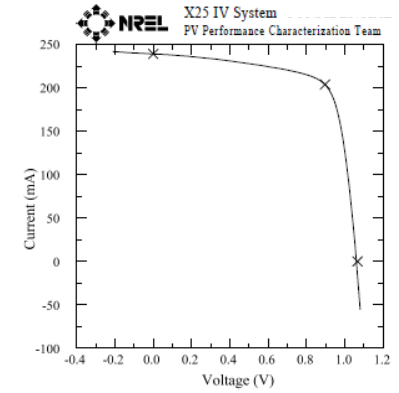
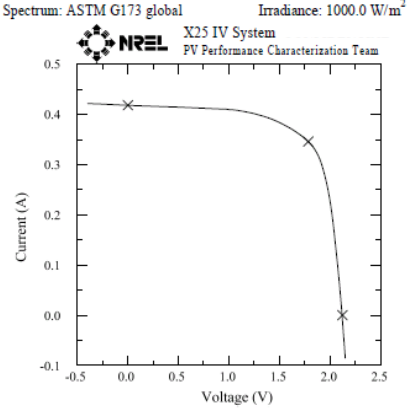
Deliverable D-4: Cell separation with minimal cracks

Deliverable D-4


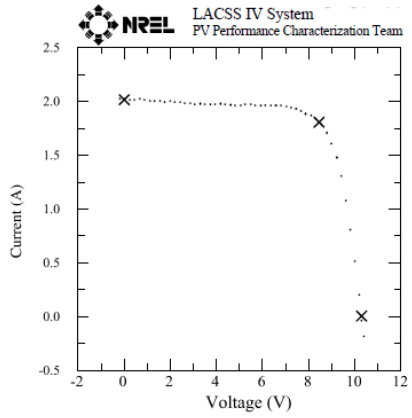
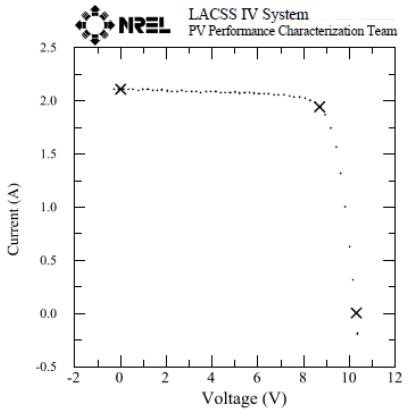
Deliverable D-5: 4-cell matrix with < 5% voltage degradation

Control cell C-5-1	Matrix D-5-1
Device ID: C-5-1 Feb 14, 2011 11:06 Spectrum: ASTM G173 global Device Temperature: 24.6 ± 0.5 °C Device Area: 9.104 cm^2 Irradiance: 1000.0 W/m^2  V_{oc} = 1.0739 V I_{sc} = 0.2374 A J_{sc} = 26.077 mA/cm^2 Fill Factor = 75.60 % I_{max} = 0.2191 A V_{max} = 0.8798 V P_{max} = 0.1928 W Efficiency = 21.17 %	Device ID: D-5-1 Feb 14, 2011 10:55 Spectrum: ASTM G173 global Device Temperature: 24.6 ± 0.5 °C Device Area: 36.14 cm^2 Irradiance: 1000.0 W/m^2  V_{oc} = 2.1411 V I_{sc} = 0.4190 A J_{sc} = 11.593 mA/cm^2 Fill Factor = 76.72 % I_{max} = 0.3812 A V_{max} = 1.8055 V P_{max} = 0.6882 W Efficiency = 19.04 %

Deliverable D-6: 4-cell mini-modules, < 5% Voc losses

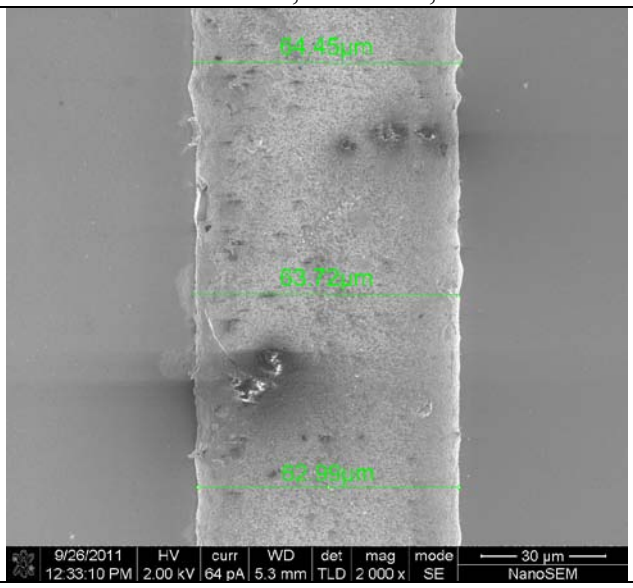
Control cell	Module D-6-1
Device ID: C-6-1 Feb 14, 2011 11:46 Spectrum: ASTM G173 global Device Temperature: 24.6 ± 0.5 °C Device Area: 9.083 cm^2 Irradiance: 1000.0 W/m^2  V_{oc} = 1.0670 V I_{sc} = 0.2391 A J_{sc} = 26.327 mA/cm^2 Fill Factor = 71.74 % I_{max} = 0.2039 A V_{max} = 0.8977 V P_{max} = 0.1831 W Efficiency = 20.15 %	Device ID: D-6-1 Feb 14, 2011 12:37 Spectrum: ASTM G173 global Device Temperature: 24.6 ± 0.5 °C Device Area: 37.07 cm^2 Irradiance: 1000.0 W/m^2  V_{oc} = 2.1241 V I_{sc} = 0.4183 A J_{sc} = 11.284 mA/cm^2 Fill Factor = 69.51 % I_{max} = 0.3458 A V_{max} = 1.7858 V P_{max} = 0.6176 W Efficiency = 16.66 %

Deliverable D-7: Two modules, > 14%, > 0.08 m^2

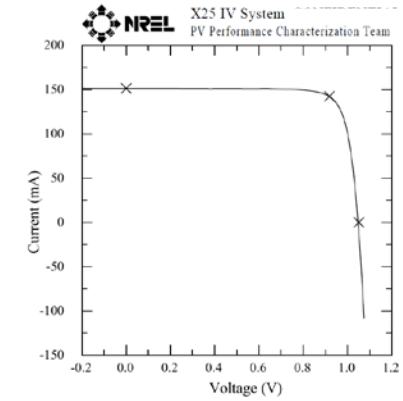
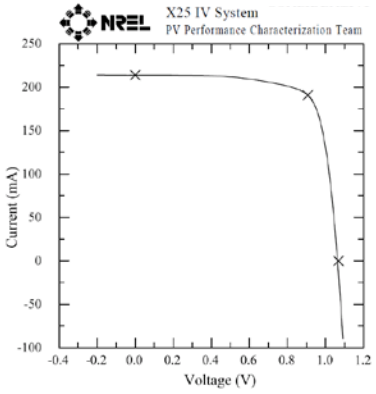
Module D-7-1	Module D-7-2
Device ID: D-7-1 Apr 01, 2011 11:10:45 MT Spectrum: ASTM G173 global Device Temperature = 24.3°C Device Area = 846.7 cm^2 Irradiance = 1000.0 W/m^2  V_{oc} = 10.32 V I_{sc} = 2.015 A Fill Factor = 73.2% Efficiency = 18.0% V_{max} = 8.435 V I_{max} = 1.806 A P_{max} = 15.24 W Device Dimensions = 50.1 x 16.9 cm SETP Deliverable, Taped aperture, Ribbon Leads	Device ID: D-7-2 Apr 01, 2011 11:14:23 MT Spectrum: ASTM G173 global Device Temperature = 24.3°C Device Area = 846.7 cm^2 Irradiance = 1000.0 W/m^2  V_{oc} = 10.30 V I_{sc} = 2.102 A Fill Factor = 78.1% Efficiency = 20.0% V_{max} = 8.701 V I_{max} = 1.943 A P_{max} = 16.90 W Device Dimensions = 50.1 x 16.9 cm SETP Deliverable, Taped aperture, Ribbon Leads

Phase II

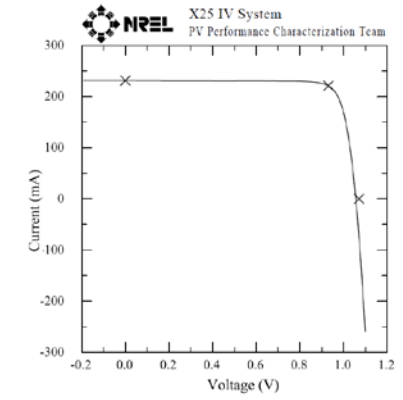
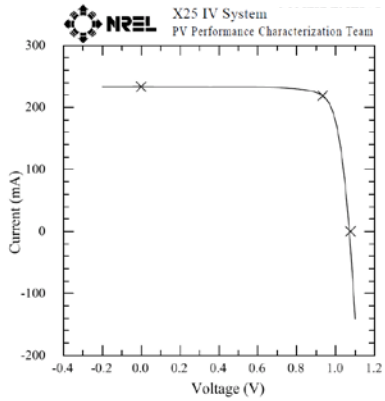
Deliverable D-8: Front metal line width < 100 µm

Deliverable D-8 Labels: 64.45 um, 63.72 um, 62.99 um


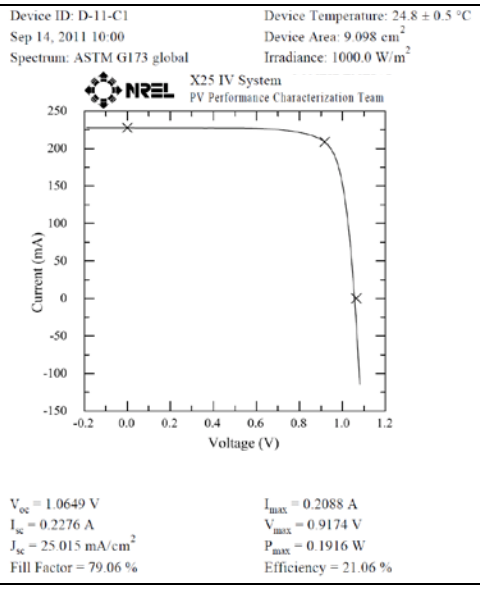
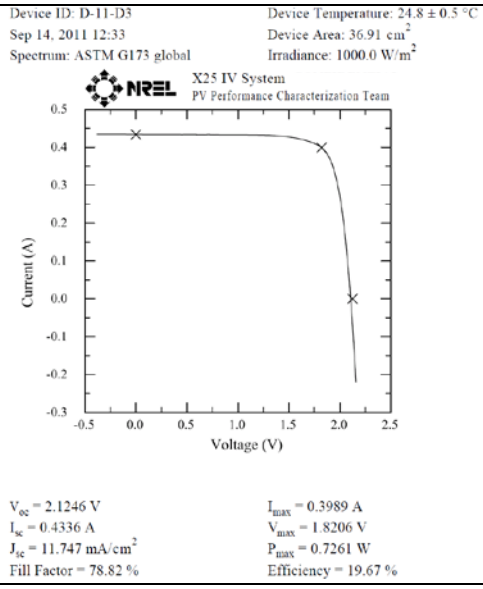
Deliverable D-9: Anti-reflection coating with >37% current boost

Control cell (no ARC)	Deliverable (with ARC)
Device ID: C-9-1 Jul 28, 2011 14:03 Spectrum: ASTM G173 global Device Temperature: 24.9 ± 0.5 °C Device Area: 9.701 cm^2 Irradiance: 1000.0 W/m^2  V_{oc} = 1.0518 V I_{sc} = 0.1512 A J_{sc} = 15.590 mA/cm^2 Fill Factor = 82.12 % I_{max} = 0.1422 A V_{max} = 0.9185 V P_{max} = 0.1306 W Efficiency = 13.47 %	Device ID: D-9-3 Jul 28, 2011 13:30 Spectrum: ASTM G173 global Device Temperature: 24.5 ± 0.5 °C Device Area: 9.957 cm^2 Irradiance: 1000.0 W/m^2  V_{oc} = 1.0678 V I_{sc} = 0.2139 A J_{sc} = 21.481 mA/cm^2 Fill Factor = 75.70 % I_{max} = 0.1907 A V_{max} = 0.9067 V P_{max} = 0.1729 W Efficiency = 17.36 %

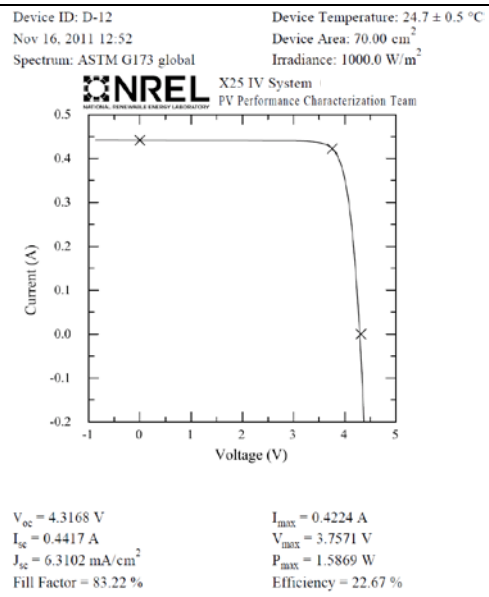
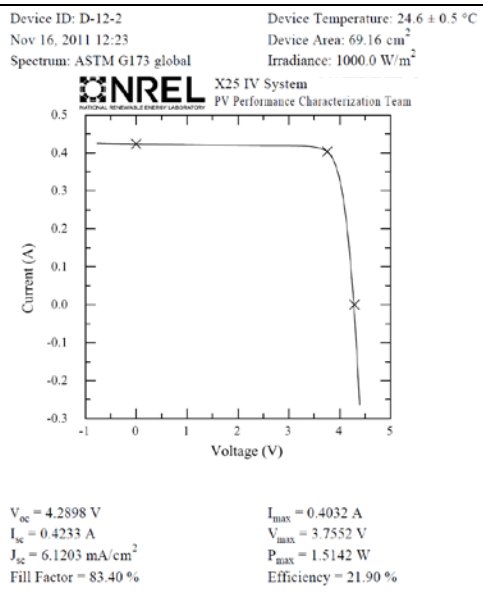
Deliverable D-10: Cell separation with < 5% efficiency loss

Control cell	Deliverable (separated cell)
Device ID: D-10 control cell 1 Aug 02, 2011 11:45 Spectrum: ASTM G173 global Device Temperature: 24.8 ± 0.5 °C Device Area: 9.064 cm^2 Irradiance: 1000.0 W/m^2  V_{oc} = 1.0710 V I_{sc} = 0.2311 A J_{sc} = 25.491 mA/cm^2 Fill Factor = 83.15 % I_{max} = 0.2211 A V_{max} = 0.9307 V P_{max} = 0.2058 W Efficiency = 22.70 %	Device ID: D-10-3 Aug 02, 2011 11:28 Spectrum: ASTM G173 global Device Temperature: 25.0 ± 0.5 °C Device Area: 9.072 cm^2 Irradiance: 1000.0 W/m^2  V_{oc} = 1.0761 V I_{sc} = 0.2334 A J_{sc} = 25.725 mA/cm^2 Fill Factor = 81.35 % I_{max} = 0.2190 A V_{max} = 0.9330 V P_{max} = 0.2043 W Efficiency = 22.52 %

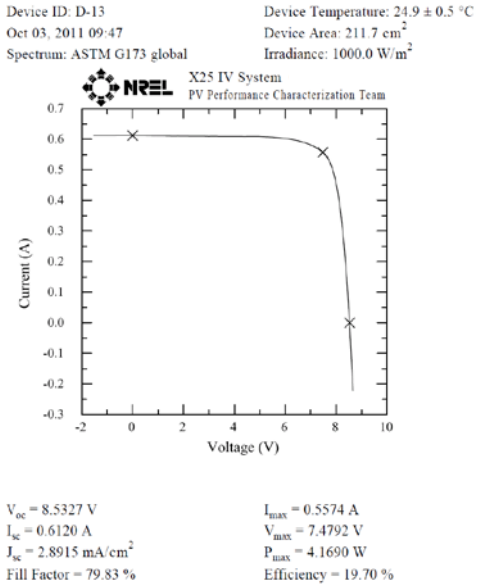
Deliverable D-11: 4-cell matrix with < 3% Voc loss

Control cell	Matrix deliverable
	

Deliverable D-12: 8-cell modules with < 3% Voc degradation

Control matrix D-12	Module D-12-2
	

Deliverable D-13: Sub-modules with area > 0.02 m^2 and efficiency > 16%



Deliverable D-14: Sub-modules with area > 0.125 m^2 and efficiency > 20%

NREL PV Standardized Module Performance Test Report #2K1215

Photovoltaic Cell and Module Measurement Group

Requester: Laila Mattos, Alta Devices — **Prepared By:** Steve Rummel

Date: December 16, 2011

	Area (cm^2)	Temp. (°C)	V_{oc} (V)	I_{sc} (A)	FF (%)	V_{max} (V)	I_{max} (A)	P_{max} (W)	Aper. η (%)
Alta Devices (GaAs submodule)									
MOD114408									
12/12/11 LACSS SpectroLab X200	1288.6	24.5	10.70	3.213	80.1	9.172	3.004	27.55	21.4
12/15/11 SOMS OUTDOORS @987W/m^2	1288.6	11.2	10.77	3.181	81.2	9.294	2.995		
Normalized and Spectrally Corrected SOMS data		11.2		3.284				28.74	22.3
12/12/11 SPIRE 4600SLP Voc to Isc rib leads w	1288.6	25.2	10.80	3.119	81.5	9.374	2.929	27.45	21.3
12/12/11 SPIRE 4600SLP Isc to Voc rib leads w	1288.6	25.2	10.76	3.112	79.7	9.172	2.908	26.67	20.7
Supplied	1295		10.77	3.3	80.66				
MOD114702									
12/12/11 LACSS SpectroLab X200	1285.2	24.4	10.76	3.228	81.0	9.289	3.028	28.13	21.9
12/15/11 SOMS OUTDOORS @993W/m^2	1285.2	15.0	10.77	3.222	81.0	9.282	3.030		
Normalized and Spectrally Corrected SOMS data		15.0		3.311				28.90	22.5
12/12/11 SPIRE 4600SLP Voc to Isc rib leads w	1285.2	25.3	10.84	3.132	81.3	9.358	2.950	27.61	21.5
12/12/11 SPIRE 4600SLP Isc to Voc rib leads w	1285.2	25.2	10.84	3.122	81.6	9.343	2.954	27.60	21.5
Supplied	1295		10.84	3.3	81.7				