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Abstract — Theoretical predictions of thin-film CdS/CdTe photovoltaic (PV) devices have suggested performance may be improved by reducing recombination due to Te-vacancy (V_{Te}) or Te-interstitial (Te_i) defects. Although formation of these intrinsic defects is likely influenced by CdTe deposition parameters, it also may be coupled to formation of beneficial cadmium vacancy (V_{Cd}) defects. If this is true, reducing potential effects of V_{Te} or Te_i may be difficult without also reducing the density of V_{Cd} . In contrast, post-deposition processes can sometimes afford a greater degree of defect control. Here we explore a post-deposition process that appears to influence the Te-related defects in polycrystalline CdTe. Specifically, we have exposed the CdTe surface to Te prior to ZnTe:Cu/Ti contact-interface formation with the goal of reducing V_{Te} but without significantly reducing V_{Cd} . Initial results show that when this modified contact is used on a CdCl₂-treated CdS/CdTe device, significantly poorer device performance results. This suggests two things: First, the amount of free-Te available during contact formation (either from chemical etching or CuTe or ZnTe deposition) may be a more important parameter to device performance than previously appreciated. Second, if processes have been used to reduce the effect of V_{Te} (e.g., oxygen and chlorine additions to the CdTe), adding even a small amount of Te may produce detrimental defects.

Index Terms — CdTe, ZnTe, Contacts, Stoichiometry, Defects

I. INTRODUCTION

Although photovoltaic (PV) devices based on thin-film CdTe have demonstrated performance and reliability sufficient to establish a viable commercial industry, laboratory devices continue to demonstrate lower open-circuit voltage (V_{oc}) and fill factor (FF) than expected for a semiconductor material with a ~ 1.5 -eV bandgap. Further, CdS/CdTe superstrate devices produced using different processes sequences at different locations ultimately demonstrate remarkably similar V_{oc} and FF. This suggests that present CdTe device fabrication processes (all of which involve the use of oxygen, chlorine, and copper — either intentional or unintentional) produce similar material properties that likely result from similar defects. It is further likely that some of these defects are limiting device performance.

Previous studies indicate that much of the performance limitation in present CdS/CdTe devices originates from high recombination in the quasi-neutral region. Because improving collection in this region is critically important to higher device performance (i.e., higher CdTe net-acceptor doping can lead to higher open-circuit voltage — but this will be accompanied by voltage-dependant collection, and thus lower FF),

recombination in this region of the device must be understood and reduced. Although some control of CdTe recombination has been achieved historically through the careful incorporation of oxygen, chlorine, and copper, [1,2] many technologists believe a more promising avenue to improve CdTe PV device performance is to understand and control formation of intrinsic CdTe defects. This is supported by theoretical studies that suggest much of the improvement associated with oxygen, chlorine, and copper is due to their interaction with cadmium and tellurium vacancies (V_{Cd} and V_{Te} , respectively). [3,4]

For CdS/CdTe superstrate devices, we believe most junction-formation processes can be viewed through the following sequence of defect-formation events: The CdTe is deposited from a nominally stoichiometric source where, depending on source pre-conditioning and deposition parameters (primarily substrate temperature), the resulting CdTe film can contain Te or Cd deficiencies (up to ~ 0.01 at.% at thermodynamic equilibrium). This can lead to the formation of various intrinsic defects, including Te and Cd vacancies, interstitials, and/or anti-site defects. Of these, the Te vacancies and interstitials are believed to be more problematic because both may be mid-gap defects, and thus could limit minority-carrier lifetime. [3] Both oxygen (either intentional or unintentional during CdTe deposition) and Cl (from the post-deposition CdCl₂ treatment) may help limit the detrimental effect of V_{Te} through the formation of defect pairs with cadmium vacancies (i.e., $V_{Cd}+O_{Te}$ and $V_{Cd}+Cl_{Te}$). These defect pairs may both reduce the concentration of V_{Te} and provide shallower acceptors than the singly ionized V_{Cd} defects they partly replace, thus making the CdTe layer more p-type at typical operating temperatures. [3]

Following the CdCl₂ treatment, Cu diffusion from a Cu-containing contact further increases the net acceptor concentration (N_A-N_D) by displacing Cd to form Cu_{Cd} acceptor defects. [4] Although this defect is not as shallow as the V_{Cd} or defect pairs discussed above, optimal concentration of Cu_{Cd} will increase N_A-N_D and reduce the junction space-charge width (W_D). It has also been suggested that Cu diffusion greater than the optimal concentration can reduce N_A-N_D through the formation of Cu interstitial donor (Cu_i) defects. [4]

With all these processes in mind, one can see why producing an optimized CdS/CdTe device is a delicate (and often unappreciated) balance between the formation of beneficial and detrimental defects. Specifically, optimum

performance is attained when W_D (controlled by the formation of $V_{Cd+O_{Te}}$, $V_{Cd+C_{Te}}$, and Cu_{Cd}) is narrow enough to produce a drift field in the CdTe absorber that is strong enough to overcome the relatively poor lifetime of the minority-carriers (controlled by the presence or formation of V_{Te} , Te_i , Te_{Cd} , and Cu_i), but still wide enough to limit the effects of voltage-dependent collection (i.e., photocarriers should be generated primarily within the depletion region when the device is biased near the maximum power point [MPP]). [1] To further complicate matters, other studies suggest that for some process conditions, Cu diffusion from the contact reduces both minority-carrier lifetime in the CdTe and doping in the CdS (both effects reducing device performance). However, for other process conditions, Cu diffusion can increase minority-carrier lifetime (thus increasing device performance!). [2]

In contrast to the relatively complicated description above, we believe an alternative pathway to produce CdTe layers with superior material quality may be to control the formation of intrinsic CdTe defects by modifying deposition and/or post-deposition processes. In this study, we report on one post-deposition process in which the CdTe back surface is exposed to a small partial pressure of Te before the application of a ZnTe:Cu/Ti contact. These initial results provide a captivating suggestion that the range of optimum stoichiometry between the formation of V_{Te} (insufficient Te) and Te_i and/or Te_{Cd} (excess Te) may be more narrowly bounded than previously appreciated.

II. EXPERIMENTAL

The superstrate devices used for this study had the structure glass/SnO₂:F/SnO₂/CdS:O/CdTe/ZnTe:Cu/Ti. The glass was 1-mm aluminosilicate; TCO layers were deposited by CVD by reaction of tetramethyltin + oxygen (+ bromotrifluoromethane - if doped); the CdS:O layers were deposited by chemical bath deposition; the CdTe was deposited by close-space sublimation at 600°C; and treated in CdCl₂ vapor at 400°C for 5 min.

The ZnTe:Cu/Ti contact that did not include Te exposure was produced as follows: Samples were placed into a multisource vacuum-processing chamber and preheated for 120 min to a contact-deposition temperature of 340°C. Prior to ZnTe:Cu deposition, approximately 100 nm of material was removed using Ar ion-beam milling with a 3-cm Kaufman-type ion gun operating at a beam energy and current of 500 eV and 6 mA, respectively. ZnTe:Cu layers (2 wt.% Cu) were deposited by radio-frequency (r.f.) sputtering to a thickness of 0.4 μm followed by 0.5 μm of Ti was deposited using direct current (d.c.) magnetron sputtering. The contacted samples were allowed to cool in the vacuum chamber for at least 2 hrs after Ti deposition. For samples that included Te exposure, the CdCl₂-treated back surface was exposed to Te as the sample temperature was raised to 340°C in the same chamber that is used for contacting (i.e., before the ion-beam milling step). At this time the amount of Te added to this surface is uncertain,

but it is believed to be a relatively small — on the order of a few nm if it were allowed to condense into a Te film.

Following the contact formation processes, a pattern of individual 0.25-cm² cells was defined photolithographically on all samples. Cell definition was done by two-step chemical etching, first using TFT Ti Etchant (Transene Co. Inc., Rowley, MA) to remove the Ti, followed by an aqueous solution of 39% FeCl₃ to remove the ZnTe:Cu and CdTe. A perimeter contact onto the SnO₂ layer was formed with soldered indium.

Analysis of the resulting materials and devices included light/dark current voltage (LIV/DIV), capacitance voltage (CV) at 100 kHz, room-temperature spectroscopic photoluminescence (RTPL), low-temperature spectroscopic photoluminescence (LTPL), time-resolved photoluminescence (TRPL), and secondary ion mass spectrometry (SIMS) measurements. RTPL, LTPL, and TRPL measurements are taken from the glass side of the superstrate devices. Additional experimental details are provided in ref. 2.

III. RESULTS

Figure 1 shows a sequence of LIV curves detailing the change in LIV performance of CdS/CdTe devices before and after exposure of the back contact to Te. The figure shows that, immediately before Te exposure, the devices demonstrate a baseline efficiency of ~14% (device 14480 in Fig. 1). This is typical for CdS/CdTe devices made at NREL using the processes described in the Experimental section.

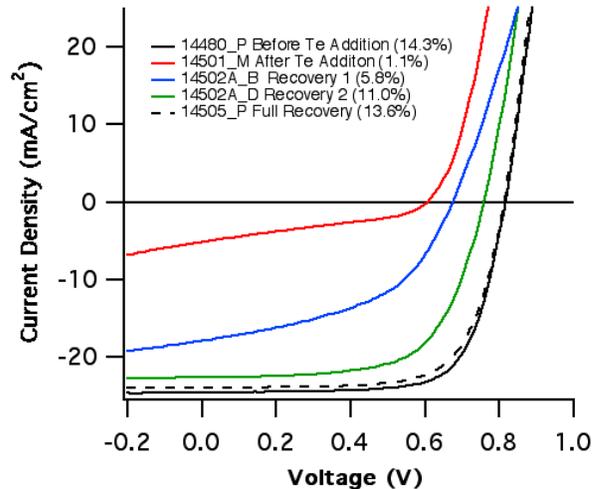


Fig. 1. LIV characteristics of CdS/CdTe devices produced before and after Te exposure prior to the ZnTe:Cu/Ti contacting process.

When the back surface of the devices is exposed to Te, the LIV efficiency drops to ~1% (device 14501 in Fig. 1). Furthermore, after the vacuum system is used for Te exposure, the next several devices contacted in the same vacuum system demonstrate poor performance (see representative devices

14502A_B and 14502A_D in Fig. 1). It is not until ~4–6 additional devices are produced in the vacuum system, and the chamber is cleaned using a thermal treatment, that the ~14% performance baseline is restored (device 14505 in Fig. 1). This trend has been confirmed in several different run sets, three of which are represented in Table 1. At this time, extensive efforts to link this functionality to other process steps (i.e., CdS, CdTe, or CdCl₂) have been unsuccessful.

The LIV performance shown in Fig. 1 is different from that observed previously in CdS/CdTe devices produced with an NREL-ZnTe:Cu/Ti or an NREL-paste contact. Previous studies have indicated that V_{oc} , FF, and short-circuit current (J_{sc}) are reduced when insufficient Cu diffuses from the contact into the CdTe (all manifestations of low N_A-N_D). However, overall performance this low, and related only to the contacting process, has not been previously observed.

Figure 2 shows dark CV profiles of devices following Te exposure. The measurements show the Te exposure causes the space charge to become very wide and relatively insensitive to device bias, suggesting that the resulting net-acceptor density is reduced by Te exposure. As the chamber is used for subsequent depositions, the space charge narrows until the fully recovered devices demonstrate a CV profile consistent with good-quality devices. [1] The analysis suggests that the primary cause of the low J_{sc} shown in Fig. 1 is that Te exposure yields devices with W_D is too wide for the resulting minority-carrier lifetime. However, subsequent vacuum-system use reduces W_D so that the junction field can more effectively assist collection of minority-carriers.

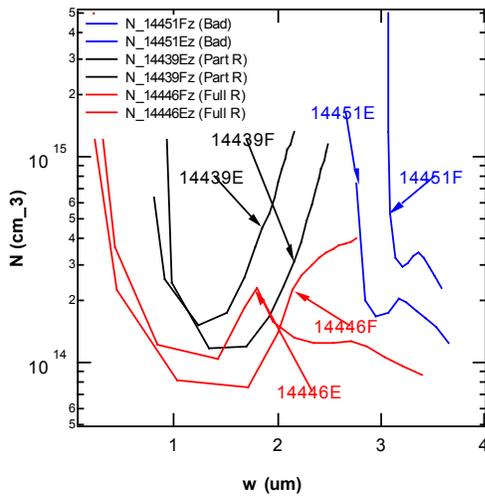


Fig. 2. Dark CV data showing changes in net-acceptor doping profile as a function of number of runs after Te addition to back-contact region.

Figure 3 shows TRPL measurements of devices both after the Te exposure and after subsequent use of the vacuum system. Previous studies of minority-carrier lifetime in CdS/CdTe devices using TRPL measurement have indicated that the TRPL decay rate is biexponential, with a fast (t_1) and

slower (t_2) regime. [5] The data in Fig. 3 show both the bi-exponential trend and that, although both t_1 and t_2 become shorter when Te is added at the back contact, both parameters recover as the vacuum system is used for subsequent depositions. Table 1 lists the values of t_1 and t_2 for several of the sets of samples used in this study. It is worth noting that for all these sample sets, the longest values of t_1 indicated are generally shorter than previously reported for our high-performance devices. [2] This could be an important part of the reason why the J_{sc} s of these devices appear to be sensitive to any reductions in lifetime and/or junction field strength.

Taken together, LIV, CV, and TRPL analysis indicate that the Te exposure yields a device in which both the junction field and carrier lifetime are each reduced to the point that significant voltage-dependant collection dominates the LIV. This means that the minority-carrier lifetime has become so short that collection is highly bias assisted.

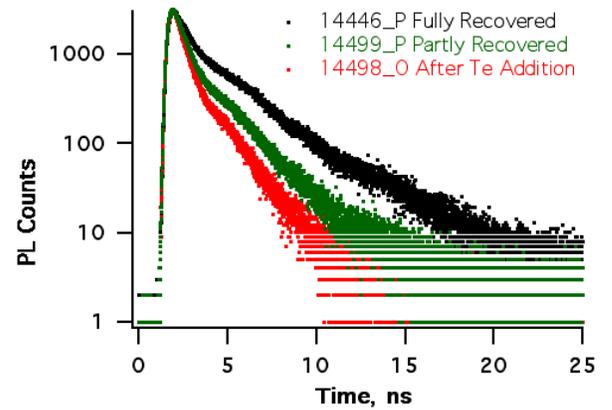


Fig. 3. TRPL data showing changes in radiative recombination before and after adding Te to the contact process.

TABLE I
PL DECAY RATES FOR THREE SETS OF SUPERSTRATE CdS/CdTe DEVICES. RECOVERY PARAMETER IS DEVICE J_{sc} , AND VALUES OF $\sim 2 \text{ MA CM}^{-2}$ ARE TYPICAL FOLLOWING TE ADDITION.

Set	ID	Recovery State	J_{sc} mA cm^{-1}	t_1 (ns)	t_2 (ns)
A	14446 P	Full	>22	0.69	2.96
A	14499 P	Partly	~ 22	0.55	2.14
A	14498 O	None	~ 2	0.50	1.67
B	14505 J	Full	>22	0.53	2.86
B	14503 I	Partly	~ 22	0.48	2.08
B	14501 J	None	~ 2	0.45	1.81
C	14446 L	Full	>22	0.56	4.01
C	14451_P	None	~ 2	0.50	2.00

To probe the cause of the reduction in W_D and carrier lifetime, LTPL was performed on Set B of Table 1. Figure 4 shows that significant changes occur to the low-temperature photoluminescence spectra when the back contact region is

exposed to Te. It is worth noting that, like the TRPL data, the LTPL spectra are taken from the glass side of the device, whereas the Te exposure occurred on the contact side $\sim 3 \mu\text{m}$ from the region being probed by the LTPL.

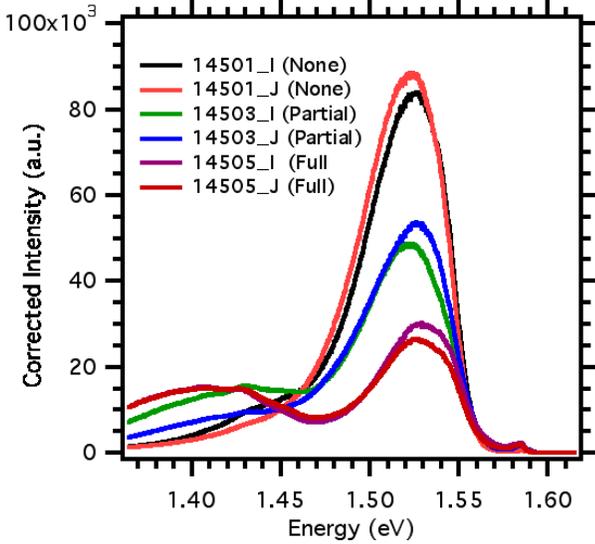


Fig. 4. LTPL spectra of devices from Set B of Table 1 showing the reduction of the peak centered at 1.52 eV and the increase of the peak at ~ 1.4 eV as the device recovers from Te exposure.

The spectra show a peak centered at ~ 1.520 eV that reduces in intensity as the vacuum chamber is used following Te addition, revealing a set of lower-intensity peaks centered at ~ 1.53 eV and ~ 1.54 eV. Because LTPL for these devices is acquired from the glass side of the devices, peaks in this spectral region are likely influenced by luminescence from the $\text{CdS}_x\text{Te}_{1-x}$ alloy region of the device (the effective room-temperature bandgap of these devices is ~ 1.46 eV, suggesting $x \sim 0.1$ in the $\text{CdS}_x\text{Te}_{1-x}$ alloy).

Figure 4 also shows that a broad peak centered at 1.4 eV becomes evident as the chamber is used. Broad peaks in this region have been observed previously with high-performance CdS/CdTe devices contacted with a ZnTe:Cu interface layer, and are believed to be associated with the formation of a defect pair comprised of a copper interstitial and a substitutional O on a Te site ($\text{Cu}_i+\text{O}_{\text{Te}}$). [6] The observation that the peak centered at ~ 1.4 eV is reduced after Te exposure may suggest that the Te exposure is reducing the V_{Te} defect.

Although firm assignments of peaks centered at ~ 1.52 eV– 1.54 eV are not established at this time, Fig. 5 (RTPL) shows that the position of the main peak does not depend greatly on additions of Te at the back contact. Other studies, where Cu concentration within the $\text{CdS}_x\text{Te}_{1-x}$ layer has been systematically controlled, have shown noticeable variation of this peak position. Taken together, the RTPL suggests that Te addition at the back contact does not strongly influence Cu concentration in the $\text{CdS}_x\text{Te}_{1-x}$ layer.

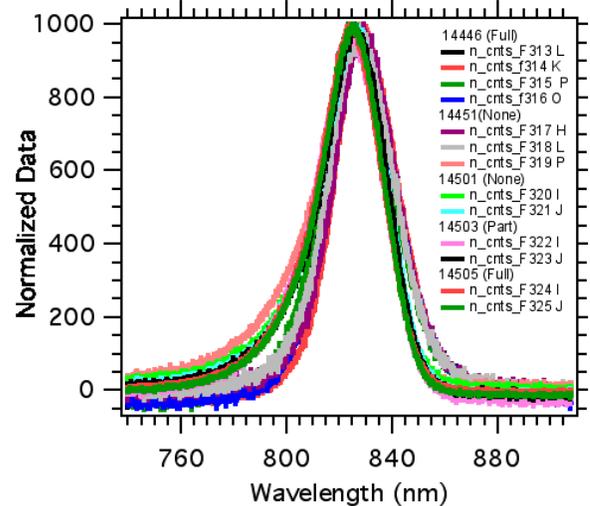


Fig. 5. RTPL spectra of devices from Sets B and C of Table 1 showing that the position of the main luminescent peak does not shift when Te is added at the back contact.

Preliminary SIMS analysis of the devices (Set C of Table 1, SIMS data not presented here) also did not reveal significant differences in Cu concentrations in the CdTe or CdS layers of the two devices. Further, there was not an increase in Cu concentration at the ZnTe:Cu/CdTe interface that might have indicated gettering of Cu by a Te layer or Te inclusions at that interface. Finally, the Te signal at the ZnTe:Cu/CdTe interface was not significantly different between the two samples.

IV. DISCUSSION

Although questions remain regarding the extent that Te exposure of the back contact incorporates Te into the CdTe layer, the combination of LIV, CV, and TRPL analyses forms a reasonably clear explanation of the electrical changes caused by the Te exposure. Device performance decreases primarily because of reduced concentration of net acceptors in the CdTe layer. This causes an expansion of W_D and an associated reduction in the junction electric field. Because minority carriers in polycrystalline CdTe have a relatively short lifetime, reduction in electric field reduces carrier collection. This poor collection is compounded by a reduction in minority-carrier lifetime in the CdTe layer. Indeed, if the minority-carrier lifetime had (instead) increased as the net-acceptor density was reduced, a change in performance may not have resulted.

The observed change in net-acceptor density could be due to one or more of the following possibilities: #1 - The Te exposure reduced Cu diffusion from the ZnTe:Cu into CdTe; #2 - The Te exposure did not reduce Cu diffusion, yet produced a lower concentration of Cu_{Cd} acceptor defects; #3 - The Te exposure did not reduce Cu diffusion or Cu_{Cd} formation, but produced a significant concentration of compensating donor defects in the CdTe. Because both RTPL

and SIMS analyses do not indicate a difference between Cu concentration in the CdTe or CdS layers after Te exposure, or an increase in Cu at the ZnTe:Cu/CdTe interface, it seems that possibility #1 is not supported by the available data. Considering possibility #2, Te can substitute onto a Cd vacancy (Te_{Cd}), thereby eliminating some of the V_{Cd} acceptors (as well as subsequent Cu_{Cd} acceptors) and forming instead mid-gap or deep-donor defects (depending on charge state). [3] This is a likely situation if Cd-poor growth conditions exist. In this case V_{Cd} can form easily, and Te_{Cd} has a relatively low formation energy. [7] Considering possibility #3, in addition to antisite Te_{Cd} defects, Te could also form interstitial defects (Te_i) that are calculated to be deep or mid-gap acceptors (or donors, depending on the particular calculation method). These defects could supply compensating donors and/or, because they are near mid-gap, could reduce minority-carrier lifetime. However, the Te_i defect is expected to have relatively high formation energy of 3.4 eV–3.5 eV. [3] Because the formation of the Te_{Cd} antisite defect (discussed in possibility #2) may be both a compensating donor as well as a path to limit Cu_{Cd} formation, the presence of this defect appears a likely explanation for the observed changes.

Regarding the likely defect changes during Te additions, an additional question remains regarding if/how the Te exposure may be affecting V_{Te} defects that may exist. Density functional theory calculations using the local density approximation indicate the V_{Te} is expected to be a mid-gap defect and therefore a significant recombination center. [3] If Te additions eliminated some of these defects, the recombination rate of the CdTe should be reduced (i.e., minority-carrier lifetime should increase). Because we observed that the recombination rate increases following Te additions, it seems V_{Te} are either not present in significant concentrations, are not highly detrimental for CdTe used to produce these devices, are not affected by the Te additions, or that the possible formation of Te_{Cd} or Te_i defects represent even more effective mid-gap recombination centers. Additionally, the reduction in minority carrier lifetime is not unexpected because, as indicated above, the O and Cl processes are likely to alter the function of the V_{Te} , and processes involving both of these elements were performed prior to the Te additions. Future studies are planned that will investigate Te additions onto devices that were not pre-treated with O or Cl.

Finally, a question might be asked as to why other contacting processes that involve a Te (or Te-rich) layer at the back contact have not shown similar results. Several answers could be considered: One is that the contacting temperatures in these other processes were not high enough to cause sufficient Te diffusion (i.e., the ZnTe:Cu/Ti contact temperature of $\sim 340^\circ\text{C}$ is higher than many other CdTe contact processes). Another possibility is that our Te-treated contact experiences high temperature before Cu is added, and therefore Cu diffusion is not competing for the CuTe formation. Still another possibility is that the high substrate temperature,

combined with the ion-beam processing, interacts to yield a condition more conducive to Te diffusion into the CdTe layer.

V. CONCLUSIONS

We have observed that when the back polycrystalline CdTe surface of a CdS/CdTe thin-film PV device is exposed to a Te vapor prior to application of a ZnTe:Cu/Ti contact, the resulting device performance is much lower than expected. This is primarily due to significant voltage-dependant collection. CV analysis of the devices after Te exposure shows that W_D in the CdTe layer is expanded, while TRPL analysis shows that minority-carrier lifetime is reduced. Indications from SIMS suggest that the Te additions do not significantly change the extent of Cu diffusion from the ZnTe:Cu layer. Also, RTPL suggests that the amount of Cu in the $\text{CdS}_x\text{Te}_{1-x}$ layer does not change significantly. Based on available information, the most likely explanation of the device observations is that the Te exposure leads to the formation of a Te_{Cd} antisite defect.

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