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Process Optimization for High Efficiency Heterojunction c-Si Solar Cells Fabrication Using Hot-Wire Chemical Vapor Deposition

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Abstract — The researchers extensively studied the effects of annealing or thermal history of cell process on the minority carrier lifetimes of FZ n-type c-Si wafers with various i-layer thicknesses from 5 to 60 nm, substrate temperatures from 100 to 350°C, doped layers both p- and n-types, and transparent conducting oxide (TCO). Hot-Wire Chemical Vapor Deposition (HW-CVD) was used to achieve high lifetime, high open circuit voltage (V_{oc}), and high efficiency in crystalline silicon (c-Si) heterojunction (HJ) solar cells. The minority carrier lifetime with i-layer passivation in as-grown state was found to peak at 200°C substrate temperature. Annealing c-Si with as-grown layers affects the lifetime significantly. The optimized annealing temperature is from 250-350°C. It was also found that the lifetime of c-Si wafers with a very thin i/p passivation decreases significantly when annealed at temperatures higher than 250°C. However, the lifetime of the i/p passivated c-Si wafers is not affected by the p-layer even when the i-layer is as thin as 10 nm. Fourier Transform Infrared Spectroscopy (FTIR) was used to understand the annealing effect. For the c-Si wafers with i/n passivation, the minority carrier lifetime is usually longer than 2 ms and slightly improved by annealing. Minority carrier lifetime greater than 1 ms in a double side HJ structure with i/n and i/p layers can be achieved by controlling thermal history of the cell process. HJ cells were fabricated with an efficiency >18% on n-type wafers without texturing, and an efficiency of 19.2% with texturing.

Index Terms — passivation, c-Si, heterojunction a-Si:H, carrier lifetime

INTRODUCTION

Good surface passivation of crystal silicon wafer by using amorphous silicon (a-Si) thin layers is critical to achieving high open circuit voltage (V_{oc}) and high efficiency in heterojunction silicon solar cells [1-2]. Researchers at the National Renewable Energy Laboratory (NREL) found a very long minority carrier lifetime can be obtained by annealing plasma enhanced chemical vapor deposition (PECVD) and intrinsic a-Si:H (i-layer, ~ 50 nm thick) as the passivation layers at low temperatures (100°C ~ 155°C) [3]. However, the passivation quality is usually degraded by annealing at 200°C ~ 250 °C when the boron doped a-Si:H layer (p-

layer) and a thin i-layer were used as the passivation layer for c-Si [4]. Hydrogen effusion was considered to cause the passivation quality degradation of i/p layers [4]. Therefore, it is important to understand the annealing effect of intrinsic and doped a-Si layers in order to obtain good passivation quality by controlling the process temperatures and sequence in the solar cell fabrication process. The annealing effect of a-Si passivation layers deposited by HWCVD is reported in this paper. Minority carrier lifetime >1 ms in a heterojunction structure was achieved by controlling the thermal history of the processes. A heterojunction cell efficiency as high as 19.2% was achieved on N-type textured Czochralski (CZ) wafers.

I. EXPERIMENT

Double side polished (100) N-type FZ wafers 300 μm thick with resistivity of 1 ~ 3 $\Omega\text{-cm}$ were used for the minority carrier lifetime study. The wafers were cleaned by using Piranha solution ($\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2$, 4:1) for 10 minutes or a GEN-4 surface cleaning method (RCA cleaning and aggressive acid etching) [5]. The oxide layer on the wafer surface was removed by a 4% HF solution for 30 seconds before a-Si thin film deposition. The a-Si:H thin films were deposited in an HWCVD system using Ta wires. The intrinsic a-Si:H layers were deposited from SiH_4 gas at different temperatures, while the p-layer and n-layer were deposited from $\text{B}_2\text{H}_6\text{/SiH}_4\text{/H}_2$ and $\text{PH}_3\text{/SiH}_4\text{/H}_2$ gas mixtures at 250°C and 200°C respectively. The a-Si passivated c-Si wafers were then annealed in oven at different temperatures. The minority carrier lifetimes were measured by using a Sinton Consulting WCT-120 system. All reported values were measured at a carrier injection density of $1 \times 10^{15} / \text{cm}^3$ in the generalized mode. The passivated c-Si wafers were characterized using FTIR in transmission mode by subtracting c-Si signal as the background. The polished N-type FZ wafers mentioned above were used for heterojunction cell fabrication. N-type CZ wafers were textured using 3% KOH solution with IPA at 80°C

followed by RCA1 and RCA2 cleaning. Thin i/n and i/p layers were deposited by HWCVD as the base and the emitter of the heterojunction solar cell. Indium tin oxide (ITO) layers were deposited on both base and emitter as anti-reflecting coating using evaporation. Ti/Ag/Pd metal layers were deposited by using e-beam evaporation to form a front-side finger and back-side contact. The cell efficiencies were measured by the NREL XT-10 solar cell characterization system.

II. RESULTS AND DISCUSSION

A 20 nm a-Si:H i-layer was deposited on both sides of the N-type FZ wafers at temperatures ranging from 100°C to 275°C, and annealed at temperatures ranging from 150°C to 400°C for 30 minutes. Fig. 1 below shows that the optimized i-layer deposition temperature is 200°C with a minority carrier lifetime ~ 1.3 ms after annealing at temperatures of 250 ~ 350°C, while a low deposition temperature $<150^\circ\text{C}$ is usually preferred for PECVD [3].

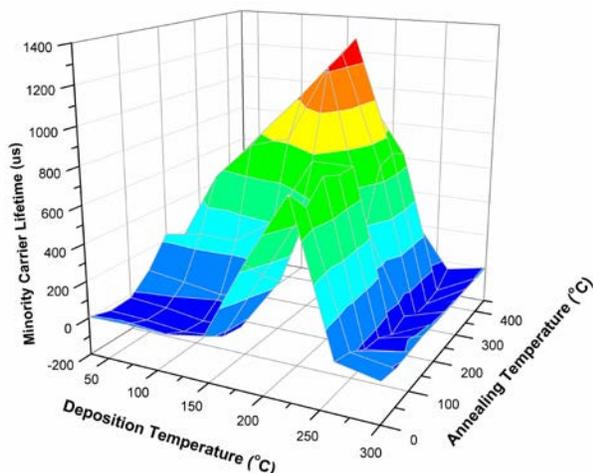


Fig. 1. Minority carrier lifetimes of c-Si wafers passivated with a 20 nm i-layer on both sides as a function of i-layer deposition temperatures and post-deposition annealing temperatures.

Fig. 2 shows little difference between FTIR results before and after annealing, suggesting that i-layer is stable at temperatures up to 300°C.

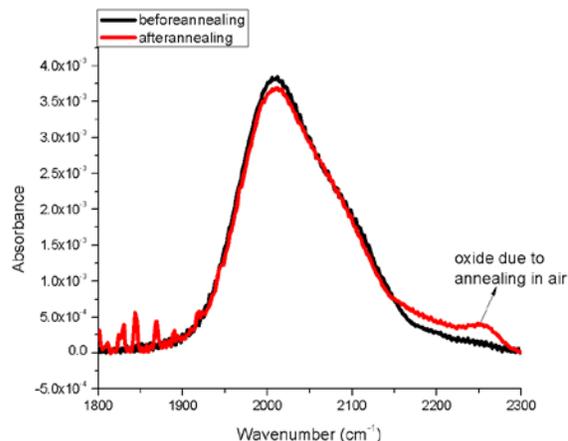


Fig. 2. Absorbance spectra of (100) N-FZ wafers passivated with 20 nm i-layer deposited at 200°C before and annealing at temperatures up to 300°C.

As 20 nm i-layers deposited at 200°C show good passivation quality, another side of the c-Si wafers were replaced by i/p layers with i-layer thicknesses of 0 nm, 3 nm, 5 nm, 10 nm, and 20 nm. These samples were annealed at temperatures of 200°C, 250°C and 300°C for 30 minutes each. Fig. 3 shows that when the i-layer thickness is ≥ 10 nm, the minority carrier lifetime seems unaffected by the above p-layer. When the i-layer thickness is < 10 nm, the minority carrier lifetime drops significantly after annealing at 300°C. The minority carrier lifetime is relatively long (~ 1 ms) after annealing at temperatures $\leq 250^\circ\text{C}$. This suggests that the i-layers deposited at 200°C using HWCVD are possibly more robust and can go through higher processing temperatures, compared to the reported PECVD i-layer [4].

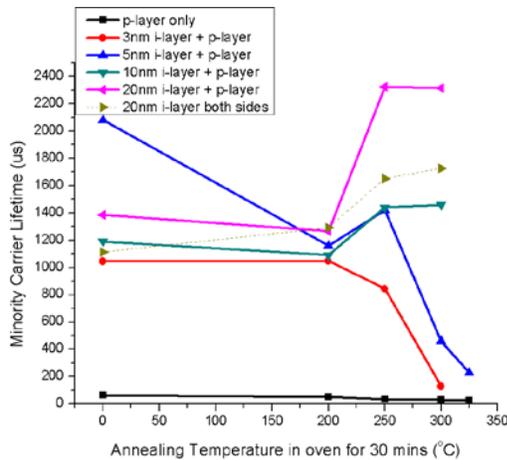


Fig. 3. Minority carrier lifetime of (100) N-FZ wafers with a 20 nm 200°C i-layer on one side and i/p layers on the other side as a function of annealing temperature, compared to a sample with a 20 nm 200°C i-layer on both sides.

FTIR spectra (Figs. 4 and 5) of the sample with 3 nm i-layer and p-layer passivation after annealing at 300°C shows significantly lower absorbance at 2080 cm⁻¹, compared to the spectra of the sample before annealing. This suggests that the minority carrier lifetime degradation of the HWCVD i-p passivation is likely due to hydrogen effusion as well. More specifically, the hydrogen effusion led to lower di-hydride (SiH₂) bonding concentration, but very little change to monohydride (SiH, 2000 cm⁻¹ [1]).

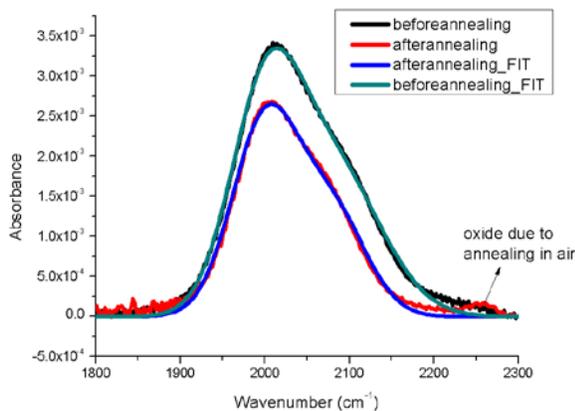


Fig. 4. Absorbance spectra before and after annealing of a (100) N-FZ wafer with a 20 nm i-layer on one side and 3 nm i-layer + p-layer on the other side at 300°C, compared to the curves from peak fitting.

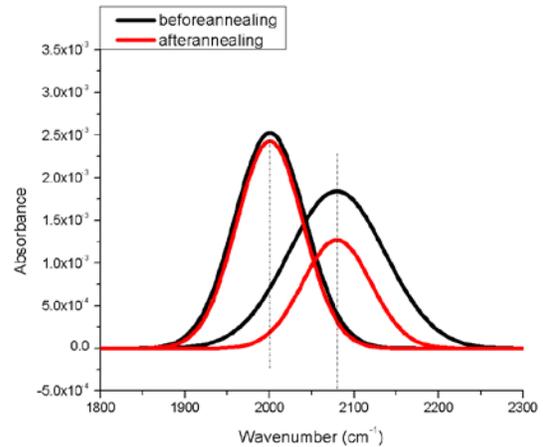


Fig. 5. Curve fitting of the absorbance spectra described in Fig. 4. Peaks at 2000 cm⁻¹ and 2080 cm⁻¹ are correlated to monohydride and di-hydride respectively [1].

It was found that good passivation quality can be obtained with an i-layer as thin as 3 nm for the i/n passivation, as shown in Fig. 6. The sample with i/n passivation shows longer minority carrier lifetime (> 2 ms) than that with a 20 nm i-layer on both sides, most likely due to the help of the electrical field. The sample with n-layer only passivation showed a relatively long minority carrier lifetime ~ 200 μs, compared to that with p-layer passivation but not higher than 1 ms. The n-layer is stable after annealing at temperatures up to 250°C.

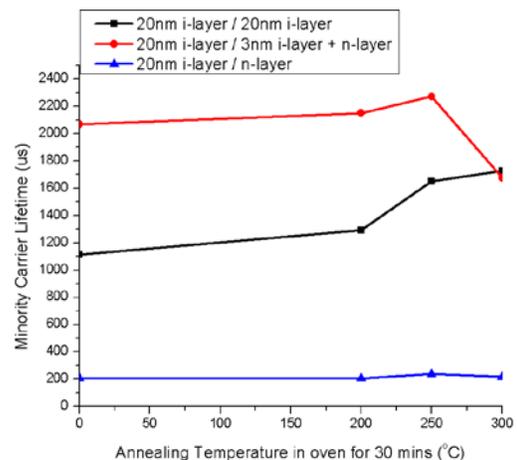


Fig. 6. Minority carrier lifetime of (100) N-FZ wafers with 20 nm 200°C i-layer on one side and n, i/n layer on the other side as a function of annealing temperature, compared to a sample with 20 nm 200°C i-layer on both sides.

By optimizing the HWCVD process and annealing temperatures, heterojunction solar cells have been

fabricated on polished FZ wafers with V_{oc} of 703 mV, J_{sc} of 33.1 mA/cm², FF of 77.4%, and an efficiency of 18.0%. Such cells have also been fabricated with textured CZ wafers with V_{oc} ~ 690 mV and an independently confirmed efficiency of 19.2%, as shown in Fig. 7. We plan to further study the surface cleaning chemistry after KOH texturing, so that higher V_{oc} and efficiency can be achieved.

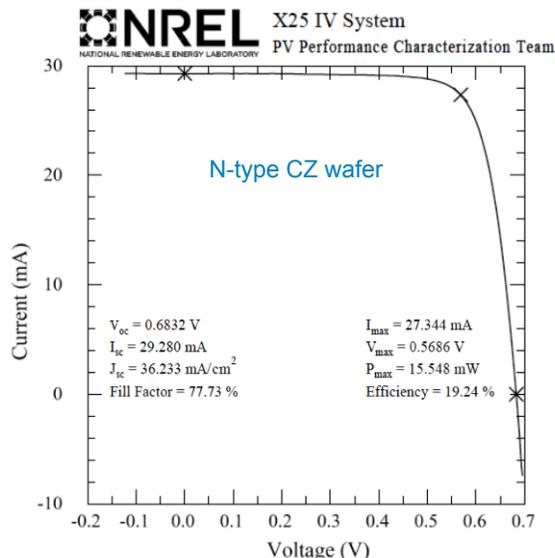


Fig. 7. Independently confirmed J-V characteristics of heterojunction solar cells (1cm×1cm size) on textured CZ wafers by using HWCVD.

III. ACKNOWLEDGEMENT

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V. REFERENCES

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