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NREL Technical Monitor: Harin S. Ullal
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1 Summary

In this program we have been developing a technology for fabricating thin ($< 50 \mu\text{m}$) single crystal silicon wafers on foreign substrates. We reverse the conventional approach of depositing or forming silicon on foreign substrates by depositing or forming thick (200 to 400 μm) ceramic materials on high quality single crystal silicon films $\sim 50 \mu\text{m}$ thick. Our key innovation is the fabrication of thin, refractory, and self-adhering 'handling layers or substrates' on thin epitaxial silicon films in-situ, from powder precursors obtained from low cost raw materials. This 'handling layer' has sufficient strength for device and module processing and fabrication. Successful production of full sized (125 mm X 125 mm) silicon on ceramic wafers with 50 μm thick single crystal silicon has been achieved and device process flow developed for solar cell fabrication. Impurity transfer from the ceramic to the silicon during the elevated temperature consolidation process has resulted in very low minority carrier lifetimes and resulting low cell efficiencies. Detailed analysis of minority carrier lifetime, metals analysis and device characterization have been done. A full sized solar cell efficiency of 8% has been demonstrated.

2 Introduction

2.1 Background

Silicon wafer based photovoltaics dominate the PV industry today with over 80% of all PV products manufactured and deployed today being based on crystalline silicon technology. Notwithstanding the dominant position of this technology, future cost reductions need a dramatic change in the way wafer based PV is manufactured. In particular the materials and capital intensive nature of the manufacturing process need to be addressed with radical technologies.

1. Silicon wafer thicknesses have been reduced over the years but seem to have reached a limit of around 160 to 180 microns based on wire saw technology. In addition kerf loss below about 100 microns does not appear to be feasible due to limitations in wire diameter and wire strength. A major problem with wafers below about 160 microns is the need to develop entirely new concepts for handling and processing thin (especially wafers $< 50 \mu\text{m}$ thick- the minimum thickness for achieving the maximum efficiency) wafers during device and module manufacture. In addition the cost reduction achievable by these approaches is not substantial.
2. A second approach for reducing silicon usage is to deposit or form silicon films on foreign substrates such as glass, metal, ceramic, using CVD or PVD techniques. However these approaches also suffer from major drawbacks: the silicon films are not single crystalline, since no epitaxy is involved, generally being amorphous or micro or multi crystalline; advanced cell processing approaches, such as back and front surface passivation, the formation of effective back side dielectric mirrors, cannot be applied to such structures as the back side (the silicon- foreign substrate interface) is not accessible. These factors preclude achieving high cell efficiencies.

In this program we have been developing a technology which avoids the problems discussed above with thin wafers and silicon on foreign substrates by combining the two concepts in a novel way. We reverse the conventional approach of depositing or forming silicon on foreign substrates by depositing or forming thick (200 to 400 μm) ceramic materials on high quality

single crystal silicon films $\sim 50 \mu\text{m}$ thick. Our key innovation is the fabrication of thin, refractory, and self-adhering ‘handling layers or substrates’ on thin epitaxial silicon films in-situ, from powder precursors obtained from low cost raw materials. This ‘handling layer’ has sufficient strength for device processing, including module fabrication. This approach will:

- Minimize silicon usage by a direct vapor to solid process for thin, single crystal silicon wafer manufacture. This process eliminates the need for polysilicon, crystal growth or ingot casting and the machining and wafering of crystals and ingots (poly free, ingot free, kerf free process). This is a core technology being developed at Crystal Solar. Wafers from this activity are made available to this program.
- Enable handling and processing of thin ($< 50 \mu\text{m}$) large area (currently 125 mm X 125 mm) single crystal wafers by the fabrication of the composite silicon- ceramic wafers.
- Robust wafers that can be handled in processing and packaging by combining thin silicon with strong ceramic substrates.

The major features of our technology include the following:

3. Electrochemically creating thin (< 3 microns) porous silicon layers of the desired microstructure on high quality single crystal silicon wafers.
4. Growing epitaxial films on the porous layers to thicknesses of ~ 50 microns. An in- site p+p junction is created to function as a back surface field in the solar cell by increasing the boron doping level for the last 2 to 4 microns of the epitaxial layer.
5. Following this, a dense and strong ceramic substrate from powder precursors is formed on the rear side (front side of the epitaxial film). The ceramic is formed in a grid pattern to incorporate openings in the ceramic for the back contact for the subsequently fabricated solar cell. The materials, in the form of a paste are dispensed on the wafer followed by elevated temperature consolidation of the ceramic to form a rigid body.
6. Following the formation of the strong ceramic reinforcing grid the epitaxial film with the device structure is exfoliated (removed) at the porous silicon interface and the original silicon substrate reused, multiple times, for subsequent porous layer creation, epitaxial deposition and ceramic formation.
7. The thin epitaxial layer attached to the thicker (up to 400 microns) ceramic film is now easy to handle for solar cell processing (surface cleaning, texture etching, junction formation, surface passivation and silicon nitride ARC layer deposition followed by front and back side metallization) and for interconnecting and packaging of the cells using conventional technology.

3 Task Descriptions, Results, and Discussion

Task 1: Develop ceramic compositions suitable for the in-situ fabrication of handling layer on thin epitaxial silicon wafer to facilitate solar cell processing.

We initially developed and evaluated four candidate materials for the handling layer. These materials are characterized by their ability to sinter from powder in the temperature range of 850 ° to 1000 °C, to reasonably strong (MOR ~10000 psi) ceramic bodies having coefficient of thermal expansion, CTE, matched to that of silicon, and adhering well to oxidized silicon. The MgO-Al₂O₃-SiO₂ glass composition finally selected sinters well from its powder in the temperature range from 825° to 975 °C, concurrently crystallizing to low CTE cordierite glass-ceramic body. We could manipulate the CTE of the glass-ceramic layer in small increments and in a controlled manner, by adding mineral cordierite. This enabled us to fabricate ceramic layers that closely followed the CTE curve for silicon from its firing temperature, as shown in Figure 1. While little or no curvature is desired in the composite wafer, the CTE of ceramic has to remain higher than that of silicon, to avoid putting the silicon in tension. This will create convex curvature towards silicon, depending on the thickness of the ceramic layer. With ~ 200- 300 μm ceramic, the wafer curvatures from 150 to 100 μm, respectively, in our 125 mm wafers, could be obtained with chosen ceramic composition. These wafers became nearly flat after phosphorus diffusion because of the compressive stress generated on the front surface of the epitaxial silicon.

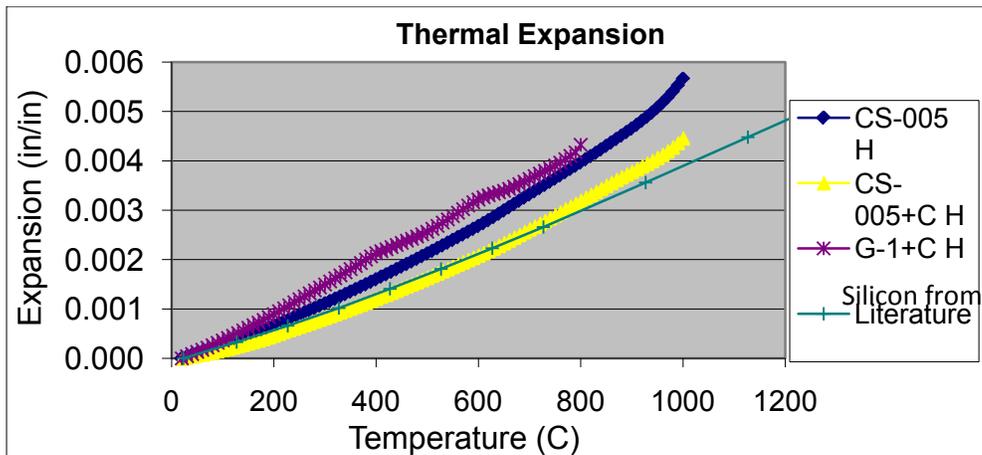


Figure 1. Variation of Coefficient of Thermal Expansion of Three Ceramic Candidates as compared with that of silicon. Credit: Crystal Solar.

Figure 2 shows cross sections of the silicon –ceramic composite wafer showing a continuous, void free interface between the two materials.

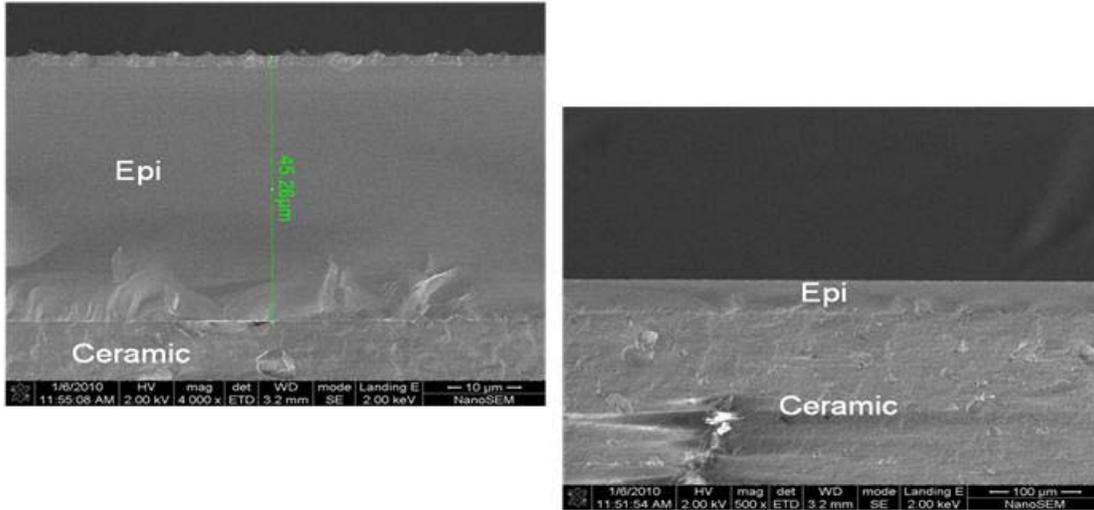


Figure 2: SEM Cross-Section through epi Silicon – Ceramic showing good interface between the two. (Data from NREL)

Modeling of ceramic-epi configuration

The ceramic layer was formed in a grid structure with openings to the wafer surface to allow for forming backside cell contacts. The presence of these openings was of concern for its possible impact on stress and curvature. We modeled a configuration that had 3 mm wide ceramic lines with 1 mm line spacing, with 300 μm thick, in an X and Y grid pattern. The model shows very minimal tensile stress in the ceramic (Figure 3) and, more importantly, a small compressive stress in the silicon attached to it.

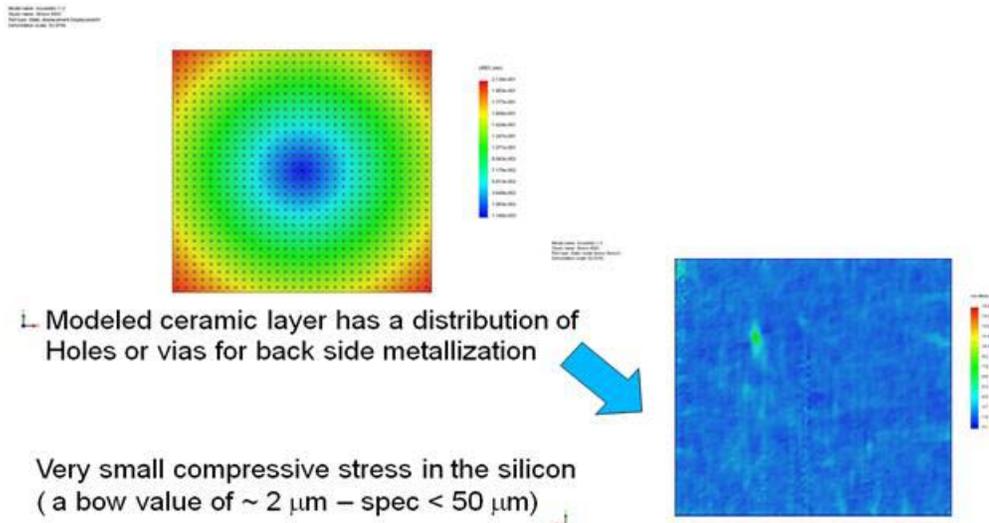


Figure 3. Results of stress model of a ceramic – Si composite wafer with a multiplicity of holes in the ceramic for ohmic contacts to the back side of the solar cell. Credit: Crystal Solar.

The chosen ceramic was found to be compatible with process chemicals and other device processing operations. Although HF attacks the glassy phase on the exposed surfaces of the

ceramic surface, reasonable exposure to HF, Alkali (hot KOH) for texture etching of silicon are safe for the ceramic layer. Thermal compatibility requires re-heating of the Si-ceramic composite wafers to diffusion, and or thick film firing temperatures of ~ 900 C. The thermal shock resistance of the ceramic-silicon composite under RTP conditions was also tested and found to be excellent.

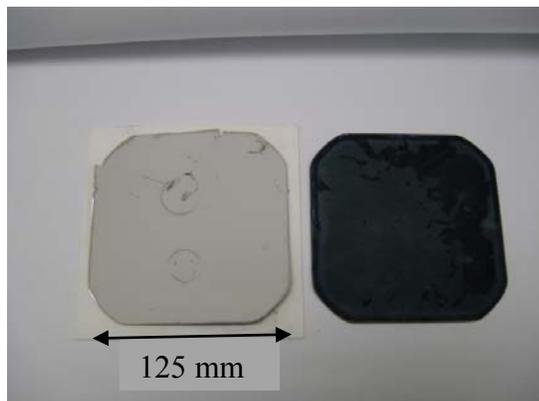


Figure 4. Example of our early attempts at the fabrication of thin silicon on ceramic wafers. On the left is shown the back, ceramic side and on the right is the silicon epitaxy. In this case a blanket ceramic layer was dispensed on to the epitaxial film, consolidated at elevated temperature and the thin epi exfoliated from the substrate. We transitioned into fabricating a ceramic grid structure to enable back contact formation. (Figure 5) Credit: Crystal Solar.

Task 2: Development of optimized application methods for forming ceramic handling layer on the epitaxial surface

Several known techniques for depositing the ceramic precursor were explored. These included stencil printing, green tape attachment, and nozzle dispensing. For these explorations we developed in-house capabilities for making suitable pastes and slurries. Each of these methods had certain advantages and disadvantages. The requirement for making numerous, small, and well distributed openings in the ceramic layer posed the biggest challenge. Nozzle dispensing of the ceramic paste with a programmable ‘robot’ has been able to produce thick (~ 600 μm) paste deposits in a regular X – Y grid pattern, with the openings generated automatically (Figure 5). The non-contact nature of the dispensing method is of particular advantage because of the delicate nature of the epi-silicon surface. It has the ability to independently vary the deposit thickness, the line width and spacing, to produce deposits with a range of openings. We now routinely fabricate full sized, ceramic-grid-supported- epitaxial-silicon wafers, for cell fabrication.

Task 3: Materials Quality

Minority carrier lifetime

An attraction of thin silicon wafers is that the minority carrier lifetime can be relatively low as long as the diffusion length is 2 to 3 times the wafer thickness. So for a 50 micron thick film a diffusion length of ~ 150 microns for 1 Ohm-cm p type epitaxial film would need to have a minimum diffusion length of 5 to 10 micro seconds.

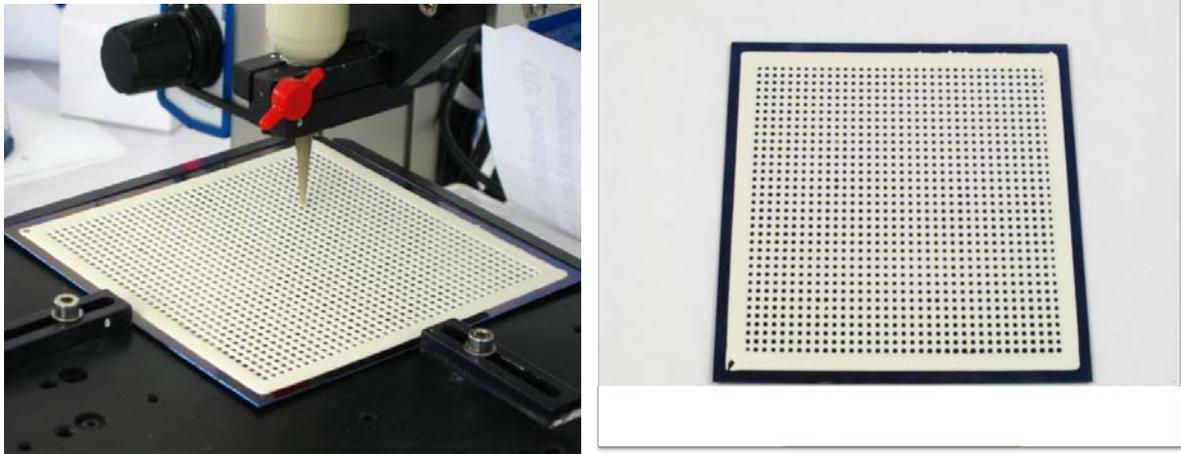


Figure 5. Ceramic dispensing tool (left) with an X-Y translatable nozzle for creating the grid pattern on the pi layer. On the right is shown the ceramic grid on the epitaxial layer after consolidation on a 125 mm X 125 mm wafer. Credit: Crystal Solar.

A substantial aspect of this program has dealt with approaches to preserving the inherently good minority carrier lifetime of the epitaxially deposited films, following ceramic formation and consolidated on these films. Figure 6 shows the minority carrier lifetime of epitaxial films (50 microns thick) after gettering, using a typical phosphorus diffusion step characteristic of junction formation processes for solar cell fabrication. These samples have not been integrated with the ceramic materials. Average lifetime of 50 micron thick wafers fabricated over the course of a year is $\sim 25 \mu$ seconds.

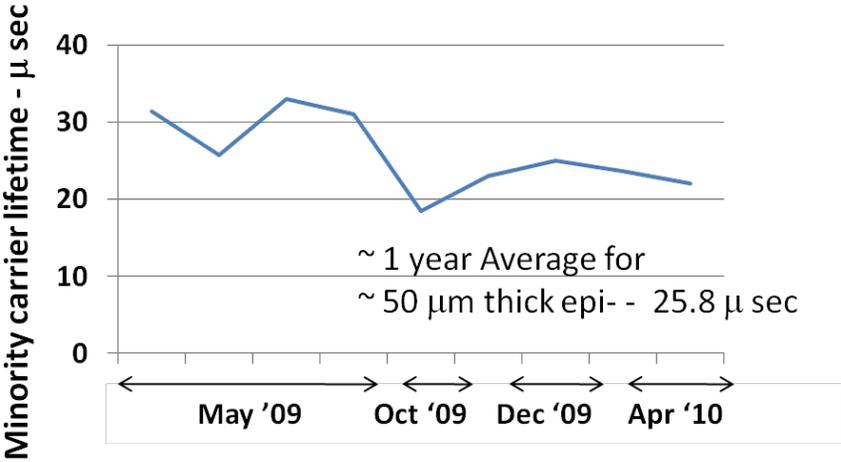


Figure 6. Minority carrier lifetime, as measured by the microwave PCD technique, of gettered thin (50 μm) epitaxial films plotted as a function of time. Average lifetimes of ~ 25 microseconds are realized which translates to a diffusion length over 250 microns- 5 times the wafer thickness. These films have not been subjected to ceramic processing. Credit: Crystal Solar.

In this program a goal was to have lifetime degradation of $< 20\%$ from a baseline of 10μ -secs due to impurities in the ceramic handling layer and the potential diffusion of these impurities into

the silicon. We have used the microwave PCD tool for lifetime mapping of wafers as the primary metrology for establishing the quality, in terms of carrier lifetime, of the silicon-ceramic wafers. Figure 7 shows microwave PCD maps of a 50 micron thick silicon wafer and a silicon on ceramic wafer. Both these sample were subjected to a phosphorus gettering step at 925 C for 60 minutes. Despite gettering the lifetime for the silicon-ceramic wafer is below 1.0 μ -secs while the epi film alone, without being attached to the ceramic, has a minority carrier lifetime of 23 μ -sec. In addition to possible impurity contamination of the silicon from the ceramic, the rear surface, the interface between the silicon and the ceramic is not passivated while the top surface of the silicon is passivated with iodine during lifetime measurement. Consequently carrier recombination at the rear surface and bulk recombination are contributing to the low overall lifetime.

In order to prevent or minimize impurity transfer from the ceramic into the silicon we have evaluated diffusion barriers, such as silicon oxide, and silicon nitride. Table 1 summarizes the data on diffusion barriers.

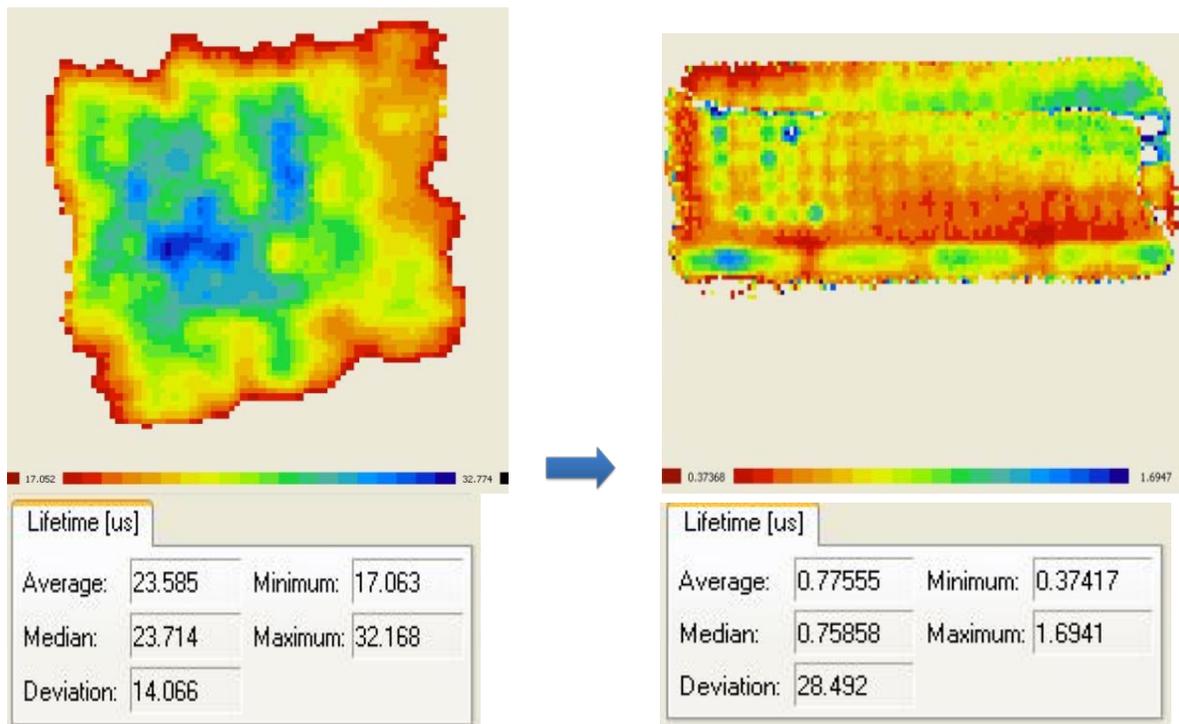
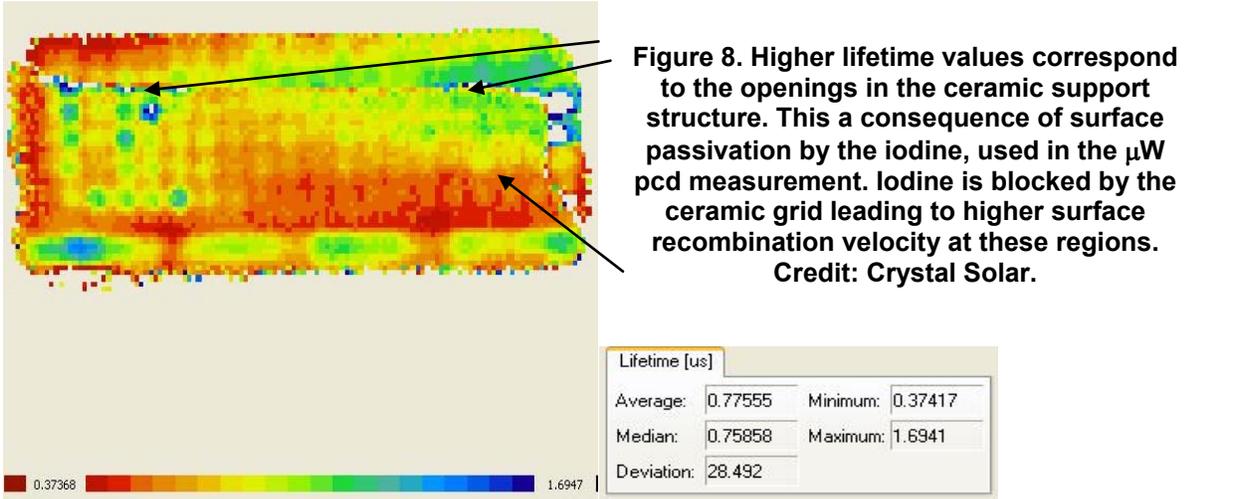


Figure 7. Impurities from the ceramic are transported into the silicon degrading lifetime from a baseline value of ~ 23 μ sec to < 1 μ sec. Credit: Crystal Solar.

Table 1. Impact of Nitride and Oxide diffusion barriers between the epitaxial layer and the ceramic. Although an oxide was found to be better than a low temperature PECVD Nitride film as a diffusion barrier the degradation in lifetime was still not acceptable in terms of meeting the target, indicating that these dielectrics are not good diffusion barriers to heavy metals.

Sample and process	Ave. lifetime	Median	Std. Deviation	Comments
~ 50 μm thick epitaxial film with an ~ 6 μm p+ layer for a BSF followed by phosphorus gettering at 890 C for 30 min. followed by the deposition of a Si3N4 film (70 nm)	6.0 μ sec	6.23 μ sec	20.00%	Represents the bulk lifetime of this epi sample
Above film integrated with ceramic material by forming a ceramic grid on the epi (with a 6 micron BSF and a Si3N4 layer) followed by thermal consolidation	0.63 μ sec	0.63 μ sec	43.60%	Silicon Nitride not a very effective barrier to metal diffusion.
Above film integrated with ceramic material by forming a ceramic grid on the epi (with a 6 micron BSF and 100 nm layer of thermal oxide)) followed by thermal consolidation	4.01 μ sec	3.8 μ sec	27%	Thermal oxide is better diffusion barrier to metallic impurities than than low temperature PECVD Nitride
Above film integrated with ceramic material by forming a ceramic grid on the epi (with a 6 micron BSF and a Si3N4 layer) followed by thermal consolidation. Sample gettered at higher temperature of 925 C for 60 minutes	4.65 μ sec	4.73 μ sec	41.40%	Higher temperature gettering improves lifetime slightly. Higher temperature may also densify PECVD nitride and improve its ability to function as a diffusion barrier

Thicker (1 μm) oxide films as well as composite oxide-nitride films have been tested as diffusion barriers with no improvement. We also find a distribution of lifetime in the silicon that corresponds to the ceramic grid pattern an example of which is shown in Figure 8.



Metals analysis

The substantial reduction in lifetime of the epitaxial films following the ceramic dispensing and consolidation process can be attributed to metals contamination of the silicon, although there is some indication that stress in the silicon can contribute to lifetime reduction (1). The silicon in

the composite material is kept in compression by manipulating the CTEs of the two materials. However our major thrust has been in understanding impurity effects as this is the most likely cause of lifetime degradation. Metallic impurities, particularly iron and titanium occur in amounts of 0.5% by weight in the ceramic materials.

We have attempted to analyze the silicon wafers, after ceramic formation and consolidation for heavy metals with mixed results.

ICPMS Analyses of Epi-silicon attached to ceramic

We carried out Laser - ICPMS analysis of the epitaxial silicon, a technique that permitted analysis of the silicon while still attached to the ceramic grid structure. This technique showed no contamination in the epi-silicon. The detection limits for the impurities of interest was 0.05 ppm or 50 ppb. To improve on the detection limit of Laser ICPMS, a sample of the same wafer was prepared for ICPMS by total solution method, by dissolving away the ceramic grid over 3 days in concentrated HF acid. This analysis again showed no impurities attributable to the ceramic. However, two anomalies showed up in this sample, copper at 94 ppb, and silver at 119 ppb. These impurities were far above the detection limits for these elements in the ‘Laser ICPMS’ of 20 ppb and 2 ppb, respectively. Also, silver is an unlikely impurity in the ceramic. We attribute its presence in the latter analysis, and by association that of copper, to adventitious impurities entering the large, open dish we used during 3 days of glass dissolution. Figure 9 shows the results of these two analyses superimposed.

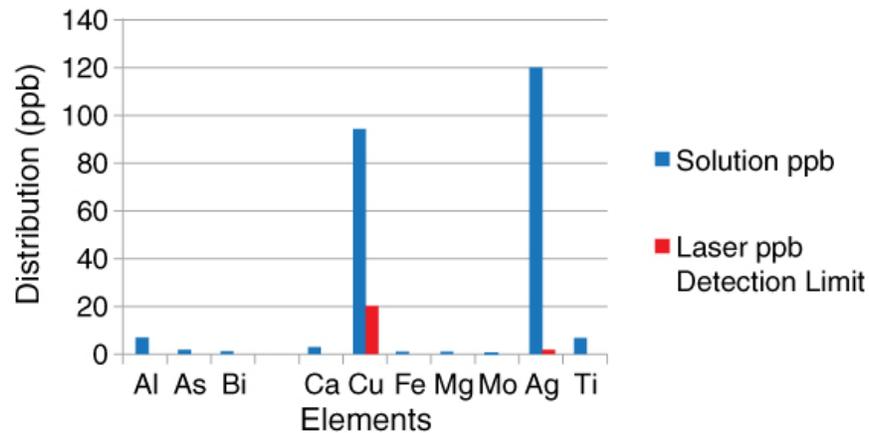


Figure 9. Solution and Laser based ICPMS of a silicon on ceramic wafer showing very low levels of metals and spurious amounts of Copper and Silver. Credit: Crystal Solar.

Iron detection by μW -pcd

A very elegant technique for detecting Iron in silicon is the use of the μW pcd technique. The process is as follows:

1. Obtain the lifetime map of the sample using a μW - pcd tool (before)
2. Dissociate Fe-B pairs by high intensity illumination of the sample (flash lamp of 3000W).
3. Obtain lifetime map after illumination (after).
4. Calculate the iron concentration using the relation:

$$N_{\text{Fe}} = C \left(\frac{1}{\tau_{\text{before}}} - \frac{1}{\tau_{\text{after}}} \right)$$

$$C = 3.4 \cdot 10^{13} \text{ } \mu\text{s/cm}^3$$

This procedure works well when the measured lifetime is dominated by bulk recombination and the surface recombination is negligible.

Figure 10 shows data using this technique indicating an iron concentration of $1.5 \text{ E}13/\text{cm}^3$ in the silicon on ceramic sample. With this technique we find iron concentration to be about two orders of magnitude higher than in typical, good quality, Czochralski wafers.

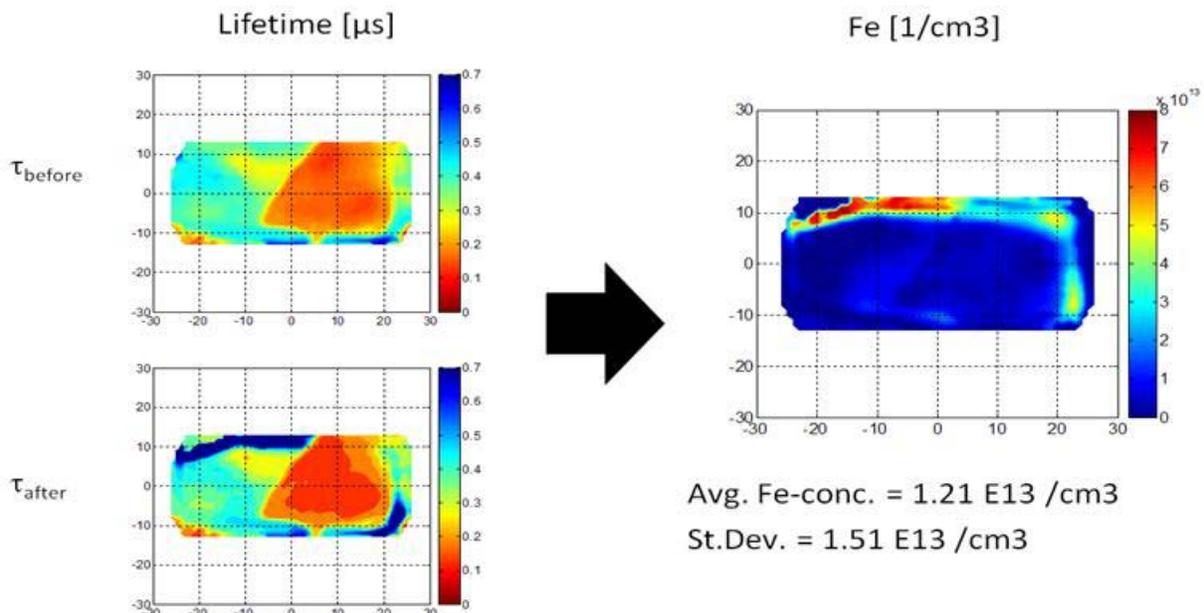


Figure 10. Microwave pcd technique in combination with light induced dissociation of Iron – Boron pairs for Iron detection. Credit: Crystal Solar.

The conflicting metals data with different analytical techniques can be attributed to process variations in the fabrication process with different samples being contaminated to different degrees. In order to unambiguously establish the impurity content and type in the silicon on ceramic wafers a much larger and statistically meaningful data set is required. Since the governing factors are minority carrier lifetime and solar cell I-V data we have concentrated our efforts on these parameters.

Task 4: Device fabrication and testing

The basic process flow for solar cell fabrication we have developed with the silicon on ceramic structure is shown schematically in Figure 11. We have processed the ceramic-epi composites into silicon solar cells, based on front junction architecture (n+/p/p+). Device details include:

- (1) Production of 50 micron thick, p-type, epitaxial films on porous silicon with ~ 1 ohm-cm bulk resistivity with a 2 to 5 μ m thick heavily boron doped layer on the surface to function as a p+p back surface field
- (2) Oxidizing or depositing a silicon nitride layer by PECVD on the epitaxial film. [These films were originally expected to perform three functions- diffusion barriers for metallic impurities from the ceramic, as rear surface passivation and as a means of blocking phosphorus diffusion at the back during the subsequent emitter formation step. However the oxide (or nitride) is found to only function as a barrier to phosphorus diffusion and not as a barrier to fast diffusers (Table 1) and the potential passivation effects of the dielectrics are destroyed by the high temperature associated with ceramic consolidation and impurity diffusion from the ceramic.]
- (3) Integrating the candidate ceramic layer on the wafer with appropriate openings in the ceramic for ohmic contacts
- (4) Consolidating the ceramic material at a temperature of ~ 1000 C to densify it to form a rigid handle material.
- (4) Exfoliate the thin epitaxial layer with the attached ceramic to form a free standing wafer with 50 micron silicon on a ceramic handle.
- (5) Front side device processing with texture etch, phosphorus diffusion, ARC layer deposition and TiPdAg grid by lift-off process.
- (6) Formation of back side contacts by evaporating/sputtering aluminum/ nickel vanadium.

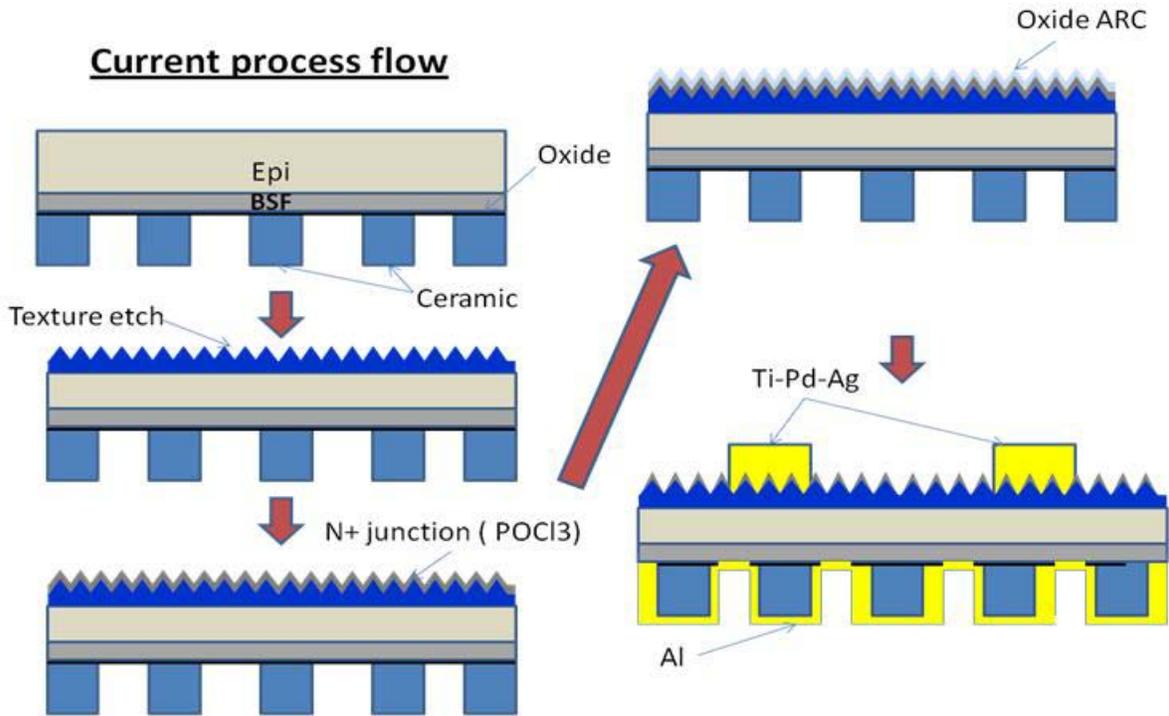


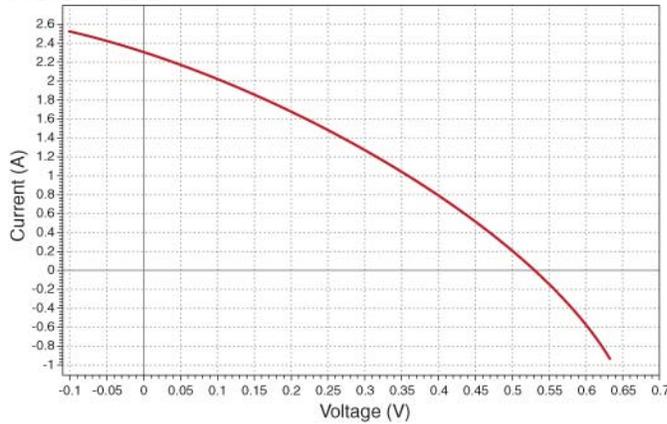
Figure 11. Basic fabrication sequence for silicon on ceramic wafers. Credit: Crystal Solar.

The process flow is shown in detail in Figure 12.

Incoming Silicon – 125mm perfect square 725um
SC-1 Clean – 75C, 15m
Anodically etch silicon
Epitaxy (50um with 4-6 um in-situ grown p+ BSF)
1000A Thermal oxidation – Diffusion barrier
Dispense Ceramic slurry on epi top surface in cross-grid lattice pattern + sinter
Exfoliate epi
Dilute HF/KOH + 2% TMAH/3% IPA/DI @ 75C, 30m Texture
Junction formation (POCl3) – 40-50 ohm/sq, followed by PSG removal (BOE dip)
Pre oxidation clean + 1000A Thermal oxide (passivation and ARC)
Spin photo resist and bake
Lithographically pattern oxide for front grid
Evaporate Ti-Pd-Ag (200A/500A/2um)
Resist/metal lift off
Deposit blanket Al (with Ni-V flash) on the back-side (ceramic side)
Cell test # 1 after back side metallization
Forming Gas anneal (275C, 15m)
Cell test # 2 after forming gas anneal

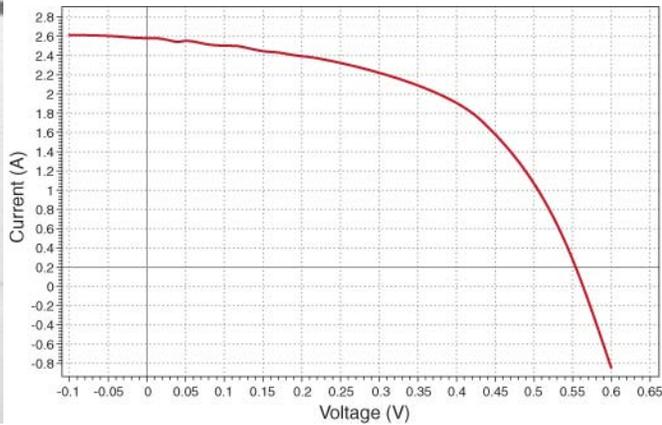
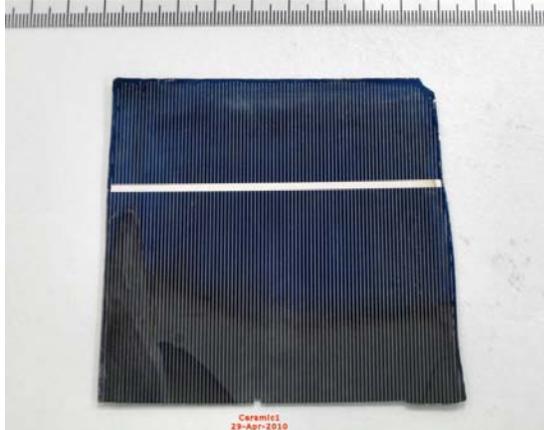
Figure 12. Device process flow for solar cell fabrication using 50 micron thick silicon on ceramic wafers. Credit: Crystal Solar.

Solar Cell Data



Area (cm ²)	117
Isc (mA)	2296
Jsc (mA/cm ²)	19.62
Voc (mV)	528.2
Fill factor (%)	30.9
Efficiency (%)	3.2

As fabricated



Area (cm ²)	103
Isc (mA)	2573
Jsc (mA/cm ²)	24.98
Voc (mV)	561.9
Fill factor (%)	52.5
Efficiency (%)	7.37
R-series (ohm)	0.048
R-shunt (ohm)	2.65

Figure 13. I-V characteristics of 50 micron thick device on ceramic substrate, before and after forming gas anneal. Photograph shows the first device (~ 100 sq.cm.) fabricated with the novel Si on Ceramic wafers. Credit: Crystal Solar.

Annealed in Forming Gas

Solar cell data from early in the program is shown in Figure 13. We see a substantial impact of annealing the device, at 275 C for 15 minutes, in forming gas after device fabrication. We attribute this to improved ohmic contact at the rear side of the device, between the aluminum and the silicon. We find a direct correlation between the conversion efficiency and the Rs (the series resistance) as shown in Figure 14.

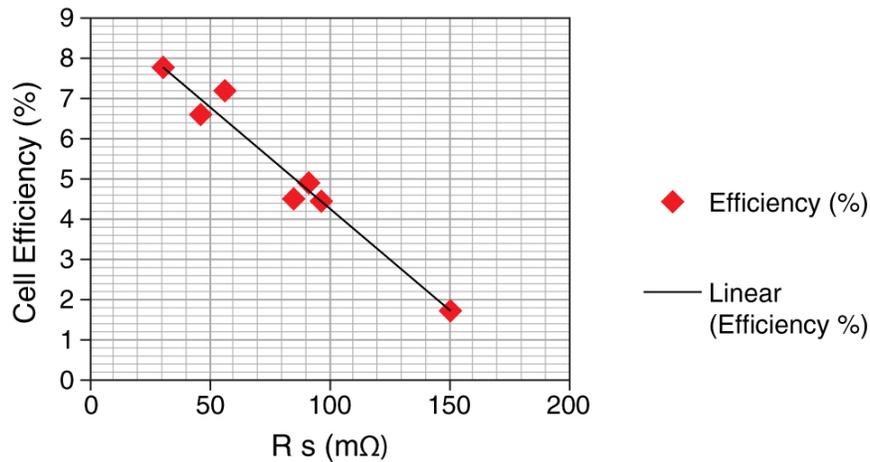


Figure 14. Conversion Efficiency Vs Rs in Early Epitaxial Silicon on Ceramic solar cells

We have been using PC-1D simulations to guide the process development efforts in cell fabrication. In the chart in Table 2 we compare the measured cell efficiency of 7.37 % and the associated cell parameters with predictions from PC1D simulations.

Table 2. Comparison of measured data and PC1D simulation

	Parameter	Ceramic cell - April 2010	Improve lifetime
Process Details	Emitter sheet res	40-50 ohm/sq	
	Passivation/ARC	1000A thermal oxide	
	Refractive Index	1.5	
	Reflectivity after ARC	2%-15%	
	Front-side metallization details	200A Ti/500A Pd/2 um Ag followed by lift-off	
Measured I-V Data	Jsc (mA/cm2)	24.98	
	Voc (mV)	561.9	
	Fill Factor (%)	52.5	
	Efficiency (%)	7.37	
	R-shunt (ohm-cm2)	273	
	R-series (ohm-cm2)	4.93	
PC-1D Simulation Parameters	Epi Thickness (um)	45	45
	Front texture depth (um)	10	10
	Exterior Front Reflectance (%)	14	14
	Internal Rear Reflectance (%)	0	0
	Junction Depth (um)	1.25	1.25
	p+ BSF Thickness (um)	6	6
	Bulk lifetime (usec)	0.8	5
	Front SRV (cm/s)	700000 (7.0e5)	700000 (7.0e5)
	Rear SRV (cm/s)	1e7	1e7
	1/R-shunt (Siemens)	0.38	0.38
	R-series (ohm)	4.8E-02	4.8E-02
PC-1D Simulation Results	Jsc (mA/cm2)	24.15	25.35
	Voc (mV)	590.5	610.1
	Fill Factor (%)	61.6	61.9
	Efficiency (%)	8.78	9.57

PC1D predicts an efficiency of 8.8% when the various device and material parameters are entered into the model. The short circuit current values are fairly well predicted. However the Voc and the fill factors predicted by the model are higher than measured values, indicating issues with junction quality, contact resistance and possible shunting effects. We achieve efficiencies of 7.37% (8.78 % as predicted by the model) for lifetime values of < 1 μ -sec. Clearly higher lifetime will increase the efficiency as indicted in the simulation where a 5 microsecond lifetime predicts efficiencies near 10%.

A device with close to 8% efficiency was fabricated by improving the back contact resulting from better pre metal cleaning. The I-V curve and the spectral response are shown in Figure 15.

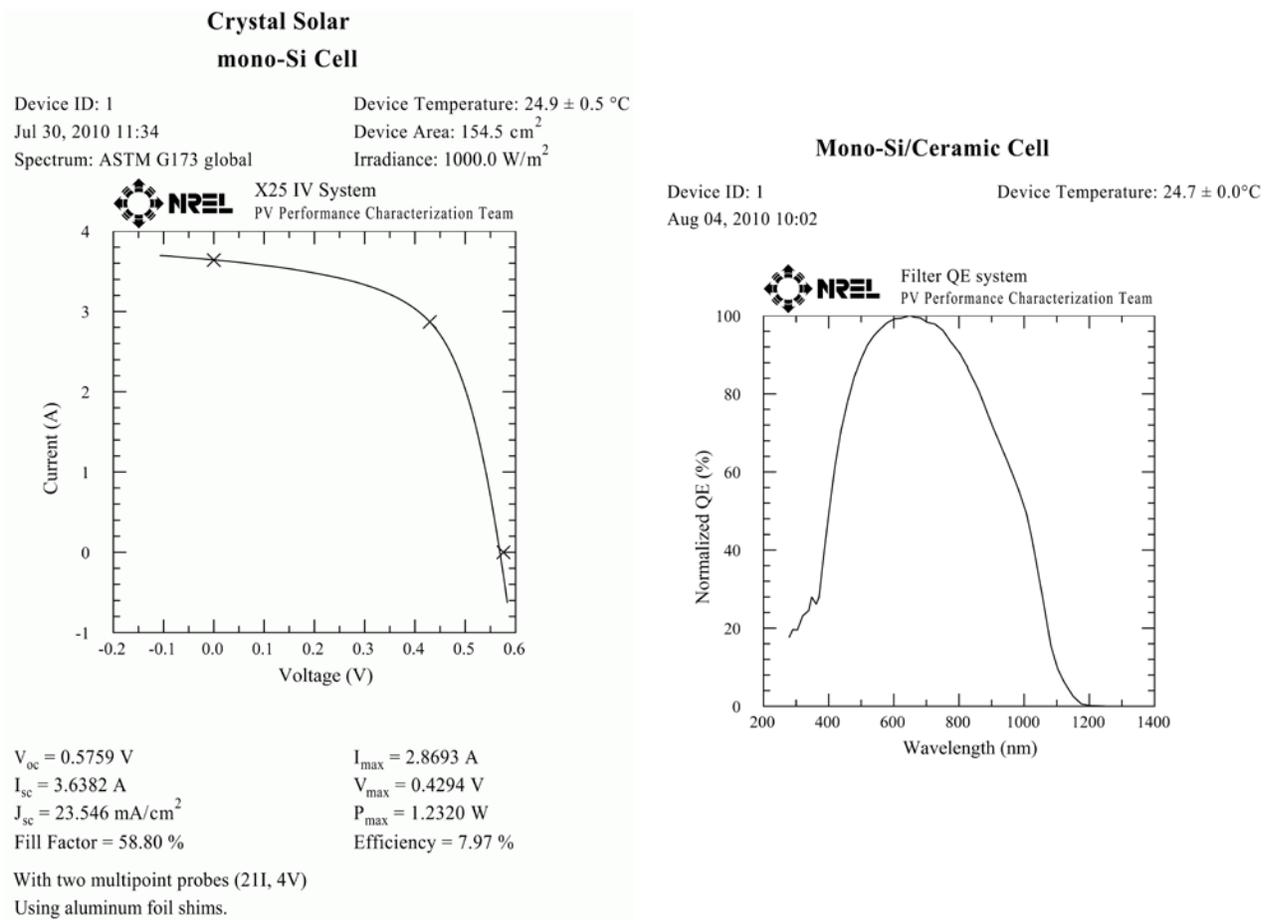


Figure 15. I-V and spectral response characteristics of full area (154.5 sq.cm), highest efficiency silicon on ceramic device fabricated to date. (Data from NREL). A quantum efficiency of 100% is achieved at a wavelength of 656 nm but with a rapid drop off at shorter and longer wavelengths on either side. This is discussed further below.

A more detailed PC1D simulation has been carried out with some key controllable parameters as inputs to determine the achievable efficiency with these wafers. The data is shown in Table 3.

According to the simulations the achievement of > 15 % efficiency requires a lifetime of 10 μ -sec. Other device improvements that enhance efficiency include:

- Shallower junctions for increased blue response
- Substantial reduction in the front surface recombination velocity by over two orders of magnitude
- Improved front reflectivity (better texturing and AR coatings)

Table 3. PC1D simulation showing the impact of critical device and materials parameters on achievable cell efficiency

Parameter	Ceramic cell - May 2010	Shallower emitter	Reduce series resistance (better back contact)	Improve Front SRV (surface cleans)	Reduce front reflectivity	Improve R-shunt	Improve Lifetime
Emitter sheet res	40-50 ohm/sq	80-90 ohm/sq	80-90 ohm/sq	80-90 ohm/sq	40-50 ohm/sq	40-50 ohm/sq	40-50 ohm/sq
Passivation/ARC	1000A thermal oxide	1000A thermal oxide	1000A thermal oxide	1000A thermal oxide	130A thermal oxide + Hi-temp PECVD SiN (700A, 360C)	130A thermal oxide + Hi-temp PECVD SiN (700A, 360C)	130A thermal oxide + Hi-temp PECVD SiN (700A, 360C)
Refractive Index	1.5	1.5	1.5	1.5	1.9	1.9	1.9
Reflectivity after ARC	2%-15%	2%-15%	2%-15%	2%-15%	2%-8%	2%-8%	2%-8%
Front-side metallization details	200A Ti/500A Pd/2 um Ag followed by lift-off	200A Ti/500A Pd/2 um Ag followed by lift-off	200A Ti/500A Pd/2 um Ag followed by lift-off	200A Ti/500A Pd/2 um Ag followed by lift-off	Ferro NS33-510 Ag paste; 980C, 100in/min Despatch	Ferro NS33-510 Ag paste; 980C, 100in/min Despatch	Ferro NS33-510 Ag paste; 980C, 100in/min Despatch
Jsc (mA/cm2)	24.98						
Voc (mV)	561.9						
Fill Factor (%)	52.5						
Efficiency (%)	7.37						
R-shunt (ohm-cm2)	273						
R-series (ohm-cm2)	4.93						
Epi Thickness (um)	40	40	40	40	40	40	40
Front texture depth (um)	10	10	10	10	10	10	10
Exterior Front Reflectance (%)	10	10	10	10	6	6	6
Internal Rear Reflectance (%)	0	0	0	0	0	0	0
Junction Depth (um)	1.25	0.6	0.6	0.6	0.6	0.6	0.6
p+ BSF Thickness (um)	4	4	4	4	4	4	4
Bulk lifetime (usec)	0.5	0.5	0.5	0.5	0.5	0.5	10
Front SRV (cm/s)	700000 (7.0e5)	700000 (7.0e5)	700000 (7.0e5)	7000 (7.0e3)	7000 (7.0e3)	7000 (7.0e3)	7000 (7.0e3)
Rear SRV (cm/s)	1e7	1e7	1e7	1e7	1e7	1e7	1e7
1/R-shunt (Siemens)	1	1	1	1	1	0.38	0.38
R-series (ohm)	4.8E-02	4.8E-02	1.0E-02	1.0E-02	1.0E-02	1.0E-02	1.0E-02
Jsc (mA/cm2)	23.92	25.8	26.73	29.3	30.61	30.81	32.84
Voc (mV)	581	578.6	578.5	592.4	593.8	597.3	643.2
Fill Factor (%)	56.2	56.0	64.4	65.5	65.9	72.8	74.1
Efficiency (%)	7.81	8.36	9.96	11.38	11.97	13.41	15.65

Two key features required for achieving high efficiency in thin silicon wafers - back surface passivation and back reflectors using appropriate dielectric stacks for reflecting IR light, are not readily feasible for the silicon on ceramic structures. This is a result of:

Rear surface passivation: Typically rear surface passivation is achieved with dielectrics such as silicon oxide and silicon nitride. Although we either grow oxides or deposit nitride films on the epitaxial film surface the high temperatures associated with the subsequent ceramic consolidation step and more importantly, the diffusion of impurities from the ceramic is expected

to severely compromise the quality of the interface between the silicon and the dielectric, negating any positive impact of surface passivation.

However the lack of effective rear surface passivation is not expected to be an issue since the use of epitaxy to grow the films enables the formation of an in-situ p+p junction which shields electrons from the rear surface of the wafer. Since all our wafers have built in electron reflectors (p+p junction) we are not depending upon rear surface passivation for reduced SRV.

Rear photon reflectors On the other hand the need for rear reflectors for infrared light that is not absorbed by the silicon becomes more important as the wafer thickness is reduced. A very effective dielectric stack on the back is required to reflect long wavelength photons back into the silicon to achieve higher currents. Typically a dielectric stack would be composed of low refractive index dielectric (such as SiO₂) with a reflective metal (Al) film on top with appropriate contact openings in the dielectric for back ohmic contact. With the ceramic consolidation process being a high temperature (> 800° C) process such a dielectric stack would not survive ceramic consolidation and the aluminum would melt at these temperatures.

Quantum Efficiency Characterization

We have done a more detailed analysis of the quantum efficiency of the silicon-ceramic cell as compared with thin epitaxial device bonded to glass (using EVA) which enables the processing of the back side of the cell for the formation of dielectric stacks.

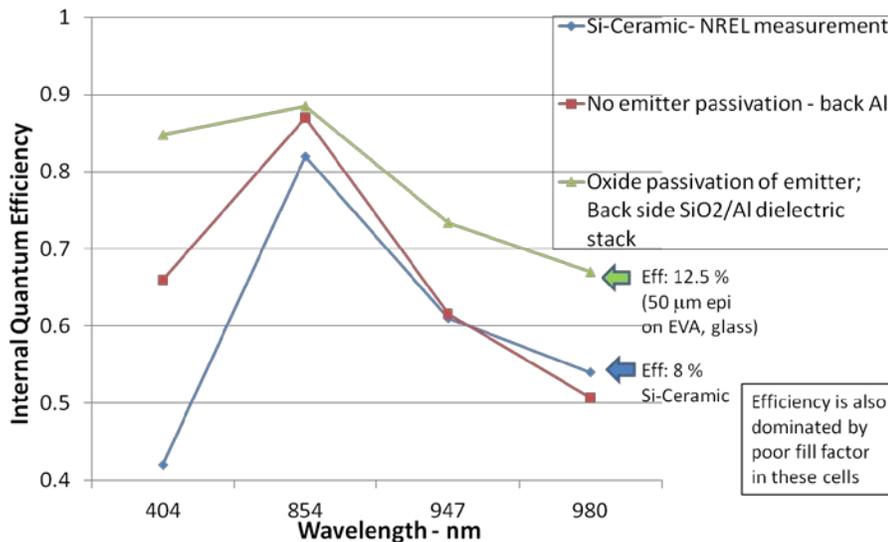
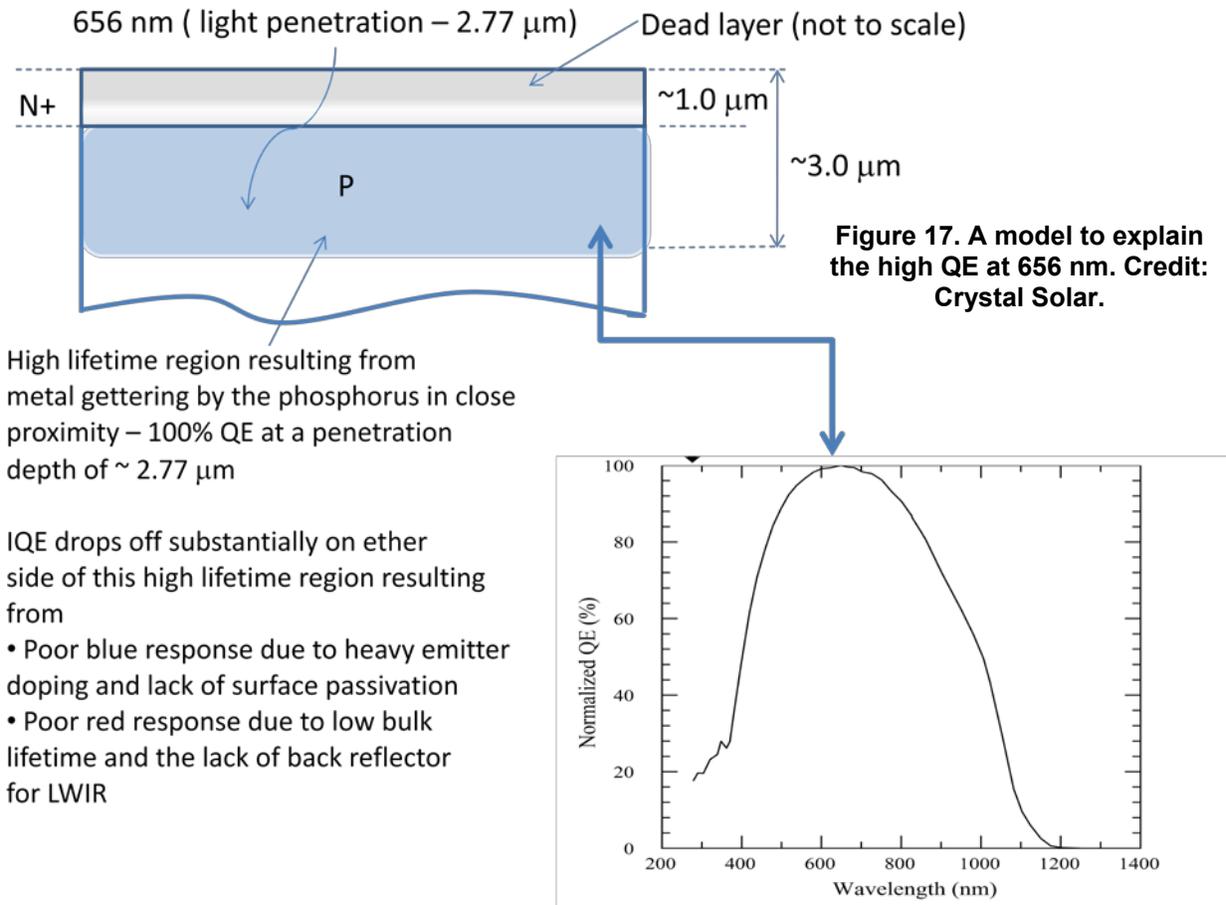


Figure 16. IQE vs. wavelength using a LBIC tool comparing the silicon- ceramic device (NREL data) with two 50 micron thick cells bonded to glass using EVA. Emitter passivation and a dielectric stack on the back have substantial impact on the blue and red response respectively, as expected. The Si-Ceramic cell suffers from poor blue and red response due to the lack of these two surface attributes. Our LBIC tool has only the four wavelengths shown; consequently the observed 100% QE for the Si-Ceramic cell at 656 nm is not shown. Credit: Crystal Solar.

In Figure 16 is compared the QE of the ~ 8% efficiency Silicon on Ceramic cell with two cells fabricated using silicon bonded to glass. These two cells were processed differently with in one case no emitter passivation and no dielectric stack on the back and in the second case a passivated emitter and a SiO₂/Al dielectric stack on the back.

The observation of a quantum efficiency of 100% at a wavelength of 656 nm can be explained according to the following model shown schematically in Figure 17.



Although the bulk lifetime of the silicon on ceramic wafer is low ($< 1 \mu\text{-sec}$) regions of the wafer in close proximity to the phosphorus doped region (the n+ region) can be effectively gettered and the local metals content reduced. This region is also the region being sampled by the 656 nm wavelength light and shows a quantum efficiency of 100%. At shorter and longer wavelengths the QE is substantially reduced as a consequence of losses in the heavily doped emitter, the lack of emitter passivation, poor lifetime in the bulk and lack of a back reflector. (see Figure 16)

Based on work to date on this program we are unlikely to improve the lifetime of the silicon on ceramic wafers with existing ceramic materials and the high temperatures of consolidation of the ceramic. Consequently the only opportunity for improving device characteristics is to improve the front side of the device – better junction quality, uniformity, oxide passivation of the surface and more uniform ARC. Fill factor improvement has to be addressed by better junction quality (reduced junction leakage) and better contacts, especially at the back.

In this context the last set of devices fabricated with silicon on ceramic wafers on this program are based on the following process flow:

Typical POCl_3 based emitter formation is done with a two step process with a pre-deposition step involving the formation of a Phospho-Silicate glass (PSG) on the silicon surface by injecting oxygen and POCl_3 into the diffusion furnace at ~ 845 C. Following this is a drive in step at ~ 850 to 1000 C whereby the phosphorus is driven in deeper to achieve the requisite junction depth. An issue with this diffusion recipe is the formation of a region near the surface with very high phosphorus concentration exceeding the solubility of phosphorus in silicon ($2\text{E}20$ atoms/cc). This region, often called the dead layer, introduces high surface and near surface recombination. An approach for reducing the surface concentration and hence the surface recombination velocity is to perform an additional drive in after removal of the PSG from the surface. Since the PSG is the source of phosphorus, removing this will enable redistributing the phosphorus in the silicon, reducing surface concentration and increasing the junction depth. Janssen et. al. (2) have demonstrated a reduction of the SRV by this means. King et.al (3) have measured the surface recombination velocity as a function of surface phosphorus concentration. Figure 18 combines the data from these two publications to show the impact of an additional drive in on surface concentration of phosphorus and the SRV.

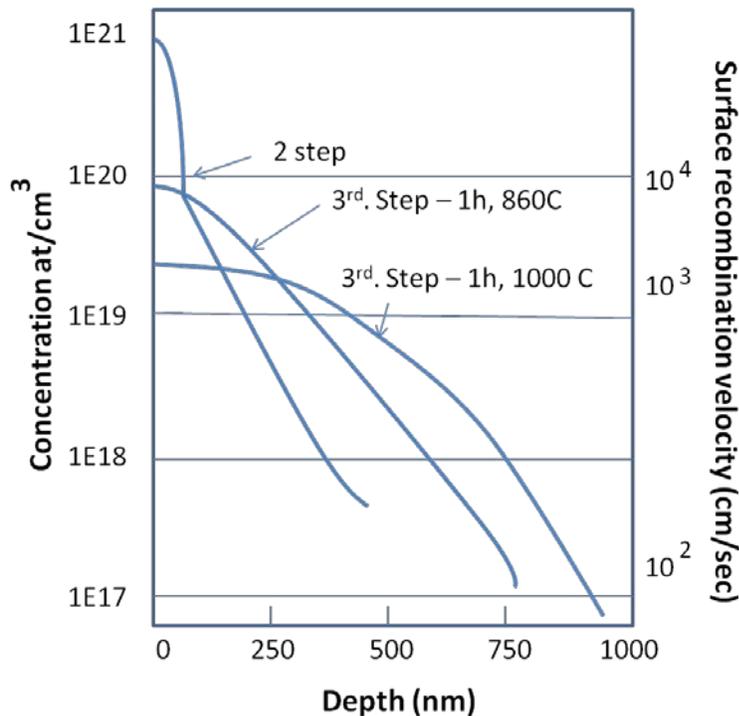


Figure 18. Schematic of expected emitter profiles with POCl_3 diffusion under different conditions (2). The surface recombination velocity for various phosphorus surface concentrations is also shown (3).

We have used a modified version of the process flow based on the 3 step diffusion, with the expected diffusion profile shown in Figure 18, (2) and added a final oxidation step to attempt to achieve a low SRV with an oxide passivated emitter. The details of the junction formation process are as follows:

- 1st. step - POCl_3 predep at 840 C - 35 minutes
- 2nd. step - Phosphorus drive in at 840 C -12 minutes
- PSG removal and clean

- 3rd. step - Phosphorus dive in (without PSG) for 1 hr at 900 C in nitrogen
- 4th. Step - Dry oxidization at 800 C for 3.5 minutes to achieve ~10 nm thermal oxide.

Devices fabricated with this process flow unfortunately failed as a result of several process problems including poor quality of the texture etch and severe device shunting problems. We attribute the device failure to multiple causes:

The fundamental problem is the contamination from the ceramic which not only adds metallic impurities to the epitaxial silicon film during ceramic consolidation but also outgases during the POC13 diffusion step further contaminating the surface of the silicon wafer during diffusion.

The surface of the silicon after ceramic consolidation appears to respond differently to texture etching process as compared to epitaxial wafers not attached to a ceramic handling layer. Texture etching results have been very poor with non uniform etching, local staining and other undesirable attribute. This may be a result of surface contamination that is not entirely removed by the traditional SC1, SC2 clean.

Since we use a ~ 1 micron thick oxide on the silicon, between the epitaxial layer and the ceramic to function as a diffusion mask during emitter formation, the integrity of this layer is critical to prevent phosphorus diffusion in the openings in the ceramic layer at the back of the wafer. This layer also has to withstand the texture etching and pre diffusion wet cleaning steps. Although we have established that the KOH/IPA based texture etching solution etches the oxide film at a slow rate the possibility exists that, in local regions at the back, the oxide is removed leading to local phosphorus diffusion at the back of the silicon leading to shunting paths in the device.

Task 5: Cost estimates for integrated process flow

Based on our high rate, multiple wafer epitaxial tool the cost of manufacture of thin silicon wafers (< 50 μm in thickness) will be substantially less than conventional silicon wafers ~ 200 μm thick based on the traditional poly silicon production, ingot growth and wafering. Figure 19 compares the costs of traditional wafers with that of thin epitaxial films.

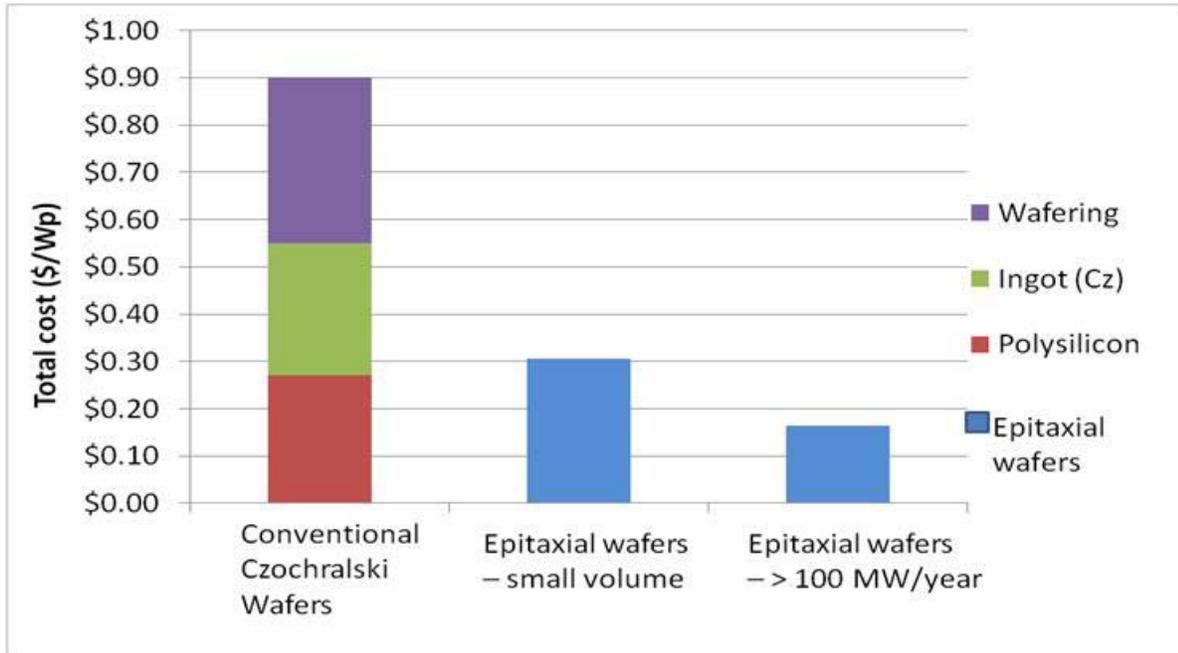


Figure 19. Cost comparison between conventional solar wafers (~ 200 μm thick, Czochralski wafers) and 50 μm thick epitaxial wafers. Credit: Crystal Solar.

The cost-adder due to the ceramic addition to the epitaxial silicon wafer fabrication comes almost entirely from the cost of the ceramic precursor powder. We have, on record, volume price quote from a leading US Supplier of the ceramic powder, of \$25/ kg. We believe that this cost can be lowered to \$5- \$10/kg once committed agreements can be made with a wider choice of vendors. The ceramic thickness needed today of between 200 – 400 microns, can be fixed at the lower end of this range with further material and process experience. Based on a cell efficiency of 15% these improvements will enable cost projections for ceramic adder shown in Table 4.

Table 4. Cost projections of ceramic materials

	Thickness (μm)	Cost of glass feedstock (\$/kg)			
		5.00	10.00	25.00	50.00
Cost of 100 μm handling layer (\$/watt)	100	\$0.01	\$0.03	\$0.07	\$0.14
Cost of 200 μm handling layer (\$/watt)	200	\$0.03	\$0.06	\$0.14	\$0.29
Cost of 400 μm handling layer (\$/watt)	400	\$0.06	\$0.11	\$0.29	\$0.57

In the above table, the green areas represent our target costs.

4 Achievements and Learning from this Program

Key achievements of this program are summarized below:

- We have taken our approach to producing very thin ($< 50 \mu\text{m}$) single crystal epitaxial silicon wafers and successfully developed a technique for handling and processing these thin wafers by integrating them with strong ceramic materials
- For the first time the integration of very thin, single crystal silicon wafers with non silicon substrates has been demonstrated
- Ceramic compositions that result in structures that are expansion matched to silicon have been formulated and tested
- Full size (125 mm X 125 mm) wafers have been produced with $\sim 50 \mu\text{m}$ thick silicon wafers integrated with 200 to 400 μm thick ceramic substrates formed in the form of a grid to enable back side contacts to the solar cell
- A novel technique for dispensing ceramic paste precursors in a predetermined pattern using a simple robotic device has been developed.
- A solar cell fabrication process flow with composite silicon- ceramic wafers has been developed and used to fabricate large area devices
- A cell efficiency of $\sim 8\%$ (125mm X 125 mm silicon on ceramic device) has been achieved.

Challenges with the technology:

- Although we have successfully reinforced thin epitaxial films with a ceramic backing material to enable handling and processing of the thin silicon, impurity contamination of the silicon from industrial ceramic materials limits this technology.
- In spite of being able to tailor the CTE differences between silicon and the ceramic materials we have not been able to achieve the required flatness in the resulting wafers to achieve high yields in device processing. This may not be a fundamental show stopper but with the limited numbers of wafers we have fabricated and the lack of statistics the currently fabricated wafers do suffer from unacceptably high bow and warp.
- The highest cell efficiency we have achieved with large size ($\sim 156 \text{ cm. sq.}$) solar cell is 8%. Devices are limited by low lifetime, the lack of surface passivation and the inability to provide effective back reflectors.

Below we excerpt some key comments by the reviewers at the DOE program review in May 2010:

Relevance to overall DOE objectives – the degree to which the project supports the goals and objectives of the EERE Solar Program Multi-Year RD&D plan

Comments: Difficult to assess the cost of epi growth followed by ceramic bonding. Would be the ultimate technology for crystal Si cells. Combines best of wafer and thin film Si. They are using a technique that is being explored in other groups around the world and the United States

needs to explore this approach (Si wafer re-use) as well. This then represents a good match to SETP goals. The goal of the effort is a technology to reduce the material and energy required to produce a moderate efficiency (>15%) silicon solar cell. This is aligned with the EERE goals.

- *Aware that barrier to contamination from ceramic must be solved to get acceptable efficiency.*
- *The proposed use of printed/sintered ceramic support may not be the optimal solution. The ceramic has low thermal conductivity, blocks the formation of full area back surface optical features (BSR, diffuser, etc.) and most likely undergoes sufficient volumetric change upon sintering to stress the Si material.*
- *Problems are well understood. Well-organized and logical approach to meeting goals. Good plans based on barriers and efficiency results encountered. They are considering other oxides and even the use of other "handles" to make a module. There are decision points based on results. The future development plans are reasonable, but continue the focus on the printed ceramic support substrate. As mentioned previously, it may be appropriate to consider alternate support materials.*
- *These films are being degraded by the ceramic support (strain and impurity diffusion), thus alternate support layers may be required.*

We have essentially concluded, based on the research conducted in this program, that the reviewers comments are right on track and technology development for the manufacture, processing and packaging of very thin, high quality epitaxial films and solar cells will be based on using alternative support materials that do not have the drawbacks of the identified issues with ceramic backing materials. The alternative supporting material we are using is glass with the epitaxial layer being bonded to glass using EVA or other suitable encapsulants (such a silicones) after the front side of the device fabrication is completed. After bonding to glass the substrate silicon is exfoliated and the back side of the solar cell appropriately processed by adding a dielectric stack and contact metal for rear reflection and rear contact.

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