Light Trapping for High Efficiency Heterojunction Crystalline Si Solar Cells

Preprint

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Presented at the China Semiconductor Technology International Conference 2011
Shanghai, China
March 13-14, 2011

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Conference Paper
NREL/CP-5200-51248
April 2011

Contract No. DE-AC36-08GO28308

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Light Trapping for High Efficiency Heterojunction Crystalline Si Solar Cells

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Light trapping plays an important role to achieve high short circuit current density (J_{sc}) and high efficiency for amorphous/crystalline Si heterojunction solar cells. Si heterojunction uses hydrogenated amorphous Si for emitter and back contact. This structure of solar cell posses highest open circuit voltage of 0.747 V at one sun for c-Si based solar cells. It also suggests that over 25% record-high efficiency is possible with further improvement of J_{sc}. Light trapping has two important tasks. The first one is to reduce the surface reflectance of light to zero for the solar spectrum that Si has a response. The second one is to increase the effective absorption length to capture all the photon. For Si heterojunction solar cell, surface texturing, anti-reflectance indium tin oxides (ITO) layer at the front and back are the key area to improve the light trapping.

Introduction

Crystalline Si solar cells with hydrogenated amorphous silicon (a-Si:H) emitters and back contacts (1-9) possess high open-circuit voltage and high efficiency in addition to low temperature (<250ºC) and manufacturable processes. The best cell efficiency has reached 23% from Sanyo R&D lab (1). High open-circuit voltage of over 0.700 V is a key to obtain low temperature coefficient of the power (2). Processing temperature below 250°C in crystalline Si (c-Si) solar cell production enables a low thermal budget and avoids bowing of thin wafers: this is a promising approach for the future thin c-Si wafer manufacturing. To further improve the performance of Si heterojunction solar cell, light trapping will be essential. Si heterojunction solar cell suffers low short circuit current density in compared to the other high performance c-Si solar cell. The difference may come from the absorption of amorphous Si and ITO layers, and light trapping scheme. In this paper, we will present our recent process and understanding in surface texturing and anti-reflectance layer for high efficiency Si heterojunction solar cells. Random pyramidal surface texturing of c-Si is one of the effective means. With the help of ITO layer, the reflectance at optimized surface can be reduce to less the 4% for a wide range spectrum that Si has a response.

Experimental

High quality float-zone (FZ) both *n*-type and *p*-type crystal Si wafers (either polished or anisotropically textured) were used for high-efficiency cell development and light trapping study. The Si wafers are (100) orientated, about 250 μm in thickness, and 1-4 Ω·cm in resistivity. The minority carrier lifetime is in the order of 1 ms measured by the

Sinton PCD lifetime tester. The c-Si wafer is either polished or textured. KOH with IPA were used for random pyramid texturing. ITO was thermally evaporated from 90% In and 10% Sn source in the presence of O_2 atmosphere. The reflectance measurements were made using an n&k analyzer model 1280 from the n & k Technology, Inc. and Cary G5 for integrated reflectance measurement. Scanning electron microscopy (SEM) was used to study the structure of the textured surfaces. All Si film layers were deposited using the hot-wire CVD process. We use the multi-chamber T-system (11) at NREL to fabricate the intrinsic passivation layer, the emitter and back a-Si:H contacts and a final 2-5% HF cleaning before being loaded into a HWCVD a-Si:H deposition chamber.

Results and Discussions

Both crystalline and amorphous Si material have a highly reflective surface, more than 35% of visible light reflects off the surface because of its high index of refraction. Reflected light translates to a direct loss in the solar cell performance, especially in the short circuit current. To recover this loss, many light trapping methods are applied. Anti-reflectance coatings and surface texturing are a few very effective means.

Figure 1 shows a light-trapping scheme for c-Si solar cell. The Si material is sandwiched between two optical dielectric layers. When the light is shining on the front surface, light will be partially reflected. Choosing the proper index of optical layer and adjusting its thickness can minimize the reflected light. For the light through the Si, the light can have a total internal reflectance on the other side surface of Si so that the light will bounce more than twice and increase the effective absorption length. Figure 2 shows the photo-generated current density as a function of Si thickness. The maximum J_{sc} for an infinite thickness of Si is 44 mA/cm^2. One can use this chart to figure out the effective absorption length.

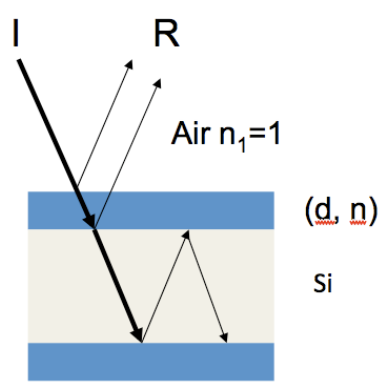


Figure 1, A scheme of the light trapping for c-Si solar cell.

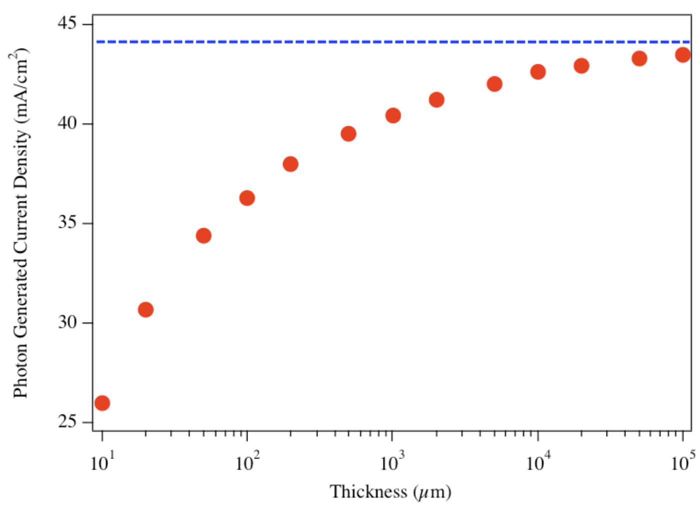
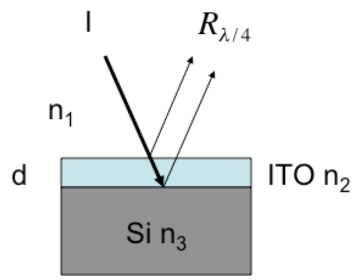


Figure 2, Photon generated current density as a function of c-Si thickness. The current density is calculated from the integration of standard solar flux at one sun with assumption of 100% QE.



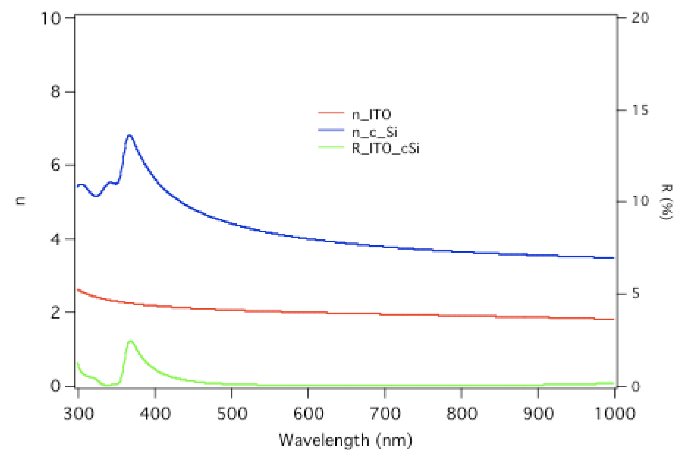


Figure 3. Schematic of single layer anti-reflectance on c-Si.

Figure 4. The index of refraction of c-Si and ITO, and calculated R a quarter wavelength as a function of wavelength.

For example, for a Si solar cell with a thickness of 200 μm, if the J_{sc} with the light trapping is at 40 mA/cm^2, the effective length will be equal to 700 μm, a gain of 3.5. The best reported J_{sc} is at 43 mA/cm^2, a 98% capture of all the photons for c-Si materials. However, the best short circuit current density for a c-Si heterojucntion solar cell is at 39 mA/cm^2, which is only 89% capture of all the photons. There is still a room for further improvement of J_{sc} for a heterojunction c-Si solar cell.

To recover this loss of reflectance at the front surface, anti-reflectance coating is applied. We will present our study of ITO as the anti-reflectance coating and its optimization to the Si heterojunction solar cells. Figure 3 shows the structure of a single ITO layer to c-Si to reduce the reflectance. Optically, light coming from the air will bounce at the ITO surface and the c-Si surface. By adjusting the thickness of ITO layer, the reflectance can be reduced. At the optimized condition, the reflectance can be near zero. From Equation 1, it is clear that the reflectance (*R*) will be at zero if n_2 = square root of n_1 x n_3, where, n_1 is the index of air, n_2 is the index of ITO, and n_3 is the index of c-Si.

$$R_{\lambda/4} = \frac{(n_1 n_3 - n_2^2)^2}{(n_1 n_3 + n_2^2)^2} \qquad [1]$$

Figure 4 plots the index of ITO and c-Si as a function of wavelength. Fortunately, the reflectance of quarter wavelength at the structure of ITO layer on c-Si, according to equation 1, can be very smaller for wide range of wavelength except the short wavelength, around 380 nm, the highest reflectance is less than 3%, which is still much smaller than 30% reflectance of c-Si surface.

Experimentally, we deposit various ITO thicknesses from 515 to 1039 nm to c-Si and measure the reflectance. For every ITO layer, there is a minimum reflectance at certain wavelength. Figure 5 shows the reflectance of two ITO thicknesses as a function of wavelength. We also checked the relationship between the wavelength at minimum reflectance and ITO thickness and it does follow equation 2.

Another interesting result is that the ITO thickness on c-Si is color sensitive. The calibration of color to the ITO thickness is inserted in the Figure 5. In general, the thinner ITO shows a brown color, and thicker ITO layer appears light blue. Most c-Si solar cells show a dark blue or purple appearance, which corresponding to the ITO thickness around 720 nm. In the later section, we will explain why most cells appear dark blue color.

$$\lambda_{\min} = 4\,n(\lambda)\,d \qquad [2]$$

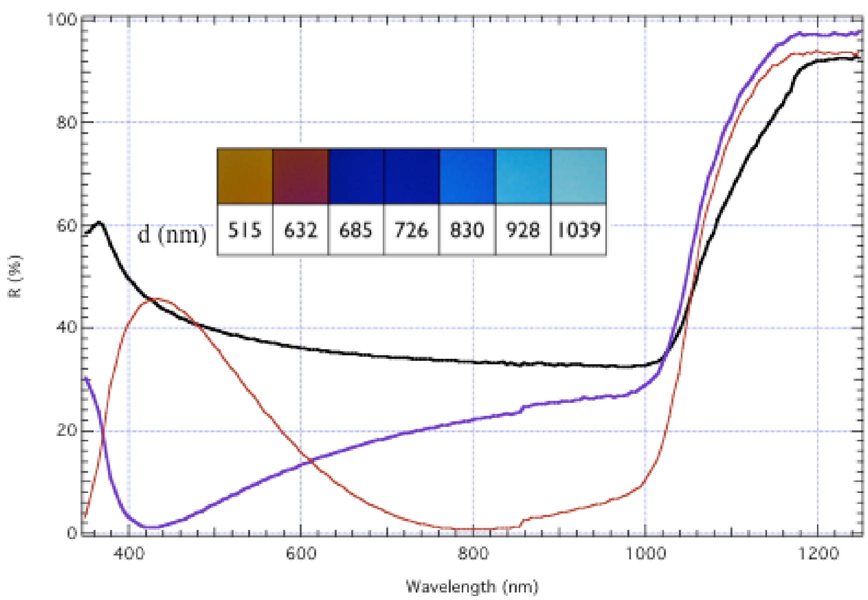


Figure 5. Reflectance of c-Si and two ITO thicknesses (460 nm and 930 nm) on c-Si as a function of wavelength. Insert is sample color that appears from the various thicknesses of ITO on planar c-Si wafer.

One caveat of single layer ITO on c-Si is that there is only one minimum in the solar spectrum. An ideal solar cell would have a zero reflectance in the wide range of wavelength, for example, from 300 to 1200 nm for c-Si based solar cells. Applying a single layer anti-reflection coating cannot meet the goal. Therefore, double layers anti-reflectance coating (ARC) will have a better result than a single layer ARC. There are many references about the double-layer coating, interested readers can refer to the reference (12).

Surface texturing is other technique used to reduce the surface reflectance. For c-Si, KOH etching with IPA can very effectively achieve random pyramid surfaces. A SEM picture of a textured c-Si surface is insert in Figure 6. The surface is populated with various sizes of small pyramids. The largest feature can be at 10 µm. The facet of each pyramid is (111) oriented. In addition, amorphous Si layer can be conformal deposited on the textured surfaces (10). Cleaning and conformal deposition of a-Si:H are the key components that enable the use of random pyramidal texturing for Si heterojunction solar cells.

Figure 6 shows the results of reflectance from various surfaces. With this random pyramidal surface, the reflectance is reduced to only 15% from 35% on a flat surface. With an ITO coated layer, the reflectance can be further reduced to only less than 4%. This is much better result than single layer ITO on planar c-Si in Figure 5. Therefore, by texturing the front surface with anti-reflectance coating or applying double layer anti-reflectance coating, the reflectance can be reduced. Another approach to reducing the reflectance is to use a graded-index of Si. The reflectance is reduced to less than 1% without anti-reflectance layer. The graded index layer with nano-size cones are made either by chemical or dry etching or photolithographic process.

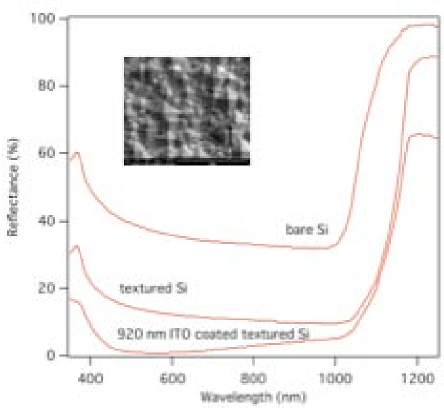


Figure 6, Reflectance of ITO coated textured c-Si, textured c-Si and bare c-Si.

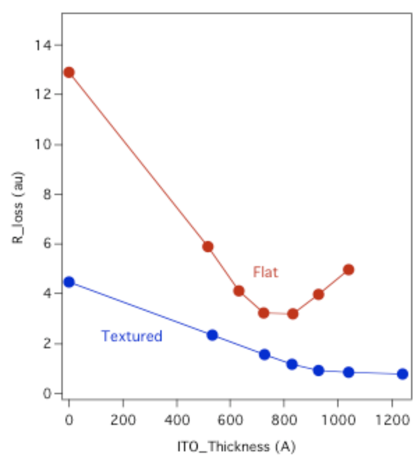


Figure 7. Reflectance loss as a function of ITO thickness for ITO on planar and textured c-Si.

We use the integration of the reflectance as a loss over the solar spectrum at AM 1.5 to optimize the ITO thickness. In Figure 5, we show that, for a thin ITO, one can reduce the blue loss but not in the red; one can reduce the red loss but not in the blue. By integrating the reflectance over the visible spectrum, we can find the optimal thickness of ITO to achieve the best spectral response from the solar cell. Figure 7 shows the summary plot of relative loss from reflectance for ITO on planar and textured c-Si as a function of ITO thickness. Clearly, the optimized ITO thickness is at 730 nm for ITO on planar c-Si. This is the thickness that corresponds to a dark blue color in Figure 3. Most c-Si solar cells should appear in the dark blue following an optimize thickness for single layer anti-reflectance coating. For ITO on textured c-Si, we found that there is a broad minimum, we use an ITO thickness of 900 nm. But for thicker ITO than 900 nm, it does not seem to harm the cell's photon collection.

For photons reach the back of c-Si, they can be totally reflected if the incident angle greater than internal reflectance angle defined by the c-Si and optical layer such as ITO. For a normal incident light on textured surface, it changes its path at the front pyramidal surface. Internal reflectance increases the effective absorption length so that thinner Si wafer can be used. For c-Si, a gain about 7 has been reported (13).

Acknowledgements

We would like to express sincere thanks to Anna Duda and Scott Ward at NREL for their help in device processing, and David Young for assistance on integrated QE software. This work was supported by the U.S. Department of Energy under Contract No. DE-AC36-08-GO28308 with the National Renewable Energy Laboratory.

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1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
April 2011	Conference Paper	

4. TITLE AND SUBTITLE
Light Trapping for High Efficiency Heterojunction Crystalline Si Solar Cells: Preprint

5a. CONTRACT NUMBER
DE-AC36-08GO28308

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Q. Wang, Y. Xu, E. Iwaniczko, and M. Page

5d. PROJECT NUMBER
NREL/CP-5200-51248

5e. TASK NUMBER
PVA9.CT10

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

8. PERFORMING ORGANIZATION REPORT NUMBER
NREL/CP-5200-51248

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
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13. SUPPLEMENTARY NOTES

14. ABSTRACT *(Maximum 200 Words)*
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15. SUBJECT TERMS
light trapping; solar cells; silicon

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
Unclassified	Unclassified	Unclassified	UL		19b. TELEPHONE NUMBER *(Include area code)*

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