



# **The Self Aligned Cell: Scaling Up Manufacture of a Cost Effective Cell Architecture for Multicrystalline Silicon Photovoltaics**

**Phase I: 01/30/09 — 12/31/09**

**Phase II: 01/20/10 — 10/19/10**

A. Gabor and F. van Mierlo  
*1366 Technologies, Inc.*  
*Lexington, Massachusetts*

NREL is a national laboratory of the U.S. Department of Energy, Office of Energy Efficiency & Renewable Energy, operated by the Alliance for Sustainable Energy, LLC.

**Subcontract Report**  
NREL/SR-5200-49934  
December 2010

Contract No. DE-AC36-08GO28308

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NREL Technical Monitor: Bolko von Roedern  
Prepared under Subcontract No. NAT-9-88012-01

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Cover Photos: (left to right) PIX 16416, PIX 17423, PIX 16560, PIX 17613, PIX 17436, PIX 17721



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## Executive Summary

Over the course of this subcontract, 1366 Technologies has evolved from a young, unknown startup company with promising technology to a well respected company with successful commercialization of work performed under the subcontract. We have both booked profitable orders and signed key partnerships. We are on the way to having a major impact on the PV industry, and the government support under this subcontract was critical in making this happen.

The goal of the contract was to develop two areas of technology for fabrication of higher efficiency Si-wafer solar cells: The first area is the formation of structured texturing that is an improvement over the industry-standard isotexture process that is applied to multicrystalline wafers. Such a surface has the benefits of 1) Lower reflectivity, 2) Decoupling the performance of the texture from the saw damage, thus allowing for better advances in sawing and a more robust wet process, and 3) Equal performance with lower-cost kerf-free wafers such as 1366 Direct Wafers that have no good existing texturing solution due to their lack of the saw damage required for isotexturing. The second area is the formation of fine line (<50 micron) metallization seed layers in a self-aligned manner where the fingers can be automatically and perfectly lined up to a selective emitter and where expensive silver screen printing paste can be mostly replaced by plating up the seed layers with silver or copper.

The SETP goals of lower \$/W manufacture of solar cells is supported by this program in the following ways:

- Both the texturing and metallization technologies increase cell efficiency with little or no increase in manufacturing cost/wafer
- The texturing process is enabling for next generation kerf-free wafers. This enables a large reduction in \$/W for wafer production.
- The use of metallization seed layers enables the use of cheaper copper plating. This is essential for Terrawatt production due to limitations of silver supply.

Under the contract, 1366 Technologies developed 2 pilot machines for 1) deposition and patterning of low-cost resist layers to enable simultaneous Honeycomb front texturing and groove formation for multicrystalline Si wafers, and 2) fine-line dispensing of materials that are self aligned to the grooves (e.g. – P dopant material for selective emitter formation, and Ag ink for finger seed layers to be later plated up). Multicrystalline cells with *1366-Texture* and standard screen printed metallization showed efficiency improvements as high as 0.4% absolute in comparison to isotextured control cells, and encapsulated multicrystalline cells using both *1366-Texture* and *1366-Metallization* achieved NREL verified efficiencies close to 18%.

In terms of commercialization, a contract has been signed with a large cell manufacturer for converting their factories to *1366-Texture*, and a partnering agreement has been reached with the largest in-line wet processing equipment company in the PV industry. This company, RENA GmbH, is customizing their wet benches to perform the etching part of the process, and the combination of the *1366-Patterning* Machine, the RENA wetbench, and the RENA loading/unloading equipment will be marketed and sold as a cluster solution. The marketing of the texturing equipment began during the 5<sup>th</sup> World Photovoltaic Energy Conference and Exhibition in Valencia, Spain during September of 2010, and 1366 was

recognized with an oral presentation during the conference on both the texturing and metallization technologies.

## Task Descriptions

Work under the contract was divided into the following tasks:

- Patterning – Developing the process, materials, pattern design and equipment to pattern a low cost resist. Developing the etching chemistry and process to etch through the patterned resist to form the light trapping surface texture and grooves for self-aligned metallization on multicrystalline wafers.
- Metallization – Developing the process, materials, and equipment to form seed layers within grooves that are suitable for plating up with silver or copper for formation of narrow fingers.
- Cell integration – Integrating the advanced texture and self-aligned fine-line metallization to make high-efficiency multicrystalline solar cells. Develop a process for selective emitter formation such that the metallization and highly doped grooves are self-aligned to each other.
- Scaleup - Build pilot line equipment for patterning and metallization leading to commercial production.

The sections below detail each of these tasks.

### Patterning Task

Work under this task consisted of 1) Developing an apparatus to pattern a low-cost mask layer into an array of hole or line openings for texture, and line openings for fingers; 2) Developing specialized chemistries for etching silicon through these mask openings to create the texture and metallization grooves. A v-groove texture was formed by etching through an array of line openings, while a honeycomb texture was formed by etching through a hexagonal array of point openings. A downselect was performed early on to concentrate on the lower reflectivity honeycomb approach. Honeycomb texture is the most promising surface for multicrystalline wafers but solutions to implement this have been complicated and expensive. The foremost industrial method pursued to date has been developed by Mitsubishi and has been utilized in their record efficiency multicrystalline cells. However the apparent process flow, as is shown below, involves multiple wetbenches, an expensive vacuum deposition step and intensive laser processing to produce many millions of holes per wafer in the SiN etchmask. Contrast this to the much simpler method being pursued by 1366.

#### Mitsubishi Process

Wetbench1: Planar Si etch

Vacuum Dep: SiN etchmask

Laser: Ablate holes in SiN

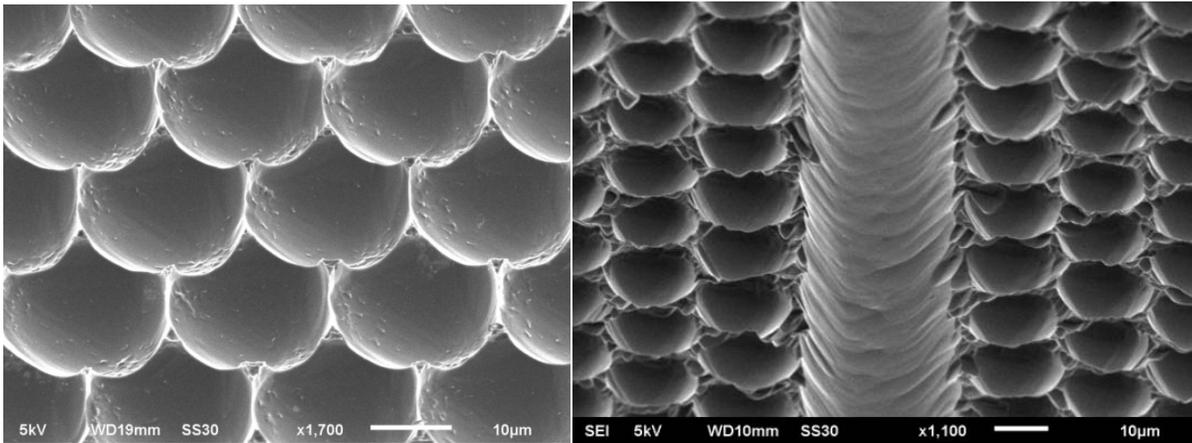
Wetbench2: Etch pits in Si

#### 1366 Process

1366-Patterning Machine

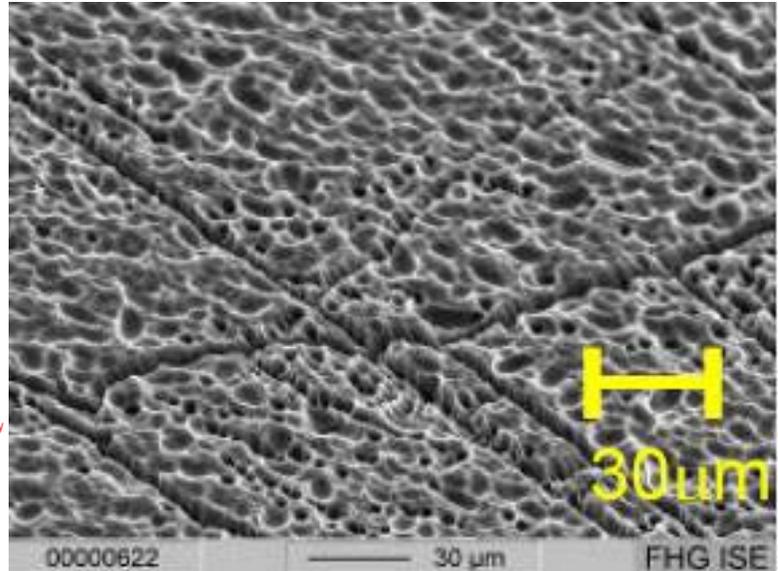
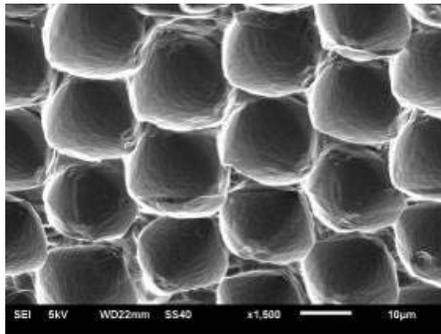
Customized RENA Wetbench

Examples of our resulting surface structure for honeycomb texture and for honeycomb texture with finger grooves is shown in the SEM images below. The processes and equipment were optimized to meet our goals of reflectivity, tolerance to surface defects in the wafers, cosmetic uniformity, cost, scalability, and throughput. We have demonstrated reflectivities superior to the industry standard isotexture on a wide range of multicrystalline and kerf-free wafer substrates. In contrast to many other methods of texturing, the improved reflectivity was achieved with a loss in open circuit voltage. Grooves < 30 microns in width were also demonstrated with this technology.

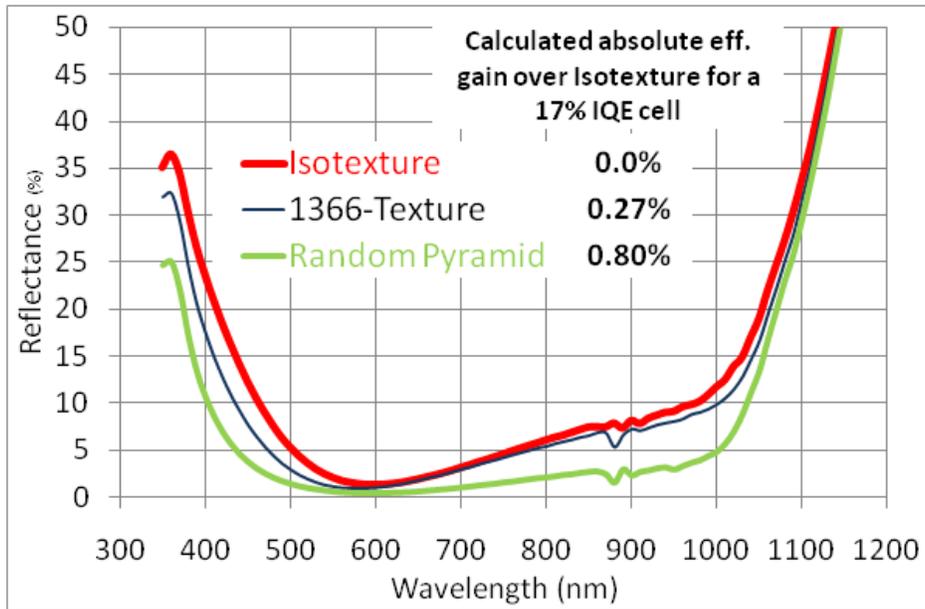


In contrast to isochemical texturing (isotexture) which requires saw damage to help nucleate the texture, *1366-Texture* is compatible with kerfless wafers such as ribbons or cleaved slices which have no saw damage. This technique uses a single etch chemistry for different wafer surfaces and crystallographic orientations. Since the acid compositions used are different from those used for isotexture, the nature of how the etchant interacts with grain boundaries and dislocations is also different. The “riff” structures seen in the isotexture image below are not seen within *1366-Texture*. This absence of deep etching at the dislocations may help cell performance and reduce the tendency for hot spot heating in modules. It has been shown that multicrystalline wafers of different qualities and dislocation densities have different optimal etching times for isotexturing in terms of maximizing efficiency. With *1366-Texture* we can expect a more uniform texturing as a function of wafer quality and possibly a tighter distribution of cell performance. In the honeycomb image below a barely observable grain boundary is present where the pits have a slightly different shape on the two grains. Improvements in the uniformity of the reflectance will be achieved in the future by modifying the etchant to attain more isotropic etching. In addition, the process allows for an optional polished rear side with no added complexity. This gives the wafers compatibility with advanced cell structures using rear dielectric passivation that would otherwise require a second polishing step. Thus we can accomplish up to three goals with the addition of just one

machine: 1) advanced texture, 2) finger grooves for advanced front metallization, and 3) rear polishing for advanced back structures.



The graph below shows an example of the lower reflectivity of nitrided wafers with *1366-Texture* as compared to isotexture. This would correspond to an absolute efficiency increase of 0.27%. The development of the equipment, processes, and materials is still ongoing, and we have programs in place to further improve the texture. These improvements will close the gap between *1366-Texture* and random pyramid texture, which could lead to an efficiency gain of 0.8%. Comparison experiments with isotextured cells to date have shown efficiency benefits as high as 0.4% absolute.



Wafer strength appears to be excellent following texturing as is shown by the 4pt bending tests below for wafers subjected to both compressive and tensile stress on the textured side, although statistical comparisons need to be performed. Anecdotally, wafers appear to be stronger than isotextured control wafers.



### Metallization Task

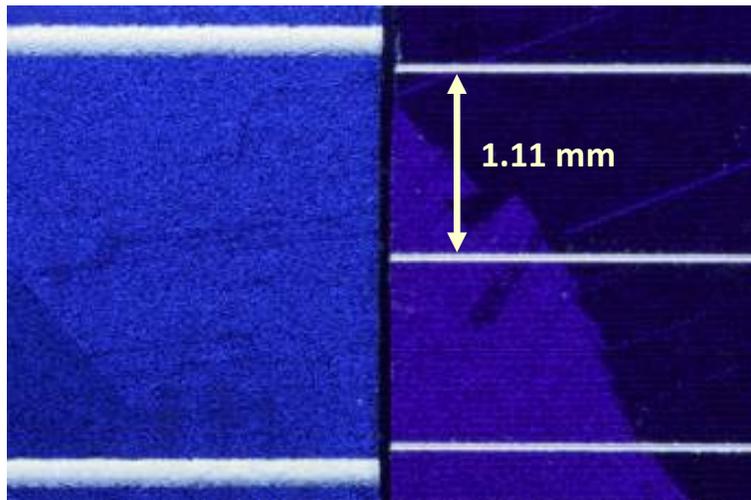
Conventional screen printed front fingers have two main problems: 1) the cost of the silver paste, and 2) the width of the fingers. The silver paste is already the second highest materials cost in making a solar cell (after the wafer), and as PV production levels climb toward the Terrawatt level, the limited availability of silver would cause silver prices to climb further. Plated silver has better bulk conductivity than sintered silver paste which can help reduce silver consumption to some degree, but eventually most of the silver needs to be replaced by plated copper which is much more abundant and

lower in cost. We have taken the approach of developing seed layer dispensing technology that allows for very fine finger formation for higher cell efficiencies, and which is compatible with plating to deposit the bulk of metal.

We have focused on two main areas within this task: 1) Development of a deposition system that deposits metal ink seed layers into grooves in the wafer surface in a self-aligned manner, and 2) Optimization of ink formulation to achieve our goals in terms of finger width, contact resistivity, adhesion strength, finger continuity, deposition reliability, and deposition rate.

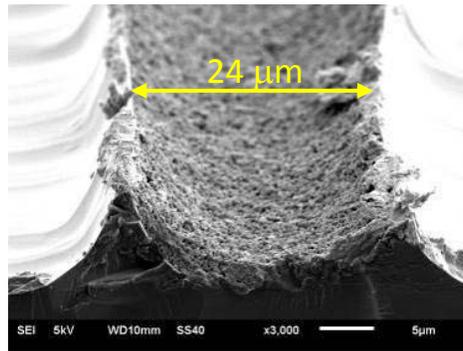
After much internal work and consultation with potential customers, a downselect was made during Phase1 of the contract to focus on deposition of inks that are modified versions of standard fired-through silver pastes. After a standard co-fire process, the seed layers are plated up with Ag or Ni-Cu-Sn stacks. This approach was seen to have the most near term industrial acceptance as well as the best near term reliability and performance. However, the deposition system was developed to be compatible with future technology nodes involving all-plated contacts.

Narrower fingers are a clear requirement for improved metallization performance, and a reduction in the use of Ag paste will also help reduce materials costs. The formation of finger grooves has some advantages over finger formation on a flat surface. Metallizing within grooves can increase finger adhesion strength and limit the amount of lateral finger growth during plating to minimize shading. The image below demonstrates the closer finger spacing that can be achieved with our fine line metallization in contrast to screen printing. Fingers are placed closer together for reduced resistive losses in the emitter, further allowing lower emitter doping for improved blue response, while also reducing finger shading.

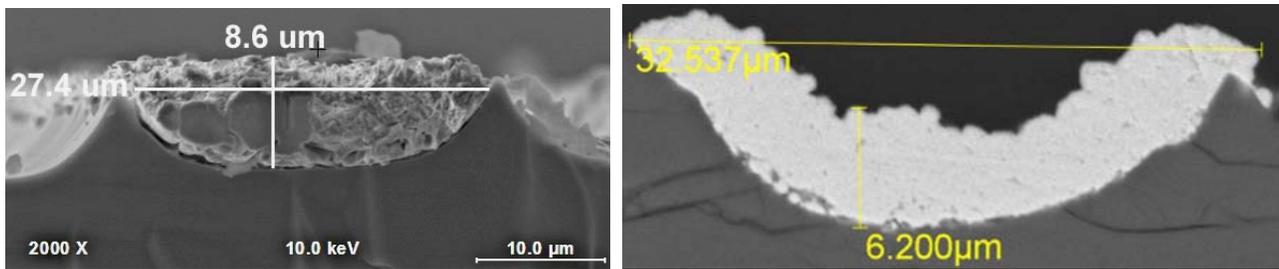


With our high-speed, self-aligned *1366-Dispensing* system, we have achieved seed layer fingers with widths below 30 microns and with fired thicknesses below 2 microns as is seen below. Upon co-firing

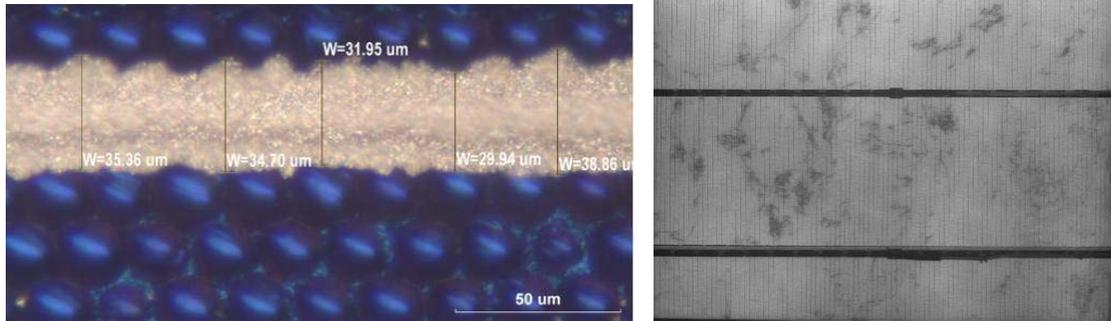
of the front and rear metallization pastes, the front Ag fires through the  $\text{SiN}_x$ . Due to the lack of sharp features in the grooves, shunt resistances are high, even on shallow emitters.



Following light induced plating, the finger heights are usually 6-9 microns as is seen in cross-section SEM micrographs of samples below.



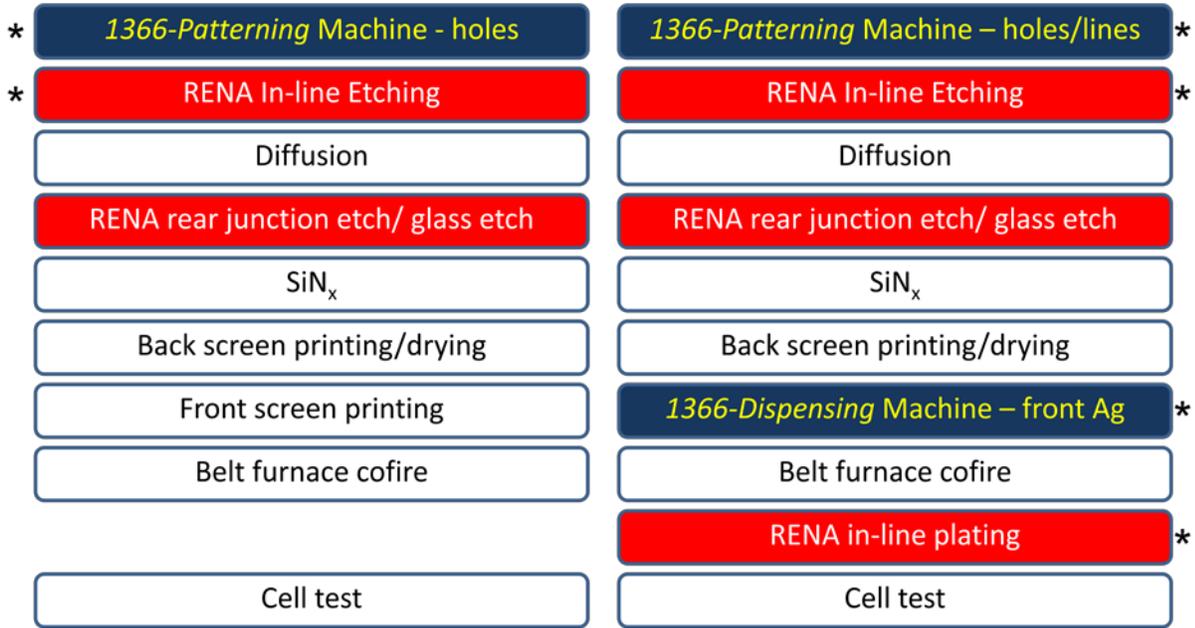
A top view optical micrograph of a finger is shown below as is an electroluminescence image of a finished cell which shows no significant finger discontinuities. We have seen that the narrowest plated fingers, fully contained within the grooves, can be obtained by dispensing paste only on the bottom region of the grooves. For better contact resistance and adhesion, paste is more commonly deposited to cover the full surface of the groove. In this case, the fingers grow in width outside the grooves during plating. Contact resistivities are typically below 2 milliohm-cm<sup>2</sup> for uniform sheet resistivities of 90 ohms/sq. Selective emitters may not be necessary for structures with the plated-up seed layer approach based on these results. However, the selective emitter approach will likely be valuable for an all-plated approach to widen the process window.



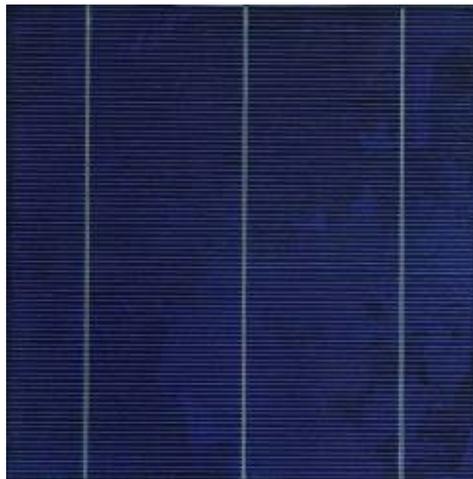
Although the primary application used to date for the *1366-Dispensing* system has been for deposition of silver ink into grooves, the system is a general purpose tool capable of dispensing a wide range of materials. The self-aligned nature of this system allows for the automatic alignment of one processing step to a subsequent step – a powerful manufacturing concept. As is discussed in the section below, we demonstrated this concept by self-aligning a selective emitter pattern to the metallization pattern. We have also explored other applications and expect more to evolve.

### **Cell Integration Task**

The *1366-Texture* described above can be either combined with *1366-Dispensing* or stand on its own and be combined with conventional screen printing for front contact formation. The flowcharts below describe the planned industrial approach for these two cases. RENA wet processing equipment will be described in the next section. For the development work under this contract, nearly all etching and plating was performed in batch mode at 1366. Proof of concept in-line etching and plating was demonstrated to reduce scale-up risk.

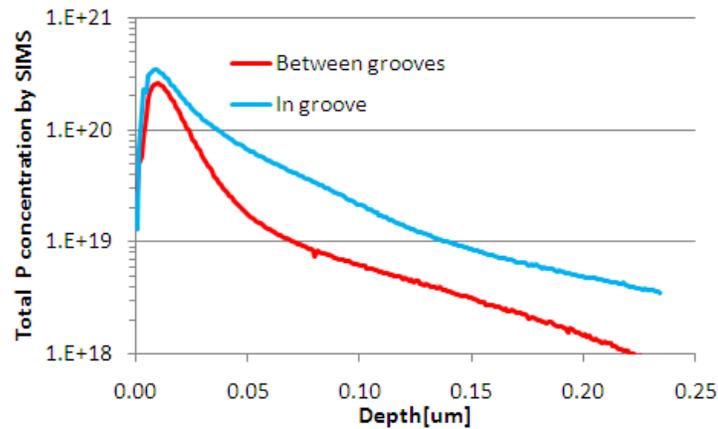
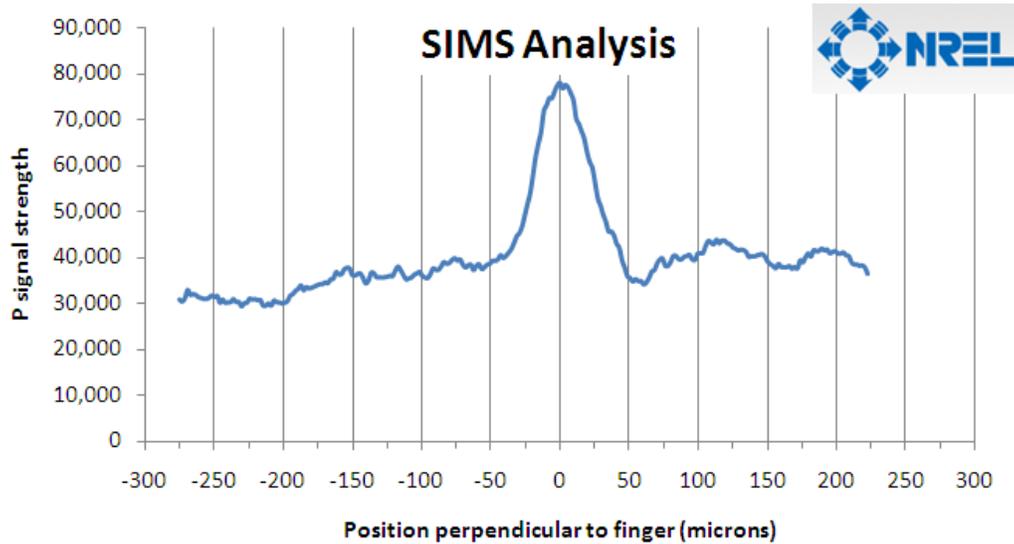


An image of a typical cell is shown below. Since encapsulated cell efficiencies are the most relevant and since the light trapping from the honeycomb texture is dependent on the encapsulation, reflectivity measurements were often made with index matching oil to take into account encapsulation effects, and encapsulated cell coupons were regularly made to gauge our progress. An image of an encapsulated cell is shown below.



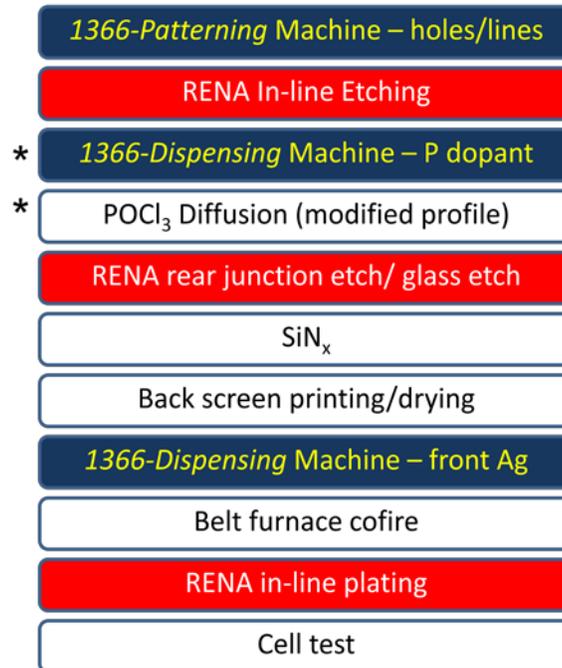
Dispensing of a phosphorus-containing dopant into the grooves prior to POCl<sub>3</sub> diffusion allows the formation of a selective emitter profile with deep diffusion in the grooves. The selective emitter profile promotes good contact resistance and low shunting, while retaining a shallow diffusion in the field

between grooves for an improved blue response. The plot below shows a SIMS depth profile of the P concentration in two portions of a bare wafer following diffusion and glass etch: a region in the center of a groove and a region in the field between two grooves. The peak P concentration and the depth of the diffusion are much heavier in the groove. Also below is a SIMS line scan of surface P concentration, where the concentration in the groove is twice as high as immediately outside the groove. This demonstrates that narrow bands of heavy diffusion can be achieved by this technique.



Such a narrow diffused band is useless for conventional methods of metallization, as aligning metal fingers directly on heavily diffused regions has proved to be a challenge. In practice, manufacturers make heavily diffused bands that are significantly wider than the fingers to allow for the tolerances in alignment and process variations. Having a heavily diffused region extend significantly beyond the fingers greatly reduces the blue response of the device in these regions, giving back some of the potential gains of the selective emitter structure. In contrast the self-aligning characteristic of the 1366-

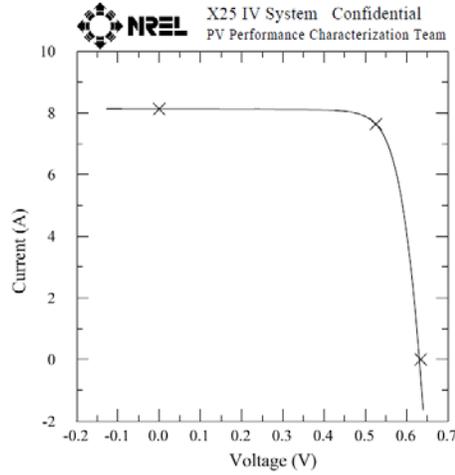
*Dispensing* method allows for perfect alignment of the dopant and metal seed layer within the grooves, and thus of the fingers to the highly diffused regions. The process is also elegantly simple, requiring only the addition of one gentle dispensing step and a modification to the diffusion recipe. This is in contrast to other methods of selective emitter formation that require the addition of several expensive steps. The process flow for our selective emitter process is shown below.



Our champion multicrystalline encapsulated cell I-V measurement, confirmed by NREL, is shown below with an efficiency close to 18%. This cell had a conventional back Al paste metallization. With improvements to the aspect ratios and uniformity of the pits in the honeycomb structure, our champion result will exceed 18% efficiency in the near future. This cell utilized a uniformly doped emitter with a sheet resistance of around 90 ohms/sq. Due to our ability to contact such low doped emitters, the potential benefits of the selective emitter structures are modest. However, implementation of the selective emitters may broaden industrial process widows and may also be particularly beneficial in combination with future all-plated metallization structures.

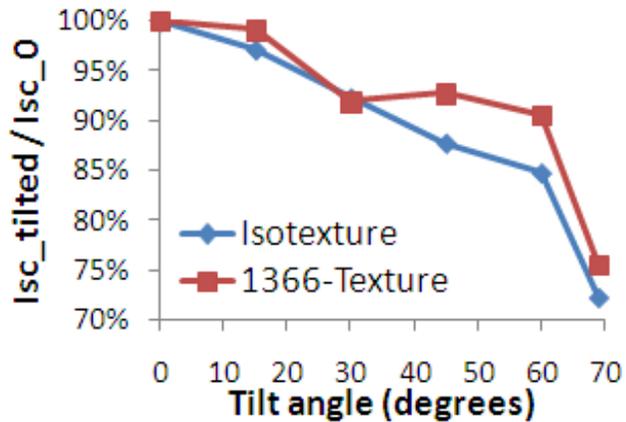
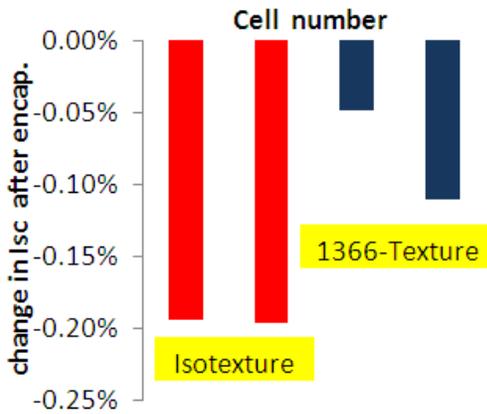
**1366 Technologies  
multi-Si Cell**

Device ID: R270-03A-024      Device Temperature: 24.8 ± 0.5 °C  
 May 07, 2010 14:53      Device Area: 224.9 cm<sup>2</sup>  
 Spectrum: ASTM G173 global      Irradiance: 1000.0 W/m<sup>2</sup>



$V_{oc} = 0.6339 \text{ V}$	$I_{max} = 7.6319 \text{ A}$
$I_{sc} = 8.1236 \text{ A}$	$V_{max} = 0.5254 \text{ V}$
$J_{sc} = 36.121 \text{ mA/cm}^2$	$P_{max} = 4.0101 \text{ W}$
Fill Factor = 77.87 %	Efficiency = 17.83 %

The graphs below demonstrate that for encapsulated cells (standard interconnect wire, EVA encapsulant, and 3mm Centrosol C+glass) under standard testing conditions the change in short circuit current after encapsulation is better for *1366-Texture*, as is the performance vs. tilt angle from the sun outdoors for the encapsulated cells. While cell performance under standard testing conditions is certainly important, in the end, the energy delivery under real world conditions is what matters most. This preliminary data suggests that modules with *1366-Texture* will perform well in the field.



## **Manufacturing Task**

To commercialize the *1366-Patterning* and *1366-Dispensing* systems, complementary downstream processing equipment is needed. For *1366-Patterning*, a customized in-line wetbench is needed, and for *1366-Dispensing*, plating equipment is needed to plate up the seed layer. To this end, we have teamed with the world leader in wet processing equipment for silicon wafer PV. RENA GmbH is our ideal partner, and is working to optimize the etching materials, process, and equipment for implement of *1366-Texture*. They have recently constructed pilot line wetbenches for etching optimization. Working with such a powerful partner will maximize our speed to market. Also, support from the market leader in the present dominant texturing technology is a strong vote of confidence for our next generation texturing solution. The combination of the *1366-Patterning* Machine, the RENA wetbench, and the RENA loading/unloading equipment will be marketed and sold as a cluster solution. The marketing of the texturing equipment began during the 5<sup>th</sup> World Photovoltaic Energy Conference and Exhibition in Valencia, Spain during September of 2010, and 1366 was recognized with an oral presentation during the conference on both the texturing and metallization technologies.

Below is a page from a data sheet for the *1366-Patterning* production system. While pilot systems were built and demonstrated at 3MW rates for both *1366-Patterning* and *1366-Dispensing*, the patterning system is further along and is the first machine to be commercialized. The first contract has recently been signed with a large cell manufacturer for converting their factories to *1366-Texture*. This first commercialization constitutes a successful close to the subcontract.



# 1366 Technologies Patterning Machine



The 1366-Patterning Machine takes unprocessed wafers and prepares them for subsequent processing in a RENA wet bench.

Together these two machines produce a honeycomb textured surface with low reflectivity on any type of silicon wafer.

This honeycomb texture does not depend on saw damage to nucleate, and the etch chemistries used do not deeply etch dislocations and grain boundaries.

The Patterning Machine patterns the wafer surface with an etch resist containing millions of small openings. Acid can then etch through these openings to form a hexagonal array of pits that have excellent light trapping properties.

## Technical Data

**Max Throughput:**  
3000 wafers/hour

**Compatible Wafer Dimensions**  
156x156mm standard  
Thickness: > 140  $\mu$ m  
Custom sizes possible

## Machine Dimensions

Length: 5613 mm  
Width: 1574 mm  
Height: 2350 mm

## Facility Requirements

Compressed Air: 10-100 L/h  
Electricity: 400-480VAC 3Ph+N+PE 50/60Hz

## Key Features

### Quality Control

Automatic inspection of patterning quality on each wafer

### Human Machine Interface

Panel PC-based touch screen provides ease-of-use and flexibility to the user  
Customized interfaces possible

### Parallel Process

The two transport belts can be operated independently, increasing overall uptime

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<b>1. REPORT DATE (DD-MM-YYYY)</b> December 2010			<b>2. REPORT TYPE</b> Subcontract final report			<b>3. DATES COVERED (From - To)</b> Phase I: 01/30/09 — 12/31/09 Phase II: 01/20/10 — 10/19/10		
<b>4. TITLE AND SUBTITLE</b> The Self Aligned Cell: Scaling Up Manufacture of a Cost Effective Cell Architecture for Multicrystalline Silicon Photovoltaics					<b>5a. CONTRACT NUMBER</b> DE-AC36-08-GO28308			
					<b>5b. GRANT NUMBER</b>			
					<b>5c. PROGRAM ELEMENT NUMBER</b>			
<b>6. AUTHOR(S)</b> A. Gabor and F. van Mierlo					<b>5d. PROJECT NUMBER</b> NREL/SR-5200-49934			
					<b>5e. TASK NUMBER</b> PV10.1199			
					<b>5f. WORK UNIT NUMBER</b>			
<b>7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)</b> 1366 Technologies, Inc. 45 Hartwell Avenue North Lexington, MA 02421					<b>8. PERFORMING ORGANIZATION REPORT NUMBER</b> NAT-9-88012-01			
<b>9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)</b> National Renewable Energy Laboratory 1617 Cole Blvd. Golden, CO 80401-3393					<b>10. SPONSOR/MONITOR'S ACRONYM(S)</b> NREL			
					<b>11. SPONSORING/MONITORING AGENCY REPORT NUMBER</b> NREL/SR-5200-49934			
<b>12. DISTRIBUTION AVAILABILITY STATEMENT</b> National Technical Information Service U.S. Department of Commerce 5285 Port Royal Road Springfield, VA 22161								
<b>13. SUPPLEMENTARY NOTES</b> NREL Technical Monitor: Bolko von Roedern								
<b>14. ABSTRACT (Maximum 200 Words)</b> Two areas of technology for fabrication of higher efficiency Si-wafer solar cells were addressed: (1) the formation of structured texturing that is an improvement over the industry-standard isotexture process for multicrystalline wafers. (2) the formation of fine line (<50 micron) metallization seed layers in a self-aligned manner where the fingers can be automatically and perfectly lined up to a selective emitter and where expensive silver screen printing paste can be mostly replaced by plating up the seed layers with silver or copper. The benefits are: a) Lower reflectivity , b) Decoupling the performance of the texture from the saw damage, thus allowing for better advances in sawing and a more robust wet process. 1366 Technologies developed 2 pilot machines for 1) deposition and patterning of low-cost resist layers to enable simultaneous Honeycomb front texturing and groove formation for multicrystalline Si wafers, and 2) fine-line dispensing of materials that are self aligned to the grooves.								
<b>15. SUBJECT TERMS</b> Multicrystalline Silicon solar cells; texturing of multicrystalline silicon solar cells; honeycomb texture; selective emitter silicon solar cell; self-aligned solar cell; solar cell manufacturing equipment								
<b>16. SECURITY CLASSIFICATION OF:</b>			<b>17. LIMITATION OF ABSTRACT</b> UL	<b>18. NUMBER OF PAGES</b>	<b>19a. NAME OF RESPONSIBLE PERSON</b>			
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