2008 Solar Annual Review Meeting

Session: Wafer Silicon
Organization: National Renewable Energy Lab
Funding Opportunity: NREL Core Program

Qi Wang
qi_wang@nrel.gov
Ph: 303-384-6681

NREL/PR-520-43200
Presented at the Solar Energy Technologies Program (SETP) Annual Program Review Meeting held April 22-24, 2008 in Austin, Texas

Budget and Solar America Initiative Alignment

Wafer Si NREL			
Project Beginning Date	**FY07 Budget**	**FY08 Budget**	**Total Budget**
10/1/07	$2.42 millions	$ 1.912 millions	$ 4.34 millions

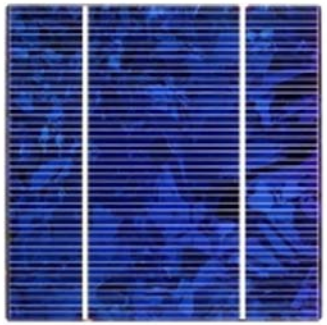
- This project supports the Solar America Initiative by working on

  - Wafer Si accounts for 92% world-wide solar cell production
  - Research to fill the industry R&D pipeline for the issues in wafer Si
  - Development of industry collaborative research
  - Improvement of NREL tools and capabilities
  - Strengthen US wafer Si research

Project Overview: Two Roadmaps

High efficiency
single c-Si

Low cost
mc-Si: casting and ribbon



Common to both roadmaps

Interconnect, packaging, reliability,
process diagnostics and modeling,
and reduced Si consumption

Project Alignment with Technology Roadmap

What needs in the Technology Roadmap are your project responding to?

What approaches are you using to address those needs?

Need	Significance	Our approach
single c-Si		
2. Surface passivation	Lower surface recombination is needed to yield cell efficiencies > 25%.	a-Si/c-Si surface passivation and high efficiency SHJ solar cells
3. Light management for thin cells	Thinner cells need very effective light-trapping and reduced metallization shadowing.	Uniform pyramid, nano feature surface, AR coating and infrared enhancement
4. Low recombination contacts	High efficiencies require metallization schemes for low recombination contacts.	Study metal to doped µc-Si and TCO contacts
mc-Si		
1. Bulk defect engineering & passivation	Identify performance-limiting mechanisms in cells made from current c-Si feedstock materials. It will provide a pathway to using lower-cost feedstock and higher efficiency on lower-cost cells.	a-SiNx and a-Si passivation and Hydrogenation at high temperature
3. Solar-quality feedstock	Reduce cost of Si materials in cell without hurting efficiency.	Evaluate solar Si feedstock

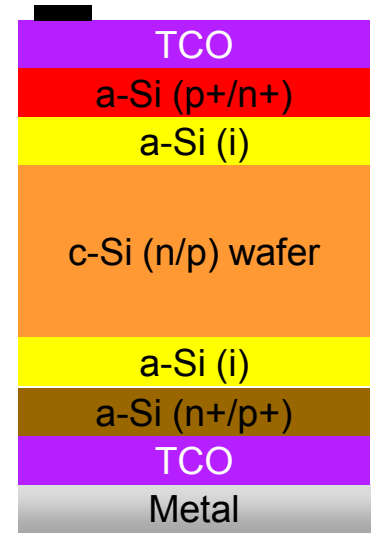
Project Update

	Planned work since last Program Review	Status
2007	Si Heterojunction solar cells	Meet FY07 milestone of 19%
2007	Measurement and characterization	Successful c-Si WS & support industry
2008	3" CZ Grower	Place order on March, 2008
2008	Si Heterojunction solar cells	Working on increase Jsc and large area cell in Si cluster tool
2008	Surface and bulk passivation	Waiting for Si cluster tool
2008	Black Si and solar cells	Master black surface preparation and work on solar cell
2008	Interdigitated/heterojunction solar cell	Mask and design near complete
2008	Direct-writing to contacts	narrow line and high conductivity on solar cells
2008	Novel TCO for c-Si solar cell	Anticipated 9/2007
2008	18th c-Si workshop	8/3-6/08 Vail, CO

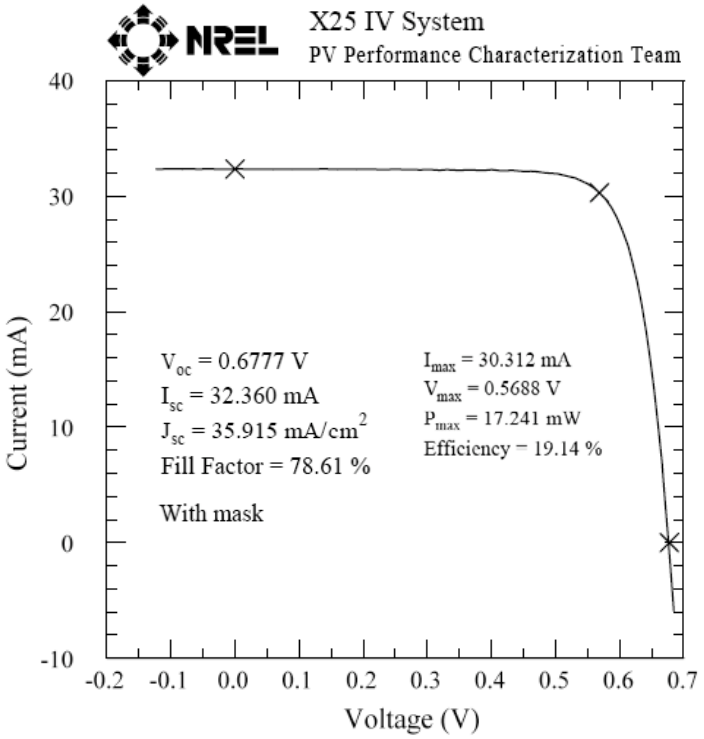
Project Update

Silicon Heterojunction solar cell

19.1% on *p*-type FZ c-Si
18.7% on *p*-type CZ c-Si



c-Si sandwich between thin Si layers



Meet FY07 19% milestone
- **FY06: 18.2%,**
- **FY07: 19.1%**
- **FY08: 18.7% on CZ wafer**

FY07 work area :
- **Back contact to increase FF**
- **Textured c-Si and cleaning**

FY 08 work area:
- **Large area SHJ solar cells**
- **Increase red absorption**

Surface and bulk passivation

a-Si:H or a-SiNx:H
using PE-, HW-, VHF-CVD

c-Si & mc-Si

Evaluation

Lifetime: ~ 1 ms
Surface velocity: ~15 cm/s
H-profile

Compare
as grow vs. annealing

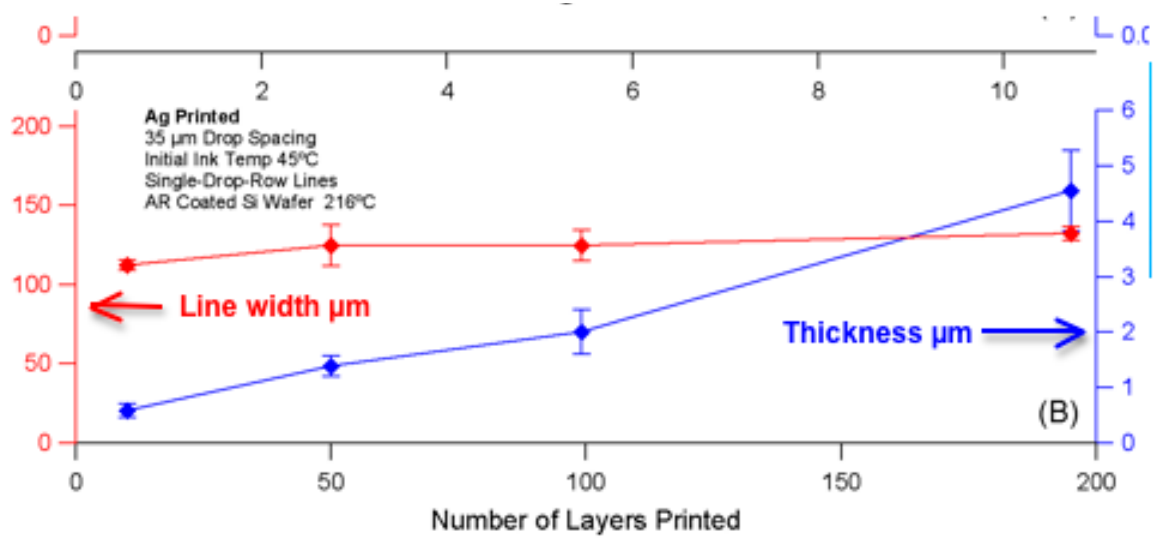
Project Update – Inkjet Contacts for Si Solar Cells

Progress	1st gen	2nd gen	**Now**	Next
Line thickness:	10 µm	15 µm	**10 µm**	15 µm
Line width:	400 µm	250µm	**80µm**	<100µm
Dep. temperature :	180°C	180°C	**180°C**	180°C
Ann. temperature:	850°C	850°C	**750°C**	<750°C
Cell efficiency	8%	8%	**13%+**	15%+

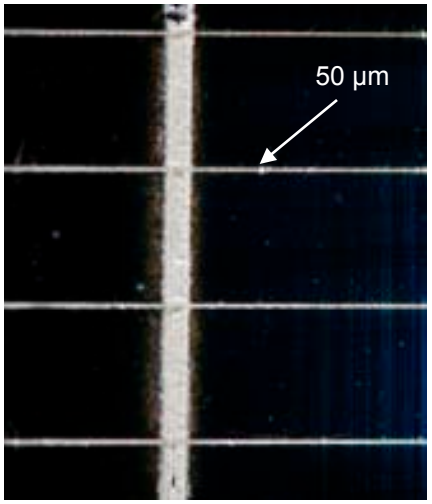
AR-coated Si substrates from Evergreen Solar

Contact Resistance 7 mΩ

Multi-layer printing of Ag showing constant line width with increasing thickness



Inkjet printed burn through and Ag contacts ~50µm wide and 10 µm thick



Project Update

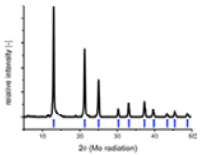
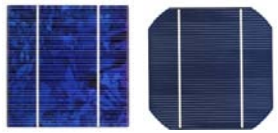
Si materials

Evaluation

Si | **Ingot** | **Wafer** | **Si analysis** | **Solar cell**





Solar Si EG-Si Mixed-Si	3” CZ Grower Casting?	ID saw Wire?	Structure Defects Impurities Electronic	Diffused SHJ Back-interdigitated Passivation Contacts Light mgmt

Obstacle Discussion

Barriers encountered or anticipated
that may inhibit success of programs

- Lack of proper equipments and sufficient staff
  - Current equipment is about 20 years old
- How to transfer laboratory cell to production
  - Scale up