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Photoconductive Decay Lifetime and Suns-V_{oc} Diagnostics of Efficient Heterojunction Solar Cells

Preprint

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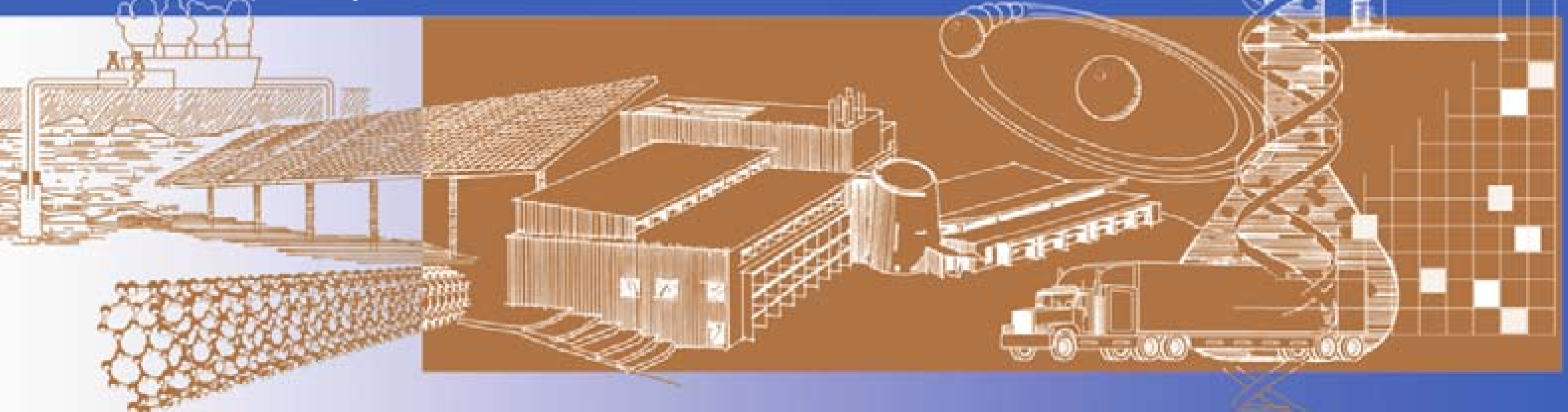
Presented at the 33rd IEEE Photovoltaic Specialists Conference
San Diego, California
May 11–16, 2008

Conference Paper
NREL/CP-520-42564
May 2008

NREL is operated by Midwest Research Institute ● Battelle   Contract No. DE-AC36-99-GO10337



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PHOTOCONDUCTIVE DECAY LIFETIME AND SUNS-V_{OC} DIAGNOSTICS OF EFFICIENT HETEROJUNCTION SOLAR CELLS

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ABSTRACT

Minority carrier lifetime and Suns-V_{oc} measurements are well-accepted methods for characterization of solar cell devices. We use these methods, with an instrument from Sinton Consulting, as we fabricate and optimize state-of-the-art all hot-wire chemical vapor deposition (HWCVD) silicon heterojunction (SHJ) devices. For double-sided SHJ devices, lifetime measurements were performed immediately after hydrogenated amorphous silicon (a-Si:H) deposition of the front emitter and back base contacts on a Silicon wafer, and also after indium tin oxide (ITO) deposition of transparent conducting oxide contacts. We report results of minority carrier lifetime measurements for double-sided p-type Si heterojunction devices and compare Suns-V_{oc} results to Light I-V measurements on 1-cm^2 solar cell devices measured on an AM1.5 calibrated XT-10 solar simulator.

INTRODUCTION

Amorphous silicon heterojunction based solar cells have excellent properties of both passivation of the crystalline Silicon (c-Si) surface enabling bulk minority carrier lifetime measurement and emitter/base current conduction capability. These properties of the SHJ on c-Si permit process optimization using the method of photoconductive decay (PCD) lifetime measurements and analysis because one can learn critical information about the final cell properties very early in the fabrication process. We found that there is good agreement between the final cell open circuit voltage (V_{oc}) from light current-voltage (LIV) measurement and implied V_{oc} derived from minority carrier lifetime measurement and analysis. Thus, we can screen our cells against process problems before lengthy final processing of cells is performed. Minority carrier lifetimes greater than 1 ms on p-type FZ and CZ wafers have been measured, which indicates well-passivated surfaces by HWCVD a-Si:H.

The excellent surface passivation capability of as-deposited a-Si:H by HWCVD enables the use of minority carrier lifetime measurement for measuring bulk or surface properties of the deposited wafer. This quick feedback is useful for tuning the device process. Lifetime measurements were done using the Sinton Consulting Inc. [1] WCT boule tester and the PCD based technique. Another measurement we have employed in the development of efficient SHJ devices is the Sinton Suns-V_{oc} system. Suns-V_{oc} is useful for determining the effect of external properties such as series resistance and also troubleshooting shunting problems within nearly completed and completed solar cells. The limit to V_{oc} in our devices is likely related to surface preparation and a-Si:H/c-Si interface properties. For Suns-V_{oc} measurement, we found nearly a one-to-one relationship to final LIV cell V_{oc}. Our best V_{oc} is 0.689 V for 3.0 Ω-cm p-type FZ material, and our best SHJ cell efficiency is 19.1% for p-type float-zone (FZ) and 18.7% for p-type Czochralski (CZ) wafer.

DEVICE FABRICATION

All the SHJ a-Si:H films reported here were deposited by HWCVD in a multi-chamber system for isolation of cross-contamination. The basis of HWCVD is the thermal catalytic deposition of silane, Hydrogen, and dopants for the growth of intrinsic and doped a-Si:H layers. We use both Tantalum and Tungsten filaments for intrinsic and doped layers, spaced 5 cm from the substrate at a deposition pressure of 10 mTorr and 60-70 mTorr, respectively. Pure silane is used for intrinsic a-Si:H (a-Si:H(i)) at a substrate heater temperature of 100ºC. Gas mixtures of approximate compositions 1:1:17 SiH_4:5%PH_3-in-H_2:H_2 (a-Si:H(n)) and 1:4:40 SiH_4:2.5%B_2H_6-in-H_2:H_2 (a-Si:H(p)) were used for our doped a-Si:H layers at a substrate heater temperature of 200ºC and 250ºC, respectively. Optimized layer thicknesses are 3 nm for a-Si:H(i) and 4-6 nm for doped a-Si:H depending upon whether the layer is the front emitter or back base contact. It is critical to avoid cross contamination of the dopants and to avoid damaging the c-Si/a-Si:H(i) interface by ion bombardment or Silicon epitaxial growth.

In the case of p-type based SHJ devices, the cell structure is grid/ITO/a-Si:H(n,i)/c-Si(p)/a-Si:H(i,p)/ITO(or no ITO)/metal with either indium tin oxide (ITO) and metal contact or metal contact directly to the a-Si:H(p) layer (Fig. 1). In our heterojunction development we

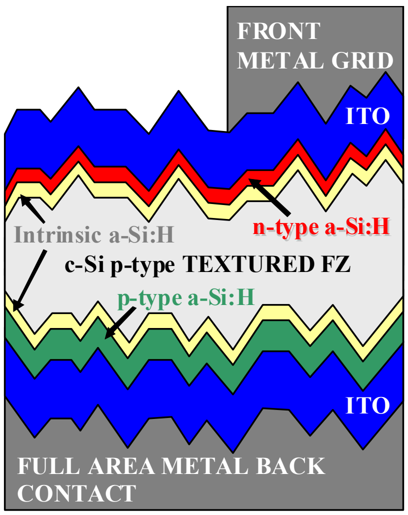

Fig. 1. Cross-sectional diagram of double-sided silicon heterojunction solar cell device for p-type textured crystalline silicon base.

have used double-sided laboratory textured and commercial polished p-type FZ and CZ c-Si wafers cleaned using both standard clean [2] (RCA process) or modified standard cleaning processes common to the integrated circuits industry [3]. The finished solar cell area is approximately 1-cm^2 with a front grid shadow loss around 5% on top of the thermally evaporated ITO. Routine LIV measurements were performed on an AM1.5 calibrated XT-10 solar simulator, and official LIV measurements were performed by the ISO-17025 accredited PV Performance Characterization Team of NREL.

After a-Si:H and ITO deposition lifetime measurements were performed using a Sinton WCT-Boule photoconductivity decay technique lifetime measurement and analysis system. This system is calibrated routinely and we use the standard infra-red-pass filter (RG-850) to ensure uniform excess carrier injection deep into the wafer bulk. Our interpretation of transient mode lifetime results comes from the interpretation of the lifetime at zero excess carrier density using a linear fit of the Auger corrected lifetime as a function of excess carrier density provided by the Sinton PCD lifetime system [4]. Suns-V_{oc} measurements were performed on finished cells using the Sinton Consulting Suns-V_{oc} measurement system in standard configuration [5].

RESULTS

We measure lifetime of every cell we fabricate both after a-Si:H deposition on both sides and after ITO deposition. Fig. 2 demonstrates the agreement between lifetime derived implied V_{oc} as measured

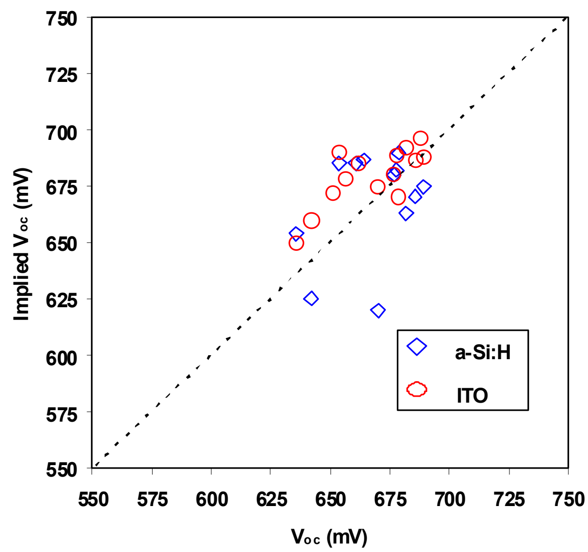

Fig. 2. Open circuit voltage for finished cell versus Sinton lifetime measurement derived Implied V_{oc} measured right after double sided a-Si:H deposition (◇) and ITO deposition (○).

immediately after a-Si:H deposition and after ITO deposition with the V_{oc} measured on the final completed solar cell. The a-Si:H deposition does not include any direct annealing of a-Si:H films under vacuum conditions as proposed by De Wolf, et. al. [6]. Our anneal takes place during ITO deposition in a reactive oxygen ambient at a substrate temperature of 180ºC for 30 min. Often times we see an improvement after ITO deposition, although this is not always the case as there are many factors affecting the V_{oc} of these devices. One complicating factor in this analysis for our research size cells is that the lifetime measurement is an average measurement for nearly the whole sample area and the LIV measurement is performed with a shadow mask defined 1-cm^2 cell area. The implied V_{oc} derived from the Sinton lifetime measurement (Fig 3) and is an accurate measure of potential solar cell LIV response

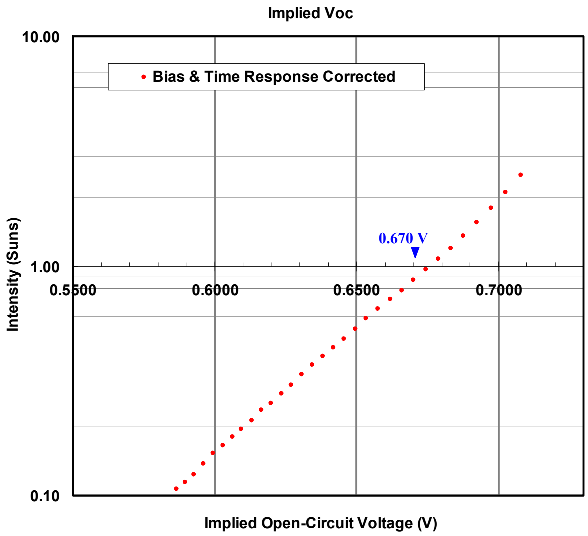

Fig. 3. Implied V_{oc} curve measured using a Sinton boule lifetime measurement system in transient mode on T3346, a p-type textured CZ sample with official LIV V_{oc} of 0.670 V (blue arrow).

when measured in the transient mode for double-sided SHJ devices. By applying the a-Si:H structure to both sides of the crystalline silicon we passivate the surfaces very well, as shown in Fig. 2 where the V_{oc} is grouped between 650-690 mV in this short series.

Fig. 4 presents the V_{oc} measured from LIV solar simulation versus Sinton Suns-V_{oc} apparatus, which is

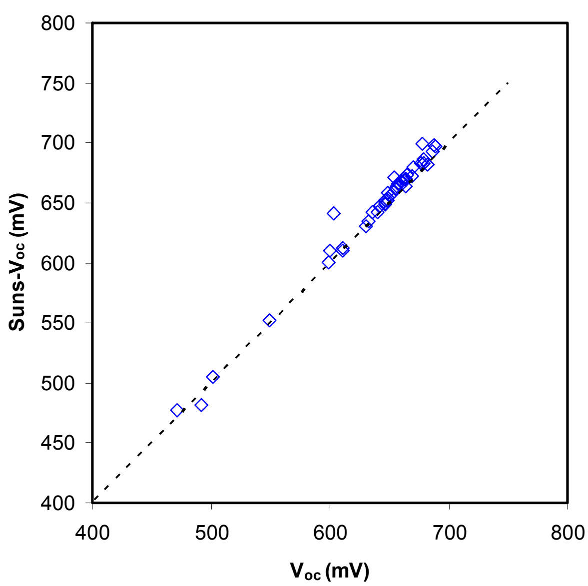

Fig. 4. Open circuit voltage for finished cell versus Sinton Suns-V_{oc} measurement showing good agreement.

the cell response assembled from the open circuit voltage of the cell that is generated as the flash lamp illumination intensity decays after the peak intensity of the flash under steady state conditions. A calibrated photodiode is used to quantify the decaying light output from greater than one sun output to zero output. The decaying light pulse signal is converted to a current in the solar cell as the voltage in open circuit decays. Suns-V_{oc} measurements are immune to series resistance contributions from the external back contact and front grid because the I-V curve is reconstructed from open circuit voltage measurements. From Fig. 4 the higher V_{oc} measured by Suns-V_{oc} is attributable to slight variations in the temperature control of the stage and variation in spectral light output of the flash lamp. In our experience the Suns-V_{oc} stage is cooler because of the room temperature control and the fact that this is a flash measurement; unlike the XT-10 tungsten lamp solar simulator which requires significant temperature control of the measurement stage.

CONCLUSION

Optimization of efficient silicon heterojunction devices requires tools for rapid diagnostics of fundamental material parameters such as minority carrier lifetime and open circuit voltage. The ability to measure both in one flash type system after the crucial step in the fabrication of a SHJ solar cell, the a-Si:H layers front and back, provides immediate feedback for device optimization. Suns-V_{oc} along with standard light I-V measurement complement each other and provide valuable information about series resistance problems and other issues related to the performance of the solar cell such as shunting. With these methods we have achieved an optimized solar cell efficiency of 19.1% and 18.7% for FZ and CZ p-type based SHJ solar cells respectively.

ACKNOWLEDGEMENT

The authors thank Anna Duda and Tom Moriarty for their device processing and characterization assistance. This work was supported by the U.S. Department of Energy under Contact No. DE-AC36-99GO10337 with the National Renewable Energy Laboratory.

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REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*
May 2008

2. REPORT TYPE
Conference Paper

3. DATES COVERED *(From - To)*
11-16 May 2008

4. TITLE AND SUBTITLE
Photoconductive Decay Lifetime and Suns-Voc Diagnostics of Efficient Heterojunction Solar Cells: Preprint

5a. CONTRACT NUMBER
DE-AC36-99-GO10337

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
M.R. Page, E. Iwaniczko, Y. Xu, L. Roybal, R. Bauer, H-C. Yuan, Q. Wang, and D.L. Meier

5d. PROJECT NUMBER
NREL/CP-520-42564

5e. TASK NUMBER
PVA74101

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

8. PERFORMING ORGANIZATION REPORT NUMBER
NREL/CP-520-42564

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES

14. ABSTRACT *(Maximum 200 Words)*
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15. SUBJECT TERMS
PV; silicon heterojunction; SHJ; photoconductive; minority-carrier lifetime; solar cell; devices; hot-wire chemical vapor deposition; silicon heterojunction; indium tin oxide; transparent conducting oxide;

16. SECURITY CLASSIFICATION OF: a. REPORT	b. ABSTRACT	c. THIS PAGE	17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
Unclassified	Unclassified	Unclassified	UL		
					19b. TELEPHONE NUMBER *(Include area code)*

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18

F1147-E(09/2007)