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16th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes

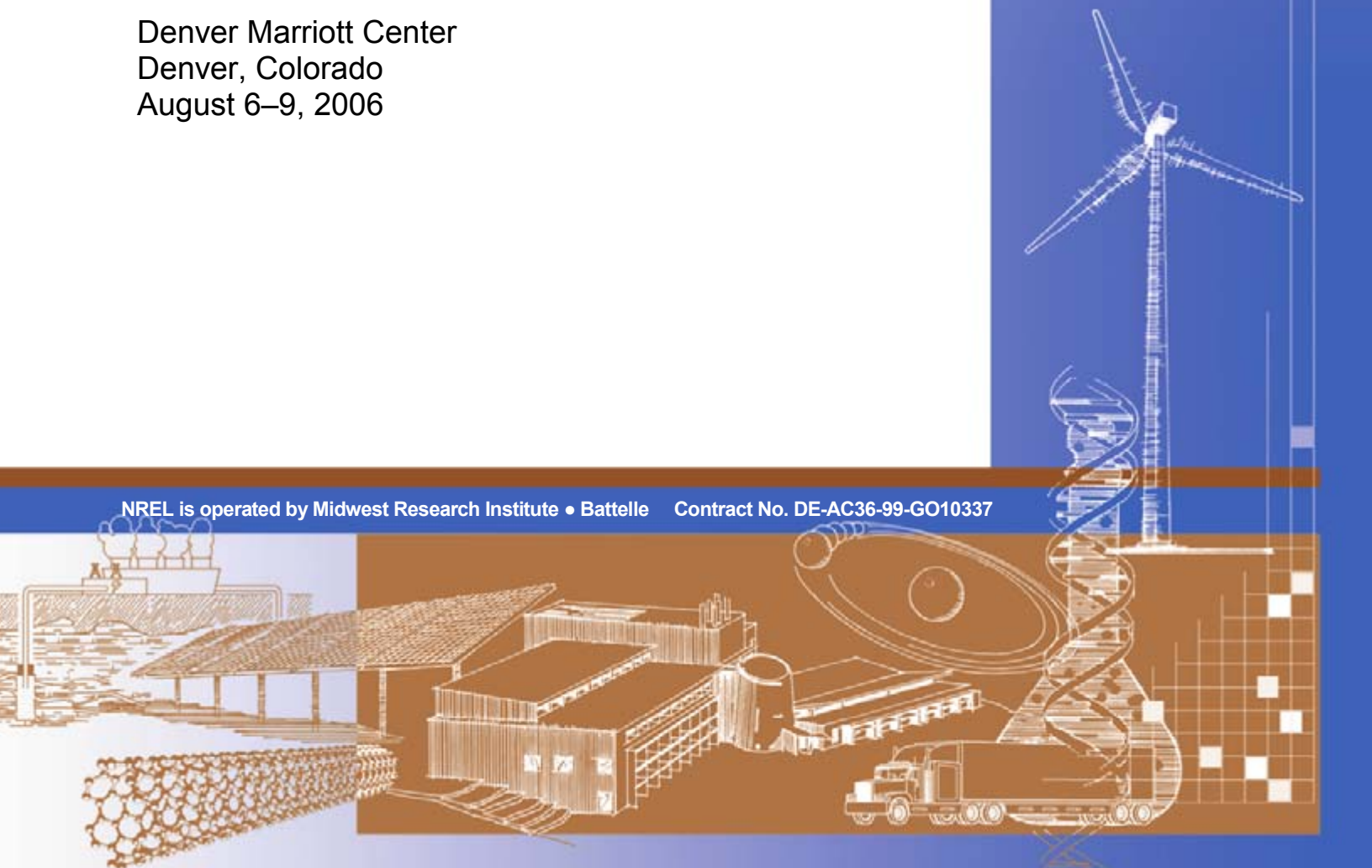
Extended Abstracts and Papers

Workshop Chairman/Editor: B.L. Sopori

Program Committee:
M. Al-Jassim, J. Kalejs, J. Rand, T. Saitoh,
R. Sinton, M. Stavola, R. Swanson, T. Tan,
E. Weber, J. Werner, and B. Sopori

Denver Marriott Center
Denver, Colorado
August 6–9, 2006

Proceedings
NREL/BK-520-40423
August 2006



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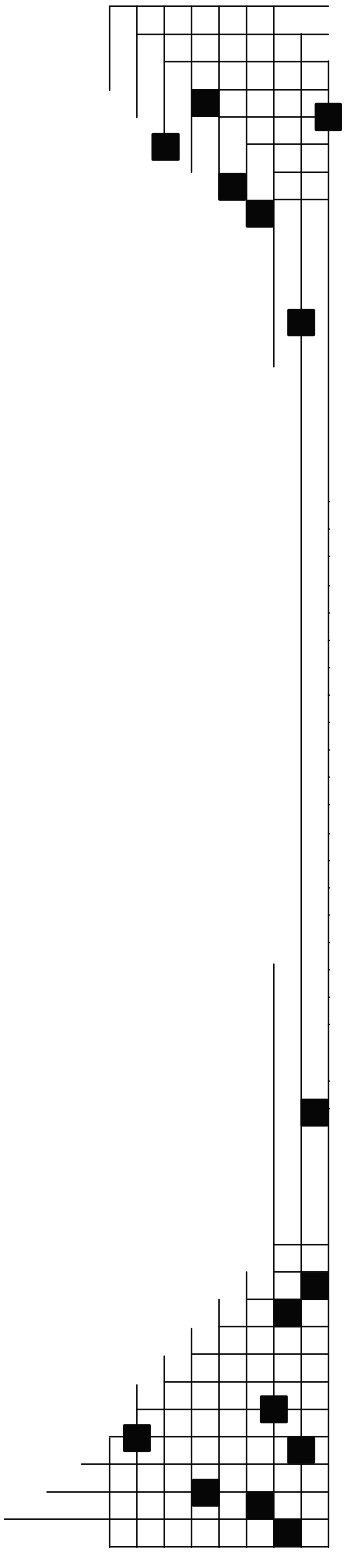
Prepared under Task No. WO97.H299



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Workshop Theme: Getting More (Watts) for Less ($i)

Bhushan Sopori

National Renewable Energy Laboratory
Golden, CO 80401

During last couple of years the demand for photovoltaic (PV) energy has grown at a phenomenal pace. This demand is being met by increasing production of solar cells and modules. While the existing PV companies are adding new manufacturing lines, new companies are entering the market. This growth appears to be limited only by the availability of silicon. The growing production has created a shortage of poly silicon feedstock. The shortage in silicon availability has prompted new approaches of efficiently using silicon in all its available forms. These include using reject wafers (which is by itself getting tight), minimizing the material that is generally discarded from the sides of ingots, exploring use of N-type silicon for solar cells, and further reduction in the wafer thickness—all aimed at getting more watts for less silicon.

Accordingly, the theme of this workshop reflects the growing need for maximizing the use of silicon to obtain the largest amount of PV energy. This workshop will include traditional sessions such as crystal growth, impurities and defects in Si, solar cell processing, module issues, and our resourceful poster sessions. In addition, there are special session, which include: Si Feedstock Issues**:** Si Refining And Purification, Diagnostic Techniques, and Thin Film Si and Heterojunction Devices. There will also be a rump session with theme: Toward 100-μm Wafer Thickness and Beyond.

I hope you enjoy this workshop. The success of the Silicon Workshops is due to active participation of all attendees who share their views on research and manufacturing issues, actively participate in discussions, prepare manuscripts loaded with latest research results, and provide feedback to further improve the contributions by the workshop. I would like to thank all speakers who present review talks for taking time to prepare excellent presentations of not only their research but also relevant results from other researchers. I am grateful to program committee for not only developing excellent programs but also inviting speakers and spending a lot of time interacting with presenters. We have had growing number of graduate students attending the workshop. I would like to thank all the companies who generously contribute to the Graduate Student Award fund.

Recent Status on Electromagnetic Casting

Kyojiro Kaneko, Keita Nakagawa, Tomohiro Onizuka, Ken-ichi Sasatani,
Nobuyuki Kubo, Michio Kida,
SUMCO SOLAR Corporation,
260-100 Funoo, Kainan, Wakayama, 642-0001, Japan

Abstract

Manufacturing of multi-crystalline silicon ingot for solar cells has been done by an electromagnetic casting, which uses a cold crucible induction melting. So far, the casting of multi-crystalline silicon ingot has been performed by a directional solidification method which uses usually a ceramic container for molten silicon. The cold crucible induction melting uses an electromagnetic field to melt metals without contact to crucible materials. From this reason, silicon can be melted without impurity contamination and the cold crucible can be used without consumption. This technique also enables the continuous casting by melting the charged material at the top of the melt and solidifying the molten material at the bottom of the melt. After the execution of governmental R&D program, the industrialization of the casting started. At present, silicon ingots are produced at the size of 35 x 35 cm² cross-section and 6 m length. Solar cell conversion efficiencies reach 15% in the solar cell production using substrates of electromagnetically cast ingot. In the present paper, the recent status of silicon electromagnetic casting and a possibility for future technological improvement are described.

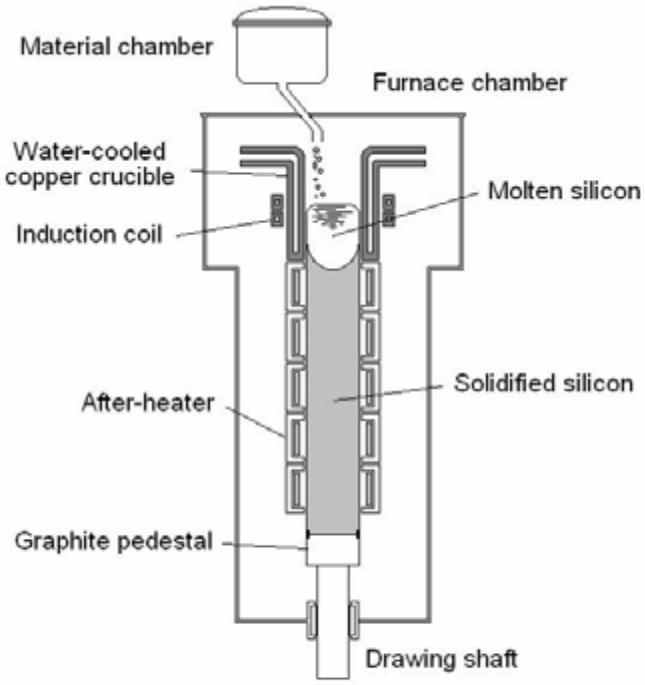


Figure 1. Schematic view of electromagnetic casting for multi-crystalline silicon ingot

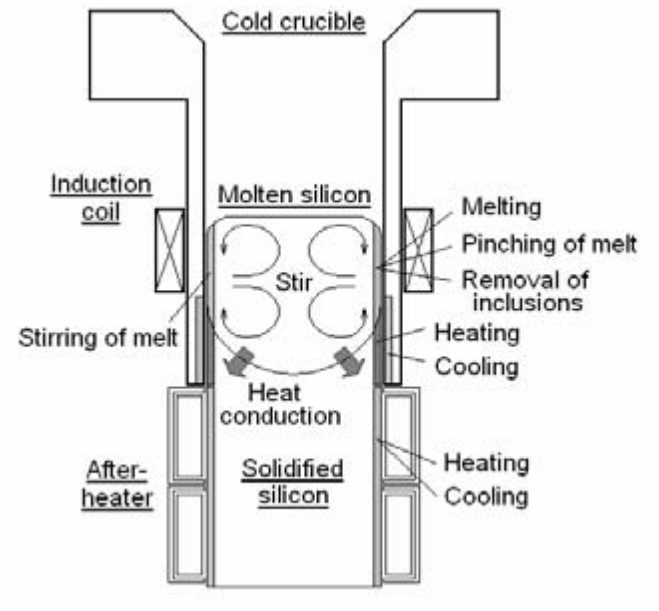
Development of silicon electromagnetic casting

Development for the industrialization started in 1986 with a crucible inner diameter of 3 cm of round cross-section [1]. Next, the cross-section of crucible changed to a square with the dimension of 12 cm side [2], and further of 22 cm side. A prototype furnace for industrialization was installed with an ingot size of 35 cm² cross-section and 3 m length, and the production of silicon ingot began in 1998.

Although the commercial production started with an ingot weight of nearly 1 ton, the production method was still not continuous and the development of continuous casting was further pursued until the year 2000. The furnace was designed to cut the solidified ingot at the bottom of the furnace. The continuous casting was performed with an ingot cross-section of 16 cm side, and the total ingot length reached 10 m with an intermittent ingot cutting of each 1 m length.

Furnace of silicon electromagnetic casting

The imposition of electromagnetic field on the molten silicon and the supply of heat to the solidified ingot affect the ingot casting behavior including the melting of charged silicon, the solidification and the cooling of ingot. The functions and the resultant effects of electromagnetic casting are described in Figure 2 to understand the proceedings of the ingot casting. As a result of the imposition of electro-magnetic field, 1) charged silicon is heated to melt (Joule heating), 2) molten silicon is self-suspended by the magnetic pressure without contact to the crucible wall (Lorentz force), 3) molten silicon is stirred due to the magnetic pressure difference, 4) contaminating inclusions with higher electric resistance in the molten silicon are ejected to the molten surface by the buoyant force due to relatively small magnetic pressure to the molten silicon. As another result of forced cooling by the cold wall of the crucible, 5) the solidification is enhanced for high speed casting due to a high rate of heat extraction, and as a further result of heat supply from the after-heater, 6) the temperature trajectory of solidified



Function and Effect
1) Heating $Q=RJ^2$: Skin depth effect
2) Magnetic force $F=JxB$: Pinching efect
3) Stirring ΔF: Heat and mass transport
4) Pressure difference ΔF: Buoyancy
5) Cold wall $Q=Q(\sigma,\kappa,h)$: Forced cooling
6) After-heater $Q=Q(\sigma,\kappa,h)$: Heat control

Q: Heat, R: Electric resistance, J: Electric current
F: Electromagnetic force,
B: Magnetic flux density
$Q(\sigma,\kappa,h)$: Heat flow by radiation, conduction and convection

Figure. 2 Explanation of function and effect of silicon electromagnetic casting

ingot can be controlled to decrease the thermal stress. The physical properties of ingot are affected by the mutual relation of these operational conditions.

Manufacturing of silicon ingot

A silicon ingot which is manufactured by the electromagnetic casting in the production line is shown in Figure 3. The side of the cross-section is 35 cm and the length is 380 cm. The weight of ingot is about 1,000 kg. Manufacturing conditions and evaluations of some crystal qualities are the followings. The casting speed is at 1.2 mm/min. The furnace operation is fully automated with a process-controlling computer. The electric power consumption is at 30 kWh/kg of shaped block for the slicing. The furnace is filled with flowing argon and the flowing rate is fixed for controlling the oxygen concentration in silicon. The argon consumption is 0.15 Nm^3/kg-Si of the shaped block. The cycle-time of 3.8 m length ingot is 90 hours. Cast ingots are cut to pieces of square block with a dimension of 15 x 15 x 40 cm^3 for the wafer slicing. The material yield of the shaped block is 77 % cutting from the as-cast ingot.

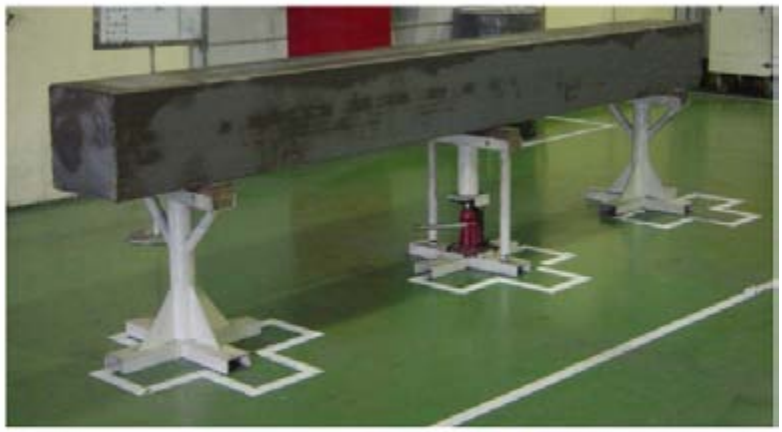


Figure 3. Silicon ingot of electromagnetic casting, 35 x 35 cm^2 cross-section and 3.8 m length

Electrical resistance is adjusted to 1 to 2 Ω·cm by the addition of boron dopant. Oxygen and carbon concentrations are less than 0.5 x 10^{17} atoms/cc and 2.5 x 10^{17} atoms/cc, respectively. Minority carrier diffusion length ranges from 50 to 130 μm. The shaped blocks are processed to the wafer slicing at 200μm thickness. The sliced wafers are fabricated to solar cells at solar cell manufacturers. The solar

Table 1. Comparison of ingot and substrate manufacturing methods for solar cells

Method	Size: Cross Section	Batch Weight	Solidification Rate	Production Rate	Conversion Efficiency	Necessary Silicon Amount
	(cm)	(kg)	(mm/min)	(m^2/day)	(%)	(g/W)
CZ Pulling	15	50	0.6 – 1.2	30	16 - 18	8 - 10
DS Casting	69	240	0.1 – 0.6	70	15	8 - 10
EMC	35	1000	1.2 – 1.5	500	15	8 - 10
EFG Ribbon	100	3.7	17	25	15	7

cell conversion efficiencies are from 14.9 to 16.0 % in the average at each solar cell production line using silicon substrates of electromagnetic casting.

Comparison of manufacturing technologies for bulk silicon solar cell

Bulk silicon solar cells in production are consisted of single, multi and ribbon crystals. A comparison is made in Table 5 with each manufacturing method. The single crystal is mainly manufactured by a Czochralski pulling method. The multi-crystal is manufactured by the methods of mold directional solidification (DS) and electromagnetic casting (EMC). The mold casting uses fundamentally a ceramic vessel to hold the melt and uses usually the Bridgemann method to perform the directional solidification. The electromagnetic casting uses a metallic crucible and performs the directional solidification, but the crucible has no contact to the melt and is not consumable. The necessary conditions to manufacture multi-crystalline ingots are firstly to grow a large crystalline grain and secondly to decrease crystalline defects during a cooling. The directional solidification works well for these purposes and is useful for the release of internal stress in the ingot at the final solidification. An edge-defined film-fed growth (EFG) method manufactures the ribbon crystal [3]. The ribbon technology is highly advantageous by a direct production of sheet-shaped substrate that needs no slicing process. The EFG technology manufactures tubes with octagonal shape of 5.3 m height.

Crystalline properties of pulled single crystals are high with a large diffusion length of minority carrier, and yield high solar cell conversion efficiency. However, although the conversion efficiencies of multi-crystalline solar cells are not much high as the single crystal solar cell, the productivity of multi-crystalline ingot manufacturing is high and the production cost of multi-crystalline ingot is low, compensating a drawback of low conversion efficiency. The productivity of the electromagnetic casting is remarkably high due to a large ingot size and a high solidification speed.

Consideration of limit of casting speed by thermal balance at solid-liquid interface

Under a steady state of electromagnetic casting, which implies the shape of the solid-liquid interface is fixed at a constant casting speed, the following thermal balance can be expressed between the heat flow into the interface and the heat flow out of the interface.

$$Q_l + \Delta H_{fusion} = Q_s \quad (1)$$

Here, Q_l is the heat flow into the interface, ΔH_{fusion} is a heat of fusion for silicon, Q_s is the heat flow out of the interface. Each heat can be calculated as $Q_l = h_l S \Delta T$, $Q_s = \lambda_s S dT/dR$, $\Delta H_{fusion} = H_{fusion} M$, where, h_l is a heat conduction coefficient of liquid silicon, S is an area of the interface, T is a temperature, λ_s is a thermal conductivity of solid silicon, dT/dR is a temperature gradient of solid silicon in a normal direction to the interface, H_{fusion} is a latent heat of fusion for silicon, and M is a

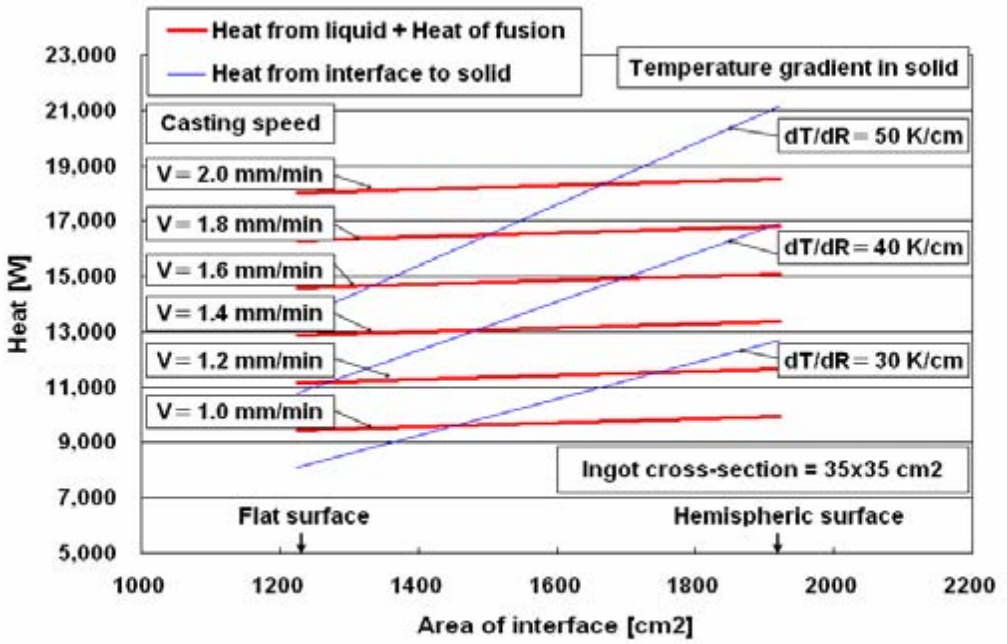


Figure 4. Thermal balance at the solid-liquid interface of silicon electromagnetic casting with changes of casting speed and temperature gradient of ingot

solidification rate of silicon.

Taking the heat conduction coefficient of liquid silicon as 0.058 W/(cm².K), the thermal conductivity of solid silicon as 0.22 W/(cm.K), the latent heat of fusion for silicon as 0.501 kWh/kg, and the temperature of liquid silicon as 1425 ºC, then, the relation of thermal balance can be calculated as the functions of the solidification rate, the temperature gradient of solid silicon and the area of the interface, as shown in Figure 4. The calculation is done for the ingot dimension of 35 x 35 cm².

The interfacial areas of 1225 cm² and 1923 cm² in Figure 4 are the areas of the flat surface and the hemispheric surface, respectively. But, the flat surface can not be realized at the electromagnetic casting. At a usual condition of casting speed at 1.2 mm/min, the shape of solid-liquid interface is observed nearly as a hemisphere or a little shallower spherical surface by the experimental measurements, so that the interfacial area can be supposed to be about 1800 cm². From the above experimental observation, it can be deduced from Figure 4 that the normal temperature gradient in solid silicon at the interface is about 30 ºK/cm at the solidification rate of 1.2 mm/min.

It is necessary to keep the shape of solid-liquid interface at a hemisphere or a little shallower spherical surface for a safe and stable casting operation. So, when the casting speed is increased, the temperature gradient of solid at the interface must be increased to maintain the same interfacial area by the thermal balance. Usually, the temperature gradients range from 30 to 40 ºK/cm for a Czochralski pulling method and from 80 to 100 ºK/cm for a float zone method. To increase the casting speed to 2.0

Table 2. Future development of silicon electromagnetic casting for solar cells

Item of development	Aim
Separation of melting and solidification by two cold crucible systems	High speed melting and high speed casting
	Crystal quality control
Continuous casting	High productivity
Large ingot cross-section	50 x 50 cm² cross-section
Selection of induction frequency	Stable casting and uniform quality

mm/min for the electromagnetic casting, the temperature gradient must be increased to about 45 ºK/cm according to the thermal balance in Figure 4.

Above discussions are based on the thermal balance calculation of an ingot of 35 x 35 cm² cross-section. However, when the shape of the solid-liquid interface is kept geometrically similar, the ratio of heat flow is same for a larger cross-sectional ingot so that the relation of the casting speed to the temperature gradient of solid ingot does not change for the larger cross-sectional ingot.

Future of silicon electromagnetic casting

It proves that the electromagnetic casting is useful for the production of multi-crystalline silicon ingot for solar cells. However, there is still room for improvement. In Table 2, items of possible future technical developments are presented with some remark. As one of technical improvements to realize high productivity with high crystalline quality, an idea of the separation of melting and solidification is possible by means of using two independent cold crucible induction equipments. By doing so, the function of the conventional cold crucible for a melting with a simultaneous solidification in one crucible will be separated to enhance the melting and the solidification independently. The continuous casting has been already developed by a proto-type furnace at a small scale of 16 cm² cross-sectional ingot. There is no obstacle for the industrialization of continuous casting. Large ingots with a dimension of 50 x 50 cm² cross-section will contribute to high productivity. Appropriate selection of induction frequency contributes to a stable casting and a uniform crystalline quality.

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An Investigation of Temperature and Impurities Distributions in a solidified Si ingot by Unidirectional Solidification Method by using a Dynamic Global Model

Koichi KAKIMOTO, Lijun LIU and Satoshi NAKANO

Research Institute for Apllied Mechanics, Kyushu University

6-1, Kasuga-Koen, Kasuga 816-8580, JAPAN

ABSTRACT

The unidirectional-solidification process is a key method for large-scale production of multi-crystalline silicon for use in highly efficient solar cells in the photovoltaic industry. Since the efficiency of solar cells depends on the crystal quality of the multi-crystalline silicon, it is necessary to optimize the unidirectional-solidification process to control temperature and impurity distributions in a silicon ingot. We developed a transient global model for the unidirectional-solidification process. We carried out calculations to investigate the temperature and impurity distributions in a silicon ingot during solidification. Conductive heat transfer and radiative heat exchange in a unidirectional-solidification furnace and convective heat transfer in the melt in a crucible are coupled to each other. These heat exchanges were solved iteratively by a finite volume method in a transient condition. Time-dependent distributions of impurity and temperature in a silicon ingot during the unidirectional-solidification process were numerically investigated.

1. Introduction

The unidirectional-solidification method is a key method to produce multi-crystalline silicon for use in highly efficient solar cells [1]. Since the efficiency of solar cells depends on the quality of the multi-crystalline silicon, which is determined by the crystallization process such as cooling rate and rotation rate of a crucible, it is important to investigate and optimize the unidirectional-solidification process to control the distributions of temperature and impurity in a silicon ingot during the solidification process.

Numerical calculation has become a powerful tool for investigation and optimization of a unidirectional-solidification process and crystal growth process with development of computer technology and new algorithms [2-12]. Since a unidirectional-solidification furnace has a highly nonlinear thermal system, transient simulation with global modeling is an essential tool for investigation and improvement of a unidirectional-solidification process from melting to cooling through the solidification process. We developed a transient code with a global model for the unidirectional-solidification process, and we carried out calculations to investigate distributions of temperature and impurity in a silicon ingot during the unidirectional-solidification process.

2. Model Description and Computation Method

Figure 1 shows the configuration and dimensions of a small unidirectional-solidification furnace for producing multi-crystalline silicon. The melt, a crystal, a crucible and a pedestal are denoted as 1, 2, 3, 4, 5 and 6, respectively. Thermal shields are labeled as 7 to 11. The two heaters marked by 12 and 13 were set to the furnace. The following points are assumed in the present calculation: (1) the geometry of the furnace configuration is axisymmetric, (2) radiative heat transfer is modeled as diffuse-gray surface radiation, (3) the melt flow in the crucible is laminar and incompressible, and (4) the effect of gas flow in the furnace is neglected.

The domains of all components in a unidirectional-solidification furnace are subdivided into a number of block regions, as shown in the left part of Fig. 1 in order to establish a discrete system for numerical simulation. Each block is then descritized by structured grids, which is shown in the right part of Fig. 1.

Conductive heat transfer in all solid components, radiative heat exchange between all diffusive surfaces in the unidirectional-solidification furnace, and the Navier-Stokes equations for the melt flow in the crucible are coupled and solved iteratively by a finite volume method in a transient condition. The impurity such as iron, gallium and boron distributions in the silicon melt and solidified silicon ingot were

solved by taking into account the thermal field and melt flow in a crucible. Impurity segregation at the melt-solid interface was taken into account. The shape of a melt-solid interface was obtained by using a dynamic interface tracking method. The global iterative procedure was described so far [13].

The boundary conditions of iron concentration are as follows. Concentration of iron on the crucibles wall and the segregation coefficient of iron k_0 were set to $2x10^{15}$ cm^{-3} and $8x10^{-6}$, respectively. We used the reported data of diffusion constants of iron in solid and liquid, which are expressed in eq. (1) [14, 15],

$$\begin{aligned} D_m &= 1.0\times 10^{-3}\, cm^2/s \\ D_s &= \exp[-(3.028+3286/T)\ln 10]\, cm^2/s, \end{aligned} \tag{1}$$

where D_m and D_s are diffusion constants of iron in the melt and the solid, respectively. We used the diffusion constant of iron in a solid, as a value of single crystalline silicon, while the actual crystal for solar cells is a poly crystal. The segregation at a melt-solid interface was expressed by eq. (2),

$$D_m \frac{\partial C_m}{\partial n} + V_g C_m (1-k_0) = D_s \frac{\partial C_s}{\partial n}, \tag{2}$$

where C_m and C_s are iron concentrations of the melt and the solid, respectively. V_g is growth velocity of the interface between melt and solid.

The segregation coefficients of gallium and boron were set to 0.01 and 0.8

respectively [15].

Results and discussion

Figure 2 shows heater power, fraction solidified and growth velocity as a function of time during a unidirectional-solidification process. We imposed heater power as a function of time as a process parameter in this study. The heater power was decreased at a constant rate until 400 minutes. Subsequently, the heater power was then kept constant. Finally, a fast cooling rate was set during the cooling process after the end of solidification. Solidification was started from the bottom of the crucible at 108 minutes after the start of the process, which corresponds to the time when the decrease of heater power was started. The growth rate was increased during the period of decrease of heater power, while it was decreased when the heater power was kept constant. The fraction solidified was gradually increased and finally reached unity. The whole process was completed in about six hours in this study.

Figure 3 shows the distribution of iron concentration in a solidified silicon ingot that had been cooled for one hour during the cooling process. The figure shows a vertical cross section of iron concentration in the crystal. The scale of iron concentration should be multiplied by $1x10^{10}$ cm^{-3}, therefore, the periphery of the

crystal contains order of $1x10^{15}$ cm^{-3}.

Areas with high iron concentration were formed at the top of the melt due to segregation of iron. Moreover, areas with a high concentration of iron were formed close to the crucible walls. Such areas were formed by diffusion, which occurred during solidification and cooling process. This is based on the small activation energy of iron diffusion in the solid of silicon. The center area of the ingot has a small concentration of iron after the above solidification process as shown in Fig. 3.

Figure 4 shows line profiles of iron, gallium, carbon and boron concentrations along the center of silicon crystalline in the z-direction. The initial concentrations of gallium, boron and carbon in the melt were set to $1x10^{17}$, $1x10^{16}$ and $1x10^{16}$ cm^{-3}, respectively. The iron concentration is decreased rapidly near the bottom of a crucible to the inside of the crystal and then gradually increases up to a position of 0.15 of fraction solidified due to the segregation effect of iron during the solidification process. Subsequently, the iron concentration is increased near the top of the crystal. The key point for producing highly efficient solar cells is how to reduce areas with high concentration of iron in a crystal, since iron acts as a lifetime killer of minority carriers in the crystal.

The concentration of gallium and boron increased monotonically, which is

based on the normal freezing phenomena. The calculated data are similar to those reported by [16].

4. Summary

A transient global model and code were developed for analyzing a casting process. We predicted the distribution of temperature and iron distributions as a function of time. The results showed that iron diffused even after the end of solidification, which is due to the rather small activation energy of iron in silicon. A U-shaped distribution of iron in the z-direction could be predicted by using the newly developed code, which can calculate transient phenomena of a casting process of silicon for photovoltaic devices.

Acknowledgement

This work was supported by a NEDO project, a Grant-in-Aid for Scientific Research (B) 14350010 and a grant-in-aid for the creation of innovation through business-academy-public sector cooperation from the Japanese Ministry of Education, Science, Sports and Culture.

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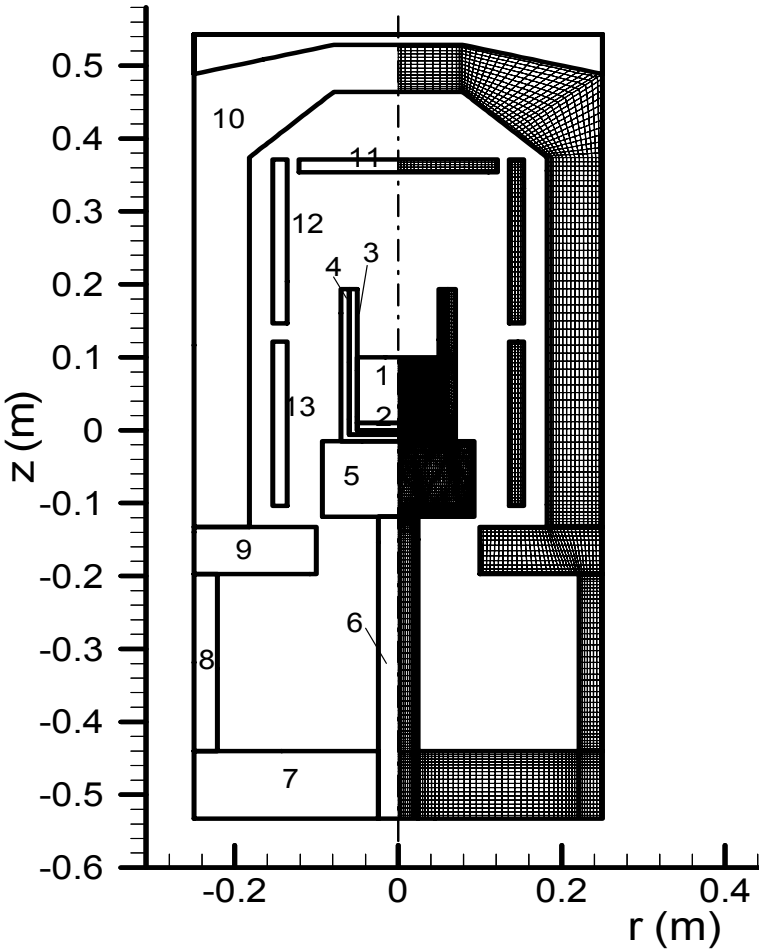
Figure captions

Fig. 1. Configuration and computation grid of a casting furnace. The melt, a crystal, a crucible and a pedestal are denoted as 1, 2, 3, 4, 5 and 6, respectively. Thermal shields are labeled as 7 to 11. The number of 12 and 13 show multi heater.

Fig. 2. Heater power, solid fraction and solidification rate as a function of time during the casting process.

Fig. 3. Distribution of iron concentration in a solidified silicon ingot after the solidification process. The scale of iron concentration should be multiplied by $1x10^{10}$ cm^{-3}. The periphery of the crystal contains order of $1x10^{15}$ cm^{-3}.

Fig. 4. A log-log plot of iron, gallium, carbon and boron concentrations at a center of a crucible in the z-direction.


0.5
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0.2
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-0.2
-0.3
-0.4
-0.5
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z (m)
-0.2
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0.2
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r (m)
10
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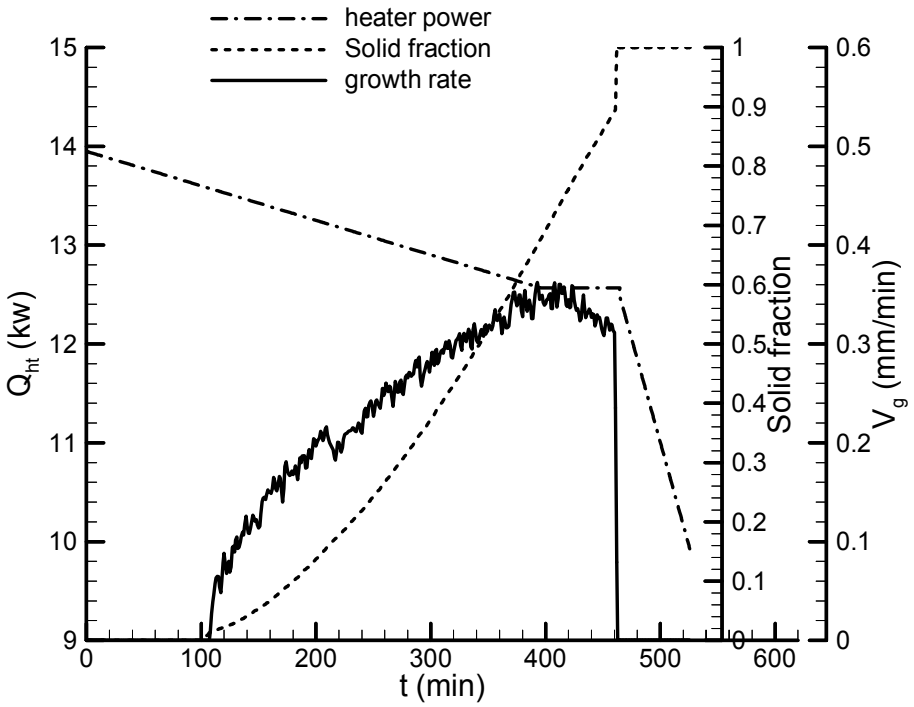
7

Fig. 1


heater power
Solid fraction
growth rate
15
14
13
12
11
10
9
Q_{ht} (kw)
0
100
200
300
400
500
600
t (min)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Solid fraction
0.6
0.5
0.4
0.3
0.2
0.1
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V_g (mm/min)

Fig. 2

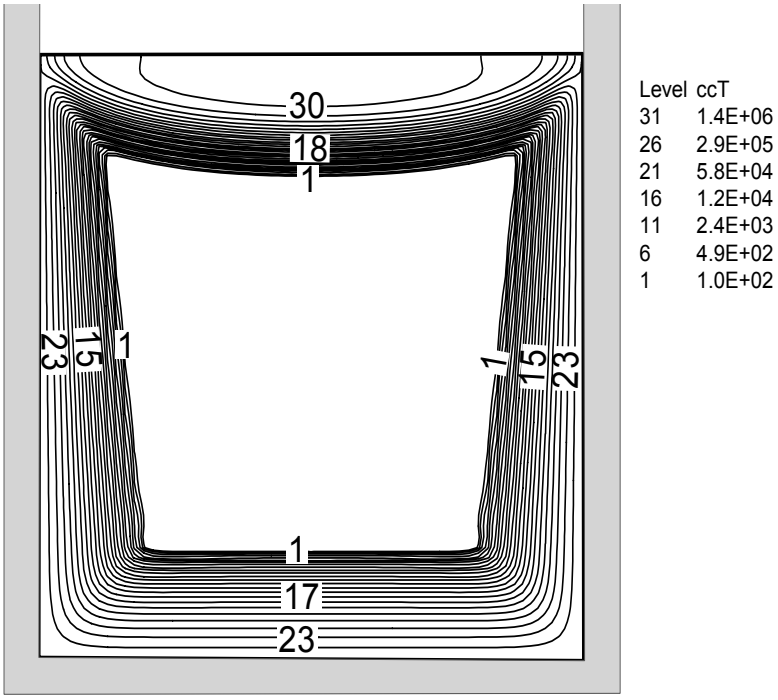
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Fig. 3

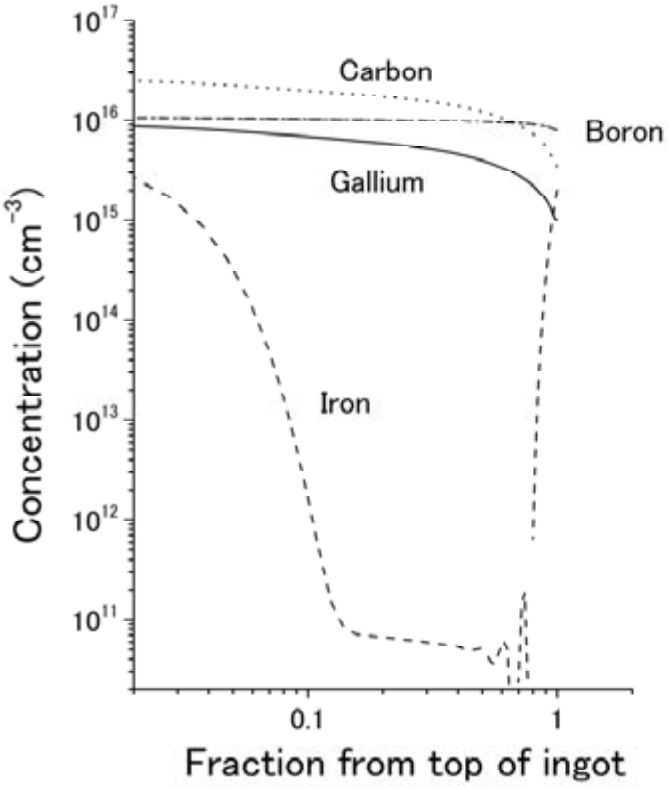
Carbon
Boron
Gallium
Iron
Concentration (cm^{-3})
10^{17}
10^{16}
10^{15}
10^{14}
10^{13}
10^{12}
10^{11}
0.1
1
Fraction from top of ingot

Fig. 4

Solar Advisor Model (SAM) Overview

David Mooney, Mark Mehos, Nate Blair, Craig Christensen, Steve Janzou, and Paul Gilman

A comprehensive solar technology systems analysis model is being developed to support program planning and the Solar America Initiative for the U.S. Department of Energy's Solar Energy Technologies Program's (SETP). This model calculates the costs, financing, and performance of current solar technologies systems including photovoltaics, concentrating solar power, and solar heat (typically solar domestic hot water). The primary function of the model is to allow users to investigate the impact of variations in physical, cost, and financial parameters to better understand their impact on key figures of merit including the levelized cost of energy over a system's lifetime.

A central idea for SAM is to have a user-friendly interface while at the same time having a detailed, accurate analysis for each of the technologies in each of the areas of cost, financing, and performance. The underlying performance engine, which is transparent to the user, is TRNSYS, which already contains an extensive library of solar technology models. SAM also has built-in cost models, or, the user can access their own spreadsheet-based cost models that can automatically interface with SAM. The financial model is an extension of an existing validated finance model.

This presentation will discuss the goals and implementation of the model, SAM's role in the Solar America Initiative, and present several sample results for interesting sensitivities.

The National Center for Photovoltaics Process Integration Project

Brent Nelson, Steven Robbins, Qi Wang, and Peter Sheldon
National Center for Photovoltaics, National Renewable Energy Laboratory (NREL),
Golden, CO 80401-3393, USA, brent_nelson@nrel.gov

ABSTRACT

The purpose of the process integration project of the National Center for Photovoltaics (NCPV) is to develop an infrastructure that will allow researchers to gain new knowledge that is difficult—if not impossible—to obtain with existing equipment. This difficulty is due, in part, to the state of our existing tool set, which lacks sufficient in-situ or real-time measurement capabilities, or lacks access to analytical tools where the sample remains in a controlled environment between deposition and processing or measurement. This new infrastructure will provide flexible and robust integration of deposition, processing (etching, annealing, etc.), and characterization tools via a standardized transfer interface such that samples move between tools in a controlled ambient. This facilitates the integration of new materials and processing into existing device structures as well as characterization of layer and interface properties within a device. Ultimately, this synergistic effort between NREL staff, universities, and the photovoltaic (PV) industry—around an integrated tool base—will add to the PV knowledge base and help move many PV technologies forward.

1. Objectives

We will achieve the purpose stated above by building a collection of integrated deposition, characterization, and processing tools. These integration standards must be flexible to allow for changing research needs, yet be robust and reliable. Deposition tools must be able to deposit uniformly and reproducibly over areas that are large enough to be meaningful to industry and be able to handle a wide variety of sample substrates. The benefits of having integrated tools include allowing researchers to:

- Answer previously inaccessible research questions.
- Control and characterize critical surfaces and assess the impact of these interfaces on subsequent layers.
- Assess process-related source chemistry, surface chemistry and kinetics, and bulk reconstruction.
- Grow layers and alter interfaces using controlled transfer ambients (without exposure to air).
- Develop new techniques, methodologies, device structures, materials, and processes.
- Develop new characterization techniques, try new applications for analytical equipment, and incorporate more in-situ and real-time analysis.
- More effectively collaborate with university and industrial researchers.

2. Technical Approach

Individual deposition, processing, and characterization techniques will be integrated via one of several different modes[1]. Ideally, characterization techniques will be used for real-time analysis of deposition and processing techniques. The next best solution is in-situ diagnostics (in the original place, but not real-time data). When neither of these integration methods is possible, techniques will be integrated by transferring samples from one location to another either via intra-tool or inter-tool sample transport. See Figure 1 for a summary of the various integration approaches as they relate to the characterization of materials and interfaces. *Intra-tool* transport is the movement of samples between techniques within the same set of interconnected chambers, that is, a cluster tool. Initial cluster tools will use robotic transfers. *Inter-tool* transport is the movement of samples between techniques where those techniques do not share direct connection. These techniques could be in a stand-alone tool or a part of a cluster tool. The sample is moved from one tool into the pod, which is sealed and disconnected from that tool before being wheeled to another tool, where the process is reversed. See Figure 2 for a summary of the ways chambers can be integrated. The transfer ambient within the pod can be either an atmosphere of ultra-high-purity inert gas or high vacuum.

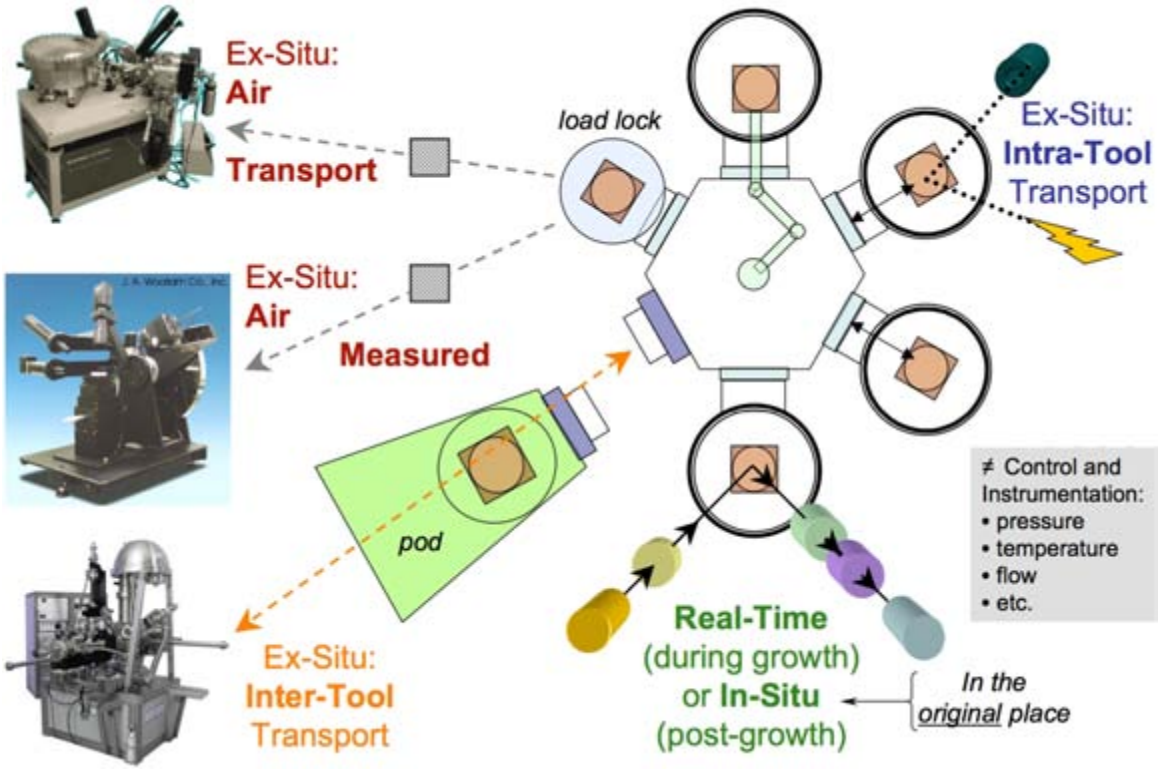

Figure 1: Sample Integration for various types of measurements.

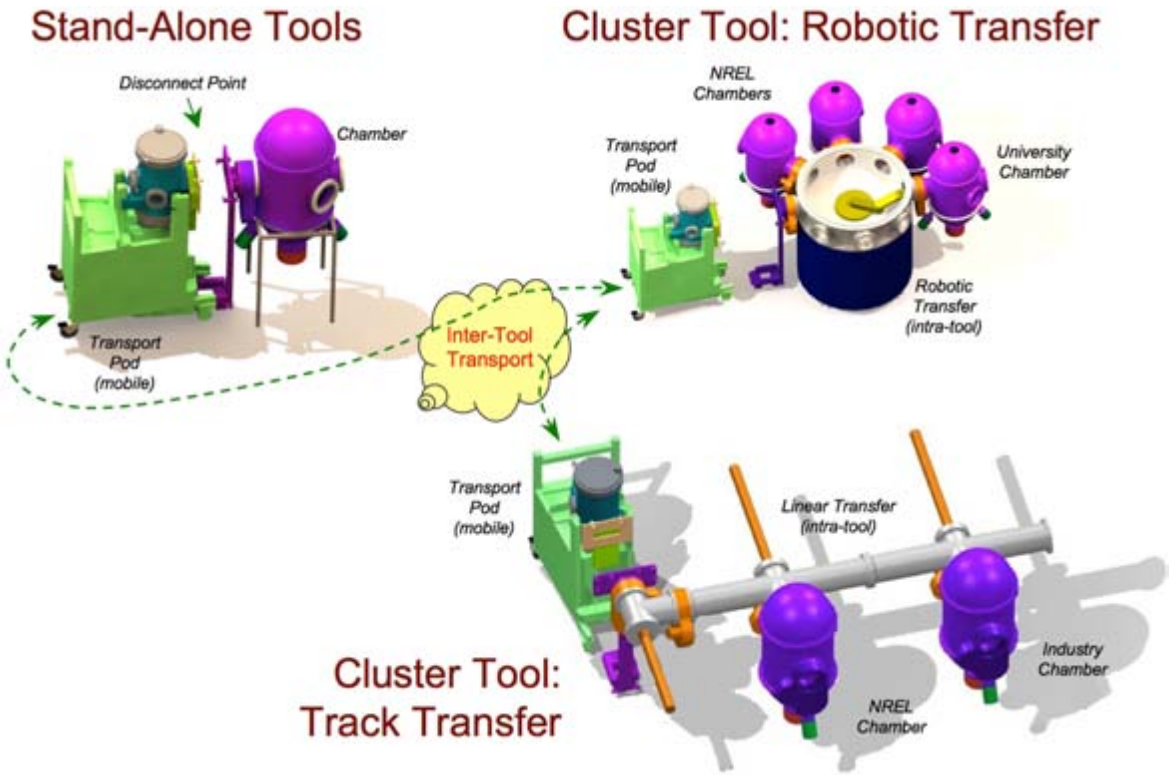

Figure 2: Chamber integration for various types of sample transfers.

This integration via a controlled ambient container is similar to the Standard Mechanical InterFace (SMIF) used by the integrated-circuit (IC) industry to enclose and transport wafers between 200-mm tools or the newer Front-Opening Unified Pods (FOUP) used on 300-mm tools. One of the keys to the success of the IC industry was the creation of these mini-environments, in which the industry significantly reduced the contamination of wafers between processing steps[2]. While SMIFs and FOUPs are typically operated with particulate free, dry air—as particulates are their main device killer—our initial pods will operate under high vacuum using a battery powered ion pump. This will also us to control exposure of materials or interfaces to air that may react with oxygen or water vapor.

The main design goals of the NCPV Process Integration project are to:

- Develop a standard sample transport between tools
- Ensure the sample transport mechanism is robust
- Control the ambient of that sample transfer
- Be able to deposit uniformly and reproducibly over areas large enough to be meaningful to industry
- Handle a wide variety of sample substrates
- Standardize control and data logging software
- Integrate as many techniques as practical[3]

To integrate a diverse tool set requires a "universal" maximum substrate size and shape to be held in a platen. The platen drives the requirements for the entire design. Agreement by the various groups within the NCPV have set the maximum substrate size the platen can handle to be 157 mm x 157 mm (approximately 6" x 6"). This size was primarily chosen because it supports the silicon photovoltaic industry (having a "6-inch square" protocol in mult-crystalline and a "6-inch round" protocol in single crystalline). However, this size also more than adequately supports the other technological areas studied by the NCPV as it's a size that is technologically relevant to thin-film manufactures. It's not so small as to be considered "research only" and yet large enough that mini-modules could be constructed from devices on this scale. While 6" x 6" is larger than almost all our existing tools can accommodate, basic science can still be done on this form factor while some of the more applied and integrated investigations cannot be on a smaller scale. Various platen designs will accommodate a variety of substrates, such as soda-lime or high-temperature glass, crystalline wafers, foils, ceramic, or other exotic materials.

3. Progress and Status

The development of these integrated tools is a multi-year project. We have received our first inter-tool transport pod as well as the first standalone chamber, which is a sputtering chamber for the development of new transparent conducting oxides (TCOs). The use of the inter-tool transport pod between this tool and the first cluster tool—described below—will allow us to test and improve our pod design features.

The silicon group will operate the first cluster tool that will arrive to NREL in September of 2006. This tool consists of a central transfer chamber with robotic intra-tool transport and ten ports as illustrated in Figure 3. This will serve as the project's first test for intra-tool transport having internal transfer zone containing a vacuum robot. There are five chambers for various types of chemical vapor deposition of thin-film, silicon-based depositions. Three of these chambers are equipped with elaborate mechanisms for combinatorial depositions [4]. This tool has many purposes. It will facilitate the development of SiN passivation layers for multi-crystalline devices. It will allow the integration of thin-film layers with crystalline silicon structures; for example, for improving the performance and understanding of heterojunction solar cells. It also has full amorphous silicon device deposition capabilities, including the ability to deposit TCOs without exposure to air between any of the steps. One port is for a load lock and another has the dock for the inter-tool transport pod. Finally, there is an open port where we can add a future chamber for analytical capabilities via intra-tool transport. This could be an Auger Electron Spectroscopy system or other analysis technique.

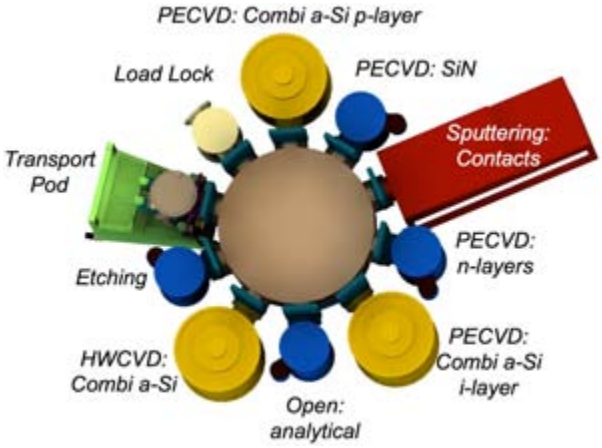

Figure 3: Schematic of the silicon cluster tool.

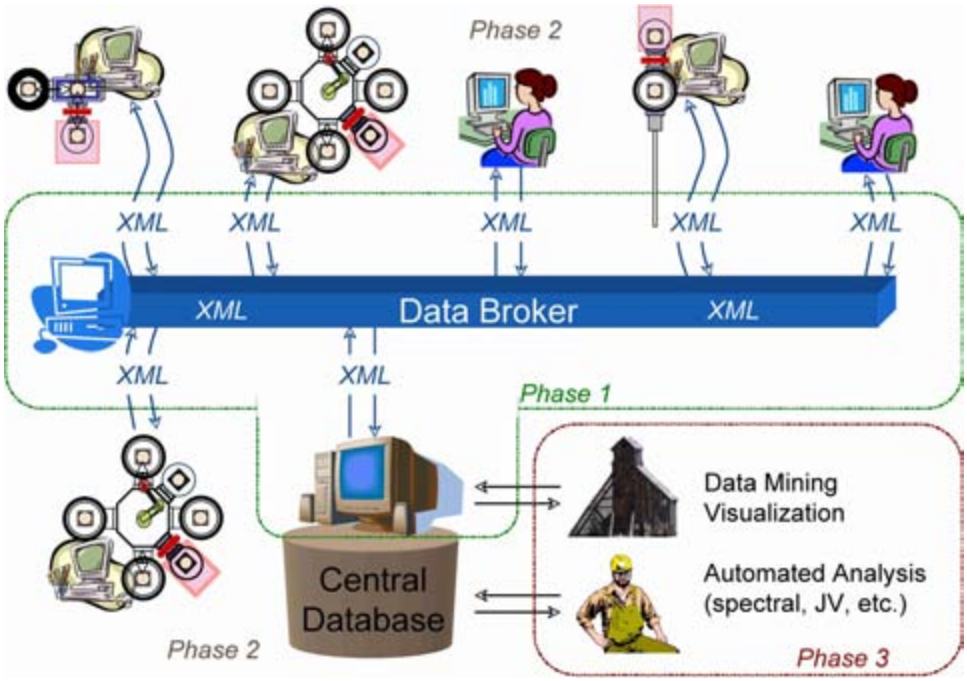

Figure 4: Schema for software integration.

We are collaborating with the Manufacturing Research Center at Georgia Tech to develop the use of recipe/run control, as well as data logging, using XML-based data transfer schema[5] (Figure 4). It basically shows that an operator can send a recipe from their computer to a tool, the tool can process that recipe and perform the experiment accordingly, and any data logging can be fed back to a central database. Software is critical to having fully integrated tools, not only for automation, but for easy access to the data out of which information can be gleaned and knowledge built. Ultimately the ability to glean meaning out of the data will require more sophisticated data mining and visualization technology. This is being developed in collaboration with NREL's Scientific Computing Center. Of course, this will all be done with appropriate firewalls and security to protect intellectual property and proprietary data.

4. Conclusions

We have achieved remarkable consent from individuals with a diverse spectrum of research interests in the development of these process-integration standards. We are progressing toward our goal of having integrated hardware, integrated software, and having the right people working around those tools to answer the most important questions. Our first generation of tool will allow us to refine the integration standards as we use our sample transport schemes so that future generations are not only compatible but help us perform research with higher quality data and with more rapid throughput.

ACKNOWLEDGEMENTS

This work is supported by the U.S. DOE under Contract No. DE-AC36-99GO10337. The authors wish to thank the entire NCPV for their support and encouragement in this project and the many industrial collaborators too numerous to cite.

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PV Manufacturing Initiative at Georgia Tech

S. Danyluk, S. Melkote, A. Dugenske, D. Furbush, F. Li, X. Brun, V. Garcia

Georgia Institute of Technology
Manufacturing Research Center and the
George W. Woodruff School of Mechanical Engineering

1 Introduction

Georgia Tech is currently working under an NREL contract on manufacturing issues in PV panel production. Part of this activity involves close cooperation with industrial groups in the automation, handling, inspection and factory information systems for the use of large thin wafers. Two workshops have been held at Georgia Tech; PV cell manufacturers and PV equipment (tool) manufacturers contributed to prioritization of research topics and some have committed resources to this activity. This paper summarizes the equipment vendor workshop results and presents two technical topics of particular significance to PV panel manufacturing: Bernoulli gripping and the deformation of thin wafers, and the CAMX Information software for control of PV manufacturing equipment.

2 Workshop Summaries

Two independent workshops were held at Georgia Tech: on October 12, 2004 and February 2, 2005. The 2004 workshop included the cell manufacturers, RWE Schott, Evergreen, and BP Solar. The 2005 workshop included some select equipment manufacturers. In each case, the participants were asked to rank order the challenges for the next generation cells and panels. The outcome of the vendor workshop survey is shown in Table 1.

Equipment Vendor
1 Wafer Assembly Stress Management
2 Cracks in Wafers
3 Air Conveyors
4 Robot Transfer Forces
5 Belt Transfer
10 Wafer Stress Management
14 Factory Communication

Table 1. Rank Order of Research/Development Priorities

The Georgia Tech initiative has addressed many of these priority research items in a laboratory testbed, shown in Figure 1. A portion of the testbed consists of a pick and place station using various grippers, and a transport and residual stress inspection system.

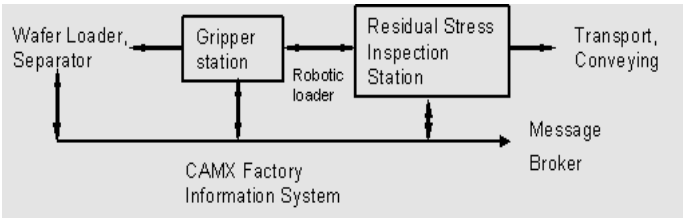


Figure 1. A portion of the testbed

The next section describes some key elements of the Bernoulli gripper results and the CAMX Factory Information System.

Bernoulli Gripper Results

Bernoulli grippers operate on the principle that a controlled air flow in the vicinity of solid surface creates a vacuum above the surface. As the surface (wafer) is drawn to the gripper, the surfaces of the wafer and gripper are separated by rubber standoffs.

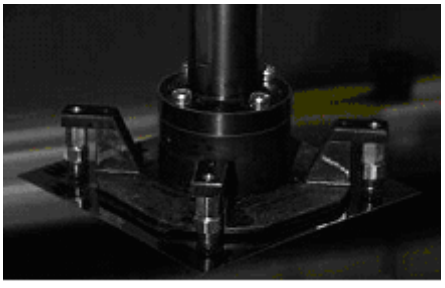
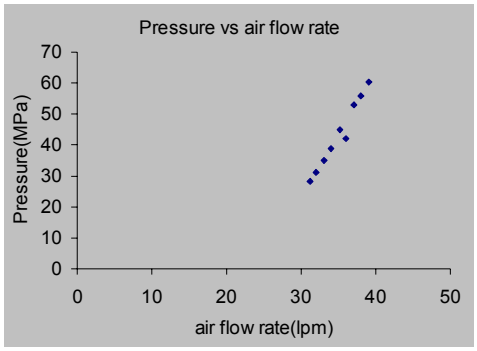


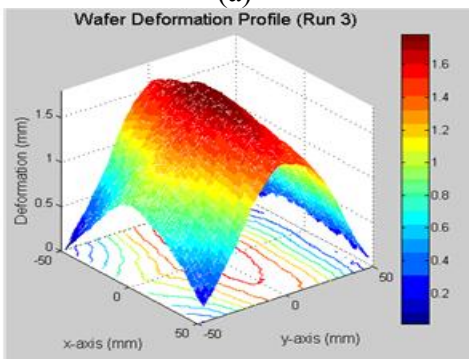
Figure 2. Bernoulli gripper

Bernoulli grippers are particularly useful in handling thin wafers since the vacuum forces can be easily controlled, on-the-fly, by the control of the air flow. Pick-up-forces can be adjusted for wafer thickness, residual stresses, transport distances, etc. Figure 3 shows a typical result of the vacuum

pressures, vs. air flow, and deflections for 150 µm thick 4 x 4 inch wafers.



(a)



(b)

Figure 3. (a) Pressure vs. air flow rate
(b) Deformation of a 150µm, 4×4 inch wafer

CAMX Factory Information System

The yield, efficiency and the eventual cost of PV panels will be linked to the manipulation and control of the process tools, and the monitoring of the tool process parameters. We are currently using an XML-based factory information system, CAMX, computer-aided manufacturing using XML to control and monitor the testbed. CAMX makes use of a virtual message broker which exchanges XML messages between tools and a centralized server over the internet. Figure 4 shows the software architecture for the CAMX system as related to the residual stress wafer inspection station.

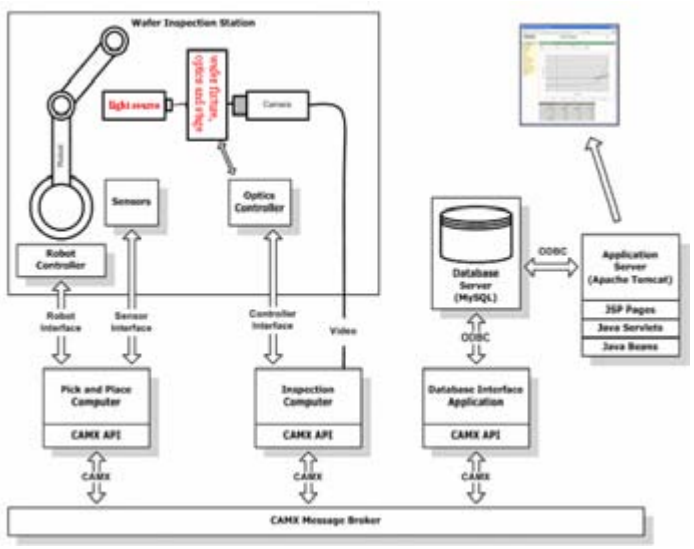


Figure 4. Software architecture for the CAMX system

The CAMX message broker controls the robot and sensor interfaces, compiles a database and prepares a report.

3 Conclusions

The Georgia Tech PV Manufacturing Initiative is addressing some of the top priority items identified by two industrial group workshops in the handling, transport and inspection of large thin wafers. A web-based control and monitoring factory information system, CAMX, has been implemented.

4 Acknowledgements

This project is supported by NREL under control #B01-6D0. The authors appreciate the support of Dr. Rick Matson in this effort.

Fundamental interactions involving Fe in silicon

Mahdi Sanati and Stefan K. Estreicher

Physics Department, Texas Tech University, Lubbock, TX 79409-1051

Abstract: Ongoing theoretical research deals with the fundamental interactions between interstitial Fe and a variety of simple defects (vacancy and self-interstitial) and impurities (hydrogen, oxygen, carbon, iron, shallow acceptors) in crystalline Si. We present here preliminary results of these calculations.

1. Introduction

Iron is a common transition metal contaminant in Si. It is known to diffuse as an interstitial at low to moderate temperatures, to form pairs with shallow acceptors, and to precipitate at or near oxides, grain boundaries, or dislocations. The properties of Fe in Si have been the topic of several recent reviews [1,2]. Yet, little is known about the basic chemistry of Fe in Si, in particular the interactions between interstitial iron and isolated impurities and native defects.

Some Fe is always present in the as-grown material, and the impurity is often inadvertently added during various processing steps. Fe and the complexes it forms are electrically active and reduce minority carrier concentrations and lifetimes. Despite decades of studies, very little if any information exists on the fundamental interactions involving Fe and isolated native defects or isolated impurities. Thus, with exception of iron-acceptor pairs [2], the basic chemistry of Fe in Si is not known. The few experimental data of microscopic nature which can lead to the structural identification of simple Fe complexes in Si come from photoluminescence (PL) [3,4]. While PL bands are notoriously difficult to calculate from first principles, the phonon replicas often associated with the zero-phonon line (zpl) can be used to identify specific defects [5,6].

In this paper, we present preliminary results of first-principles calculations involving interstitial Fe and native defects and impurities in Si. We predict stable and metastable configurations, energetics, spin states, and vibrational spectra. Calculations of the (approximate) position of electrically-active gap levels will be performed at a later time, when an appropriate marker [7] will be identified.

2. Theoretical background

Most of our results were obtained with first-principles, self-consistent density functional theory coupled to molecular-dynamics simulations, as implemented in the SIESTA package [8]. The host crystal is represented by periodic 64-host atom supercells. The *k*-points sampling is a 2×2×2 Monkhorst-Pack [9] mesh. All the calculations were performed within the generalized gradient approximation for the exchange-correlation potential as parameterized by Perdew, Burke and Ernzherof [10]. In these calculations we use standard norm-conserving pseudopotentials generated according to the procedure of Troullier and Martins [11]. The partial-core correction for nonlinear exchange-correlation [12] for Fe has been included. The basis sets for the valence states are (numerical) linear combination of atomic orbitals. We used double-zeta basis sets for the first two row elements (H, B, C, O) and added a set of polarization functions for the heavier elements (Si, Al, Fe, Ga).

The geometries of the various defect complexes were optimized using conjugate gradients with a maximum force component tolerance of 0.005eV/Å. The energies of the final configurations

were compared to those of the dissociated species to get binding energies. The vibrational spectra were obtained from dynamical matrices calculated in the frozen-phonon approximation.

3. Results

Our calculations include interstitial iron (Fe_i), its interactions with a vacancy ($Fe_i + V \rightarrow Fe_s$) and a self-interstitial ($Fe_i + I \rightarrow \{Fe_i,I\}$) as well as with common impurities such shallow acceptors, C, O, another Fe, and H. We are calculating stable and metastable configurations, binding energies, spin states and, for the stable complexes, complete vibrational spectra. Future calculations will involve estimates of the electrical activity of the various Fe-related complexes. Preliminary results are discussed below.

Interstitial iron:

As expected, we find Fe_i^+ to be stable at the tetrahedral interstitial (T) site in the spin 3/2 state (the spin 1/2 state is 0.22eV higher in energy). An upper limit to the activation energy for diffusion of Fe_i^+ was obtained by assuming that the diffusion occurs when Fe jumps from T to T site through the hexagonal interstitial site. This barrier was found to be 0.58eV, slightly lower but consistent with the diffusivity of iron in Si [2], $1.3 \cdot 10^{-3}$ exp{-0.68eV/k_BT} cm^2/s.

Fe_i interactions with the vacancy and the self-interstitial:

When $^{3/2}Fe_i^+$ encounters a pre-existing vacancy V^0, it becomes substitutional $^{3/2}Fe_s^+$ with a gain in energy of 2.28eV. However, an additional 0.22eV is gained when a spin flips and $^{3/2}Fe_s^+$ becomes $^{1/2}Fe_s^+$. In the neutral charge state, $^1Fe_i^0 + V^0 \rightarrow {}^1Fe_s^0$ provides a comparable 2.54eV gain in energy. Then, an additional 0.38eV is gained when a spin flips and $^1Fe_s^0$ becomes $^0Fe_s^0$. Note that the energy gain in Fe_i-vacancy interactions is comparable to that predicted for Cu_i-vacancy interactions [13].

Interstitial iron also strongly interacts with the Si self-interstitial: $^1Fe_i^0 + I^0 \rightarrow {}^{1\{}Fe_i,I\}^0 + 1.00eV$. The complex is shown below. This is again very similar to the Cu_i+I situation. This large binding energy contrasts with the very small numbers we find for Fe_i-O_i interactions (to be discussed elsewhere). This suggests that Fe does not trap *at* oxides but at the self-interstitials that are created when oxygen precipitates.

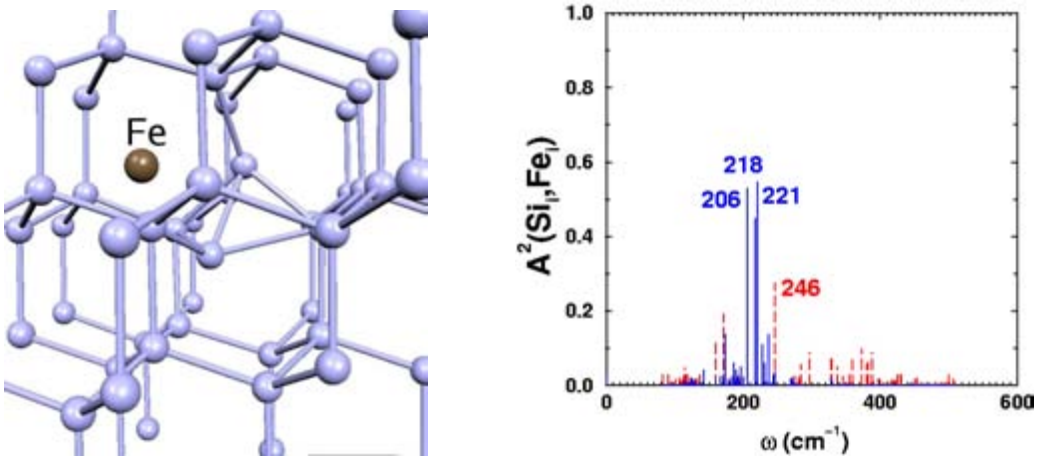


Fig. 1: Interstitial Fe easily traps at a Si self-interstitial (left). Several Fe (solid blue lines) and Si (dashed red lines) related pseudoLVMs (right) are characteristic of this complex.

Fe-acceptor pairs:
Iron forms pairs with shallow acceptors in Si. The experimental situation has been reviewed recently [2]. We have considered here the reactions $^{3/2}Fe_i^+ + X^- \rightarrow {}^{3/2}\{Fe_i,X\}^0$ where X is B, Al, or Ga. The $^{1/2}\{Fe_i,X\}^0$ state is about 0.2 to 0.4eV higher than the $^{3/2}\{Fe_i,X\}^0$ state. The predicted binding energies involve comparing the total energies of two charged supercells ($Si_{64}Fe_i^+$ and $Si_{63}X^-$) to those of neutral cells ($Si_{63}FeX$ and Si_{64}). This is a problem since the (unknown) Madelung energy correction needed when considering charged supercells is missing twice on one side of the equation. We have yet to resolve this issue, and therefore our binding energies have an error bar that could be as large as ~0.3eV (see e.g. Ref. 14). Indeed, our binding energies are 0.31, 0.37, and 0.24eV for B, Al, and Ga, respectively. There is little if any covalent interaction between Fe and the shallow acceptor, and the binding results almost exclusively from the Coulomb interaction between Fe_i^+ and X^-. This suggests that the correct binding energies should be of the order of 0.5eV. Ongoing calculations in 128 and 216 atom cells confirm that the binding energies increase with the size of the supercell.

We find two possible configurations for each {Fe,X} pair, a fact we tentatively attribute to the size of the acceptor. One of them has trigonal symmetry (Fig. 2, left) with Si-X···Fe aligned along the same <111> axis, and the other orthorhombic symmetry (Fig. 2, right) with Fe off along the <100> direction. In the case of B, the stable pair is trigonal, and the orthorhombic configuration has a very small binding energy (0.07eV). In the case of Al and Ga, the orthorhombic structure is more stable, albeit by only 0.02eV for Al and 0.06eV for Ga. Note that the relative energies of the two metastable configurations involve the comparison of two electrically neutral supercells, and these values are reliable. The vibrational spectra of the {Fe,B} pair shows that the B modes are perturbed by Fe. In the case of Al and Ga, only weakly localized pseudolocal modes exist. More details about this will be published later.

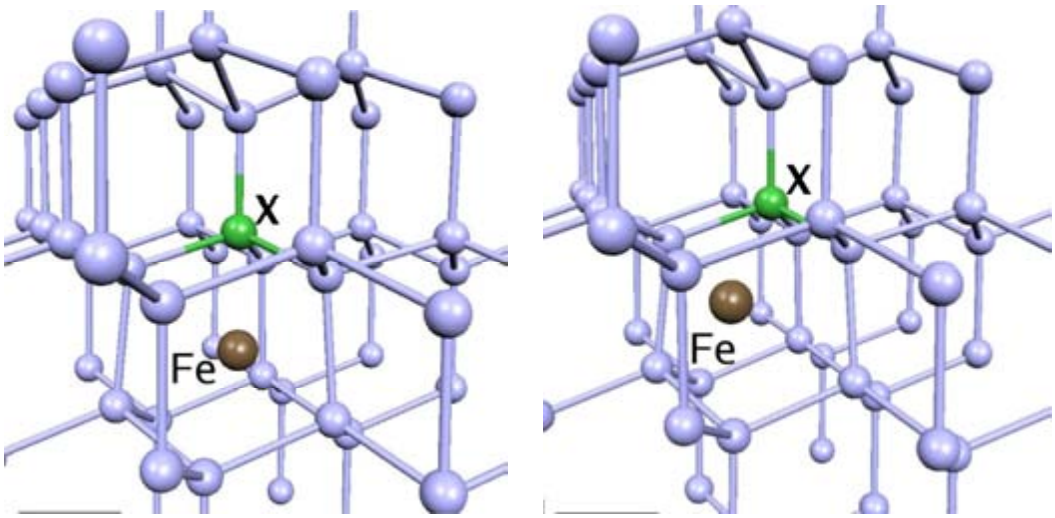


Fig. 2: Fe_i^+ traps at shallow acceptors (X = B^-, Al^-, or Ga^-) and forms either a trigonal (left) or tetragonal (right) complex. The relative energies of the <111> and <110> pairs vary with X.

4. Summary
Interstitial iron in Si interacts strongly with pre-existing vacancies and self-interstitials. Fe_i also interacts with Fe_s, and the $\{Fe_i,Fe_s\}$ pair has a stable trigonal configuration and a metastable orthorhombic one. Fe_i also forms metastable pairs with shallow acceptors. In contrast, Fe_i

interacts very weakly, if at all, with oxygen or carbon in Si. More details on this and other features of the chemistry of Fe in Si will be published elsewhere.

Acknowledgements
This work is supported in part by a contract from NREL and a grant from the R.A. Welch Foundation.

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IMPACT OF MO AND FE ON MULTICRYSTALLINE FLOAT ZONE SILICON SOLAR CELLS

G. Coletti[1], L. J. Geerligs[1], P. Manshanden[1], S. Riepe[2], W. Warta[2], J. Arumughan[3], R. Kopecek[3]
Tel.: +31 224 564382 Email: coletti@ecn.nl

[1] ECN Energy research Centre of the Netherlands, Solar Energy, Westerduinweg 3, NL 1755 LE Petten, the Netherlands
[2] Fraunhofer ISE, Heidenhofstr. 2, 79110 Freiburg, Germany
[3] University of Konstanz, Faculty of Sciences, Department of Physics, Jakob-Burckhardt-Str. 27, 78464 Konstanz, Germany

ABSTRACT: The aim of this work is to provide an updated reference of the incorporation and the impact of impurities on solar cells performance in the current process technology for monocrystalline and multicrystalline silicon (Si) wafers. Molybdenum (Mo) and iron (Fe) are introduced in the Si melt from which Float Zone (FZ) ingots are crystallised. The impurity concentration in the feedstock ranges from 2.6 to 900 ppma for Fe and from 25 to 2800 ppma for Mo. A major drop in Voc and IQE is visible for samples with the highest Mo level. Fe results in different behaviour in mono and multicrystalline FZ Si wafers. In monocrystalline wafers the solar cell process is able to largely remove the Fe from the Si-bulk for concentrations up to 54 ppma. In multicrystalline Si, for all the Fe-impurity levels investigated, the results are equivalent and comparable to the worst results obtained for industrial directionally solidified mc-Si reference wafers.

1 INTRODUCTION

At the moment, the PhotoVoltaic (PV) industry is facing a shortage in silicon feedstock. This has led to a steady introduction of less pure silicon. Also, it is expected that SOlar Grade silicon (SoG-Si) made through the direct- or metallurgical purification route will become available on the market soon. Therefore, the PV industry should address the question how cell processes can be best adapted to less pure material, one of the topics of this study.

In this work we study the role of iron and molybdenum when intentionally introduced in a silicon melt before the crystallisation. The choice for these two elements is based on their known importance as a contaminant in wafers [1], and the fact that their physical properties are quite different [2]. The impact of the contaminants during industrial solar cells processing will be shown and analysed.

Some of this work is similar to the research performed in the 1980's by Westinghouse Corp [3]. Those results are still used as reference for the effect of impurities on the solar cell performance. However, those results were obtained with cell processing technology of the 1980's, and mostly on monocrystalline material. We expect additional and essential information from the comparison between multicrystalline and monocrystalline Si wafers.

The aim of this work is to provide an updated reference for the role of particular impurities in the current cell process technology for multicrystalline and monocrystalline silicon wafers.

2 APPROACH

The best way to investigate the impact of specific metal contaminants is to intentionally contaminate the material with a well-defined impurity concentration. At the same time the concentrations of other impurities should be kept as low as possible. In this experiment interactions with carbon and oxygen will not be considered since it complicates analysis of results.

Clean material can be most conveniently obtained by producing FZ ingots. FZ ingots can be grown from a multicrystalline seed, resulting in a multicrystalline ingot with a range of crystal sizes. The crystal structure and the temperature history are not necessarily comparable to industrial directionally solidified (DS) multicrystalline silicon (mc-Si). However, varying the thermal history of FZ silicon and understanding its effects, will also improve the knowledge of the industrial mc-Si.

Unintentional contamination is most unlikely in the FZ growth technique, in contrast to small scale DS-Si. This is a big advantage, which was decisive in our choice for the method.

The other advantage of the FZ approach is the possibility for comparison between monocrystalline and multicrystalline material. This permits to study the incorporation and impact of impurities when present together with crystal defects.

2.1 Choice of the impurities

The impurities used for investigation in this work are iron and molybdenum. Fe is a dominant metal impurity in silicon wafers. It is a relatively fast diffusing impurity, thus it can be gettered. The diffusivity of Mo is not exactly known, but it is not a fast diffusing impurity [2]. Therefore precipitation and gettering are expected to be significantly different. Mo is not present in similar levels as Fe in silicon wafers but it is very detrimental for the lifetime. It has been detected in cast mc-Si by neutron activation analysis [1].

2.2 Material

Fourteen FZ ingots were grown, introducing three different concentrations of Mo and Fe and growing both monocrystalline and multicrystalline structures. Two reference ingots were grown without added impurities.

Impurity / Cont. level	Mo		Fe	
	Mono	Multi	Mono	Multi
1	25		2.6	
2	240		54	
3	2800		860	

Table I: Impurities added in the silicon melt in ppma.

The amount of impurity introduced is reported in Table I. Those ranges have been estimated targeting typical value of Mo and Fe in mc-Si [1]. The crystal solidification velocity varied between 1 and 2 mm/min.

The ingots were boron doped with a base resistivity of ~0.8 Ω·cm for the Fe-contaminated ingots and ~1.7 Ω·cm for the Mo

ones. The ingot diameter was 40 mm. All ingots were grown with pedestal growth technique at IKZ Berlin.

After crystallisation the ingots suffer from residual stress. Thus it was not possible to wafer some of them before relaxing the stress by a thermal annealing. Monocrystalline Mo-doped samples could, so far, not be processed because the ingots were too fragile before annealing. In the case of Iron samples of both monocrystalline and multicrystalline wafers were characterised and processed.

In this work we present first results, from non-annealed ingots only. The reference FZ ingots have not been processed yet. So far, industrial DS mc-Si was used as reference.

2.3 Cell process

The solar cell process was a standard industrial firing through SiN_x process. The wafers received an alkaline saw-damage etch, a phosphorous diffusion in a belt furnace, and a remote plasma-enhanced CVD of SiNx at ECN. The SiNx is optimised for multicrystalline Si wafers in order to obtain a good anti-reflective coating as well as bulk- and surface-passivation properties at the same time. The screen-printed metallisation and co-firing was carried out at the University of Konstanz. The solar cells were then cut to 2x2 cm^2. The solar cell efficiency on reference DS mc-Si was about 15%. The solar cell results are summarised in section 4.

3 LIFETIME MEASUREMENTS AND INTERPRETATION

The as-grown wafers received chemical polishing and a PECVD SiNx deposition to passivate the surface in order to measure the bulk recombination lifetime.

	Mo [µs]		Fe [µs]	
	Mono	Multi	Mono	Multi
1	n/a	3.6	5.3	2.7
2	n/a	2.3	0.7	n/a
3	n/a	0.5	n/a	0.3

Table II: QSS-PC lifetime @ $\Delta n=1\times10^{15}cm^{-3}$. n/a means ingot could not be sawn before anneal due to stress.

In Table II the lifetime as measured with the QSS-PC is shown. The lifetime is quite low for all the wafers, and decreases with increase of both Mo and Fe concentrations, indicating the dominant impact of the impurities. The lifetime of the monocrystalline sample is higher than that of the multicrystalline sample with the same melt doping.

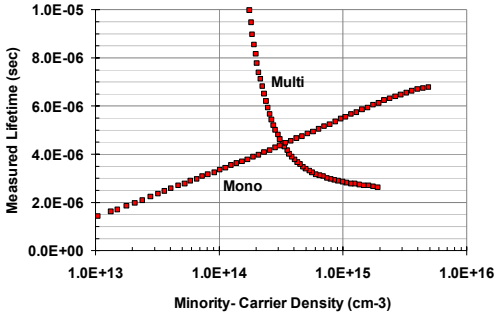

Figure 1: Effective lifetime as a function of minority carrier concentration for mono and multicrystalline samples with the lowest level of Fe.

The QSS-PC lifetime consistently shows trapping [4] for both the iron and molybdenum-doped mc-Si. In Fig. 1, as an example, the τ_{eff} versus Δn is reported of the samples with the lowest amount of Fe. A higher apparent lifetime is visible for the mc-Si sample at low injection level. It is otherwise clearly visible that no trapping is present in the case of monocrystalline samples.

Therefore, the trapping seems to be directly related to the grain boundaries or decoration thereof, rather than to just the presence of either Fe or Mo.

3.1 Modelling

To interpret the lifetime variation shown in Table II a simple model is adopted. The aim is to analyse the relationship between the impurities intentionally introduced and the lifetime obtained.

The effective lifetime can be modelled using Shockley-Read-Hall theory:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{other}} + \frac{1}{\tau_{SRH}} = a + b \cdot N_t \qquad (1)$$

$1/\tau_{SRH}$ is the recombination due to defects created by the contamination with impurity (Fe or Mo). $1/\tau_{SRH}$ is proportional to the density of such defects (N_t). $1/\tau_{other}$ is the recombination not linearly related to the concentration of the added impurity. $1/\tau_{other}$ may still be related to the presence of the impurities but it is not a function of their concentration.

We hypothesize that N_t is proportional to the amount of impurity introduced (Conc.) in the melt

$$\frac{1}{\tau_{eff}} = a + b \cdot k \cdot Conc \qquad (2)$$

N_t could e.g. be related to point defects or small homogeneously nucleated precipitates.

In Fig. 2 the inverse effective lifetime is shown as a function of Mo concentration (open squares). The figure shows a striking linearity between the inverse effective lifetime and the Mo concentration. The concentration of the defects N_t and the Mo concentration are proportional. There is not yet enough data to verify whether this holds for Fe, too.

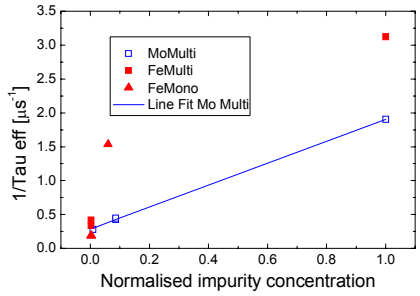

Figure 2: Inverse effective lifetime as function of impurity concentration. The impurity concentration is normalised to the highest introduced (see table I).

Concentrations of interstitial iron (Fe_i) were calculated from lifetime measurements [5] and are shown in Table III. These measurements are hard to do accurately for high iron concentrations, and the level in sample 3 is very uncertain.

	Fe in melt [cm^{-3}]	Fe_i [cm^{-3}]	
		Mono	Multi
1	5×10^{17}	6×10^{12}	7×10^{12}
2	1×10^{19}	4×10^{13}	
3	2×10^{20}		$\sim5\times10^{13}$

Table III: Fe_i calculated from lifetime measurements.

Chemical analysis is in progress in order to determine the total Fe concentration, and therefore the actual amount of Fe segregated in the solid silicon. It will then be possible to know, besides the effective segregation coefficient of Mo and Fe in silicon (for the mono and multi-crystalline structure), also the percentage of Fe present in form of interstitial impurity. In addition DLTS measurements are being performed, and when successful, will give similar information for Mo.

4 SOLAR CELL RESULTS

The solar cell process was carried out on three neighbouring wafers for each impurity concentration, of the available ingots shown in table I.

A set of four wafers of the same size as the contaminated ones was cut from a conventional multicrystalline wafer. This reference mc-Si wafer originated from a central brick of a good-quality industrial DS ingot. The Voc obtained ranges from 580 to 600 mV. This variation is due to the variation of the material quality inside this single wafer.

4.1 Molybdenum in solar cells

The Voc of the solar cells are shown in Fig. 3.

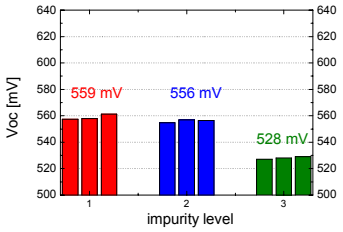

Figure 3: Voc of the solar cells contaminated with three different concentrations of Mo. Reference cast mc-Si average value is 592 mV.

The solar cells with the lowest and middle concentration (1 and 2 in Fig. 3) result in the same Voc, which is 35 mV lower than the reference cast mc-Si value of 592 mV. A drop in the Voc of about 60 mV occurs for the cell with the highest concentration of Mo.

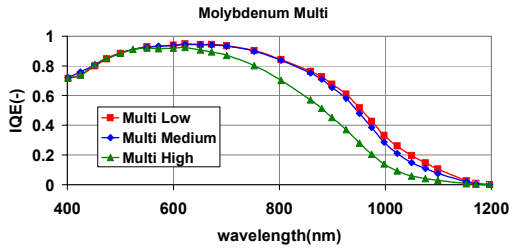

Figure 4: Internal quantum efficiency of solar cells with the three different Mo concentrations.

Also in the internal quantum efficiency at 1000 nm (Fig. 4) the difference between the first two concentrations is still very small.

4.2 Iron in solar cells

Fig. 5 depicts the results from the solar cells contaminated with Fe in case of monocrystalline (left) and multicrystalline (right) structure.

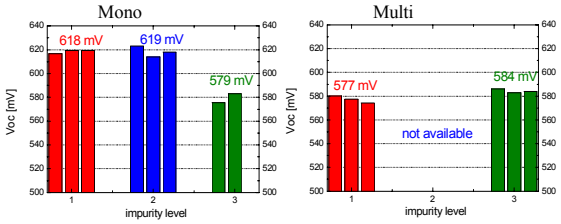

Figure 5: Voc of the solar cells contaminated with three different concentrations of Fe for mono (left) and multi (right).

In the case of multicrystalline Si the Voc remains at the same level for the highest and the lowest concentration of Fe. A drop of 40 mV is instead present in the case of monocrystalline solar cells with the highest level of Fe. Still this Voc is comparable to the Voc of multicrystalline Fe-samples and to the lower value found on the reference DS mc-Si wafers. It is surprising that such low lifetime values for mono Fe wafers result in high Voc. This will be analysed in a further work.

The Voc of the Fe contaminated samples is in all cases higher than the Mo one.

The IQEs confirms the Voc results as visible in Fig. 6.

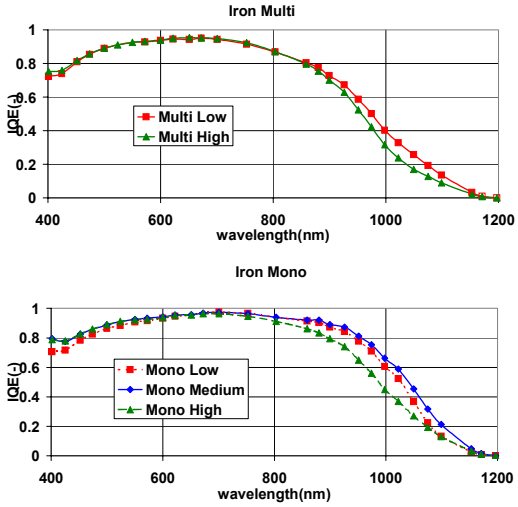

Figure 6: Internal quantum efficiency of solar cells with three different Fe concentration. Multicrystalline top, monocrystalline bottom.

Furthermore from the overlapping of the IQE curves in Fig. 4 and 6 for low wavelength (<600nm) we conclude that the emitter diffusion and the SiN_x deposition were stable for all the solar cells.

5 DISCUSSION

The results for Mo, when compared with equation 1, show the presence of a high recombination activity independent of the

Mo concentration (τ_{other}). This recombination is characterised by a lifetime of 3.6 μs and is dominant in the samples with the two lowest concentrations. This is not the case for the highest amount of Mo where the defects proportional to the Mo-contamination in the melt dominate. A possible interpretation is that in all the three cases Mo is completely decorating crystal defects and only in case 3 enough dissolved Mo is available to further increase the recombination noticeably (i.e. in form of precipitates or cluster or intra-grain atomic impurity), further lowering IQE and Voc.

The fact that the results for Voc and IQE in the case of Mo concentration 1 and 2 are so similar is indicative that the solar cell process is not able to clean the wafers and lower the recombination (in the crystal defects, according to our hypothesis). This is not unexpected considering that Mo is not a fast diffusing impurity.

In the case of iron the linearity of $1/\tau_{eff}$ versus Fe concentration could not be verified due to lack, so far, of sufficient wafers with different concentrations. However assuming the same model holds, it results in a τ_{other} of 2.7 μs for the multicrystalline sample. This value is in rough agreement with the value found for Mo. The slightly lower value might be related to the lower resistivity of the Fe contaminated wafers.

The high "other" recombination activity in the mc-Si samples can have several origins: for example, i) the crystal defects are highly recombination-active as soon as they are decorated by even a small amount of Mo or Fe, or ii) there is unexpected contamination from other impurities or iii) the crystal defects are intrinsically active. This will be analysed using the uncontaminated samples, grown with the same technique. The first hypothesis should be the most plausible considering the cleanliness of the FZ technique.

The lifetime of the monocrystalline (Fe-doped) samples is lower than one would expect (i.e., τ_{other} is not very high). This can again have several origins, e.g. i) not defect-free crystals (i.e. dislocations) as also this ingot revealed the presence of residual stress and inhomogeneous lifetime maps, and/or ii) bulk nucleation of Fe precipitates, or iii) unexpected contamination from other impurities. This will be further clarified with investigations on annealed crystals.

The high levels of Voc and IQE @1000 nm obtained in the case of monocrystalline Fe samples with the low and middle concentration level, suggests that the specific solar cell process applied is tolerant to Fe up to a concentration of about 54 ppma in the silicon feedstock. This can be explained by the gettering effect of the phosphorous diffusion carried out for the emitter preparation. In the case of the highest level of Fe the large amount of iron or the presence of precipitates result in a less effective gettering. This results in the lower Voc shown, and the suppressed IQE.

For the multicrystalline Fe case, the cell results are suppressed, similarly to the case of Mo. The process seems not be able to improve the wafer quality even in the case of the lower amount of Fe. However the results are comparable to the worst results obtained for the reference DS mc-Si wafers. The question is why the cell properties are so much worse than in the monocrystalline wafers. The formation of precipitates is maybe enhanced at the grain boundaries of the multicrystalline samples, or gettering is hindered in multicrystalline silicon, for example by trapping at crystal defects or because precipitates are more stable when formed at crystal defects. This means that grain boundaries do not lower the impact of the impurities but prevent them from being gettered. It is alternatively possible that impurities segregate more in the grain boundaries. Thus the total Fe in the wafers would be higher than in the monocrystalline wafers.

6 CONCLUSIONS

FZ growth has been used in order to investigate the incorporation and the impact of Mo and Fe on monocrystalline and multicrystalline Si solar cells. The different concentration of impurities, introduced in the silicon melt, result in corresponding lifetime variation. This indicates that the impurity concentrations have a dominant impact on the wafer quality, thus the material can be used for the investigation aims.

By means of a simple model it is possible to demonstrate the proportionality between the number of SRH defects (N_t) and the amount of the introduced impurities.

Trapping is visible only in multicrystalline samples, revealing its relationship with the grain boundaries.

The cell process is not able to clean the wafers contaminated with Mo. A drop with respect to standard cast mc-Si between 35 and 60 mV is visible. In the case of multicrystalline cells contaminated with Fe, no variation between different concentrations can be observed. In the case of low Fe (2.6 ppma) the Voc values are comparable to the worst results obtained for the reference DS mc-Si wafers.

For monocrystalline cells Voc is high (30 mV higher than for the mc-Si reference) for the lower and middle Fe concentration. It is possible to conclude that the solar cell process is able to tolerate Fe contamination up to a concentration of about 54 ppma in the silicon feedstock.

These first results are very promising in order to quantify the impact of the impurities on solar cell level.

7 ACKNOWLEDGEMENTS

This work is part of the FP6 CrystalClear project and funded by the European Commission under Contract number SES6-CT_2003-502583.

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U.S. Department of Energy
Energy Efficiency and Renewable Energy

SOLAR AMERICA INITIATIVE

SAI

Overview for Crystalline Silicon Workshop

Denver, CO
August 6 – 9, 2006
Jeffrey Mazer

U.S. Department of Energy
Energy Efficiency and Renewable Energy

SAI Cost Goals and Timeline

Acceleration of the 2020 Goals

- ***Reduced-cost components / systems between now and 2015***
- ***The 2020 DOE PV goals are now scheduled for 2015***

Market Sector	Current U.S. Market Price Range (¢/kWh)	Cost (¢/kWh) Benchmark 2005	Cost (¢/kWh) Target 2010	Cost (¢/kWh) Target 2015
Residential	5.8-16.7	23-32	13-18	8-10
Commercial	5.4-15.0	16-22	9-12	6-8
Utility	4.0-7.6	13-22	10-15	5-7

2

The Solar America Initiative (SAI)
Approach

Reducing Solar Costs to Grid Parity in All U.S. Markets By 2015

SAI Photovoltaic (PV) R&D activities will emphasize technologies with the greatest potential for cost reductions to meet SAI goals. SAI will also continue current efforts on CSP systems R&D.

To accelerate goals, SAI will employ public-private partnerships **(Technology Pathway Partnerships)** to develop components and systems, and demonstrate manufacturing approaches, that deliver low-cost, high-reliability commercial products.

SAI partnership members will develop and market components and systems, while SAI technology acceptance efforts tackle non-R&D barriers to market penetration for both PV and CSP systems.

3

Technology Pathway Partnerships
Phase 1 (FY 2007 – 2009)

Develop Lower Cost 1st/2nd Gen Tech, Demo Pilot Production

- R&D project duration of 3 yrs; then pathway to commercial production
- Two classes give companies the flexibility to align projects with their business model, technical capabilities, and product/process maturity
  - **Component Class:**
    Up to $4M / yr DOE award; 50% cost share required.
  - **Systems Class:** Development of turnkey systems
    Up to $10M / yr DOE award; 50% cost share required.
- Possible down-selects following intermediate stage gates (every ~12 mo)

4

SAI Funding Plan
Phase 1 (FY 2007 – 2009)

- **Max SAI funding (subject to earmarks):**
  - FY 2007 $50 M
  - FY 2008 $55 M
  - FY 2009 $65 M
- **10 – 15 component development awards**
- **4 – 10 system development awards**
- **Universities are encouraged to participate in the industry-led TPPs. In addition, DOE is planning a separate university research solicitation for FY 07.**

5

Contributor Roles Under SAI
Criteria for Choosing Industry-Led TPP's

How Much Will They Impact Solar Markets?

- Magnitude of expected cost reductions and manufacturing capacity.
- Competitive position of proposed system/components in market(s).
- Viability of sales/marketing strategy to achieve threshold production volumes.

Can They Execute Technically?

- Technical feasibility of product R&D roadmap and manufacturing scale-up plan.
- Ability to achieve SAI cost goals given manufacturing & supply chain approach.

Can They Execute from a Business Perspective?

- Experience and qualifications, as well as adequacy of resources and infrastructure.
- Soundness of team's structure and relationships with key partners or suppliers.

Do They Support Other Policy Considerations?

- Domestic manufacturing presence and I.P. ownership.
- Diversity of markets/applications/technologies in DOE investment portfolio.

6

Contributor Roles Under SAI
Major Contributions from Sandia, NREL

- **Sandia and NREL will support Industry and Universities by:**
  - Conducting R&D in support of Industry in core competency areas
    - Cooperation with TPPs for R&D on manufacturing-scale prototype technology (including use of key lab facilities, e.g., the new S&TF)
    - Development of laboratory-scale technology of use to broader industry
  - Leading collaborative R&D on 3rd Gen. devices (e.g., organics, quantum dots)
- **Sandia and NREL will support DOE by:**
  - Providing analytical support for Industry solicitation and technical monitoring
  - Conducting independent test and evaluation of industry deliverables, including measurements & characterization, reliability testing, etc.

7

DOE Photovoltaics Budget
All Activities

FY 2006 budget after earmarks	**$ 60.0 M**
FY 2007 request	**$ 139.5 M**
House mark	**$ 134.5 M**
Senate mark	**$ 120.3 M**

8

Direct Route for the Production of Solar-Grade Silicon (SoG-Si) from Metallurgical-Grade Silicon (MG-Si)

Aud Wærnes[1], Eivind Øvrelid[1], Ola Raaness[1], Bart Geerligs[2], Sven Santeen[3], Benno Wiersma[4], Harsharn Tathgar[1]

1) SINTEF Materials and Chemistry
2) Energy Research Centre of the Netherlands
3) Scanarc Plasma Technology AB
4) Sunergy Investco BV

1. Abstract

This paper gives a status on the availability and the production techniques for solar-grade silicon (SoG-Si). A new direct route for the production of SoG-Si (SOLSILC concept) is presented. Sources of impurities, the formation of inclusions and their effect is discussed. Carbon (C), Titanium (Ti) and Aluminium (Al) impurities are used in the calculations because they are important with respect to cell efficiency and yield.

2. Market for silicon feedstock

The sources of fossil fuels are limited and the high energy prices and public awareness for the global warming problem have opened up the market for solar cells. The photo-voltaic (PV) industry has an average growth rate of about 30% for the last 10 years. Today, the majority of solar cells are based on silicon, and most experts assume that crystalline Si PV-technology will dominate the PV market for the next decade. The only commercial source for SoG-Si has been rejected and non-prime silicon from the semiconductor industry. This makes the PV industry highly exposed to the cyclic changes in the semiconductor market. REC Silicon at Moses Lake in US is the world's first dedicated producer of polycrystalline silicon for solar cells.

The dramatic growth in the PV industry has, however, caused a lack of solar grade silicon SoG-Si, *i.e.*, silicon with the required chemical purity for PV applications, resulting in the increased prices for such material. Presently, the shortage of low-cost SoG-Si is the main factor preventing environmentally friendly solar energy from becoming a giant in the energy market in a generation or two. A direct metallurgical route for production of solar grade silicon uses less than half energy than the conventional Siemens process that uses more than 100kWh/kg Si /1/. A metallurgical route would reduce the energy payback time for solar cells to typically 1 year.

As can be seen from Figure 1, the demand for SoG-Si is expected to grow rapidly. The growth rate of the PV industry is estimated to be more than 40% per annum in the coming 5 years /2//3//4/. The world production of high-purity silicon is estimated to increase from 32.000 tons in 2005 to 85.000 tons in 2010. Approximately 19.200 tons is supplied (including inventory) to the semiconductor industry, and 19.500 to the PV industry. Figure 1 shows the predicted growth in the demand of silicon from PV industry with 19.500 tons in 2005 and 71.000 tons in 2010, taking into consideration 40% reduction in the silicon usage per watt of module shipped. The rise of 1.7GW capacity in 2005 to 10GW in 2010 gives an average 43% growth in the next 5 years.

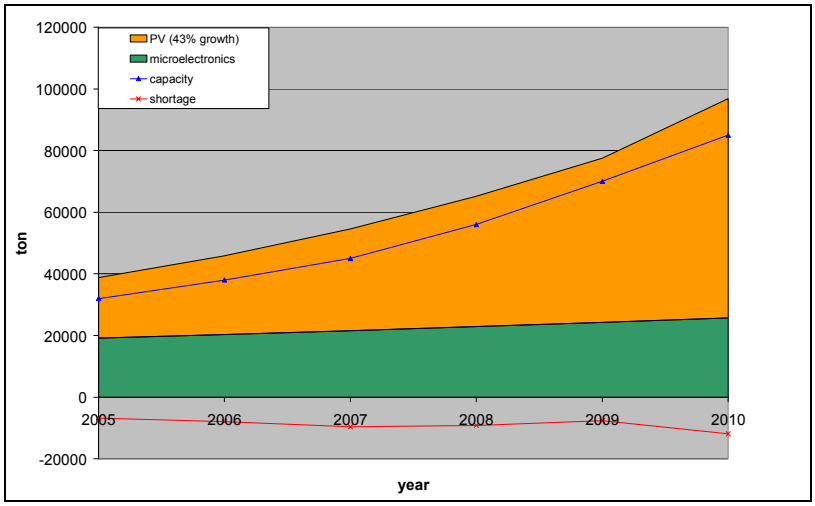

Figure 1: The demand and supply of SoG-Si with a growth rate in the PV industry of 43% /2/.

The main goal for the next coming years is to secure the availability of SoG-Si at low costs, through mass volume production. This growth is not possible to achieve only by the present supply route. Therefore, it is essential to develop an independent, dedicated energy efficient silicon feedstock supply chain, which secures supply of low cost silicon to the PV industry. The shortage of SoG-Si is leading to high prices and a secure supply of SoG-Si for wafers and cells at reasonable costs is crucial for being in the business.

In principle, there is not a shortage of silicon in the world today. In the metallurgical industry, 900,000 ton/y metallurgical-grade silicon (MG-Si) is produced by carbothermic reduction of quartz with a purity of about 99%. The main impurities are iron, aluminium, titanium, phosphorus and boron. Half of the silicon produced is used as an alloying element for aluminium, and 45% is used in the silicone industry. The remaining 5% is used as the raw material in the chemical processes of semiconductor industry. The silicon has to go through a very energy consuming process in order to achieve the purity that is required by the semiconductor industry. Research shows that the quality requirements for solar grade silicon are not as high as electronic–grade silicon (EG-Si), at least for specific cases such as carbon and dopants.

3. Different routes for silicon feedstock to solar cells

Due to the dramatically increased demand for SoG-Si over the last decade, many poly-silicon producers are now in the process of developing new feedstock routes to produce SoG-Si. However, the gap between demand and supply of poly-silicon has so far not resulted in new commercial processes. This means that every producer of silicon based wafers is waiting for a new affordable feedstock that is available in large quantities. The public knowledge of the different process initiatives is limited. The silicon value chain to feedstock for solar cells is shown in Figure 2. In principle, there are several different ways to SoG-Si.

3.1 Traditional feedstock for solar cells

The traditional route to semiconductor silicon is shown on the left hand side of Figure 2. Scrap, rejected, and non-prime material from this production is the main supply route of today. For a large part, the non-prime poly-silicon is deliberately produced by operating the conventional Siemens process with more economical parameters (e.g. faster, lower energy, less quality control).

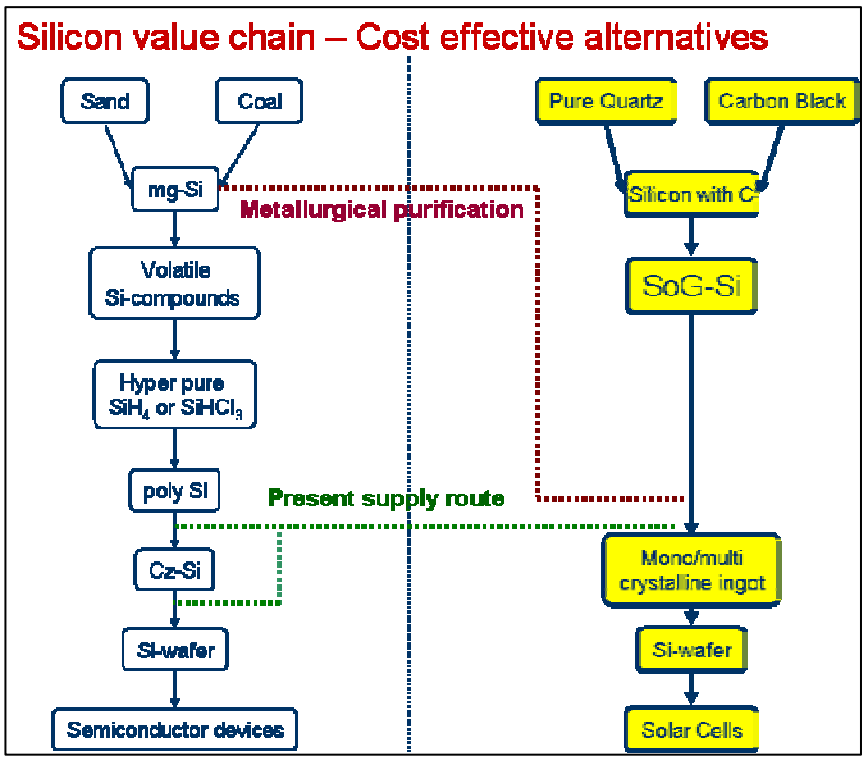

Figure 2: Alternative routes to Solar Grade Silicon

3.2 Modified chemical route

Several companies (Wacker, REC silicon, etc) are making a big effort to economise the chemical route by shifting from rod decomposition of TCS (Trichlorosilane) to fluidised bed in the last step of the polysilicon production. The joint venture of Degussa and Solar World, Joint Solar Silicon (JSSI), is testing a free space reactor. Tokuyama is testing a strongly modified filament reactor for their "Vapour to Liquid Deposition (VLD)" process.

3.3 Purification of metallurgical silicon

The purification of metallurgical silicon has, so far, not resulted in a commercially viable process for a feedstock to solar cells. Several companies (Elkem, FerroAtlantica, Dow Corning etc.) are working on this route to SoG-Si. Elkem has been working on the development of a new process for the production of SoG-Si for a very long time /5//6//7/. They started already in the 80ties and 90ties together with the oil company Exxon and Texas Instruments.

Elkem has further enhanced its "standard" metallurgical products through refining to produce SoG-Si. They have developed a two step refining process. The first step is slag refining of the silicon to remove certain elements. The next step is a leaching process that will remove other elements. The energy consumption of the silicon process is 20-25% of the traditional Polysilicon route. Elkem Solar has shown that their SoG-Si may be used to produce cells of an efficiency of 15 to 16% /5/. Elkem emphasize low costs, big volumes and low energy consumption as the main asset.

3.4 Direct carbothermic reduction of quartz

Another source of solar grade silicon might be the direct carbothermic reduction of quartz and carbon as indicated on the right hand side of Figure 2. The SOLSILC route is an example of that.

3.5 Electrolysis/electrochemical refining

Electrolysis has been the way to aluminium for more than 100 years. Silicon can also be produced by electrolysis. This route has so far only been investigated on a laboratory scale. This could be a viable process on long term. SINTEF and NTNU are working on the development of this route.

A process has also been patented by Stubergh /7//8/ in 1994. The process is based on the dissolution of quartz in a fluoride-containing bath at 1000°C, and decomposition of the quartz. Pure silicon deposits at the electrode and the impurities remain in the electrolyte. Afterwards, the silicon is crushed and cleaned with acid.

3.6 Recycling

Recycling of ingot off-cuts, off-specs blocks, broken wafers and cells has a major focus these days. Approximately 10% of the silicon is lost between the melting step and the block to be sliced in wafers. Approximately 50% of the silicon is wasted as saw dust in the slicing step. Slurry (SiC (Silicon Carbide) + PEG (Poly-Ethylene-Glycol)) used as cutting medium in Multiple Wire Saw (MWS) technology has been recycled for a long time.

4. Direct Metallurgical Route - SOLSILC

The Direct Metallurgical route produces silicon from ultra-high purity raw materials. Silicon production according to the SOLSILC technology /9/ has resulted in silicon of very high purity. Research is presently in a progressive stage through the EC funded SiSi/FoXy project. This carbothermic production route can, in principle, reduce the cost of feedstock to below € 20/kg.

The idea behind the SOLSILC Technology was to develop a new two-step high temperature plasma-process for SoG-Si production, based on carbothermic reduction. The SOLSILC Technology relied on expertise of the metallurgical production methods for Silicon and SiC, and PV cell processing, see Figure 3.

Figure 3: SOLSILC pilot silicon metal production.

A principle sketch of the SOLSILC concept is presented in Figure 4. After reduction of quartz with carbon in the electric arc furnace, the metal goes through several refining steps. It should be noted that the various steps may be added or omitted.

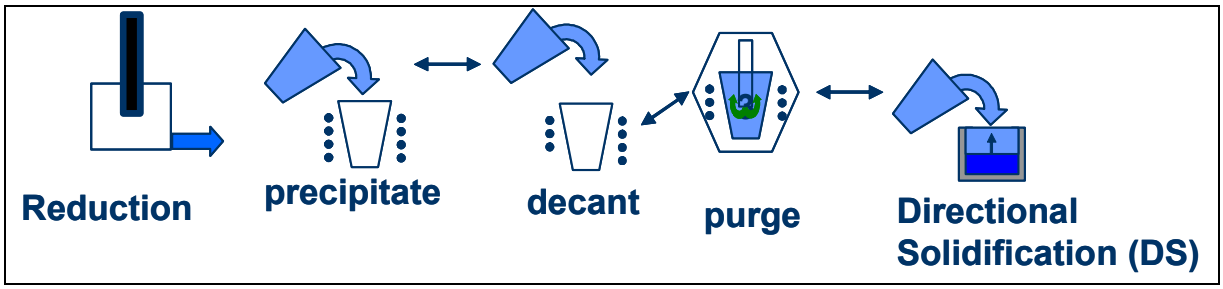

Figure 4: Various steps in SOLSILC concept.

Tolerance for impurities

As to our knowledge, there is no standard for SoG-Si describing the limits for the impurity levels. In the SOLSILC concept, SoG-Si silicon is produced from clean raw materials to give high purity material directly from the reduction furnace. In the SOLSILC concept, carbon and quartz with very low contamination levels are used. Silicon produced with the SOLSILC concept has resulted in a new standard of cleanliness for a carbothermic reduction process, and has already been running campaigns at a pilot scale of 20kg Si/h. Table 1 shows the impurity levels in ppm-w (parts per million by weight) which is estimated to be necessary for solar grade silicon, based on our own investigations of artificially contaminated material /10/, and on recent experiments on highly doped silicon /11/. However, only limited information has been published on this subject and these numbers have a considerable amount of uncertainty. For comparison, specification on material used today and results from conventional high-purity metallurgical silicon (Silgrain from Elkem) are also shown.

Table 1: Estimates on the impurity levels (ppm-w) by the SOLSILC route and impurity levels to make solar cells.

	Fe	**Ti**	**Al**	**P**	**C**
SOLSILC Final product estimated	<0.1	<0.1	<0.1	--	<50
Demands /10/	1-10	0.17	0.08	0.1-1	10-50
Lowest commercial grade /12/	<0.1	<0.1	<0.1	<0.1	<4
Metallurgical (Silgrain, Elkem)	400	21	1100	--	--

The impurity levels in silicon from the SOLSILC direct route are close to the presently estimated requirements. This means that the need for additional cleaning of raw materials is limited, and consequently the cost of cleaning. This carbothermic production route can therefore, in principle, reduce the production cost of feedstock to below € 20/kg.

As mentioned previously, there is no standard for SoG-Si. A lot of effort has been made to assess the SOLSILC material with respect to cell performance. The best cells efficiency so far is 13.7% (>90% of reference) with screen-printing (industrial) process steps, on n-type mc-Si, made from a blend of 1/3 SOLSILC silicon after SiC removal and 2/3 clean silicon /13/.

Formation of inclusions

In a direct carbothermic route, the liquid silicon is tapped at a temperature between 1600°C and 1800°C. In addition to the dissolved carbon, the tapped material contains SiC (Silicon Carbide) particles and oxide films /14/. If the final metal is used as a raw material for solar cells, it is required that all particles above a certain size are removed. SoG-Si is crystallised in quartz crucibles coated with Si_3N_4 (Silicon Nitride). Both SiC and Si_3N_4 act as nucleation sites for precipitation of the other crystal /15/. These precipitates/needles going through grain boundaries result in shunting of the solar cells. To clean molten silicon, advanced refining techniques are necessary where high melting point and high reactivity towards refractories are extra challenges.

Removal of inclusions by settling

The densities of SiC and Si_3N_4 particles are higher than the Si-melt.
ρ(SiC) = 3.2 gm/cm^3, $\rho(Si_3N_4)$ = 3.4 gm/cm^3, $\rho(SiO_2)$ = 2.6 gm/cm^3, ρ (Si) = 2.3 gm/cm^3 /1/

$$V_s = \frac{d^2 g(\rho_1 - \rho_2)}{18\eta}$$

The first step to remove the particles is by settling in a quiet bath given by Stoke's equation: Where g is the acceleration of gravity, d the diameter of inclusion, η the viscosity of silicon. ρ_1 is the density of an inclusion and ρ_2 density of silicon melt.

The refining efficiency is dependent on the settling times and the SiC particle size /14/. Theoretical calculations have shown that after one hour, 10 μm particles are removed down to 15% of the initial concentration, while almost all 20 μm are removed. These calculations were used to design a pilot scale reactor. Experiments were performed with SOLSILC material, containing 700 ppmw of total carbon. After the settling process, the concentration of carbon in liquid silicon was less than 50ppm.

Refining by solidification

As a part of SoG-Si production, casting of the material after refining is necessary. A substantial refining effect can be attained if planar front is achieved during the solidification. The solubility of major impurities is higher in the liquid phase than in the solid phase.

At the solid/liquid interface, the concentration of the impurities in the silicon to solidify will be in equilibrium with the molten metal. The ratio between the two concentrations are defined as the partition coefficient given by $K = C_s/C_l$. C_s is the concentration in solid and C_l is the concentration in liquid. For $K < 1$ there will be a refining effect. Assuming that there is thermodynamic equilibrium at the solid/liquid interface, no diffusion of impurities in solid, and complete mixing in the liquid, the maximum refining effect is given by the well-known Scheil equation:

$$\frac{C}{C_0} = (1 - f_s)^{K-1}$$

Where C is the concentration in the liquid at a given fraction solid, f_s, and C_0 is the nominal (average) concentration of the silicon. The refining of aluminium was studied by addition of 8ppm Al to EG-Si /14/. 12 kg ingot was produced by directional solidification in SINTEFs

Crystalox DS250 laboratory scale furnace. The concentration of Al in the solid silicon was determined by resistivity measurements.

Figure 5 shows a comparison between the measured aluminium content in the solidified Si at different positions, the corresponding aluminium concentration in the liquid silicon, and the theoretical curve calculated by Scheil's equation.

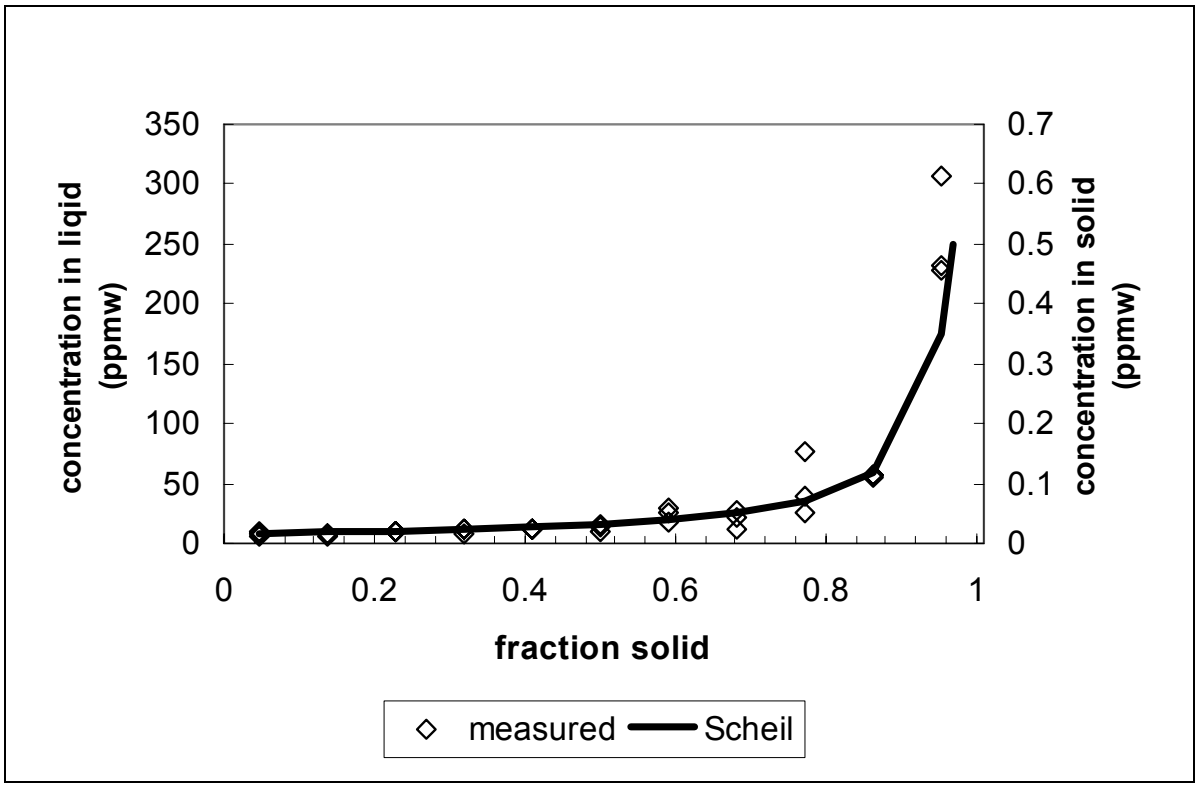

Figure 5: Measured and calculated distribution of initial 8 ppm added aluminium over the height of ingot after directional solidification. K=0.002

The curve corresponds well to Scheils's equation, indicating that the solute build up at the solidification front is negligible (i.e. the assumption regarding complete mixing in liquid is valid). A similar relationship can be given for Ti with $K = 10^{-5}$ /12/.

5. Conclusions

There is a big demand for SoG-Si due to tremendous growth in PV-industry for the last 10 years. There are several initiatives for making new SoG-Si feedstock materials for the PV-industry. The prospect for the future for the PV industry is very promising as long as the supply of silicon is adequate. The consequence is that there will probably be room for more than one new process.

It has been shown theoretically that it is possible to make clean enough material with the refining steps in the SOLSILC process. Based on composition of the raw materials and furnace parameters, the metal that leaves the furnace will contain some impurities. These are mainly Ti, Al, Fe and C. In the previous work /9//11/ limits for tolerable levels in solar grade silicon has been given. This paper shows that it is possible to reduce the impurities below these levels with settling and directional solidification.

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Luminescence imaging: an ideal characterization tool for silicon

T. Trupke, R.A. Bardos, M.D. Abbott, F.W. Chen, K. Fisher and J.E. Cotter

Centre of Excellence for Advanced Silicon Photovoltaics and Photonics,
The University of New South Wales, Sydney, NSW, 2052, Australia,
Telephone: +61 02 9385 4054, Facsimile: +61 02 9662 4240,
E-mail : thorsten@trupke.de

INTRODUCTION

Electroluminescence (EL) imaging[1] of silicon solar cells and Photoluminescence (PL) imaging[2] of silicon wafers and solar cells are two related techniques that have recently emerged as fast and efficient characterization and process monitoring tools for silicon. This paper reviews some of the progress in the development and application of various luminescence based characterization techniques at UNSW, with particular emphasis on luminescence imaging.

PL LIFETIME MEASUREMENTS

The terminology "luminescence" was used for the first time by the German physicist Eilhard Wiedemann, who defined luminescence as "the emission of light by specific materials without corresponding increase of the temperature"[3]. In semiconductors luminescence is emitted if electrons from the conduction band and holes from the valence band recombine radiatively, i.e. with the emission of a photon. Consequently the rate of spontaneous emission r_{sp} is proportional the electron and hole concentrations n_e and n_h:

$$r_{sp} = B(\Delta n) \cdot n_e \cdot n_h \approx B(\Delta n) \cdot \Delta n \cdot (N_D + \Delta n), \quad (1)$$

where N_D is the doping concentration, Δn is the excess carrier concentration and $B(\Delta n)$ is the injection level dependent radiative recombination coefficient[4]. The luminescence intensity I_{PL} that is measured experimentally is proportional to the rate of spontaneous emission and thus according to Eq.1 linear in the *product* of electron and hole concentrations. This sets luminescence based characterization techniques apart from other techniques used in photovoltaics research, such as photoconductance, microwave reflectance or infrared free carrier absorption, where the measured signals are related to the *sum* of majority and minority carriers or the variation of that sum upon illumination. This fundamental difference has some quite important consequences regarding the sensitivity of these techniques to various experimental artifacts.

In wafers with a grown or induced junction the so called depletion region modulation (DRM) effect[5,6] leads to an overestimation of the effective minority carrier lifetime at low carrier concentrations in quasi steady state photoconductance (QSS-PC) lifetime measurements. In contrast, it has been shown both theoretically and experimentally that QSS-PL measurements are unaffected by these artifacts[7].

Minority carrier trapping is another mechanism that leads to an overestimation of the minority carrier lifetime in QSS-PC measurements at low to moderate carrier concentrations. PL lifetime measurements have been shown to be negligibly affected by this mechanism[8].

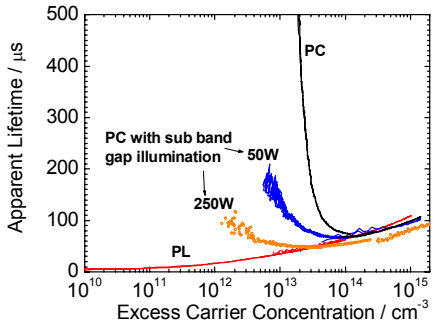

Fig.1 *Effective lifetime from QSS-PL (red) and from QSS-PC (black) for a 1.2 Ωcm p-type wafer with trapping. The blue and orange curves show the lifetime from QSS-PC with simultaneous sub-band-gap illumination.*

As an example Fig.1 shows a comparison of injection level dependent QSS-PC and QSS-PL lifetime measurements on a multicrystalline 1.2 Ωcm p-type wafer (data from Ref.8). The increase of the measured QSS-PC lifetime at injection levels < $10^{14}cm^{-3}$ is caused by minority carrier trapping. The curves labeled 50W and 250W show that the influence of trapping on the PC data can be reduced to some extent by simultaneous sub-band-gap illumination[9], but that it cannot be completely removed at least with the sub-band-gap light intensities conveniently achievable with the emission from a 250W QTH lamp that is filtered through a 3mm thick polished silicon wafer. Fig.1 shows experimentally that the QSS-PL data are unaffected by the trapping effect, which is well understood theoretically[8] and a direct consequence of the dependence of luminescence signals on the product of electron and hole concentrations.

Another important and somewhat surprising aspect of QSS-PL lifetime measurements which will be discussed in the context of luminescence imaging below is the high sensitivity. The combination of high sensitivity and robustness against DRM effect and minority carrier trapping make QSS-PL the only lifetime technique that allows reliable measurements of the minority carrier lifetime at low to moderate injection levels. This is particularly important for

defect characterization based on advanced lifetime spectroscopy methods[10] and for the investigation of various detrimental effects that dominate device characteristics at low voltages.

SUNS-PL

With $n_e * n_h = n_i^2 * \exp(\Delta\eta/kT)$ the rate of spontaneous emission from Eq.1 can also be expressed as

$$r_{sp} = B \cdot n_i^2 \cdot \exp(\Delta\eta / kT) \qquad (2)$$

with $\Delta\eta$ the separation of the quasi Fermi energies. The latter is directly linked to the voltage of a solar cell and consequently the measured luminescence signal can be interpreted in terms of an implied voltage. This is the basis of the Suns-PL technique[11] in which implied IV curves are measured in analogy to Suns-Voc measurements but with the voltage measurement replaced by a luminescence measurement. The advantage is that such measurements are contactless and do not require a device structure, i.e. they can even be performed prior to junction formation. Examples of applications of the Suns-PL technique will be discussed further below.

LUMINESCENCE IMAGING

Motivation The rapid expansion of the photovoltaic industry and the desire for higher yield and higher average efficiency in industrial manufacturing demand for advanced characterization tools that can ideally be applied in-line on every sample. With a typical throughput in a modern automated production line of one wafer every two to three seconds and allowing for some time for wafer loading and unloading the actual data acquisition time during such in-line characterization must not exceed one second per wafer.

For non-spatially resolved techniques such as the QSS-PC or QSS-PL lifetime techniques a data acquisition time of one second per wafer does not represent a serious limitation. Very valuable information about processing and material or device properties is however also contained in spatially resolved measurements. A characterization technique that measures the spatially resolved electronic properties of silicon wafers, that is fast enough to be applied in-line on every sample would thus be desirable.

Background Examples for existing spatially resolved techniques include mapping techniques, where the sample surface is scanned with each pixel measured one at a time and imaging techniques, where the signal from the entire sample is captured with a camera. An in-line microwave reflectance mapping system to measure relatively coarse (4mm resolution) line scans of the minority carrier lifetime has recently become commercially available[12]. Two dimensional mapping tools are orders of magnitude too slow to be used as in-line tools, even with only moderate spatial resolution. Imaging techniques include Infrared Lifetime Mapping [13] (ILM) and Carrier Density Imaging [14] (CDI), and also Lock-In thermography[15], which is used primarily for shunt detection and quantitative shunt analysis. While ILM/CDI are faster than mapping techniques, it has been shown that to achieve the desired measurement time of one second with an acceptable signal to noise ratio on an industrial size silicon wafer with a minority carrier lifetime of 1 μs the spatial resolution must be reduced to 1 cm [16]. Most spatial information is obviously lost in that case. In addition the wafer must be heated to a temperature of ~70 degrees in order to achieve that sensitivity, which is impractical for in-line applications and it is unclear (at least to the authors of this paper) how these techniques are affected by surface texturing. Both ILM and CDI are also affected by both the DRM effect and by minority carrier trapping, a fact that has recently been used to image trap distributions in silicon wafers[17]. Summarizing, prior to the recent demonstration of luminescence (EL[1] and PL[2]) imaging there has been no existing experimental technique that was even close to being fast enough for spatially resolved in-line process monitoring of large area silicon wafers or solar cells.

Quantitative PL imaging In our PL imaging set up the emission from a 25W cw infrared laser illuminates an area of up to 15x15 cm^2 with up to one Sun equivalent intensity and with lateral intensity variations <10%. The spatially resolved emission from the sample is captured with a commercially available thermoelectrically cooled one megapixel

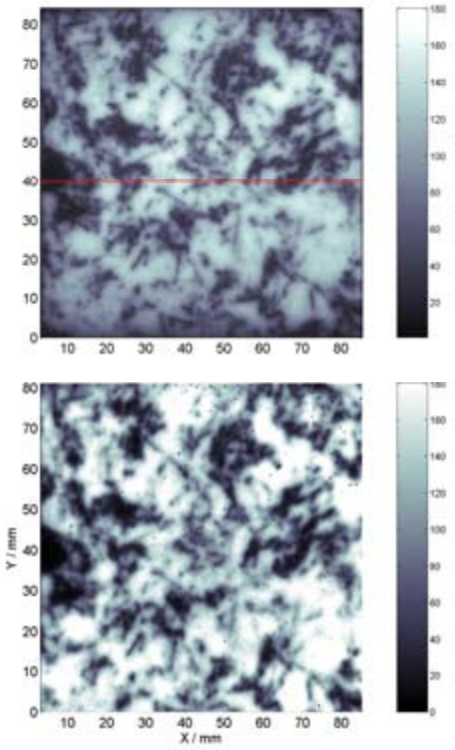

Fig.2 *PL image (top) and CDI measurement (bottom) on a polished 8.5x8.5 cm^2 mc-Si wafer.*

silicon CCD camera. Fig.2 (top) shows a calibrated PL image (from Ref.2) taken on a polished 8.5x8.5 cm^2 mc-Si wafer (the color bar indicates the lifetime in microseconds). A CDI measurement taken at ISE, Freiburg on the same wafer and with similar illumination conditions as the PL image is shown for comparison in Fig.2 (bottom). The two

independently calibrated images show very good quantitative and qualitative correlation, with absolute variations between the two measurements on the order 10%. This demonstrates that PL imaging can be used to obtain quantitative information about the spatially resolved absolute minority carrier lifetime.

Importantly the data acquisition time for the PL measurement was only 1.5s with 130µm spatial resolution, whereas the CDI measurement took 30s with lower spatial resolution of 350µm per pixel. By upgrading various components of our PL imaging system at UNSW we have managed to further improve the sensitivity by a factor ~40. Silicon wafers with significantly lower effective minority carrier lifetimes of only 1-2 µs can now be measured with a data acquisition time of only one second with binning of 2x2 pixels. *High resolution PL images can thus now be taken with a data acquisition time of ~1s per wafer before and after each processing step in photovoltaic manufacturing*.

Surprising sensitivity of PL imaging: At first sight the high sensitivity of luminescence techniques when applied to silicon is somewhat unintuitive because silicon is an indirect band gap material and as such generally has comparatively poor luminescence quantum efficiency. However, a simple estimation shows that the short data acquisition times in luminescence imaging as discussed above are not so surprising after all.

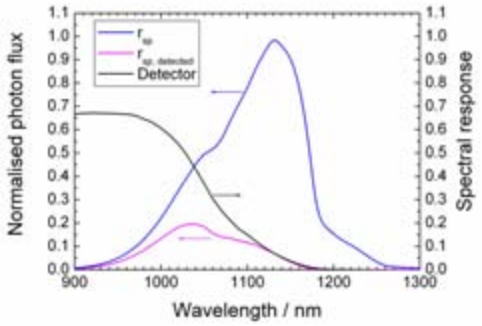

Fig.3 *Spectral rate of spontaneous emission from crystalline silicon (blue) and spectrum that can be captured (magenta) with a typical silicon photo-detector.*

Commercially available silicon CCD cameras are used in both EL and PL imaging. As shown in Fig.3 the choice of a silicon detector for luminescence measurements on silicon samples is not optimal. The product of the calculated spectral rate of spontaneous emission from silicon at room temperature (blue line) with the spectral response of a silicon PIN diode used in our lab (black line) shows that only a relatively small fraction of photons (in this case 20%) in the spectral range around 1050nm can be captured. Generally the spectral response of silicon CCD cameras falls off at shorter wavelengths compared to the Si PIN detector used for these calculations, leading to a significantly lower response in the spectral range 900nm-1200nm, where luminescence occurs. As a conservative lower limit for the fraction of detected photons we use 1%. To estimate the emitted luminescent photon flux in a PL experiment we assume one Sun equivalent illumination which corresponds to ~$2.5*10^{17}$ $s^{-1}cm^{-2}$. The external luminescence quantum efficiency of low quality silicon with a minority carrier lifetime of a few microseconds is on the order 10^{-6}, which gives ~$2.5*10^{11}$ $s^{-1}cm^{-2}$ luminescent photon flux. For a 10x10cm^2 wafer the total emitted photon current is thus $2.5*10^{13}$ s^{-1}. With the optics required to image a wafer of that size onto a typical CCD chip only a fraction of ~1% of luminescent photons are collected giving a total of $2.5*10^{11}$ s^{-1} photons entering the camera of which 1%, i.e. $2.5*10^{9}$ s^{-1} can be detected. In a 1Megapixel chip this corresponds to 2500 counts per pixel per second. In modern high quality silicon CCD cameras the noise is dominated by the shot noise at this signal level and a signal to noise ratio of 50 is thus achieved even with relatively conservative estimates of the fraction of detected photons and under the assumption of poor quality silicon. It is thus by no means surprising that good quality luminescence images on moderate or high quality silicon wafers with minority carrier lifetimes of tens to hundreds of microseconds can be obtained with data acquisition times of one second or less.

Qualitative PL imaging One general disadvantage of luminescence lifetime measurements compared to e.g. QSS-PC experiments is that the calibration of the measured signal into an absolute excess minority carrier concentration varies strongly from one sample to the next. This is mainly because the calibration depends on the sample geometry and on the doping concentration. As a result the calibration of PL images (i.e. counts per pixel) into absolute lifetime requires a separate calibrated lifetime measurement to be carried out on each distinct sample. To elucidate this point we consider two otherwise identical samples, one with planar surfaces, the other one with Lambertian surfaces. Between the planar and the textured sample the total emitted luminescence intensity can vary by up to a factor $2n^2$, where n is the refractive index. For the same excess carrier concentration (i.e. lifetime) the emitted luminescence signal can thus vary by up to a factor ~26. In practice the variations are smaller, because the silicon sensor primarily measures short wavelength luminescence, the intensity of which is less strongly affected by the surface texture. Nevertheless, a separate calibration of the measured luminescence image for a given sample is unavoidable. In industrial applications where a large number of samples with very similar geometry and doping are measured this may be less critical.

An integrated system with built-in absolute calibration is currently under development at UNSW. However up to now the separate calibration of PL images represents a quite significant amount of additional experimental effort, especially if a large number of samples are measured. One focus of the initial work at UNSW has therefore been qualitative PL imaging, where only relative variations of the PL signal across a given sample are considered. Such qualitative PL imaging has been used extensively by the buried contact solar cell group at UNSW and has revealed an unexpectedly rich variety of problems with standard processing techniques some of which had been in use for more than ten years. Within a few months of its introduction at UNSW,

PL imaging revolutionized not only quite a few processing steps, but also the way process monitoring is routinely carried out. A few of the numerous examples for extremely fast and thus efficient process monitoring using PL imaging shall now be discussed.

Process monitoring at UNSW has traditionally been done using a Sinton[18] bridge to perform photoconductance lifetime measurements on samples after each high-temperature furnace process. Values for the bulk lifetime, emitter saturation current and 1-Sun implied voltage were used to compare the electrical performance between batches. This data was used to optimize diffusion settings and to indicate when furnace maintenance was required, e.g. TCA furnace cleaning or replacement of diffusion sources. This technique of process monitoring is limited in that it only provides spatially averaged information, which in many cases makes it difficult to determine the actual cause of the reduced lifetime. The addition of PL imaging to our process monitoring revealed a wide variety of process-induced defects, many of which were not related to the traditional scapegoat of a "dirty" furnace. In many cases the spatial information provided by PL imaging makes it immediately obvious to the process engineer what has gone wrong with a particular sample and provides an excellent tool to characterize alternative processes to remove the problem. Several example PL-images of samples with process-induced defects are shown in Fig.4.

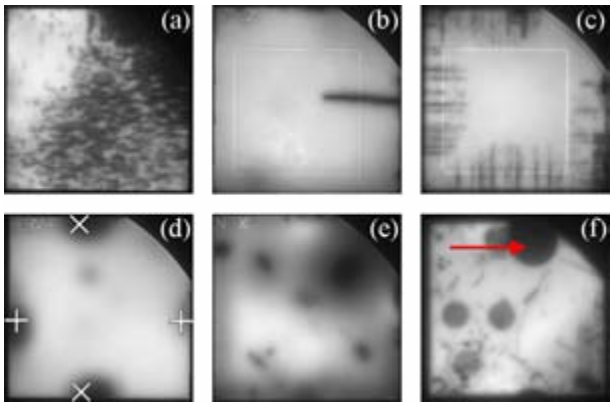

Fig.4 *One Sun PL images of samples with a variety of process induced defects (see text for details).*

Sample (a) is afflicted by a furnace contamination that occurred during a phosphorous surface diffusion. Sample (b) displays a region of enhanced recombination extending from the contact point with the diffusion boat. Here a poor unloading procedure has resulted in the formation of a crack (not visible optically). Sample (c) displays microcracks extending from all four laser processed edges. In this case the laser power used to cut the 2" samples from a 4" wafer was too weak. Stress generated during the subsequent cleaving process resulted in the formation of the damaged regions. Sample (d) has areas of enhanced recombination at the sample edges caused by plastic tweezer handling (location of tweezer contact marked with X and +). This contamination occurs to varying degrees in all samples handled in a drying technique traditionally used at UNSW on samples that are too small to spin dry. Sample (e) shows a pattern of enhanced recombination caused by a four-point probe used to monitor sheet resistance. Sample (f) has scratches, damage from a micrometer and a region of poor surface passivation (dome shaped dark area at the top, red arrow) caused by the substrate holder used during deposition of PECVD nitride.

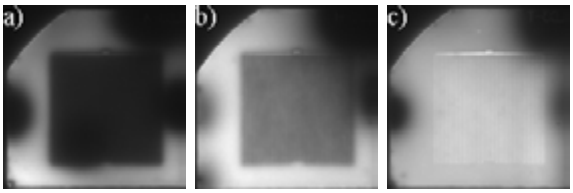

Fig.5 *One-Sun PL images of samples after laser scribing, thermal cycling and surface passivation with pre-thermal cycle NaOH etch times of a) 0 minutes, b) 8 minutes and c) 20 minutes.*

Process monitoring with PL techniques allows failures such as those presented above to be immediately identified. This allows defective wafers to be removed from the line before they undergo any further processing, which saves valuable resources at UNSW and suggests obvious benefits in a high throughput manufacturing environment. E.g. in the case of furnace contamination a cleaning procedure could be activated before the dirt spreads to subsequent wafers or other locations on the production line. Assessment of wafer processing also allows for optimization of handling procedures, such as the use of plastic tweezers discussed above. Within a high-throughput environment there are numerous handling processes that may be adversely affecting the yield. PL provides an excellent tool to identify and remove such problems from the production line. The possibility to detect microcracks with PL imaging is also highly relevant for industrial applications.

PL tools were used to optimize and monitor the performance of chemical processes. Laser ablation is used at UNSW to form the contact grooves in a variety of cell designs. After the laser grooving process it is necessary to remove a thin layer of laser damaged silicon with a NaOH or KOH etch prior to high-temperature processing. PL images of samples fabricated with different etch times are shown in Fig.5[19]. Sample (a) and (b) display a clearly reduced minority carrier lifetime in the region of the laser contacts. Sample (c), etched for the longest time, has no increased recombination in the groove region. In a production line, PL imaging of samples with such laser formed contacts could be used to ensure the time and temperature of an etching process remains adequate. PL techniques could also be used to determine the optimum etching conditions required to avoid the formation of defects.

PL techniques have also been shown to be an excellent characterization tool to monitor and optimize the application of PECVD nitride[20]. One example is the effect of thermal gradients during annealing processes. Annealing is commonly used with nitride films to improve the surface passivation quality. PL images of two identical samples that

were annealed under the same conditions in two different furnaces are shown in Fig. 6.

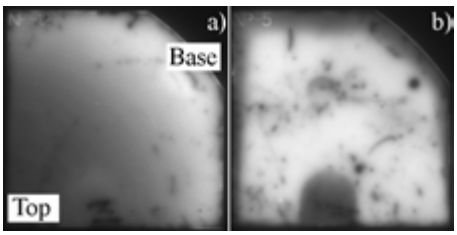

Fig.6 *One Sun PL image of silicon nitride passivated samples annealed at 500ºC for 5 minutes in (a) furnace #1 and (b) furnace #2.*

Sample (a) displays a variation in effective carrier lifetime from the base (where it contacted the diffusion boat) to the tip. This is attributed to a thermal gradient, probably due to thermal pinning from the large quartz boat, which has resulted in a temperature gradient across the wafer. Sample B displays no such gradient in annealing quality. The spatial information provided by the PL image and the fact that the gradient in the lifetime was observed on all samples annealed in that specific furnace allowed this particular problem to be identified and rectified very efficiently.

SERIES RESISTANCE IMAGING

The series resistance R_s is an important parameter that affects the efficiency of solar cells. High series resistance causes a reduced fill factor and can even result in lower short circuit current density[21], both detrimental effects that contribute to a reduced efficiency. Contributions to the total series resistance of a solar cell include e.g. the contact resistance from the semiconductor to the metal electrodes and also lateral series resistance due to a limited conductivity of the emitter. Generally these contributions to the total series resistance vary laterally across a cell. Existing experimental techniques to quantify such spatial variations of the series resistance include Corescan[22,23] and CELLO[24], both mapping techniques and also various recently introduced imaging techniques based on dark (Rs-DLIT) and illuminated (Rs-ILIT) infrared lock-in thermography (LIT)[25]. These techniques require data acquisition times of typically tens of minutes up to several hours per solar cell.

It has recently been demonstrated that luminescence imaging is another promising experimental technique to measure series resistance variations across a cell[26]. Fig.7 shows three luminescence images taken on an industrial 12.5x12.5 cm^2 screen printed monocrystalline solar cell. The efficiency of that cell (14.4%) is significantly lower than the efficiency (~16%) of average cells from the same batch, which according to the IV characteristics is caused by a lower fill factor, which in turn is due to a large series resistance. A PL image taken with about one Sun equivalent illumination intensity and an EL image taken with 25mAcm^{-2} forward current density are shown in Figs.7a and 7b, respectively.

The most prominent feature in those images is the dark pattern in the central area of the cell that is observed in the EL image (7b) but not in the PL image (7a). The PL image clearly shows that the reduced EL intensity from the central area is not caused by a deteriorated lifetime.

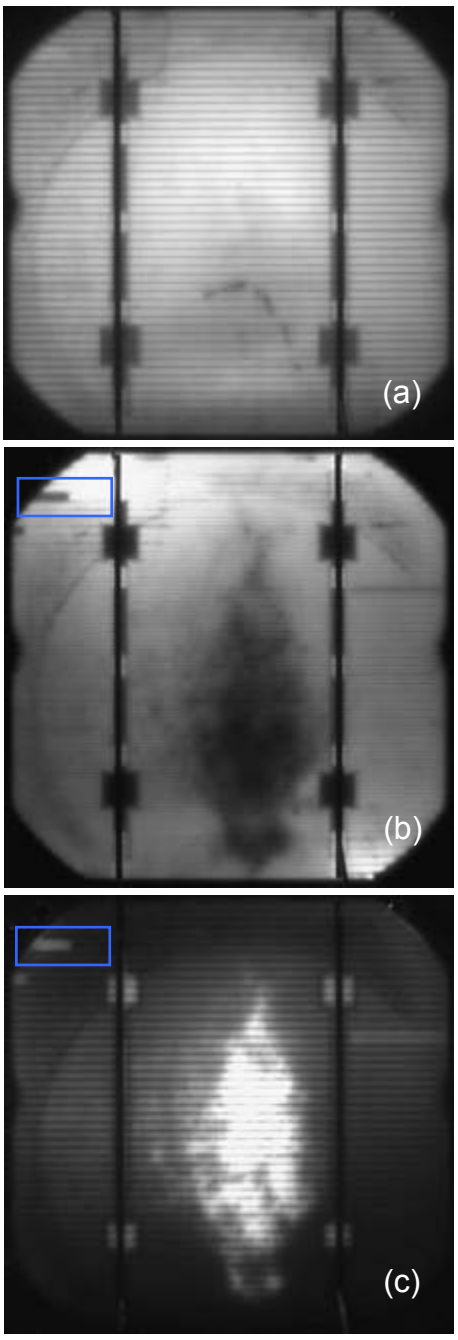

Fig.7 *Luminescence images of an industrial screen printed solar cell: (a) PL with ~1 Sun illumination, (b) EL with 25mA/cm^2 current density, (c) PL with external short circuit.*

Fig.7c shows a PL image that was taken with simultaneous control of the external voltage, a new variation of luminescence imaging that was introduced in Ref.26. In this case the two busbars were short circuited during the PL measurement. Clearly, exactly those areas that appear dark

only in the EL (7b) image but not in the PL image (a) appear bright in the short circuit image (7c). In Ref.26 it was concluded that the patterns in Fig.7b and 7c are caused by a locally enhanced series resistance. At forward bias a voltage drop over the series resistance causes a lower voltage across the junction in those areas and correspondingly lower luminescence intensity. In contrast, under illumination and with the busbars short circuited the voltage drop over the series resistance due to the current flow leaves the resistively coupled areas at higher voltage across the junction resulting in higher luminescence intensity. Another conclusive argument for the interpretation of the observed features in terms of series resistance variations is the fact that a very similar "chain-like" structure in the series resistance pattern that is particularly clear in the upper half of the EL image (7b) was also reported in Corescan measurements in the literature[23].

At this stage the analysis of luminescence images on finished cells in terms of series resistance variations is only qualitative, i.e. regions of higher and lower series resistance can be distinguished from each other. A quantitative analysis of series resistance images obtained from luminescence is currently under intense investigation at UNSW and from our initial experimental results there is no doubt that such a quantitative analysis is feasible. Compared to existing methods to measure series resistance variations luminescence imaging has the advantages that it is orders of magnitude faster, contactless, non-destructive and also detects series resistance variations at the rear surface, as for example in the areas under the square shaped silver pads on the rear (see Fig.7c).

The images in Fig.7 were taken with data acquisition times of 1s each. In the near future luminescence imaging could thus be utilised to monitor series resistance variations on finished cells in-line on every cell in an industrial production. Problems e.g. with the firing of the metal contacts, which can cause such series resistance variations, could then be recognized and rectified quickly.

A particular series resistance effect was observed on a very large number of screen printed solar cells from various manufacturers that were investigated at UNSW. Elongated areas along specific grid fingers appear dark in the EL image and bright in the PL image with external voltage control (blue square in Figs.7b and 7c). Inspection of such areas under an optical microscope revealed broken metal fingers in those locations. Some of these interruptions of the metal fingers are identified with the naked eye others are extremely narrow and would most likely not be detected in an automated optical inspection system. EL imaging or PL imaging with voltage control allow an unambiguous identification of broken metal fingers, which appears to be a common problem in industrial screen printed solar cells.

COMBINING LUMINESCENCE TECHNIQUES

A nice example of how different luminescence based characterization techniques, in particular QSS-PL lifetime measurements, Suns-PL and PL imaging can compliment each other is the application of these techniques during the recent development at UNSW of an edge isolation method for small area high efficiency solar cells[27]. It has been known for some time that even without shunted areas around the edge as in industrial screen printed solar cells, edge recombination can dominate the recombination in high efficiency silicon solar cells at low voltages (i.e. low carrier concentrations)[28]. It has also been suspected that edge recombination is responsible for an ideality factor n=2

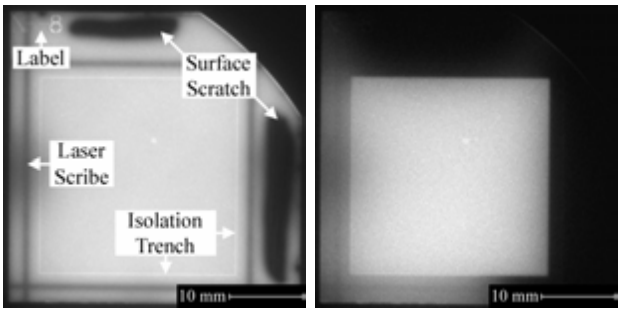

Fig.8 *PL images of a silicon wafer with isolation trench after laser scribing the rear surface and scratching the front surface, taken with ~5 Suns illumination intensity (left) and ~0.1 suns illumination intensity (right).*

that is often observed in the lower part of the IV curve of high efficiency devices. In order to isolate the edge from the active cell area it is sufficient to cut a passivated isolation trench at some distance around the perimeter of the cell area into the emitter, which is the only path for bulk minority carriers to reach the edge. PL techniques were used to test the effectiveness of that edge isolation method. The left hand side of Fig.8 shows a PL image taken with about 5 Suns equivalent illumination intensity of a wafer with such an isolation trench. The white square shaped line indicates the position of the isolation trench, which has a different surface roughness compared to the rest of the surface, resulting in slightly higher luminescence intensity. The black lines correspond to laser scribes on the rear surface of the wafer, the black areas at the top and on the right to diamond pen scratches through the emitter on the front surface. Fig.9 shows the Suns-PL (i.e. implied IV curves) measured contactlessly on one sample with isolation trench (label a) and on another sample without isolation trench, the latter after emitter diffusion (b) after laser scribing (c) and after scratching the front (d). The sample with the isolation trench was subject to the same processing but no measurable variation in the Suns-PL curves was observed before and after laser scribing and scratching, which already is a good indication that the active cell area is unaffected by what happens outside the isolation trench. Comparing curve a) and b) clearly shows an n=1 behavior in the wafer with isolation trench and an n=2 behavior in the wafer without the trench, which confirms the edge as the origin of enhanced n=2 recombination. The curves c) and d) show how laser scribing at the rear and scratching through the emitter lead to further enhancement of the n=2 contribution and to a

shunt-like behavior, respectively, which is a nice demonstration of how the influence of individual processes on the terminal characteristics can be quantified.

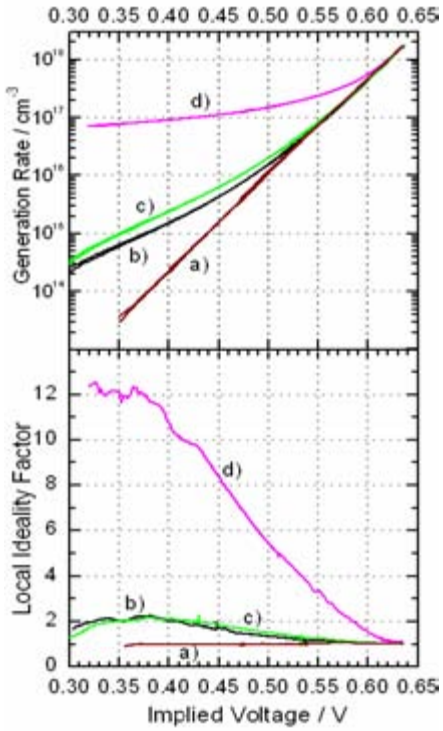

Fig.9 *Suns-PL curves (top) and corresponding local ideality factor curves (bottom). Curve (a) corresponds to the wafer with isolation trench from Fig.8, curves (b),(c) and(d) to an otherwise identical sample but without isolation trench, after: emitter diffusion, after laser scribing on the rear and scratching the front surface, respectively.*

It is interesting to compare the influence of the scratches on the PL images taken with high and low intensity. In the leftt hand image in Fig.8 the scratches through the emitter appear as relatively sharp and well localized areas. This is because at higher intensities the enhanced recombination in the scratched areas can no longer drag down the carrier density in the entire surrounding area because carrier flow into that area is impeded by the limited conductance of the emitter. The right hand of Fig.8 shows a PL image taken on the same wafer but with the equivalent of 0.1 Suns illumination. The carrier density (and thus luminescence intensity) in the entire area outside the isolation trench is dragged down by the high recombination in the scratched area, while the cell area located within the isolation trench is unaffected by anything that is done to the area outside the trench. The unimpeded flow of carriers through the emitter into high recombination areas at low illumination levels and the limited carrier transport at higher intensities lead to the shunt like IV curve (curve d), an effect that has been described in the literature[28] as "series resistance limited enhanced recombination".

Fig.10 shows QSS-PL lifetime curves on two 1 Ωcm n-type samples (one with and one without isolation trench) after emitter formation. The same trend as in the Suns-PL measurements is observed, i.e. the edge recombination dominates the recombination at low carrier densities in the sample without isolation trench, whereas the sample with isolation trench shows a typical Shockley Read Hall lifetime, i.e. bulk dominated recombination. At high intensities the lifetime curves converge, because as discussed above the cell area is then effectively isolated from the edge by the limited conductivity of the emitter. The graph clearly shows that in cases where an emitter (or more generally a junction) is present, edge recombination must generally be mitigated in order to get information about bulk properties.

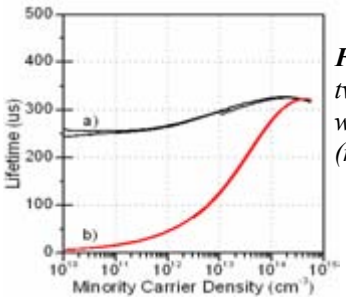

Fig.10 *QSS-PL lifetime of two 1Ωcm n-type samples with (black) and without (red) isolation trench.*

SUMMARY AND CONCLUSIONS

Luminescence based characterization techniques have been used in photovoltaics research for quite some time but have only recently been demonstrated to be competitive, fast and quantitative process monitoring tools that have some inherent advantages over existing, more established characterization techniques. Luminescence *imaging* (PL, EL and PL with external bias control) techniques are particularly promising for industrial applications, because with typical data acquisition times of 1s per high resolution image they close the gap that hitherto existed for spatially resolved process monitoring tools that are fast enough to be used for in-line photovoltaic manufacturing. Apart from the unrivalled short data acquisition times luminescence imaging is also attractive from a practical point of view for various other reasons: 1) Both textured and planar wafers of any practical size can be measured. 2) The samples remain at room temperature during measurements. 3) Measurements are not critically affected by temperature variations during measurements, i.e. no temperature control is required. 4) The measurements are non-destructive. 5) Scientific silicon cameras are commercially available and compared to IR cameras used in CDI/ILM or LIT they provide better spatial resolution are cheaper and generally more highly developed. 6) Luminescence imaging is simple to use and images are generally easy to interpret. After the fingerprint of a certain processing induced defect in the luminescence image (e.g. dark lines in EL images due to broken metal finger) has been identified images can even be interpreted by users without any scientific background.

PL imaging is particularly appealing because it is contactless and as such can be applied to silicon wafers before and after each manufacturing step, allowing a specific analysis of the influence of that processing step including

the possibility to identify sources of contamination in-line. Recent work in our labs has also shown that PL images can even be carried out on non-passivated raw material including mc-Si, string ribbon or EFG material, which may allow a whole range of industrial applications such as wafer quality monitoring and a correlation of the raw material quality with the electrical characteristics of the finished cell.

EL imaging and PL imaging with external bias control carried out on finished cells offer further attractive possibilities, only some of which (R_S-imaging, detection of broken metal fingers) have been mentioned or discussed here. Shunt detection by luminescence imaging is another interesting field that we are intensively working on with very promising initial results. In this specific case it is already clear that luminescence images will never provide as quantitative information about shunts as for example LIT methods. However, in many cases the qualitative information about the position of shunts combined with the knowledge of the influence of the shunt on the terminal characteristics (IV curve) of the cell are sufficient. The same holds for many aspects of luminescence images, where calibration e.g. into absolute lifetime or absolute series resistance variations is generally possible, but where the relative variation of those quantities across the image are often enough information to identify a problem. The rapid progress with the development of new or optimized cell concepts in the buried contact solar cell group at UNSW over the last year is an impressive example. We are confident that similar rapid improvements of cell efficiencies can be made in many industrial production lines especially when these techniques are applied to a large number of cells and/or wafers and correlated with the electrical characteristics of the cells. Our initial application of luminescence imaging techniques to solar cells from various manufacturers in which a variety of interesting and often unsuspected problems was identified confirms this view.

In short, luminescence imaging is an exciting new characterization tool that should find a variety of applications in PV research and in the PV industry that we have only started to explore. The combination of luminescence imaging with other imaging techniques such as LIT is one example of scientifically exciting projects that we are envisaging for the near future.

Acknowledgement: The Centre of Excellence for Advanced Silicon Photovoltaics and Photonics is supported under the Australian Research Council's Centres of Excellence Scheme.

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Characterization of Multicrystalline Silicon by Photoluminescence Spectroscopy, Mapping and Imaging

Michio Tajima, Hiroki Sugimoto, Masaaki Inoue and Kiyoto Araki

Institute of Space and Astronautical Science / Japan Aerospace Exploration Agency
3-1-1 Yoshinodai, Sagamihara 229-8510, Japan
Phone: +81-42-759-8325, Fax: +81-42-759-8463, E-mail: tajima@isas.jaxa.jp

Abstract

Spatially and spectrally resolved photoluminescence (PL) characterization was performed of recent multicrystalline Si wafers for solar cells. Comparison of band-edge PL intensity mapping and imaging with minority carrier diffusion length (lifetime) mapping on a whole wafer showed that low PL intensity regions correspond to short diffusion length (lifetime) regions. Microscopic PL mapping revealed that the low intensity regions are present inside grains and consist of micron-sized dot, line and/or plane defects. Low-temperature PL spectroscopy and mapping revealed that the dislocation-related lines, D1-D4, appeared only in the defect areas. We conclude that these defects are ascribable to dislocations decorated with heavy metals and are responsible for substantial degradation of the lifetime.

1. Introduction

Recent energy and environmental problems have created a broad and urgent demand for the development of solar cells. Multicrystalline silicon (mc-Si) solar cells are attracting much attention because of their recognized advantages of high-efficiency and low-cost. Previously the reduction of the effects of grain boundaries was most important because they acted as recombination centers and degraded the performance of the cells. The quality of the wafers has now been improved by enlarging the grain size; their size recently has been more than a few cm and an average minority carrier diffusion length of more than 400 μm.[1)] Under these circumstances, the effects of the intra-grain defects on the cell performance have become greater than those of grain boundaries.[2)] Understanding the electrical activity of the defects is essential to the development of high quality mc-Si wafers.

Photoluminescence (PL) spectroscopy is a powerful technique with which to analyze the electronic properties of defects and impurities in semiconductors, and highly spatially resolved PL mapping is quite useful to examine their distributions. The combination of spectrally and spatially resolved analyses allows us to discuss the origin of defects, the interaction between impurities and defects and the mechanism of defect formation. In this paper we review our recent investigations on defect characterization in the latest mc-Si using PL spectroscopy, mapping and imaging.[3,4)]

2. Experimental Technique

2.1 Samples

We describe the results of three mc-Si crystals (A, B and C) grown by a multi-stage solidification controlling method [5)]. Samples A and B were sliced parallel to the growth direction from the ingots fabricated with rapid and slow solidification, respectively. Sample C was sliced perpendicular to the growth direction from the ingots fabricated with rapid solidification using a different furnace. Sample B had extremely large grain size which exceeded a few cm. They were boron doped with a resistivity ranging from 1.0 to 2.5 Ωcm, and their sawing damage was etched off by the HNO_3/HF solution. No further surface treatments

were necessary for PL measurements. Minority carrier diffusion length was measured for samples A and B by the surface photovoltage (SPV) technique. Minority carrier lifetime was measured for sample C by the microwave photoconductivity decay method.

2.2 PL Measurements

PL spectroscopy was performed at room temperature and liquid helium temperature (4.2 K) under the excitation of the 532 nm line of a Nd: YVO_4 laser and the 647 nm line of a Kr^+ laser. The excitation power and laser beam diameter were about 1-30 mW and 1-2 mm, respectively. PL from the samples was transferred to a grating monochromator and detected by a cooledGe pin diode. The detected signal was processed with a lock-in technique. The spectral response of the measurement system was calibrated with blackbody radiation.

We used three systems for investigating the spatial variation of PL intensity on wafers. The characteristics of the three systems are summarized in Table I. For macroscopic and microscopic mapping we used an apparatus of wafer-scanning type, which had an accurate and fast *X*-*Y* stage with a position-repeatability as high as 0.3 μm and a maximum translation speed of 100 mm/s.[6] The spatial resolution of the macroscopic and microscopic mappings, which was determined by the beam diameter, was set at about 300 μm and 10 μm, respectively, in the present study. Luminescence light was collected by the objective, passed through narrow band-pass filters to extract a specific spectral component, and detected by a cooled InGaAs photomultiplier. The detected signal was processed with the lock-in technique. A typical time required for a wafer mapping shown in this paper was about 30 min.

Low-temperature microscopic mapping[7] was performed for the region of interest. Sample chips were cut from the wafers and mounted on a temperature-variable cryostat. The excitation laser beam was deflected by the mirrors and focused on the sample surface with a diameter of 10 μm. PL from the sample was collected with an *F*=1.5 lens system and passed through narrow bandpass filters, and then transferred to a cooled Ge pin diode. A typical time required for a 1 mm x 1mm area mapping was about 120 min.

Table I. Comparison of our apparatus for investigating the spatial variation of PL intensity.

	Scanning-Wafer Type	*Scanning-Beam Type*	*Imaging*
Practical Spatial Resolution	1 - 500 μm (variable)	10 μm	50 - 500 μm (variable)
Measurement Area	1x1 - 300x300 mm^2	1x1 mm^2	5x5 - 150x150 mm^2
Position Repeatability	± 0.3 μm	± 2 μm	-
Sample Temperature	Room Temperature	15 - 300 K	Room Temperature
Excitation	UV - Visible Laser (266, 364, 488, 532, 647, 1064 nm)	Visible Laser (488, 532, 647, 1064 nm)	LED array (370, 500, 900 nm)
Detector	InGaAs Photomultiplier (-80°C)	Ge pin diode (-200°C)	CCD (-80°C)
Spectral Range	0.4 - 1.7 μm	0.4 - 1.7 μm	0.4 - 1.1 μm
Spectroscopic Mapping	Yes (Band-edge and deep-level emission)	Yes (Band-edge and deep-level emission)	No (Only band-edge emission)
Max. Data Points	1000 x 1000	100 x 100	1024 x 1024
Typical Meas. Time	15 - 30 min	100 - 150 min	1 - 100 sec

Recently Trupke *et al.*[8] demonstrated the effectiveness of PL imaging for fast characterization tool for mc-Si wafers and solar cells. We also tried PL imaging by using a cooled CCD camera and an LED array as an excitation source. Near IR light from the LED was cut by filters, and the band-edge emission from Si was extracted by bandpass filters. PL intensity patterns similar to those by PL mapping were obtained; an example is shown in Fig. 8. Although the data acquisition time for PL imaging was just 1-100 s which is two or three orders of magnitude shorter than our scanning-wafer type PL mapping, the practical spatial resolution was inferior to our PL mapping.

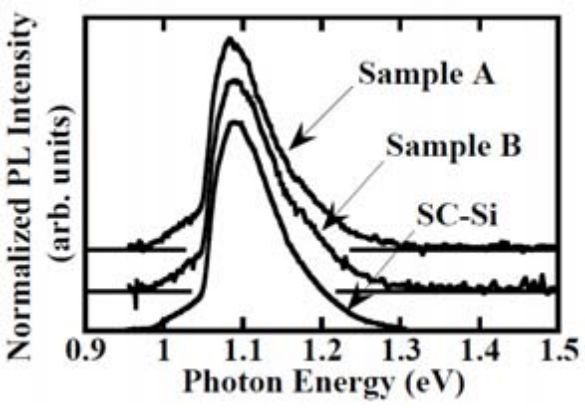

Fig. 1. PL spectra from sample A, sample B and typical sc-Si wafer at room temperature. Each PL intensity was normalized at peak.

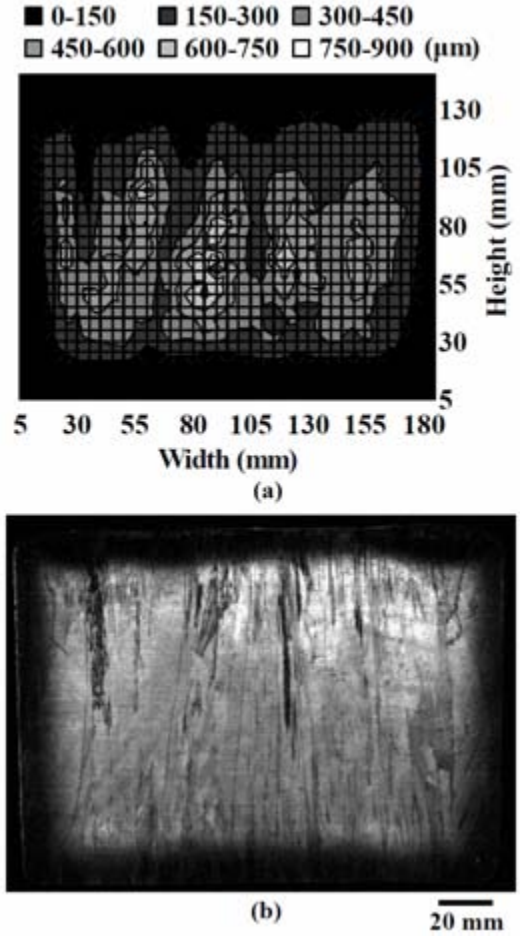

Fig. 2. Comparison between (a) distribution of minority carrier diffusion length and (b) PL macroscopic mapping (185 x 140 cm^2) on sample A. Whiter regions indicate higher PL intensity. Interval of sampling points is about (a) 5 mm and (b) 0.5 mm, respectively.

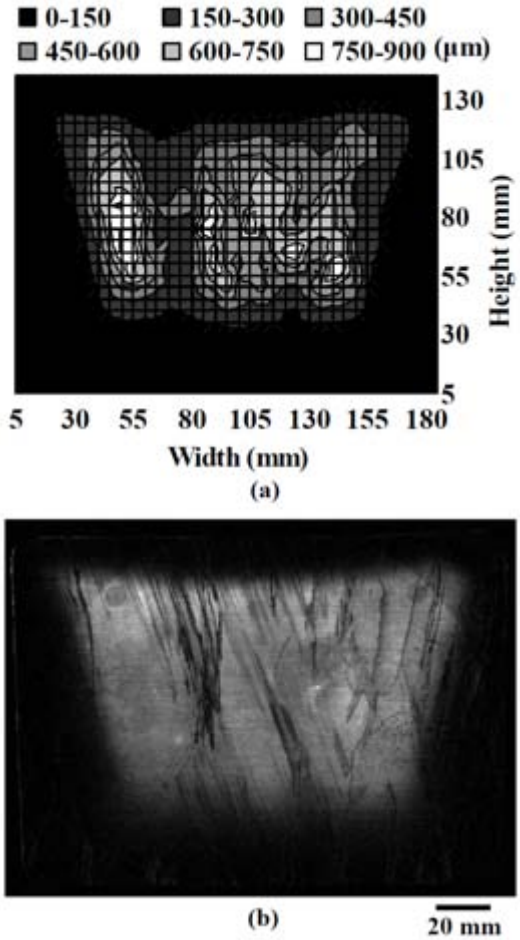

Fig. 3 Comparison between (a) distribution of minority carrier diffusion length and (b) PL macroscopic mapping (185 x 140 cm^2) on sample B. Interval of sampling points is (a) 5 mm and (b) 0.5 mm, respectively.

3. Results and Discussion

3.1 Room-Temperature PL Spectroscopy

Near band-edge PL spectra from the shorter and the longer minority carrier diffusion length region on samples A and B were obtained by the PL spectroscopy at room temperature.[3] We show PL spectra of the longer diffusion length region on samples A, B and of a typical single crystalline Si (sc-Si) in Fig. 1. The PL intensity of sample A is 20 % higher than that of sample B. That of sc-Si is higher than that of mc-Si. However, the full-width at half-maximum (FWHM) of PL spectra are hardly different. This shows that the crystallinity of the longer diffusion length region on sample A and B are almost the same as that of sc-Si.

PL intensity of the shorter diffusion length region is less than 20 % that of the longer diffusion length region, and the FWHM of PL spectrum of the former region is 18% wider than that of the latter region. Deep-level emission is below our detection limit. From these results, we confirmed that the crystallinity of the shorter diffusion length region is degraded.

3.2 Wafer Mapping

We compared the PL macroscopic mapping with the distribution of minority carrier diffusion length on sample A as shown in Fig. 2.[3] Low PL intensity regions were observed on the periphery and the upper center regions of the sample. We found that these regions correspond to the short diffusion length regions. The degradation of the diffusion length on the periphery is known to be due to the iron contamination during the solidification of the ingot. The high spatial resolution of the PL mapping enables us to find that dark patterns exist in these regions. We confirmed that these dark patterns are not due to surface scratches, because nearly the same patterns were obtained from backside of the sample. High PL intensity regions do not necessarily correspond to the long diffusion length regions; the PL intensity increases on upper regions of the sample while the long diffusion length regions exist on the center. We can estimate that this is because upper regions of the sample have a low resistivity, that is, a high impurity concentration.

Comparison between the distribution of minority carrier diffusion length and the PL macroscopic mapping on sample B is shown in Fig. 3. Just same as sample A, low PL intensity regions were observed on the periphery and the upper center regions of the sample. We also confirmed that low PL intensity regions correspond to the short

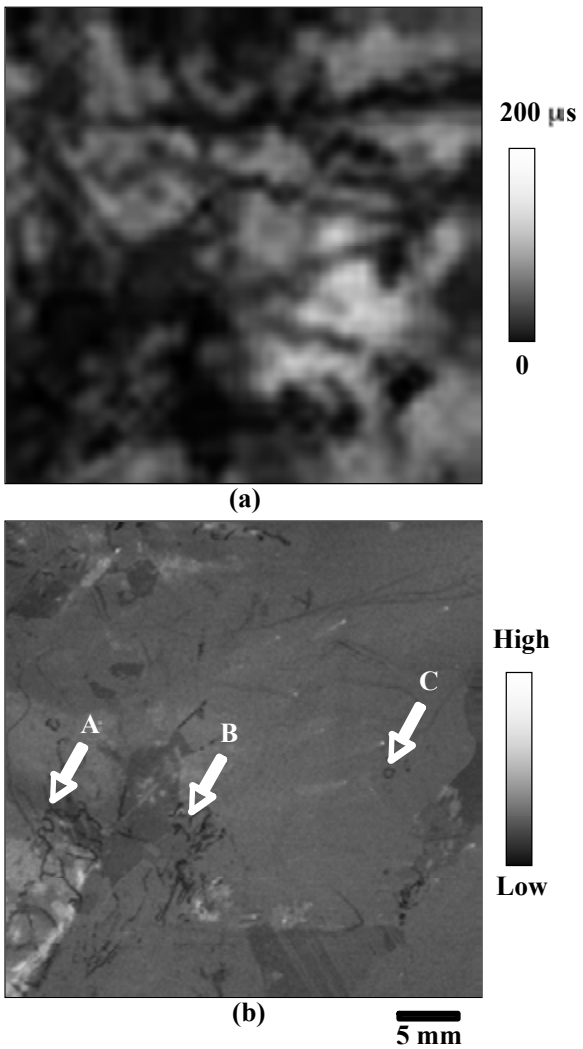

Fig. 4. Comparison between (a) minority carrier lifetime mapping and (b) band-edge PL mapping on sample C. Whiter region indicates long lifetime and high PL intensity region. Spatial resolution of (a) and (b) is 1 mm and 100 μm, respectively.

diffusion length regions. Dark areas on the periphery spread wider than that of sample A. This is because sample B was suffered from plenty of the iron contamination during the long-term solidification. In the PL mapping, we can find that dark lines exist on center regions. From these results, we assumed that these dark lines relate to the defects which degrade the cell performances.

Figure 4 shows a comparison between the band-edge PL intensity mapping and the minority carrier lifetime mapping on sample C.[4] We found that the low PL intensity regions correspond to the short lifetime regions, while the pattern of the grain boundaries hardly correlates with the distribution of the lifetime. The spatial resolution of the PL mapping was ten times higher than that of the lifetime mapping, which enabled us to learn there are dark-line PL patterns in the short lifetime regions. We also confirmed that there are few dark-line patterns in the long lifetime regions as in the case for samples A and B.

3.3 Microscopic Mapping

We zoomed into the short and long diffusion length regions on samples A and B with the PL microscopic mapping, as shown in Figs. 5 and 6.[3] Figure 5 (a) shows the short diffusion length

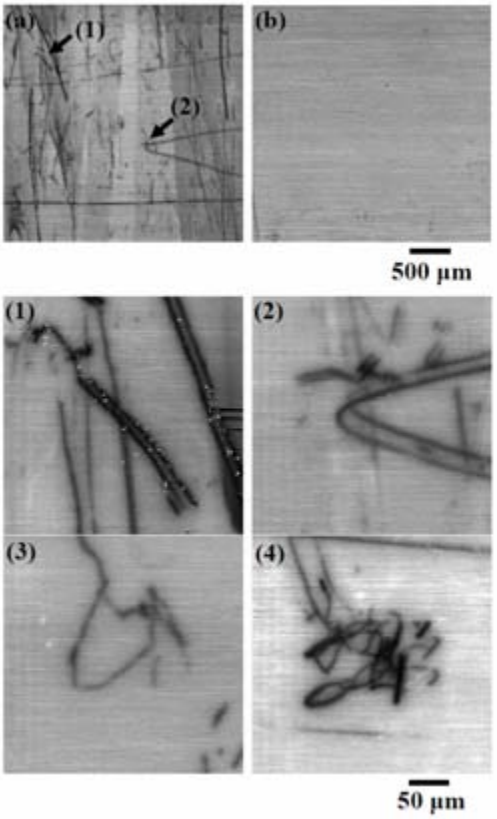

Fig. 5. PL microscopic mappings (3 x 3 mm^2) in (a) short minority carrier diffusion length region (shorter than 100 μm) and (b) long minority carrier diffusion length region (longer than 700 μm) on sample A. (1)-(4) are PL microscopic mappings (300 x 300 μm^2) nearby characteristic micro patterns. (1) and (2) are indicated in (a). (3) and (4) were obtained from different areas. Interval of sampling points of (a) and (b) is 10 μm and that of (1)-(4) is 1 μm.

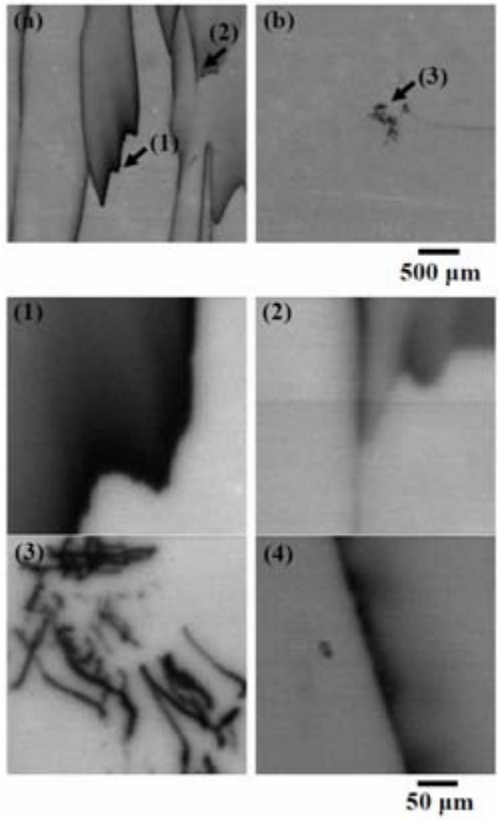

Fig. 6. PL microscopic mappings (3 x 3 mm^2) in (a) short minority carrier diffusion length region (shorter than 100 μm) and (b) long minority carrier diffusion length region (longer than 700 μm) on sample B. (1)-(4) are PL microscopic mappings (300 x 300 μm^2) nearby characteristic micro patterns. (1)-(3) are indicated in (a) or (b). (4) was obtained from different area. Interval of sampling points of (a) and (b) is 10 μm and that of (1)-(4) is 1 μm.

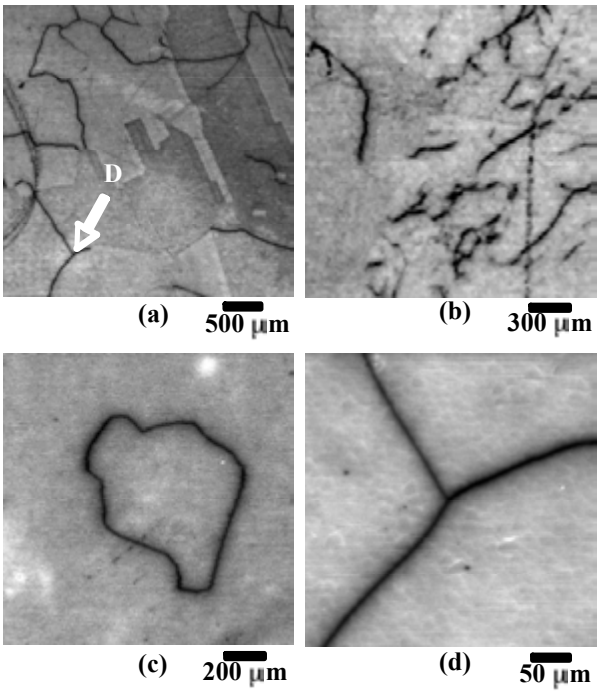

Fig. 7. PL microscopic mappings in short minority carrier lifetime region on sample C with higher spatial resolution than 10 μm. (a), (b), (c) and (d) is the identical region shown in Fig. 4(b) A, B, C and Fig. 7(a) D, respectively.

region of sample A. There are plenty of dark lines and some dark planes; densities of these patterns are about 2000 lines/cm^2 and 30 planes/cm^2. Since grain boundaries are known to induce background contrast variations, we conclude that these dark patterns are not grain boundaries. The long diffusion length region of sample A is shown in Fig. 5 (b). There are few lines; the density of dark lines (about 20 lines/cm^2) is much less than that of short diffusion length regions. We investigated more closely around characteristic micro patterns of sample A, as illustrated in Fig. 5 (1)-(4). We found that many kinds of micro patterns exist, such as (1) twin lines, (2) twin curved lines, (3) a loop and (4) spirals.

Figure 6 (a) presents the short diffusion length region of sample B. Patterns are quite different from sample A; almost all patterns are dark planes (about 100 planes/cm^2). The long diffusion length region of sample B is shown in Fig. 6 (b). Though some dark spirals happen to exist in this region, there are few dark patterns around over 1 cm^2; the density of patterns is about 5 spilals/cm^2. We investigated more closely around characteristic micro patterns of sample B, as illustrated in Fig. 6 (1)-(4). We also found that many kinds of micro patterns exist, such as (1)-(2) planes, (3) spirals and (4) a dot.

We further examined the short lifetime regions of sample C, as shown in Fig. 7.[4] Various characteristic patterns, such as dark lines, micron-sized dark spots and a dark loop were observed. Figure 7 (a), (b), (c) and (d) is the microscopic mapping on the area marked A, B, C in Fig. 4(b) and D in Fig. 7(a), respectively.

From the optical microscope image, we determined that these patterns do not originate from surface scratches or the grain boundaries. Therefore, we believe that these patterns originate from the intra-grain defects responsible for the degradation of the lifetime. There was a strong resemblance between these patterns and the well-established dislocation patterns.

3.4 PL Mapping *vs* PL Imaging

We compared PL mapping with PL imaging for samples A and A', where the two samples were sliced parallel and perpendicular to the growth direction, respectively, from the same rapid-solidified ingot. Essentially the identical PL intensity pattern was observed for PL mapping and imaging as shown in Fig. 8. The practical spatial resolution for PL mapping was better than that for PL imaging. It should be pointed out that the PL pattern for sample A looks like poles parallel to the growth direction, while that for sample A' exhibits a cellular structure. The latter pattern was also observed for sample C sliced perpendicular to the growth direction. From these findings we speculate that the dark-line defects distribute along walls of a tube-like structure. We hypothesize that the diameter of the tube is larger for slow-solidified sample B

than for rapid-solidified sample A.

3.5 Low-Temperature Spectroscopy and Mapping

To analyze the origin of the intra-grain defects, we performed low-temperature PL spectroscopic measurement.[4] In Fig. 9, PL spectra from the long and short lifetime regions are presented. The PL spectrum of Fig. 9 (a), (b) and (c) was obtained from the short lifetime region in Fig. 7 (c), (b) and (a), respectively. Figure 9 (d) depicts one of the examples of the spectrum taken from the long lifetime regions. The 1.093 eV line marked B_{TO} is the TO-phonon replica of the boron bound exciton. Intensity of B_{TO} from the long lifetime regions was higher than that from the short lifetime regions. In the short lifetime regions, D1-D4 lines which were reported to be due to dislocations [9] were observed besides the band-edge emission. In Fig. 9 (a), the D1 and D2 lines broadened and the spectral shape was similar to the spectrum reported by Tarasov *et al.* [10] on mc-Si wafers grown by a edge defined film-fed growth technique. The intensity of the D1 line was extremely low in Fig. 9 (b). To our knowledge, there have been no reports on the D-line spectrum missing only the D1 line. Broadband emission around 0.86 eV appeared in Fig. 9 (c) in addition to the D1-D4 lines. The origin of the 0.86 eV band has not yet been revealed. The deep-level luminescence from the long lifetime regions was below our detection limit. The sharp line at 1.00 eV in Fig. 9 (d) was not the D4 line but the zone-center optical phonon sideband of the two-hole transition in the boron bound exciton. These findings show clearly that the intra-grain defects relate to the dislocations. We also found that the D-line spectral patterns, that is, the variation of the full-width at half-maximum (FWHM), relative intensities and peak positions of the

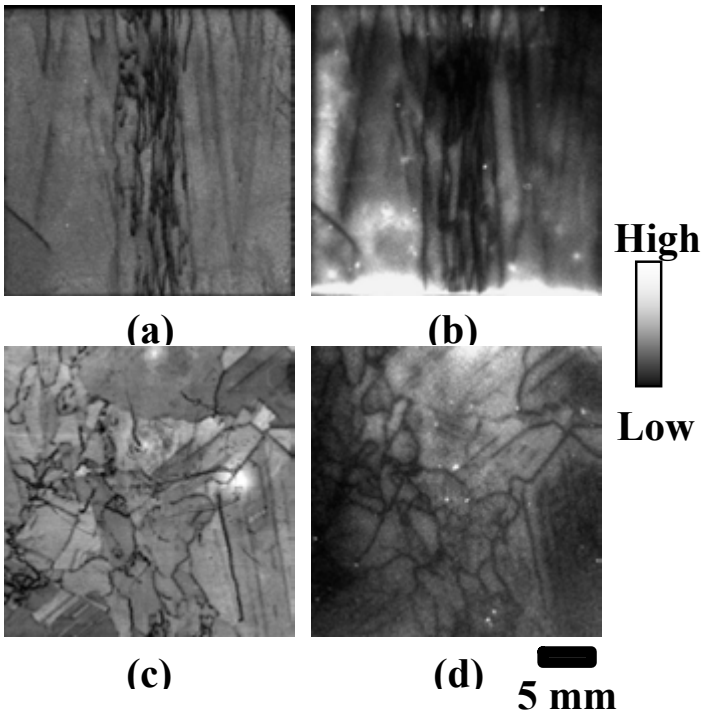

Fig. 8. Comparison between (a)(c) PL mapping and (b)(d) PL imaging. (a)(b) samples A and (c)(d) sample A' were sliced parallel and perpendicular to the growth direction, respectively, from the same ingot.

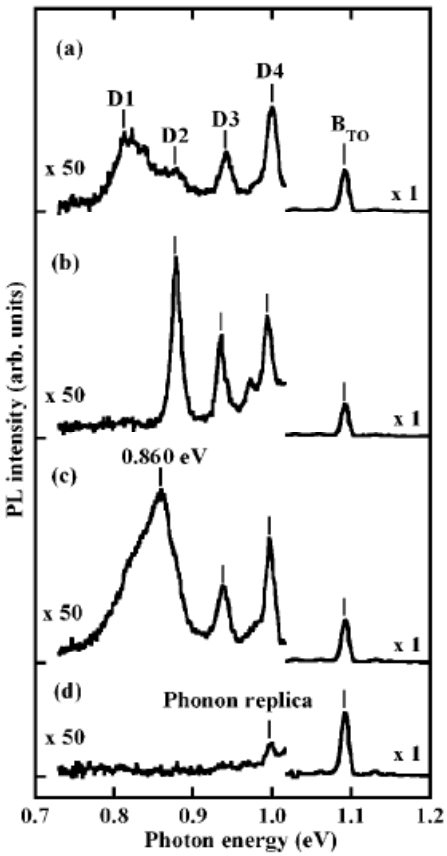

Fig. 9. PL spectra at 4.2 K of (a)-(c) short minority carrier lifetime regions and (d) long lifetime region. Symbol 'x 50' denotes relative amplitude.

D-lines, differ depending on the measurement points.

We performed microscopic mapping of the above low-temperature PL lines around the loop-like dark-line defect in Fig. 7(c). The intensity mapping of the band-edge (BE) and D1-D4 lines at 15 K are shown in Fig. 10, where that of the BE emission at room temperature is also shown in (a) for comparison. Although only the loop-like pattern was observed at room temperature, partitioned segments were recognized beside the loop for the BE line at 15 K. The intensity patterns for D1-D4 lines were grouped into two categories: D1/D2 and D3/D4 lines. It should be noted that this grouping also occurred for mapping of D1-D4 lines in dislocated sc-Si, such as plastically deformed float-zoned Si[9,11] and oxygen-precipitated Czochralski-grown Si.[12] The intensity of the D1/D2 lines was lower on the loop and was surrounded by a bright area. This feature is characteristic to the pattern for D1/D2 line in dislocated sc-Si, and the effect of the metal contamination has been discussed. The D3/D4 lines showed the segmented pattern similar to the BE line. The contrast of the respective segments was, however, almost opposite with respect to the BE line.

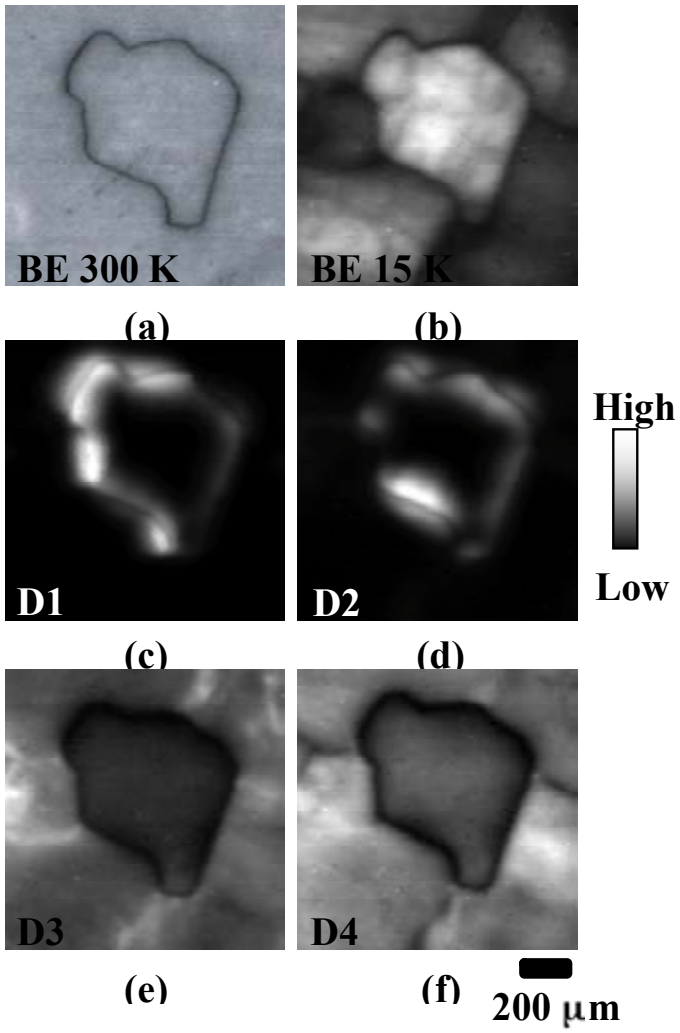

Fig. 10. PL mappings around loop-like defect at (a) room temperature and (b)-(f) 15 K. (a) and (b) are intensity mapping of band-edge emission, and (c), (d), (e) and (f) are that of D1, D2, D3 and D4 line, respectively.

The D-line spectral pattern is dependent on the density and the type of dislocations [9]. In addition, the recombination activity of dislocations greatly depends on the metal contamination.[11,13] Arguirov *et al.* suggested that the D1 and D2 lines would be especially influenced by a local condition such as material stress [14]. We believe that the intra-grain defects observed in the PL mapping are dislocations decorated with the heavy metals, and we theorize that the variety of the D-line spectral shape reflects the variation of the dislocation density and the amount of metal contamination.

4. Conclusions

We have characterized defects in the latest mc-Si using PL spectroscopy, mapping and imaging. The dark-line PL patterns existed in the short minority carrier diffusion length (lifetime) regions. PL microscopic mapping revealed that the dark lines consisted of micron-sized dot, line and/or plane defects. We found that these defects were responsible for the considerable degradation of the lifetime but the grain boundaries did not primarily degrade the lifetime. For low-temperature PL spectroscopic measurement, dislocation-related lines, D1-D4, were observed

only in the defect areas. The intensity patterns for D1-D4 lines were examined microscopically around the defect at 15 K. The patterns were categorized into the D1/D2 and D3/D4 group, as in the case for the grouping in dislocated sc-Si. We believe that the inra-grain defects observed in the dark-line patterns are ascribable to dislocations decorated with the heavy metals.

Acknowledgements

The authors would like to thank T. Saito, M. Dhamrin, K. Kamisako, I. Yamaga and T. Eguchi for the supply of samples A and B and other related samples together with their diffusion length data and for useful discussions and comments. They are also indebted to Y. Ohshita, A. Ogura, K. Arafune and K. Kakimoto for the supply of sample C with their lifetime data and for helpful discussions and comments.

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Circuit-based Analysis of Injection Level Dependent Lifetime Data

J.E. Cotter, F.W. Chen, M.D. Abbott, T.A. Li and K.C. Fisher
Centre of Excellence for Advanced Silicon Photovoltaics and Photonics
University of New South Wales, Sydney, Australia 2052

Abstract

This paper outlines a technique to analyze photoconductance and photoluminescence lifetime data based on PSPICE circuit simulation. Free and commercially available circuit simulation packages are easy to use and can quickly solve circuits with a wide variety of elements, including custom elements. The circuit-based approach is advantageous when considering non-symmetrical devices, and especially devices that are affected by complex, non-linear parasitic electrical effects, like scratches, cracks, damaged edges, edge-junction recombination and edge-bulk recombination. Here, we present an equivalent PSPICE model of a typical lifetime test device and exercise the model in a few case studies.

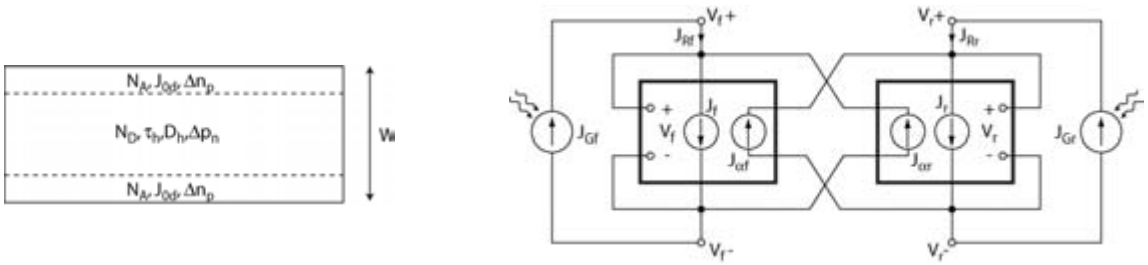
1. Introduction

Photoconductance (PC) and photoluminescence (PL) lifetime spectroscopy techniques are one of the most important characterization tools for the development and manufacture of crystalline silicon solar cells. Both techniques are contactless, so they can be applied to partially finished solar cells, allowing process monitoring of solar cells in many stages of fabrication, allowing fast and direct development of solar cell processes and designs. Quasi-steady state photoconductance (QSS-PC) [1,2] lifetime techniques have been used successfully for a wide variety of applications. Photoluminescence lifetime techniques [3,4], coupled with photoluminescence imaging techniques [5,6,7], are rapidly emerging as a powerful tool for characterizing and developing solar cell processes and designs.

In this paper, we use a circuit-based approach to extend the analysis of QSS-PC and QSS-PL lifetime data taken on samples containing p-n junctions. We use a freeware student version of PSPICE9.1 [8], which has a good graphical-user-interface that allows circuit layouts and simulations to be set up quickly and provides fast and flexible numerical solutions to complex, non-linear circuits. The paper first develops an equivalent PSPICE circuit model of a typical QSS-PC or QSS-PL test device, and then examines three case studies to demonstrate the utility and flexibility of the circuit-based analysis technique.

2. Equivalent Circuit Models

Figure 1a shows a typical test devices used for PC or PL measurements, for example, for lifetime monitoring, diffusion optimization or surface passivation studies. The device comprises a high-lifetime, n-type silicon wafer with both surfaces p+ diffused and both surfaces well passivated. An equivalent circuit model of this test device structure is shown in Figure 1b.



(a) (b)

Figure 1. (a) Cross sectional diagram of a typical PC or PL test device, and (b) Ebers-Moll equivalent circuit.

Under nearly all PC or PL illumination conditions, the diffused regions remain in low injection, however the n-type base region may be in either high or low injection. For the work presented here, we use high-quality silicon wafers and take care to preserve the wafer lifetime during processing. Thus, we make the "narrow-base" assumption, which is that the minority carrier diffusion length in the base region is much longer than the width of the wafer. We also assume flat quasi-fermi levels across the depletion regions and quasi-neutrality everywhere outside of the depletion regions. For the case of Figure 1, the recombination current densities in the two junctions can be described using an Ebers-Moll [9] model of two coupled recombination currents. We use the Taylor series expansion $\coth(x) \approx 1/x + x/3$ and approximate the base recombination current associated with either junction as $q \cdot W \cdot \Delta p_n / 2 \cdot \tau_b$ to arrive at

$$J_{Rf} = J_f - J_{\alpha r} \approx \left(\frac{q \cdot D_h}{W} + \frac{1}{3} \cdot \frac{q \cdot W}{\tau_p} \right) \cdot \Delta p_{nf} + \frac{J_{0d}}{n_i^2} \cdot \Delta p_{nf} \cdot \left(\Delta p_{nf} + N_D \right) - \left(\frac{q \cdot D_h}{W} - \frac{1}{6} \cdot \frac{q \cdot W}{\tau_p} \right) \cdot \Delta p_{nr}$$

$$J_{Rr} = J_r - J_{\alpha f} \approx \left(\frac{q \cdot D_h}{W} + \frac{1}{3} \cdot \frac{q \cdot W}{\tau_p} \right) \cdot \Delta p_{nr} + \frac{J_{0d}}{n_i^2} \cdot \Delta p_{nr} \cdot \left(\Delta p_{nr} + N_D \right) - \left(\frac{q \cdot D_h}{W} - \frac{1}{6} \cdot \frac{q \cdot W}{\tau_p} \right) \cdot \Delta p_{nf} \qquad (1)$$

where Δp_{nf} and Δp_{nr} are the excess minority carrier concentrations at the edge of the front and rear depletion regions, respectively; N_D and W are the doping level and width of the base, respectively; and τ_p, D_p and J_{0d} are the minority

carrier lifetime in the base, the minority carrier diffusivity and the saturation current density of the diffused regions, respectively. The voltage of each junction V_f or V_r is related to the excess minority carrier population at the respective depletion region edge by the standard expression that accounts for high injection conditions in the base region:

$$\Delta p_{nf} = \frac{N_D}{2}\left[\sqrt{1+4\cdot\frac{n_i^2}{N_D^2}\cdot\left(\exp\left(\frac{qV_f}{kT}\right)-1\right)}-1\right] \text{ and } \Delta p_{nr} = \frac{N_D}{2}\left[\sqrt{1+4\cdot\frac{n_i^2}{N_D^2}\cdot\left(\exp\left(\frac{qV_r}{kT}\right)-1\right)}-1\right] \quad (2)$$

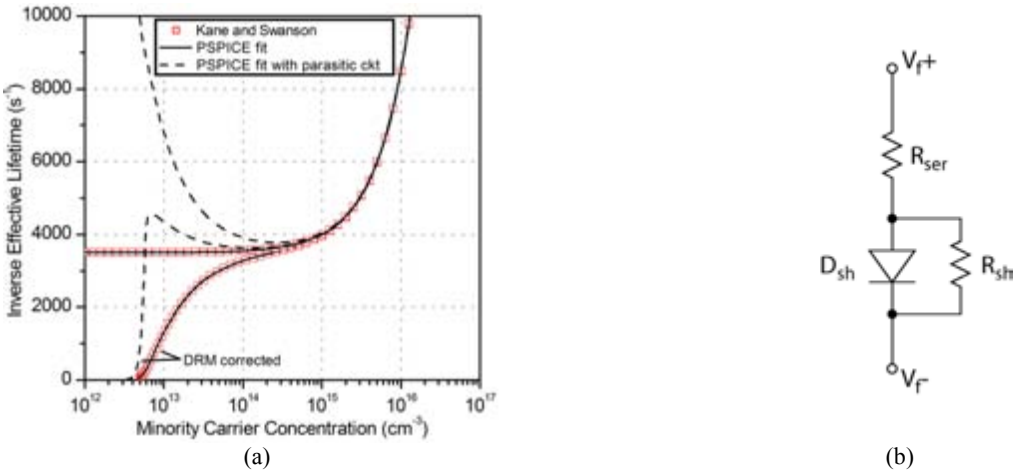
Together, (1) and (2) describe the implied J-V characteristics of the device of Figure 1a, but in a form that is convenient for PSPICE simulation in the circuit shown in Figure 1b. In the general case of $\Delta p_{nf} \neq \Delta p_{nr}$, the excess minority carrier concentration is not uniform in the base. The narrow-base assumption, however, implies that the excess carrier populations Δp_{nf} and Δp_{nr} decrease linearly away from their respective depletion region edges to zero at the opposite depletion region edges. Superimposing the minority carrier populations associated with the front and rear junctions and integrating the recombination over the width of the base region leads to an expression for the effective lifetime

$$\frac{R_{tot}}{\overline{\Delta p_n}} \equiv \frac{1}{\tau_{eff}} = \frac{J_{Rf}+J_{Rr}}{\overline{\Delta p_n}\cdot q\cdot W} = \frac{J_{Gf}+J_{Gr}}{\overline{\Delta p_n}\cdot q\cdot W} \text{ where } \overline{\Delta p_n} = \frac{\Delta p_{nf}+\Delta p_{nr}}{2} \quad (3)$$

Summing equations for J_{Rf} and J_{Rr} for the symmetrical case of $\Delta p_{nf} = \Delta p_{nr}$ and transforming using equation (3) leads to the familiar inverse lifetime expression of Kane and Swanson [10] (with twice the diffused region saturation current):

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_p} + \frac{2\cdot J_{0d}}{q\cdot W\cdot n_i^2}\cdot\left(\Delta p_n + N_D\right) \quad (4)$$

A typical simulation varies the generation current J_G over several orders of magnitude and collects voltage data at both junctions. The properties of the test device are modelled in PSPICE using equations (1) and (2), which are programmed into a PSPICE "GVALUE" 4-port transconductance circuit element and the circuit layout shown in Figure 1b. Parasitic effects are modelled by adding additional circuit elements to the Ebers-Moll circuit at the appropriate location. A scratch on the front surface, for example, might be modelled with a shunt resistor, or other circuit, across V_f+ and V_f-. The inverse effective lifetime graph is produced by converting the J_G-V data into $1/\tau_{eff}$-Δp_n data using equations (2) and (3). Figure 2a shows a baseline simulation of a symmetrical Ebers-Moll circuit and confirms its equivalence of the Kane and Swanson expression.



(a) (b)

Figure 2. (a) Comparison of lifetime curves extracted from PSPICE simulation and the Kane and Swanson lifetime expression (for τ_b = 0.001 s; W = 0.025 cm; J_{0d} = 100 fA/cm^2; D_h = 11 cm^2/s; N_D=5e15 cm^{-3}), with depletion region modulation (DRM) included in the QSS-PC calculation. (b) Parasitic circuit element used in (a) to produce the altered (dashed line) lifetime curves (R_{ser}=1000 Ω; R_{sh}=∞ Ω; N_{Dsh}=2.0; IS_{Dsh}=50 nA/cm^2) to demonstrate its effect on lifetime curves.

The point of developing the Ebers-Moll model and deploying a circuit-based analysis is (1) to emulate the asymmetrical case of $\Delta p_{nf} \neq \Delta p_{nr}$, which can occur, for example, when a sample is illuminated or diffused differently on one side compared to the other, and (2) to emulate complex, non-linear parasitic effects, which can also affect the test device asymmetrically. We have observed a wide variety of physical defects and their influence on QSS-PC and QSS-PL lifetime data, including scratched surfaces, cracked wafers, chipped edges, edge-junction and edge-bulk recombination. Such parasitic effects can interfere with lifetime-based experiments and, in some cases, degrade the performance of high efficiency solar cells. In most cases, these parasitic effects can be detected by QSS-PC and QSS-PL techniques, in the low injection region of the lifetime data. To illustrate this, Figure 2a includes a plot that includes the influence of a hypothetical parasitic effect, modelled with the circuit in Figure 2b (in this case, resistance limited, edge-junction (n=2) recombination). In this case, the analytical solution is transcendental, so numerical techniques, like those employed by circuit simulators, are required.

3. Three Brief Case Studies

Figures 3 illustrates some of the kinds of parasitic effects that we observe on lifetime test structures at UNSW. It shows a PL image of a high-lifetime, n-type, float zoned silicon wafer with oxide-passivated boron diffusions on both surfaces. We have observed a wide variety of physical defects with PL imaging techniques [6,7] and their influence on PC and PL lifetime data [11]. In the image of Figure 3, dark regions on the image correspond to a various physical defects including scratches from 4-point probe measurements, edge damage from the quartz diffusion boat, one completely dead edge (cause unknown) and other unidentified sources of poor PL response.

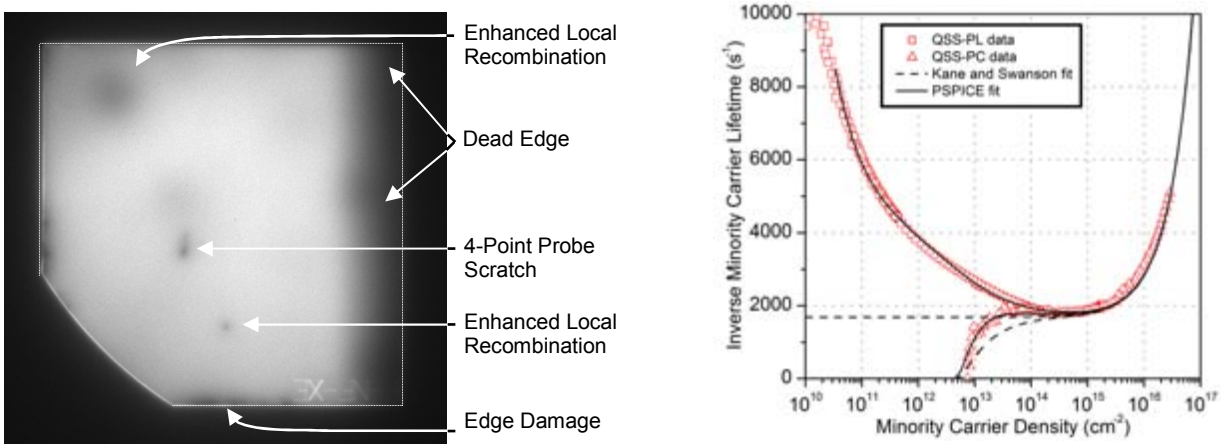


Figure 3. (a) PL image of a double-side boron-diffused, thermal oxide passivated, n-type float-zoned silicon wafer showing regions of low effective lifetime and causes, where known. The physical edges of the wafer are outlined with a thin white line. (b) QSS-PC and QSS-PL data of the wafer shown in (a) with (dashed line) Kane and Swanson fit and (solid line) PSPICE fit using the parasitic circuit shown in Figure 2b (R_{ser}=600 Ω; R_{sh}=0.8 MΩ; N_{Dsh}=1.1; IS_{Dsh}=1000 fA/cm^2).

QSS-PC and QSS-PL data for the sample of Figure 3a are shown in Figure 3b, along with a best fit of the data using the Kane and Swanson model and data extracted from a PSPICE circuit model. The Ebers-Moll equivalent circuit model includes the circuit element shown in Figure 2b across the V_f+ and V_f- terminals to emulate the defects apparent in the PL image of Figure 3.

Our choice of the lumped parameter circuit model for this simulation is somewhat arbitrary, but not unreasonable. Neither injection-level-dependent Shockley-Read-Hall bulk or surface recombination, nor a purely resistive parasitic circuit (a linear shunt) provides very good fitting for any reasonable set of recombination parameters or circuit parameter values. On the other hand, various combinations of R_{ser}, R_{sh}, N_{Dsh} and IS_{Dsh} provide a reasonably good fit to the data. More experimental data is needed to extract equivalent circuit parameters with any confidence, but nonetheless, the success of the fit shows that a circuit-based approach to lifetime analysis is effective at simulating the kinds of complex, non-linear behaviour apparent in the QSS-PC and QSS-PL lifetime data shown in Figure 3b.

Figure 4 shows lifetime data extracted from QSS-PC measurements made on two silicon nitride passivated, high-lifetime, n-type, float zoned silicon wafers, each boron-diffused on both surfaces. The two samples are identical, with the exception of the boron diffusions (50 Ω/sq versus 240 Ω/sq), including the type of silicon nitride film used for passivation and the annealing environment. The lifetime data of the two samples are strikingly different, however. Each sample was fitted using PSPICE simulation of the Ebers-Moll circuit with the parasitic lumped parameter model of Figure 2b. A good fit is achieved by varying the diffusion saturation current and bulk lifetime while keeping the parameters of the parasitic circuit R_{ser}, R_{sh}, N_{Dsh} and IS_{Dsh} fixed for each sample.

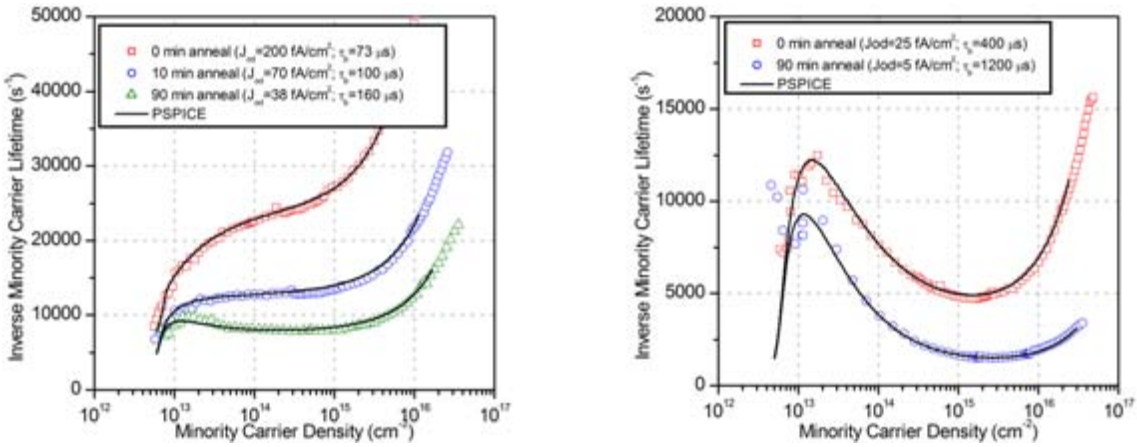


Figure 4. Two boron-diffused samples passivated with a silicon nitride film at various stages of annealing. Left: QSS-PC data and PSPICE fit for a 50 Ω/sq boron diffusion with PSPICE fits (R_{ser}=700 Ω; R_{sh}=∞ Ω; N_{Dsh}=2; IS_{Dsh}=60 nA/cm^2). Right: QSS-PC data and PSPICE fit for a 240 Ω/sq boron diffusion (R_{ser}=20 Ω; R_{sh}=∞ Ω; N_{Dsh}=2; IS_{Dsh}=18 nA/cm^2).

Figure 5 shows generation-rate vs. implied voltage data extracted from QSS-PL measurements made on a boron-diffused, oxide passivated high-lifetime, n-type, float zoned silicon wafer. The sample was tested from both sides and then deliberately scratched on one side using a diamond pen (after [11]) and retested from both sides. The unscratched curves were fitted using PSPICE simulation of a symmetric Ebers-Moll circuit (J_{0d}=20 fA/cm^2; τ_h=750 μs; W=0.025 cm) with asymmetric illumination (J_{Gf}/J_{Gr} = 3.3). The scratched curves were fitted by adding the parasitic circuit shown in Figure 2b to either the front (V_f+ to V_f-) or the rear (V_r+ to V_r-) junction. A good fit is achieved by fixing all circuit parameters and adding the parasitic circuit of Figure 2b to either the front or rear of the circuit. The relatively poor fit of the unscratched measurements is due to an ideality factor of slightly greater than one (n≈1.09) for the main junctions of the test device, which is not accounted for in the equivalent circuit model presented here.

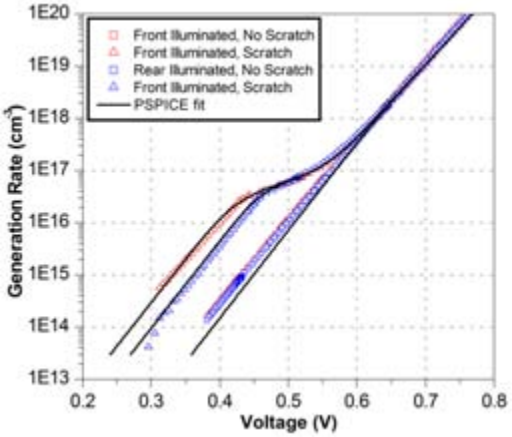


Figure 5. QSS-PL data expressed as generation rate vs. voltage data and PSPICE fit for a boron-diffused, oxide passivated sample before and after scratching from one side. The sample was measured from from the front (scratched) side and rear (not scratched) side (R_{ser}=450 Ω; R_{sh}=∞ Ω; N_{Dsh}=1.1; IS_{Dsh}=300 pA/cm^2).

4. Conclusions

Circuit-based techniques are helpful in extending the analysis of QSS-PC and QSS-PL lifetime data. Circuit simulators are easy to use and provide fast numerical solutions to complex circuit layouts that cannot be solved analytically. We emulated a typical double-side passivated and diffused lifetime test structure with an Ebers-Moll equivalent circuit. Although we did not present equivalent models here, it should be straightforward to extend the circuit-based analysis to include p^+nn^+, or even n+nn+, test devices, with appropriate expressions for equation (1). Also, the narrow-base assumption is not necessary to employ circuit-based analysis, although the form of equation (1) will be modified.

The three case studies illustrate the applicability of the technique, however, additional experimental work would be needed to extract equivalent circuit parameters with any confidence. At least, some insight can be gained into the nature and influence of parasitic effects that influence lifetime data taken on test samples that contain p-n junctions. Applications of the technique might include characterization or monitoring physical defects (scratches, cracks or edge damage) or characterization of edge recombination processes and development of schemes to minimize their effects.

5. Acknowledgements

The authors would like to thank Thorsten Trupke and Robert Bardos for helpful discussions on the interpretation of QSS-PL and QSS-PC data. This work was funded by the Australian Research Council through the Centres of Excellence Scheme.

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Bulk passivation of mc-Si solar cells: Summary of the Crystal Clear workshop.

H.F.W. Dekkers – IMEC vzw, Belgium
I.G. Romijn and A.W. Weeber – ECN Solar Energy, The Netherlands
G. Hahn – University of Konstanz, Germany

On Nobember 3rd 2005, a workshop on the passivation properties of amorphous hydrogenated silicon nitride was held within the 6th European Framework Program integrated project Crystal Clear. Four contributing European research centers organized this public workshop to exchange knowledge on this topic. This workshop was a unique opportunity to define and discuss open questions around this topic. In this paper, presentations discussions and conclusions are summarized.

Introduction

Amorphous hydrogenated silicon nitride (SiNx:H) is an extraordinary surface anti-reflection coating for silicon solar cells. Its ability to passivate both surface and bulk of multi-crystalline substrates increased the overall efficiency of industrially applicable solar cells. This led to a fast and successful introduction of SiNx:H coatings into large scale solar cell production. Despite this application in PV, the passivating properties of a-SiNx:H are still under debate. To help this debate forward and to exchange knowledge, insights and experience, a public workshop was organized within the 6th European Framework Program integrated project Crystal Clear. ECN (The Netherlands), UKON (Germany), Fraunhofer ISE (Germany) and IMEC (Belgium) organized this workshop, held on November 3rd 2005 at IMEC in Leuven, Belgium. Around 85 people from all over the world attended this workshop. The 3 subjects of discussion were the different deposition systems with their corresponding processes, bulk passivation of silicon wafers and surface passivation. In this paper, we summarize the presentations and discussions on bulk passivation. An overview of the understandings, open and ideas is given, completed with some additional results obtained after the workshop. While we will refer to the presentations given at the workshop (all available on the web: www.ipcrystalclear.info), we will mention the publications where some of the presented results can also be found.

The crucial questions concerning bulk passivation from SiNx:H

Plasma assisted deposition of SiNx:H is a successful method to achieve silicon surface passivation of crystalline silicon solar cells. As, in addition, SiNx:H shows excellent optical properties, it is particularly attractive for the front side layer, acting both as surface passivation layer and good anti-reflection coating. But this successful combination is not the only reason why the rather complicated deposition method of SiNx:H found its way into commercial cell manufacturing. SiNx:H provides an effective and fast hydrogenation process for defected Si materials. This hydrogenation occurs simultaneously with the formation of rear and front contacts by firing or thermal treatment. The introduction of this process in cell manufacturing turned out to be the turning point towards commercial high efficiency mc-Si cells. Despite the fast introduction of PECVD silicon nitride, some questions always return: 1. Is it really the hydrogen that passivates defects, and, if yes, which defects are getting passivated? 2. What are the required properties of SiNx:H to guarantee the most optimal bulk passivation? 3. What is the exact mechanism behind this passivation?

Monitoring of hydrogen release and diffusion

The fact that the first question is still asked reflects the difficulty to monitor hydrogen diffusing from the silicon nitride layer into the Si bulk. It is well established that hydrogen bonded to Si and N is released at annealing temperatures above the deposition temperature of the SiNx:H layer. However, the rapid thermal contact formation process (contact firing) is often too fast to expect a significant release of hydrogen from the silicon nitride layer. Moreover, the concentration of hydrogen in the silicon substrate after firing is found to be very low.
To detect hydrogen in SiNx:H layers, Fourier Transformed Infra Red (FTIR) measurements or Elastic Recoil Detection (ERD) is used. In the

first method, infrared (IR) absorption by Si-H and N-H bond vibrations is measured. In the second method, ions accelerated towards the SiNx:H sample recoil atoms with a mass smaller than the impacting ions. By analyzing the energy of the recoils, their concentration over the depth of the sample can be determined. Using heavy ions to recoil H from the SiNx:H provides information on absolute hydrogen concentrations. Both techniques found a decrease of hydrogen concentration in SiNx:H, after thermal treatment with temperatures close to the estimated values in the contact firing process [1,2,3]. However, there is one limitation. To be able to detect a significant decrease, the thermal treatments need to be extended, e.g. 5 minutes at 800°C (ECN [1]) or 30 minutes at 560-690°C (IMEC [2]). The total amount of hydrogen being released is not always easy to determine accurately from FTIR measurements. The Utrecht University concluded that care has to be taken for determining the hydrogen concentration from FTIR [3].

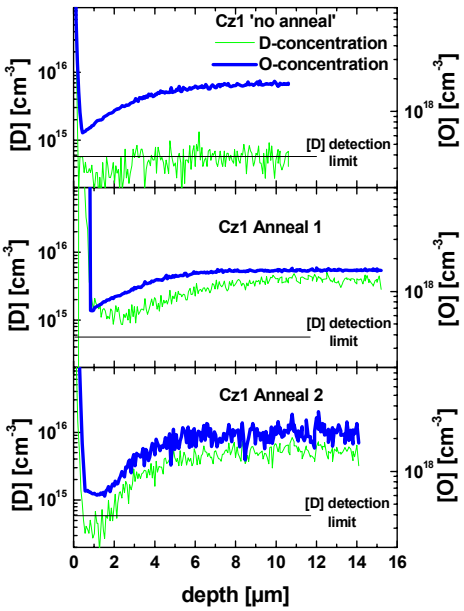

Figure 1, Deuterium profiles of oxygen rich Si. Deuterium concentration increases due to the creation of oxygen related traps, obtained by different anneals. After [4]

A combination of FTIR and ERD showed that obtained IR absorption constants for Si-H and N-H bonds are different from values found in the literature. The different compositions of the film probably have a direct effect on this coefficient.
Another point is that it is hard to find a significant concentration of hydrogen back into the Si by methods such as Secondary Ion Mass Spectroscopy (SIMS) after thermal treatment; especially when SIMS detection is carried out after treating the samples correctly. This means that one has to use a hydrogen isotope (Deuterium) in the silicon nitride and the removal of the nitride layer after thermal treatment is necessary. Deuterium is used as a kind of tracer to circumvent the problems of a high background signal of SIMS, originating from residual moisture in the vacuum chamber. Silicon nitride has to be removed since the high atomic concentration in the layer causes a 'push-in' effect during the ion sputtering, which overshadows the hydrogen (deuterium) concentrations near the silicon surface. Deuterium concentration inside (mc)-Si quickly drops below the detection limit at depth of more than 100 nm [4,5]. During the contact firing, temperatures above 800°C are high enough to diffuse hydrogen deep into the silicon [6]. The only requirement is that hydrogen is in atomic form.
Hydrogen (Deuterium) concentration in Si rises if hydrogen is trapped as is the case in oxygen rich material. UKON found that plasma hydrogenation of oxygen rich ribbon material is slower due to the oxygen related traps [4]. Trapping of Deuterium by oxygen also occurs during firing of SiNx:D layers (Figure 1). With formation of oxygen related traps it was proven that hydrogen diffuses deep into the bulk Si, leading to an estimate that the diffused amount is around 10^{14} cm^{-2}. It means that only 0.1 – 1 % of the total Deuterium concentration is released from the SiNx:H layer, which is in agreement with the almost undetectable release of hydrogen upon short annealing observed from FTIR. Deuterated nitride experiments on thin-film polysilicon layers (grain size between 0.1 and a few µm) have shown very high Deuterium incorporation in such layers [7, 12].

Defect passivation from SiNx:H hydrogenation

Surprisingly, despite the relatively low hydrogen concentration in the SiNx:H layers, hydrogenation occurs in defected mc-Si material. There are many evidences for this hydrogen passivation from SiNx:H. Generally, they are presented as an increase in solar cell performances or, more directly, an increase of the minority carrier lifetime. Still it is unclear which defects are passivated in mc-Si. It is very unlikely that passivated defects are dangling bonds as is the case in poly-Si (material with grain size in the µm range).

Rinio *et al*. nicely demonstrated that dislocation networks are one of the most recombinative areas of mc-Si, especially after the phosphorous diffusion process [8]. From several other experiments it is clear that those dislocations are internal gettering centers, where metals are clustered. Those areas that are subject to hydrogen passivation from SiNx:H. Rinio *et al*. also demonstrated that recombinative grain boundaries can be passivated with silicon nitride. It was even shown that the electrical activity of the grain boundary is lowered with the well known improvement of PECVD SiNx:H by adding hydrogen to the plasma [9,10]. The passivation of decorated areas gives us a hint that the defects that get passivated are related to metals. Until now, the exact nature of the defects remains unclear. Nevertheless, it can be said that there is convincing evidence that hydrogen, originating from the deposition of SiNx:H, diffuses into mc-Si and passivates defects.

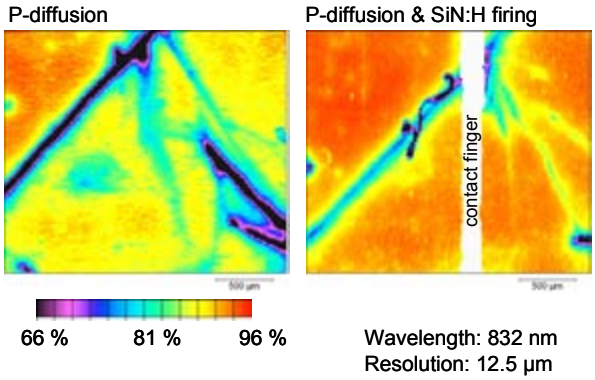

Figure 2, Light induced current mapping on neighboring substrates, demonstrating the improvement from SiNx:H induced hydrogenation. After [8]

Where exactly this hydrogen comes from has been a matter of debate. One hypothesis is that the hydrogen is incorporated into the silicon during the nitride deposition, in the thin, damaged surface region of the Si substrate, and not from the nitride layer itself. This would be consistent with the low amount of hydrogen that is found to diffuse into the substrate. The plasma used for nitride deposition is hydrogen rich due to dissociation of SiH_4 and NH_3. A pre-treatment with a NH_3 plasma, often used to improve the interface quality of the SiNx:H layers, i.e. to avoid blister formation during firing, often somewhat improves the solar cell characteristics. One can argue that this pre-treatment acts as a hydrogenation step. This hypothesis has to be extended according a few important findings presented in the workshop:

1. Bulk passivation has been found to depend on the 'quality' of SiNx:H layers, which is determined by the deposition parameters.
2. Bulk passivation is also observed when high quality layers are deposited on top of thin SiNx:H layers of low quality.
3. The SiN_x:H layer can be used several times as a source of hydrogen.
4. From SIMS measurements, it is observed that the Silicon-Silicon Nitride layer is not a diffusion barrier.
5. Experiments with thin-film polysilicon material demonstrate that the incorporated amount of hydrogen (deuterium) during nitride firing is much more than what is introduced during a simple deposition.

PECVD Tdep	LPCVD Thickness	Jsc [mA/cm2]	Voc [mV]	Effective η [%]
250 °C	-	31.4 ±0.08	596.2 ±1.8	14.0
400 °C	-	32.9 ±0.10	607.0 ±0.3	15.0
400 °C	5 nm	33.1 ±0.05	607.9 ±0.9	15.1
400 °C	8 nm	33.1 ±0.04	609.0 ±0.4	15.1
400 °C	11 nm	32.7 ±0.02	604.5 ±1.1	14.8

Table 1, cell characteristics for SiNx:H on top of thin LPCVD layers.

The extent of bulk passivation depends on the quality of the SiNx:H which in turn depends on the deposition parameters. This fact alone cannot disprove the hydrogenation-during-deposition hypothesis. Stronger evidence that the SiNx:H layer itself is the hydrogen source is obtained from the other points. Point 2 was demonstrated earlier in [11], showing that bulk passivation from a stack consisting of a thin nitride at the interface and a thick nitride with different properties is not determined by the thin layer but by the thick top layer. Similar experiments in which a thin hydrogen poor or hydrogen free layer was first deposited (respectively LPVCD and reactive sputtering with nitrogen), led to the same conclusion. Despite the absence of hydrogen in the interface layer, similar cell results can be achieved when there is a layer of high quality SiNx:H deposited on top of that thin layer (see Table 1). As long as the interface layer is not too thick (acting then as a diffusion barrier for hydrogen), the cells show a similar hydrogenation effect. An initially hydrogen free silicon near the interface SiNx:H has seemingly no influence on the final cell efficiency.

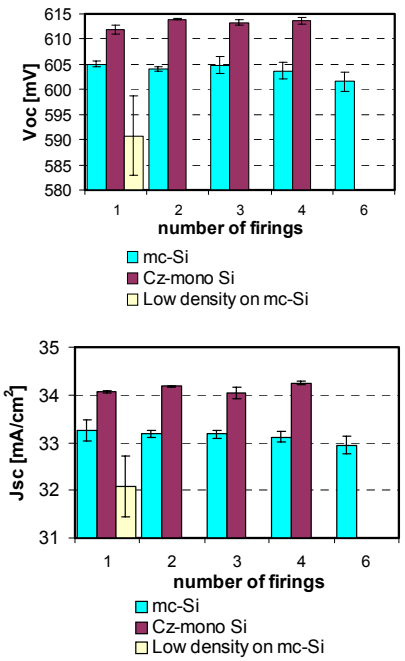

Figure 3, cell characteristics after multiple firing steps. The number of firing steps includes the last step, in which the contacts were realized. Results show that both Voc and Isc start to drop at the sixth firing. For comparison, results of a low density silicon nitride are given. After [2]

Point 3 is illustrated in Figure 3. Here, not yet metallized solar cell samples were fired several times before the final metal screen printing and firing steps were carried out. It is shown that multiple firing is possible, up to 4 times, without degradation of the cell characteristics. This shows that a SiNx:H layer can be used several times, before the stored hydrogen becomes exhausted. If hydrogen originated from the silicon near the interface, it should already be fully diffused after the first firing step and no longer available for passivation during subsequent thermal treatments. Again, a sample with low quality silicon nitride was added in the experiment for comparison.

Those results are consistent with earlier observations that hydrogen in silicon nitride diffuses slowly, and that not all hydrogen is released during the firing process. In Figure 4, deuterium diffusion profiles in nitride layers are shown. They depend on the density of the silicon nitride and clearly show the hydrogen diffusion length to be in the range of 20-200 nm. Point 4 is illustrated in Figure 5 where is shown that this hydrogen diffusion is not hindered by the Silicon-Silicon nitride interface. Deuterium, diffusing out of a SiNx:D layer, sandwiched between two SiNx:H has diffusion profiles towards the surface and towards the silicon substrate, equal and almost symmetrical in shape. If the interface was a barrier to Deuterium, the profile as plotted in green would occur. This is clearly not the case. Once the Deuterium reaches the silicon, its diffusion is accelerated dramatically, testified by the sudden drop in concentration. Thus even if there is hydrogen incorporated in the Si near the SiNx/Si interface, the release of hydrogen from SiNx:H cannot be neglected.

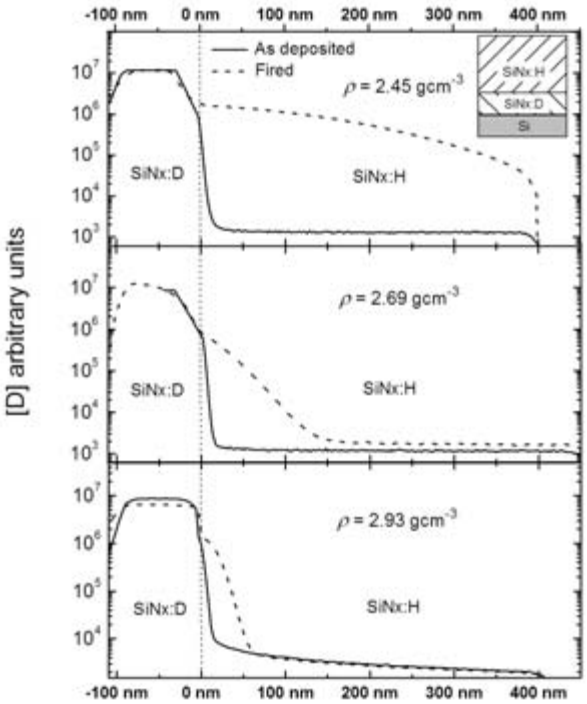

Figure 4, Deuterium diffusion through SiNx:H layers of different density. The depth is rescaled to the SiNx:D/SiNx:H interface.

Finally point 5 is illustrated in Figure 6. Here one looks to the incorporation of deuterium in poly-Si layers, before and after firing [12]. Because the grains of poly Si are very small, the concentration of hydrogen/deuterium traps is much higher than in Cz or mc-Si. Any form of hydrogenation can be observed easily by measuring concentrations with SIMS. It is observed that during deposition, a small amount of deuterium indeed is incorporated in the layer. However, this amount is much lower than the final concentrations after firing. Clearly, most deuterium diffuses from the silicon nitride. The amount of deuterium initially present in Si after deposition is very small compared to the amount diffusing from the nitride layer. However, the amount of incorporated hydrogen might play some role. In fact, with carefully executed bulk lifetime measurements improvements can even be detected after SiNx:H deposition without firing.

So the deposition temperature of around 400°C is high enough to diffuse some of the hydrogen into the bulk [13]. But of course one cannot distinguish if the hydrogen comes from the Si/SiNx:H interface or is diffusing out of the SiNx:H layer during deposition.
It is reasonable to expect that the situation for poly-Si can be extended to the case of mc-Si, because the 'quality' of the silicon nitride has exactly the same effect on both poly-Si and mc-Si.

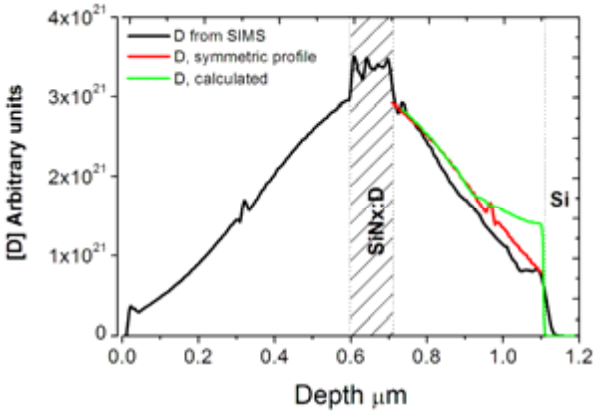

Figure 5, diffusion profile of Deuterium, diffusing from a SiNx:D layer, sandwiched between to similar layers of SiNx:H of equal density. The red curve is a mirror image of the deuterium diffusing towards the surface (on the left side of the SiNx:D layer). The green line is the calculated profile, assuming that no hydrogen penetrates through the Si interface.

Optimizing SiNx:H

The influence of certain deposition parameters of SiNx on bulk passivation was already determined in early experiments on SiNx:H induced passivation. For example, in LF PECVD a higher deposition temperature leads to a better bulk passivation. However, this trend is not caused by the hydrogen incorporation during deposition, but to a better 'quality' of silicon nitride. This 'quality' is strongly related to the density of the silicon nitride film which can be modified by the deposition parameters [2]. The importance of density was first observed by Hong *et al.* [14] who showed that the film density is dependent on the deposition method. Similar trends in density were clearly observed by other groups [1,2,15,16] (see Figure 7-9). Of four different deposition methods, presented at this workshop, it was found that bulk passivation is optimal at a high density. For the expanding thermal plasma deposition of OTB [16], the maximum is achieved at 2.5 g/cm^3. ISE obtained a similar maximum as IMEC: 2.9 g/cm^3, which is getting close to LPCVD SiNx (3.0 – 3.1 g/cm^3) or the ultimate density of crystalline Si_3N_4 (3.19 g/cm^3).

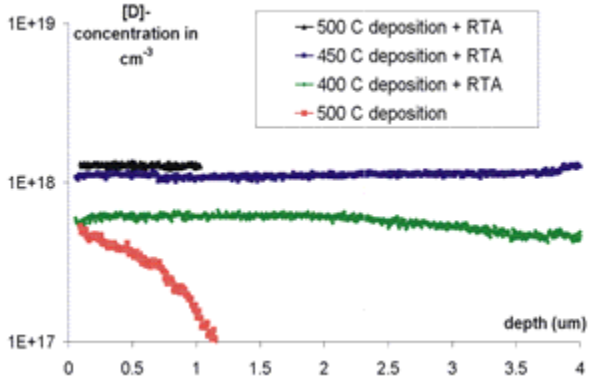

Figure 6, deuterium profiles in Poly-Si films before and after firing (RTA) of SiNx:D ARC layers. The given deposition temperature corresponds to the SiNx:D density. After [12]

ECN defined the density of SiNx:H in Si-N bond concentration, observed by FTIR. This is a slightly different definition for density and takes the stoichiometry into account. They found an optimum at 1.3x10^{23} cm^{-3} Si-N bonds and at a larger density the passivation starts to decrease [1]. This drop of passivation for layers beyond the optimal density is also observed by ISE and might be related to the low concentration or low diffusivity of hydrogen in those layers. From experiments of the individual participants it is not completely clear whether an absolute optimal density of SiNx:H exists. This might depend also on the Si/N ratio and hydrogen concentration in the film, which again influences the density [1].

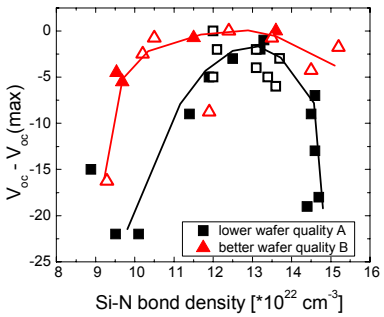

Figure 7, Open symbols: SiNx:H layer made with NH3 + SiH4, Closed symbols: SiNx:H layer made with N2 and SiH4. After [1]

A round robin within the Crystal Clear project, organized by ISE showed that passivation results for different deposition methods are equal [15]. It appears that the quality of SiNx:H deposited by different methods can be optimized so that the difference in bulk passivation between different deposition systems is minimal.

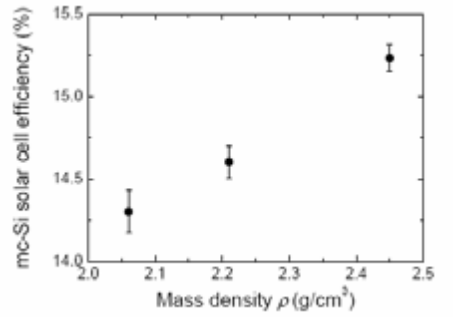

Figure 8, cell efficiency as a function of mass density of SiNx:H ARC, deposited with expanding thermal plasma. After [16].

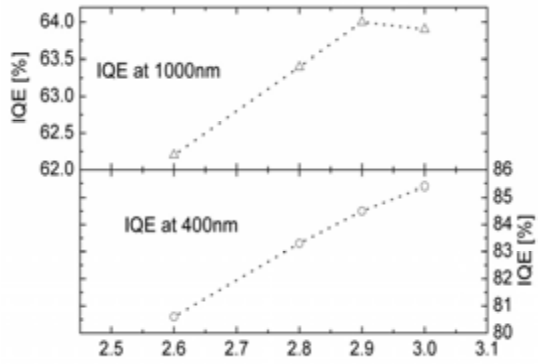

Figure 9, IQE as a function of mass density of sputtered SiNx:H ARC, deposited with reactive sputtering. After [15].

Release mechanism

A paradox arises when one considers the amount of hydrogen stored in the SiNx:H layers and the amount of hydrogen released during annealing. The denser the SiNx:H layers, the less hydrogen is incorporated in the films and the more stable the Si-H and N-H bonds are against thermal annealing, which means that less hydrogen is released from the film. One would therefore expect that bulk improvement decreases with increasing density. However the opposite is true. An explanation to this apparent contradiction can be found in the way hydrogen is released. It is widely accepted that hydrogen gets released in molecular form according the reaction

$$\text{Si-H} + \text{N-H} \rightarrow \text{Si-N} + \text{H}_2.$$

Evidence for this reaction is found in the fact that the release of hydrogen happens with a simultaneous increase of Si-N bond density. This can be directly monitored by FTIR (ECN [1]), but also by the decrease of the etch rate in liquid HF or the increase of tensile stress (IMEC [2]). This reaction is exothermic and might therefore explain the relatively easy release of hydrogen, which is difficult to explain assuming that atomic hydrogen gets released by breaking the strong Si-H or N-H bond directly. The transition point of the H_2 release reaction is unknown but is probably small for low density nitride films since it must be strongly dependent on the configuration energy. If the distance between N-H and S-H sites is large, or when the SiN network is less flexible, it is hard to bring those sites together for the reaction to take place. So the reaction requires more energy to occur. In other words, the energy of the transition point is higher. Therefore this reaction is less likely to happen in dense silicon nitride, which generally has lower hydrogen concentrations and a less flexible structure. It is therefore proposed that for dense nitrides hydrogen is released in atomic form instead in of taking place in molecular form.

Effusion experiments on SiNx:H/SiNx:D/SiNx:H stacks have given strong evidence that hydrogen is released in atomic form. In effusion experiments, species diffusing out of samples at high temperatures are measured by mass spectroscopy. Hydrogen and deuterium are always detected in molecular form, since recombination of atoms always occurs, at the surface or in the vacuum ambient [17]. Evidence for release of atomic hydrogen can be found in the flux of effusing HD molecules. A theoretical flux of HD, assuming that hydrogen/deuterium release is taking place under atomic form is calculated from the measured H_2 and D_2. This flux is compared to the measured HD flux (see Figure 10). At temperatures above 800°C, both fluxes become equal. This is an indication that at those temperatures, atomic hydrogen recombines with atomic deuterium in the vacuum ambient or inside silicon nitride. Thus atomic hydrogen in SiNx:H during thermal treatment definitely exists, even if it is only temporary. If hydrogen is mainly present in atomic form, it can be an explanation for the slow diffusion of hydrogen through dense SiNx:H. Experiments with an atomic deuterium ambient (deuterium plasma) shows that atomic

hydrogen diffuses slowly, independent of the density of the nitride. This is possible since atomic hydrogen is constantly trapped by broken Si and N bonds [2].

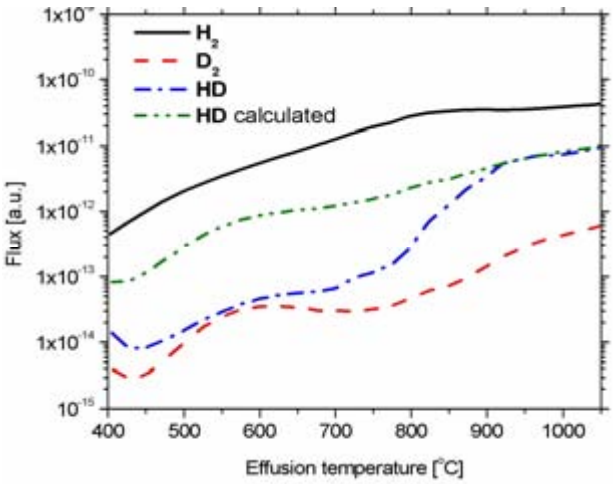

Figure 10, Effusion of H_2, D_2 and HD from nitride triple layers. H_2 and D_2 effusion rates are used to calculate the HD effusion rate for the case of diffusion by atomic H and D.

As discussed above, the extent of hydrogenation can be excellently monitored by hydrogenation of poly-crystalline Si layers. The grain-size determines the average concentration of dangling bonds and thus the amount of trapped hydrogen. It has been experimentally confirmed that poly-crystalline Si with grains in the range of 0.1-0.2 μm captures around 5-10 times more hydrogen than material with 1-5 μm grains. The density of the silicon nitride controls the passivation of the Poly-Si films. This is not only observed from electrical characteristics for the layer, but also directly from the amount of hydrogen (deuterium) incorporated in the poly-crystalline film (Figure 6). Low density nitride gives lower deuterium incorporation even though more hydrogen is released. The passivation of poly-Si films and the analogy with passivation of mc-Si clearly shows that the release of hydrogen from silicon nitride must be more in atomic form when the density of the silicon nitride increases.

A remaining question is: which mechanism is responsible for the formation of atomic hydrogen? How does the density of silicon nitride influence the release of hydrogen atoms from SiNx:H? A first possible explanation is that the hydrogen release shifts from the reaction of molecule formation to a direct release of atomic hydrogen, depending on the density. In that case, formation of atomic and molecular hydrogen are two competing reactions. If the formation of H_2 becomes difficult, the direct dissociation of Si-H or N-H bonds prevails.

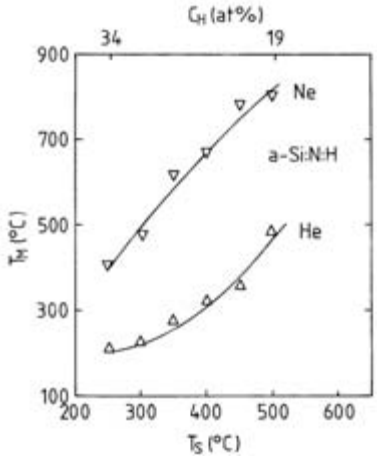

Figure 11,Temperatures (T_M) of effusion peaks for Ne and He, implanted in SiNx:H layers, deposited at different temperatures (T_S).

A second possibility is that there is a change of chemical potential for H_2 and H inside the SiNx:H. This change can be mediated by an increase of electron density of the silicon nitride film, which is a result of a higher density. The change of dissociation energy of H_2 inside SiNx:H might be the result. If the lowering of the dissociation energy is not enough for a direct breaking of H_2, still it might be beneficial for the cracking of H_2 which might occur at dangling bonds.

$$Si^* + H_2 = Si\text{-}H + H$$

The density of SiNx:H films also has an important impact on the diffusivity of H_2 through SiNx:H layers. A low density silicon nitride has more open channels for H_2 to diffuse through. If the density increases, these diffusion channels are getting narrower [17]. This can be observed from effusion of implanted Ar and Ne. Both noble gases are chemically inactive and approximately have the radius of respectively H and H_2. So they mimic the geometrical hindrance of these particles during diffusion through SiNx:H [17]. The effusion peak of Ne is moved to effusion temperatures of 800°C

Figure 11). It is possible that diffusion of H_2 is mediated by (temporary) dissociation, explaining the increase of the HD flux at temperatures above 800°C. This is still speculation and other possible explanations exist. More careful experiments are needed to reveal the true nature of hydrogen dissociation and the mechanism of bulk passivation.

Conclusions

Facts and experience on hydrogenation effects from SiNx:H have been presented at a workshop held within the Crystal Clear project. A general consensus is obtained that hydrogenation happens after thermal treatment of SiNx:H ARC coatings. This causes passivation of certain defects in the mc-Si bulk, such as decorated grain boundaries and dislocations. There is no evidence that a specific deposition mechanism is superior in terms of bulk passivation. The density of the silicon nitride increases the bulk passivation, until the hydrogen diffusion in the nitride becomes too low to be effective. But this aspect can be optimized towards an optimal bulk passivation. The origin of the density effect is not fully clear, because the amount of hydrogen involved in the release and passivation is small and only 0.1-1% of the total amount of hydrogen bonded in SiNx:H. Many experiments indicate that hydrogen originates from the SiNx:H layer itself, besides a possible implantation below the surface occurring during deposition. Hydrogen is released from the SiNx:H mainly in molecular form, but the amount for released hydrogen decreases with increasing density. It appears that a competing release mechanism, which provides atomic hydrogen, becomes more active with increasing nitride density. Determining the exact mechanism of hydrogen release and passivation requires more careful experimental work.

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Temperature dependent c-Si surface passivation properties of intrinsic PECVD a-Si:H films

Stefaan De Wolf and Michio Kondo
National Institute of Advanced Industrial Science and Technology (AIST), Central 2, 1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan

In this article we report on the temperature dependence of the surface passivation quality obtained by direct-plasma enhanced chemical vapor deposition (PECVD) at radio frequency (13.56MHz) of intrinsic hydrogenated amorphous silicon (a-Si:H) films deposited on low resistivity (~3Ω.cm) *p*-type float-zone silicon substrate surfaces. We argue that for stable films of the highest quality, the deposition-temperature should be kept well below the point where an epitaxial interface may be grown. The best passivation is obtained by subsequent annealing of the films, presumably leading to structural relaxation.

1. Introduction

Intrinsic amorphous silicon films have attracted in recent years considerable attention within crystalline silicon photovoltaics, mainly for their outstanding surface passivation properties. On device level, these layers have found applications either as passivation layer for the rear surface of the device,[1] or as buffer-layer for the fabrication of high quality heterostructure emitters and back surface fields.[2] Necessary conditions for high quality surface passivation by such films have been described in the past in terms of surface cleaning and soft film deposition. For hot-wire chemical vapor deposition, where no ion-bombardment takes place, it is known that the deposition temperature, T_{depo}, should be kept sufficiently low to avoid epitaxial growth.[3,4] In this article, we report that for direct PECVD, the value for T_{depo} is crucial too. The ideal passivation sequence appears to be film-deposition at a sufficiently low temperature to assure an abrupt interface, followed by an annealing treatment for film relaxation.

2. Experimental

To eliminate the influence of substrate surface roughness on the passivation properties,[5] bifacially mirror polished low resistivity (~3Ω.cm) *p*-type float zone FZ-Si(*p*) wafers have been used. Prior to deposition, the samples were cleaned in a (H_2SO_4:H_2O_2) (4:1) solution for 10min, followed by a rinse in de-ionized water. The chemically grown oxide was then stripped off in a dilute HF solution (5%) for 30sec, upon which the samples were immediately transferred to the deposition chamber. During deposition, a 20sccm SiH_4-flow was used and the pressure was kept at 0.5Torr. The electrode-distance and -diameter were respectively 20mm and 230mm, and the used power was 5W. Only T_{depo} was varied (from 105°C to 255°C). After deposition, the samples were annealed in a vacuum furnace for consecutive annealing cycles of each 30min, and ranging from 120°C to 260°C. For effective carrier lifetime, τ_{eff}, measurements, a WCT-100 quasi steady state photoconductance system from Sinton Consulting was used, operated in the so-called *generalized* mode. The thickness of the deposited films was measured by a J.A. Woollam Co., Inc. EC-400/M-2000S spectroscopic ellipsometer. Fourier transform infrared (FTIR) spectra were taken by a Perkin Elmer Spectrum 2000 FTIR spectrometer. For thermally stimulated desorption (TSD), an ESCO EMD-WA1000S system, coupled to a Balzers AG

QMG 421 quadrupole mass spectrometer to measure H_2-effusion from a-Si:H films, was used.

3. Results

Figure 1 shows the surface passivation quality for films deposited at 5W, which is the lowest power at which the plasma still could be maintained, as function of the deposition temperature, T_{depo}. This graph gives values for τ_{eff} measured after deposition, but also after an annealing sequence (260°C for 30min) and after 10 days of exposure to air. The influence of annealing in a vacuum furnace on the surface passivation quality of PECVD a-Si:H(*i*) films for different T_{depo} is given as well in an Arrhenius plot (figure 2). From the slopes of the exponential fits of this plot, an activation energy, E_a, can be extracted which may be interpreted as a potential barrier to a relaxed a-Si:H network of the deposited films. This is shown in figure 3, as function of the deposition temperature, T_{depo}. Figure 4 shows the deposition-rates at the initial deposition stages, calculated from (*ex situ*) spectroscopic ellipsometry data of thin films. For this, the measured data was fitted to a two-layer model (film roughness plus bulk of the film, see inset figure 4). Interestingly, from a given deposition temperature on (~205°C), no thickness can be measured, which suggests that from that temperature on (at least in the initial film growth stages) the films are crystalline. Finally, figure 5 shows the Si-H stretching modes of films deposited at different temperatures obtained from FTIR measurements (film thickness was about 850 nm), whereas figure 6 shows TSD data for similar films (film thickness was about 50 nm).

4. Discussion

A first important point to note from figure 1 is that in the case where a post-anneal is applied, the optimal surface passivation obtained by PECVD a-Si:H(*i*) films occurs at a remarkably lower value for T_{depo} than for the as-deposited case (~150°C vs. ~200°C). Moreover, the best passivation achievable in the post-annealing case is superior to that of the as-deposited case. The graph suggests that two different passivation mechanisms may be at work, a point which is as well suggested by the "activation energy" graph, as shown in figure 3. This graph is based on figure 2, where it can clearly be seen that for all

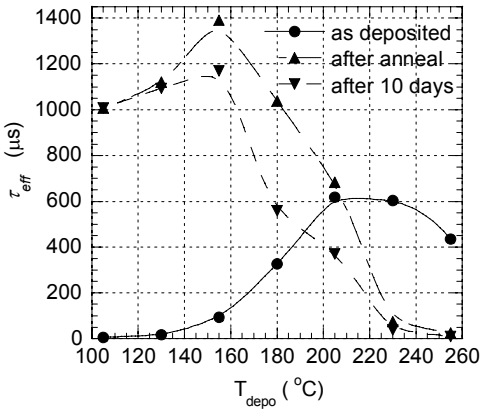

FIG. 1. Influence of T_{depo} of PECVD a-Si:H(*i*) films (P = 5W) on surface passivation quality on c-Si substrates. Results show films after deposition, after annealing sequence and after 10 days exposure to air.

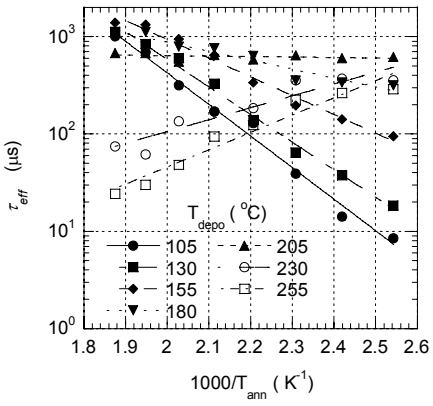

FIG. 2. Influence of T_{ann} on surface passivation quality for PECVD a-Si:H(*i*) films with different T_{depo}. Each sample underwent consecutive annealing-treatments. The lines are exponential fits.

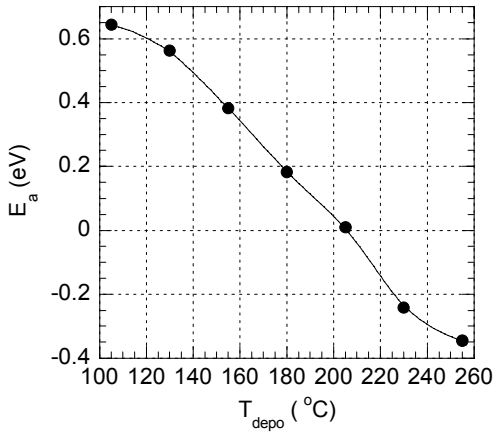

FIG. 3. "Activation" energy E_a as function of T_{depo} for the films shown fig. 2.

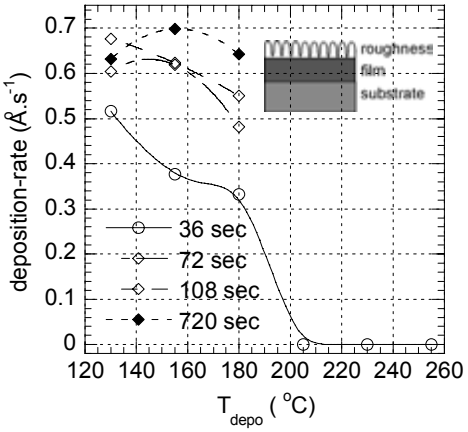

FIG. 4. Calculated deposition-rates from spectroscopic ellipsometry measurements as function of T_{depo} and for several deposition-times.

deposition conditions the passivation quality changes in a close to exponential way upon low temperature (120°C to 260°C) annealing. The lower the value for T_{depo}, the more pronounced the improvement is. For a given value of T_{depo} (in our case T_{depo}~205°C), which is where the value of E_a becomes zero, post-annealing does not seem to have any influence any more. For higher values of T_{depo}, post-annealing even has a detrimental effect on the passivation quality of the films.

The onset of epitaxial growth appears to coincide with the point where post-annealing results in losses in the passivation quality, or in terms of figure 3, where the value of E_a becomes negative. From this knowledge we can conclude that for as-deposited films, the best passivation quality is obtained for those films that are deposited on the edge of epitaxial interface formation. Note that it is believed that it is *only* the interface of the film that is crystalline. In case T_{depo} is much higher, the passivation quality goes down again, possibly due to a lack of hydrogen that is incorporated in these films. It is important to note as well that in any case the films deposited at epitaxial conditions do not seem to be stable over time. In this respect, FTIR measurements show that the high stretching mode

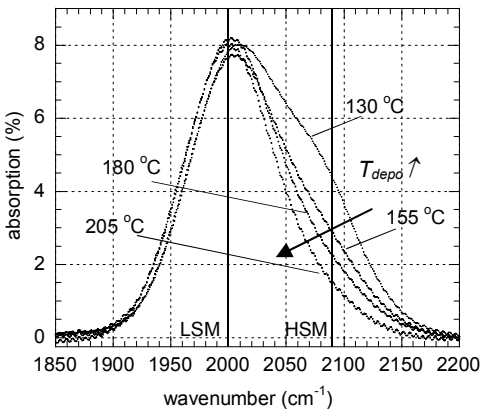

FIG. 5. Detail of FTIR spectra for films deposited at different T_{depo}. Shown as well are the positions of the Si-H low stretching mode (LSM) at 2000cm^{-1} and the Si-H high stretching mode (HSM) at 2090cm^{-1}.

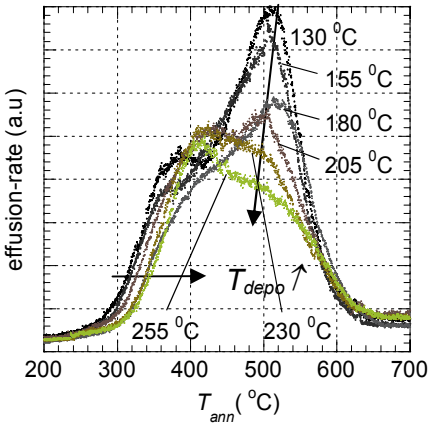

FIG. 6. TSD data for films deposited at different T_{depo}, showing the relative amount of H_2 escaping from the films during annealing under high vacuum. Heating rate was about 10.5 K.s^{-1}

(HSM) decreases for films deposited at higher temperatures. The HSM has been interpreted for hydrogen-rich films as a measure for the void density in the bulk whose surfaces are terminated by hydrogen.[6] The low stretching mode (LSM) is related to monohydride configurations in the bulk of the material.[7] Possibly, the presence of such voids may provide an effective path for oxidation of the interface. However, since in our case for the films where the degradation is the worst, the HSM signature is the least pronounced, it can be concluded that the encountered degradation is not likely to be related to oxidization but rather is due to the nature of the interface itself.

Regarding the films deposited below epitaxial conditions, it is remarkable that for all films values for τ_{eff} in excess of 1 ms can be measured after annealing, even for those films that initially gave no rise to any surface passivation at all. Apart from the fact that the interface is abrupt for these films, it is also important to note that their hydrogen content is higher than for those films deposited at higher temperatures. This can be seen both from FTIR (figure 5) and TSD data (figure 6). Moreover, most of the additional hydrogen in the low T_{depo} films appears to be present in the previously discussed HSM configuration, of which the Si-H bonds seem to be more stable than that of the LSM configuration (see TSD graph). In any case, the used annealing temperatures to obtain good surface passivation must be regarded to be too low to cause bond-ruptures. This is confirmed by performing both FTIR and TSD measurements on films that first received an annealing treatment of 260°C for 30min. No real differences could be observed compared to the data for as-deposited films (hence this data was omitted from the graphs). From this it must be concluded that most likely during the low-temperature anneal, a relaxation of the film is taking place, without any bond-rupture, but which may be sufficient to anneal out defects from the films.

5. Conclusion

In this paper we have shown that good stable passivation for c-Si by means of direct-PECVD a-Si:H(*i*) deposition has a very sharp processing boundary which is defined by epitaxial growth conditions. In case the interface is abrupt, the deposited films can benefit tremendously from a low temperature anneal, which is believed to yield in film relaxation. Moreover, we argue that, based on the activation-energy plot (see figure 3), lifetime measurements as function of annealing temperature may be a valuable low-cost tool to determine whether the c-Si / a-Si:H(*i*) interface is abrupt or not.

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Crystalline Silicon on Glass: Dialogue with a Sceptic

Author
Dr. Paul A. Basore
CTO, CSG Solar AG
for everyone at CSG Solar

Location
NREL Silicon Workshop
Denver, Colorado, USA

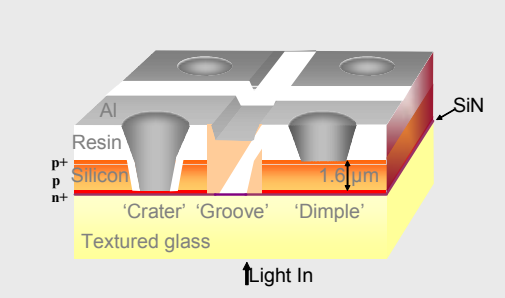
Language
Australian

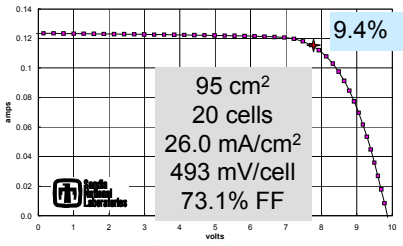
Date
6-9 August 2006

csgsolar
taking the next step

A One-Page Introduction to CSG

- Developed in Australia since 1995
  - PECVD, SPC, RTA, H (numerous patents)
- CSG Solar AG formed in June 2004
  - Factory constructed in Thalheim, Germany
  - 20 MW nominal annual capacity, 1.4-m^2 framed modules
  - Borosilicate Glass-Si-EVA-Tedlar (superstrate)
  - First functional modules produced: April 2006
  - Expected module efficiency: 7- 8% (100 watts)





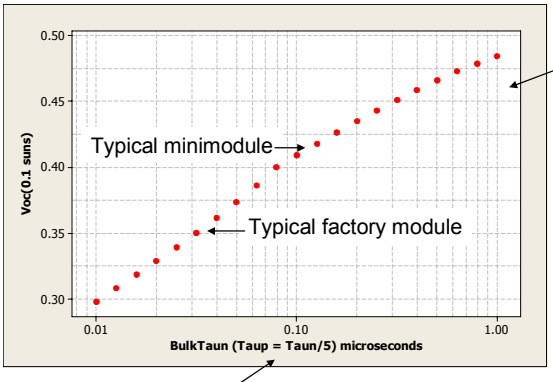
csgsolar

"People have been trying to put polycrystalline silicon on foreign substrates for 30 years. Nobody has succeeded in getting the efficiency over 10% on anything bigger than a thumbnail."

- CSG has demonstrated 9.4% over 95 cm^2 (independent validation), and recently 9.9% over this area (without an aperture mask). Produced 55 of these 'mimos' over 9%
  - The processes used to achieve these results are not radically different from what is used in production, though their economical application over large areas has not been established
- CSG differs fundamentally from all previous efforts
  - Avoids most contamination issues by not melting the silicon
  - n^+ and p^+ layers are grown-in rather than diffused
  - Light-trapping scheme that approaches the lambertian limit
  - Low-loss fault-tolerant contact scheme maximises active area

"CSG is almost at 10% efficiency despite our production focus." csgsolar

Voltage

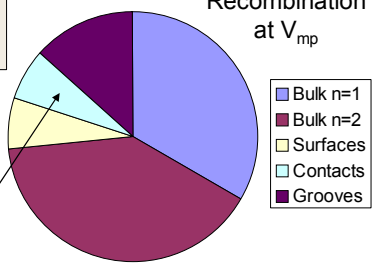


PC1D model with S_f=S_r=2E6 cm/s.

Surfaces play only a minor role in determining the voltage, which is dominated by bulk recombination.

In order to match PC1D modelling to both SunsV_{oc} and IQE, it has been found necessary to postulate that the hole lifetime is one-fifth the electron lifetime in the junction and base.

Recombination at V_{mp}



Contact and groove losses are from test cells. See paper from *31st IEEE PVSC*.

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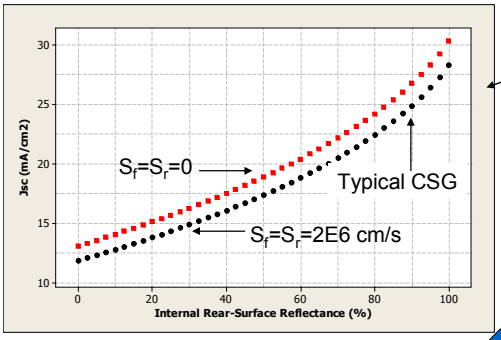
Photocurrent

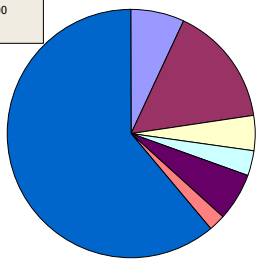


PC1D model with SiN ARC, 92% internal front-surface reflectance

Surfaces play an important role for recombination at short-circuit.

The inactive areas in a CSG module are the crater contacts (3%) and the cell separation grooves (1%). The dimple contacts (3%) and metal scribes (8%) are areas of reduced rear-surface reflectance but the junction in these areas is still active.

Photocurrent Components



- Front surface
- Escape reflectance
- Parasitic absorption
- Bulk recombination
- Surface recombination
- Inactive area
- Collected

Total = 41 mA/cm²

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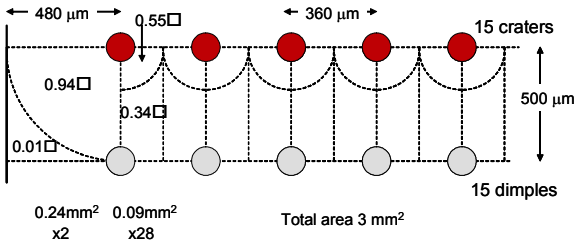
Series Resistance



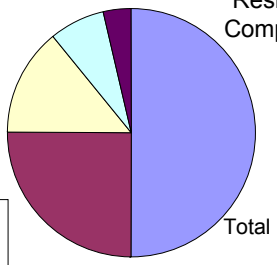
A partitioned evaluation of the sheet resistance shows that dot contacts increase R_s by 25% compared to a one-dimensional flow (0.035 □ vs 0.028 □).

$$Squares(quarter\ circle, photogeneration) = \frac{2}{\pi}\left[\ln\frac{b}{a} - \frac{I_{int}I_{ext}}{I_{tot}^2}\left(1-\frac{a^2}{b^2}\right) - \frac{I_{int}^2}{I_{tot}^2}\left(\frac{3}{4}-\frac{a^2}{b^2}+\frac{1}{4}\frac{a^4}{b^4}\right)\right]$$

$$Squares(linear, photogeneration) = \frac{1}{3}\frac{L}{W}\left(\frac{I_{int}^2}{I_{tot}^2}\right)$$

$$Squares = \frac{(28)0.89(0.09mm^2)^2 + (2)0.95(0.24mm^2)^2}{(3.00mm^2)^2} = 0.035$$

Series Resistance Components



- p+ layer
- n+ layer
- Contacts
- Metal
- Tabs

Total = 2.5 Ωcm²

R_s is dominated by the lateral sheet resistance plus some current crowding at the contacts.

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"The high costs of module assembly and balance of system clearly favour more efficient PV technologies for power generation."

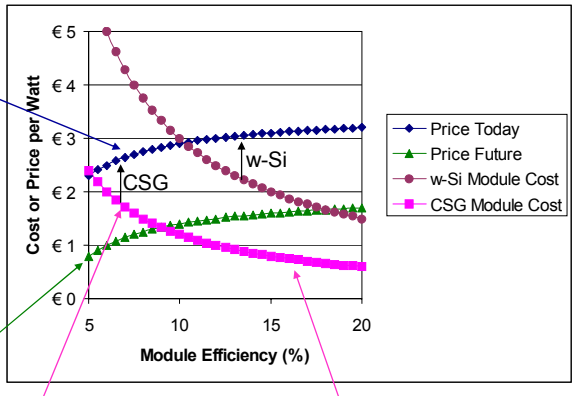
- The module assembly cost for CSG-2 is €40/m^2
  - Frame with two support bars sufficient for snow loads
  - Junction box with industry-standard quick-connect leads
- The sales price as a function of efficiency is known
  - Multi-megawatt contracts signed with two experienced customers
- Neither is an impediment to profitability of CSG at present
  - Despite the use of relatively expensive borosilicate glass
  - Despite the high cost of deposition equipment
  - Despite the relatively low efficiency expected in production
- As market prices decline, CSG looks even better
  - The high-efficiency benefit of putting more watts in a limited space does not apply if that technology cannot sell at the market €/W

"CSG technology aims to minimise the cost per delivered kWh." csgsolar

Impact of Efficiency on Sales Margin

The current market price for PV in Germany as a function of efficiency. It implies an area-related BOS cost for large field installations of €60/m^2.

In future, if all area-related costs (module and BOS) stay the same, higher efficiency is needed by all technologies to meet the lower market price.



As a new technology, CSG must sell below the market price, but today at 7% it is still as profitable as w-Si. In future, it needs to be at least 10%.

CSG-2 manufacturing cost of €120/m^2 including depreciation. Cost in future factories expected to decrease as their size increases.

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"Thin films of all types have a poor record for field reliability despite claims to the contrary."

- Harsh combined-cycle testing (sequential Temp Cycle + Humid Freeze + Damp Heat) shows CSG to be as durable as wafer silicon and more durable than other thin films
  - CSG can even survive this combined cycle test without lamination!
- CSG provides lateral conductance in the crystalline silicon
  - No transparent conducting oxides are needed
  - The conductor polarities are separated everywhere by >40 μm
- CSG tabs are ultrasonically soldered directly to aluminium-coated glass
  - No conductive paste
  - Lead-free

"CSG is a thin version of crystalline silicon, not a crystalline-silicon version of thin film."

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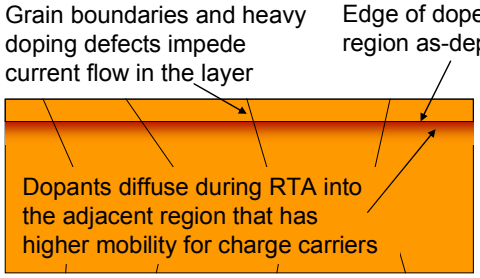
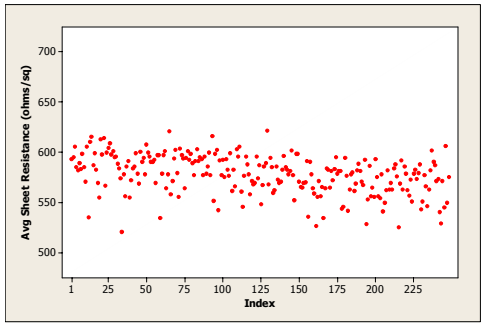
Lateral Conductance in Polycrystalline Silicon



A typical n-layer dose is 4×10^{14} cm^{-2}, giving a sheet rho of ~700 Ω/sq after RTA. Compare to sc-Si at 250 Ω/sq.

A typical p-layer dose is 1.5×10^{14} cm^{-2}, giving a sheet rho of ~1400 Ω/sq after RTA. Compare to sc-Si at 650 Ω/sq.



The average sheet resistance for each of 250 consecutive factory panels measured using inductance shows that the parallel conductance of the n and p layers in CSG material is consistent to within ±10% (3σ).

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"As a relatively small private enterprise, with a technology largely ignored by government research programs, CSG Solar does not have the resources to keep up with improvements in wafer silicon or even microcrystalline silicon."

- CSG Solar's shareholders understand the importance of R&D to the value of the Company now and in the future
  - Commitment to continue the €2M/yr pilot-line effort in Sydney
  - Another €2M/yr in funds from factory cash-flow for additional R&D
- CSG Solar will utilise expertise and equipment of others
  - Sponsored research relating to key topics of interest
    - Up to 8 research teams (~€250k/yr each placed over next 12 months)
    - We require a no-cost non-exclusive licence to developed IP
  - Collaborative research to expand awareness of CSG technology
    - We supply material in return for acknowledgement and access to data

"We have a well-funded and innovative approach to R&D."

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Key Research Topics of Interest to CSG Solar

- What is the dominant recombination mechanism in CSG?
  - Crystal defects, grain boundaries, impurities, clusters, stress
- How can we make hydrogen passivation more effective?
  - Influence of thin surface layers, water vapour, temperature
  - Role of fluorine (from chamber cleaning), boron (p^+ doping)
  - Loss of passivation due to laser heating (metal patterning)
- Can we use soda-lime glass with our contacting scheme?
  - Heat Si not glass, bubble formation, lateral conductance, cracking
- How can we deposit suitably doped silicon with lower cost?
  - Dep rate and uniformity, chamber cleaning, ammonia-free nitride
  - Equipment availability for rapid expansion using large glass sheets
- How can we improve ink-jet printing of caustic inks?
  - Ink-jet heads, ink chemistry, xy stages

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High-quality Si multicrystals with same grain orientation and large grain sizes controlled by the new dendritic casting method

Kazuo Nakajima, Kozo Fujiwara, Wugen Pan, Masatoshi Tokairin,
Yoshitaro Nose, and Noritaka Usami

Institute for Materials Research, Tohoku University
Katahira 2-1-1, Aoba-ku, Sendai 980-8577, Japan

We propose the "dendritic casting method" as a novel crystal growth technique to realize multicrystallie Si (mc-Si) ingot with controlled grain orientation and large grain sizes for solar cell applications. The method consists of the dendrite growth along the bottom of the crucible at the initial stage and the subsequent directional growth on top of the dendrite crystals. By using this method, {110} or {112} oriented mc-Si ingot with a diameter of 15cm and large grain sizes (≥3cm) can be obtained. Furthermore, superior solar cell performance was confirmed compared with solar cells based on conventional mc-Si.

Introduction

In the present photovoltaic (PV) industry, bulk crystalline Si including multicrystalline Si (mc-Si) and single crystalline Si (sc-Si) is the most dominant material for PV modules. Especially, the raise in the share of mc-Si driven by the advantage in terms of the low production cost stimulates the demand for improvement in the conversion efficiency of the solar cells based on mc-Si.

An approach to satisfy this demand is to somehow control the structural elements in mc-Si such as grain orientations, grain sizes, grain boundary characters and so on. The standard anisotropic chemical etching for surface texturing could be applied to mc-Si with perfectly aligned grain orientations for improved light trapping, leading to the increase in the photocurrent. The undesirable carrier recombination at grain boundaries could be avoided by realization of mc-Si with electrically inactive grain boundaries and/or decreasing grain boundary density. Furthermore, additional improvement in crystal quality as well as mechanical stability could be realized by appropriate control of structural parameters in mc-Si. To realize such a high-quality mc-Si ingot, we need to establish a novel crystal growth technique based on deep understanding of the crystal growth mechanisms.

In this paper, we report on our fundamental research to investigate the melt growth processes of Si to explore mechanisms for controlling structural elements in mc-Si. Furthermore, an attempt was made to implement the knowledge obtained by the fundamental research to practical growth method, which lead to the proposal of the "dendritic casting method" to obtain high-quality mc-Si ingot with controlled grain orientation and grain sizes. A preliminary result on the solar cell performance is also reported to demonstrate that the dedritic casting method is very promising for growing mc-Si ingot for solar cell applications.

Experiments and Results

To explore the growth mechanism to control the grain orientation and the grain size, we newly developed an in-situ observation system as shown in Fig. 1 to directly observe the growing interface at higher temperature than 1400°C [1,2]. A Si growth melt was placed in the silica crucible, and they were set inside the small furnace with a temperature gradient to drive the directional growth. The growing interface can be directly observed through a silica window by the microscope.

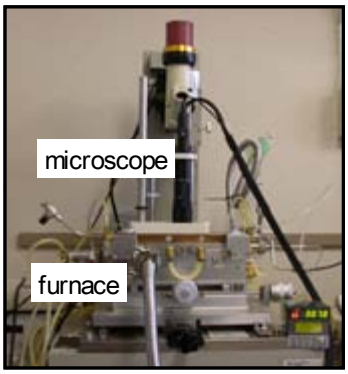

Fig. 1 In-situ observation system used in this study

Figure 2 is the arrangement of the growth melt. The Si growth melt directly contacts with the crucible. Figure 3 shows a microscopic image of the Si dendrite growth under proper growth conditions. In addition, we found that a Si dendrite crystal grew along the bottom of the crucible at the initial stage of the growth followed by the directional growth on the upper surface of the dendrite crystal by in-situ observation [3] and ex-situ analysis of the grown ingot [4].

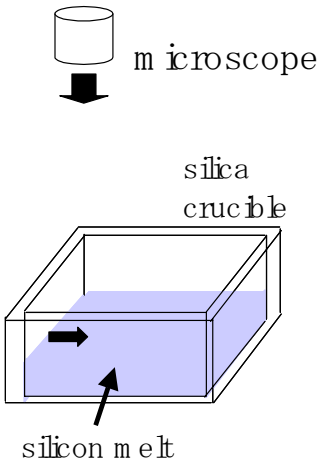

Fig.2 Arrangement of the growth melt.

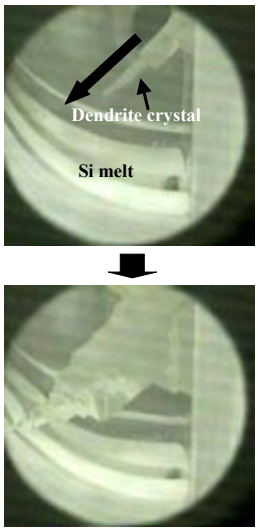

Fig.3 Microscope image of the dendrite growth

The orientation of dendrite crystals depends on the amount of the supercooling of the Si growth melt as shown in Fig. 4. When the supercooling is between 5 and 50 °C, the preferential orientation of dendrite crystals is <112> or <110> [5]. The dendrite crystals have two twins with Σ3 grain boundaries, and the Σ3 grain boundaries have the same {111} facets. Therefore, the upper surface of the dendrite crystals can be controlled as {110} or {112} by the amount of the supercooling.

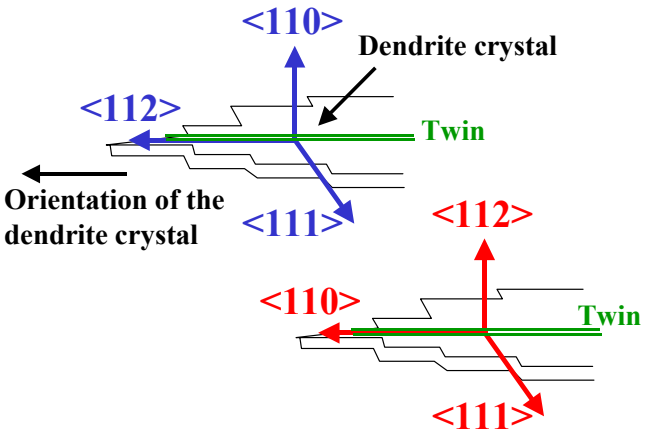

Fig. 4 Orientation of dendrite crystals

Figure 5 shows how we attempted to apply the knowledge obtained by the fundamental research to the practial growth method to obtain mc-Si ingot with controlled grain orientation and grain sizes. At first, dendrite crystals with the <110> or <112> direction are grown along the bottom of the crucible under appropriate growth conditions.

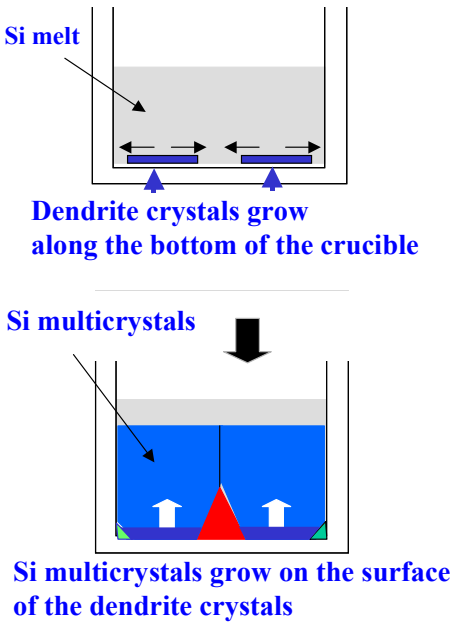

Fig. 5 Growth concept to control the grain orientation and the grain size.

Subsequently, the growth conditions are switched to cause directional growth on the upper surface of the dendrite crystals. Figure 6 shows the cross sections of the bottom and center of a Si multicrystal grown by the dendritic casting method. It is seen that a dendrite crystal with a {112} upper surface appears along the bottom of the crucible. Importantly, the Si multicrystal grows on the {112} upper surface of the dendrite crystal, which results in the {112}-oriented grains during growth. As the growth proceeds, the grain size becomes larger. Consequently, the dendritic casting method permits to obtain high-quality mc-Si ingots with a diameter of 15 cm on the {110} or {112} oriented dendrite crystals.

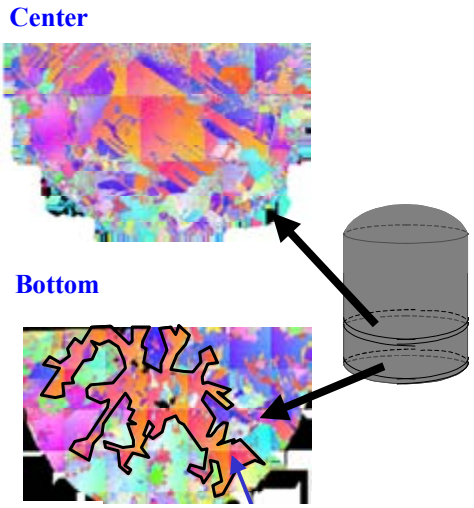

Fig. 6 Orientation distributions in cross-sections of the bottom and center of a Si multicrystal grown by the dendritic casting method

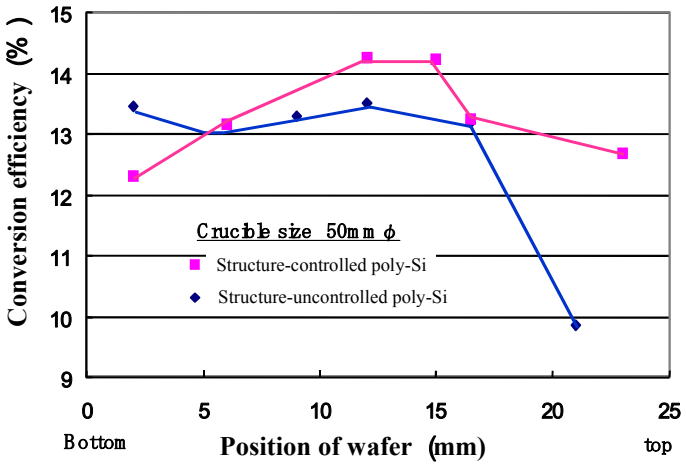

Fig. 7 Comparison of the conversion efficiency of solar cells based on mc-Si grown by the dendritic casting method and the conventional one.

The grown crystals were cut perpendicular to the growth direction, and a part of samples were processed to 1.5 cm x 1.5 cm solar cells. Detailed processes were described

elsewhere [6]. Figure 7 compares the conversion efficiency of solar cells based on mc-Si grown by the dendritic casting method and the conventional casting method. Obviously, the solar cells based on mc-Si grown by the dendritic casting method showed superior performance except the bottom part of the ingot. Especially, the solar cells processed from the top part of the crystal showed less degradation, which is of practical importance.

Figure 8 shows the conversion efficiency of solar cells based on mc-Si ingot grown by the dendritic casting method. It is noted that the diameter of the crucibles was systematically changed for 50 mm, 80 mm, and 150 mm. The outlook of the ingot with a diameter of 150 mm was shown in Fig.9. The grain size is quite large and amounts to larger than 3 cm. With increasing diameter of the crucible, the conversion efficiency was found to increase. Although the conversion efficiency was not independently confirmed, the obtained effeiciency of 17% without surface texturing and hydrogen passivation is close to our standard level based on sc-Si, which shows that high-quailty mc-Si ingot was successfully obtained by the dendritic casting method.

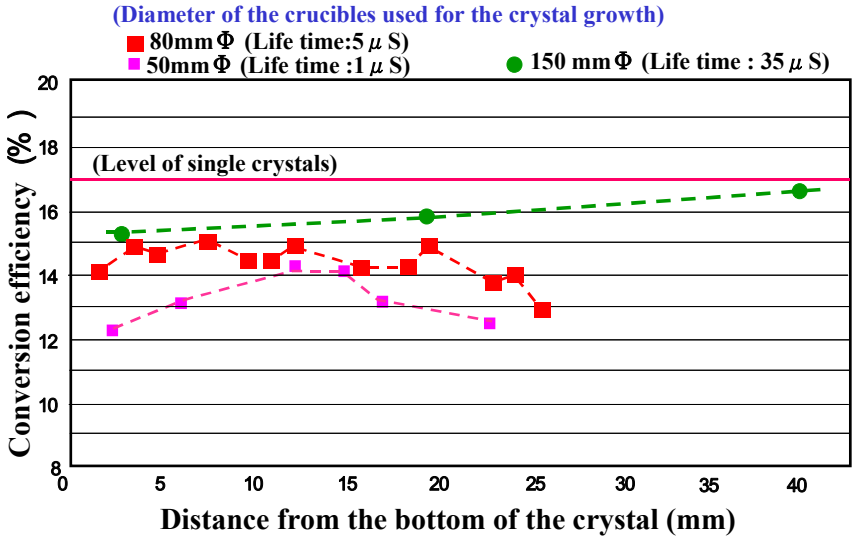

Fig. 8 Conversion efficiency of solar cells based on mc-Si grown by the dendritic casting method.

Fig. 9 Mc-Si ingot with a diameter of 15 cm grown by the dendritic casting method

Conclusions

The dendrite growth along the bottom of the crucible, which was found during in situ observation of Si melt growth, was implemented to a new growth technique to realize high-quailty mc-Si ingot with the same growth orientation and large grain sizes. The dendritic casting method permits to control the growth direction to {110} or {112} depending on the amount of the supercooling without any seed crystals. In fact, we successfully obtained extremely high-quality mc-Si ingot with the same grain orientation, very large grain sizes (≥3cm), and the longer lifetime more than 35 μs without hydrogen passivation. The conversion efficiency of the solar cells prepared by the mc-Si grown by the dendritic casting method was found to be improved compared with those based on conventional mc-Si. Furthermore, the conversion efficiency reached our standard level of sc-Si, which demonstrates that the mc-Si ingot is of extremely high quality.

Acknowledgments

This work was supported by NEDO of Japan, and a Grant-in-Aid for Scientific Research from the Ministry of Education, Culture, Sports, Science and Technology.

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Electrical Characteristics of an n-type crystalline Si/ i-n-type amorphous Si:H structure

Yutaka Hayashi[1),2)] and Tohru Nakamura[1)]

1) Nanotechnology Research Institute, National Institute of AIST (Advanced Industrial Science and Technology), Central 2, 1-1-1 Umezono, Tsukuba, 305-8568, JAPAN

2) Institute of Materials Science, University of Tsukuba, 1-1-1 Tennoudai, Tsukuba, 305-8573, JAPAN

[Abstract] The current–voltage (IV) characteristics of an n-type crystalline silicon/ non-doped/n-type hydrogenated amorphous silicon (abbreviated as "n-cSi/i-n-aSi:H" hereafter) hetero-junction was investigated. Electrical measurements were done on the back-side hetero-junction of HIT solar cells [1], [2], which consists of n-cSi/i-n-aSi:H. As the HIT cell has also a front side hetero-junction, the electrical potential of a probe on the n-cSi was monitored to extract the IV characteristics of the n-cSi/i-n-aSi:H hetero-junction, while the IV characteristics of the cell are measured between it's front electrodes and back electrodes. In addition, change in the Fermi energy of the n-cSi near the crystalline/amorphous interface was measured by a scanning Kelvin force microscope (KFM). As a result, the n-cSi/i-n-aSi:H junction was proved to operate not as a junction generating a photo-voltage but as an ohmic interconnection between the photovoltaic part of the solar cell and the back electrodes of the cell. Electron accumulation in n-cSi near the back side hetero-junction was confirmed by the KFM measurement.

[Introduction] Out of crystalline silicon solar cells, a hetero-junction solar cell with hydrogenated amorphous silicon (aSi:H)/crystalline silicon (cSi) hetero-junction like the HIT solar cell[1] has shown leading high efficiency in volume production. A metal back electrode contacted on the n-type cSi was used as the back ohmic contact for early HIT solar cells[2] with a front p-type-i-type aSi:H/n type cSi (p-i-aSi:H/n-cSi) hetero-junction but addition of aSi:H to the back surface of the cell to make n-cSi/n-aSi:H hetero-junction revealed further enhancement in the conversion efficiency[3]. However, it has not been clearly shown whether this back side cSi/aSi:H hetero-junction is a photo-voltage generating junction or has a role of passivated ohmic interconnection from cSi to the back electrode of TCO/metal. This paper intends to reveal the role of the back side hetero-junction by extracting the IV characteristics of it while the cell is operating under DC voltages and by observing the Fermi energy change in cSi near the back side hetero-junction.

[Experiments] To extract the electrical characteristics of the back side hetero-junction, the electrical potential at n-cSi near to the back side junction was monitored while IV characteristics between the front and back electrodes were measured.

This approach was adopted to extract the characteristics of both front ant back side hetero-junctions without separating the two junctions. The separation of two junctions by slicing the n-cSi in between the two junctions will result different carrier conduction from that of an actual solar cell

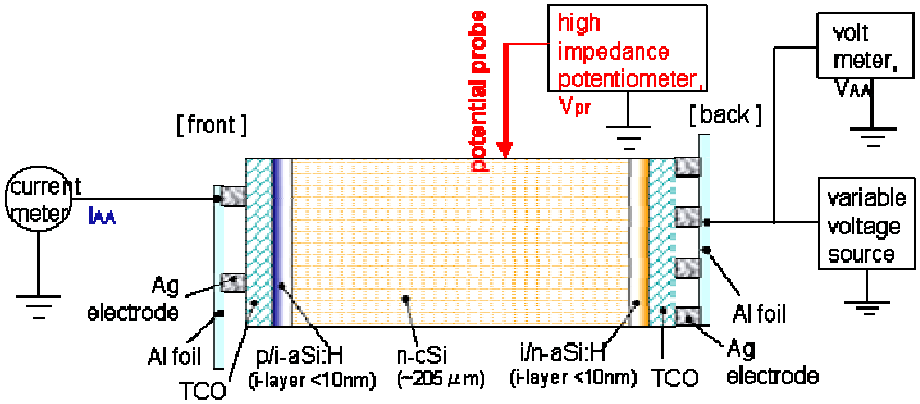


Fig.1 Schematic diagram of the measurement set up and the cross section of the sample (not to the scale)

operation. A schematic measurement set up is shown in Fig.1.

Sheets of aluminum foils are attached by silver paste to silver striped front electrodes and sliver striped back electrodes to realize low contact resistance at the electrodes and to realize uniform current distribution across the cell surface. Reproducible IV measurement was also realized due to the pasted Al foils. Solar cell samples were taken out from a HIT module HIP2717 and broken into several~few mm x few mm in the planar dimension when the tempered cover glass was diced. Fig. 2 shows a typical sample with Al foils for the measurement.

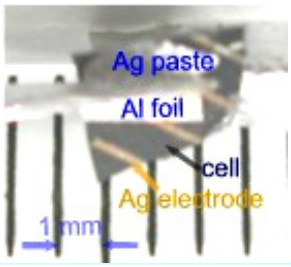


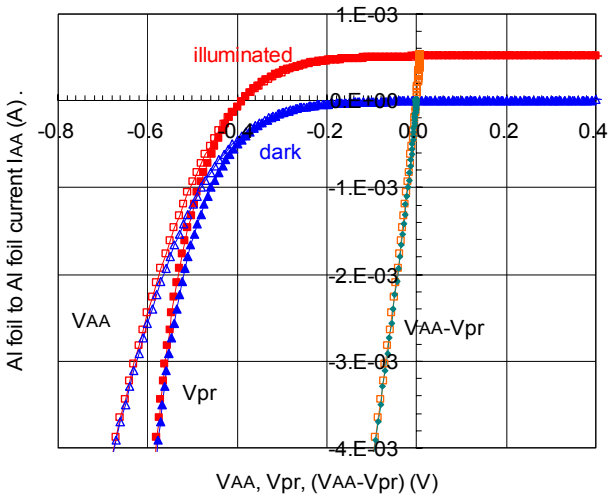
Fig. 2 A sample with Al foils

The cross-section of the sample is schematically shown in Fig.1. The front (light receiving) part of the cell consists of silver stripe electrodes/ TCO/ p-aSi:H/ i-aSi:H/ n-cSi and the back part of the cell consists of n-cSi/ i-aSi:H/ n-aSi:H/ TCO/ silver stripe electrodes.

For the IV and n-cSi potential measurement, the Agilent Technology semiconductor parameter analyzer 4156C and a multi-probe system were used. For light illumination to generate in the sample photo current of around 0.5 sun equivalent, a small halogen lamp JDR110V75W-FL/K5E (color temperature: 3000K) was used.

To measure change in Fermi energy of n-cSi near the back hetero-junction, thin Al sheets were attached on both surfaces of a sample by epoxy adhesive and the sample sandwiched with the Al sheets were angle lapped to 5 degree from the surface to obtain a smooth transition from the surface of the sample to Al sheet. The lapped surface was finished by Ar ion milling to reduce mechanical defects and roughness made by the mechanical lapping process. Prior to measurement by a scanning Kelvin force microscope, the sample surface was dipped in a dil-buffered HF and cleaned in a UV ozone cleaner. As the result, the sample surface was covered thin oxide. The thickness of the oxide measured on a reference n-type (100) silicon wafer was 1.7nm. For the KFM measurement, a scanning probe microscope Seiko Instruments Inc. SPA-300HV was used and the measurement was done in the dry nitrogen atmosphere to prevent the increase of Q factor for the KFM probe and also to avoid further absorption of water molecules on the sample surface. The front and back surface of the sample was electrically short-circuited by silver paste to avoid the Fermi level change by the stray light from the laser diode used in the equipment[4]. The sample was kept in a chamber of the equipment under high vacuum (ca. 10^{-8} - 10^{-7} torr) over 24h for the desorption of hydrocarbons and water molecules.

Fig. 3 IV characteristics, #6 dark and illiuminated



[Results] One of obtained results on IV and n-cSi potential measurements is shown in Fig. 3, where V_{AA} and I_{AA} denote the voltage and current between the front and back Al foils. A positive value of V_{AA} corresponds to a positive bias given to the back Ag electrodes and that of I_{AA} corresponds to current flowing into n-cSi from the back Ag electrodes, because the front Al foil is connected to a common potential through the electric current meter. This bias

arrangement was adopted to show clearly that the n-cSi potential V_{pr} follows the back electrode voltage and input impedance of the equipment for the potential measurement is high enough to obtain accurate information on the n-cSi potential.

I_{AA} vs. V_{pr} characteristics shows IV characteristics of the front part of the cell and I_{AA} vs. (V_{AA}-V_{pr}) shows IV characteristics of the back hetero-junction and lateral resistance of n-cSi and TCO. Effect of the vertical (thickness direction) resistance of n-cSi is negligibly smaller than that of the lateral one. Thus, as shown in Fig.3, the IV characteristics (I_{AA} vs. V_{AA}) of the total cell reflects mainly that of the front part and the IV characteristics of the back hetero-junction are of low resistance and almost linear. To show detailed resistance value, Rbk = (V_{AA}-V_{pr})/ I_{AA} is also plotted in Fig. 4. The back side resistance stays within the range of 17~23 ohm For the forward current of 0~3.4 mA.

Fig.4 IV characteristics and Rbk, #6 dark and illuminated

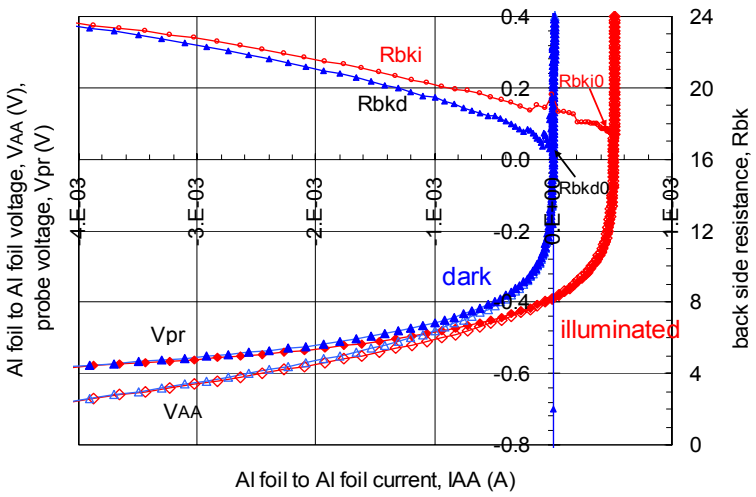


Fig. 5 shows a distribution of KFM signal taken at the back side part of the sample along n-cSi to aSi:H. The KFM signal is closely related to the Fermi energy of the sample with reference to the vacuum level. The measured KFM signal stays relatively constant above n-cSi apart from the back side hetero-junction. However, it increases when the probe approaches to the interface with the back side aSi:H. It means that the difference between the Fermi level and the conduction band of n-cSi becomes smaller near the interface. In another word, electrons accumulate in n-cSi near the back side interface.

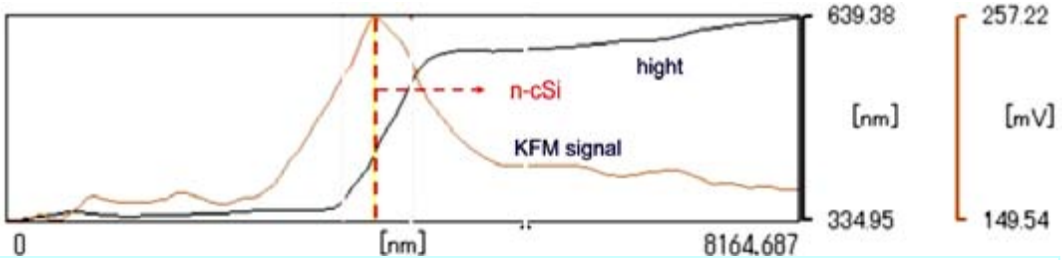


Fig.5 KFM signal obtained around back side part of the cell. A signal from aSi:H will not be obtained because the thickness of the aSi:H is too small (<10nm) compared with the resolution of the equipment

[Discussion] There still exist lateral current flows along TCO and n-cSi to the back Ag electrodes at the back side part of the cell even if the Al foil was attached to the electrodes and (partly) to TCO and this may result current crowding effect. The back side resistance estimated at nearly zero forward current may show the value less suffered from the current crowding near back Ag electrodes. 17 ohm in dark (Rbkd0 in Fig. 4) and 17.5 ohm under illumination (Rbki0 in Fig.4) still contain lateral resistance of n-cSi and TCO at the back side. The illuminated area of the sample was about 0.036 cm^2 and (junction resistance)*(unit area) under illumination will be less than 0.63 ohm-cm^2. Considering 1 sun photo-current density for a high efficiency

crystalline silicon solar cell (= 40 mA/cm^2), IR drop for the 1 sun photo-current density across the back side hetero-junction and the back Ag electrode is less than 25 mV which will be 3.6% of V_{OC} (0.7V) of a high efficiency cSi solar cell. The net IR drop at the hetero-junction only will be smaller than this value when the equivalent lateral resistances will be cleared.

To confirm whether the above KFM signal increase near the back surface is reasonable, the KFM measurement was tried above n-cSi near the front surface. The KFM signal decreases when the probe above n-cSi approaches to the front side hetero-junction. This suggests the surface depletion or inversion of n-cSi near the front side interface. This indication by the KFM signal is quite consistent with the photovoltaic generation at the front side part of the cell. This opposite change of the KFM signal between the part near the front side interface and the part near the back side interface insures the electron accumulation at the part near the back side junction. Details will be reported else where.

[Conclusion] It has been experimentally demonstrated that the back side hetero-junction ohmically interconnects n-cSi and the back TCO/Ag electrodes with small resistance and small nonlinearity. Since the small nonlinearity of the back side hetero-junction has been proved, we can use one of linear resistance network models to clear the lateral resistance effect of TCO and n-cSi in future.

The measured KFM signal indicated the accumulation of electrons at the back side part of n-cSi near the back side hetero-junction. This is one of evidences of the back surface field to prevent for minority carriers to reach and recombine at the back surface.

The above two results proves that the back side hetero-junction acts as a passivated ohmic interconnection between the n-cSi and TCO/Ag electrode.

[Acknowledgement] A part of this work was conducted in AIST Nano-Processing Facility (NPF), supported by "Nanotechnology Support Project (NPPP)" of the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan. Authors are indebted to Drs. H. Akinaga, N. Nakagiri, A. Ohi, M. Iitake, S. Kazama and Ms. S. Matsunaga for their guidance and support for using NPF/NPPP for a part of these experiments. They are also grateful to Dr. H. Yokoyama, Director of Nanotechnology Research Insitute of AIST for his encouragement and guidance.

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18.2% DOUBLE-HETEROJUNCTION SILICON SOLAR CELL WITH WELL PASSIVATED a-Si:H BACK CONTACT *

M.R. Page[1], E. Iwaniczko[1], Y. Xu[1], Q. Wang[1], Y. Yan[1], L. Roybal[1], T.H. Wang[2] and Howard M. Branz[1]

[1] National Renewable Energy Laboratory (NREL), 1617 Cole Blvd., Golden, CO 80401, USA
[2] Suntech Power Holdings Co., 17-6 Changjiang South Road, New District, Wuxi, Jiangsu Province 214028, People's Republic of China

ABSTRACT

We have developed hydrogenated amorphous silicon (a-Si:H) back contacts to p-type silicon wafers, and employed them in double-heterojunction solar cells. These contacts are deposited entirely at low temperature (<250°C) and replace the standard diffused or alloyed back-surface-field contacts used in single-heterojunction (front-emitter only) cells. High-quality back contacts require excellent surface passivation, indicated by a low surface recombination velocity of minority-carriers (S) or a high open-circuit voltage (V_{oc}). The back contact must also provide good conduction for majority carriers to the external circuit, as indicated by a high light I-V fill factor. We use hot-wire chemical vapor deposition (HWCVD) to grow a-Si:H layers for both the front emitters and back contacts. Our improved a-Si:H back contacts contribute to our recent achievement of a confirmed 18.2% efficiency in double-heterojunction silicon solar cells on p-type textured silicon wafers [1].

INTRODUCTION

When applied to the full area of a crystalline silicon (c-Si) wafer, thin hydrogenated amorphous silicon (a-Si:H) layers have an excellent passivation capability and enable good carrier transport. These layers can serve as both the front emitter and back-surface-field (BSF) contact. The unique combination of passivation and current conduction of a-Si:H on c-Si offers many possibilities for high-efficiency device structures processed at temperatures below 250°C. Optimization of the i/n a-Si:H front emitter allowed us to achieve 17.1%-efficient single-heterojunction solar cells on p-type silicon wafers with a screen-printed Al-BSF [1]. However, an Al-BSF introduces a back-surface-recombination velocity on the order of 10^3 cm/s which limits further improvements in device performance. The Al-BSF leads to a high back-surface dark saturation current component that limits the open-circuit voltage. Further, an Al-BSF has to be processed at temperatures above 800°C, and this may cause severe bowing of the thin (~200 μm) wafers now being introduced. Such bowing contributes to problems in wafer-handling and module assembly in manufacturing.

Here, we report on the development of deposited a-Si:H back contacts for textured p-type silicon wafers. Any dark-current path through inadequately passivated interface states reduces both the V_{oc} and the collection of photogenerated charge carriers. Therefore, high V_{oc} is the key to high-performance solar cells: V_{oc} and S indicate the effectiveness of an a-Si:H/c-Si heterointerface. We first demonstrated excellent surface passivation using HWCVD a-Si:H thin layers at the back-surface to achieve a very low S of 15 cm/s. This advance enabled us to obtain a V_{oc} of 667 mV on textured p-type silicon wafers in a double-heterojunction structure with a front n/i a-Si:H emitter and back i/p a-Si:H contact. In comparison, an Al-BSF on a p-type silicon wafer yielded far lower V_{oc} of 636 mV. With a pure a-Si:H full-area back contact to a p-type wafer, we obtain a good fill factor of 77%, indicating excellent hole conduction across the back c-Si(p)/a-Si:H(i/p) interface.

*This work has been authored by an employee or employees of the Midwest Research Institute under Contract No. DE-AC36-99GO10337 with the U.S. Department of Energy.

EXPERIMENTAL

We use commercially available (100) float-zone (FZ) c-Si wafers for our silicon heterojunction (SHJ) device development and optimization because they have the highest bulk carrier lifetimes. The absence of significant boron-oxygen pair metastability in the FZ p-type B-doped wafers is also significant. We use HWCVD, rather than plasma-enhanced CVD, to grow the a-Si:H layers for both the front emitters and back contacts, because there is no possibility of plasma damage deleterious to the high-quality c-Si wafers we use. For all devices, including single- and double-sided planar SHJ and those on wafers textured in-house or by collaborators, we employed identical cleaning procedures, discussed in detail below.

For SHJ devices, the junctions are formed at the a-Si:H/c-Si interfaces, so it is critical to have a clean interface just prior to a-Si:H deposition. The goal is to avoid introducing defects and impurities at the interface that would cause junction recombination and hurt surface passivation. We employ a cleaning procedure that begins with a degreasing step using commonly available laboratory chemicals, with ultrasonic agitation for particle removal. Thorough rinsing and stripping of organic residues is essential, so we use modified RCA cleaning steps for final organic and metallic contaminant removal. We have found that the chemically grown oxide works well as a capping layer for the sensitive c-Si interfaces. The stable cap is stripped using a 2.5% hydrofluoric acid flush immediately before loading in our HWCVD vacuum deposition system with a base pressure slightly above 10^{-8} torr.

Double-sided texturing of c-Si substrates to reduce reflection losses using standard alkaline texturing solutions and practices yields pyramidal features on the order of 5 μm. The sharp tips of the pyramid peaks and deep valleys at the pyramid bases present challenges during deposition of thin a-Si:H layers. Our HWCVD layers provide excellent conformal coverage of a textured substrate with very little evidence of shunting at the tips. Cleanliness and surface passivation are all the more important on the increased surface area of the textured surface. Because of the excellent surface passivation of a-Si:H, one can use bifacially textured c-Si and reflective backing for improved light trapping in thin silicon wafers.

Our HWCVD deposition systems are capable of i-, n-, and p-layer deposition in separate chambers, but only with an air break between i- and n-layer depositions. Our optimized a-Si:H layer deposition conditions are summarized in Table 1.

Table 1. Summary of optimized a-Si:H deposition conditions for SHJ solar cell devices.

LAYER	THICKNESS (nm)	T (°C)	DEPOSITION RATE (Å/s)	GAS
i	~ 5	<150	3 - 12	SiH_4
n	~ 5	~200	~ 3	PH_3 SiH_4 H_2
p	5 - 6	~200	3	B_2H_6 SiH_4 H_2

Thermally evaporated indium tin oxide (ITO), deposited at below 200°C, with a thickness of 60-80 nm, is used for the transparent top contact to a-Si:H emitter and as the single-layer antireflection coating. Our full-area back contact and the shadow-mask-defined front contacts are deposited using electron-beam evaporation of Al or Ti/Pd/Ag metal stacks at room temperature. We have used a number of isolation techniques to form the 1-cm^2 solar cell area including photolithography, a dicing saw, and physically masked argon ion milling.

An important diagnostic used in our solar cell device development process is the measurement of effective minority-carrier lifetime using a Sinton lifetime tester. Lifetime is a sensitive measure that probes both the bulk lifetime and surface passivation of a c-Si wafer. We measure the interface quality of our devices prior to ITO contact deposition so we can avoid wasting effort and materials applying

ITO to bad devices. With high bulk-lifetime FZ-Si wafers, we can estimate surface recombination velocities and the implied device V_{oc}. For rapid feedback on device quality, we also measure the V_{oc} of 0.05-cm^2 ITO dots at the edges of the full device region, as defined by shadow-masked ITO deposition. High-resolution transmission electron microscopy (HRTEM) was helpful for optimizing the SHJ interface; we used it to determine whether the initial HWCVD-deposited layers were a-Si:H, microcrystalline silicon (μc-Si:H), or epitaxial c-Si. HRTEM micrographs were made in the ITO dot region and correlated to I-V measurements on fully isolated 1-cm^2 solar cell devices measured on an AM1.5 calibrated XT-10 solar simulator.

RESULTS AND DISCUSSIONS

a-Si:H for better passivation instead of c- or μc-Si:H

We optimized thin HWCVD a-Si:H surface passivation layers to achieve a low S of 15 cm/s. It is critical to avoid formation of epitaxial c-Si or μc-Si:H. This is achieved by limiting the initial undoped a-Si:H layer deposition temperature to 150°C or less. As seen in Fig. 1, the effective minority-carrier lifetime rises and the surface recombination velocity falls as the deposition temperature is reduced from 230° to 100°C. We have shown earlier [2] that for deposition temperatures above 150°C for (100) wafers or 200°C for (111) wafers, epitaxy can occur and this reduces V_{oc}. On a textured p-type wafer having an Al-BSF back contact and an a-Si:H emitter, we attain a respectable maximum V_{oc} value of 636 mV.

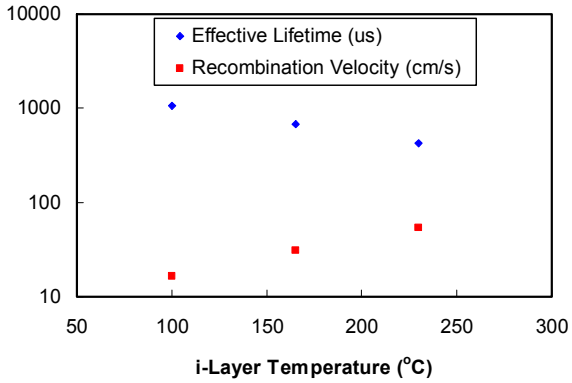

Fig. 1. The i-layer deposition temperature effect on passivation.

a-Si:H back contacts instead of Al-BSF

We obtained a high V_{oc} of 667 mV on textured p-type FZ c-Si wafers in the double-heterojunction structure (front n/i SHJ emitter and back i/p SHJ contact). This result indicates that both back- and front-surface passivation are excellent (see Fig. 2). For comparison, replacing the SHJ back contact on a p-type c-Si wafer with an Al-BSF yields a V_{oc} of only 636 mV, as shown in Fig 2. Although traditional alloyed BSF contacts have excellent contact-resistance characteristics, a-Si:H back contacts are superior for their combined passivation and current-transport capabilities.

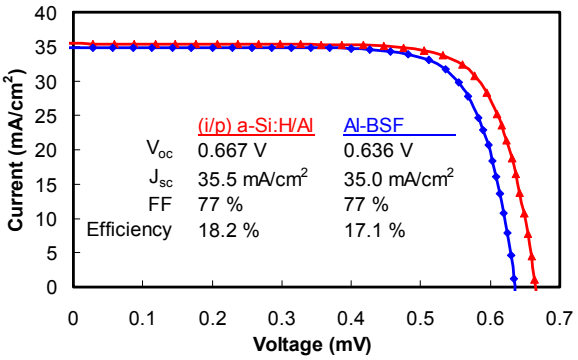

Fig. 2. Good fill factors on front heterojunction textured p-type FZ c-Si solar cells with screen-printed Al-BSF (◆) and SHJ back contact (▲).

Fill factor (FF) is another important measure of back-contact performance. When using dielectric back-surface passivation with insulating materials, one must employ local contact windows [3] to obtain low resistance and effective majority-carrier collection. Conversely, with simpler full-area back contacts of a-Si:H, it is possible to obtain excellent hole conduction across the back c-Si(p)/a-Si:H(i/p) interface; we obtain a good fill factor of 77% (Fig. 2). Our SHJ back contact compares very favorably to the state-of-the-art screen-printed Al-BSF with its maximum fill factor of 77%. On n-type wafers, Sanyo's excellent HIT cell [4] results showed that they have solved the electron transport across the c-Si(n)/a-Si:H(i/n) back contact; we also found the heterojunction contact to p-type wafers straightforward to

make. Other groups have required a μc-Si:H p-layer for good back contact to c-Si(p) [5]. In contrast, we make an a-Si:H (i/p) back contact to c-Si(p), as shown clearly in HRTEM (Fig. 3).

Back-surface reflection

In addition to good passivation, the back contact must provide good back-surface optical reflection. Figure 4 compares the internal QE (IQE) of two different back contacts, thereby removing the effect of the reflected light from the identically textured front surfaces. Enhanced long-wavelength response with the a-Si:H(i/p)/Al back contact indicates better surface passivation at the back contact and improved optical reflection from the back metal on a-Si:H compared to the screen-printed alloyed Al-BSF.

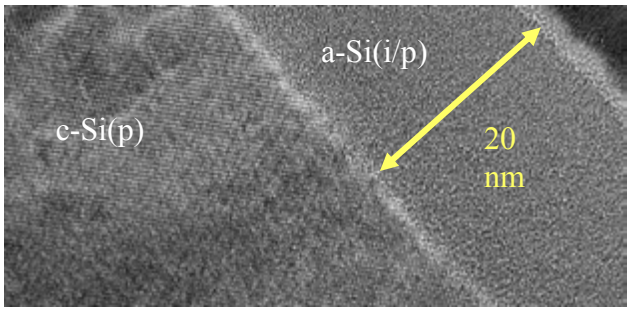

Fig. 3. High-resolution TEM of abrupt c-Si(p)/a-Si:H(i/p).

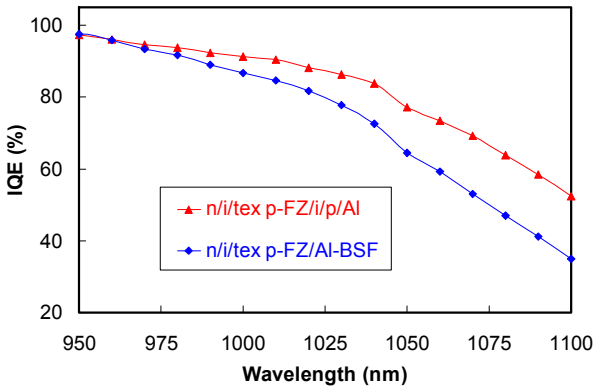

Fig. 4 Significant enhancement in IQE by front ITO/texture coupled with an effective a-Si:H(i/p)/Al back reflector, as compared to a simple Al-BSF.

CONCLUSIONS

We successfully replaced the conventional high-temperature Al-BSF in double-heterojunction solar cells. These cells employ HWCVD a-Si:H front emitters and HWCVD a-Si:H back contacts on p-type silicon wafers. A full metal layer directly on an a-Si:H(i/p) back contact significantly enhances back-surface reflection. The a-Si:H(i/p)/Al back contact has enabled us to achieve fill factors exceeding 77% and conversion efficiencies of 18.2% on textured p-type FZ silicon wafers.

ACKNOWLEDGMENTS

We thank Scott Ward, Anna Duda, and Bobby To for their valuable technical contributions and Ajeet Rohatgi, and Vijay Yelundur for providing textured wafers with and without Al-BSF. We acknowledge Keith Emery and Tom Moriarty for providing confirmed AM1.5 I-V measurements. This work is supported or funded under U.S. DOE Contract No. DE-AC36-99G010337.

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OVERCOMING THE FUNDAMENTAL PERFORMANCE LIMITATIONS OF SCREEN-PRINTED SOLAR CELLS

S.R. Wenham [1,2], Z. Shi [2], L. Mai[1], B. Tjahjono[1], J. Ji [2]
[1]School of Photovoltaic Engineering, University of New South Wales, Sydney, NSW 2052, Australia
[2] Suntech Power Co. Ltd., China

ABSTRACT

Conventional screen-printed solar cells have suffered from poor response to short wavelength light since their invention 30 years ago due to the metallisation's requirement for a heavily diffused emitter. Two new approaches have been developed to facilitate compatibility between screen-printed metal contacts and lightly diffused emitters with sheet resistivities in excess of 100 ohms/square. One approach limits the depth of metal penetration so as to minimise the contact resistance to the lightly diffused emitter. Efficiencies of 17-17.5% appear feasible with near unity internal quantum efficiencies for short wavelength light. The second approach involves a new emitter design incorporating semiconductor fingers for use with conventional screen-printing technology. Direct comparison between conventional screen-printed cells and those incorporating semiconductor fingers shows the latter to have about a 10% performance advantage with efficiencies in the vicinity of 18% demonstrated on 150cm^2 devices.

STANDARD SCREEN-PRINTED CELLS

Conventional screen-printed solar cell technology has remaind virtually unchanged for almost 30 years and yet continues to dominate commercial photovoltaic manufacturing, with well over 50% share of international markets. In recent years, the photovoltaic industry has been booming, with product shipped having more than doubled in the last 2 years. A large majority of the new manufacturing capacity is still based on conventional screen-printed solar cell technology, aided significantly by the availability of appropriate screen-printing equipment and the relatively low CAPEX costs (typically US$0.5-1.0 million per MWp) for such expansion based on this technology. Despite the dominance of this technology shown in Figure 1, the structure has significant performance limitations that limit the cell efficiencies to well below those achievable in research laboratories around the world. In particular, the front surface screen-printed metallisation necessitates a heavily diffused emitter to achieve low contact resistance and also adequate lateral conductivity in the emitter since the metal lines need to be widely spaced compared to laboratory cells to avoid excessive shading losses. Such cells therefore typically have emitter sheet resistivities of 40-50 ohms per square, which inevitably significantly degrades response to short wavelength light. To raise this sheet resistivity to above 100 ohms per square as required for near unity internal quantum efficiencies for short wavelength light, serious resistive losses are introduced, both in the emitter and the contact resistance at the metal/silicon interface. This is shown in Table 1, where standard commercial screen-printed solar cells were fabricated with the surface sheet-resistivity being the only variable which was adjusted by varying the diffusion temperature. The fabrication sequence was typical of commercial sequences: saw damage removal/texturing; top surface diffusion; edge junction isolation; diffusion oxide removal; PECVD silicon nitride; screen-print rear metal and dry; screen-print front metal and dry; co-fire metal contacts.

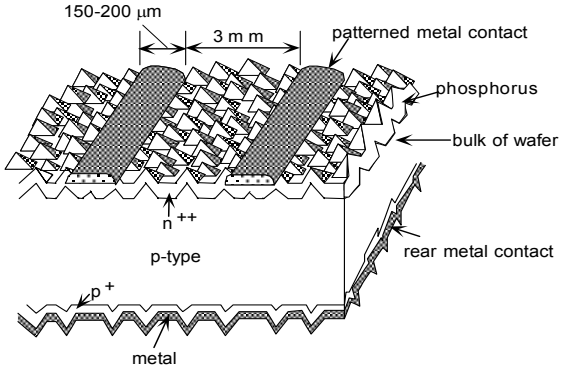

Figure 1: Conventional screen-printed solar cell with heavily diffused emitter and large metal/silicon interface area for the front surface metallisation.

Table 1: Screen-printed cells fabricated with standard processing except for the use of a range of different diffusion conditions to give the corresponding emitter sheet resistivities as shown.

Sheet Resistivity	Jsc mAcm^{-2}	Voc mV	FF %	Efficiency %
30	32.6	612	79.1	15.8
45	34.5	620	77.0	16.5
80	36.0	611	66.2	14.5
115	36.5	595	44.1	9.5

These results are typical of those found by various companies and research groups in the past although in this work, a special paste that does not contact p-type silicon (and hence won't shunt the junction) was used. The shunt resistance values for all cells therefore remained high although fill factor and Voc loss was still sustained in the cells that had the highest emitter sheet resistances as metal penetrated to the junction causing significant junction recombination. It is also interesting to get rough approximations to the various components of resistive loss in these devices to give insight into the loss mechanisms. In particular, the effective contact resistance rapidly increases with increasing emitter sheet resistivity, partly due to the actual contact resistance increasing due to the reduced phosphorus doping concentration at the silver/silicon interface, and partly due to the current crowding that occurs for current trying to enter the edges of the screen-printed metal lines because of how close to the junction the silver penetrates with the more lightly diffused emitters. These two components are lumped together under the heading "Contact resistance", and compared to the metal and emitter resistance losses in Table 2. These values have been approximated via measuring the surface voltage values at a large number of points across the cell surface with the device under short circuit conditions and under 1-sun illumination. Interestingly, the power loss in the contact resistance is approximately double the actual emitter resistance loss for each emitter sheet resistivity used in this work.

Table 2: Rough values for % power losses in the various components of series resistance related to the top surface of the screen-printed solar cell

Sheet Resistivity	Contact Resistance	Emitter Losses	Ag Metal Losses	FF %
30	1%	0.5%	1%	79.1
45	2%	1.0%	1%	77.0
80	12%	5%	1%	66.2
120	18%	7%	1%	44.1

When drawing conclusions from the results of Tables 1 and 2, it is not surprising that the general consensus is that emitter sheet resistivities approaching 100 ohms per square are not compatible with screen-printed metal contacts. However, in this work, two approaches have been identified for overcoming the incompatibility between screen-printing metalisation schemes and such lightly diffused emitters that facilitate the achievement of near unity internal quantum efficiencies for short wavelengths of light.

LOW PENETRATION DEPTH OF AG METAL

It is clear from Table 2 that contact resistance is the dominant resistive loss in the devices with lightly diffused emitters. Although not shown in the Table, high ideality factors due to juntion recombination are another significant contributor to the low fill factors of these cells. Both major loss mechanisms however have been shown to be able to be greatly reduced by restricting the silver metal penetration depth: firstly because the metal doesn't reach the juntion region to cause junction recombination; secondly, because the metal/silicon interface remains in a region of higher doping, therefore minimising the contact resistance; and thirdly, it avoids the current crowding that inevitably occurs at the edges of the metal lines with greater metal penetration depth. In this work, a technique has been developed for reliably controlling the penetration depth of the screen-printed metal. Table 3 shows a direct comparison between two identically processed batches of cells (even with the same emitter sheet resistivities) except for one batch using the new techniques for limiting the n-type metal penetration depth.

Table 3: Average cell parameters for two identically processed batches of cells, with the same emitter sheet resistivities, except for one batch using the new techniques for limiting the n-type metal penetration depth.

N-type Contact	Ohms/ squ	Jsc $mAcm^{-2}$	Voc mV	FF %	Effic %
Standard metal	115	36.5	595	44.1	9.5
Shallow metal	110	36.3	625	73.7	16.7

As expected, the short circuit current density remains virtually identical. As seen from the spectral response in Figure 2, the current from these cells is probably close to the maximum possible for a screen-printed solar cell without either improved minority carrier diffusion lengths in the wafer and/or reduced rear surface recombination velocity.

However as also seen from Table 3, a large increase in Voc of 30mV was achieved through avoiding the metal penetration into the juntion region and the apparent corresponding junction recombination, with a significant increase also in fill factor due to the reduced ideality factor. The largest increase in performance though appears to be from reduced contact resistance. The components of resistive loss are again roughly compared in Table 4.

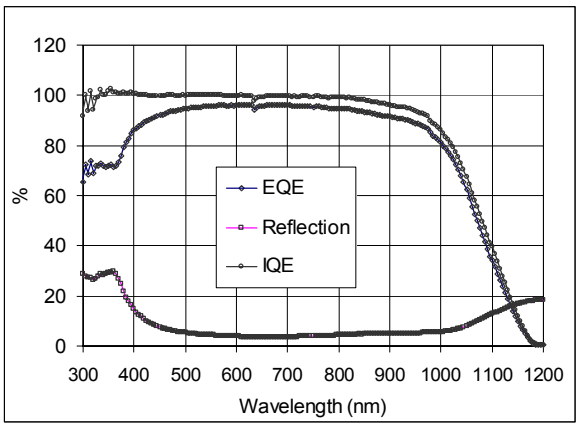

Figure 2: Spectral response for a screen-printed cell with emitter sheet resistivity >100 ohms/squ

Table 4: Resistance power losses for two batches of cells both with emitter sheet resistivities in the vicinity of 100 ohms/square, but with one batch using reduced Ag metal penetration.

N-type Contact	Contact Resistance	Emitter Losses	Ag Metal Losses	FF %
Standard metal	18%	7%	1%	44.1
Shallow metal	4%	6%	1%	73.7

An important aspect of the results from Table 3 is that the cell design is no longer optimal for this emitter sheet resistance. For example, reducing the metal finger spacing from 2.8mm to 2.0 mm should approximately halve the emitter losses to about 3%, reduce the contact resistance losses to below 3%, and reduce the silver metal losses to about 0.7%. In combination, and allowing for the increased metal shading loss of 2%, cell efficiencies should increase from the 16.7% shown in Table 3 to above 17% efficiency. Despite this, the resistive losses will remain high as a percentage power loss (>6% for the emitter and contact alone) opening the opportunity for further innovations in cells design, such as through the use of semiconductor fingers in the next section, to further increase the efficiencies of screen-printed solar cells.

SEMICONDUCTOR FINGER CONCEPT

Rather than reducing the metal finger spacing to reduce the emitter and contact resistance losses shown in Table 4, an alternative is to add thin stripes of heavily phosphorus diffused silicon, called semiconductor fingers, running perpendicular to the metal fingers. These semiconductor fingers potentially have two very important benefits, firstly in reducing the contact resistance by providing extremely heavily doped silicon at the metal/silicon interface and secondly by eliminating the majority of the emitter resistance losses by carrying the bulk of the current to the metal contact [1,2]. A schematic of this structure is shown in Figure 3 showing a cross-section of the heavily doped grooves that form the semiconductor fingers with the metal fingers runninging perpendicularly to the grooves and making contact to the silicon within the grooves. Figure 4 shows a photo of the new cell top surface where the metal finger can be seen crossing the horizontal semiconductor fingers that are typically spaced 0.5-1mm apart. Table 5 shows the significant improvements in fill factor and resistive losses achieved with this new emitter design.

Table 5: Reduced resistive losses and improved fill factor through the use of semiconductor fingers and an emitter sheet resistivity >100 ohms/squ

N-type Contact	Contact Resistance	Emitter Losses	Silver Losses	FF %
Shallow metal	4%	6%	1%	73.7
Semiconductor Fingers	<0.5%	<0.5%	1%	79.5

With such low emitter resistive in the cells with 17.9% efficiency, a more optimal design is one with wider metal finger spacing.

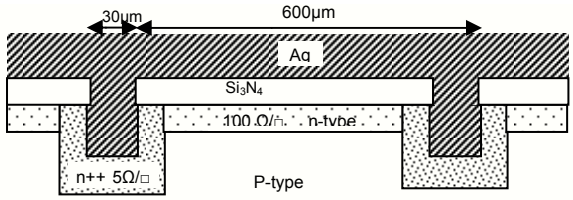

Figure 3: Cross-section of the heavily doped semiconductor finger grooves showing the perpendicular screen-printed metal fingers and the antireflection coating. The latter also passivates the lightly diffused emitter surface while simultaneously isolating the screen-printed metal from the lightly diffused top surface of the wafer.

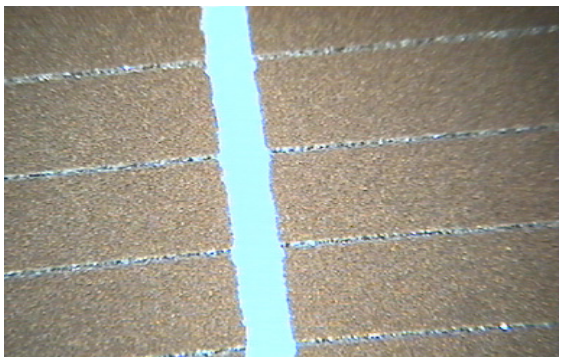

Figure 4: Screen-printed fingers running perpendicular to the heavily diffused grooves where electrical contact is made.

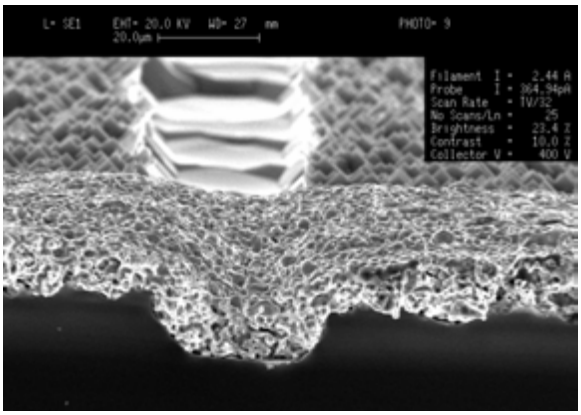

Figure 5: SEM of a screen-printed metal line crossing a semiconductor finger.

IMPROVED OPEN CIRCUIT VOLTAGES

Another weakness of the conventional design of figure 1 is the poor surface passivation, particularly in the metalised regions as a result of the large metal/silicon interface area and the lack of a selective emitter to more effectively isolate this high recombination velocity interface from the active regions of the cell. Even when good ohmic contacts can be made to the lightly doped emitter as demonstrated with the shallow metal in Table 3, the large metal/silicon interface area still significantly limits the voltages due to the corresponding high contribution to the device dark saturation current. These voltage limitations are not of major significance for current technology due to the limitations imposed by the substrates and rear surface. However, in the future as wafer thicknesses reduce to improve device economics, cells will have the potential for improved Vocs, but only provided the surfaces, including under the metal, are better passivated than at present.

The semiconductor finger devices fabricated in this work achieved an improvement in Voc of about 2% on average compared to conventional cells. The magnitude of this improvement appears to be limited by the dark saturation current contributions from the substrate and the rear surface. The new emitter design and corresponding front surface metalisation are believed to be compatible with achieving Vocs well in excess of 650mV due to the use of a selective emitter with heavy doping beneath the metal contact, low metal/silicon interface area below 1%, and a well passivated lightly diffused surface layer. This should be of significant value in future evolutions of this technology with the use of thinner wafers and improved rear surfaces.

CONCLUSIONS

The fundamental performance limitations of screen-printed solar cells, originating from the need for heavily doped emitters, can be potentially overcome in several ways. One approach is to limit the penetration depth of the metal thereby making it feasible to achieve good ohmic contact to relatively lightly diffused emitters with sheet resistivities >100 ohms/square. Such emitters when passivated with conventional PECVD silicon nitride, have been shown in this work to achieve short wavelength responses as good as the best laboratory cells, an area where screen-printed solar cells have traditionally performed very poorly. This approach appears capable of taking screen-printed cells from about 16.5% at present to 17-17.5% efficiency in the future.

A second approach is through the use of a new emitter design that makes use of semiconductor fingers to alleviate the need for a heavily diffused top surface. This facilitates the achievement of near unity internal quantum efficiencies for short wavelength light. Other advantages compared to conventional screen-printed solar cells include reduced shading losses through wider metal finger spacing, reduced emitter resistive losses facilitated by the semiconductor fingers, lower contact resistance by virtue of the very heavy doping at the metal/silicon interface and improved voltages by reducing the metal/silicon interface area by an order of magnitude. The net result of these improvements is an increase in performance of more than 10% to efficiencies above 18%. Just as importantly, the new designs are compatible with existing screen-printing cell equipment and infrastructure with the cells in this work having been fabricated on a standard commercial cell production line.

ACKNOWLEDGEMENTS

The presented work has been jointly supported by Suntech Power Co Ltd in China and the Australian Research Council's Photovoltaics Centre of Excellence. The cells used in this work were manufactured on the production line of Suntech Power.

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PASTE DEVELOPMENT FOR LOW COST HIGH EFFICIENCY SILICON SOLAR CELLS

Jalal Salami, Ben Cruz and Aziz Shaikh
Ferro Corporation, Electronic Material Systems
1395 Aspen Way, Vista, CA 92083, USA
Phone: (760)-305-1062, Fax: (760)-305-1100
Email: Salamij@ferro.com

ABSTRACT

Increasing cell efficiency and lowering the manufacturing cost is a continuous challenge in solar cell industries. Higher efficiency concepts like interdigitated back contact (IBC), emitter wrap through (EWT), and bifacial cells are ways to reduce the total solar cell manufacturing cost by increasing the solar cell efficiency. Typically the high efficiency concepts require costly extra processing steps. Developing the proper paste for printing application of high efficiency concepts could make these designs cost effective and reduce the manufacturing cost by using screen-printing technology. This paper describes newly developed low cost phosphorous, boron, and diffusion barrier pastes. It shows the characterization of the newly developed phosphorous paste (99-038), boron paste (99-033), and diffusion barrier paste (99-001). These low cost pastes can easily be printed using typical low cost screen-printing or ink jet printing methods. Another way to reduce solar cell manufacturing cost is to use thinner silicon wafers. Currently manufacturers are trying to use less than 200 μm thick silicon wafers. Newly developed aluminum boron (Al/B) paste is introduced as a low-bow lead-free replacement for typical Aluminum (Al) paste for 150 to 200 μm thick silicon wafers with less than 1.5 mm bowing.

INTRODUCTION

Silicon solar cell manufacturers want to reduce manufacturing cost by using thinner silicon wafers (less than 200 μm) and high efficiency solar cell concepts. A major problem with Silicon wafers below 200 um is bowing after Al back surface field (BSF) formation. A printable boron or Al/B paste that can form BSF at typical processing temperature is an ideal solution to wafer bowing. Boron paste makes it possible to use both p-type and n-type wafers in typical solar cell manufacturing. It also makes it possible to fabricate a bifacial solar cell by simultaneous diffusion of phosphorous and boron paste in a single diffusion step. Other high efficiency concepts like IBC cells and EWT cells need n^+ diffusion (phosphorous paste), p^+ diffusion (boron, Al, Al/B or Ag/Al paste) and a diffusion barrier paste to isolate the n^+ regions from the p^+ regions during contact formation. Diffusion barrier paste can easily be applied as the mask to isolate n^+ areas from the p^+ areas. The newly developed low-bow lead-free Al/B paste, phosphorous paste, boron and diffusion barrier paste by Ferro can pave the way for the next generation of low cost high efficiency solar cells.

EXPERIMENTAL

The phosphorous diffusion paste 99-038, Boron diffusion paste 99-033, and diffusion barrier paste 99-001 were developed and screen printed on 100 cm^2 CZ wafers with thickness of 300 μm and resistivity of 1 to 2 Ω-cm to investigate diffusion properties. All the pastes were screen-printed using a 200-mesh screen with emulsion thickness of 0.5 to 0.7 mils. Measured deposited weights are about 1 to 2 mg/cm^2 for all diffusion pastes that are dried at

200^{o} C for 2 to 5 minutes. All the pastes were fired at different temperatures in air ambient using an infrared belt furnace. The resulting emitters were characterized by four-point probe. Depth profiles were measured using spreading resistance analysis.

Low-bow lead-free Al/B paste formulation involves finding an optimum in Al powder size, morphology, frit chemistry, organic and inorganic additives to make up the paste. Varieties of environmentally friendly organic and inorganic compounds were tested to improve sintering without increasing the bowing of silicon solar cells. An optimum paste formulation was engineered from the combination of all the additives and compounds. Adding boron to Al paste will make it possible to achieve higher concentration of p^{+}-doping in BSF with lower amount of Al paste. New Al/B paste can control BSF profile thickness and maximum doping concentration. The amount of paste deposited on silicon wafers determines the thickness of BSF layer and the alloying temperature controls the doping concentration from 3E18 to 9E19 cm^{-3}.

RESULTS

Phosphorous Paste

Figure 1 shows measured sheet resistance for phosphorous paste as a function of diffusion temperature for different phosphorous concentration. Measured minority carrier lifetime was improved after diffusion from 10 µsec to 25 µsec. Figure 2 shows the measured junction depth and surface concentration. Regions with higher phosphorous concentration had emitter depth of 0.4 µm and surface concentration greater than 10^{20} cm^{-3}. Regions with lower phosphorous concentration show shallower emitter depth of 0.15 um and surface concentration of 10^{19} cm^{-3}. This allows for selective emitter diffusion concept to be controlled by changing the phosphorous concentration and keeping the temperature constant.

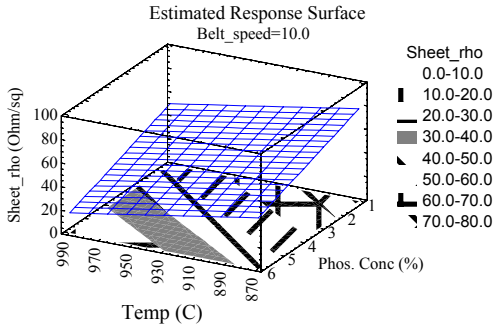

Fig. 1. phosphorus sheet resistance as a function of phosphorus concentration and diffusion temperature.

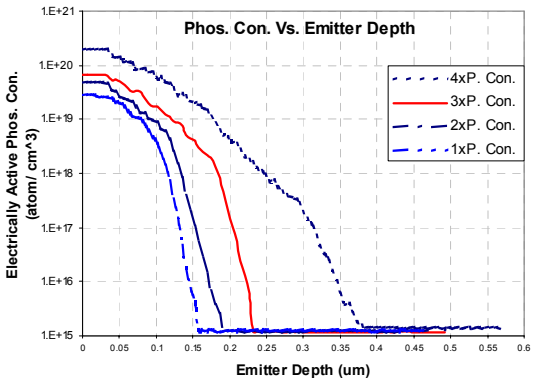

Fig. 2. Measured phosphorous concentration and emitter depth using spreading resistance technique.

Boron Paste

Figure 3 shows the measured sheet resistance and a linear model to describe the relationship between boron diffusion temperature and measured boron sheet resistance with 95% confidence limits. Figure 4 shows the measured junction depth and surface concentration. Boron paste and phosphorous paste can be printed and dried and co-diffused at the same time to get an emitter and a BSF. This is an inexpensive way to make bifacial solar cells.

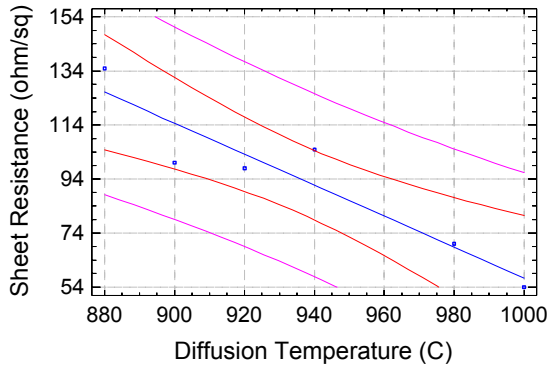

Fig. 3. Measured boron sheet resistance at different temperatures and a fitted linear

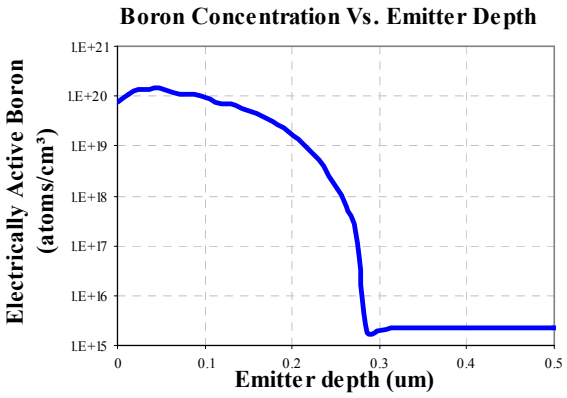

Fig. 4. Measured boron concentration and emitter depth using the spreading resistance technique.

Diffusion Barrier

99-001 developed diffusion barrier paste forms a TiO_2 layer after curing at 450 to 500°C. Silicon wafers were printed with diffusion barrier paste and after curing the diffusion barrier paste the wafers were screen printed with phosphorous paste. Then samples were heat treated at 980 °C for 5 minutes. Figure 5 shows spreading resistance measured after diffusion under the diffusion barrier layer. This shows that diffusion barrier 99-001 can easily be used to block phosphorous diffusion. 99-001 can lower the manufacturing cost of IBC type solar cells.

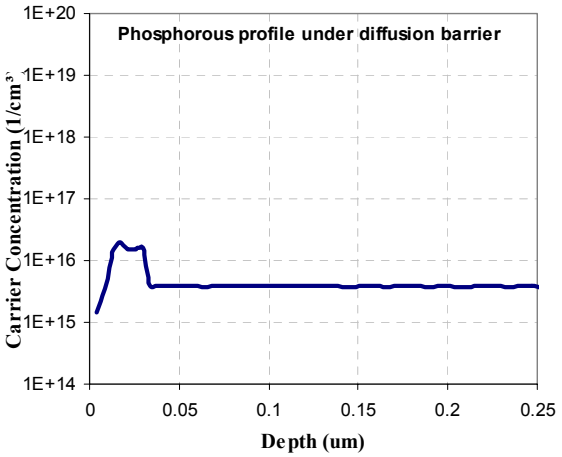

Fig. 5. Measured phosphorus concentration through diffusion barrier paste.

Low-Bow Lead-Free Al/B Paste

The screen printed alloyed aluminum BSF is the standard rear passivation and contact for more than 85% of industrial silicon solar cell production. Most manufacturers like to use thinner silicon wafers to reduce the production cost. In an industrial silicon solar cell process, a thick layer of about 30 to 60 µm of Al paste is screen printed onto the backside of Si wafer and fired at 750 to 850ºC for a few seconds to alloy Al and form p+-doping in silicon. The wafer bowing is caused by thick aluminum paste deposit and different thermal coefficients (CTE) of expansion of aluminum and silicon. Ferro Al/B paste is designed to reduce bowing by engineering the paste ingredients to minimize the CTE effect and be able to deposit less paste without losing rear surface passivation. Figure 6 shows modeling results for reducing effective surface recombination velocity by increasing the BSF doping. The new Al/B paste is formulated with a boron source that can provide higher concentration of p+ dopant during the Al alloying process. Al alloying process without boron is limited to solid solubility of Al in silicon. This results in doping concentration of 2 to 3E18 cm^{-3} at typical firing temperatures and belt speeds. Figure 7 shows the measured doping profile using the spreading resistance technique for Al/B paste. It shows that Al/B

paste can yield a BSF layer with carrier concentration of one order of magnitude higher than Al doping profiles.

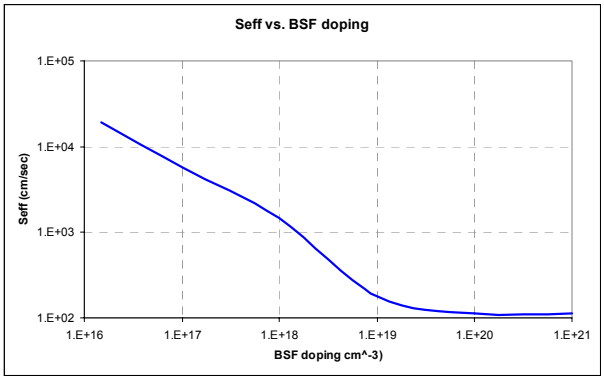

Fig. 6. PC1D modeling of effective surface recombination velocity vs. BSF doping

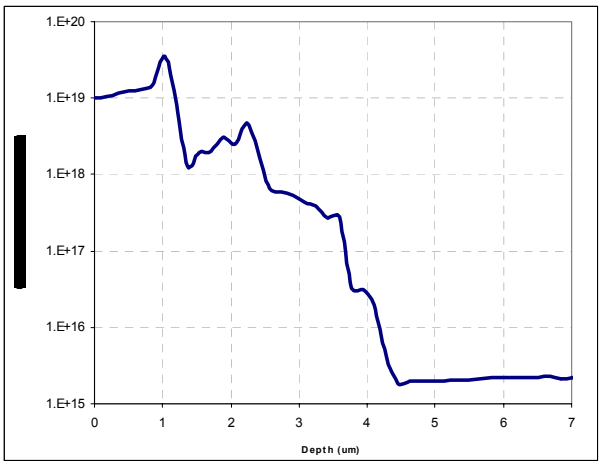

Fig. 7. Measured carrier concentration vs. BSF depth using spreading resistance method.

We have printed the newly developed Al/B paste on 6-inch square and 160 µm thick multi-crystalline wafers using a 200-mesh screen. The initial wet deposited weight is about 6.9 mg/cm^2 and after firing the deposited weight is about 4.9 mg/cm^2. The wafer is then co-fired at typical firing temperature at 120 IPM belt speed. The following table shows average measured electrical parameters for these cells:

Paste	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
Al/B	603.4	32.9	76.1	15.1

The averaged bowing of these wafers ranges from 0.5 to 1.2 mm.

SUMMARY

Ferro has introduced the following diffusion related pastes: phosphorous paste 99-038, boron paste 99-033, and diffusion barrier paste 99-001. These new high quality diffusion pastes and diffusion barrier pastes can reduce manufacturing costs and make it possible to use less than 180 µm thick silicon wafers for selective emitter solar cells, IBC cells, emitter-wrap-through (EWT) cell design, and bifacial solar cell application. Also we have reported on the development of a new low-bow lead-free Al/B paste (53-120) for 150 to 200 µm thick silicon wafers.

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PV Module Encapsulation – Materials, Process, and Reliability

F.J. John Pern
National Center for Photovoltaics
National Renewable Energy Laboratory
1617 Cole Blvd., Golden, CO 80401

Abstract

This paper presents a general overview on the encapsulation of photovoltaic (PV) modules and related encapsulation materials, common practices of encapsulation process, and performance reliability issues. More emphasis is placed on the types, properties, and performance of encapsulation materials ranging from glass superstrates to pottants such as EVA and non-EVA polymers, substrate backfoils, and edge sealants. Photothermal discoloration and effects of moisture ingress on adhesion of EVA encapsulants and corrosion of metallic components are illustrated. In general, PV module reliability is often affected by the property of the encapsulation materials and the quality of the encapsulation process.

Introduction

Inadequate or defective packaging can be the predominant cause of failure in PV modules. Although there are some differences in the module encapsulation methods between crystalline-based and thin film-based PV modules, similar construction configurations have been employed that includes a superstrate, an encapsulant (pottant), and a substrate, as schematically illustrated in Fig. 1. Crystalline Si-based modules typically use a glass/pottant/solar cells/ pottant/backfoil configuration; for their building-integrated modules, a double-pane configuration of glass/pottant/solar cells/pottant/glass is generally used. On some modules, a polymeric Tefzel superstrate cover may be employed with a light-weight supporting substrate. A common feature in all three cases is that the solar cell strings are sandwiched between two layers of encapsulant film. For thin film modules, with the solar cell arrays being deposited either on a superstrate or substrate, which may be a hard solid plate (e.g., glass or ceramic) or a flexible materials (e.g., stainless steel foil and polymer sheet), only one layer of encapsulant film is needed.

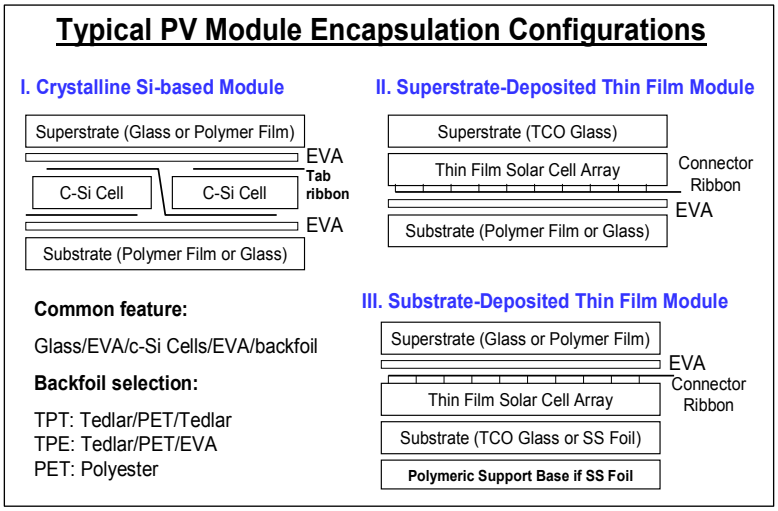


Fig. 1. Simplified illustration of encapsulation schemes for crystalline-Si and thin film modules, with common feature and backfoil materials indicated for c-Si module.

Due to the diversity of module designs, a large variety of encapsulation materials, ranging from glass, to non-glass, polymeric encapsulants, and multilayered backfoils, are available for selection for use. The diversity also results in the differences in the use of encapsulation or

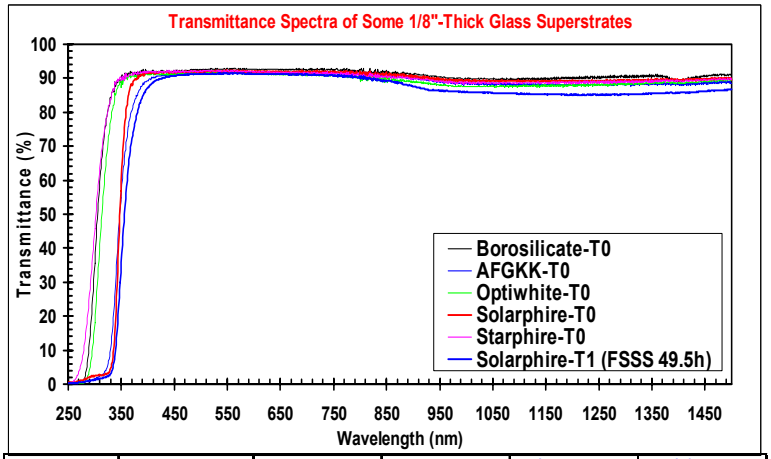
lamination method and equipment. In the following, an overview is given on the types and properties of the encapsulation materials, encapsulation process, and potential performance reliability issues. The cited data or information are either obtained from a large number of experiments in our labs over the years, reported in the literature, or private communications or interactions with industrial personnel.

Encapsulation Materials

The encapsulation materials constitute the majority of a PV module construction and play the indispensable role of supporting and protecting the solar cells. For the sake of convenience of discussion hereafter, they are generally divided into three subcategories: superstrates, encapsulants (or pottants), and substrates.

1. Superstrates. The superstrates are typically light transmitting materials for solar cells laid or deposited underneath.

1-a. Glass Plates. They have been the most widely used superstrates (or cover plates, as some prefer to calling it this way), and may have texture on one side. A majority of the glass plates are the low-iron type to avoid high absorption of light by the iron ions in the visible-IR range such as in the case of greenish window glasses. For safety reasons, they are normally tempered. After the "EVA browning" problems were recognized in the early 1990's, UV-filtering glass containing cerium oxide such as PPG's Airphire (or Solarphire) was confirmed in our laboratory around 1994 capable of reducing or minimizing the EVA photodiscoloration rate [1]. Various Ce-glass products, such as AFG's Krystal Clear, Solatex, and Solite, have been used by PV industry for the past decade. The UV-filtering extent depends on the doping concentration of the cerium oxide. Although it can effectively reduce or minimize the EVA yellowing rate, the Ce-glass also found itself a disadvantage that arises from its rapid solarization [2], as shown in Fig. 2. The integrated transmittance losses for five glasses due to solarization by exposing under a full-spectrum solar simulator (FSSS) for 49.5 h are given in the table under the figure. The solarization on Ce-glasses reduces a 1.4~2.4% light transmission in the solar cell-sensitive region of ~700-1500 nm and a smaller 0.7~1.1% loss in the 350-420 nm region (see the two columns on the right in the table), which can cause a noticeable loss of module power. Lately, some PV



Glass Type	Borosilicate		Pilkington OptiWhite		PPG Starphire		AFG Krystal Klear (CeOx)		PPG Solarphire (CeOx)	
Integation/Loss	T0*	T1 (loss%)*	T0	T1 (loss%)	T0	T1 (loss%)	T0	T1 (loss%)	T0	T1 (loss%)
Int(300-1500nm)	108643	**0.83**	106180	**0.44**	107620	**0.15**	103453	**2.10**	104469	**3.62**
Int(300-500nm)	17578	**0.60**	16943	**0.56**	17652	**0.33**	13906	**0.66**	14128	**1.07**
Int(700-1500nm)	72629	**0.20**	71049	**-0.16**	71676	**-0.17**	71339	**1.37**	72045	**2.42**

* T0 = 0 h before exposure. Numbers are integrated transmittance for each range specified
T1 = 49.5 h expsosure under full-spectrum solar simulator (5~7 UV suns in 300-400 nm range) at BPT ~80°C
Loss (%) = change (T0-T1)/Int(300-1500) at T0 * 100

Fig. 2. Transmittance spectra of various glass plates measured by a Cary 5G UV-vis-NIR spectrometer with an integration sphere before exposure under a full-spectrum solar simulator (FSSS) for 49.5 h. Spectrum for solarized Solarphire was shown. The attached table shows the integrated transmittance under indicated ranges before and losses after solarization.

manufacturers have changed to the non-Ce-glass such as Pilkington's OptiWhite or SunPlus, which has transmittance spectrum similar to a Pyrex or borosilicate. These glass plates also show solarization, as seen in the table of Fig. 2, but in the UV region, which in fact is beneficial to slow down the EVA yellowing rate in later stage of light exposure.

Another relatively new development is the anti-reflection (AR) coating applied on glass superstrates that were first shown in 1998 to improve light transmission and cell photocurrents [3]. Apollon Solar of France uses SiOx AR coatings on glass superstrates to reduce the light reflection losses on their "NICE" modules that are assembled without encapsulant [4,5]. JiangSu Almaden PV Glasses of China recently reported the development of a self-cleaning AR coating for PV glass application, but technical information is not readily available. The long-term performance reliability/durability of these AR coatings has yet to be demonstrated, however.

1-b. Polymer films. Fluoropolymer thin films such as DuPont's Tedlar and Tefzel that have excellent weatherability are more commonly used on flexible a-Si modules such as Iowa Thin Films and United Solar's products. Recently, SBM Solar employed Tefzel for their light-weight c-Si module panel designs [6]. These fluoropolymer films typically have a corona-treated side (cementable side) to allow better adhesion with EVA. Because of their air permeability that allowed for photobleaching, EVA in the c-Si laminates using Tefzel as either superstrate or substrate cover film would not become yellow-brown like in glass laminates, as demonstrated in our early work [1]. Low cost polyolefin films were also investigated and showed inadequate adhesion strength, as had been tested in our lab for a PV company, but their use in commercial products is not clearly known.

2. Encapsulants (Pottants):

2-a. Functions. The encapsulant may be considered as the most critical element in the assembly and performance reliability of PV modules. Generally speaking, depending on module construction configuration, the encapsulant layer serves all or part of the following functions:

- Optical coupling - between glass superstrate and encapsulant, which requires good matching of refractive index (e.g., n ~ 1.5 for glass and 1.48 for EVA or ~1.5 for most polymer pottants) as well as high transmittance (>90~92%) and low UV-induced yellowing of the encapsulant.
- Mechanical support – fixation of c-Si solar cell strings to the glass plate and/or backfoil, which requires high and durable adhesion strength from the encapsulant layers.
- Physical insulation – separation of neighboring solar cells and strings from contact.
- Electrical insulation – for solar cells (and modules) from shorting or arcing as well as high voltage insulation in a large PV system, which requires high dielectric strength and volume resistivity of the encapsulant.
- Physical protection – from weathering-induced degradation and environmental damages, which requires low moisture absorption/retention, durable adhesion strength against damp heat, high mechanical strength and resistance to break or tear of the encapsulant.
- Thermal conduction – for helping dissipation of heat from solar cells.

2-b. Materials. Several polymer materials, in the form of films or liquid, have been used or under investigations for module encapsulants. The list includes EVA (ethylene vinyl acetate), PVB (polyvinyl butyral), TPU (thermoplastic polyurethane), ionomer based on Surlyn, silicones, epoxy, and UV-curable resins, etc. While there is a lack of test standard or qualification program for the evaluation of an encapsulant, we typically conduct at least several basic measurements:

- Light transmittance in the 250-1500 nm range using a Varian Cary-5G scanning UV-vis-NIR spectrophotometer equipped with an integration sphere.
- Curing and gel% analysis.
- Volume resistivity using a Keithley 6517A high resistance electrometer and a Keithley 8008 resistivity test fixture with alternating polarization at ±700V.
- Adhesion strength on a smooth surface of glass plate such as AFG Krystal Klear (KK) and on common backfoils of interest, such as primed-TPT, TPE, PET, and/or Tefzel, measured by using an Instron Model 5500 tensile-test apparatus at 90-degree pull.

On performance reliability, we commonly conduct accelerated exposure/weathering tests:

- Photothermal stability (UV-induced yellowing) test by exposing glass/encapsulant/glass laminates under a full-spectrum solar simulator (FSSS, average ~6 UV suns) at black panel temperature (BPT) ~80^{o}C for ≥1000 h, or in a Atlas Ci4000 weatherometer for >3~6 months. Periodic measurements of color indices (primarily, yellowness index, YI) and transmittance are conducted before and during the course of exposures.
- Damp heat resistance test at 85^{o}C and 85% RH in couple with periodic peel strength test.
- Effects of encapsulants on solar cells may also be conducted when needed or upon request.

2-b-1. EVA. Among the list of encapsulants, EVA has been the most widely used on PV modules for two decades since 1980s, mainly for the reason of being relatively inexpensive. A critical review of the use of EVA as module encapsulants was given by Czanderna and Pern [7]. Because of the serious EVA yellow-browning problems, as seen in earlier modules (Fig. 3, left) that were installed with two Al reflection side panels at the Carissa PV plant, CA, substantial light transmission loss through EVA and consequent large system power losses were reported. At NREL, we had investigated and elaborated the degradation mechanisms as well as stabilization methods from 1990 on [8], resulting in the development and a patent of non-yellowing EVA formulations [9,10]. Newer and better performance EVA formulations have also been developed by STR. Additional to the non-yellowing formulations, we have also been developing and testing high-performance, damp-heat resistant EVA formulations (see below), which are derived from damp-heat resistant glass priming formulations, in the past three years [11,12].

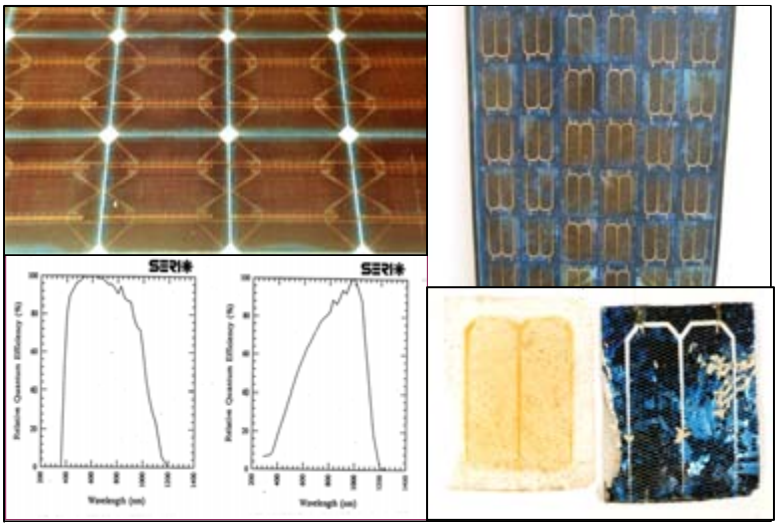


Fig. 3. Photographs of a Carissa module with dark brown EVA (left) and the spectral responses (bottom left) of a Si cell covered with a clear EVA and the browned EVA, and a module that started showing yellowing EVA (right). The EVA removed from the cell exhibits the grid pattern on the cell.

In addition to the expanded production capacities by the existing companies, the number of new EVA manufacturers is increasing globally because of the recent rapidly expanding PV productions and demands for the EVA. However, the quality, shelf-life, and/or performance of the various EVA products tested in our lab can differ substantially. For

examples, Fig. 4 compares the net YI changes (i.e., photothermal stability) of several EVA films, made in NREL (including the PMG), U.S., Germany, Taiwan, and China, respectively, exposed under FSSS. The encapsulants ranged from fast-cure to slow cure, and all were laminated with borosilicate top plate except one (curve: Taiwan KK) with AFG KK to demonstrate the Ce-glass' stabilizing effect [1]. Table 1 compares some curing-gel%, volume resistivity, and initial adhesion strength to smooth glass for some EVA products. Fig. 5 illustrates the difference in the effect of storage time on the initial adhesion strength between two fast-cure EVA products from US and Taiwan, and effect of damp heat exposure on the former. The EVA formulations developed at NREL have shown significant improvements of adhesion strength for damp heat resistance [12]. These differences in properties and performance result from the variation of formulation and processing details, which are normally treated as proprietary.

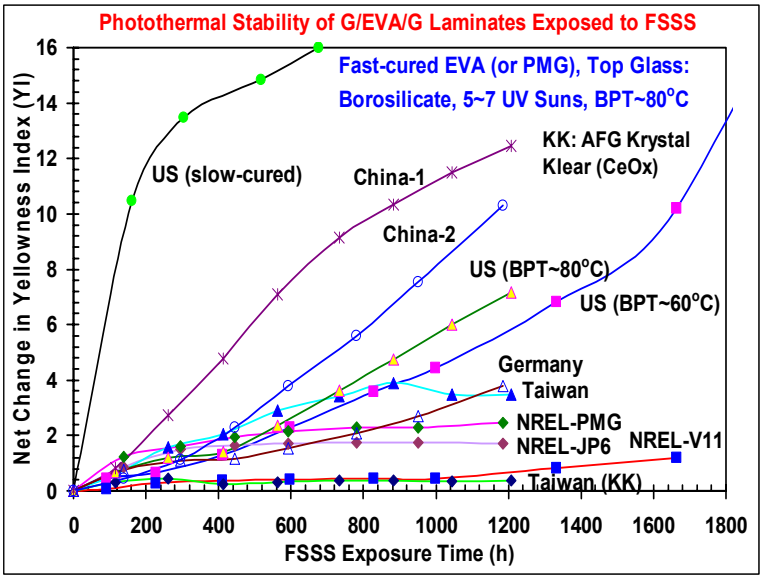


Fig. 4. Net changes in yellowness index for a number of different EVA formulations and one NREL PMG laminated between a borosilicate top plate and another glass substrate exposed under a full-spectrum solar simulator (FSSS). One sample (Taiwan KK) was laminated with Ce-glass AFG KK top plate.

Table 1. Gel%, Volume Resistivity, and Adhesion Strength to Smooth Glass for Some EVAs

EVA Source	145°C/8min Cure Typical Gel (%)	Typical Volume Resistivity (ohm-cm) Uncured EVA	Cured (145oC/8min)	Initial 90° Peel Strength TPE/EVA from KK (N/mm)
China-1	95	N/A (deep texture)	2.3~5.8E+14	
China-2	84	2.2E+14	1.1E+14	
China-3	>90	8.8E+13		
Japan-1	94	1.1E+14	1.2E+14	
Japan-2	86	N/A (deep texture)	3.4E+14	
NREL*	88	0.6~5.5E+14	0.2~1.4E+16	9 ~ 12
US	88	0.8~1.1E+14	0.7~7.0E+14	9 ~ 10.5
Taiwan	88	1~4E+14	1~3E+15	10 ~ 12
Germany	86			
* formulation-dependent with 7 different formulations in study.				

2-b-2. Non-EVA. PVB has been long used for the windshields on the cars and safety glasses. Its use as module encapsulant was short-lived and had been terminated after irregular yellow-browning problems were observed as early EVA on rooftop-mounted ARCO Solar modules in the same period of time. Partly because of its low cost, there are some efforts in the past few years to revive its use by a group in Fraunhofer ISE, Germany [13,14]. We have tested PVB samples from four difference sources, and the results showed that they have good photostability without yellowing when laminated between borosilicate plates and exposed under UV light from

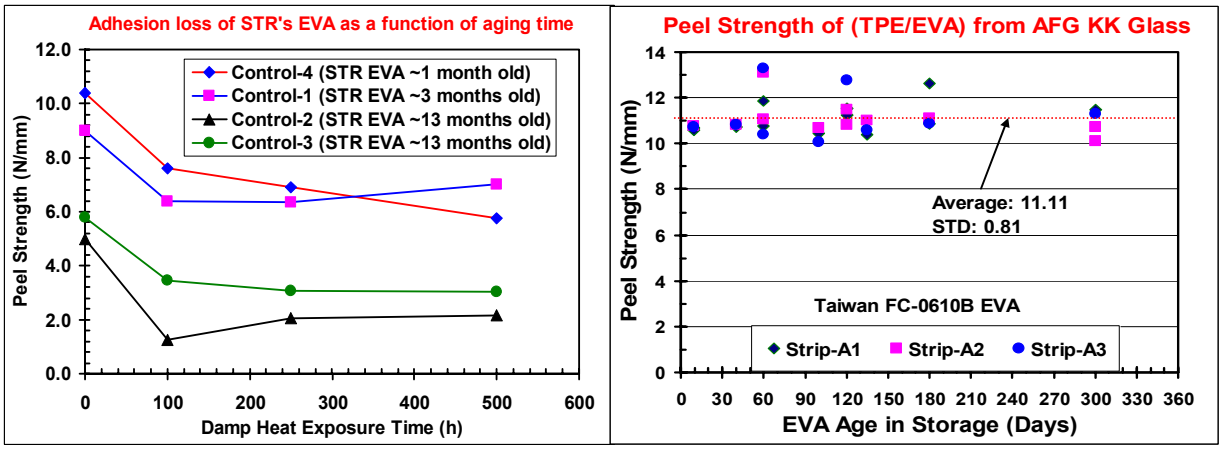


Fig. 5. Adhesion loss as a function of storage time in zipped PE bags in the dark and damp heat exposure for a U.S. STR fast-cure EVA formulation (left), and essentially unchanged initial adhesion strength (without exposing to damp heat) for a Taiwan fast-cure EVA. The test laminates were TPE/EVA/AFG KK and 90-degree peel test.

a FSSS for ~1250 h. However, the PVB films have low volume resistivity in the order of 10^{12} ohm-cm level, and are probably suitable only for glass-glass module laminates since they can't be bonded adequately to common backfoils such as TPE and TPT. Relatively low volume resistivity was also obtained for TPU films from two sources (Germany and US). TPU can be laminated with TPT backfoil but not with TPE. New experiments studying TPU's photostability from two sources are on-going at the present, using glass/TPU/glass laminates in a Atlas Ci4000 weatherometer (WOM, 2.5 UV suns at 60°C and 60% relative humidity) in our lab. A preliminary study earlier by group member M. Kempe has shown yellowing at the TPU/glass interface and cohesive delamination after 3500 h exposure in the Ci4000 WOM. A waxy product was observed on the cohesively torn faces, probably due to hydrolysis of the TPU from Germany. The yellowed TPU was studied with florescence analysis and the results suggested the formation of conjugated double bonds in a way similar to the EVA photodiscoloration [8]. Lately, the adhesion strength of US TPU/TPT to the glass was found by group member G. Jorgenson to have largely degraded when tested in damp heat chamber for >500 h.

Starting from last year, a group in the Dow Corning has been investigating the silcones and their application to novel packaging solutions under a PVMaT subcontract work [15]. Additionally, NREL has developed and tested a non-EVA encapsulant, PMG, which is an ethylene-mathacrylate copolymer containing glycidyl groups. The PMG is slightly higher than EVA in the cost of raw resins, but its fabrication and use as extruded films is similar to that of EVA. The PMG formulations developed at NREL have shown excellent photostability (non-yellowing, see Fig. 4), high adhesion strength to glass substrates, and high damp heat resistance [12]. On the other hand, when compared to EVA, uses of encapsulants such as Surlyn ionomer and liquid epoxy and UV-curable resins are relatively limited on glass-glass modules and/or consumer products.

3. Substrates:

Substrates for PV modules can be glass or multilayer polymer film-based backfoils. SBM Solar employs a special honeycomb Al composite as substrate in couple with Tefzel as top cover film for their light-weight c-Si modules [6]. We will focus the discussion on the multilayer polymer

film-based backfoils that are used on the majority of PV modules. A variety of backfoils are available for selection from several manufacturers such as DuPont, Madico, and Isovolta. They are required to have medium-to-high adhesion strength to the encapsulant, mechanical strength, electrical insulation, and moisture blocking in order to protect the solar cells and metallic components in modules from environmental elements. The more commonly used for years are Tedlar-based films, which have been proved to be highly stable against weather-induced degradation. In recent years, because of the desire to further reduce the costs of backfoils, relatively inexpensive polyester (PET)-based films are gradually becoming more popular. Table 2 lists some of the Tedlar-based multilayer backfoils from Madico and their constitutional components, waver vapor transmission rates (WVTR), and volume resistivity measured in our laboratories. Some data for EVA, PVB, and TPU are also included for comparison.

Table 2. Water Vapor Transmission Rates and Volume Resistivity of Some Encapsulant and Backfoil Films

Backfoil Film Description	Source	Film Construction	Thickness (mm)	Temp (oC)	RH (%)	WVTR (g/m2/day)	Volume Resistivity* (ohm-cm)
EVA 15295	STR	(as-made, uncured)	0.46	37.8	82	28.45	8.42E+13
PVB	Trosifol	(as-made)	0.561				1.69E+12
PVB (2 layers)	Sekisui S-LEC	(as-made)	2 x 0.412**	38.5	100	40.05**	8.40E+12
PVB (2 layers)	Solutia Saflex	(as-made)	2 x 0.792**	38.6	100	33.36**	4.41E+12
PVB (2 layers)	Solutia Saflex	(as-made)	2 x 0.792**	61	100	148.47**	4.41E+12
TPU	Etimex	(as-made)	0.466				1.07E+12
TPU-A4700	Deerfield	(as-made)	0.412				6.39E+13
TAPE	Madico	T1.5/Al0.7/P3/Black EVA	0.240	39.9	100	<.05	1.12E+16
TAPE				84.5	100	<.05	
TAT	Madico	Tedlar1.5/Al0.7/Tedlar1.5	0.105	37.8	86	0.04	4.31E+14
TAT				85	100	0.83	
TPE	Madico	Tedlar1.5/PET3/EVA4clear	0.208	37.9	100	4.48	1.10E+16
TPE				60	100	22.99	
TPE				85	100	94.39	
TPT-primed	Madico	T1.5/P3/T1.5 - primer	0.170	20	84	0.89	2.71E+15
TPT-primed				39	100	7.83	
TPT-primed				83	100	142.77	
TPW-2	Madico	T1.5/P2/White EVA	0.208	39.7	100	6.34	1.07E+16
TPW-2				84.4	100	183.26	
TPW-5	Madico	T1.5/P5/White EVA	0.280	39.6	100	3.50	3.34E+16
TPW-5				84.1	100	76.77	
Solar Edge Tape	TruSeal***	Thermoplastic butyl	1.524			0.26	2.29E+10

* Volume resistivity was measured at room temperature (~21^{o}C).
** Used double layers for higher temperature WVTR measurements
*** Solar Edge Tape data are from TruSeal product bulletin. Voulme resistivity measured at 23^{o}C.

4. Edge Sealants.

Another component in completing module encapsulation is the edge sealant that is often used particularly on Al-framed modules to block moisture from ingress. They are typically polymer materials made of thermoplastic/hot-melt butyl or polyisobutylene (PIB), and may be formulated with fine particles of oxides such as SiO_2 and TiO_2. PIB is one of the best moisture-blocking polymers. The WVTR and volume resistivity of the Solar Edge tape from TruSeal, a thermoplastic butyl, are given in Table 2. Some PV manufacturers in China are using formulated silicone pastes in tubes, but their WVTR, volume resistivity, and adhesion properties are not readily known.

Encapsulation Process

Double-bag vacuum lamination: Because of the popular use of hot-melt EVA encapsulants, the most commonly used encapsulation process in the past two decades has been the employment of a double-bag vacuum laminator that is program-operated with a laminator-dependent temperature-pressure-time (T-P-t) profile. Rapid evacuation of the chamber to achieve moderate vacuum level (e.g., < 5 torr in 1 min or less) is required to remove air from the multiple interfaces to avoid bubbling within the module stack. Heating is needed to melt the EVA and induce cross-linking reaction to produce sufficient gel% (prefer > 80%). Pressing by the silicone diaphragm from the upper chamber is needed to ensure the module components are properly pressed and adhered to each other with EVA.

For c-Si modules, the typical process requires (1) stacking of glass, first EVA layer cut to the size, solar cell strings, second EVA layer, and finally backfoil film cut to the size, (2) slit an opening through the second EVA layer and backfoil film, (3) slide the electrodes through the slit opening and tape down, (4) lay up the module stack on the laminator, (5) initiate the lamination T-P-t process, and finally (6) remove the laminated modules and cut off with a knife the extra backfoil and squeezed-out EVA around the module edges. (For thin film modules, only one layer of EVA is needed.) The above process is very labor intensive and is a production bottleneck within the entire cell-to-module fabrication process. Partial automation for feed-in and move-out large-size modules is available. However, total automation to complete all six steps is still not readily available. Spire has been working in past several years to develop such equipment. However, the very high capital cost requirement for such total automation can be a critical concern. In China where labor costs are still relatively cheap, several large PV module manufacturers perform all the tasks manually from cell-tab ribbon soldering to cells-string soldering, EVA and TPT cutting, module component stacking, lay-up and removal of laminated module, edge cleaning, and silicone edge sealant application, and Al framing. The expensive, automatic cell-tab ribbon soldering and stringing equipment has been idled aside (or not even considered for use) because of cell breaking rate by the tabbing machine was higher than manual tabbing.

The actual lamination process and T-P-t profile in work usually vary from one manufacturer to another, even the same fast-cure EVA formulation is being used. The actual T-P-t profile is also dependent on encapsulant materials and formulation. For example, two versions of EVA formulations are available – fast-cure and slow (or standard)-cure. The main difference is in the curing agents used for cross-linking reactions. The EVA encapsulation process in a double-bag vacuum laminator basically consists of two parts: lamination of the components by melting the EVA under vacuum at lower temperature (e.g., 100-120^{o}C) and curing of the EVA at higher temperature (135-150^{o}C). The two parts can be carried out sequentially by a “One-step, Two-Temperature” method in a programmable laminator with fast heating ramp-up, or by a “One-Step, One-Temperature” method when oil-heating, large laminators with slow heating ramp-up. In practice, many PV manufacturers have elected to use a “Two-step, Two-Temperature” method by performing lamination in vacuum laminator and then curing in a heated oven in the air, even the EVA is the fast-cure. The “Two-step, Two-Temperature” approach is believed to increase the production because a large number of laminated modules can be oven-heated in one batch. A potential issue with this approach is the photodiscoloration of EVA, as we had demonstrated that EVA cured in the air tend to yellow earlier and greater than the EVA that was laminated and cured all in vacuum [16].

Non-vacuum Roll-Press Method: Because of its bottleneck nature with the use of EVA and vacuum laminator in the entire module fabrication process, a recent effort is being invested in

the use of TPU and a roll-press method to avoid needing the vacuum. This approach was demonstrated by Stollwerck et al. using a roll press equipment for both c-Si and thin film modules [17]. In our lab, we also studied this method several years ago by two directions: the first was to develop a new EVA formulation that can be laminated and cured at lower temperatures (e.g., ≤ 130^{o}C) [18], and the second is to use a lab-press with heating platens to conduct the lamination/curing in the air. The results were successful on making small-size glass/EVA/c-Si cell/EVA/glass laminates without having trapped air bubbles. But in the absence of a large press or a roll-press equipment, we could not conduct experiments to confirm whether our press approach using the low-T fast-cure EVA is practically feasible on large-size modules.

Others: A much less used module encapsulation process is the double-pane glass/glass modules that used liquid UV-curable resin. The resin is first sucked from below by vacuum into the modules to fill the gap between the two glass plates, and then is cured by brief exposure to UV light from both sides of the glass plates. The advantage of this process is the very short time required for UV curing. Whether this approach is still being used at the present is not clear. Another encapsulation method is the no-pottant encapsulation developed by Apollon Solar of France for their "NICE" modules. In the NOCE modules, the c-Si solar cell strings are secured by using adhesive strips and further by bended tab ribbons in touch with top glass plate [5].

Reliability

The long-term performance durability and reliability of PV modules is affected by many factors that have already been "embedded" during encapsulation process. Simply put, they are related to the quality of the encapsulation materials and the quality of encapsulation process. Upon deployment in the field, whether on the racks on the ground or rooftop mounted, a PV module will subject to the environmental factors as depicted in Fig. 6. The key degrading elements include UV light, oxygen, water moisture, and heat from sunlight, air, rains/snows/hails, and temperature fluctuations during diurnal and seasonal changes. These elements can potentially degrade optical, electrical, and/or mechanical properties on a module.

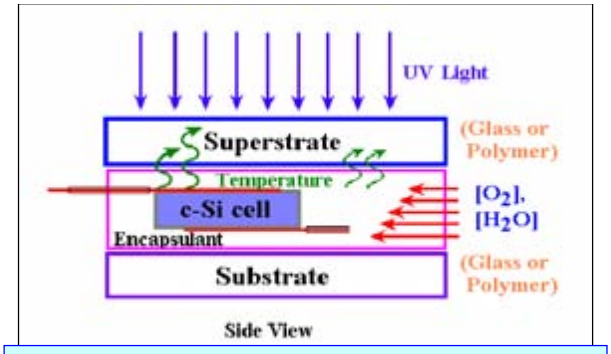


Fig. 6. Schematic illustration of potential degrading factors and their pathways into a module laminate caused by daily and seasonal climatic changes as well as environments.

In the course of IEC or UL qualification tests (QT), detrimental effects of some of the "embedded" factors may or may not be amplified to a level where modules are rated failed to pass the tests. By using accelerated weathering tests (AWT), greater amplification of these factors resulting in definite failures can be revealed in a shorter time. In general, within predefined test conditions and test duration, QTs may be sufficient to expose and identify the quality problems related to electrical properties such as breaking of tab ribbon interconnections in thermal cycling and current leaking in the damp heat test, and mechanical properties such as delamination of encapsulant from glass or cells in humidity freeze cycle and/or damp heat test. However, current QTs are inadequate to determine the optical properties such as long-term photothermal stability of encapsulant, i.e., UV-induced yellow-browning. In the following, we will discuss only two major degradations through AWT: photodiscoloration of the encapsulant

caused by prolonged UV exposure, and loss of adhesion strength (delamination) of encapsulant and corrosion of metallic components caused by moisture ingress and retention.

Other than the electrical factors, the power output of a module is proportional to the optical transparency of the encapsulant. For EVA, yellow-browning (see Fig. 3) can reduce sunlight transmitting through for solar cells to produce photocurrent. Using a FSSS with a 1-KW Xe lamp producing an average of ~6 UV suns in the 300-400 nm range, the net changes in yellowness index for several EVA products over 1200 h exposure at a BPT ~80^{o}C are compared, as shown in Fig. 4. Although all of EVA samples are fast-cure, difference in individual formulation was responsible for the variation in the photothermal stability. Accordingly, it is advisable to choose a low-yellowing EVA product to ensure a stable photocurrent output over the module lifetime. In similar FSSS tests and/or in Ci4000 weatherometer exposure, NREL-developed EVA and PMG, PVB, and TPU are relatively stable, producing low level of YI changes.

Moisture ingress is a major cause for most degradations, especially for the modules without moisture-blocking edge sealant. The moisture can permeate through the module edges, encapsulant, and backfoil. (See the WVTR data in Table 2). In an earlier study using the Ci4000 weatherometer with a light-dark cycle with periodic front water spray [19], we found that (1) moisture ingress resulted in haziness of EVA, (2) moisture retention due to light-hot/dark-cool cycles resulted in condensation of water in specially designed laminates, (3) cracking of glass plates, (4) corrosion of tab ribbon and soldered region (see Fig. 7(left)), and (5) certain degrees of adhesion loss of EVA from glass plates. The corrosion was greatly accelerated on bare (intentionally not encapsuated) Si cells with tab ribbons after 1000-h exposure in damp heat chamber at 85^{o}C and 85%RH, as illustrated in Fig. 7(middle and right), showing the front and back side of a tested cell.

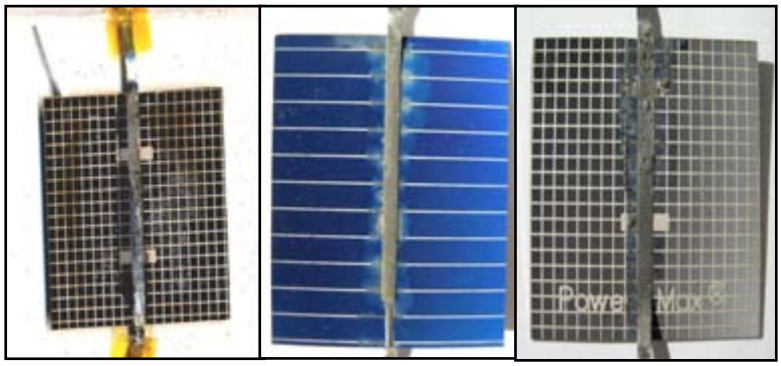


Fig. 7. Photographs showing an glass/EVA/c-Si cell/EVA/ glass laminate with cracked top plate and corroded tab ribbon after exposing in Ci4000 weatherometer (left), and corroded tab ribbons, AR coating, Ag gridlines on the front and back sides of a bare c-Si cell exposed in damp heat chamber for 1000 h (middle and right).

Damp heat exposure can also reduce the adhesion strength of EVA to the glass surface as demonstrated in Fig. 8. Just like photodiscoloration (Fig. 4) discussed above, the peel strength loss also depends on the EVA formulations. However, it should be noted that the adhesion of EVA to glass is mostly realized by the presence of adhesion promoting silane in the EVA formulation. The -Si(OR)$_3$ on the silane and the silanol groups, -SiOH, on the glass surface form Si-O-Si bonding via condensation reaction, which can be reversed via hydrolysis reaction. Therefore, unless the EVA is physically separated from the glass surface, the adhesion of EVA-glass is reversible/recoverable. In the case of EVA physically separated from the glass surface, the original optical coupling will be lost and light scattering can cause some degree of current loss.

Because of the great damaging potential by moisture ingress at high temperatures, PV module performance reliability and durability can be much improved or enhanced by using backfoil and edge sealant with high moisture blocking properties (i.e., low WVTR). Another approach being

investigated in recent years is to apply a thin layer of moisture-blocking oxide barrier directly on thin film solar cells prior to encapsulation [20]. Extensive studies have been conducted in the testing of various packaging materials for improved PV module reliability by our group in the past years [21-23].

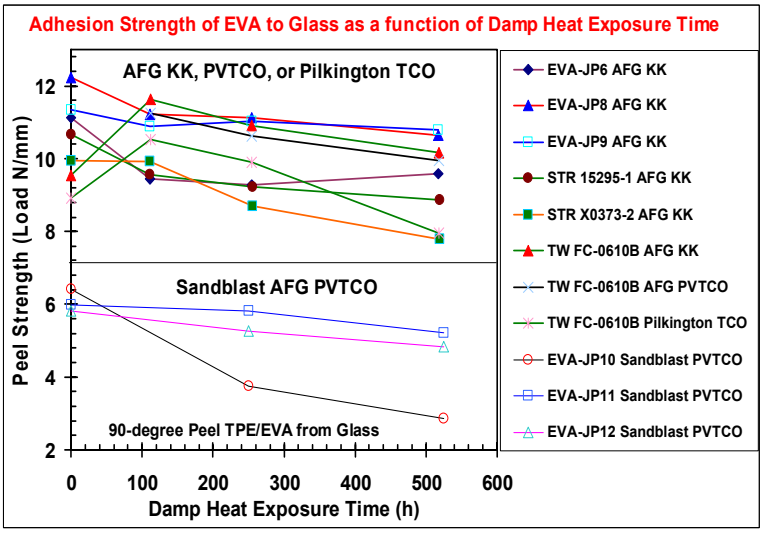


Fig. 8. Adhesion strength of various EVA on different glass substrates as TPE/EVA/glass laminates during damp heat exposure was affected by formulations. Adhesion of EVA on un-sanded glass surfaces (top portion) was generally greater than on sand-blasted AFG PVTCO glass (bottom three curves). NREL EVA formulated with Z-6032 primer (JP8, 9, 11 and 12) performed better than those (JP6 and10) with Z-6030.

Conclusion

The various types of encapsulation materials, encapsulation process, and their properties and potential effects on module performance reliability are discussed in this general overview. Although high-performance glass superstrates, encapsulants, backfoils, and edge sealants are available for module encapsulation, the present module constructions and encapsulation process appear to be largely influenced by practical considerations on the costs and production speed. However, the diversity and the differences of these materials, their properties, and the encapsulation process in module fabrications result in turn the variations in the module performance reliability and long-term durability.

Acknowledgements

The author thanks his colleagues Dr. A. W. Czanderna, Steve Glick, Gary Jorgensen, and Kent Terwilliger in National Center for Photovoltaics (NCPV) of NREL for various collaborative work or studies over the years on materials and module degradation analysis, AWT, damp heat and peel tests, and WVTR measurements. The variety of polymer resins and films (EVA, PMG, PVB, and TPU), chemicals and silanes used in formulations, glasses, and backfoils were kindly provided by a number of difference sources or companies in the world. Supports from Division and Center managements are greatly appreciated. This work was performed at the NCPV of NREL under DOE contract DE-AC36-99-GO10337.

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MODULE MUSINGS – PRESENT AND FUTURE

Jack Hanoka
Evergreen Solar, Marlboro, MA 01752
hanoka@evergreensolar.com

ABSTRACT - As part of an overall effort to lower the costs of module materials, work at Evergreen Solar on a possible future module design and alternative encapsulant materials are described.

EVA and other encapsulants – EVA is used by a vast majority of the PV crystalline silicon industry. One of the main vendors, STR, has steadily improved it over the years. At Evergreen another encapsulant material that does not require vacuum lamination was developed, patented and then tested extensively under mirror enhanced sunlight in Arizona. This encapsulant was a kind of sandwich structure, with thin outer layers of Ionomer or an acid co-polymer of polyethylene and an inner layer of metallocene polyethylene. A patented U. V. stabilization package was developed for this material and it proved to offer far better U. V. protection than the standard one used for EVA at that time. The EVA used at the time was STR TBEC (about 9 years ago). Figure 1 shows the comparative results where 4 samples laminated between two pieces of glass of EVA and 4 of Evergreen's encapsulant were exposed to mirror enhanced sunlight at a test facility in Arizona. In the figure the degree of yellowing (the Yellowness Index, YI) is plotted vs. time in months. The mirror enhancement is on the order of 5 to 7x ordinary sunlight.

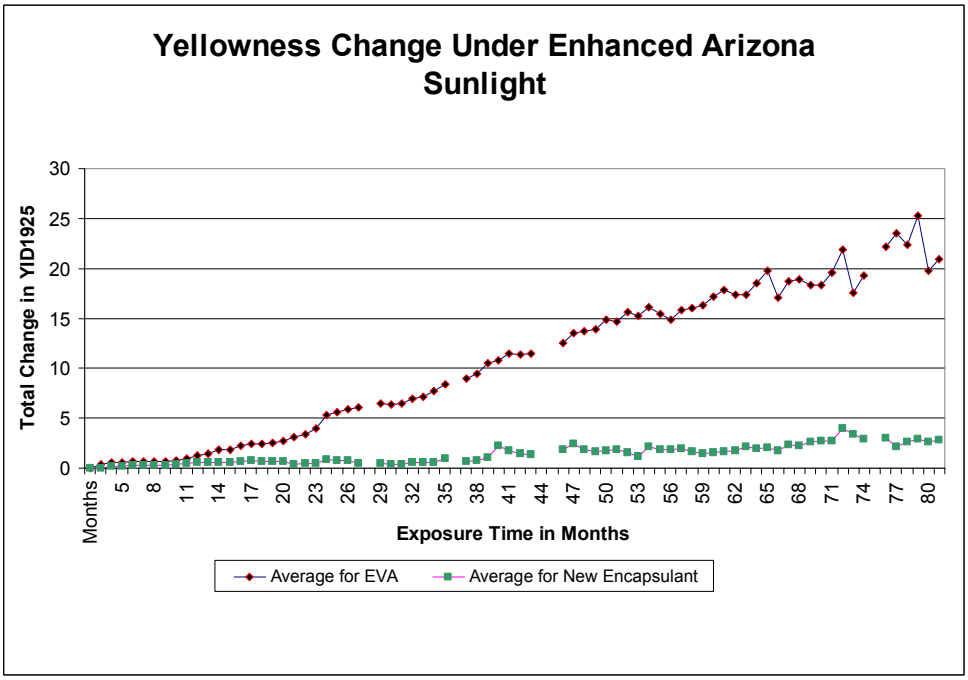

Figure 1 – YI for EVA and Evergreen encapsulant.

It can be seen that the combination of this new encapsulant and our patented U.V. stabilization package resulted in substantially better U.V. stability than the EVA at that time.

Future module design - There is much interest today in rear contact cells. Work on wrap-around contact cells and a module design that incorporates them was started some time ago at Evergreen. In such a configuration, no wires are used to interconnect the cells, instead a set up as shown in Figure 2 is used.

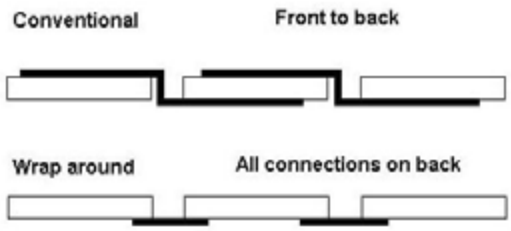

Figure 2 – Configuration for wrap-around contacts.

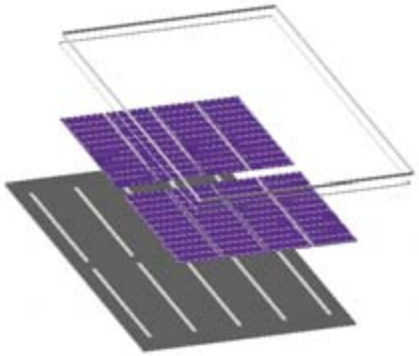

Figure 3 – Set up using wrap-around cells,

This configuration requires that a backskin material be employed that allows for conductive adhesive bars to be printed onto it and that these bars and the rest of the backskin bond directly to the back of the cells, without any encapsulant layer behind the cells. The proprietary backskin material developed at Evergreen bonds directly to the back of the cells and so satisfies this. The configuration would be constituted as shown in Figure 3. The top layer is glass, below it is the transparent encapsulant layer, below that are the String Ribbon cells with wrap-around contacts, and below the cells is the backskin with the conductive adhesive bars printed on it. Small, 25W size modules were made this way using 8 cm x 15 cm String Ribbon cells that were cut in half. These modules were made as in the set up shown in Figure 3. One of the key issues in making such a module is that of the electrical and mechanical integrity of the conductive adhesive. Extensive thermal cycling is widely used as a criterion for this. Figure 4 shows the power change after thermal cycling for a number of these modules. Note that even after some 1600 thermal cycles, generally no significant power drop was seen for these modules. (the module tester at that time was, at best +/- 2%.)

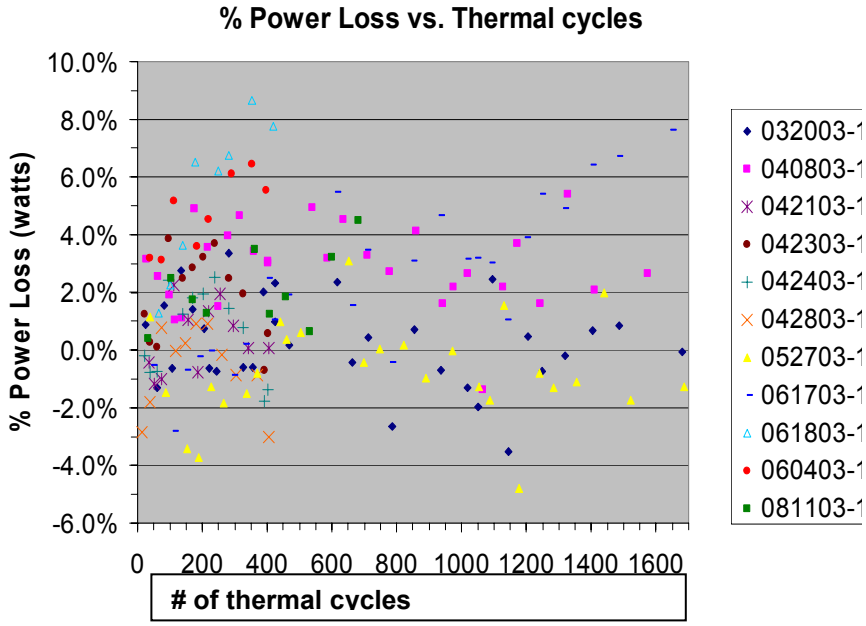

Figure 4 – Thermal cycling of modules made as per figure 3.

Crack Detection in Photovoltaic Quality Control

P.S.Raghavan, Yuepeng Wan and Chandra P.Khattak
GT Solar Technologies, A division of GT Equipment Technologies, Inc.,
243 Daniel Webster Highway, Merrimack, NH-03054

Abstract

Defects in crystalline silicon wafers range from cracks, edge chipping etc. to voids and inclusions. Cracks (micro or macro) are induced in silicon wafers/solar cells by thermo-elastic stresses during the post growth, cutting, heat treatment, and soldering processes. In the ingots or bricks, cracks are induced due to thermal disturbances, stress, etc. Likewise inclusions or voids are also seen due to the silicon carbide particles or gas entrapment during the growth. Manual methods of defect detection by visual inspection, optical or microscopical methods on silicon wafers are tedious, time consuming and prone to errors. A non contact, high speed and inexpensive technique is the need of the day in the photovoltaic industry quality control to reduce the cost of manufacturing operation at various stages, such as, after sectioning of ingots into bricks, after wafer cleaning, after solar cell testing, before and after tabber and stringer. We have developed a non-contact infrared (IR) imaging system for speedy detection of cracks, voids, inclusions and microcrystalline structure in bricks and in wafers. This paper briefly reviews the various crack detection systems.

1. Pre-amble:

Though there are crack detection techniques, based on electrical conductivity probing, eddy current, ultrasound, laser scanning, high resolution grey scale imaging, etc., these systems are not fast enough to allow integration in a modern production line with throughput rates of 2000 wafers/hour.

In the ultrasonic crack detection technique [1], ultrasonic vibrations are coupled to the wafer from the piezoelectric transducer. An air-coupled ultrasonic probe captures the standing wave generated in the wafer and maps the acoustic image of the vibrating wafer. Researchers have also attempted the combination of ultrasonic and IR imaging to detect cracks. The ultrasonic vibrations induced to the silicon wafer results in localized heating in the area around the cracks due to friction between the cracked regions and the IR image reveals the nature of cracks.

The use of single and multiple laser and photodiode combinations through which the wafers are scanned are also reported for crack detection. The main drawback is the slow speed of operation which prevents it from being incorporated as an in-line tool.

Near infrared (NIR) Imaging Cameras provide a novel tool for non-destructive detection of cracks in multicrystalline silicon wafers. The combination of digital signal processing and interrupted thermal conductivity [2-4] gives quantitative data on cracks, including crack dimensions, number of cracks, etc. in a silicon wafer. The transmission mode infrared imaging technique on bricks or ingots provides valuable information on cracks, inclusions, voids, microcrystallinity and dopant level.

2. Crack Detection Systems

2.1 IR Brick Imaging System:

The IR Brick Imaging System is an inspection tool to evaluate defects formed during the growth of multicrystalline silicon ingots by directional solidification or single crystals using Czochralski process. Defects vary in form and location within the silicon ingots. From the transmission spectrum in Fig.1, it can be seen that Silicon is opaque in the visible region and is transparent in the infrared region (from 0.8 –5.5 microns), i.e., the IR radiation just passes through the silicon. If there are defects present in the silicon the incident IR radiation is absorbed or scattered/diffracted by the defect centers, thereby changing the intensities in the images, as observed by an IR imaging camera. The yellow marker indicates the range of the camera sensitivity region.

Fig. 2 shows the GT-BIS-0100, Infrared Brick imaging system. The system comprises a light source, ingot/brick handling table, an IR videcon camera fixed with filters and lens system to capture the image of the full brick, video capture board, display monitor and computer with image processing software. The ingot/brick handling table can accommodate square or round ingots and facilitates easy rotation of the table, so that the image can be captured from all the faces of the ingot/brick.

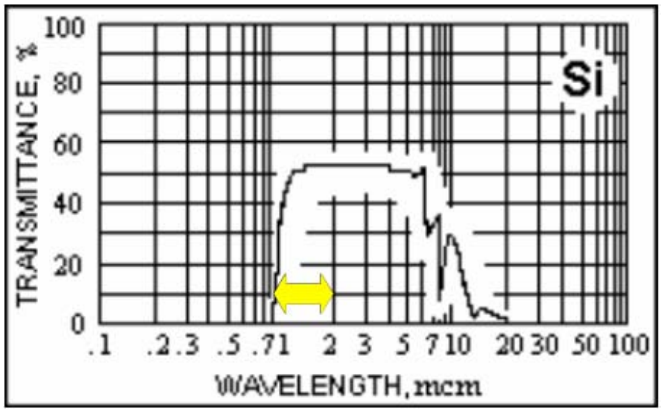

Fig. 1: Optical transmission spectrum of silicon

Fig. 3 shows the IR transmission images obtained on the mullticrystalline silicon bricks. Fig 3a shows the image obtained from brick with microcrystalline structure. The small grains present in the brick scatter the light thereby producing a shadow in the image. Fig. 3 b shows the IR image with SiC inclusions in the top of the brick. Fig. 3 c shows the cracks in the bricks. Fig. 3 d shows the image produced by a low resistivity (higher impurity concentration). Fig 3 e shows the IR transmission image of a flawless brick.

Fig. 2: GT-BIS-0100 for silicon ingot inspection.

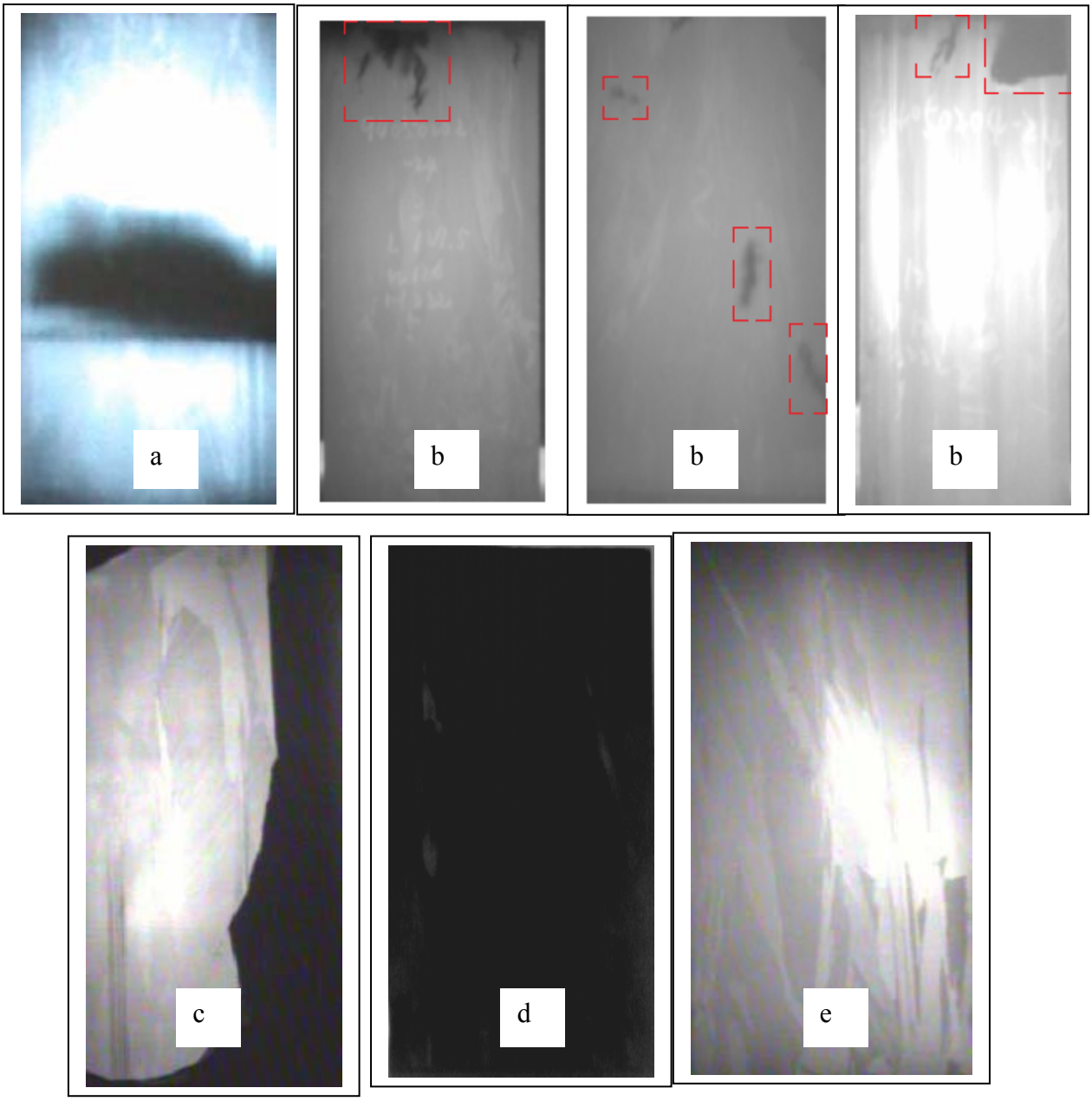

Fig 3: a) 156 x 156 x 245 mm brick with microcrystals; b.) Bricks with SiC inclusions; c) Brick with a crack; d) Brick with low resistivity; e) A flawless brick

2 2. Wafer Crack Detection System.

Fig 4 schematically depicts the wafer inspection station for cracks. The source of radiation is a large-area black body relatively at a high temperature. The radiation detector is a near infrared radiometer (Focal planar array). The digital image processing board provides a serial interface and four RS-422 control lines for the camera. The board is installed into a computer, captures as many as 16 bits of data at a clock speed of 40 MHz, and delivers a total acquisition rate of 80 Mbytes/sec. An on-board 16-Mbyte memory accommodates on-board buffering, which captures large images and sustains real-time throughput. The digital signal processing board in the vision

system drives and receives data from the camera using the EIA-644 or low-voltage differential signaling protocol. This protocol is similar to RS-422, but works at lower voltage levels. The wafer carrier is based on a walking beam concept with the stacker moving up or down to receive the wafers. There are duplicate bin locations to enable continuous operation even when one set of bins is empty of wafers. Fig. 5 shows some of the cracks detected in wafers.

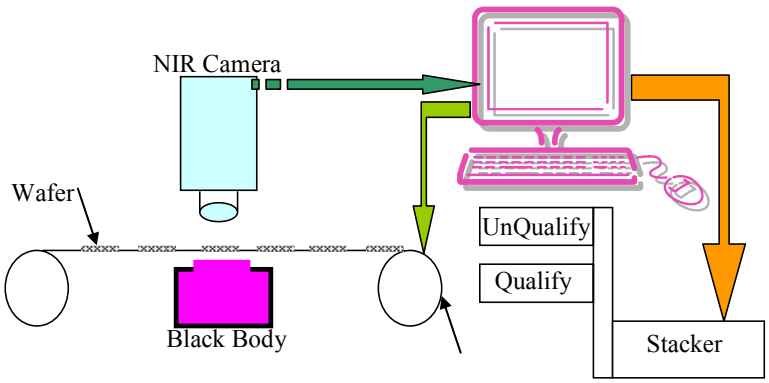

Fig. 4: Conceptual design of a wafer inspection station based on the IR transmission technique.

3. Conclusions

GT Equipment Technologies, Inc. (GTi) has developed a crack detection technique based on IR transmission through silicon. This technique has been implemented in its brick inspection product. It is also being developed for GT's turnkey lines (wafer, cell and module line) to weed out cracked wafers. The technique is based on snap shot method that is compatible with high throughput processing environment of multicrystalline silicon wafer lines. The brick image system reduces costs and saves man hours by preventing bricks with cracks, inclusions (which cause wire breakage and damage to wire guides) and microcrystalline regions from proceeding into wiresaw operations.

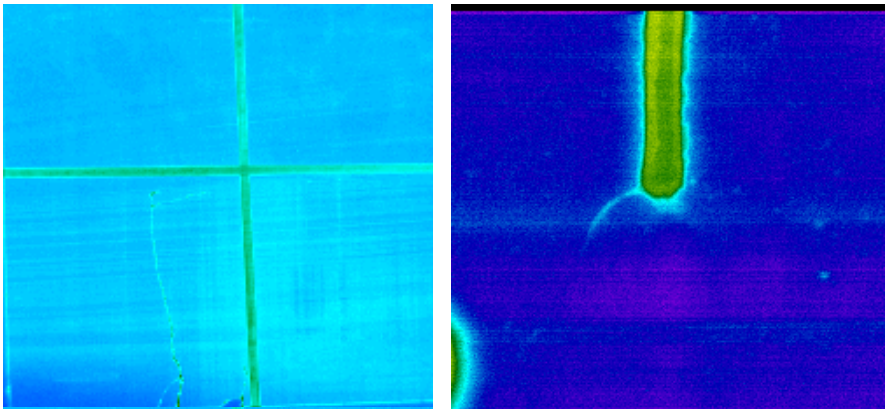

Fig. 5: a) Centimeter size crack in a wafer, b) micro-meter size crack after laser cutting. Pictures taken by IR cameras.

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5. Acknowledgement

Thanks to RWE-Schott and Dr. Juris Kalejs for their support on part of the research work.

Wafer Breakage Mechanism(s) and a Method for Screening "Problem Wafers"

Bhushan Sopori, Pete Sheldon, and P. Rupnowski

National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401

INTRODUCTION

One of the strategies for lowering the cost of silicon-based photovoltaic (PV) energy is to use thinner wafers for solar cell fabrication. Reducing the wafer thickness offers a two-fold advantage: it reduces the wafer cost, and it can lead to an increase in the solar cell efficiency, provided appropriate cell design and processing techniques are employed. Although the concept of reducing wafer thickness is quite straightforward, it is difficult to implement in manufacturing. The experience in industry is that even for the current wafers (nominal thickness ~250 μm), the breakage during solar cell fabrication is already quite high. The estimated fraction of wafers that break during cell fabrication and module encapsulation ranges between 5% and 10%. A reduction in the wafer thickness has been found to further decrease the yield to unacceptable values. Because the yield loss due to wafer breakage has a tremendous influence on the solar cell economy, it is important to maximize the wafer yield at every step of cell fabrication. In particular, because the loss in revenue associated with wafer breakage increases as cell fabrication progresses, it is desirable to exclude those wafers that may break during cell processing from entering the fabrication lines. Thus, there is a great deal of interest to identify the sources of wafer breakage and to develop methods for detecting and separating wafers that are susceptible to breakage, preferably at early stages of solar cell fabrication.

Wafer breakage is not a major issue in the semiconductor industry, which has developed certain criteria for wafer preparation and procedures for device fabrication to minimize wafer breakage. The PV industry in not able to incorporate these preventive measures because of the high cost associated with them. Thus, the excessive breakage of wafers in the PV industry is primarily the result of inadequate wafer preparation, inexpensive wafer handling, and low-cost device processing methods— all aimed at minimizing the solar cell cost.

WAFER BREAKAGE: GENERAL ISSUES

A semiconductor wafer breaks if it experiences a tensile stress exceeding the critical stress. A semiconductor wafer experiences mechanical stresses from a variety of sources during device fabrication. These include:

- Wafer handling, such as mechanical handling during wafer transport
- Structure of the device, for example, asymmetry in the device configuration due to deposition of dielectric and/or metallic thin films, which can cause wafer loading
- Device processing, which can induce stress during thermal treatments or rapid thermal processing.

The intrinsic critical stress for most solid materials is quite high, $\sim 10^6$ psi. A good mechanical/thermal design of a wafer, wafer transport, and fabrication process sequence strives to limit the wafer stresses well below the critical stress values. The semiconductor industry uses design criteria for wafer preparation/handling and processing to achieve these goals. Because the mechanism of wafer breakage is that of a fracture, much research was done in the early days of the semiconductor industry on wafer fracturing. Initial studies were carried out to evaluate stress produced by various thermal profiles in conventional furnaces. These studies determined that two parameters—wafer diameter and wafer thickness—are important from stress considerations. Thus, the semiconductor industry uses standardized wafer thicknesses for various wafer sizes.

Later studies—including those on metals and glasses—determined that, even for a suitably selected wafer (of appropriate diameter and thickness), stress levels close to the intrinsic value can only be reached for "well-prepared" wafers. Other wafers fracture at stress levels well below these values. This reduction in the wafer strength was related to the surface and edge characteristics of the wafer.

1. **Surface characteristics**

Surface characteristics important from the point of view of wafer breakage relate to shape, roughness, and surface damage. The shape of a semiconductor wafer is typically circular and planar for many reasons. For example, in considering device processing, the wafer surface must be planar and (in most cases) polished. Polishing also helps in mitigating the breakage. It has long been known that microcracks strongly control the mechanical strength of various commercial glasses. It was argued that crack-like defects act as stress raisers. Under uniaxial tensile loading of a material containing microcracks, the cracks begin to grow, causing failure at stresses much below the theoretical strength. Microcracks are typically generated in wafer-cutting processes such as sawing. In the semiconductor industry, cutting or sawing operations are followed by damage removal and polishing. The wafers are chemically etched to remove the damaged layer at the surface, typically 10–20 μm in thickness, and then polished on one side.

2. **Edge characteristics** (shape of the edges and the technique of edge preparation)

In some cases, the edge damage can be more harmful than the surface damage. The edge shape can also have a significant effect on the breakage. Edge shaping typically uses a grinding process to "round off" the edges to minimize wafer breakage.

The semiconductor industry takes great care in preparing and handling wafers to avoid breakage. They have developed standard procedures in wafer preparation that minimize the susceptibility of wafer breakage. Some of the wafer preparation techniques in the semiconductor industry are:

1. Large wafer thickness to support unintentional stresses
2. Edge grinding
3. Wafer polishing
4. Nearly isothermal processing.

Fortunately, these criteria for minimizing wafer breakage also match criteria for making high-quality devices with a high yield. For example, wafer polishing is also necessary to achieve devices of small dimensions.

WAFER BREAKAGE IN SOLAR CELL FABRICATION

Solar cell fabrication requires many process steps to convert an ingot of silicon into wafers and then process them into solar cells. Typically, these steps include sawing, etching, formation of an n/p junction, and deposition of metallic and/or dielectric layers (some patterned and others in a blanket form). While many process steps are performed at lower temperatures (<400°C), some of these processes, such as phosphorus diffusion and Al alloying, are performed at elevated temperatures where the temperature of the wafer itself can be nonuniform. Because cell processing is in many ways similar to the microelectronic device fabrication, the Si PV industry had initially attempted to adopt many rules observed in the semiconductor industry. However, with increased production and higher demands for solar cell cost reduction, the parallelism has significantly diminished. The need for cost reduction has led to evolution into technologies that leave wafers more fragile, leading to very significant breakage rates.

Although the exact science for increased breakage is not known, it can be related to some of the procedures that are used in the PV industry (as summarized below).

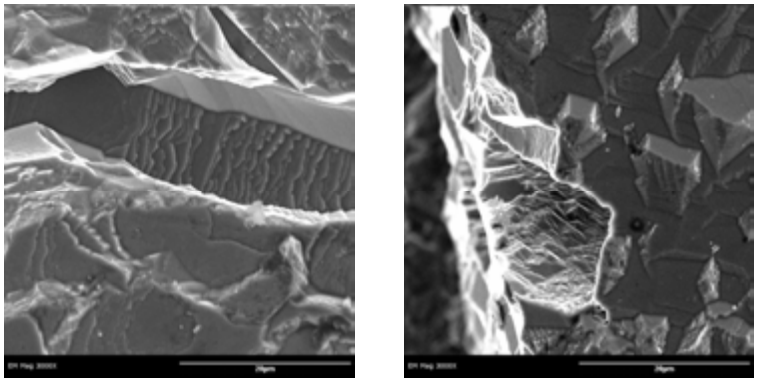
These solar cell fabrication steps can be mechanically very demanding on the strength of the wafer. The PV industry cannot expend the resources/expense to suitably prepare wafers to reach the intrinsic critical stress level. The critical stresses for PV wafers are considerably smaller; the measured value of critical stress depends on the history of the wafer. Reported values of tensile critical stress are ~10^3 psi (~10^8 dynes/cm^2).

It is believed that the dominant sources that reduce the critical stress below the intrinsic values and lead to early breakage are the microcracks. Microcracks are typically generated in wafer-cutting processes such as sawing and laser cutting. In most cases, cutting or sawing operations are followed by damage removal (etching away the damaged layer at the surface, typically 10–20 μm in thickness). In some cases, the microcracks may be deep enough that they are not removed by etching. The residual microcracks can be the sites where wafer cleavage initiates, which can result in wafer breakage. Saw damage exists at the wafer surfaces, as well as at the edges. In some cases, the edge damage can be more harmful than the surface damage. The edge shape can also have a significant effect on the breakage.

The major features of the PV industry that contribute to high breakage are:

- High throughput, which demands wafer transport transported via cassettes with high wafer transfer rates and/or use of conveyor belts, suction cups, and other robotic devices.
- Thin wafers–PV wafers are considerably thinner than those used in the semiconductor industry. For a given stress, the thinner wafers are more susceptible to breakage.
- Inadequate wafer preparation can change mechanical strength of a wafer. For example, sawing is a process of material removal by fracture (where little fragments of material are chipped away). Such a process produces damage that can propagate quite deeply below the surface into the material. Another process step that alters the mechanical properties of the wafer is texture etching. Although texture etching removes the saw damage (making it less likely to break), it exposes cleavage planes of the wafer, making them more likely to break in handling. Thus, cell processing itself can influence the state of stress in the wafer, which can change the propensity of the wafer to breakage.

- Little or no edge preparation (particularly important for ribbons)
- Residual stresses: The other major source of breakage is related to wafers having residual stress. This mechanism is particularly true for ribbon wafers. Whether it is microcracks or residual stress, the external impetus that results in breakage is a source of stress.
- Thick and unbalanced metallizations: In addition to the characteristics of the wafer, some of the solar cell design makes it prone to generation of mechanical stress in the device. For example, the metallization of solar cells occupies a large area of the device (typically 8% of the front and nearly 100% on the back side).
- Higher throughput also requires faster processing times, leading to non-isothermal processing.



(a) (b)

Figure 1. SEM images of a Si wafer after standard saw damage removal—wafer edge (a) and wafer surface (b).

Figure 1 shows scanning electron microscope (SEM) images of microcracks on the edge and the surface of a multicrystalline (mc)-Si wafer after saw damage removal. Because edge cutting is done by an inside-diameter (ID) saw, whereas the surface is cut by a wire saw, the edge cracks are typically larger than the surface cracks. Wafer breakage occurs as a result of external stress applied in a direction that causes one or more of the following:

1. An increase in residual stress beyond critical stress
2. The "opening up" of a microcrack.

Figures 2a and 2b illustrate the geometry and stress distribution, respectively, associated with a microcrack. The breaking strength in tension due to a microcrack of length c can be written as:

$$\sigma_c = (2\gamma E/ \pi c)^{1/2}$$

Here, γ is the specific surface energy of the material, and E is Young's modulus.
This expression can be approximated as:

$$\sigma_c \sim [E /20] \times (a /c)^{1/2}$$

Here, a is the atomic radius. Thus, it is seen that the larger the crack, the lower the strength of the wafer. From this equation, we can estimate the critical stress required for different crack sizes. We will use a "reasonable" value of $E = 1.17 \times 10^{12}$ dynes/cm^2 and a = 5.43 Å. Hence,

$\sigma_c \sim [1.17 \times 10^{12} /20] \times (10.9 \times 10^{-4})^{1/2}$ dynes/cm^2, or $\sigma_c \sim 3.5 \times 10^{10}$ dynes/cm^2, if the crack is 1 μm in length. For a crack 100 μm in length, the critical stress will be reduced by a factor of 10, to 3.5×10^9 dynes/cm^2.

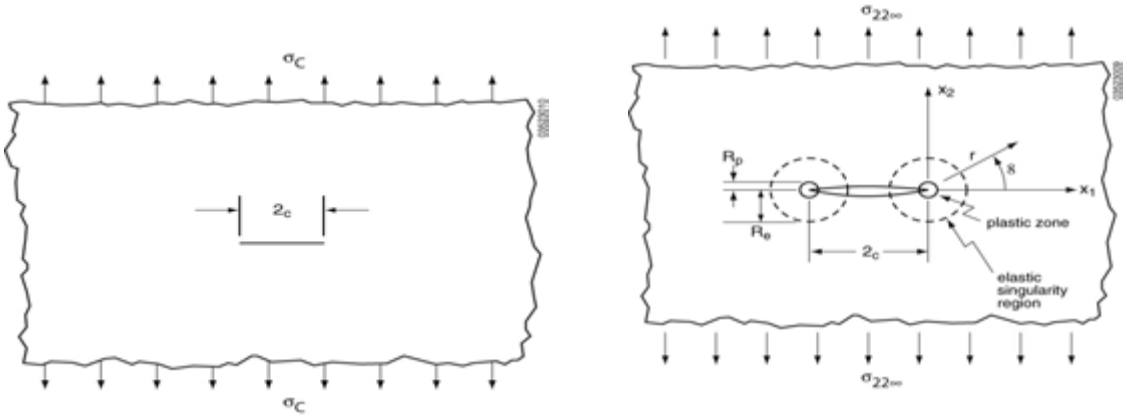


Figure 2. Illustration of a tensile critical stress normal to the crack.

CURRENT APPROACHES FOR STUDYING CRACKS

Although wafer breakage is a serious drawback in the PV industry, current techniques for prevention are not cost-effective. There is some hope that research into the formation and elimination of cracks will unlock some information that can help mitigate their influence on wafer breakage. Some techniques are being studied to directly "observe" cracks in solar cell wafers and devices.

IR imaging

Infrared (IR) imaging is used to determine precipitates and other defects in Si. Typically, IR imaging requires double-sided polished wafers through which an IR beam is passed and its local transmission observed. Like a precipitate, any discontinuity in a wafer will alter the IR transmission. Thus, a crack is expected to produce an increased transmission when a small beam illuminates the region in the vicinity of a crack. Unfortunately, PV wafers are not polished—they have rough or textured surfaces for good antireflection and light-trapping properties. However, it is likely that IR imaging may have some use in ribbon wafers because their surfaces are somewhat shiny (but they have thickness striations and global variations). Because ribbons are laser cut, this technique may have some application in identifying edge cracks in ribbons.

Microcracks can be anywhere in a single-crystal or cast mc-Si wafer. It is difficult to image cracks because they can be very small.

Thermal imaging

A crack produces a discontinuity in the thermal impedance of the wafer. Hence, if a wafer is heated, there will be a temperature discontinuity at the crack size.

A major problem in imaging a crack is that microcracks are typically small. Thus, it is difficult to select wafers based on the detection of microcracks. Although imaging cracks and microcracks may be useful in studying their origin and other behavior, it is not easy to relate the presence of microcracks to wafer breakage. For example, wafers with microcracks can easily survive certain processes that are "gentle" (produce very little stress) or if they can be handled in suitable ways. Hence, a more appropriate approach to deal with the problem of cracks in substrates is to determine if a wafer (produced under given processing conditions) is likely to break during a set of processing and handling conditions. Thus, it is generally sufficient to determine if the presence of cracks will lead to a failure of the wafer during cell fabrication. To date, it seems reasonable to identify wafers that are likely to break during solar cell processing and to remove them.

ISOLATING "PROBLEM WAFERS": PROPOSED METHOD

Clearly, one way to determine if a wafer will break in a given process sequence is to simulate the stresses/stress-distributions (or the most stringent distribution) that the wafer will experience during that process. This is not a new concept because the standard method to determine critical stress is to apply a local tensile stress to a wafer until it fractures. A well-known approach consists of three-point loading wherein the applied stress is increased until the wafer breaks. In a typical application, three-point loading is applied on a local region. This approach is good for double-sided polished wafers free from surface defects. When defects are present, the measured critical stress may depend on whether the measurement region contains surface defects. In this case, a reasonable approach is to apply stress to the entire wafer. However, a mechanical means of applying stress to the whole wafer is not convenient (for example, wafers may not have the same thickness, or each wafer may not be uniform in thickness). It requires an elaborate means of holding the wafer and a means of applying the stress. In particular, it is difficult to control the mechanical stress if the wafer is warped or does not have uniform thickness.

We have developed a novel method for testing the propensity of a wafer to break in typical solar cell processing that overcomes the difficulties of applying mechanical stress. This technique is a noncontact method. The basic principle of this approach is to apply suitable stresses to a wafer with predetermined configurations representative of solar cell processing/handling conditions. If the wafer breaks during this testing, the wafer is automatically pulled out of the processing line to save further processing costs. Another objective of this method is to select wafers for further analyses that can identify reasons for wafer breakage.

The proposed method is to create a stress distribution in the wafer by imposing a thermal profile through an optical excitation. The process consists of heating a wafer in a nonuniform manner to generate predetermined stresses. Figure 3 illustrates the generation of thermal stress due to laterally uniform illumination. Instead of using mechanical stress (such as bending) to introduce tensile stress, we propose using thermal stress introduced by optical heating. Figure 3 illustrates a simple means of creating stress in the wafer. The wafer is partially illuminated with absorbing light (such as that from a tungsten-halogen lamp or a bank of lamps). Typical light intensity is in the range of 4–8 W/cm^2, which can produce a local wafer temperature in the range of 400°–1000°C. Because of the partial illumination, the wafer will acquire a temperature distribution, as illustrated (qualitatively) in Fig. 3. This temperature distribution will, in turn, lead to stresses.

Qualitatively, one can see that the illumination of Fig. 3 will generate a tensile stress in the illuminated region of the wafer and compressive stress in non-illuminated regions. The amplitude of the stress depends on the light-intensity distribution (based on some simple assumptions), which dictates the temperature distribution. The stress developed in the wafer is a

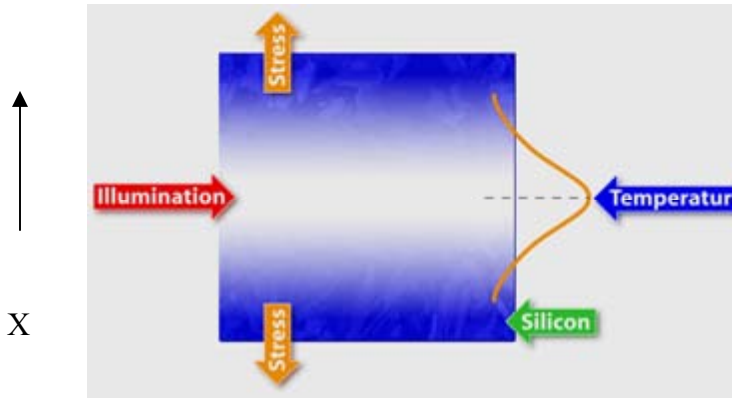


Figure 3. Illustration of a temperature gradient produced by optical illumination of a Gaussian profile along X-direction.

function of non-linearity in the temperature gradient, as well as the maximum temperature. The temperature distribution itself (of the wafer) is determined by the incident flux distribution and the convection flow. Here, we will show that the temperature range required to produce desirable levels of stress are quite reasonable, and the equipment needed to induce such stress levels can be quite simple and inexpensive.

The practical implementation of the above principles may easily be performed in a system consisting of a light source and a conveyor belt arrangement, as shown in Fig. 4, which shows a schematic of a simple setup for isolating wafers likely to break during solar cell processing. The wafers are sequentially placed on a belt, which preferably supports the wafers at the edges. They are conveyed into a region that has a narrow illuminated zone. As the wafers pass under this illumination, each wafer acquires a temperature distribution that depends on the intensity pattern of the light, size of the wafer, and belt speed. This results in a predetermined thermal stress.

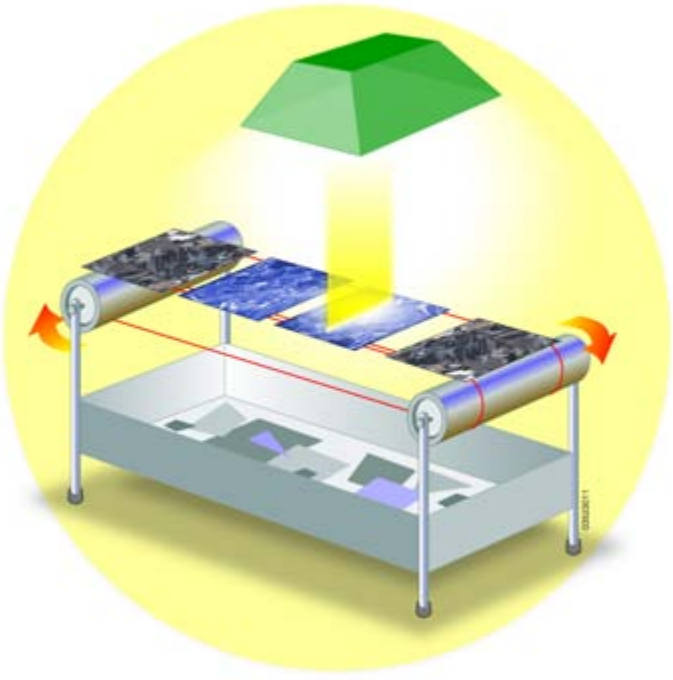


Figure 4. A schematic of a simple setup for isolating wafers likely to break during solar cell processing.

As a result of nonuniform heating, a stress distribution is induced in the wafer. The illumination pattern is chosen to simulate the stress levels commensurate with the process conditions (for a given solar cell sequence). The illumination pattern for a given belt speed may be calculated using theoretical analysis. Such a calculation involves: (i) determining the temperature profile of the wafer for a given illumination pattern, and (ii) using this temperature profile to calculate the dynamic stress distribution in the wafer.

The illuminated zone may be established using light sources such as tungsten-halogen lights with suitable reflectors and masks. Any suitable light source that provides the desired illumination may be employed. The illumination distribution is typically adjusted such that the induced stress levels are below the critical stress values for wafers that have small or no microcracks, and above the critical level for "large" microcracks. In the illumination zone, the wafers may be convection cooled to tweak the temperature nonuniformities needed to acquire stresses of the magnitude identified in this disclosure. Such convection cooling may be performed by the flow of gases directed by suitable nozzles. The power controller that energized the light source may control the exact level of stress. Thus, wafers with cracks that may be fatal for a solar cell process will break during their travel through the illuminated zone. The broken wafers are likely to lose the support from the belt and fall into a collector below, or may be mechanically removed when they exit the machine.

OPTICALLY INDUCED THERMAL STRESS COMPUTATIONS

When a wafer is illuminated, the optical absorption causes the wafer to heat, creating a temperature distribution that depends on the spatial distribution of the optical flux distribution, its spectrum, and the material properties. Nonuniformities in the temperature gradient lead to the generation of mechanical stress. Hence, the stress levels generated in a wafer in an optical furnace depend on optical, thermal, and mechanical properties of the wafer itself and the illumination system. As a result of the illumination, desired temperature distributions can be generated in a wafer in a controllable fashion. The temperature can be a highly nonuniform function of position and time and will determine the magnitude of thermal stress in the wafer.

The relation between the temperature distribution and thermal stresses in a plane, unconstrained wafer is governed by a well-known partial differential inhomogeneous biharmonic equation. Based on this formula, the solution for stresses can be computed numerically for any given wafer shape and any temperature distribution. One general characteristic of the solution of the biharmonic equations, which was already mentioned, is that the highest stresses are usually generated in the regions where the temperature becomes highly non-linear. Consequently, the stresses in the wafer can be set to a desired level by increasing the curvature (second derivative with respect to position) of a temperature profile.

To illustrate the concept of stressing a wafer by means of optical illumination, we will briefly discuss thermomechanical simulations on a square silicon wafer subjected to a given temperature distribution. The temperature was assumed to vary along the x direction, while it was kept constant along the y direction. Three different Gaussian-like temperature profiles, shown in Fig. 5, were analyzed. The temperature peaks in the figure have different heights (400° and 800°C) and various widths, and can easily be generated using a proper illumination. The resultant maps

of stress components (σ_X, σ_Y, σ_{XY}) are shown in Figs. 6 and 7. Due to symmetry, only one quadrant of a wafer is presented in the figures.

Several general observations can be made based on the resultant stress maps in Figs. 6 and 7. We found that the three stress components are nonzero over the majority of the wafer area. Only the corner of the wafer remains free of stress, as should be expected for a mechanically unconstrained system. The highest stress is a tensile stress along the x direction, and its magnitude depends strongly on the chosen temperature profile. As one would expect, the narrow temperature profile with a 800°C peak, generated the highest value σ_X = 252 MPa. It can also be noted that both tension and compression stresses along the x and y directions are present at various locations in the wafer. One can also note that even at the 400°C peak temperature distribution, the stresses can exceed the nominal critical stress.

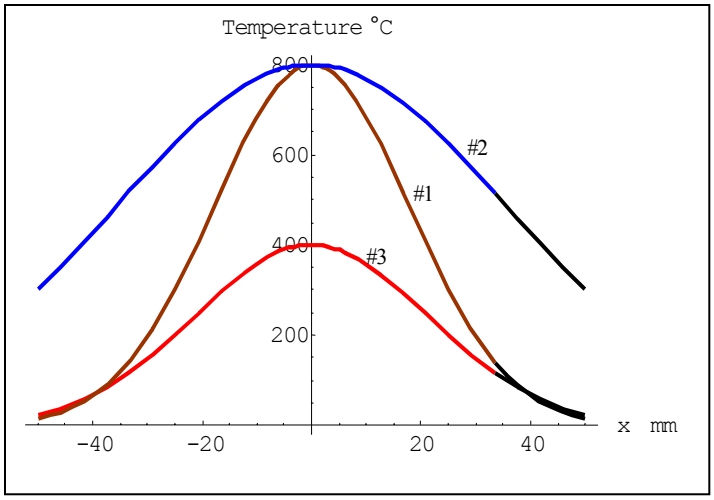


Figure 5. Three temperature profiles used in thermomechanical simulations.

From the point of view of crack detection, the simulation results obtained are very promising. They show that high magnitude tensile stresses can be easily produced in a wafer by proper illumination. The highest temperature on the wafer can be quite low. This is very significant because the required temperature distributions can be obtained with reasonably low power and at high speeds. It is important that the wafer is subjected to the load along both x and y directions over the majority of the area. This guarantees that microcracks of various orientations and location can be activated by the thermal stress. The other advantage of optical illumination is that the stresses are usually constant through the thickness of the wafer. Consequently, both the surface and deep micro-cracks can cause the wafer to break during the screening process.

We built a test machine and performed a variety of experiments on samples that went through different solar cell processing steps. Some of the general results are the following:

1. Wafers without adequate saw-damage removal have a higher propensity for breakage.
2. In most cases, wafer breakage initiates from the edges.
3. Thinner wafers break easier than thicker ones of the same surface and edge quality.

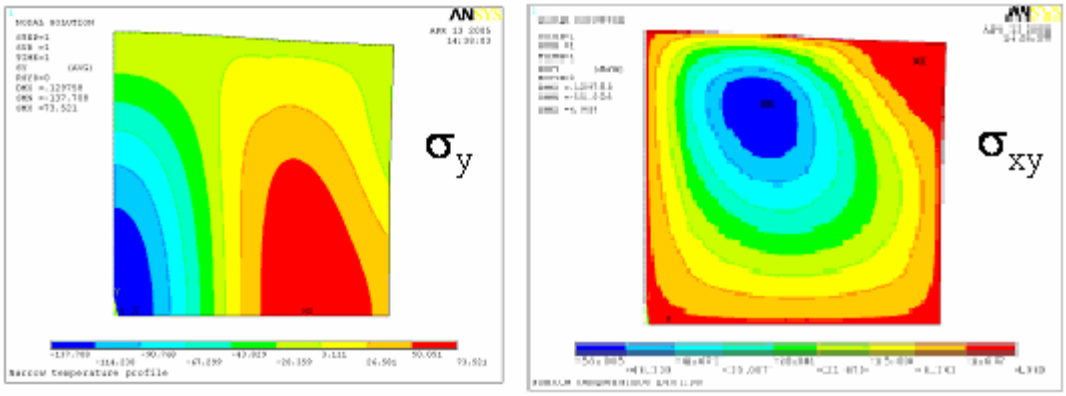


Figure 6. Stresses σ_Y and σ_{XY} for temperature profile #1. Note that only the upper right quadrant of the wafer is shown in the figure.

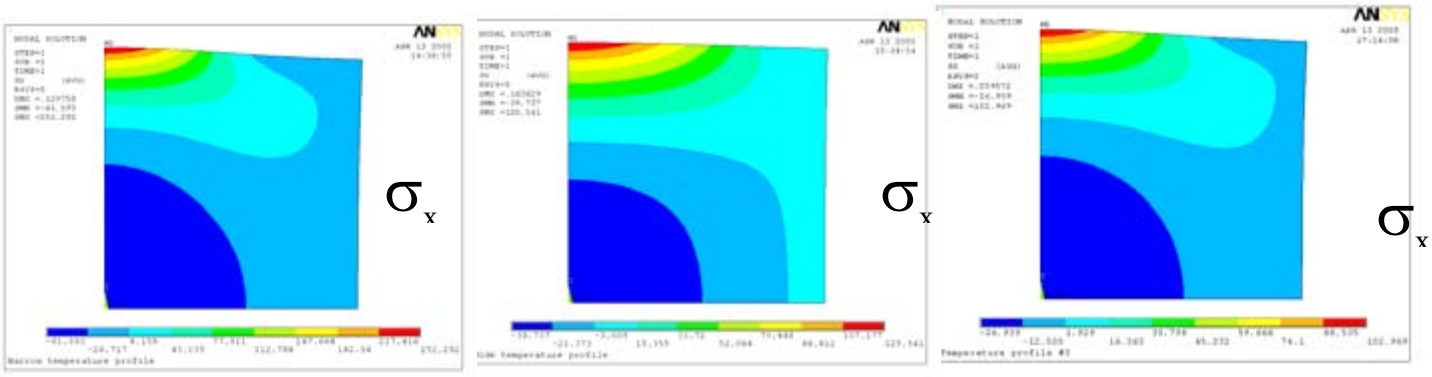


Figure 7. Stress σ_X maps in a wafer for temperature profiles #1, #2, and #3.

CONCLUSIONS

In this paper, we presented a review of mechanisms of wafer breakage in solar cell industry. We also described a new method for screening "problem wafers" that is based on optical generation of thermal stress, which causes weak wafers to crack during screening. Only the wafers that survive this thermomechanical test are allowed to proceed through further solar cell processing.

The advantages of the proposed method are the following:

- It is a non-contact method.
- It represents real process conditions in which parameters can be changed to reflect changes in process conditions.
- It is relatively easy to control the stress configuration(s).
- This test can be combined and made part of solar cell processing. For example, it could be used as a high-temperature step as a pre-gettering process to dissolve impurity precipitates.

Resonance Ultrasonic Vibrations for Crack Detection in PV Crystalline Silicon Wafers

W. Dallas, O. Polupan, S. Ostapenko

Nanomaterials and Nanomanufacturing Research Center, University of South Florida,
4202 E Fowler Avenue, Tampa, Florida 33620

ABSTRACT. Resonance Ultrasonic Vibrations (RUV) technique is adapted to fast and non-destructive crack detection in full-size Si wafers for solar cells. The RUV methodology relies on deviation of the frequency response curve of the wafer with periphery crack versus regular non-cracked wafers. This effect offers a convenient in-line test for rejection of the fragile and mechanically unstable wafers to increase the yield of production lines. We performed analyses of the RUV at different vibration modes to assess sensitivity versus crack length. Finite Element Analyses confirmed experimental data.

INTRODUCTION. The photovoltaic industry provides a pathway to allow renewable energy to meet world wide consumer energy needs. Past and present research and development on silicon based solar cells have helped make them one of the dominant players in the photovoltaic industry. One of the current technological problems is to identify and eliminate sources of mechanical defects such as thermo-elastic stress and cracks leading to the loss of wafer integrity and ultimately breakage of as-grown and processed Si wafers and cells. The problem is of increased concern as a result of the current strategy of reducing wafer thickness down to 100 microns and increasing the wafer size up to 156 mm. Cracks generated during wafer sawing or laser cutting can propagate due to wafer handling and solar cell processing such as, phosphorous diffusion, anti-reflecting coating, front and back contact firing, and soldering of contact ribbons. The development of a methodology for fast in-line crack detection and control is required to match the throughput rate of cell production lines, which is typically at 2 seconds per wafer. At this time, there are several experimental methods, which address the problem of crack detection. They include Scanning Acoustic Microscopy, ultrasonic lock-in thermography [1], optical crack detection [2], electro-luminescence [3], and bending strength tests [4]. In this paper, we further develop a new experimental approach based on the Resonance Ultrasonic Vibrations (RUV) methodology, which was recently applied to detect stress and cracks in silicon solar-grade wafers [5, 6].

EXPERIMENTAL. In the RUV method, ultrasonic vibrations of a tunable frequency are applied to the silicon wafer (Fig.1). Ultrasonic vibrations are generated in the wafer using an external piezoelectric transducer vacuum coupled to the bottom of the wafer. The vibrations form standing acoustic waves at resonance frequencies. The resonance frequencies can be analyzed with a broadband ultrasonic probe. Using a computer controlled frequency sweep (f-scan) through a particular resonance mode, the RUV system provides accurate measurements of the resonance frequency, the maximum vibration amplitude, and the bandwidth (BW) of the resonance curve. In the present design, the ultrasonic probe measures the longitudinal vibration mode characteristics by contacting the edge of the wafer with a controlled contact force. The

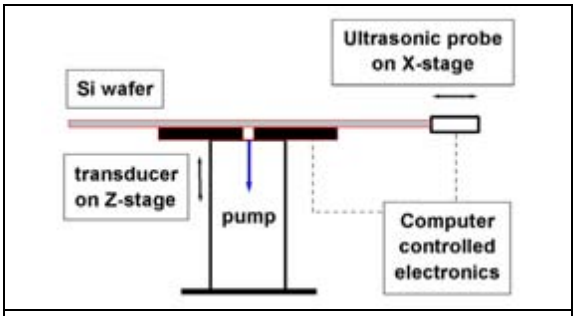


Figure 1: Schematic of experimental RUV system.

piezoelectric transducer also acts as a transport device through its vacuum ports. We also used the *HS1000 HiSPEED*™ Scanning Acoustic Microscope (SAM) for identification of cracks on selected wafers to compliment the RUV data. In this study we used commercial Cz and cast silicon wafers from different vendors.

RESULTS AND DISCUSSION. Initially when dealing with wafers of new geometries and sizes a broad-band frequency spectrum is measured and analyzed to identify RUV peaks, as illustrated in Figure 2. Peak position of RUV modes is varied with the wafer size. A simple relation is observed which is confirmed by FEA results that the resonance frequency of the individual RUV peak is inversely proportional to the wafer size. The RUV peaks are characterized by significant amplitude and narrow bandwidth ~100 Hz in Cz and cast wafers. Once they are identified further analysis is possible on wafers with similar size and shape. By analyzing RUV f-scans and evaluating peak frequency position, bandwidth, and amplitude, of identical wafers, deviations of the RUV parameters can be quickly detected. The RUV method is capable of fast, within a few seconds, measurements which include data acquisition, analyses, wafer loading and unloading. This high speed of measurement has given this method an advantage over other methods for crack detection. Work is currently being done to lower this time and bring it into the sub 2 second range.

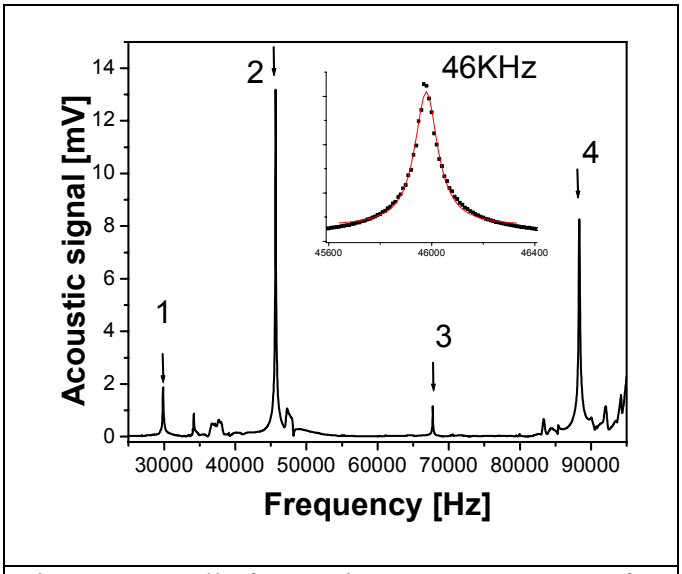


Figure 2: Full f-scan in 156mm cast wafer. Arrows show four individual RUV modes. Insert shows f-scan of 46KHz mode (points) and Lorentzian fit (solid line).

Understanding the effect of a crack on the resonance frequency of a wafer is a key to accurate crack detection. Modeling with finite element analysis (FEA) is used to help understand the resonance vibration response to a crack. In order to assure that our FEA modeling is valid we conducted an experiment to physically determine the mode shape from the vibration amplitude measurements along a wafer's edge. Resonant vibration modes were found using full spectrum frequency scans similar to the one in Figure 2.

Once the peak vibration frequency of a specific mode was found the mode shape was analyzed by conducting a single peak scan along one edge of the square shaped Si wafer. The probe moved in a program mode along the wafer's edge with a constant step and the probe measured individual f-scans. The resonant peak edge scan was measured with steps of 3 to 5mm along one edge of the wafer to construct a representative mode shape. The change in peak amplitude along the edge of the vibrating wafer was found to be representative of

the specific mode shape at the respective frequency. FEA using the ANSYS® software package was used to model the resonant vibrations in the free-edge wafer and produce a representative mode shape. A 156 mm x 156 mm cast Si wafer was used for the test and the results for one particular mode (46 kHz) are shown in Figure 3. The strong correlation between the theory and experimental data allows us to continue using FEA when analyzing new wafer geometries and crack positions and lengths.

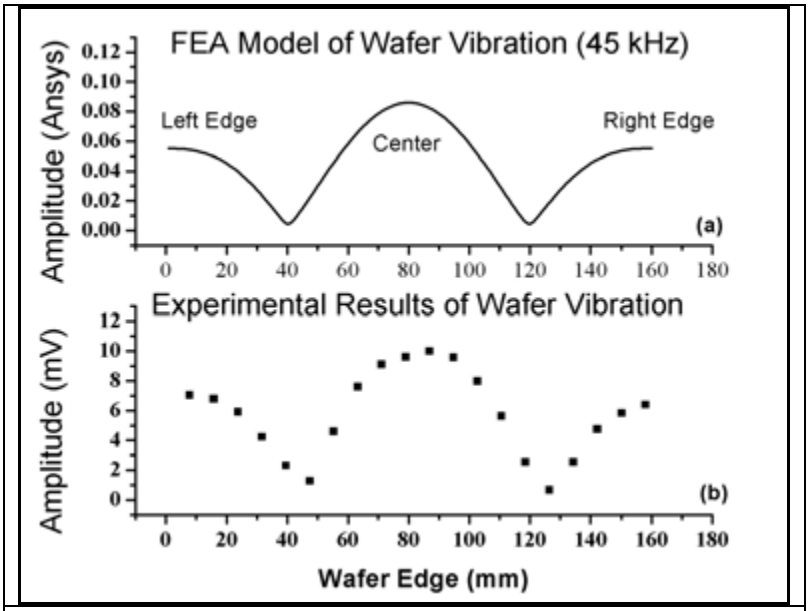


Figure 3: (a) 46 kHz FEA modeling of the RUV edge scan, (b) experimental data on 156 mm size cast wafer.

Through the use of FEA analysis we have been able to understand the apparent selective sensitivity of certain RUV modes to periphery cracks. A study was carried out using Cz-Si wafers to determine the sensitivity of the RUV system to cracks propagating from the edge center. Figure 4 shows an example with a 125 x 125 mm Cz-Si wafer, for two vibration modes with peaks at 56 KHz and 87.5 KHz. Calculating a scaling factor, these modes correspond to #2 and #3 resonance peaks presented in Figure 2. Both RUV peaks were measured with no damage to the wafer and after a 6 mm crack had been made at the center of the wafer as confirmed by SAM imaging.

It can be seen that at this particular crack position the 56 kHz mode is less sensitive to the 6 mm central crack with a small downward frequency shift of 18 Hz, negligible bandwidth broadening and only a slight reduction in amplitude (0.2 mV). The 87.5 kHz mode shows a substantial downward frequency shift of 655 Hz along with the amplitude reduction (1.7 mV) and bandwidth increasing by 40 Hz. These experimental data were compared with FEA analyses using the algorithm described in Ref [6]. The model crack was located at the wafer center at 45^0 with respect to the wafer edge, similar to the experiment. Crack length was changed from 1 mm to 16 mm and peak position was calculated for vibration modes at 40, 58 and 86 KHz (mode numbers 1, 2 and 3 in Figure 2). The result presented in Figure 5a illustrates that in the case of central crack a shift of the mode with highest frequency of 86KHz is the largest. We also evaluated the effect of the crack vibration damping which was modeled by a spring elements with variable stiffness. Stiffness increase as expected reduced the shift as illustrated in Figure 5b for the 10mm central crack. This fitting parameter allows better match the experimental RUV data with FEA modeling. In conclusions, RUV experiments and FEA modeling on different vibration modes indicated that sensitivity of crack detection using RUV test is varies at different vibration modes.

The work was partially supported by the NREL subcontract No. AAT-2-31605-06.

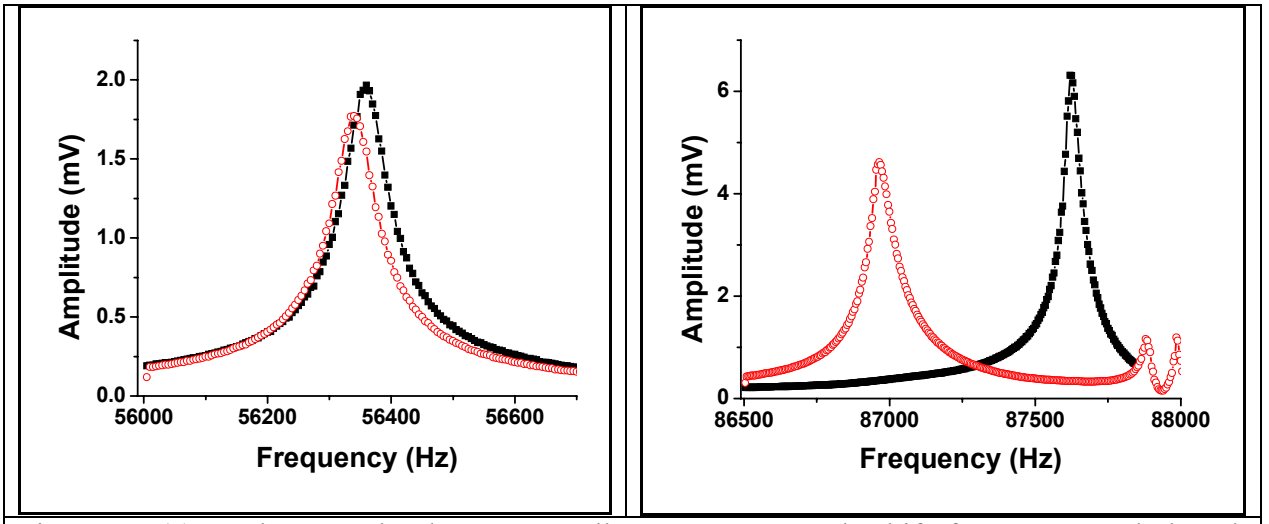


Figure 4: (a) 56 kHz mode shows a small 18Hz RUV peak shift for 6mm crack length compared to a large 655Hz peak shift of 87.5KHz mode (b). Closed points represent undamaged wafer, open circles are data of the same wafer with the crack.

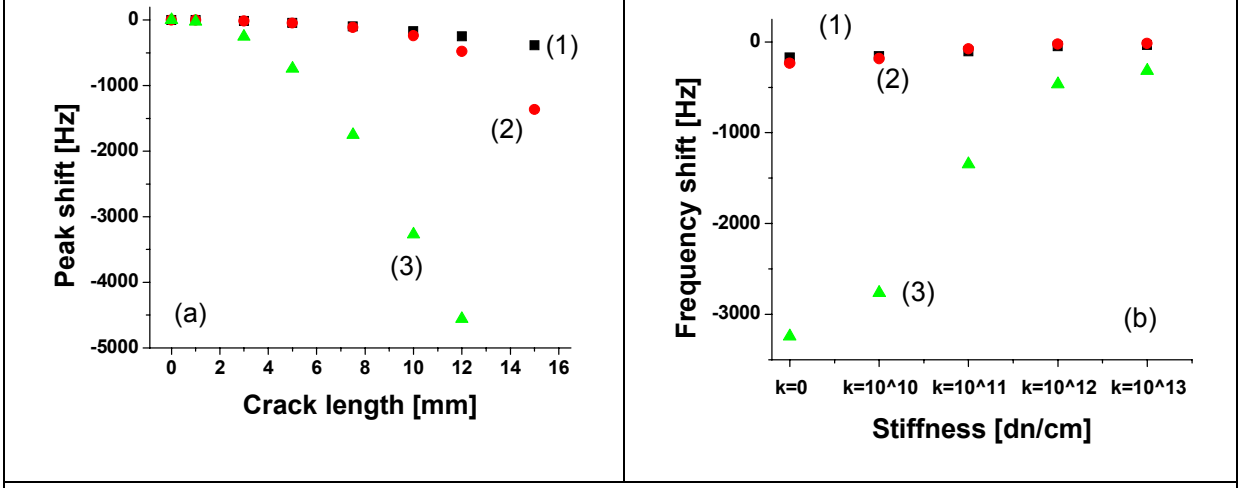


Figure 5: (a) Peak shift versus crack length dependences for three vibration modes on 125mm wafer for the center edge crack location; (b) variation of the peak shift with stiffness of the spring element. (1) – 40KHz, (2) – 58KHz, and (3) 86KHz mode.

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Analysis of Microwave Reflection for Measuring Recombination Lifetime in Silicon Wafers

R. K. Ahrenkiel [a,b] and S. W. Johnston [a]
a. National Renewable Energy Laboratory, Golden, Colorado
b. Department of Physics and Astronomy, University of Denver, Denver Colorado

Introduction

Measurement of the minority-carrier lifetime is a critical activity for a range of silicon devices, including solar cells. A current approach in silicon photovoltaic (PV) technology is to use low-cost substrates to lower the overall system cost. Lifetime measurement is a critical materials test that is used frequently in the PV research laboratory, and is more and more being incorporated in the manufacturing environment. Similar requirements have developed in the integrated-circuit industry, where the minority-carrier lifetime is used as a test of wafer quality and uniformity. Because of these testing needs, contactless techniques are mandatory, as any diagnostic requiring contact formation usually contaminates the wafer.

Here, we analyze the microwave reflection technique (MWR), which is probably the most popular diagnostic for silicon technologies. We have two measurements systems at NREL, operating at frequencies of 7 GHz and 20 GHz. In the following, we analyze the effects of injection level on the quality of the data provided by this technique.

Microwave Reflectance Lifetime Measurement Technique

Recombination lifetime is a sensitive indicator of structural integrity and crystal purity. The silicon electronics industry has adopted MWR as a standard technique for silicon wafer lifetime characterization. A microwave generator, usually operating between 10 to 30 GHz, is used as a probe beam. This beam is reflected by the free carriers of the semiconductor, and the reflection coefficient is a function of carrier density. A pulsed light source, which is usually a diode laser, is used to excite excess carriers. These excess carriers modulate the reflection coefficient of the microwave signal, and that change is recorded on a digitizing oscilloscope. The decay rate of the excess carriers is used to measure the minority-carrier lifetime. The reflection coefficients of microwaves by the free carriers of a semiconductor were calculated some years ago by Kunst and Beck [1]. Figure 1 shows the reflectance coefficients of a semiconductor at incident microwave frequencies of A: 7 GHz and B: 20 GHz for sample resistivities varying between 0.1 and 100 ohm-cm. We see from the figure that the reflection coefficient is a very nonlinear function of sample resistance. One must work with these calculated results to avoid nonlinearity, which may distort the transient time-resolved microwave reflectance.

To measure the excess-carrier lifetime, one uses a light pulse to induce a transient change in the conductivity and then monitors and records the transient reflectance decay. We can write the reflected microwave power in terms of a Taylor series:

$$\Delta P = P_{in} \frac{dR(\sigma)}{d\sigma} \Delta\sigma, \qquad (1)$$

We define the derivative $dR/d\sigma$ as the sensitivity factor A(s). As $R(\sigma)$ is a nonlinear function of conductivity, transient measurements are usually limited to the small signal

(low-injection) range. When $\Delta\sigma << \sigma$, the higher-order terms in the Taylor expansion can be neglected. We can see from Fig. 1 that the nonlinearity holds for almost all concentration ranges. In practice, one must use an excess- carrier injection level that is generally less than 0.05 times the background carrier density. Here, we will show resistivity (conductivity) regimes where larger injection levels will accurately track $\Delta\sigma$. Finally, at the highest conductivity ranges, the response will saturate, and the reflection coefficient approaches unity. For silicon doped to very high carrier densities, the excess-carrier lifetime cannot be measured by this method.

Theory of Photoconductive Decay

Using Fig. 1, the transient microwave reflectance $R(\sigma+\Delta\sigma(\square))$ tracks the transient excess conductivity following pulsed excitation. The latter can be written as:

$$\Delta\sigma = q(\mu_n + \mu_p)\rho(x,t). \quad (2)$$

Here, $\mu_{n,}(\mu_p)$ are the electron (hole) mobilities, and $\rho(x,t)$ is the excess-carrier concentration. When recombination may be described a single lifetime, τ, one can write Eq. 2 as:

$$\Delta\sigma = q(\mu_n + \mu_p)\rho(x)\exp(-t/\tau). \quad (3)$$

If one applies contacts to the material being tested and applies a dc voltage across the contacts, the transient conductivity is described by Eq. 2. If the incident pulse is monochromatic, the conductivity has the following form:

$$\Delta\sigma(t) = qI_0(\mu_n + \mu_p)(1-\exp-\{\alpha[\lambda]W\})\exp(-t/\tau). \quad (4)$$

Here, $\alpha(\lambda)$ is the absorption coefficient of the material, I_0 is the incident optical density in photons/cm^2, and W is the sample thickness. The instantaneous microwave reflectance is then given by:

$$R = R(\sigma + \Delta\sigma(t)) \quad (5)$$

where R may be found from the Kunst-Beck formulas.

Experimental Apparatus

Our experimental apparatus uses the standard wave guide configuration as described by Kunst and Beck and others [1,2]. The microwave signal is incident from the "backside" of the sample and the light pulse is incident from the opposite or "frontside" of the sample. The light source is produced for a YAG-driven Continuum Panther optical parametric oscillator (OPO) and has a pulse width of about 5 ns full-width, half maximum. The wavelength is variable over a wide range, but the measurements here were performed at 905 nm for comparison with GaAs diode laser data. The latter is often used for these measurements. The OPO beam is expanded to about 2.5 cm diameter at the sample. The beam intensity is controlled by the insertion of calibrated neutral density filters to produce the desired injection level.

A variety of p-type single-crystal silicon wafers were used in the experimental studies. The resistivities ranged from 0.3 to 200 ohm-cm. Most of the measurements were performed "in air" with unpassivated surfaces. However, a few measurements were made in a passivating iodine-methanol solution after an HF etch.

MWR Simulations

The MWR simulations shown here were produced by incorporating the Kunst-Beck formalism into Eq. 3. The silicon mobilities are a function of carrier density(n, p), and the mobilities were calculated using the values proposed by Pang and Rohatgi[3]. The lifetime was assumed to be independent of carrier density (n, p). Of course, the latter assumption is not generally correct because of the partial "filling" of recombination centers[4] during the transient decay. However, the latter effects are sample dependent and could not practically be included in a more general model. The MWR transient was calculated with the noted assumption using Matlab 7.04.

Calculation of MWR Transient.

Figure 2 shows the calculated MWR transient for a wafer that is doped p-type to a carrier density of $1x10^{14}$ cm^{-3}. Microwave probe frequencies of 7 GHz and 20 GHz were assumed for the calculation. The peak injection level used for the calculation was $1x10^{16}$ cm^{-3} electron-hole pairs, and the lifetime was assumed to be 10 μs. In the figure, Curve A represent a "pure" 10 μs decay event, and Curve B represents the calculation of the 20 GHz microwave reflection coefficient. The latter is represented as the absolute, incremental reflectance, as it may be either positive or negative, depending on the conductivity range. Curve C represents the calculation of the 7 GHz microwave reflection coefficient. We see from the calculation that the 7 GHz simulation represents the "true" lifetime over a considerable range of injection levels, whereas the 20 GHz representation gives the correct slope after a delay of about three lifetimes.

Figure 3 shows the calculated MWR transient for a wafer that is doped p-type to a carrier density of $1x10^{15}$ cm^{-3}; probe frequencies of 7 GHz and 20 GHz were assumed for the calculation. The peak injection level used for the calculation was $1x10^{17}$ cm^{-3} electron-hole pairs, and the lifetime was again assumed to be 10 μs. In this calculation, the distortion of the simulated decay curves is more severe as the transient conductivities are closer to the "knee" or minimum of the Kunst-Beck curve of Fig. 1. The 7 GHz simulation develops the correct decay slope after about four lifetimes. and the 20 GHz simulation has the correct slope after five lifetimes of delay.

Figure 4 shows the calculated MWR transient for a wafer that is doped p-type to a carrier density of $1x10^{16}$ cm^{-3}, with probe frequencies of 7 GHz and 20 GHz, and the peak injection level is $1x10^{18}$ cm^{-3}. The assumed lifetime is again 10 μs. In this calculation, the distortion of the simulated decay curve is very severe for both probe frequencies. The transient changes sign at about 2 μs for the 20 GHz probe frequency and at about 45 μs for the 7 GHz probe frequency. To extract the correct decay time at either frequency, one must delay the measurement for from seven to eight decay times. This severe distortion results from the conductivity change incorporating the minimum or "knee'" of the Kunst-Beck curve.

MWR Measurements

Figure 5 shows our MWR data using the 20 GHz measurement system on a CZ-grown sample. The sample is p-type and the resistivity is 162 ohm-cm as measured by a four-point probe. The measurements were made in iodine/methanol solution after standard HF etch. The equilibrium hole concentration is about 8×10^{13} cm^{-3} and the injection level is increased by one decade for each curve, A through F. For Curve A, the injection level is

7.5 x 10^{11} cm^{-3}, and Curves B through F represent increases from 7.5 x 10^{12} cm^{-3} to 7.5 x 10^{16} cm^{-3}, respectively. We assumed that Curve A shows the true, low-injection lifetime of about 33 μs. The initial slope of Curve F shows the MWR nonlinear distortion with a slope corresponding to over 1000 μs. The latter is far too large to result from the saturation of deep-level defects. However, lower injection levels may represent true recombination lifetimes with the gradual filling of deep-level defects.

Figure 6 shows the same passivated CZ wafer run in the 7 GHz apparatus. The lifetimes at all injection levels are similar to those of Fig. 5, and in agreement with the simulation shown in Fig. 3. Again, the initial decay slope of Curve D (7.5 x 10^{16} cm^{-3}) is undoubtedly due to the nonlinear response of the MWR signal as the carrier concentration approaches the "cusp" of the Kunst-Beck reflectance curve. However, the general features of the measurements on higher resistivity wafers indicate that MWR can be accurate at higher injection levels in such wafers.

We did similar measurements on a more heavily doped, p-type wafer, in an attempt to explore the accuracy of MWR. A number of such wafers were measured by MWR, and the sample to be examined in detail here has a resistivity of 0.3 ohm-cm.

The data of Fig. 7 were obtained from MWR measurements, using the 7 GHz probe frequency. These data were measured in air and without iodine/methanol passivation, as surface recombination is much less significant for this wafer. Curve A, measured at the lowest injection level, has an initial excess-carrier concentration of 7.5 x 10^{12} cm^{-3}, and a lifetime of about 1.1 μs. However, as seen here, the signal is very weak and lifetime extraction may not be accurate. An initial injection level of 7.5 x 10^{12} cm^{-3} produces a continuous varying lifetime. Near the end of the decay, the slope corresponds to 3.9 μs. The asymptotic decay time appears to be constant for the next two decades of injection level (7.5 x 10^{13} cm^{-3} and 7.5 x 10^{14} cm^{-3}). However, these measurements are all in the low-injection regime. Curvature of the decay becomes quite apparent for Curve D, with an injection density of 7.5 x 10^{16} cm^{-3}. However, this curvature could be either deep-level "filling" or MWR nonlinearity.

The data of Fig. 8 were obtained from the same wafer with a probe frequency of 20 GHz. The decay curves are much more erratic and are inconsistent with those of Fig. 7. At the lowest injection level, 7.5 x 10^{13} cm^{-3}, the lifetime is about 0.9 μs, which is in agreement with Curve A of Fig. 7. However, the lifetime values between the two sets of data are in poor agreement at the same injection levels.

Conclusions

Our similation and experimental results look at microwave reflection applied to wafers with resistivities ranging from about 0.1 to 200 ohm-cm. In this work, we examined the effects of injection level on the accuracy of the measurement. Our simulations and experimental results indicate that the MWR technique is quite tolerant of high injection measurements for higher wafer resistivities i.e.. in the range of 100 ohm-cm or more. The MWR signal tracks the excess carrier density over several decades of injection level. However, for wafer conductivity in the range of 0.1 to 1 ohm-cm, the situation is very different. Here, simulation results indicate serious nonlinearities of the measurement response with these higher injection levels. The experimental results indicate a dispersion of data that depends on injection level and on the microwave probe frequency.

Therefore, in this conductivity range, measurements should be limited to low injection levels. This conductivity range is a popular doping range for the base region of n^+/p silicon solar cells. Thus, the application of MWR to lifetime measurements for these higher conductivities should be done with great care and limited to low-injection conditions.

Acknowledgements

The first author (RKA) would like to thank the Denver Research Institute for partial support of the work done in this project. The second author (SWJ) acknowledges the U. S. Department of Energy for supporting this work under contract DE-AC36-99GO10337.

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FIGURES

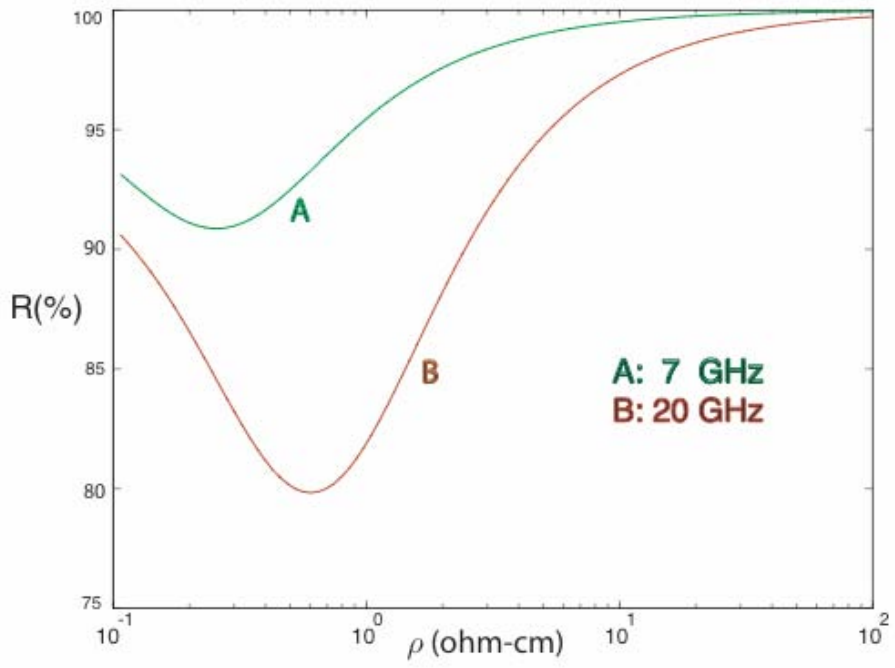

Figure 1. The microwave reflection coefficient as a function of resistivity for probe frequencies of A:7 GHz and B: 20 GHz.

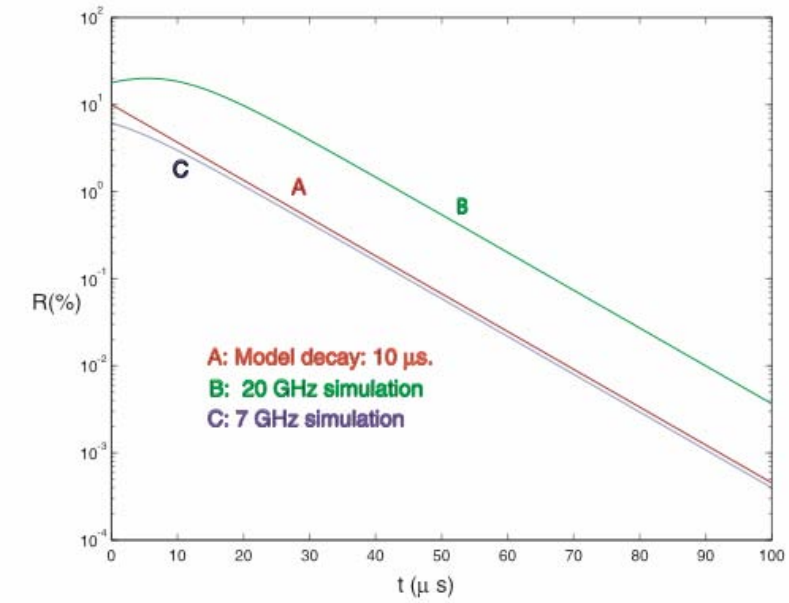

Figure 2. Simulated MWR decay for a p-type sample doped to $1x10^{14}$ cm^{-3} and with an injection level of $1x10^{16}$ cm^{-3}.

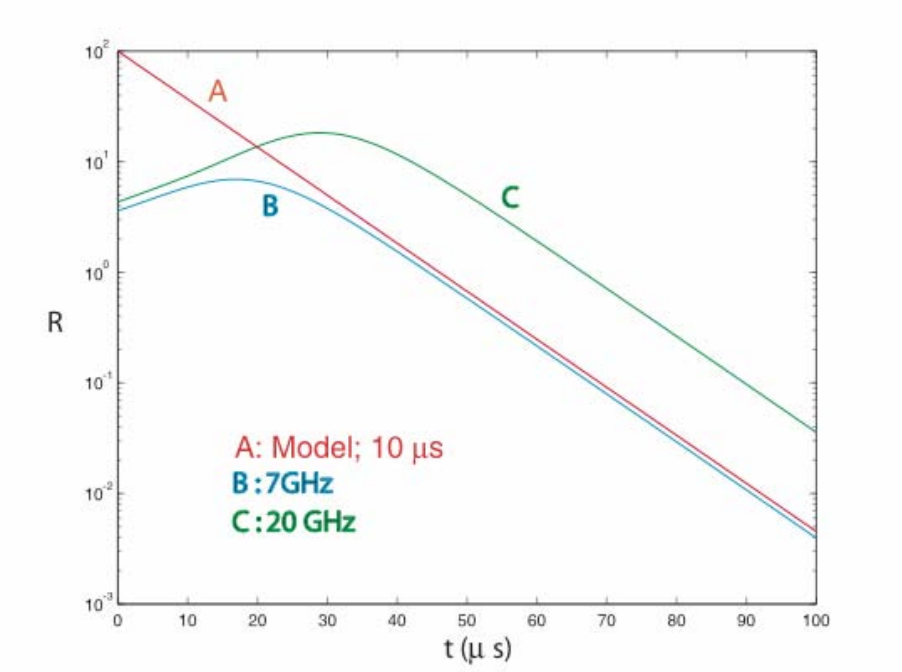

Figure 3. Simulated MWR decay for a p-type sample doped to $1x10^{15}$ cm^{-3} and with an injection level of $1x10^{17}$ cm^{-3}.

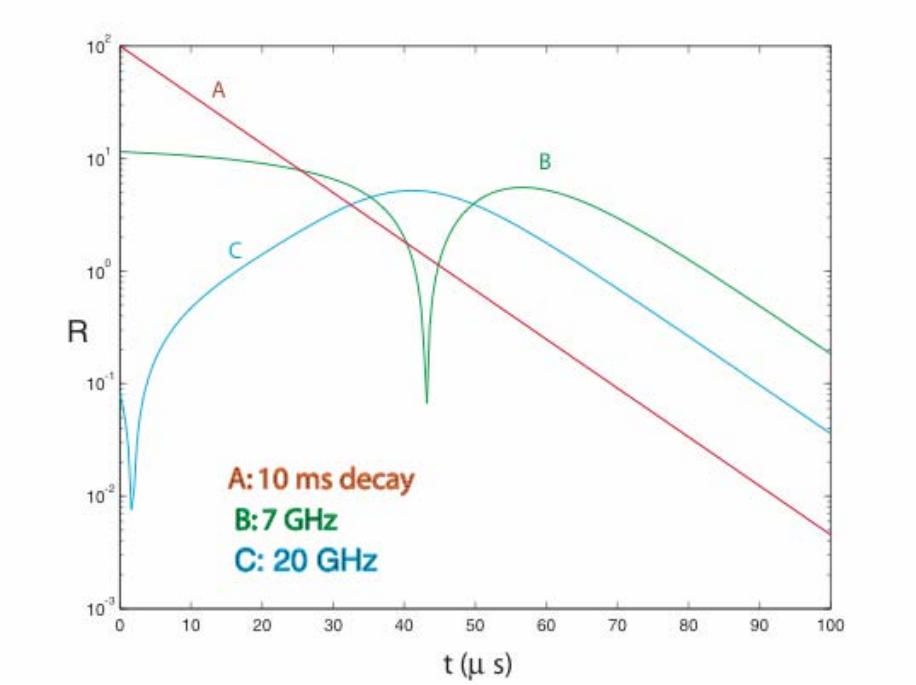

Figure 4. Simulated MWR decay for a p-type sample doped to $1x10^{16}$ cm^{-3} and with and an injection level of $1x10^{18}$ cm^{-3}.

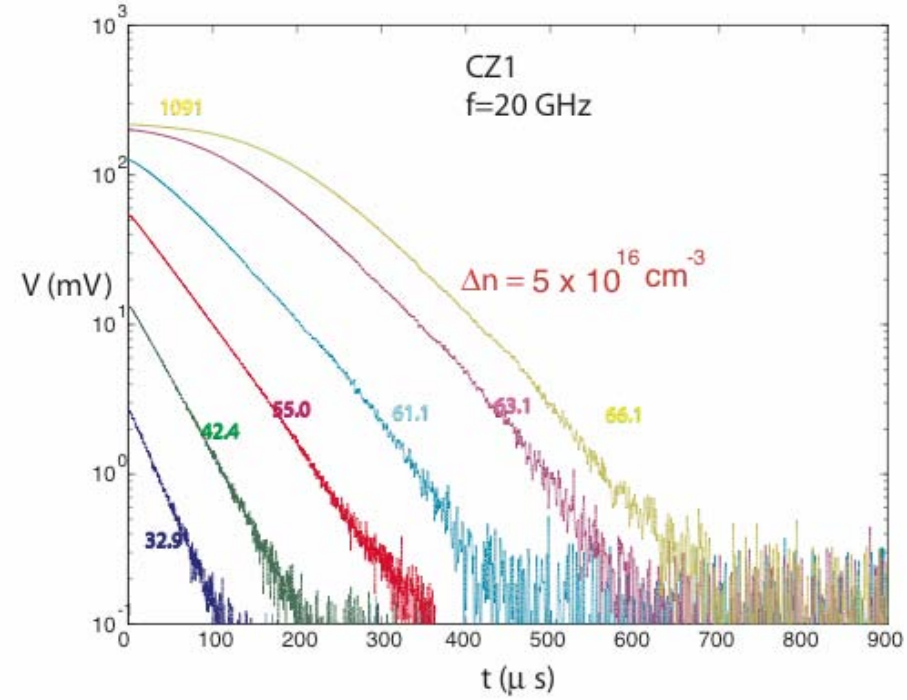

Figure 5. MWR data for a p-type sample with ρ =174 ohm-cm.

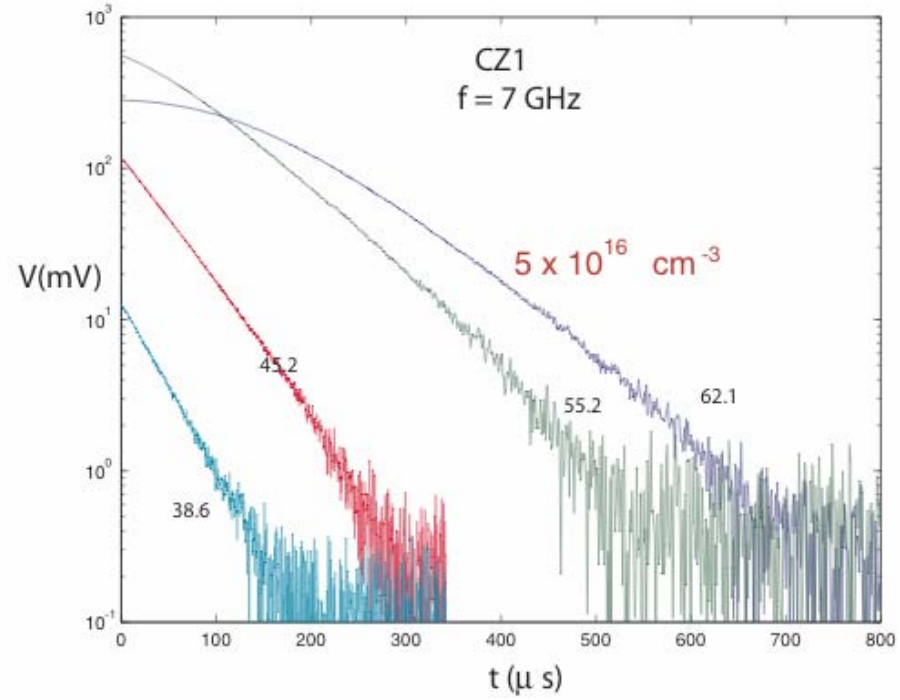

Figure 6. Same sample as above but with f=7 GHz.

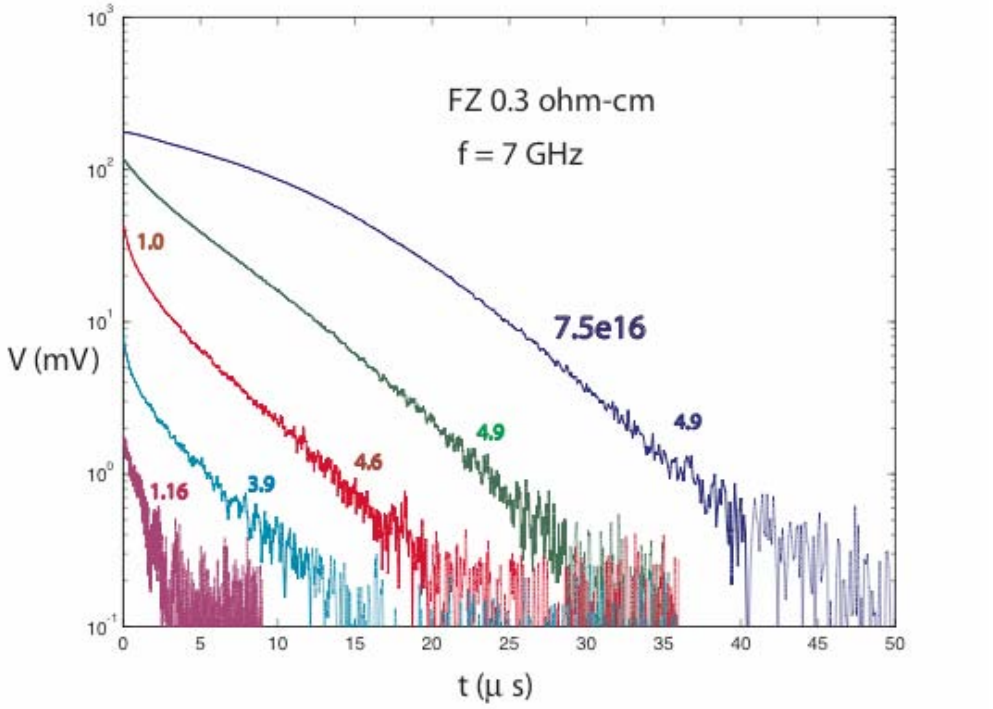

Figure 7. MWR data for a p-type sample with ρ =0.3 ohm-cm.

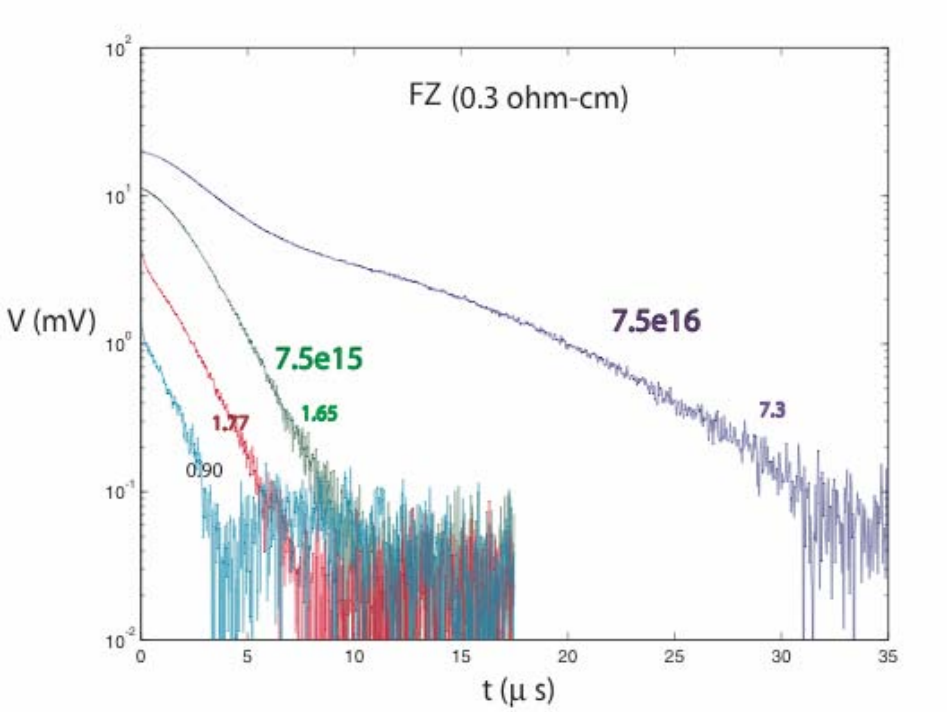

Figure 8. Same sample as above but with f=20 GHz.

Silicon epitaxy at ~100 nm/min by hot-wire chemical vapor deposition at glass-compatible temperatures

Charles W. Teplin, Pauls Stradins, Matthew Page, Kim M. Jones, Howard M. Branz, and Qi Wang
National Renewable Energy Laboratory, Golden, CO 80401

Abstract

We grow over 10 microns of silicon epitaxy on (100) silicon wafers using hot-wire chemical vapor deposition (HWCVD) at 610°C with a growth rate of 110 nm/min. Compared with previous HWCVD experiments at glass-compatible temperatures, this is an order of magnitude improvement in both the rate and achievable thickness. A study of films grown at varying substrate temperatures strongly suggests that the improved epitaxy is due to the reduced hydrogen coverage above the silicon surface dehydrogenation temperature.

Introduction

The combination of excellent electronic properties and high cost of crystal silicon has motivated numerous approaches to fabricating photovoltaics out of thin films of crystal silicon on an inexpensive substrate.[1-4] All of these approaches require two steps: First, a crystal silicon seed is established on the substrate and second, the silicon layer is thickened epitaxially. In order for these approaches to be economical, the thickening step must be rapid (high growth rate), compatible with low-temperature substrates such as glass, scalable to large areas, and manufacturable at moderate vacuum.

Previously, HWCVD epitaxy[5] has been explored at temperatures below 500°C. Over 1 micron of twinned epitaxy was achieved at the California Institute of Technology at 300°C and 1Å/s.[3] At NREL, over 400 nm of epitaxy was grown at 2Å/s at 380°C.[6] Interestingly, further increases in temperature between 380°C and 500°C did not result in thicker epitaxial layers. Compared with other techniques used for silicon epitaxy, HWCVD has the advantage of being a simple technique that could be scaled for manufacturing.

Here, we report new experiments using HWCVD at high growth rates (110 nm/min) with substrate temperatures between 500°C and 645°C. On (100)-oriented wafers, we find purely epitaxial films above 600°C, while below 600°C the growth is polycrystalline. Interestingly, thick growth on (100) substrates results the formation of aligned needle-like grains, each growing along (311) facets at the film surface. This results in a very rough surface that could be used for light trapping in solar cell devices.

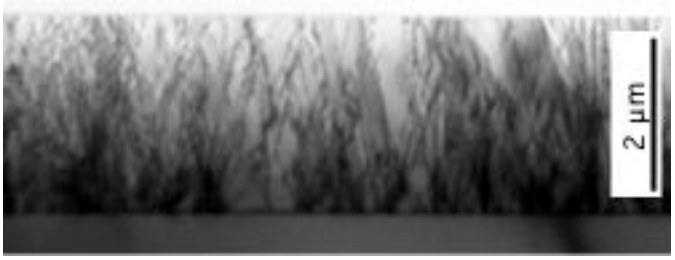

Fig. 1. TEM of an epitaxial film grown at 610°C on a (100) silicon wafer.

Experiment

Epitaxial films were grown in a hot-wire chemical vapor deposition reactor. Crystal silicon substrates were cleaned and dipped in 4% HF immediately before loading into the vacuum. System base pressures were typically 2 to 5 x 10^{-6} Torr. During deposition, 20 sccm of SiH_4 was flowed to the reactor and the pressure was held at 11 mT using a throttle valve. The SiH_4 was decomposed by heating with a 16 A current a 0.51-mm tungsten filament held 5 cm from the substrate. These conditions resulted in a growth rate of 110 nm/min. Substrate temperatures were monitored using a thermocouple touching the back of the substrate. The thermocouple readings were calibrated to the true substrate surface temperature using an optical pyrometer.

Films were analyzed using x-ray diffraction (XRD), scanning electron microscopy and optical reflectance. Selected films were also measured using transmission electron microscopy (TEM).

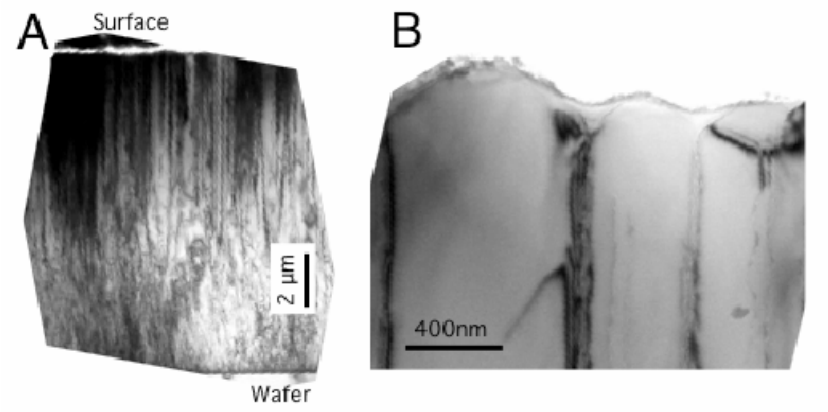

Fig. 2. TEM cross section of an 11 micron thick film grown at 610°C. In A, a low-magnification image shows the entire film. In B, a higher magnification image shows the top surface of the film.

Results

Successful epitaxy at 610°C was confirmed using TEM on selected samples. A TEM of a 2 µm thick film grown on a (100) wafer is shown in Figure 1. The lines running through the film in the image indicate the presence of dislocations. The density of dislocations appears to be highest near the substrate/film interface and lower near the surface of the film, suggesting dislocation loops beginning at the surface. It is likely that poor cleaning of the crystal silicon surface before epitaxy contributes to dislocations are at least partially caused by. Higher resolution images of the substrate/film interface (not shown here) show lattice planes clearly running through the interface, confirming epitaxy.[7]

A second TEM of an 11 micron thick film (grown under identical conditions to the film in Fig. 1) is shown in Figure 2. In Fig. 2A, a low-magnification image confirms that the entire film is epitaxial. Fig. 2A also shows that the dislocation density continues to decrease with film thickness until columnar growth of dislocation-free grains is established after ~5µm. A higher resolution image (Fig. 2B) shows that these dislocation-free regions are approximately 500 nm wide. Additionally, each of the grains in Fig 2B has an angled growth front. AFM images of this film (not shown) reveal a highly textured surface an an angle of 26±5° between the growth facet and the sample normal, consistent with growth along vicinal <311> planes.[7] This "natural" texturing acts identically to a chemically obtained light-

trapping texture and reduces the overall reflectivity of the film surface by over 20% between wavelengths of 200 nm and 1000 nm. [7]

Successful epitaxy, unsurprisingly, depends crucially on the substrate temperature. XRD results at low angles (2θ ~20-60°) for three films grown on (100) substrates are shown in Figure 3. An entirely epitaxial film would only result in diffraction at 69° [the (400) diffraction peak] and no peaks would be observed in Fig. 3. This is what we observe for a film grown at 610°. However, at 548°C and 519°C, strong (111), (220), and (311) diffraction peaks are observed, indicating that epitaxy failed at these temperatures and that polycrystalline growth occurred.

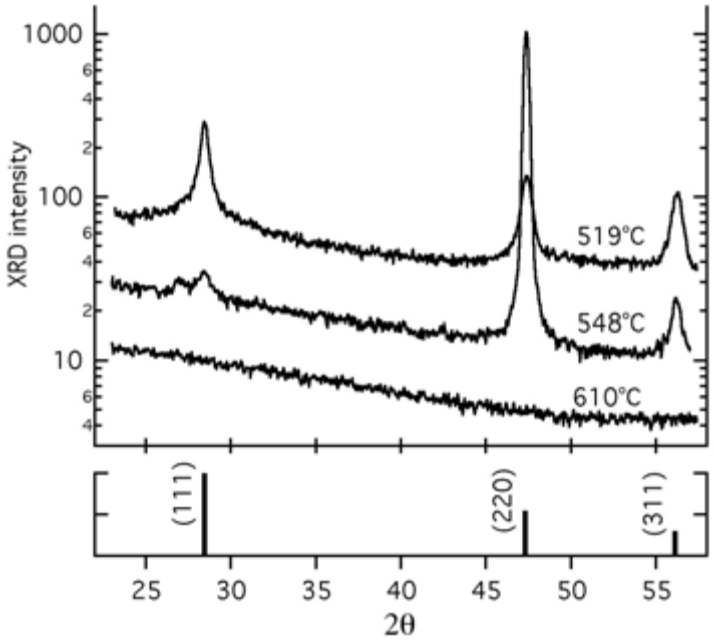

Fig. 3. XRD diffraction results for three films grown at different temperatures

Discussion

Technologically, rapid silicon epitaxy at glass-compatible temperatures using a scalable deposition technique is crucial for a number of emerging approaches to fabricating thin crystal silicon layers on glass for solar cell applications.[1-4] All of these approaches consist of two main steps: establishing a thin crystal silicon seed on an inexpensive substrate and subsequently thickening this seed epitaxially at temperatures compatible with the inexpensive substrate. Estimates of the necessary silicon thickness to adequately capture sunlight depend on the light trapping scheme employed in a device, but 10 μm of silicon should be adequate to fabricate a 15% efficient cell.

Scientifically, low-temperature silicon epitaxy has been an interesting subject since it was initially reported by Eaglesham et al. in 1990.[8] Typically, at significantly low temperatures, epitaxy is possible but only for a limited thickness. After this thickness, epitaxy fails and random polycrystalline or amorphous growth results. Nonetheless, various other deposition methods, such as molecular beam epitaxy, ion-assisted electron beam evaporation, and electron cyclotron resonance CVD have demonstrated thick epitaxy by raising the temperature above some critical value. However, no theory yet describes why a transition from limited to unlimited epitaxy exists.

In *chemical* vapor deposition techniques, such as HWCVD, the existence of hydrogen is undoubtedly important during growth. Here, we have found a transition from limited to unlimited epitaxy between 548°C and 610°C. In this temperature range, the silicon surface transitions from being monohydride terminated to hydrogen-free.[9] Thus, we believe that this transition is responsible for the improved epitaxy that we see at 610°C.

Conclusions

We have grown 11 microns of epitaxial silicon on (100)-oriented silicon substrates at 610°C and 110 nm/min using hot-wire chemical vapor deposition. At this temperature and growth rate, it would be possible to use HWCVD to thicken a silicon seed layer for photovoltaic applications.

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Near-field scanning optical microscopy of HWCVD-grown Si film

M.C. Wagener and G.A. Rozgonyi

North Carolina State University, Department of Materials Science and Engineering, Raleigh, NC 27606

1. Introduction

The growth of thin film Si by hot-wire chemical vapor deposition (HWCVD) has promise for the large scale manufacturing of inexpensive solar cells, without many of the disadvantages associated with other thin film technologies. During the development of these thin film materials, however, the evaluation of the electrical characteristics of individual defects and their subsequent effect on device parameters are often limited by the resolving power and sensitivity of the characterization tools available. For photovoltaic applications, this often involves non-contact mapping of the minority carrier lifetime by microwave-PCD, or the carrier diffusion length of finished devices by LBIC. Unfortunately, little information can be extracted concerning the activity of individual components of thin film cells without a higher resolution, electrically based image. This report expands on the LBIC approach by applying near-field scanning optical microscopy (NSOM) for investigations requiring a significantly higher degree of spatial resolution (less than 100 nm) and sensitivity [1-3].

2. Experimental details

The nano-crystalline Si thin film samples used in this report were grown at the California Institute of Technology using HWCVD. The sample set included layers grown on various substrates, i.e. Ni and Al induces templates, as well as (100) Si substrate. Since the devices fabricated on the Si substrates had the best characteristics, the initial investigation focused on these 5.5 µm thick layers. Near-field photocurrent contrast (NPC) images were obtained for these samples by monitoring the photocurrent while scanning a sub-wavelength aperture (less than 100 nm diameter) across the device surface at a constant height of ~20 nm (Fig. 1). In addition to the NPC map, the morphology and scattered light intensity is collected simultaneously. These additional maps are useful for the interpretation of the NPC images and also assist in identifying surface debris and scratches. Compared to far-field optical techniques (i.e. LBIC), the photocurrent maps obtained by a near-field optical probe is expected to have a significantly higher spatial resolution (which is determined by the aperture size instead of the wavelength), as well as an increased sensitivity to the near-surface (less than $\lambda = 632$ nm below the surface) properties of the device.

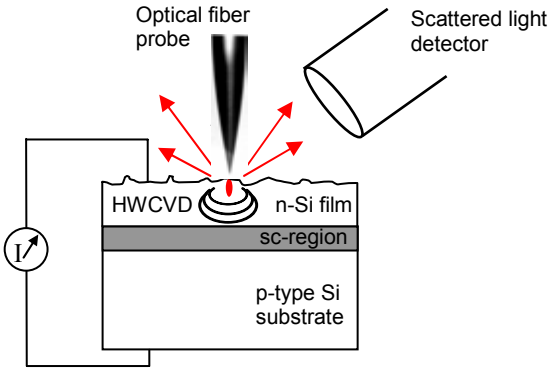

Figure 1 Illustration of the sample structure used for the NPC measurements. The generation volume is anticipated to be concentrated within the first wavelength below the surface when using a near-field excitation souce. The principle contribution to the photocurrent contrast is therefore from the near-surface region of the 5.5 μm Si film.

3. Results and Discussion

Figure 2 shows the simultaneously obtained images of the surface morphology, the collected photocurrent, and the scattered light intensity. The grains appear to be slightly elongated, with the typical grain-size less than 1 μm. The magnified morphology maps also revealed some fine-structure on the surfaces of individual grains. Althought the photocurrent contrast does occassionally show some correlation with the surface morphology (indicated by arrows in Fig. 2), the contrast generally extends over regions significantly larger than the surface features. The NPC image also appears to have very little dependence on the reflected light intensity. The dominant factor responsible for the weak correlation is most likely the surface roughness of the sample. The deep crevices between large grains are likely to impair the photocurrent contrast by preventing the probe from maintaining a near-field interaction throughout the entire scan. The effect of grain-boundaries will therefore be diminished as the probe moves between large grains. The observed photocurrent contrast is therefore more likely to represent the grain to grain variation of the diffusion length and the surface recombination velocity. Ensuring a near-field interaction throughout the scanning area is therefore expected to significantly improve the photocurrent contrast.

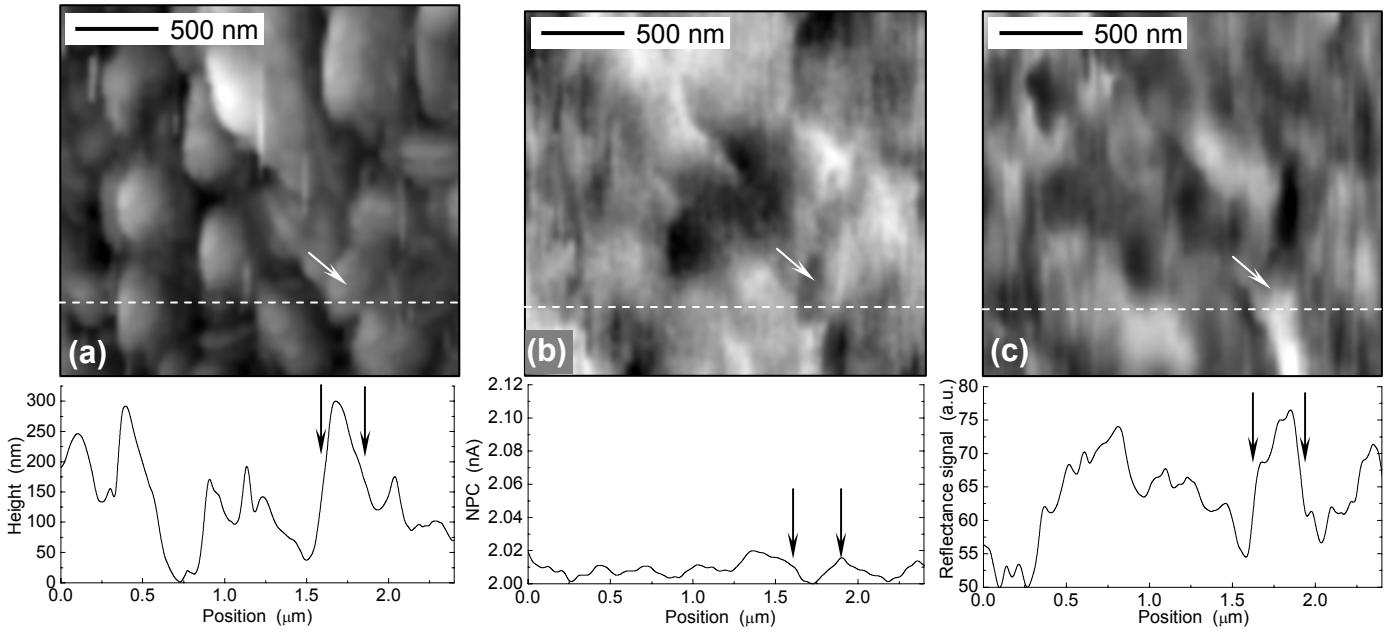

Figure 2 Morphology (a), photocurrent (b) and reflectance (c) maps obtained simultaneously of a 5.5 μm thick Si film grown by HWCVD on (100) Si substrate. The gray scale represents a 320 nm height variation, a 5% change in photocurrent, and a 54% change in reflectance. Line cuts are indicated in figures (a)-(c), respectively. For the sake of comparison, the same NPC range was used in Fig. 3. The narrow vertical features are scanning artifacts.

Transmission electron microscopy performed on a similar sample revealed that the film has a twinned structure close to the substrate interface, with the surface roughness resulting from polycrystalline growth during the later stages of film growth [4]. It was therefore anticipated that the photoresonse would also vary across the film thickness. A more suitable sample was

consequently prepared by introducing a 0.3º off-axis bevel across the surface of the device (Fig. 3). The NPC measurements could then be repeated at different positions along the bevel surface, thereby making it possible to evaluate the photoresponse at different depths below the original surface. Figure 3 depicts a typical NPC image of a region close to the top of the bevel. The contrast has been significantly enhanced compared to the as-received sample (compare line cut to Fig. 2c). Although the morphology and reflectance maps were essentially featureless, it is still possible to relate the NPC image to the grain structure with some level of confidence.

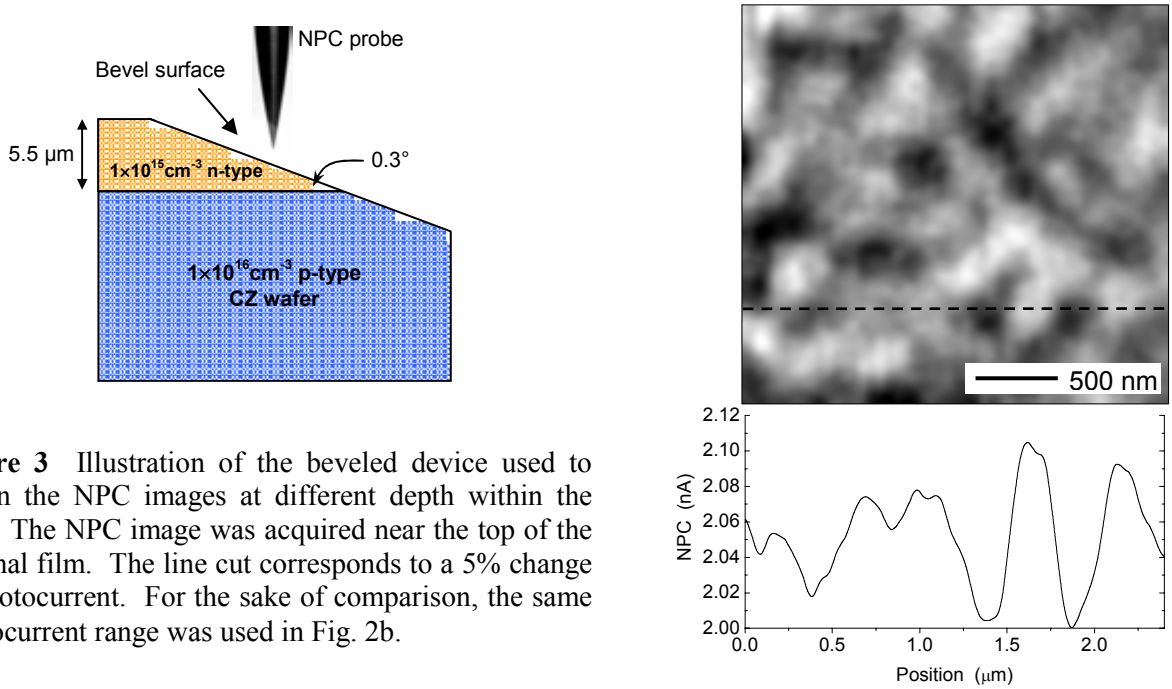

Figure 3 Illustration of the beveled device used to obtain the NPC images at different depth within the film. The NPC image was acquired near the top of the original film. The line cut corresponds to a 5% change in photocurrent. For the sake of comparison, the same photocurrent range was used in Fig. 2b.

The size and distribution of the high photocurrent (white) areas appear to coincide with the expected grain size of the film. The extended regions of low photocurrent (black) are therefore tentatively ascribed to areas bordering grain-boundaries. In order to evaluate the recombination behavior responsible for the photocurrent contrast, further details, such as the optical probe diameter, defect size and the bulk diffusion length need to be incorporated [2]. Since the interpretation of the 5% contrast would require further analysis, this initial investigation has instead concentrated on determining the photoresponse distribution at different positions along the bevel surface.

In order for the NPC map to be representative of a particular depth within the film, the photocurrent contrast needs to display a high degree of sensitivity to the near-surface region. A good test for this criterion is a comparison of the near- and far-field photocurrent maps of the same region. This is accomplished by retracting the optical probe from 20 nm (near-field) to 400 nm (far-field) during a scan. Figure 4 shows the significant decrease in photocurrent contrast as the probe is retracted half-way through the scan. Although the average photocurrent remains unchanged, the far-field image is clearly insensitive to the near-surface characteristics of the sample. Figure 4 therefore confirms that the NPC map represents a very shallow region below the surface, typically a fraction of the

excitation wavelength. Defects further below the surface are therefore effectively in the far-field and consequently contribute little contrast to the near-field photocurrent map. The sensitivity of the NPC image to the near-surface is therefore ideally suited for beveled samples, allowing one to obtain NPC images representative of different depths within the device structure.

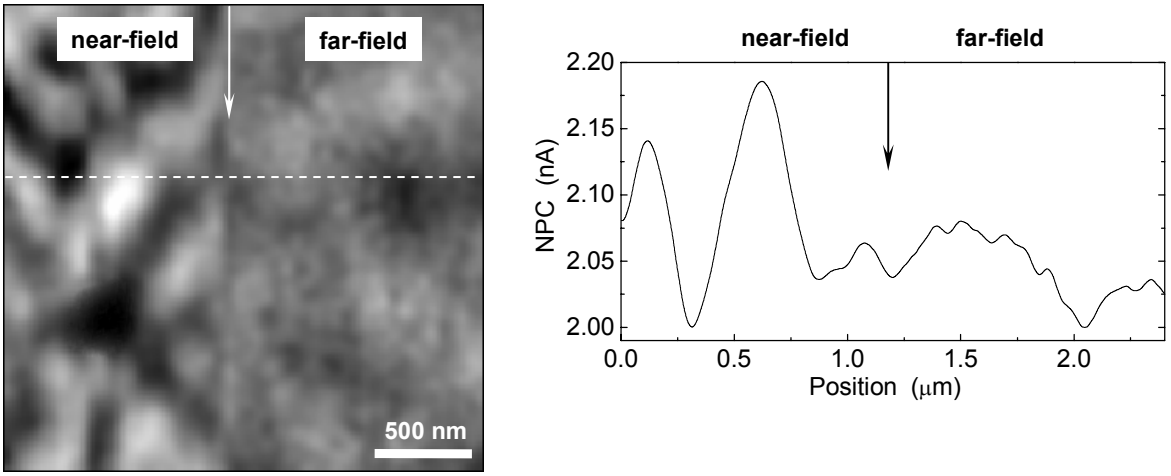

Figure 4 Comparison of the photocurrent contrast obtained under near- and far-field conditions during a continues scan. The left half of the NPC image was obtained under near-field conditions, after which the probe was retracted (indicated by arrow) to 400 nm above the bevel surface for the remainder of the scan. Although the average photocurrent remained relative unchanged, the far-field contrast was significantly diminished.

4. Conclusions

The near-field scanning optical microscope has been successfully used to evaluate the photoresponse distribution with the high degree of spatial resolution needed for nano-crystalline silicon devices. The resolution and sensitivity was dramatically enhanced by performing the NPC measurements on a beveled surface. The use of a beveled device also complemented the inherent sensitivity of the near-field microscope to the near-surface region, making it a viable approach for evaluating the collection uniformity at different depth along the film thickness.

Acknowledgments

The authors thank C.E Richardson from the California Institute of Technology for providing the samples used in this paper.

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Lamp-based Processing Technologies for Silicon Solar Cell Manufacturing

Nuggehallli M. Ravindra[1], Bhushan Sopori[2] , Anthony T. Fiory[1], Sudhakar Shet[1], Chuan Li[1], Rene D. Rivero[1] & Vincent Agnihotri[3]

[1]New Jersey Institute of Technology, Newark, New Jersey 07102
[2]National Renewable Energy Laboratory, Golden, Colorado 80401
[3]Corporate E Solutions, Franklin Lakes, New Jersey 07417

Abstract

Lamp-based processing technologies for the manufacture of silicon solar cells are described here. Two particular process technologies, namely rapid thermal processing and optical processing techniques, are considered. While reducing the cost of manufacturing of silicon solar cells, these technologies are anticipated to increase efficiency and throughput of silicon solar cells and lower energy utilization for cell fabrication.

Introduction

The State of New Jersey is expanding its commitments and support of solar cell activities. Recently, the New Jersey Board of Public Utilities (NJBPU) voted to approve new regulations which expand the State's Renewable Portfolio Standard (RPS) by extending the existing goals out to 2020 and increasing the required amount of renewable energy and solar energy [1]. Under the newly adopted regulations, 20 percent of New Jersey's electricity must come from renewable sources by 2020. The new regulations also include a 2-percent solar set aside which is forecast to require 1500 MW, the nation's largest solar commitment relative to population and electricity consumption. In addition to extending the RPS to 2020, the revised regulations also require the electricity produced by New Jersey solar photovoltaic systems to increase to 2 percent by 2020. This new solar goal will expand New Jersey's solar market from 90 MW to be installed by 2008 to 1500 MW of solar electricity by 2020.

New Jersey is one of the fastest growing solar markets in the country, having grown from six solar installations in 2001 to over 1,200 today. The new goal will continue to spur market development and is considered to be the largest solar goal in the country on a per capita basis exceeded only by California.

Figures 1 and 2 summarize the projected growth of photovoltaic (PV) power production in the State of New Jersey [2].

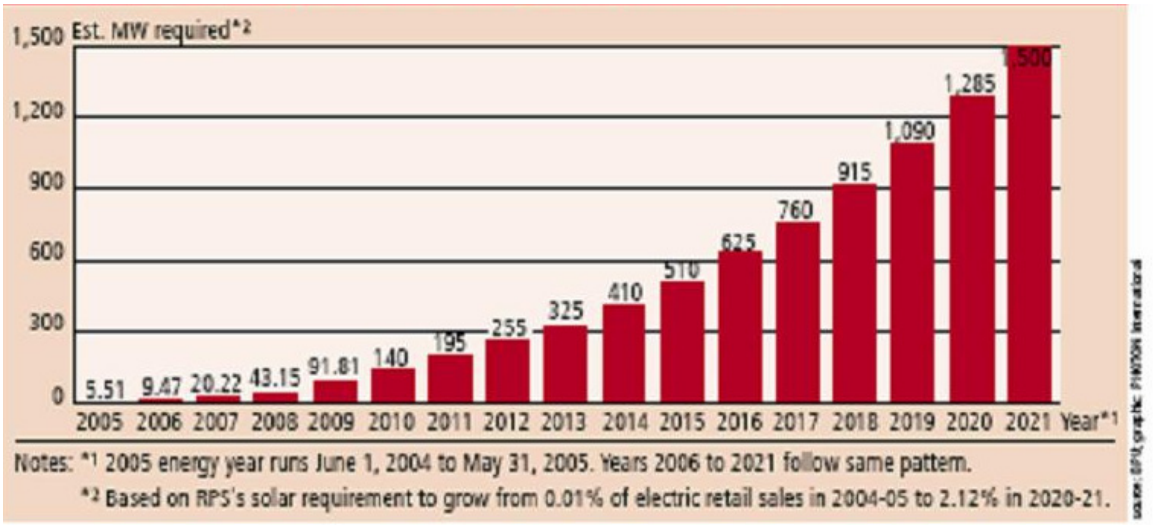

Figure 1 – Cumulative PV target of 20% Renewable Portfolio Standard (RPS) of the State of New Jersey [2].

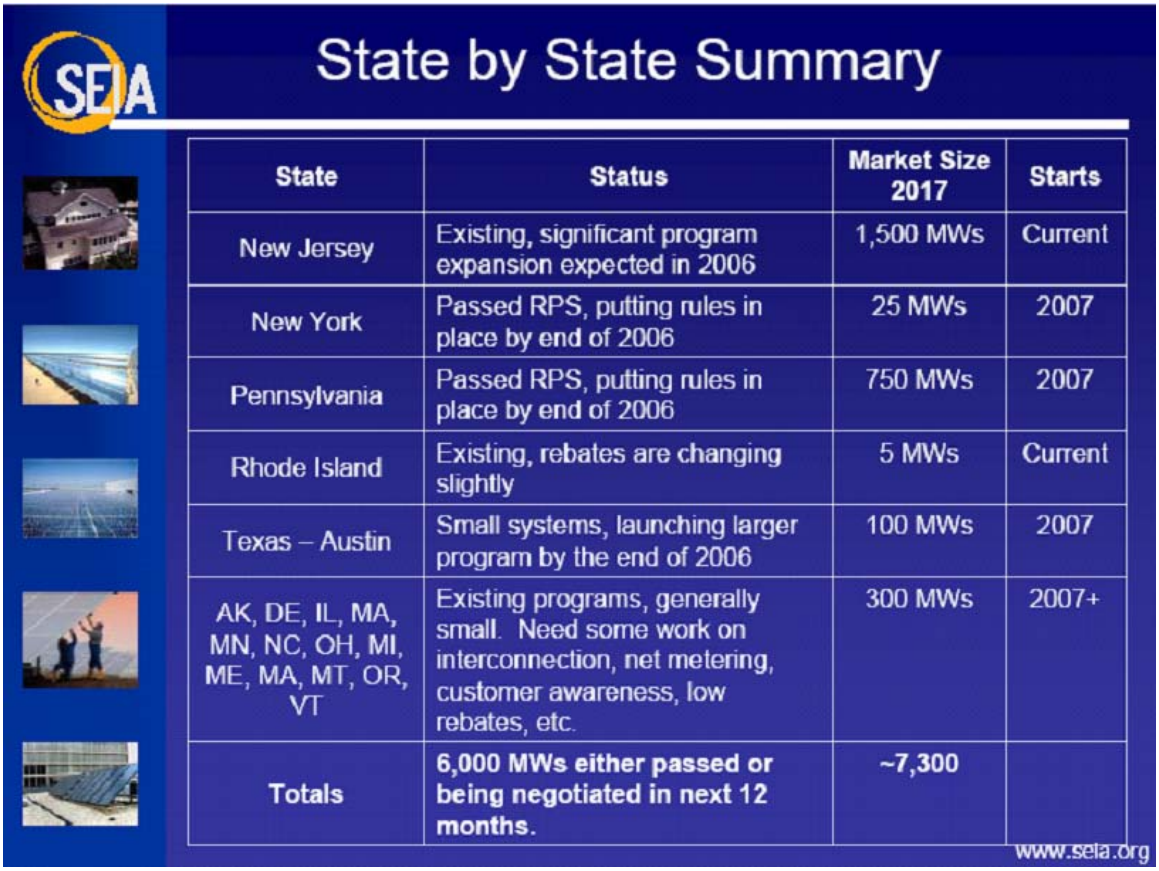

Figure 2 – State-by-State comparison of projected PV power production [2]

The silicon technology has dominated the PV industry since the invention of the crystalline silicon solar cell in 1954 [3]. In 2005, about 65% of all solar cells were made from polycrystalline or multicrystalline silicon, 24% from monocrystalline silicon and 4% from ribbon silicon [4]. While conversion efficiencies as high as 24.7% have been obtained in the laboratory for silicon solar cells, the best efficiencies for commercial PV modules are in the range of 17% to 18%. A number of companies are commercializing solar cells based on other materials such as amorphous silicon, microcrystalline silicon, cadmium telluride, copper-indium-gallium-diselenide (CIGS), gallium arsenide (and related compounds) and dye- sensitized titanium oxide [4].

In general, the goals of current solar cell research and manufacturing for a cost-effective approach include the following [5]:

- Utilize less silicon by making thinner cells;
- Deploy less expensive silicon, which may consist of large concentrations of impurities and defects;
- Improve solar cell performance with reproducible properties and high yield using inexpensive silicon;
- Increase speed and throughput of manufacturing processes;
- Simplify processing steps (this reduces fabrication costs and increases the yield) and reduce equipment costs;
- Implement improved methods to match solar spectrum with photo-generation of carriers.

In order to achieve the above objectives, the New Jersey Institute of Technology, in collaboration with the National Renewable Energy Laboratory and Corporate E Solutions is pursuing activities focused on deploying lamp-based techniques for enhancing silicon solar cell efficiencies and for subsequent implementation in the manufacturing sector.

Rapid thermal processing

Rapid thermal processing (RTP) has emerged as a key manufacturing technique for semiconductor device fabrication [6]. This has particular relevance for complementary metal oxide semiconductor (CMOS) technology, for process steps such as implant annealing, oxidation, source and drain contact junctions, shallow-extension junctions between the channel and the contacts, and electrically active polycrystalline-silicon gate electrodes [7]. The most general definition of RTP is a tool enabling rapid thermal cycles which cannot be performed with conventional quartz tube furnaces. In particular, conventional furnace processing restricts the maximum heating and cooling rates to several K/min and the minimum process time to several minutes. These restrictions are imposed by the high thermal mass of the system as well as the way the energy is transferred to the wafers.

In contrast, RTP offers the possibility to apply heating and cooling rates up to several hundred K/s and to conduct processes in the range of 10^{-8} to 10^{1} s [8]. This can be achieved because each wafer is heated individually and uniformly. Naturally, RTP tools have to make use of a fast method of transferring energy to and away from the wafer. Hence, energy sources based on radiation are used. These include lasers, electron and ion beams, and incoherent light from arc and tungsten halogen lamps [9].

Most RTP machines use tungsten halogen lamps (THL) as a source of radiative energy. Usually, this type of lamp consists of a linear double-ended quartz tube around a tungsten filament that is heated resistively. The quartz transmits the entire spectrum emitted by the filament up to an absorption wavelength of 4-5μm. The quartz envelope is filled with halogen gas to increase the filament's temperature and lifetime [9]. A THL shows a spectral intensity distribution close to that of a Planck's body with a color temperature of 2000 to 3000 K depending on the lamp current [9].

All objects at a temperature T above absolute zero emit electromagnetic radiation due to thermal motion of atoms and molecules. The spectral radiant distribution M (λ, T) is described by Planck's law [10]:

$$M(\lambda, T) = \epsilon(\lambda, T)\ \frac{2\pi hc^2}{\lambda^5}\frac{1}{\exp(hc/k\lambda T) - 1}$$

where λ is the wavelength, *k* is the Boltzmann´s constant, *h* is Planck's constant, and *c* is the velocity of light. The spectral emissivity, $\varepsilon(\lambda, T)$, is equal to unity only in the case of an ideal black body. For a so-called grey body, $\varepsilon(\lambda, T)$ is a constant between 0 and 1, i.e. independent of λ and *T*.

For very large scale integration (VLSI) circuit processing, RTP has evolved from low-ramp-rate/high-temperature for a short time to high-ramp-rate/high-temperature for ~ zero second (spike) anneals. These considerations necessitate that RTP systems be capable of very high power-density illumination, active cooling, and thermal compensation for edge-radiation losses of the process wafer. With the advent of 300-mm-diameter, double-side polished wafers in the silicon integrated-circuit (IC) industry, the problems relating to temperature non-uniformity across the wafer seem to have been minimized. However, local temperature variations can occur because of the variable emissivity across the IC patterns on the wafer [11]. In spite of the International Technology Roadmap for Semiconductors (ITRS) [12] forecasting disruptive changes in future process technologies, rapid thermal annealing (RTA) appears to be viable to at least the 60-nm node [13].

Recently, RTP-like processing has found applications in another rapidly growing field — solar cell fabrication [14]. RTP-like processing, in which an increase in the temperature of the semiconductor sample is produced by the absorption of the optical flux, is now used for a host of solar cell fabrication steps, including phosphorus diffusion for N/P junction formation and impurity gettering, hydrogen diffusion for impurity and defect passivation, and formation of screen-printed contacts using Ag-ink for the front and Al-ink for back contacts, respectively.

The demands on an RTP system for solar cell fabrication are quite different from those for traditional microelectronics applications. Here, the primary emphasis is on throughput and cost. These major considerations have resulted in RTP systems being belt-type, IR systems, which use THLs to illuminate the wafers from one side [14].

The need for low-cost equipment and high throughput (600 wafers/hour) has some ramifications for process uniformity, with concomitant implications for the device performance. Process non-uniformities in solar cell fabrication arise from several sources:

1. Commercial Si solar cells use low-cost, multicrystalline wafers. These wafers are chemically textured to minimize surface reflectance. However, because texturing is orientation dependent, grains of different orientations have different reflectance and light-scattering properties, resulting in variations in emissivity from grain to grain. Thus, even for blanket diffusions for formation of an N+ junction in an unpatterned wafer, the RTP process can have spatial temperature variations.

2. In a patterned wafer (e.g., metallization anneal) there can be thermal non-uniformities introduced by large pattern dimensions [15]. Solar cell metallization has typically 75–100 μm grid lines and 1 mm bus bars.

Furthermore, screen printed metal is 25–50 μm thick. Thermal mass and optical shadowing causes large lateral variations in the temperature. Thus, one of the common problems in the RTP of Si devices arises due to local variations in the emissivity of the wafer [15]. These variations can greatly influence solar cell performance.

OPTICAL PROCESSING

Optical Processing uses spectrally selected light to create a local melt at an illuminated semiconductor-metal (S-M) interface [16]. The thickness of the melt can be tailored by controlling the energy delivered to the device. This local melt forms an alloyed region that regrows epitaxially on the silicon substrate to form an Ohmic contact of extremely low contact resistivity. The energy delivered to the cell can also produce bulk heating to induce other predetermined thermal effects.

The interface reaction is strongly diminished if the S-M interface is not directly illuminated.

The optical processing furnace [OPF] consists of a quartz muffle that is illuminated from above by THLs. The optics of the light sources is designed so that the illumination in the process zone is highly uniform. Process gases such as Ar, N_2, and O_2 are regulated to flow through the furnace. The walls of the muffle are maintained cold by flowing N_2 along the outside walls of the muffle. The spectrum, intensity, and duration of the incident flux are chosen for a specific application. The OPF system is shown in Figure 3. It consists of an optical processing furnace, power controller and on-line data acquisition system.

Optical Processing and RTP differ in the basic mechanisms involved. In Optical Processing, the reaction occurs predominantly at the illuminated interface; the same reaction rate is reduced if the interface is masked. In contrast, a typical RTP is a thermal process that cannot discriminate between the front and the backside of the cell since such a process is completely thermally controlled [17, 18].

ADVANTAGES OF OPTICAL PROCESSING

Since heat in melting initiates at the interface (and can be confined to a thin region at the interface), the effect of the impurities in the ambient gas(es) on the characteristics of the contact is minimal compared to either furnace processing or RTA. In optical processing, the surfaces of the Al contacts typically remain shiny and do not require further preparation for additional metallization, such as solder dip. Optical processing is a “cold wall“ process, which minimizes the impurity out-diffusion as well as permeation from furnace walls. The process results in large-area uniformity of the alloyed sintered layers. This feature is evidenced by the fact that the Si-Al contacts produced are free from the ”spikes” and pitting produced by other processes. The process requires much less power than furnace or RTA (particularly when the cell has an anti-reflection coating). The process is rapid, has high throughput, and can make devices with unique characteristics. The process requires fewer steps than conventional approaches and results in significant cost savings [14].

The applications of optical processing are as follows:

- Simultaneous fabrication of front and back electrical contacts for semiconductors;
- Precise design of interfaces to either reflect or absorb light and to have either smooth or rough surfaces;
- Transformation of low-cost fine-grain amorphous or multicrystalline silicon to an improved morphology;
- Growth of high-quality, low-cost thin-film silicon oxides for solar cells, computer memory chips, or other uses.

Figure 3 - OPF system at NREL.

Conclusions

Lamp based semiconductor process systems such as RTP and Optical Processing have been described in brief. The applications of optical processing to solar cell fabrication steps have been summarized. Some of their advantages have been identified.

Acknowledgements

The partial financial support of the US Department of Energy is acknowledged with thanks. The authors appreciate very much the support of Dr. Donald Sebastian and Ms. Judith Sheft of the New Jersey Institute of Technology.

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Residual Stress and Its Relationship to Dislocation Density in EFG Silicon

F. Li, V. Garcia, S. Danyluk*
The George W. Woodruff School of Mechanical Engineering
Georgia Institute of Technology

I. Tarasov, S. Ostapenko
Nanomaterials and Nanomanufacturing Research Center
University of South Florida

D. Yates
SCHOTT Solar, Inc.

July 24, 2006

1. Introduction

This brief note presents some recent work on developing a correlation between the in-plane residual stresses in EFG wafers and the dislocation densities obtained by an etching and optical imaging technique developed at NREL. Our work has involved the use of a full field near-IR polariscope to image stresses [1,2,3] in 4 x 4 inch EFG wafers, etch, optically image and obtain the surface area of dislocation etch pits of these same wafers, and compare the images. Line scans through the images were used to obtain a quantified measure of the stresses and etch pits.

2. Polariscope Configuration

The Georgia Tech polariscope system is shown as Figure 1, which consists of two polarizers, two wave plates, a digital camera, and a narrow band infrared filter (not shown). Two 10-inch lenses are used to get collimated beams of light through the optics and the sample. A point source is located on the focus of the first big lens.

* steven.danyluk@marc.gatech.edu

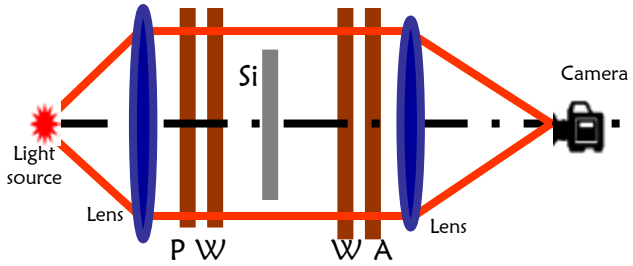
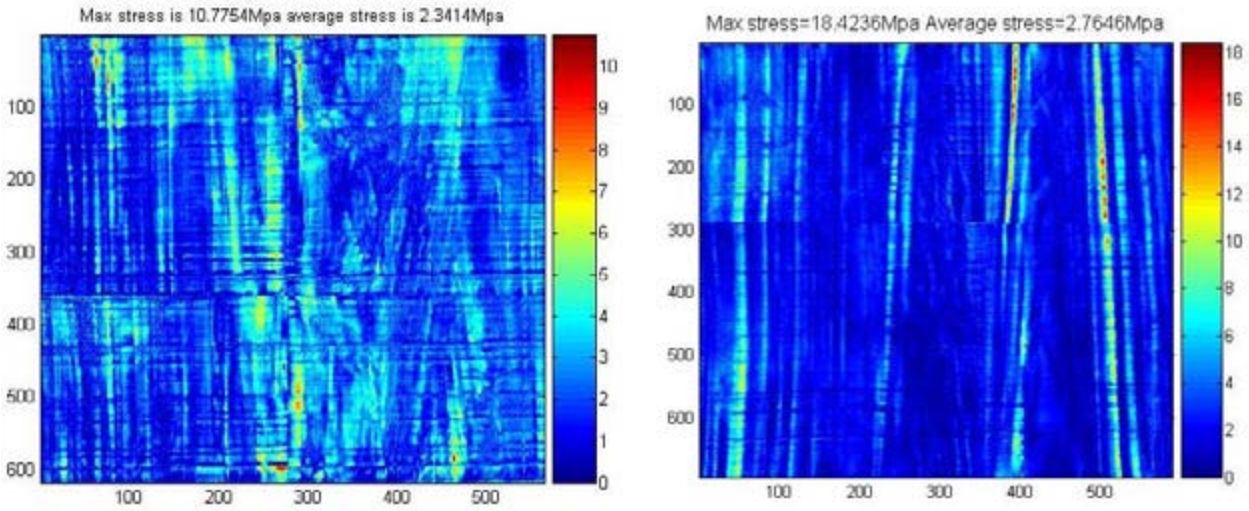


Figure 1. Near IR polariscope system.

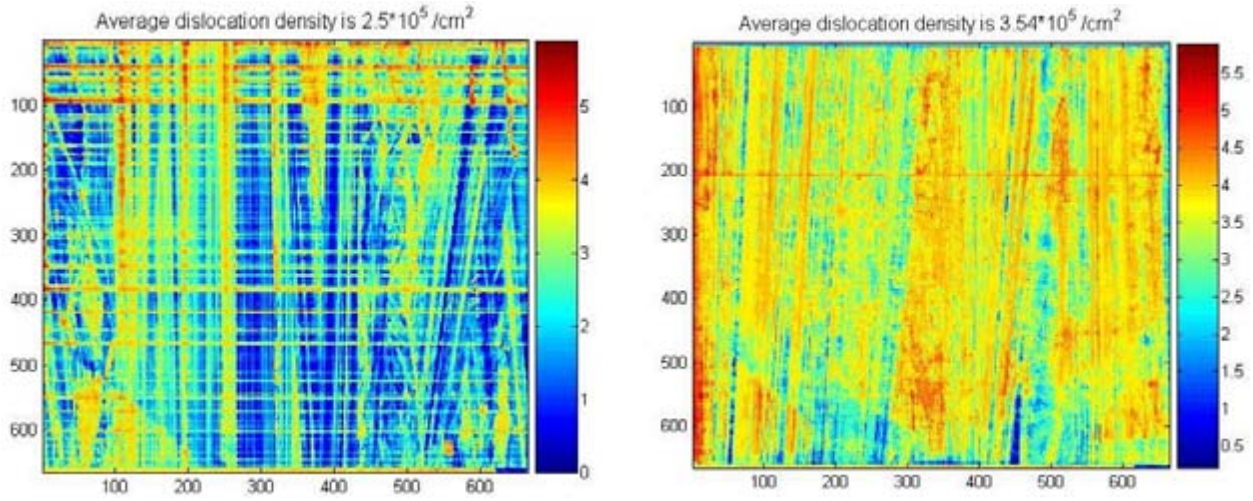
The silicon is placed at the center of the system and the collimated light passes through the sample and the transmitted light is recorded by a camera. The difficulty with this measurement is that the silicon is approximately 250μm thick so that the change in transmitted light is minute. We have used various techniques such as phase stepping and light amplification to enhance the system sensitivity. The references describe some details of these techniques [3,4]. Images of the Principal normal and shear stresses have been obtained as shown in Figure 2 for two EFG wafers.



(a) EFG1 (b) EFG2

Figure 2. Principal shear stresses in two EFG wafers.

Both wafers were then etched and imaged using the PVSCAN system and Figure 3 shows these images.



(a) EFG1 (b) EFG2

Figure 3. Dislocation density maps of wafers EFG1 and EFG2 obtained by PVSCAN.

Wafer EFG2 was also optically imaged in regions of the low and high shear stress and this is shown in Figure 4.

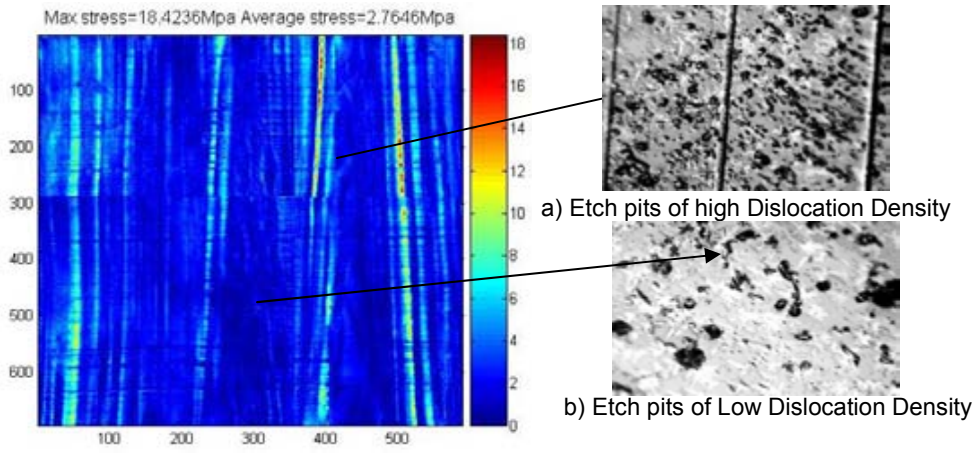
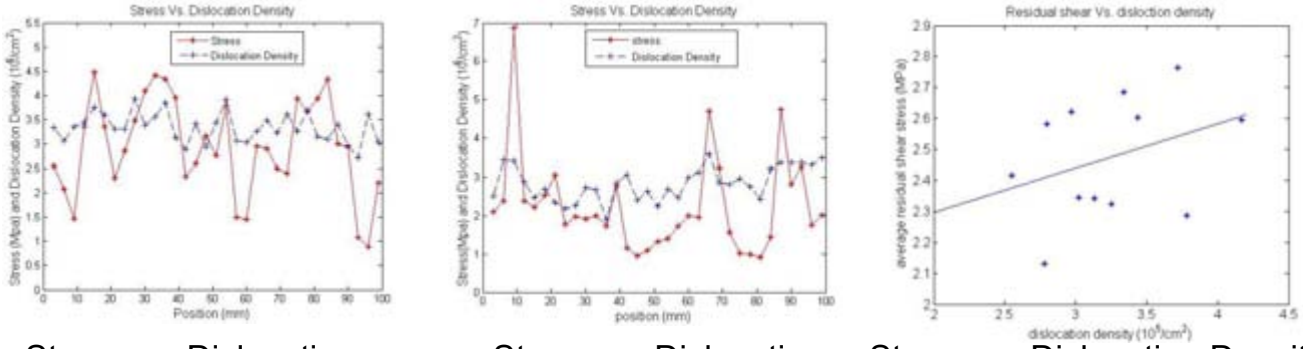


Figure 4. Principle shear stress and optical images of the etch pits in the low and high stress regions.

3. Quantitative Analysis

A perusal of the images of Figures 2, 3 and 4 lead one to believe that there is a correlation between the dislocation densities and the residual stresses and we have attempted to quantify this relationship by examining line scans at specific regions along

the growth direction. Figure 5 shows a line scan through effectively the same location of both samples and the stress versus dislocation density for these scans.



Stress vs. Dislocation (Transverse Scan of EFG1)

Stress vs. Dislocation (Transverse Scan of EFG2)

Stress vs. Dislocation Density (comparing among samples)

Figure 5. Line scans of stress versus dislocation for EFG1 and EFG2.

As can be seen, the correlation cannot be firmly established at this time; although the images of Figures 2, 3 and 4 do correlate qualitatively.

4. Conclusion

Residual stress and dislocation density has been measured in two thin flat EFG silicon wafers and the relationship between residual shear stress and dislocation density can be complex. Roughly speaking, there might be a linear relation between them.

5. Acknowledgments

This project is supported by NREL under contract #B01-6D0. The authors would like to thank Rick Matson at NREL and SCHOTT Solar, Inc.

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Carbon-Oxygen Interactions in Silicon

Daniel J. Backlund and Stefan K. Estreicher

Physics Department, Texas Tech University, Lubbock, TX 79409-1051

Abstract: The most abundant light impurities in p-type Si solar cells are boron, oxygen, and carbon. It is well known that the interactions between B and O lead to the formation of electrically active complexes involving either interstitial B (B_i) and interstitial O (O_i), in space-based devices, or $\{O_i,O_i\}$ dimers and substitutional B (B_s), in terrestrial devices. Under the same conditions, C_i interacts with O_i or C_s, while $\{O_i,O_i\}$ interacts with C_s. We report here on preliminary results of systematic studies involving carbon-oxygen interactions in silicon.

1. Introduction

The efficiency of boron-doped silicon solar cells is limited by the presence of impurities and native defects in the material. Some impurities are desirable or harmless when isolated, such as substitutional boron (B_s) or carbon (C_s), or interstitial oxygen (O_i). However, these impurities diffuse, form complexes, and become electrically active during the processing of the device, irradiation or, over time, under normal operating conditions of a solar cell. Impurity complexes often reduce the performance of the device. In space-based solar cells, irradiation causes B_s and C_s to become the rapidly-diffusing interstitials B_i and C_i, respectively. These trap at B_s, C_s, or O_i. In particular, the $\{B_i,Oi\}$ complex [1] is an unwanted recombination center. In terrestrial solar cells, the fast-diffusing oxygen dimer $\{O_i,O_i\}$ traps at B_s [2]. The resulting complex noticeably reduces the performance of the cell.

Experimental studies in Si samples containing high concentrations of O and C have shown that a number of electrically and optically active complexes containing these impurities readily form at moderate temperatures. C_s interacts with O_i and with the $\{O_i,O_i\}$ dimer. The reaction of C_s with a Si self-interstitial (I) generates the fast-diffusing C_i center. This impurity interacts with C_s and forms stable $\{C_s,C_i\}$ pairs. C_i also interacts with O_i and forms the $\{C_i,O_i\}$ pair. The latter is a strong trap for I's as well as with H interstitials. The successive reactions which occur as a function of annealing time and temperature can be monitored experimentally by techniques such as DLTS, FTIR, or photoluminescence (PL) [3-5]. However, the precise identification of the resulting defects, their energetics and chemical activities, require theoretical studies.

In this paper, we discuss the preliminary results of systematic first-principles calculations involving the simplest complexes of carbon and oxygen in Si. The results accumulated so far include the structures, energetics, and vibrational spectra of O_i and the $\{O_i,O_i\}$ pair, C_s and C_i, the $\{C_s,C_i\}$, $\{O_i,C_i\}$, and $\{O_i,C_s\}$ pairs, in various charge states. Several additional structures involving C and O, and estimates of electrical activities are still under way.

2. Theoretical background

Our results are obtained with first-principles, self-consistent density functional theory coupled to molecular-dynamics simulations, as implemented in the SIESTA package [6]. The host crystal is represented by periodic 128-host atom supercells. At this stage, the *k*-points sampling is limited to k=0. Tests with more complete k-point samplings [7] will be performed at a later stage. The exchange-correlation potential is that of Ceperley-Alder [8] parameterized by Perdew-Zunger [9]. Ab-initio pseudopotentials in the Kleinman-Bylander [10] form are used. The basis sets for the valence states are (numerical) linear combination of atomic orbitals. We use double-zeta

(DZ) basis for first and second row elements such as H, B, C, and O. The 47 Si atoms around the center of the supercell have an additional set of polarization functions (DZP). The remaining 81 Si atoms have only a DZ basis. The atoms remain at essentially undistorted substitutional sites even after a full relaxation of the various complexes. The CPU time varies as the N^3, where N is the total number of basis functions in the system. Having all the Si atoms with a DZP basis would increase N by 405 and substantially slow down the computations.

The geometries are optimized with conjugate gradients down to maximum force components smaller than 0.003eV/Å, a level of accuracy required for the calculation of dynamical matrices. The energies of the final configurations are compared to those of the dissociated species to get binding energies. The vibrational spectra are obtained from linear response theory [11].

3. Results

The O_i, C_s, and C_i defects:

Interstitial oxygen is a very well characterized impurity since the 1950's [12,13]. O_i sits at a slightly puckered bond-centered (BC) site. Its asymmetric stretch at 1136cm^{-1} (present calculations: 1161cm^{-1}) is one of the best-know IR line in Si. The wag modes, which we find to be at 168cm^{-1}, have not been directly observed. The activation energy E_a for diffusion of O_i is about 2.6eV [12]. Around 450^{o}C, $\{O_i,O_i\}$ pairs form. They diffuse much faster than O_i, with E_a~1.5eV [12,13]. C_s is electrically inactive. It is characterized by a local vibrational mode (LVM) at 607cm^{-1} [14] (present calculations: 602cm^{-1}). Finally, C_i has an acceptor (E_c-0.10eV) and a donor (E_v+0.28eV) levels [15]. It has a split-<001> configuration with C_{2v} (monoclinic I) symmetry in all the -1, 0, and +1charge states [16]. The +1 and -1 states have been seen by electron paramagnetic resonance (the G12 and L6 centers, respectively) [17]. C_i has two IR-active LVMs at 920 (A_1) and 931cm^{-1} (B_1) with intensity ratios 2:1 [18] (our calculations show LVMs at 969 and 903cm^{-1} and a pseudoLVM at 165cm^{-1}). C_i is associated with a PL band with a zero-phonon line (zpl) at 856meV [19].

The $\{C_s,O_i\}$ complex:

In the neutral charge state, the reaction $C_s + O_i \rightarrow \{C_s,O_i\}$ releases 0.53eV. Since O_i is not mobile under 450^{o}C, the $\{C_s,O_i\}$ is not very likely to form in Si solar cells under normal operating conditions.

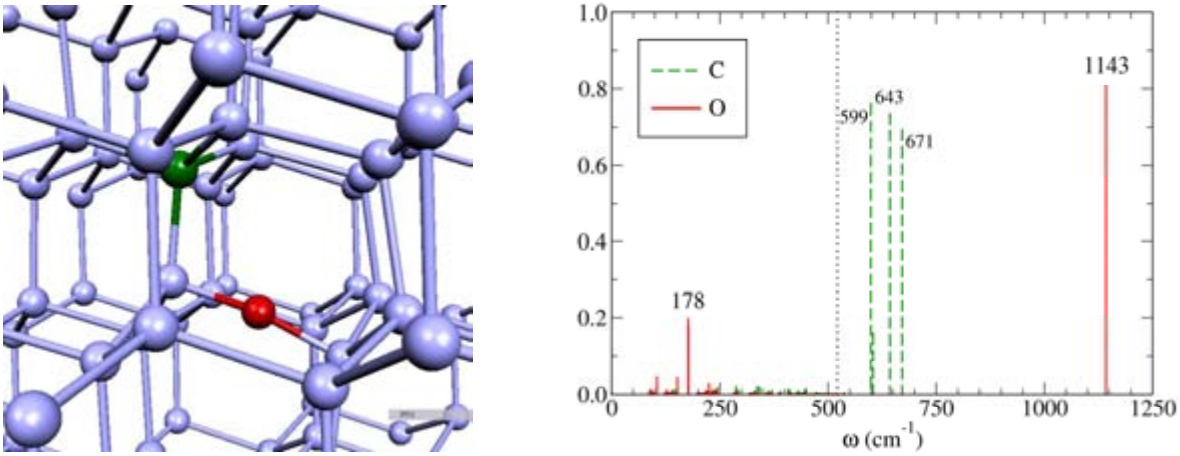

Fig. 2: The equilibrium structure of the $\{C_s,O_i\}^0$ complex (left) and the vibrational modes associated with it (right). The relative amplitudes of the oscillations of C (green dashed lines) and O (red solid line) are given.

The $\{C_i,O_i\}$ complex

This is the most studied C-O pair in Si. It has an acceptor level at E_c-0.53eV [20]. EPR studies (the 'G15 center') [21] show that the ^{13}C hyperfine tensor is very similar to that of isolated C_i. The complex has C_{1h} symmetry. The G15 center correlates with a DLTS donor level at E_v+0.38eV [22] and a PL band with zpl at 0.79eV ('C-line') [21,23]. There is also a correlation with a sharp LVM at 865cm^{-1}. The FTIR spectrum [24] also shows a line at 1116cm^{-1} as well as weak lines at 742, 550, and 529cm^{-1}. The defects anneals out at 350-450^{o}C. Two groups have studied this center using H-saturated clusters with localized basis sets [25] and 64 host atoms supercells with plane waves [26]. Our results generally agree with their predictions.

In the q = +1, 0, and -1 charge states, the reaction $C_i^q + O_i^0 \rightarrow \{C_i,O_i\}^q$ releases 1.70, 1.63, and 1.07eV, respectively (there exists a metastable configuration of the $\{C_i,O_i\}^-$ complex, 0.37eV higher in energy). The structure of the neutral pair and the vibrational spectrum associated with it are shown below. Note that the highest LVM, calculated at 1119cm^{-1} (measured: 1116cm^{-1}), is a C-Si stretch mode and involves no O motion. This is consistent with the absence of ^{18}O isotope shift for this line. The 859cm^{-1} line (measured: 865cm^{-1}) is also C related. The highest frequency associated with O is calculated to be at 781cm^{-1}.

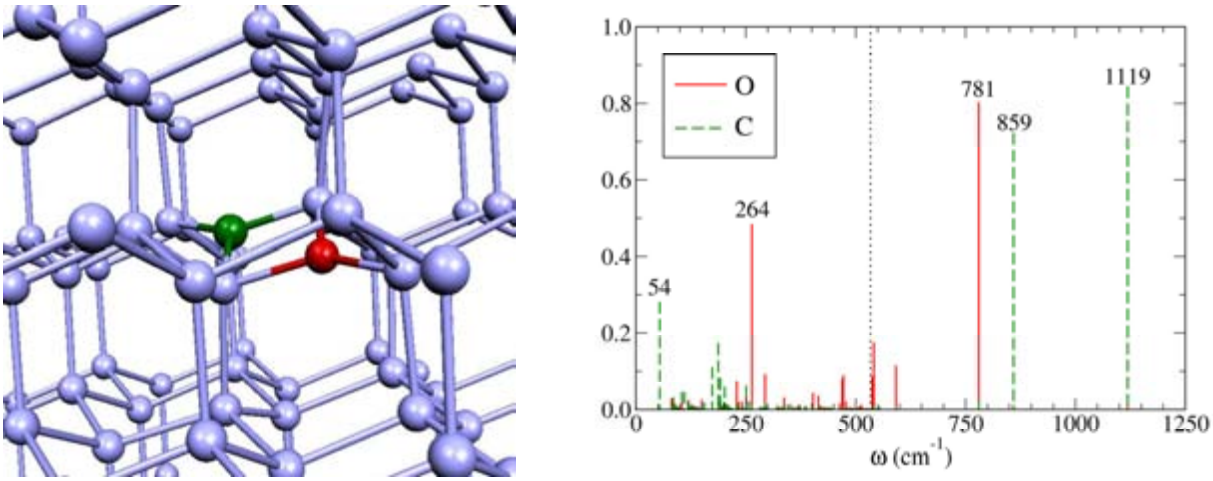

Fig. 3: The equilibrium structure of the $\{C_i,O_i\}^0$ complex (left) and the vibrational modes associated with it (right). The relative amplitudes of the oscillations of C (green dashed lines) and O (red solid line) are given.

4. Summary

We have initiated systematic calculations of C-O interactions in Si. The structures, binding energies, and vibrational spectra of various defect complexes are reported here, but the results are still preliminary, as a number of calculations have yet to be finished. The approximate positions of electrically active gap levels have yet to be calculated. More details will be reported at a later date.

Acknowledgements

This work is supported in part by a contract from NREL and a grant from the R.A. Welch Foundation.

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Observation of Impurities in Cast-grown Polycrystalline Silicon Substrates

Koji Arafune*, Hitoshi Sai, Yoshio Ohshita, Masafumi Yamaguchi
Toyota Technological Institute, 2-12-1 Hisakata Tempaku, 468-8511 Nagoya JAPAN
* E-mail : ara@toyota-ti.ac.jp

1. Introduction

The photovoltaic market is rapidly growing, and about 1.8GW PV modules were produced in 2005. This rapid growth leads to shortage of silicon feedstock. Even though silicon feedstock manufactures are increasing production, the rate of production increase will not be enough for demand. Therefore, it is necessary to consider usage of metallurgical-grade-silicon (MG-Si) feedstock. To produce high-quality polycrystalline silicon (pc-Si) ingots using MG-Si feedstock, it is important to understand what occurs during the solidification.

In this study, pc-Si ingots were grown by the conventional directional solidification technique, and the impurities in grown ingots were evaluated by several techniques.

2. Experiment

The pc-Si ingots were grown in the directional solidification furnace as shown in Fig.1. Solar grade silicon with boron as p-type dopant was melted in the quartz crucible coated with Si_3N_4. To solidify the silicon melt from the bottom to the top, the heaters were moved upward at a constant rate, V_H=15, 30, 60mm/hr. The ingots grown at V_H=15, 30, 60mm/hr were named C15, C30, and C60, respectively. The grown ingots were cylindrical shape with a diameter of 10cm and a height of 10cm. The ingots were vertically cut into two pieces. One piece was horizontally sliced to a thickness of 0.5mm for lifetime and impurities measurements, and the other was for observation of grains. The sliced substrates were etched with a solution of HNO_3 and HF to remove saw damaged layers. The minority carrier lifetime was measured by the laser/microwave photoconductance decay (μ-PCD) method. During the lifetime measurements, substrates were passivated with iodine-ethanol (0.1mol/L) solution. Fourier transform infrared spectroscopy (FT-IR) was used to evaluate dissolved carbon in the ingots. Precipitates of impurities were observed by scanning electron microscope (SEM) and analyzed by energy-dispersive X-ray spectroscopy (EDS).

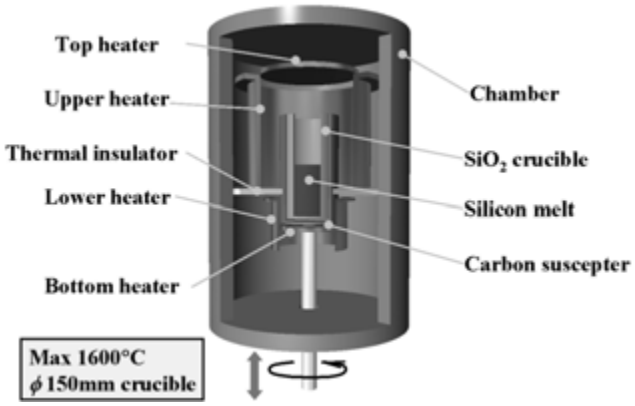

Fig.1 Schematic drawing of directional solidification furnace

3. Results and Discussion

Figure 2 shows the cross-sectional view of the C30 ingot. The grain size at the bottom of the ingot is relatively large, however, many small grains appear at the middle to the top of the ingot.

The cross-sectional views of the C15 and C60 ingots show similar tendency with that of the C30 ingot. The region in which small grains appear increases with increasing V_H. The substitutional carbon concentrations were evaluated by FT-IR measurements. The distributions of substitutional carbon concentration, C_S, as a function of fraction solidified were shown in Fig.3. Since the segregation coefficient of carbon is less than unity, the concentrations of each ingot increase in the bottom region, and reach at the constant values corresponding to the solubility limits. However, the constant value is different in each ingot. It is known that the segregation coefficient has a strong correlation to the solubility limit. Therefore, the difference in effective segregation coefficients causes the different constant value. If the carbon level exceeds the solubility, SiC precipitates may form and lead to multicrystalline growth. To find SiC precipitates, backscattered electron images were obtained. In the region that consists of small grains, needle-like precipitates were found at the grain boundaries. Figure 4 shows the backscattered electron image around the precipitates and corresponding impurities distributions analyzed by EDS. Not only carbon compounds but also nitrogen compounds were observed. From the compositional analysis, the carbon and nitrogen compounds seem to be SiC and Si_3N_4, respectively. Since the origin of Si_3N_4 precipitates is coating material for a quartz crucible, the number of Si_3N_4 precipitates can be reduced by decreasing the ratio of coating area to ingot volume. Therefore, to avoid the appearance of small grains, it is important to reduce precipitation of SiC. From this point of view, we developed new growth method, named as the Successive Relaxation of Supercooling (SRS) method [1]. The concept of this method is to suppress thermal and constitutional supercooling, and to enhance the removal of

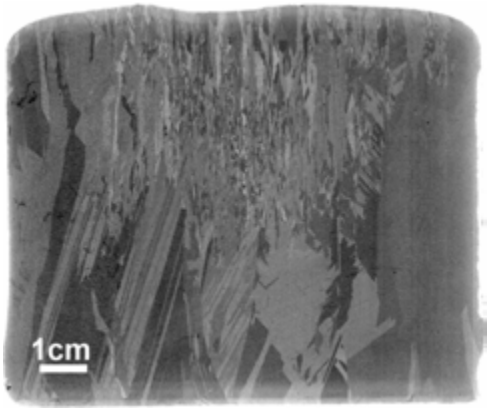

Fig.2 Cross-sectional view of C30 ingot

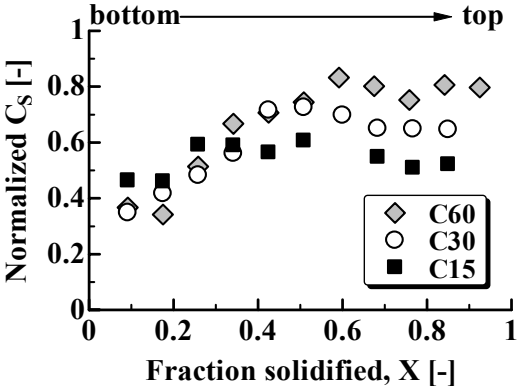

Fig.3 Normalized substitutional carbon concentration as a function of fraction solidified.

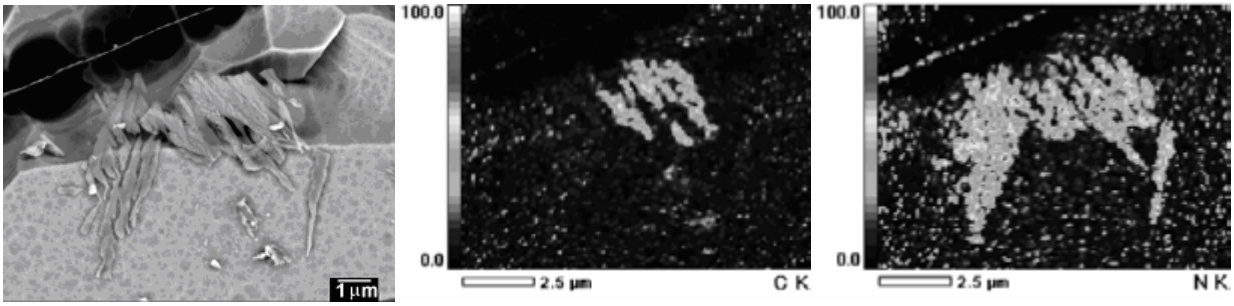

Fig.4 Precipitates at the grain boundary. Backscattered electron image (left) and impurities distributions (center : carbon, right : nitrogen)

impurities by segregation. The number of small grains in the SRS ingot was extremely decreased, and in addition, the lifetime, etch-pit density, and substitutional carbon concentration of the SRS ingot were also improved.

It is known that even low concentration of iron can cause a marked deterioration in silicon-based solar cells. Some of the iron are incorporated from the silicon feedstock and others arise during the growth of silicon ingots and the cell processes. It is important to understand and control defects related to iron atoms so that the performance of polycrystalline silicon solar cells can be improved. Therefore, we measured iron distributions before and after gettering by the X-ray microprobe fluorescence (μ-XRF) technique [2]. After gettering, remaining iron atoms were mainly trapped along the small angle grain boundary. To recognize the shape and size of iron precipitates, backscattered electron image was obtained around the iron trapped grain boundary as shown in Fig.5. Here, brighter the color in the image, the higher intensity of backscattered electrons. As can be seen, there are three bright spots along the grain boundary. To determine the element, characteristic X-ray spectra were measured at P1 (bright spot) and P2 (background) as shown in Fig.6. It is clear that iron atoms exist at P1. The size of iron precipitates were about 150nm in length and 30nm in width.

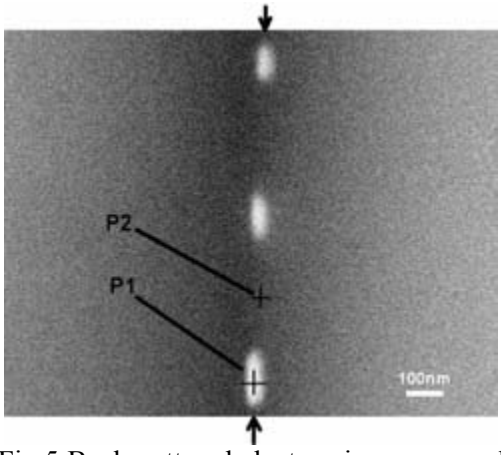

Fig.5 Backscattered electron image around small angle grain boundary. Arrows indicate grain boundary.

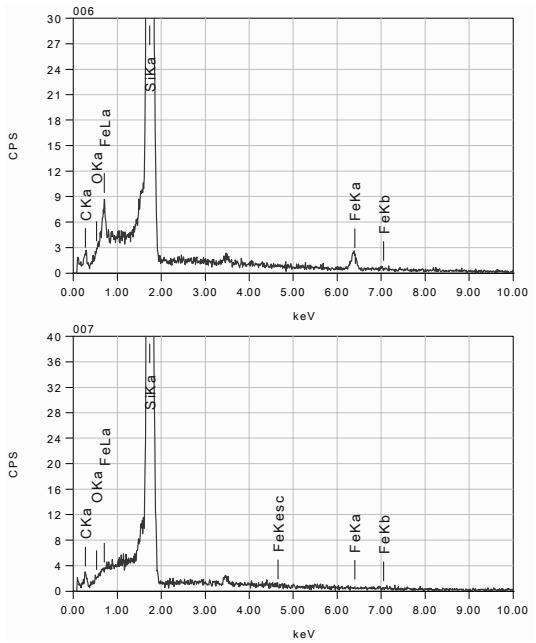

Fig.6 X-ray spectra measured at P1 (upper) and P2 (lower)

4. Summary

Polycrystalline silicon ingots were grown by the casting method. From the cross-sectional views of the ingots, there were many small grains in all ingots, and the region in which small grains appear increases with increasing V_H. In the region which consists of small grains, needle-like precipitates were found at the grain boundaries. From the compositional analysis, these precipitates seem to be SiC and Si_3N_4. We considered that precipitation of SiC leads to multicrystalline growth. To suppress the appearance of small grains, we developed SRS method. The number of small grains in the SRS ingot was extremely decreased compared with that in the ingots grown by conventional casting method. Regarding the metal impurities, synchrotron-based X-ray microprobe technique is strong tool for studying metal distribution. However, limited researchers can use the technique. In this study, we demonstrated that sub-micron size iron precipitates can be observed by SEM and EDS.

Acknowledgements

Part of this work was supported by "Academic Frontier" Project for MEXT (Ministry of Education, Culture, Sports, Science and Technology), 2002-2006.

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ANALYSING MULTIPLE DEFECT LEVELS IN SILICON BY TEMPERATURE- AND INJECTION-DEPENDENT LIFETIME SPECTROSCOPY (*T*-IDLS)

S. Diez, S. Rein and S.W. Glunz
Fraunhofer Institute for Solar Energy Systems ISE, Heidenhofstr. 2, D-79110 Freiburg, Germany
Phone ++49 761-4588-5263; Fax ++49 761-4588-9250, email: stephan.diez@ise.fraunhofer.de

ABSTRACT: The potential of temperature- and injection-dependent lifetime spectroscopy (*T*-IDLS) as a method to characterise point defects in silicon even with several energy levels is demonstrated. Lifetime measurements on an intentionally cobalt-contaminated wafer were performed at different temperatures up to 151 °C. Modelling these lifetime curves on basis of the Shockley-Read-Hall (SRH) statistics required two defect energy levels. A detailed analysis based on determination of the recently introduced defect parameter solution surface (DPSS) has been performed in order to extract the underlying defect parameters. A unique solution has been found for a deep defect level located in the upper band gap half at an energy level of E_C-E_t=0.38±0.01 eV with a corresponding ratio of capture cross-sections k=σ_n/σ_p=0.16. In addition, a deep donor level in the lower band gap half - known from the literature - could be assigned to an energy level within the DPSS analysis at E_t-E_V=0.41±0.02 eV with a corresponding ratio of capture cross-sections k=σ_n/σ_p=16±3. These results show that using DPSS analysis *T*-IDLS is a powerful method to characterise even multiple defect levels that are affecting carrier recombination lifetime in parallel.

1. INTRODUCTION

Due to the strong influence of material quality on the efficiency of solar cells, analysing recombination-active defects introduced during crystal growth and solar cell processing is an important task. Lifetime spectroscopy (LS) is a highly sensitive diagnostic tool to detect and identify impurities and defects in semiconductors like silicon. Compared to the well-established deep-level transient spectroscopy (DLTS), LS is particularly useful to analyse recombination-active defects, i.e. those affecting device performance. Injection-dependent lifetime spectroscopy (IDLS) on a sample at room temperature usually results in a broad range of defect energy levels E_t [1]. In order to increase the information on the defect characteristics and deal with the above limitation the recombination activity of the defect can be varied by performing lifetime measurements with samples of different doping level N_{dop} (N_{dop}-IDLS) or on one sample at different temperatures. The so-called temperature-dependent lifetime spectroscopy (TDLS) is based on such temperature-dependent measurements of carrier lifetime under low-level injection. The standard TDLS approach is capable to determine the energy depth but assumes temperature-independent capture cross sections σ_n and σ_p. Advanced TDLS overcomes this limitation by more sophisticated evaluation and modelling and allows increased spectroscopic information to be extracted. Combining the results of TDLS and room-temperature IDLS makes it possible to determine the defect energy level E_t and the ratio k:=σ_n/σ_p unambiguously [2, 3].

Increasing the information on the injection and temperature dependence by measuring injection-dependent lifetime curves at various temperatures should yield unambiguous spectroscopic results as pointed out within a theoretical study in Ref. [3]. In the literature [4], temperature- and injection-dependent lifetime spectroscopy (*T*-IDLS) was already performed with an experimental setup based on an apparatus intended for quasi-steady-state photoconductance (QSSPC) measurements. However, modelling of lifetime curves only resulted in a broad energy interval and thus did not allow the dominant defect level to be identified unambiguously. The most likely reason is that the covered temperature range was too small for the investigated defect to observe the turnover of the lifetime curves from an increasing to a decreasing shape. This is confirmed by another *T*-IDLS investigation which reached this turnover point and therefore allowed an unambiguous determination of a relatively deep single energy level [5].

2. EXPERIMENTAL PROCEDURE AND RESULTS

Addition of cobalt to the silicon melt before pulling a mono-crystalline Cz-Si crystal resulted in intentional contamination. The saw damage of the wafer was removed by an acidic etch. Resistance measurements based on the four-point probe technique were used to determine the doping concentration of the sample under investigation (N_A=1.1x10^{15} cm^{-3}), which is almost two orders of magnitude higher than the concentration of cobalt specified by the calculation from the manufacturer based on the segregation coefficient. The samples were passivated with a high-quality silicon nitride exhibiting surface recombination velocities as low as 10 cm/s prior to the carrier

lifetime measurements [3]. Reference samples without metal contamination were used to confirm the nitride quality and to ensure that resulting effective lifetime can be attributed to bulk defects.

T-IDLS-measurements were performed on an intentionally cobalt-contaminated *p*-type silicon sample using the well-established setup for QSSPC-technique with a photographic flash lamp [6]. A resistive element was used to heat the sample by means of a brass coil placed directly on top of the sample. The latter is built up from a system supplied by Sinton Consulting that was slightly modified. The injection-dependent lifetime curves are shown in Fig. 1a for temperatures up to 151 °C. Remeasuring the lifetime after this temperature cycle at room temperature yielded values coinciding with the initial curve at room temperature. This shows that the defect structure remained unchanged.

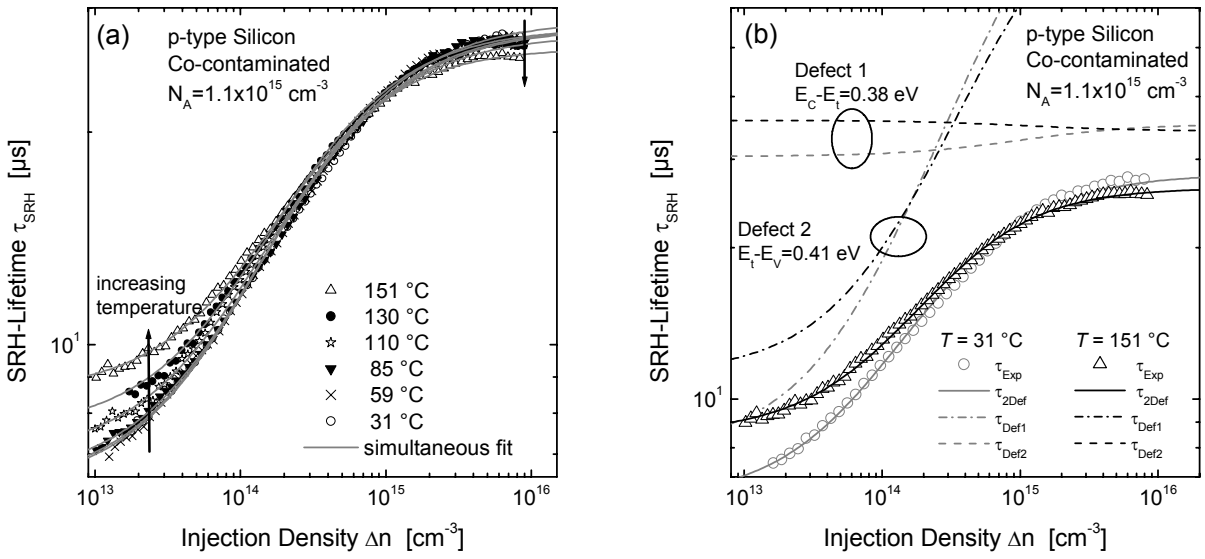

Fig. 1 (a) Injection dependence of the effective SRH lifetime measured on a Co-contaminated silicon wafer at different temperatures. The symbols represent the measured data. The solid lines represent a simultaneous fit with two defect levels whose parameters resulted from the detailed DPSS analysis (defect 1: E_C-E_t=0.38 eV, symmetry factor k= 0.16, defect 2: E_t-E_V=0.41 eV, symmetry factor k=16). (b) The measured SRH lifetime for the two extreme temperatures is plotted together with the lifetime curves for the two single defects (dashed, dash dotted) and their superposition (solid lines) whose characteristics resulted from the DPSS analysis. These curves are shown separately for 31°C (gray) and 151°C (black) respectively. Plotting SRH lifetime separately for the single defects reveals the dominance of defect 2 under low-level injection and the increasing influence of defect 1 with increasing injection level. Opposite to defect 2, the lifetime curves of defect 1 change from increasing to decreasing shape within the covered temperature range.

3. EVALUATION OF MEASUREMENTS AND DISCUSSION

For evaluation of the measured data, the temperature dependence of the carrier mobility has to be taken into account for calculating the injection level Δn from conductivity measurements [7]. Investigation of the lifetime curves to extract as much information as possible to characterise the underlying defects was performed by determination of the Defect Parameter Solution Surface (DPSS) which visualises the ambiguity of fit results of a single lifetime curve [3, 5]. The recombination lifetime attributed to a single defect was modelled by the standard SRH theory [8] with characteristic defect parameters being the energy level E_t, the electron capture time constant τ_{n0} and the capture symmetry factor $k=\sigma_n/\sigma_p$. Two defect energy levels were included in the DPSS analysis as it was not possible to model the lifetime curves simultaneously with one defect alone.

Initially, an adequate least squares fit was achieved by accounting for two arbitrary but fixed defect energy levels. All lifetime curves were modelled with these two energy levels resulting in values for the ratio of capture cross-sections and electron capture time constant for each of the two defects for each temperature. These parameters of one defect were fixed and the others were used as starting values for the following analysis. A sequence of least squares optimisation fitting a second level for a certain energy level $(E_C\text{-}E_t)^{DPSS}$ was separately performed for each of the *T*-IDLS-curves. The arising triple of curves made up of error Chi^2, optimal symmetry factor k^{DPSS} and $\tau_{n0}{}^{DPSS}$ values describing this second defect are visualised in the DPSS diagram shown in Figs. 2b1-d1 as a function of the defect energy level $(E_C\text{-}E_t)^{DPSS}$. For each temperature, these three curves represent the SRH parameterisations which are equivalent with respect to similar quality of the modelling for the considered tem-

perature. As can be seen from truncated DPSS-*Chi*^{2} curves their range of validity is limited. The fact that the fit quality (Fig. 2b1) for a specified temperature is identical for a broad range of $(E_C\text{-}E_t)^{DPSS}$ values visualises the strong ambiguity of the SRH parameterisation of a single IDLS curve as discussed in detail in Ref. [3].

The qualitative change of the underlying lifetime curves of the single defect under investigation from increasing to decreasing shape (see defect 1 in Fig. 1b) upon heating corresponds to a qualitative change of the curves within the DPSS plots of Fig. 2c1-d1. According to SRH theory, very deep defect levels are more recombination-active under low- compared to high-level injection. Thus, decreasing lifetime curves at higher temperatures like the plot for defect 1 at 151 °C in Fig. 1b embody specific characteristics in the DPSS plot of Fig. 2. A split range of validity with a gap around mid gap can be observed (break in solid curve in Fig. 2b1) because these energy values can not be used to model such a decreasing lifetime curve.

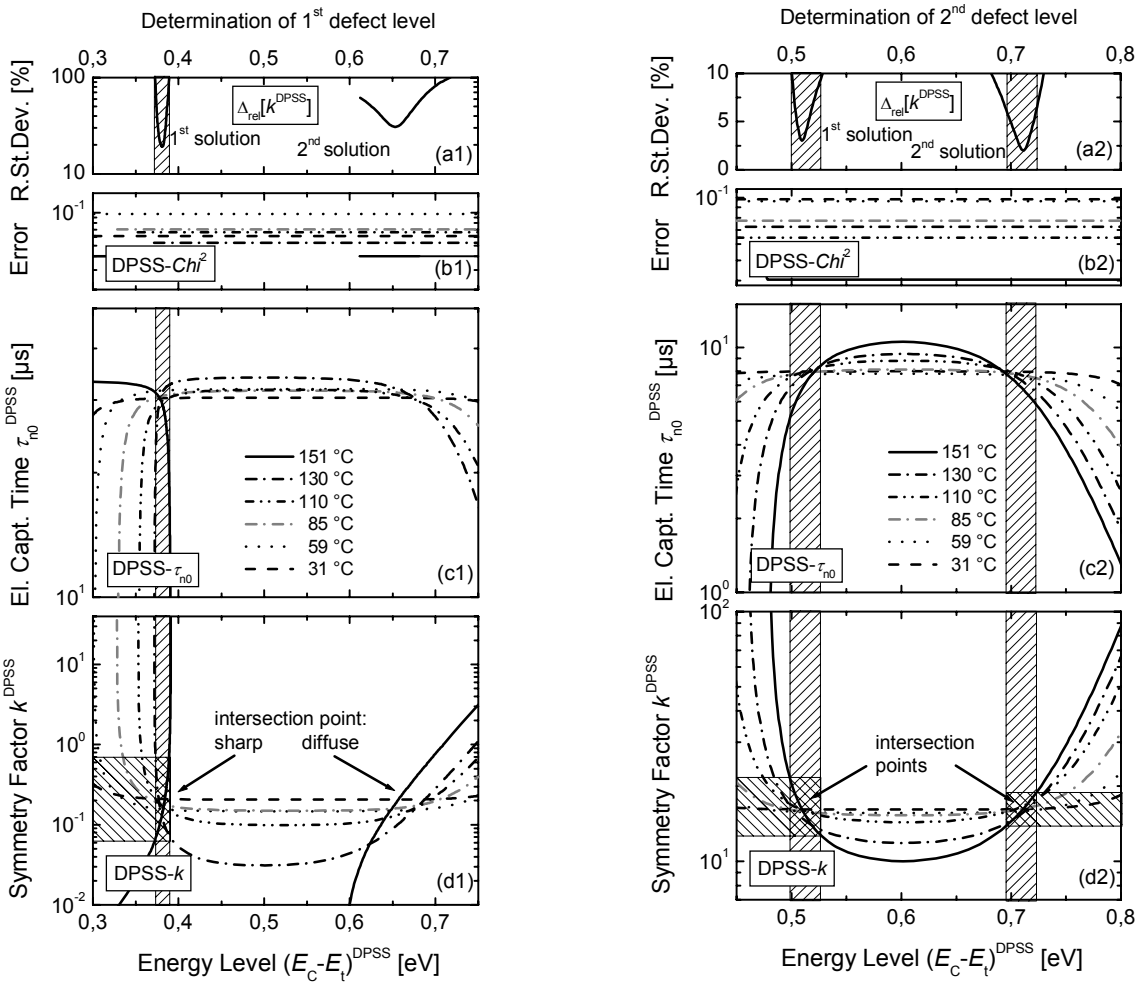

Fig. 2 Superposed DPSS analysis of *T*-IDLS curves measured on a Co-contaminated silicon wafer at different temperatures. For Fig. 2a1-d1, parameters for one defect were fixed and the energy level $(E_C\text{-}E_t)^{DPSS}$ attributed to a necessary second defect was specified but gradually varied. The resulting parameter combinations of this second defect, i.e. one k^{DPSS} and one $\tau_{n0}{}^{DPSS}$ curve calculated for each temperature separately, are superposed in Fig. 2d1 and c1 respectively. The plot of the *Chi*^{2}-results in Fig. 2b1 assesses the quality of least squares fitting. The values of the different DPSS-*k* curves were averaged for each DPSS energy. The corresponding standard deviation $\Delta_{rel}[k]$ in the vicinity of the two minima is shown in Fig 2a1.The minimum of the first solution reflects the optimum energy position for the intersection point and allows the true defect parameters to be identified (1st solution: $E_C\text{-}E_t$=0.38 eV and k= 0.16) by comparing the sharpness of the intersection points of the DPSS-*k* curves. The shaded areas represent an error estimation by tolerating parameters corresponding to three times the minimal standard deviations. For Fig. 2a2-d2, a similar analysis has been repeated with the parameters from the energy level of the first defect (sharp intersection point in Fig. 2d1) kept on fixed values. The resulting second solution ($E_t\text{-}E_V$=0.41 eV, k=16) corresponds to a donor level known from the literature which is thus identified with the second defect.

The true defect parameters for the first defect should result from a common intersection point of all DPSS-k curves. However, their superposition in Fig. 2d1 reveals two intersections. Thus, two parameter sets are valid at first glance.

However, applying a similar DPSS analysis to lifetime curves simulated with SRH theory instead of measured data reveals the difference in the two intersection points of the DPSS-k curves. Thereby, the true parameters chosen for the simulation of the investigated lifetime data correspond to a sharp intersection point. The second intersection is more diffuse if decreasing lifetime curves are included in addition to increasing ones. This effect has been quantified theoretically in Ref. [3]. To extract the true solution from the sharpness of the intersection points, both types of qualitatively different lifetime curves (rising and falling) have to be included in the analysis.

In order to distinguish between the two intersections associated with the DPSS analysis of the Co-contaminated sample, DPSS-k values at specified DPSS energies were averaged and the relative standard deviation $\Delta_{rel}[k]$ was computed. The $\Delta_{rel}[k]$ values in vicinity of the two minima are shown in Fig. 2a1. As a measure of uncertainty of the desired parameters values corresponding to three times the minimal standard deviations were tolerated and marked by shaded areas. As expected from the lifetime simulation study mentioned above [3], the DPSS-k curve corresponding to a temperature of 151 °C causes one intersection point to be more diffuse. This becomes manifest in Fig. 2a1 by a smaller minimum standard deviation of the first solution. Thus, the two solutions are not equivalent and the first intersection can be identified with the true defect parameters: E_C-E_t=0.38±0.02 eV and k=σ_n/σ_p=0.16 within the interval of uncertainty of 0.06 – 0.69 . Due to the temperature dependence of the electron capture time constant τ_{n0}, a common intersection point of all DPPS-τ_{n0} curves in Fig. 2c1 at the true defect energy level can not be expected.

These unique unambiguous defect parameters were fixed for the determination of the Defect Parameter Solution Surface of the second defect. As before, a sequence of least squares optimisation fitting a second level for a certain energy level $(E_C\text{-}E_t)^{DPSS}$ was separately performed for each of the T-IDLS curves. The arising triple of curves (error Chi^2, optimal symmetry factor k^{DPSS} and $\tau_{n0}{}^{DPSS}$ values) describing this second defect are visualised in the DPSS diagram shown in Figs. 2b2-d2 as a function of the defect energy level $(E_C\text{-}E_t)^{DPSS}$. As the defect under investigation does not change the slope from increasing to decreasing within the investigated temperature range, the two intersection points of the k^{DPSS}-curves are both sharp. Thus, the true solution is not expected to reveal a smaller minimal standard deviation (Fig. 2a2). But as is known from the literature, cobalt-contaminated silicon shows a donor level in the lower half of the band gap, the second solution of the second DPSS analysis can be identified with the second defect: E_t-E_V=0.41±0.02 eV and k=σ_n/σ_p=16±3.

The two defects resulting from the investigation enable a simultaneous modelling of high accuracy of the whole set of T-IDLS curves. This result of the detailed DPSS analysis is shown in Fig. 1a by the solid lines. In addition, Fig. 1b shows the lifetime curves measured at 31°C and 151°C together with the corresponding lifetime of the two single defects resulting from the DPSS analysis.

4. CONCLUSION

The detailed DPSS study of a cobalt-contaminated p-type silicon wafer by means of T-IDLS clearly showed the capability of this method to overcome the large ambiguousness of a single injection-dependent measurement (IDLS). The capability to analyse two deep defect levels which affect carrier lifetime in parallel has been shown. In good agreement with the literature, where an acceptor level in the upper and a donor level in the lower band gap half are reported at energy levels of E_C-E_t=0.38-0.41eV and E_t-E_V=0.38-0.42 eV respectively [9, 10], the DPSS analysis revealed two deep defect energy levels as well: E_C-E_t=0.38±0.02 eV and k=σ_n/σ_p=0.16 in the upper band gap half and E_t-E_V=0.41±0.02 eV and k=σ_n/σ_p=16±3 in the lower band gap half.

ACKNOWLEDGEMENTS

The authors would like to thank Prof. T. Abe (ShinEtsu) for supplying the investigated wafers.

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Shape-Shifting Silicon Feedstock

T.F. Ciszek
Siliconsultant Division of Geolite
P.O. Box 1453, Evergreen, CO 80437 USA
www.siliconsultant.com ⌘ ted_ciszek@siliconsultant.com

Abstract

A method for solidifying silicon into near-spherical, mm-size shot is described. Liquid silicon is pressure ejected through quartz or high-density graphite nozzles under conditions that favor Raleigh-mode break-up of the liquid stream into uniform droplets. A circulating water bath located 10-20 cm below the nozzle cools the droplets and moves the solid shot away from the impact region. Si shot in the size range 1-4 mm has been produced using both nozzle materials.

Introduction

For specialized silicon feedstock applications such as improving packing density in directional solidification crucibles or metered melt replenishment in continuous growth processes, it is desirable to have silicon feedstock in the form of small particles. In some cases, it is further advantageous for the Si particles to be uniform in size and shape. The favored source of silicon feedstock for these applications is material produced by a fluidized-bed process. However, in the current supply situation, end users are often not able to obtain this material.

One option is to crush larger pieces of silicon into small flakes [1]. These are irregular in shape, may not feed uniformly in continuous processes, may contain impurities from the materials used in crushing, and require post-crushing wet etching. A traditional way of forming metallic pellets is via the use of a tall shot tower. This has also been applied to silicon [2], but can be inconvenient due to the aspect ratio of the equipment and the need for maintaining an inert ambient over the total height. The lab-scale process described here can change various forms of Si feedstock into near-spherical, mm-sized Si shot via solidification from the melt in a short vertical height.

A laminar stream of liquid exiting a hole of diameter d_o in the bottom of a crucible tends to break up by Rayleigh instability. In Rayleigh's theory, the optimal wavelength of disturbance breaking up the column is 4.51 d_o, leading to a droplet diameter $D = 1.89d_o$, ignoring viscosity and ambient gas flow (viscosity increases D and gas flow decreases it). Liquid column breakup transitions from a drip mode, through fairly uniform Rayleigh-type droplet formation discussed above, to an atomization-type breakup depending on values of the Reynolds number Re_L and the dimensionless Ohnesorge number Oh (or Z), as shown in Fig. 1. This is for droplets in quiescent air. For other gases, there is an additional criteria that the Weber number W_A of the ambient gas must be less than ~0.4 for Rayleigh-type breakup of the column. $Re_L = \rho_L U_L d_0/\mu_L$, $Oh = Z = \mu_L/(\rho_L \sigma d_0)^{0.5}$, and $W_A = U_L^2 \rho_A d_0/\sigma$, where ρ_L is liquid density, U_L is the liquid velocity at the nozzle exit, μ_L is the dynamic viscosity of the liquid, σ is the liquid surface tension, and ρ_A is the density of the ambient gas. We applied Rayleigh-mode liquid stream breakup in this work.

Experimental

Both fused quartz and high density, fine-grained graphite crucibles were used in the experiments. They were 25 mm or 29 mm I.D. and held about 30 g of silicon. A nozzle hole in the diameter range 0.5 mm to 1.5 mm was made in the crucible bottom. The nozzles had a downward-pointing, conical exterior shape.

Induction heating at 450 kHz was used to melt the silicon feedstock charge in the crucibles. The graphite crucibles served as their own susceptor. The quartz crucibles were placed inside a graphite susceptor. In both cases, cylindrical graphite fiberboard insulation was placed around the heated components as well as on the top and bottom (with a 12 mm dia. hole for liquid stream passage).

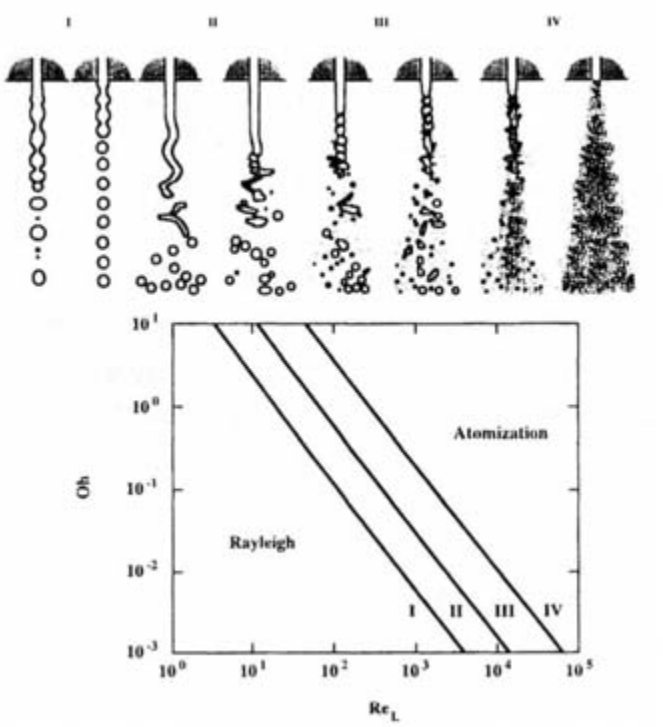
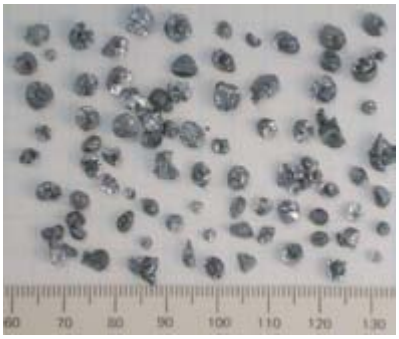


Fig. 1. Modes of liquid column break-up [3]

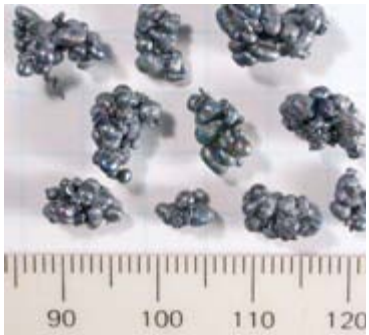
The hot zone components were contained in a vertical tubular quartz chamber 69 mm O.D. x 65 mm I. D. x 500 mm tall, with an O-ring sealed metal top plate through which argon purge and pressurizing gases could be admitted. The flat-bottomed tube had a reduced diameter (12mm O.D.) central bottom outlet which served as (1) a vacuum port for initial pump-down of the system, (2) an outlet for the purge gases, and (3) a purged passage-way for the liquid droplets exiting the nozzle and the chamber.

For initial experiments, a 55-mm-I.D. x 900-mm-tall, open-top, flat-bottom, vertical quartz container was placed under the quartz chamber, separated by an insulation block, and partially filled to various levels with distilled water, which quenched the droplets. Argon exit gas from the chamber purged the space above the water level. Three main observations (see Fig. 2) were

Fig. 2a – Pellets from liquid head pressure only, 1.5mm nozzle dia., 52-cm nozzle-to-water distance (0.63x demagnification)



2b – Pellets from 0.06 bar ejection pressure with a 1 mm nozzle dia., 69-cm nozzle-to-water distance.



2c – Pellets from 0.1 bar ejection pressure with a 0.5 mm nozzle dia., 14-cm nozzle-to-water distance

made with this set-up: (1) When gravity head pressure alone was used to establish flow from a 1.5 mm nozzle, the Rayleigh break-up mode was not achieved. Instead irregular, larger drip-mode droplets were formed as seen in Fig. 2a. With externally applied 0.06 bar argon pressure used to eject the liquid Si stream through a 1 mm nozzle 69 cm above the water, a more uniform (and smaller) pellet size was achieved, indicating Rayleigh-mode break-up. But many of the pellets were cracked as shown in Fig. 2b, presumably from solidifying substantially in the argon above the water (see inset at right), but suffering thermal shock upon impact with the water. (3) With 0.1 bar ejection pressure through a 0.5 mm quartz nozzle and a short (14 cm) nozzle-to-water distance, again Rayleigh-mode break-up resulted in uniform sized pellets. Most of them were not cracked, but many froze clustered together in the water as shown in Fig. 2c.

The conclusions from these experiments are: (1) that Rayleigh-mode liquid Si stream break-up is achievable with 0.5 – 1.0 mm dia. quartz nozzles if a moderate argon ejection pressure (0.1 bar) is used; (2) a short nozzle-to-water distance is desirable to prevent pellet splitting; and (3) previously fallen pellets must be removed from the water impact region to make way for subsequent ones if fusing of pellets into clusters is to be avoided. A system to achieve this is shown schematically in Fig. 3. A pump provides strong cross flow of 19 l/min to sweep Si pellets away from the impact region, and a short (13 cm) nozzle to water distance allows shot to form mostly uncracked.

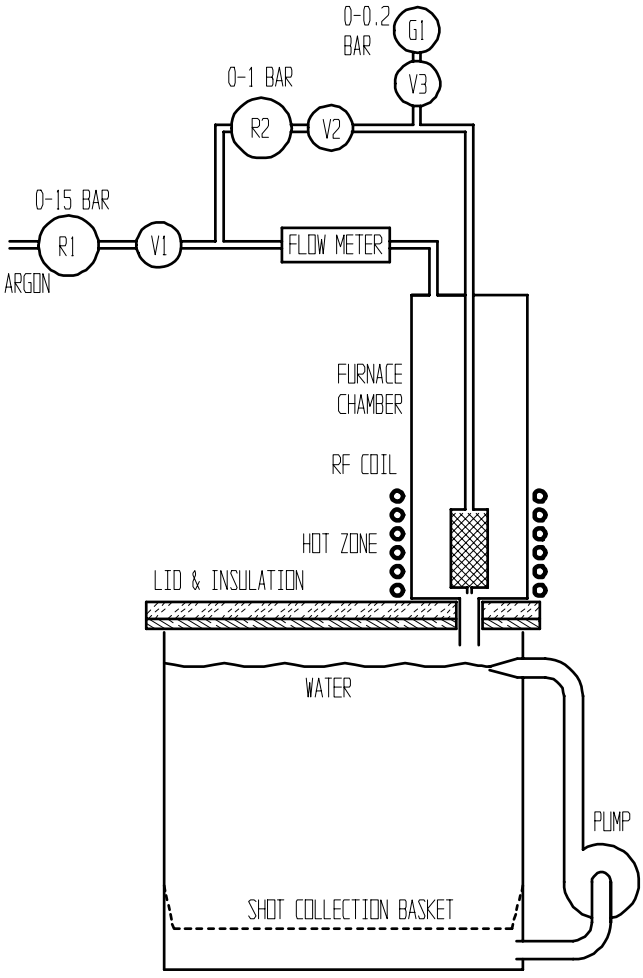


Fig. 3. Shot production schematic

Results, Discussion, and Conclusions

Figure 4 shows the Si shot obtained from 3 successive runs made with the same high-density graphite crucible. The nozzle diameter was 0.74 mm, the nozzle-to-water distance 13 cm, the ejection pressure ~ 0.1 Bar, and the water cross flow 19 l/min. Each charge was about 30 g. The grid in the photos is 6.3 mm. The crucible emptied nearly completely after each use. Clustered shot was placed at the top of each photo. Fig. 5 shows the Si shot obtained from 6 successive runs using the same quartz crucible with ~0.9 mm nozzle (other conditions were the same as for the graphite crucible. On the last of the 6, the ejection

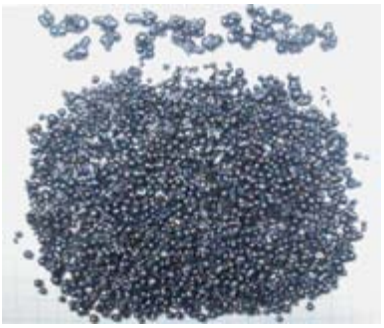


Fig. 4a Si shot (6.3 mm grid)

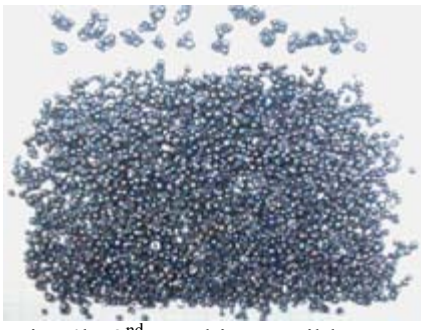


Fig. 4b 2nd graphite crucible use

Fig. 4c 3rd graphite crucible use

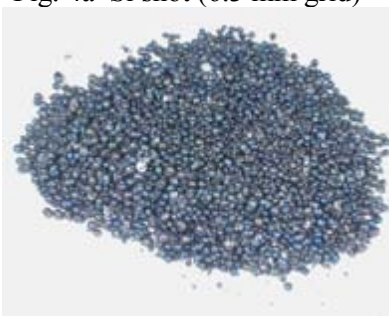


Fig. 5a Si shot, quartz crucible

Fig. 5b 2nd crucible use

Fig. 5c 3rd crucible use

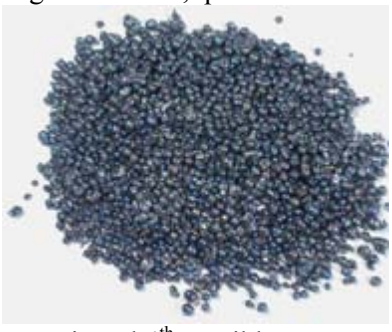


Fig. 5d 4th crucible use

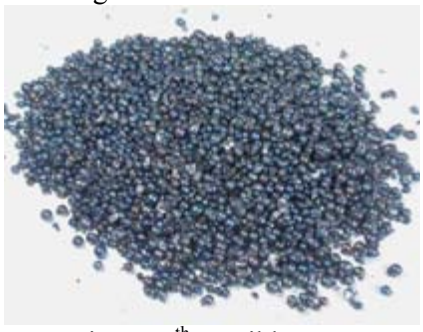


Fig. 5e 5th crucible use

Fig. 5f 6th crucible use

pressure was off for a portion of the run, resulting in large, drip-mode globs of Si.

The measured throughput rate for crucible emptying ranged from 135 to 185 kg/day/nozzle for nozzle diameters between 0.5 and 0.8 mm with 0.1 bar ejection pressure. The shot is spherical with small burst-out tails of last-to-freeze Si, as shown in Fig. 6. Graphite and quartz crucibles worked about equally well. A very thin oxide coating is present from hot Si/water interaction.

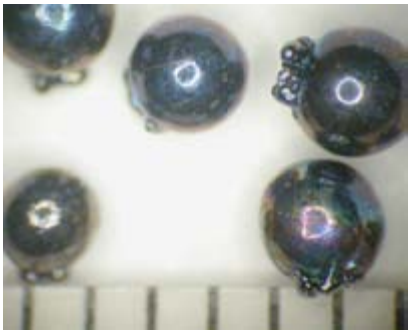


Fig. 6 Typical Si shot, 1mm scale markers (circles are reflections)

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GT-PVSCAN 8000: A Versatile Tool for Photovoltaic Mapping Analysis

Ning Duanmu, Jim Dowling, Tom Broyer, P. S. Raghavan, Heiko Moritz, and Kourosh Kamshad
GT Solar Technologies, 243 Daniel Webster Highway, Merrimack, NH 03054
Email contact: Duanmu@gtequipment.com

Bhushan Sopori
National Renewable Energy Laboratory (NREL), 1617 Cole Boulevard, Golden, CO 80401

Keyword: Solar, crystalline, silicon, photovoltaic, mapping, dislocation, reflectance, LBIC

Abstract

GT Solar Technologies (GT Solar) has designed and developed a robust, versatile, and industry standard photovoltaic characterization equipment named GT-PVSCAN 8000™ in collaboration with National Renewable Energy Laboratory (NREL). The original concept was developed by Bhushan Sopori [1, 2] of NREL, and GT Solar has obtained an exclusive patent license agreement to build these systems to customer needs. The GT-PVSCAN 8000™ system engineered by GT Solar is the first mature and commercially available instrument of this kind for the fast growing photovoltaic (PV) industry. In comparison with last generations of the PVSCAN system sold by GT Solar, GT-PVSCAN 8000™ provides a much faster, more accurate, and more convenient means of mapping and presenting the dislocation density, reflectance, and light beam induced current (LBIC) of large area crystalline silicon wafers and photovoltaic solar cells. The system has the flexibility of making LBIC and reflectivity measurements at different wavelengths and can be used for crystalline silicon or other forms of solar cells, which include a-Si, CdTe, CIGS, and dye sensitized solar cells, etc. In this paper, a brief review of the measurement principle along with the salient features of the hardware and software design is presented.

1. Introduction

"Clean energy" is attracting more and more interests, which in turn exert cost pressure on photovoltaic manufacturers for more efficient solar panel production due to the competitive situation. Because of market pressures, the PV community has been interested in implementing test equipment for material and cell analyses and for process monitoring. Wafer manufacturing and the subsequent solar cell processing are crucial steps in the crystalline silicon solar cell fabrication. Technology improvement of the crystal growth process would benefits from a fast and convenient means of counting the grow-in dislocation density of the crystalline silicon substrate which has been proven by previous research [3] as one of the major sources of aggravated minority carrier recombination. Likewise, measuring the spatial distribution of the surface reflectance and the photovoltaic response of the finished solar cell would indicate further process innovation opportunities. GT-PVSCAN 8000™ system addresses these needs in one versatile and easy-to-use instrument.

Three different measurement modes are integrated in this GT-PVSCAN 8000™ system. Defect mode yields the dislocation density map for various types of crystalline silicon substrates including mono-crystalline and multi-crystalline wafer, edge-defined grown (EFG) ribbon, and string-assisted

ribbon, etc. The enabling technology is to use an integrating sphere to collect the scattered reflection from the etched pits delineated by Sopori etching method [4]. As shown by the schematics in fig. 1., the smart optical design splits the reflected laser light into two parts: scattered and specular reflectance. The scattered light is further separated into near specular and diffuse components. Thanks to this design, the reflectance mode of this instrument can be directly used as an enhanced reflectometer on two laser wavelengths (632nm and 980nm) which generates not only the average but also the spatial distribution of the surface reflectance for large area solar cells. Finally, the LBIC mode of the system is able to measure the photovoltaic response of the finished solar cell induced by laser light at 632nm and 980nm wavelength. The LBIC measurement can be directly converted to quantum efficiency of photovoltaic devices. Combination of the reflectance mapping and the LBIC mapping generates the mapping information related to the internal quantum efficiency (IQE), which has been studied as the one of the most fundamental performance indicators for general photovoltaic devices [6, 7].

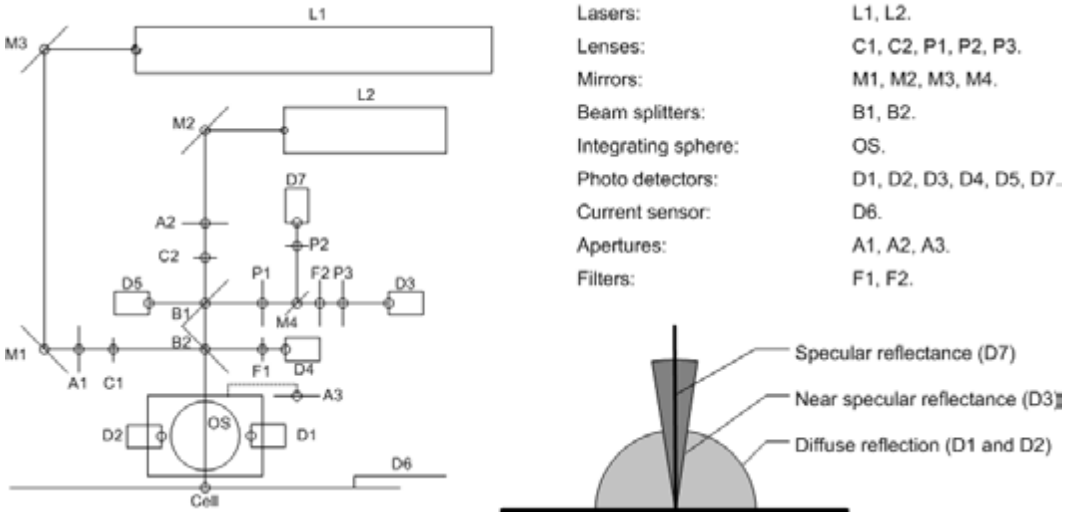

Fig. 1. PVSCAN optical schematics and measurement principle

2. System development

2.1 Fast scan

In the earlier generation of the PVSCAN system [8], the XY scanning stage was leadscrew based, posing problems such as long scanning time, backlash, skipping points, low resolution, etc. The present GT-PVSCAN 8000^{TM} system uses a state of art linear XY stage with cross roller bearing and linear encoder. It gives the maximum speed of 1m/sec and acceleration of 9.8m/sec^2. With this motion mechanism, GT-PVSCAN 8000^{TM} can finish scanning a 125mm×125mm sample within 10 minutes at a fine sampling interval of 50μm. The submicron positioning repeatability of this linear XY stage guarantees the scan position accuracy under fast scan motions within a large scan range and produces high resolution mapping information.

2.2 Refined optics

The optics is attached to a granite gantry board. Its high surface flatness and thermal stability ensures the alignment consistency for lasers as well as other optical components. According to the original optical design [5], the internal reflection between the glass front surfaces of photo detectors seems to be inevitable. It generates significant error on photo detector readings. If this error is too large,

it can not be reliably compensated by adjusting the voltage offset on the data acquisition card. To solve this problem, the photo detector fixture was redesigned such that the photo detector front surface is not strictly normal to the laser beam. Therefore, laser beam irradiates into the photo detector through a small angle such that the reflection does not go back to other photo detectors.

2.3 Mechanical integrity

The system can accommodate wafers up to 210mm×210mm, and of various thicknesses. The novel wafer holding chuck can hold samples of any arbitrary shapes and sizes. The optical quality mechanical infrastructure is another unique feature of this new GT-PVSCAN 8000^{TM} system. The whole XY stage assembly is mounted on a heavy granite base which serves to stabilize the momentum created by the fast acceleration and deceleration of the scan motion. The granite structure is isolated from outside mechanical shocks by four air-pumped rubber-made shock absorbers. All the moving parts (XY stage) and lasers are securely contained in one sealed enclosure with mechanically latched safety switch access. If the customer needs to integrate the system into the production line, provisions are available for automatic wafer feeding.

3. Measurement analysis

Fig. 2. shows the data presentation of a scan result for dislocation density mapping obtained on a 125x125 mm multicrystalline silicon wafer. The wafer was lapped and polished before subjecting to the decoration etching using Sopori etchant [4]. The mapping result is presented in a 2-D color format. Different level of dislocation density is indicated by different color on the map referenced by the legend. The color display range is easily adjusted by the user. Minimum, average, and maximum of the scan data is displayed on the screen. Other statistics can be added upon individual customer's request. The scan data is stored in a general form that is accessible to commonly used software and post-analysis options such as zooming in a region of specific interest will be provided upon request.

Defect densities were found to be in the range of 10^3 - 10^8 defects/cm^2. The 632nm wavelength laser was used to scan the sample surface. The beam size used was about 200μm in diameter. The system is calibrated against the high precision dislocation standard provided by NREL. As could be seen from the figure 1, the highest defect concentrations were found in line defect regions.

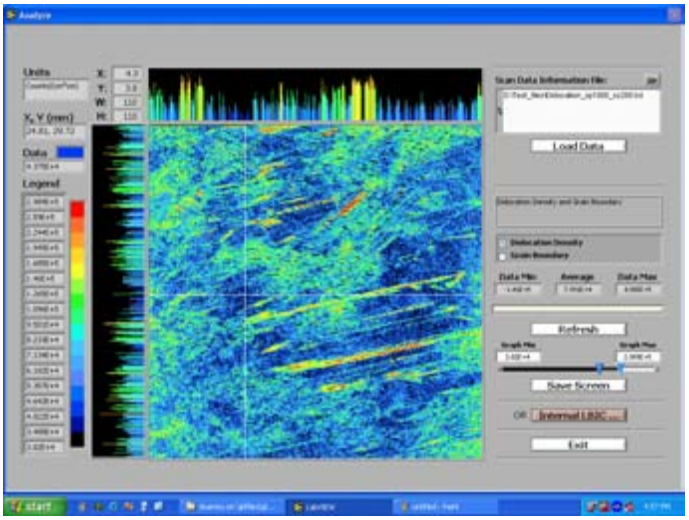

Fig. 2. GT-PVSCAN 8000^{TM} dislocation density mapping of multi-crystalline wafer after Sopori etching

Likewise, examples of reflectance and LBIC mapping results are shown in fig. 3. and fig. 4. using similar color presentation scheme. Both scans were conducted on solar cells made of multi-crystalline silicon wafers using the 980nm wavelength laser. High measurement accuracy was achieved by GT Solar's excellent electrical and data acquisition design and an accurate system calibration using NREL's reflectance and LBIC standards. The measurement range and accuracy is well beyond the need of state of art PV applications.

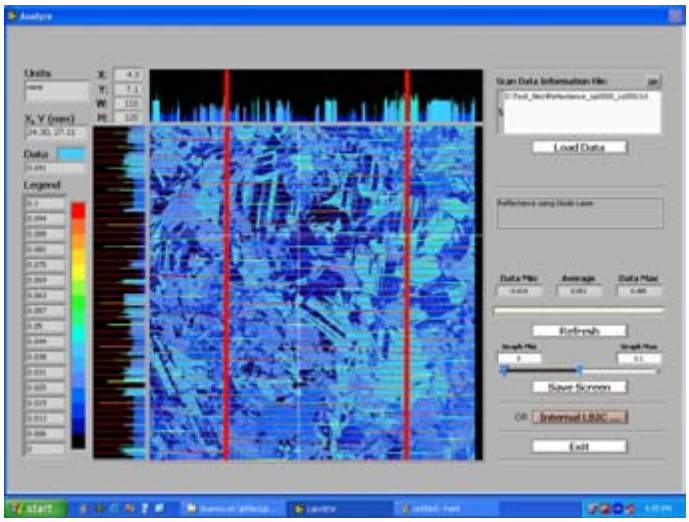

Fig. 3. GT-PVSCAN 8000^{TM} reflectance mapping of multi-crystalline solar cell using 980nm laser

In particular, in fig. 4., the region in yellow or red color corresponds to higher photovoltaic response than the region with blue and green color. These low efficiency areas might be consequences of the high reflectance caused by particular grain orientation, size or coating process shown by the reflectance mapping (fig. 3.), or the dislocation cluster in the crystalline silicon wafer characterized by the dislocation density mapping (fig. 2.). The cross-referencing of mapping results of these three measurement modes (dislocation density, reflectance, and LBIC) would indicate the source of efficiency loss in the solar cell manufacturing process.

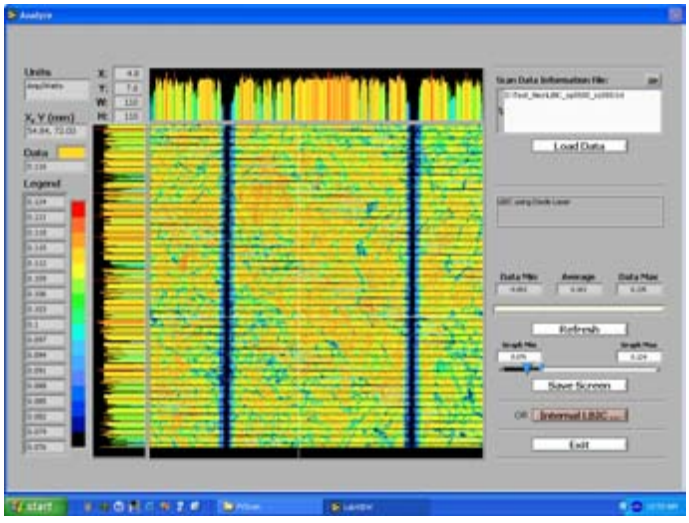

Fig. 4. GT-PVSCAN 8000^{TM} LBIC mapping of multi-crystalline solar cell using 980nm laser

4. Conclusion:

The capabilities of the GT-PVSCAN 8000^{TM} system have been improved by several folds in terms of resolution, accuracy, scan speed, wafer handling, reliability, and data presentation. Key product specifications and user benefits are summarized in table 1. The measurement results obtained on dislocation density can assist crystal growers in achieving high-quality materials and the results on reflectance and light beam induced current can help solar cell process engineers to develop fabrication processes for higher efficiency devices.

Measurement mode:	Dislocation density, reflectance, and LBIC.
Photovoltaic characterization:	Provides information related to junction recombination and minority carrier diffusion length.
Laser wavelength:	632nm and 980nm, for measuring surface and bulk properties, other wavelengths upon request.
Maximum sample size:	210mm×210mm (rectangular).
Accuracy:	25μm practical sampling interval.
Performance:	25 minutes to scan a 156mm×156mm size sample using 50μm sampling interval.
Data presentation:	Provides color map for spatial distribution of measurement results.
Operation convenience:	Camera assisted selection of scan area.

Table 1: GT-PVSCAN 8000^{TM} quick list of product specification and user benefits

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MECHANISMS OF GETTERING METALLIC PRECIPITATES FROM SILICON USING OPTICAL PROCESSING

Na Li, Teh Y. Tan, and Bhushan L. Sopori*

Department of Mechanical Engineering and Materials Science
Duke University
Durham, NC 27708-0300
*National Renewable Energy Laboratory, Golden, Co 80401-3393

ABSTRACT

Using a deposited Al layer, optical processing at a temperature below the Si-Al eutectic temperature of T_{eu}=577°C for a few minutes and followed by $T>T_{eu}$ for a few more minutes are able to getter metallic precipitates out of multicrystalline Si. To accomplish the same, a few tens of hrs is needed when using thermal annealing at 700°C. Possible mechanisms involved in optical-processing gettering are proposed. These mechanisms include vacancy injection, radiation-enhanced solubility, and radiation-enhanced diffusion of vacancies and metal impurity atoms. Using $FeSi_2$ as a model case for which the Si lattice expands concomitantly with the dissolution of the precipitates, physical modeling and numerical simulations are carried out to uncover and test the conditions for the mechanisms to be effective. The mechanisms are found to be effective provided that the injected Si vacancies due to alloy formation are nearly all retained inside and evenly distributed throughout the Si bulk at the lower temperature, and that the Fe atom migration energy barrier is reduced by ~0.15 eV by radiation at the higher temperature. On the other hand, for the gettering of a precipitate species for which the Si lattice will shrink concomitantly with the dissolution of the precipitates, the vacancy-injection mechanism will not only be ineffective but should also have a detrimental effect.

INTRODUCTION

It is well known that gettering of metallic impurity precipitates from multicrystalline (mc-) Si using Al is not effective by thermal annealing at the relatively low temperatures of ~700°C for a short time, as is appropriate for solar cell processing. Using $FeSi_2$ as a model precipitate species, we have shown that it will take more than 50 hrs at 700°C to getter them out. We identified the limiting mechanism as the slow precipitate dissolution rate.[1] In that study, the assumed conditions are that Fe was introduced at 900°C to its solubility of ~5.02×10^{13} cm^{-3} and then precipitated out to steady state at 700°C to the density of $\rho=10^{11}$ cm^{-3}. On the other hand, it is also known that, using a deposited Al layer, gettering by optical-processing are able to getter metallic precipitates out of mc-Si with a total time of minutes.[2] Optical-processing gettering consists of two steps: (i) a low temperature step below the Si-Al eutectic temperature of T_{eu}=577°C for several minutes; and (ii) a high temperature step with $T>T_{eu}$ for several minutes. In this paper, the possible physical mechanisms responsible for the effectiveness in gettering under optical-processing conditions are proposed. Using $FeSi_2$ as the model impurity precipitate, physical modeling and numerical simulations are carried out to test the effectiveness of these mechanisms by finding the appropriate conditions. The proposed mechanisms include vacancy injection, ra-

diation-enhanced solubility, and radiation-enhanced diffusion of vacancies and metal impurity atoms.

FORMULATION OF THE PROBLEM

We have recently identified the involved physical processes and accordingly modeled the gettering of metals,[1,3-6] include metal dissolution from the precipitates, diffusion of metal atoms to and their stabilization at the gettering sites, and the effect of the precipitate volume misfit with the Si matrix on the gettering effectiveness. In the present problem of optical-processing gettering of Fe and $FeSi_2$ as the gettered metal and precipitates, we assume that the misfit due to precipitate dissolution is accommodated primarily by the point defect vacancies (V).[1]

Gettering of M by the Al-Si liquid involves the segregation processes taking place at the interface of Si and the liquid layer, which occurs simultaneously with impurity diffusion. Accounting for M diffusion, segregation, and dissolution of the precipitates (in the relaxed state before gettering), the time change rate of M atoms is given by[3,6]

$$\partial C_M / \partial t = \partial / \partial x \left[D_M \left(\partial C_M / \partial x - (C_M / m_M)(\partial m_M / \partial x) \right) \right] - (4\pi r^2 \rho / \Omega_{MSi_x})(dr / dt). \quad (1)$$

In Eq. (1) D_M is the M diffusivity, C_M is the M concentration in Si, m_M is the M segregation coefficient, ρ is the precipitate density, r is the radius of the precipitate, Ω_{MSi_x} is the volume of one MSi_x molecule formed by one M atom and x Si atoms, and dr/dt is the precipitate radius change rate which is in turn given by[3,6]

$$dr / dt = \Omega_{MSi_x} D_M (C_M - C_M^*) / r. \quad (2)$$

In Eq. (2) C_M^* is the dynamical equilibrium concentration of M maintaining the precipitate to neither grow nor shrink. Irrespective of whether the impurity is a substitutional or an interstitial species, upon precipitation, there is usually a volume change between the precipitate and the involved metal and Si atoms, i.e., the misfit. On the one hand, mass conservation condition requires the reaction $M + xSi \Leftrightarrow MSi_x$ to hold, and on the other, if the precipitate is strain-free, volume conservation condition requires the relation $\Omega_{MSi_x} = \Omega_M + (x + y)\Omega_{Si}$. Here Ω_M and Ω_{Si} are respectively the atomic volumes of the M and Si atoms, and y is the misfit, with its value being either positive or negative. For M being a substitutional species $\Omega_M = \Omega_{Si}$, and for M being an interstitial species $\Omega_M = 0$. Upon continued growth or shrinkage of the precipitate, the effect of the misfit cannot be cumulative, since then the strain energy will be too large. For our present problem we assume that the precipitates are in the strain-free relaxed state to start with, and the misfit associated with precipitate dissolution is accommodated by Si vacancies V. Now, the combined mass and volume conservation condition requires $M + xSi + yV \Leftrightarrow MSi_x$ to hold, and the corresponding Gibbs free energy consideration of the system leads to

$$C_M^* = C_M^{eq} \left(C_V^{eq} / C_V \right)^y \exp\left(2\Omega_{MSi_x} \sigma / r k_B T \right), \quad (3)$$

where C_V and C_V^{eq} are the actual and thermal equilibrium concentrations of V in the Si matrix. Furthermore, the C_V change rate is obtained as

$$\partial C_V / \partial t = \partial / \partial x \left(D_V \partial C_V / \partial x \right) - y(4\pi r^2 \rho / \Omega_{MSi_x})(dr / dt), \quad (4)$$

where D_V is the V diffusivity in Si.

INITIAL NUMERICAL SIMULATION RESULTS

As an initial test of the soundness of the model, numerical simulations were carried out for optical-processing gettering of Fe in Si wafers 200 μm in thickness by a 2 μm thick Al layer at the wafer backsurface (at the 200 μm position). It is assumed that Fe was introduced at 900°C to its solubility of ~$5.02x10^{13}$ cm^{-3} and then precipitated out to steady state at 700°C to the density of $\rho=10^{11}$ cm^{-3}. For the interstitial Fe atoms $\Omega_M=0$ and for the $FeSi_2$ precipitates $\Omega_{MSi_x}=1.85\Omega_{Si}$,[8] and hence y=-0.15. The negative y value means that growth of $FeSi_2$ precipitates is associated with a Si matrix volume contraction while their dissolution with a volume expansion. Thus, generation of V or consumption of I or both will result from $FeSi_2$ precipitate growth, while generation of I or consumption of V or both will result from $FeSi_2$ precipitate dissolution. Consequently, gettering will be faster if a V-supersaturation exist.

Optical processing occurs at two temperatures, a low temperature $T_L<T_{eu}$ and a high temperature $T_H>T_{eu}$, where T_{eu} is the Al-Si system eutectic temperature of 577°C. Injection of V into Si takes place at T_L, which is assumed to be 500°C. At T_L, a solid Al-Si alloy with 0.6 at% Si forms by the migration of Si atoms into Al (not the other way around, because the Al solubility in Si is negligibly small), with each Si atom went into Al leaving one V behind in Si. Assuming that alloy formation is complete at T_L, then there will be

$$C_V = 3x10^{18} cm^{-3} \tag{5}$$

V injected into Si for the case assuming an Al layer thickness of 2 μm and a Si wafer thickness of 200 μm. Dependent upon the V diffusivity in Si at T_L under the optical processing condition, these injected V may either be essentially accumulated at the interface of the Al-Si alloy and the Si bulk, or distributed throughout the Si bulk. Now, the V contribution to Si self-diffusion is known to be[7]

$$D_V^{Si} = D_V\left(C_V^{eq}/C_o\right) = 2 \sim 3x10^{22} \exp\left(-4eV/k_BT\right) cm^2 s^{-1}, \tag{6}$$

where $C_o = 5x10^{22} cm^{-3}$ is the Si atom density. There are two sets of data in the literature of the separate D_V and C_V^{eq} values:[7]

$$D_V = 0.1\exp\left(-2eV/k_BT\right)\ cm^2 s^{-1}, \quad C_V^{eq} = 2x10^{23}\exp\left(-2eV/k_BT\right) cm^{-3}, \tag{7}$$

$$D_V = 6.17x10^2\exp\left(-0.5eV/k_BT\right)\ cm^2 s^{-1}, \quad C_V^{eq} = 4.86x10^{23}\exp\left(-3.5eV/k_BT\right) cm^{-3}, \tag{8}$$

The values given by Eq. (7) did not allow to obtain the needed optical-processing gettering results, i.e., much longer times are needed. Hence, the values of Eq. (8) are used. If it is assumed that the injected V are accumulated at the Al-Si alloy and Si interface, our simulation results showed that it is not possible to complete th gettering process at 700°C on a tome scale of minutes. Thus, the injected V will be assumed as distributed throughout the Si bulk. This is justified

using the D_V value given by Eq, (8) which in fact predicts that the injected V will be essentially distributed throughout the Si bulk with the 500°C optical annealing time exceeding a few minutes. At 700°C, considering that $C_V = 3x10^{18} cm^{-3}$ from Eq. (5) and $C_V^{eq} = 3.68x10^5 cm^{-3}$ from Eq. (8), we see that $C_V / C_V^{eq} \sim 8.15x10^{12}$, which is a huge V supersaturation. When used in Eq. (3), via the term $\left(C_V^{eq} / C_V\right)^{-0.15}$, this V supersaturation leads to an increase of the *effective* Fe atom solubility at 700°C by ~86 times. Furthermore, in order to simulate the complete gettering of the present case, the Fe atom migration energy needs to be reduced by ~0.15 eV (from 0.68 eV), which is assumed to be due to the radiation enhancement.

Using Eqs. (1)-(4) and the values given in the above discussion associated with Eqs. (5), (6) and (8), we have numerically simulated the optical-processing gettering process. In this simulation the radiation enhanced solubilities of V and Fe are not invoked, as it was not needed. Figure 1 shows the result of using thermal annealing only at 700°C, and it is seen that more than 50 hrs is needed to complete the gettering process. Figure 2 shows the results of that of the optical-processing gettering, and it is seen that the gettering process is complete with the processing time of only minutes at 500°C and followed by also minutes at 700°C.

CONCLUSIONS

It is obvious that optical-processing gettering involves hereto unconsidered physical mechanisms that introduce new challenges into the impurity precipitation/gettering modeling problem. In this initial modeling study, the mechanisms are proposed and used to demonstrate that they can give rise to improvement in the effectiveness of gettering metallic precipitates provided upon precipitate dissolution the matrix material will expand, and this is the case for $FeSi_2$ which is most common in mc-Si. Should the precipitate species be a species that upon its dissolution the Si matrix material will contract, then the opposite effect can be expected, e.g., some Ni and Cu precipitate species. This is because the proposed mechanisms include Si vacancy injection into the Si matrix to cause a V supersaturation. Consequently, such vacancies will release the compressive strain for the Si matrix expansion case. The opposite holds for the Si matrix contraction case, for which, owing to V-supersaturation due to injection, not only should the optical-gettering condition not effective, but also it might well be harmful. Verifications of the mechanism both experimentally and theoretically are needed. For instance the formation of the solid Al-Si alloy should be readily detectable after processing at T_L. Also, if a buried dopant layer is used it should be possible to detect the injected vacancies in the T_H processing step by observing an enhancement in the dopant diffusivity and dopant-V pair concentration. Examples of theoretical problems need to be addressed would include: whether the injected V did or did not substantially migrate out through the Al-Si alloy layer; obtaining a more precise physical picture of the migration energy barrier reduction through the radiation enhanced diffusion mechanism; and the role of radiation enhanced V and Fe solubilities.

ACKNOWLEDGMENT

This work is support by NREL subcontract #XEJ-6-66132-01.

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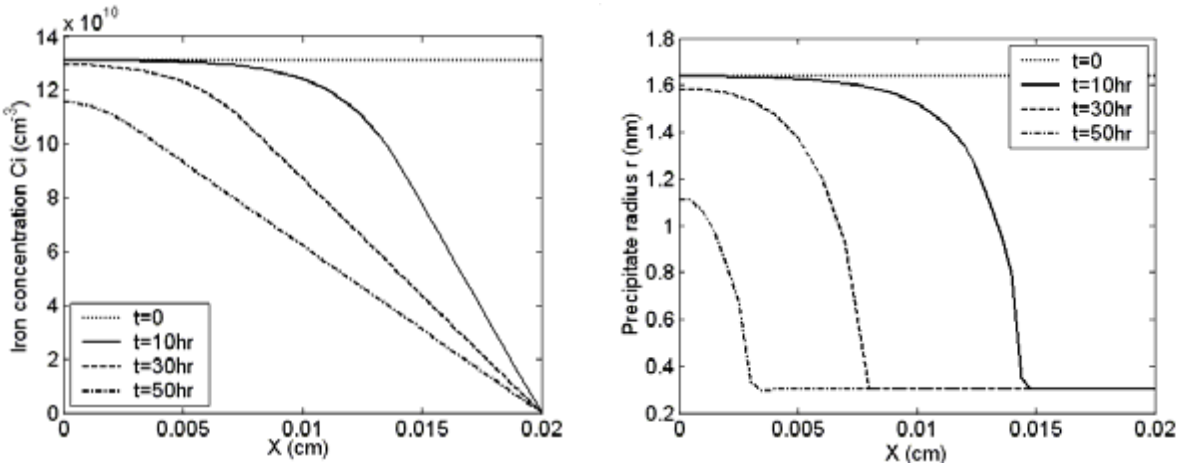

Fig. 1. Simulation results of gettering dissolved interstitial Fe (left) and $FeSi_2$ precipitates (right) from the Si matrix by a 2μm thick Al-Si liquid layer at the wafer backside (200 μm position) by thermal annealing at 700°C.

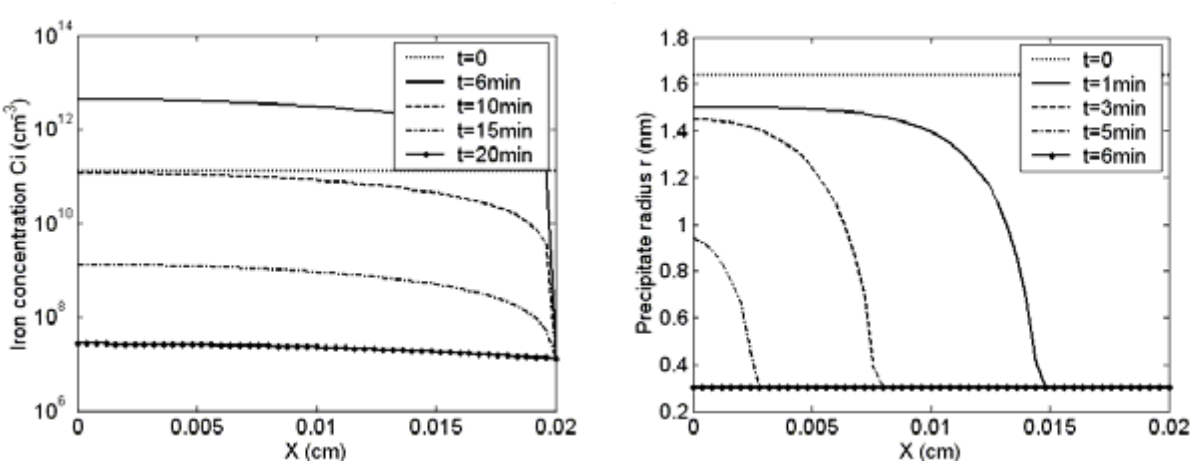

Fig. 2. Simulation results of gettering dissolved interstitial Fe (left) and $FeSi_2$ precipitates (right) for the case of Figure 1 by optical processing.

Chlorine Free Technology for Production of Silicon Feedstock

Belov E.P., Efimov N.K., Pinov A.B., Storoshenko P.A., Strebkov D.S., Zadde V.V.
INTERSOLARCenter, 2, 1-st Veshnaykovsky proezd, 109456, Moscow, Russia.
Tel. (+7095) 171-19-20, fax: (+7095) 170-51-01, E-mail: viesh@dol.ru

K.Touryan, D. Bleak
National Renewable Energy Laboratory (NREL), 1617 Cole Boulevard Golden, Colorado 80401-3393, USA

Abstract: The objective of this paper is creation of ecologically clean method for production of solar grade polysilicon feedstock (PSF) as raw material for photovoltaic solar cells, and also raw material for producing monocrystalline silicon, which is used in electronic industry.

Key Words: Solar Silicon, Monosilane, Fabrication.

1. Introduction

Due to development of solar energy industry the significant increase of PSF production will be required in nearest future. That's why creation of special technology of solar grade polysilicon feedstock production is a very important problem. Today, semiconductor-grade polysilicon is mainly manufactured using the trichlorosilane ($SiHCl_3$) distillation and reduction. The feedstock for trichlorosilane is metallurgical-grade silicon, the product of reduction of natural quartzite (silica). This polysilicon production method is characterised by high energy consumption and large amounts of wastes, containing environmentally harmful chlorine based compounds.

In the former USSR the principles of industrial method for production of monosilane and polycrystalline silicon by thermal decomposition of monosilane were founded. The process consists of two stages [1]:

1) Etherification of trichlorosilane for further producing of triethoxysilane proceeding in accordance with the reaction:

$$SiHCl_3 + 3\ C_2H_5OH \xrightarrow{catalyst} SiH(OC_2H_5)_3 + 3\ HCl$$

2) Catalytic disproportion of triethoxysilane proceeding in accordance with the reaction:

$$4\ SiH(OC_2H_5)_3 \xrightarrow{catalyst} SiH_4 + 3\ Si(OC_2H_5)_4$$

This technology was proved in industrial scale at production of gaseous monosilane and PSF.

2. Experimental

We offered new chlorine free technology (CFT). Originality and novelty of the process were confirmed by Russian and US patent [2, 3]. This technology differs by the following:

1. The reaction of metallurgical-grade silicon with ethanol at the 280 °C in the presence of a catalyst:

$$Si + 3\ C_2H_5OH \xrightarrow{catalyst} Si(OC_2H_5)_3H + H_2$$

2. The catalyst enchanted disproportion (i. e. simultaneous oxidation and reduction) of triethoxysilane will lead to the production of monosilane and tetraethoxysilane:

$$4\ Si(OC_2H_5)_3H \xrightarrow{catalyst} SiH_4 + 3\ Si(OC_2H_5)_4$$

3. Dry ethanol and secondary products such as high purity SiO_2 or silica sol can be extracted by hydrolysis of tetraethoxysilane. Ethanol will be returned to Stage 1:

$$Si(OC_2H_5)_4 + 2H_2O \rightarrow SiO_2 + 4\ C_2H_5OH$$

4. Silicon proceeding decomposed pyrolytically to pure silicon and hydrogen:

$$SiH_4 \xrightarrow{850^\circ \div 900^\circ C} Si + 2\ H_2$$

CFT provides a substantial reduction of energy consumption (40 kWh per one kg of polysilicon versus 250 kWh required for one kg of PSF produced by conventional trichlorosilane method). According to pre-calculations cost of polysilicon feedstock for large-scale production is not more than 15 USD per 1 kg [4]. For producing PFS the monosilane is pyrolysed at 800-850^{0}C, the process can be implemented in rod reactor or in fluidized bed reactor with seed silicon particles. In second case the pyrolysis process requires minimal energy at level 10 kWh/kg.

3. Results and Discussion

Characteristics of main raw materials for CTF are presented in table 1. As main raw materials the metallurgical silicon is used with comparatively low purity and ethanol, which at the stage of silica-sol production is returning to the process.

Table 1.

Name	Main parameters
Metallurgical silicon grounded	Mass share of silicon, % - not less than 98,0 Fraction content,% - bigger than 0,5 mm – not more than 5,0 not more than 0,5 – 0,072 mm – not less than 75,0 smaller than 0,072 mm – not more than – 25,0
Ethyl alcohol dehydrated, technological	Mass share of alcohol, % - not less than 98,8 Water content, % - not more than 0,1

The main advantage is absence of Cl in the process, eliminating the possibility of ingress of Cl-contained contamination to environment. Moreover, all stages of the monosilan purifying and pyrolysis are conducted at ambient temperature or at lower temperatures, down to temperature of the monosilan liquefaction; this reduce the risk of work with monosilane. Every admixtures of elements of III-V group, which present in metallurgical silicon, are converted to saturated metalorganic compounds without link element-hydrogen and, thus, are not disproportionated with creation of volatile hydrids like dibohran, phosphine and arsine. In this case main polluting admixtures in monosilane are high-boiled ethoxysilanes. Ethoxysilanes and another metalorganic compounds are removed at the next stage by adsorption of admixtures by liquid tetraethoxysilane cooled to –60^{0}C. Final purity of monosilane 99,999% is reached by adsorption of tracking admixtures by activated

charcoal and final purifying on chucks with chemisorbent. In the CTF the removal of boron in technological process occurs at two stages:

1. at purifying of raw triethoxysilane due to linkage of boron in solid nonvolatile complexes;

2. at catalytical disproportionation of triethoxysilane; because of the reaction selectivity the boron and some other elements (phosphorus,arsenic etc.) do not form volatile gaseous hydrides (B_2H_6, PH_3, AsH_3 etc.), and their liquid compounds are removed with liquid tetraethoxysilane.

Due to this the produced PSF has unique electro physical characteristics: specific resistance on boron is higher than 10000 Ω·cm and on donors - higher than 600 Ω·cm.

Measures on excluding possibilities of pollution of intermediate and main products during the technological process were undertaken at designing of the CTF. It is achieved by the appropriate choice of constructional materials for the equipment, pipelines, armature, use of minimum quantity of nipples connections, selection of optimum conditions of welding.

One of the basic advantages the CTF is ecological safety of production process [5]. First of all, it is ensured by the absence in the technological cycle of aggressive and harmful products such as chlorine, chorus hydrogen and other chlorine-containing products. Moreover, ecological safety of manufacture is ensured by absence of waste gaseous emissions, as well as liquid and solid waste products.

Main products (table 2) for the new method of PSF production are:

- Monosilane and monosilane mixtures with other gases.
- Electronic grade feedstock silicon.
- PSF for PV industry.

Table 2. Characteristics of commodities produced

Name	Parameters of quality
Main production	
PSF	Specific electric resistance of monocrystal, Ω·cm – not less than 10000. Lifetime of non-uniform carriers, μs - more than 1000
Monosilane	Mass share of elements, %, not more than: B – $6x10^{-5}$; Fe - $1x10^{-4}$; Ni - $5x10^{-5}$; Mn - $1x10^{-6}$; Al - $5x10^{-5}$; Cu - $1x10^{-4}$; Mg - $5x10^{-5}$. volume share of oxygen-containing organic admixtures, %, not more than $1x10^{-3}$
By-product	
Silicasol-30	Content of silicon dioxide (SiO_2), %mass – 30. pH of the solution– 7,5 – 9,0. kinematic viscosity at 20^0C, cst – not more than 20. Density at 20^0C, kg/m^3 – 1200 – 1210.
Tri-ethoxysilane	Main product content, %mass – 99,87. Micro admixtures content, %mass - B – $3x10^{-7}$; Fe - $5x10^{-6}$; Ti - $1x10^{-6}$; Mn – $1x10^{-6}$; Al - $1x10^{-6}$; Cu - $1x10^{-7}$; Mg - $1x10^{-7}$; Ca - $5x10^{-6}$; Cr - $5x10^{-6}$.
Tetra-ethoxysilane	Main product content, %mass – 99,8 Micro admixtures content, %mass - B – $1x10^{-7}$; (Ti, Cu, V, Mo, Mn) - $5x10^{-7}$; (P, Zn, Pb, Sb, Cr, Co, As, Sn, Bi) - $1x10^{-6}$; Mg - $2x10^{-6}$; (Ca, Fe, Al) - $5x10^{-6}$; (Ta, Li, Cd) - $5x10^{-6}$.

The technological process allows changing assortment and shares of the products in total amount depending on market situation.

High quality of monosilane and PFS are confirmed by measurements. The admixtures presence is at the level of sensitivity of modern instruments. Specific resistance of monocrystalline silicon samples produced by float zone technique is more than 10 000 Ω.cm, and lifetime of minority carriers is up to 1000 μs.

At the same time there is 24 kg of tetraethoxysilane per 1 kg of monosilane in the yield. To convert it to other useful materials several technologies were elaborated:

- As result of hydrolysis of tetraethoxysilane, silica sols are produced; they can be used as coupling agent at manufacturing transfer-molds, for textile and construction materials strengthening, for creation of composite and other new materials. After thermal treating of silica sols SiO_2 is obtained; it can be used for manufacturing of optical glass fiber and quartz wares,

- Through organ magnesium synthesis of tetraethoxysilane wide used silicone polymers are obtained [6].

- By thermal-oxidation of tetraethoxysilane superfine silicon dioxide (white soot) is obtained, it is used as a filler material.

Recently the design documentation for pilot plants complex for PFS production using chlorine-free technology with capacity 400 kg per year was created. The aim of creation of the pilot plan complex is following:

- finalizing of separate stages and processes of PFS production

- measuring of main parameters of the process for specifying of discharge rates for raw materials, by-products and energy consumption

- finalizing of hardware implementation of the process stages for further design of bigger capacity apparatus.

- accumulation and testing of test samples of PFS aiming determining of its quality and appropriateness for using in different industries (electronics, solar energy products)

- specification of cost of the products (PFS, triethoxysilane, high purity monosilane, silicasol)

- elaboration of initial data for industrial scale design.

The big attention in the project is paid to creation of original apparatuses ensuring maximal output of main products. Especially it concerns to the reactor for direct synthesis of raw triethoxysilane in which optimum contact of reacting components: technical silicon, dehydrated ethanol and catalyst – is provided.

Reactor of disproportionation of triethoxysilane it is implemented in such a manner that mixing of input components occurs due to educed gaseous monosilane and does not demand mechanical mixing devices. Thanks to this necessary tightness of the reactor and absence of pollution of gaseous monosilane with impurities from environmental atmosphere is provided. Thus, high conversion of triethoxysilane into monosilane (up to 95 %) in disproportionation reactor is provided. Similar conditions are ensured in the rest non-standard equipment of the CTF.

In 2006 in Russia the creation of the small-scale pilot plant for PSF will be completed.

4. Conclusions

Design works on the small-scale pilot plant for PSF with productivity 400 kg / year are completed. Works on creation and testing of the small-scale pilot plant can be executed at the end of 2006. Also, the initial data on design of the industrial scale plant with productivity above 100 tones per year and estimated project cost for stages will be developed.

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ANALYTICAL MODELING OF THE RELATIONSHIP BETWEEN PHOTOVOLTAIC MODULE MANUFACTURING COST AND POWER CONVERSION EFFICIENCY

Alan Ristow and Ajeet Rohatgi
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332

Abstract

In accordance with the *U.S. Photovoltaic Industry Roadmap*, photovoltaic module manufacturing costs must be reduced from their present level around \$3.00/W_p to \$1.00/W_p or less in order for PV-derived energy to become cost effective in comparison with conventional energy sources. In this work, an analytical model is derived to analyze the impact of module efficiency on manufacturing cost for crystalline silicon and thin-film PV technologies. The analysis shows that efficiency enhancement alone is not sufficient to achieve the Roadmap's long-term target for cost-effective PV systems. Instead, it suggests that the most effective path to low-cost PV is through a combination of modest efficiency improvements and significant manufacturing cost reductions. Finally, the results of the analysis are used in conjunction with the U.S. Department of Energy's Solar Advisor Model (SAM) to examine how the cost requirements might change for thin-film modules with short (20-year) service lives.

1 Introduction

In 2001, the U.S. Department of Energy released the *U.S. Photovoltaic Industry Roadmap* [1]. Developed in conjunction with representatives of the U.S. photovoltaic industry and research institutions, it sets near-, mid-, and long-term goals designed to nurture PV technology in the United States and ensure that American PV manufacturers will be competitive worldwide. It calls for installed system costs of \$3.00/W_p to \$4.00/W_p by 2010 with an industry growth rate of 25% per year. At that rate, according to the roadmap, domestic PV module shipments should be 3.2 GW_p/yr by 2020, and domestic PV capacity should approach 10% of U.S. peak generation capacity by 2030. The Department of Energy's forthcoming *Multi-Year Program Plan: 2007–2011* (MYPP) [2] further refines these goals via comprehensive PV system modeling with the recently developed Solar Advisor Model (SAM). The MYPP calls for energy costs to fall by 2020 to \$0.05/kW·h to \$0.07/kW·h for utility systems, \$0.06/kW·h to \$0.08/kW·h for grid-connected commercial systems, and \$0.08/kW·h to \$0.10/kW·h for grid-connected residential systems. To achieve these costs, it calls for PV module efficiencies of 20% for crystalline silicon and 15% for thin-film technologies, with installed PV system costs of \$1.50/W_p to \$2.25/W_p for utility systems, \$2.00/W_p to \$2.75/W_p for grid-connected commercial systems, and \$2.25/W_p to \$3.00/W_p for grid-connected residential systems. According to the MYPP, achieving these goals will require end-user PV module costs of \$1.00/W_p to \$1.50/W_p.

The MYPP estimates current average PV module efficiencies at 8% to 14%, depending upon material, technology, and application, with direct manufacturing costs of about \$3.00/W_p. This translates into an area-related manufacturing cost of \$240/m^2 to \$420/m^2; as a result, meeting the goals of the multi-year technical plan requires that module efficiencies increase by 42% to 150% over the next 14 years while area-related manufacturing costs drop simultaneously by a factor of

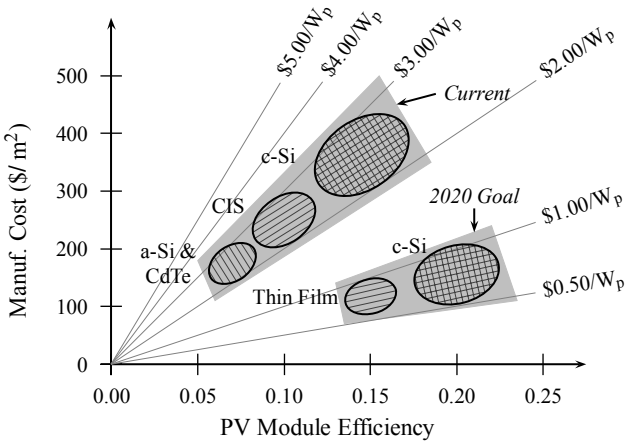

Figure 1: Current area-related PV module manufacturing cost A for thin-film and crystalline silicon technologies and U.S. Department of Energy goals for 2020.

1.2 to 2.1. Clearly, extracting maximum performance from low-cost materials and manufacturing processes is crucial.

Figure 1, which shows the present relationship between A and η for various PV technologies and compares it to the 2020 goals. The current module cost benchmarks used by the MYPP are \$3.00/W_p for direct manufacturing cost and \$4.80/W_p for retail cost, a markup of 60% from factory to end-user including all distributor markup. Assuming this markup persists for the foreseeable future, the retail cost goals for 2020 of \$1.00/W_p to \$1.50/W_p correspond to direct manufacturing costs of \$0.63/W_p to \$0.94/W_p. These are the values reflected in the manufacturing cost goals for 2020 in Figure 1.

The goal of this work is to investigate the implications of these goals on both crystalline silicon and thin-film PV technologies. Through the use of a simple analytical model, manufacturing cost is decoupled from efficiency, allowing the influence of each to be investigated separately. To this end, the work attempts to answer the question of how important efficiency is to cost reduction and investigate its role in leveraging the costs involved in PV module production.

2 Relationship between PV Module Manufacturing Cost and Efficiency

The area-and power-related manufacturing costs are related by the power conversion efficiency, η, of the module,

$$C = \frac{A}{I\eta} \tag{1}$$

where C is the module's power-related cost (e.g., \$/W_p), A is its area-related cost (e.g., \$/m^2), and I is the light intensity at which η is specified (1000 W/m^2 by industry convention). The product $I\eta$ is equal to the power output per unit area produced by a PV module (e.g., a module with 10% efficiency produces 1000 W/m^2 × 0.10 =100 W/m^2).

The power-related cost is the most commonly used metric of PV module cost because it combines both the area-related cost and the power conversion efficiency into a convenient value that has meaning to the end-user and is independent of module technology: A PV module that costs \$400 and has a power-related cost of \$4.00/W_p will produce 100 W under incident light of intensity I, regardless of its efficiency or material composition.

2.1 Modeling Changes in Manufacturing Cost and Efficiency

While the value of A is nominally independent of η, changes to the design of the module or its components can affect both its conversion efficiency and its manufacturing cost. For example,

the addition of rear-side dielectric passivation to an existing solar cell design might increase η, but will likely increase A as well. Thus, despite the fact that changes in efficiency and cost are often treated independently, in reality they are inextricable and it is important to determine whether an increase in efficiency can justify the additional cost it might incur.

To understand and express this tradeoff mathematically, consider a PV module design with area-related manufacturing cost A_1, module efficiency η_1, and power-related manufacturing cost C_1 calculated from equation (1). Suppose the design is modified such that the new area-related cost is A_2, the new module efficiency is η_2, and the new power-related cost is C_2. Then,

$$\Delta A = A_2 - A_1 \tag{2}$$

$$\Delta \eta = \eta_2 - \eta_1 \tag{3}$$

$$\Delta C = C_2 - C_1 \tag{4}$$

Substituting equations (2) through (4) into equation (1) and solving for ΔC yields

$$\Delta C = \frac{\Delta A - C_1 I \Delta \eta}{I(\eta_1 + \Delta \eta)} \tag{5}$$

Thus, equation (5) uses information about the current power-related cost and module efficiency to calculate the change in power related cost resulting from expected changes in area-related cost and module efficiency.

3 Implications for Crystalline Silicon and Thin-Film Photovoltaic Technologies

According to the MYPP, current PV module manufacturing costs are approximately \$3.00/W_p. As previously discussed, this cost needs to decrease to about \$1.00/W_p for PV to be economically competitive with fossil fuels for electricity generation. Using these figures, C_1 and C_2 are \$3.00/W_p and \$1.00/W_p, respectively, yielding a desired ΔC of −\$2.00/W_p. Substituting these figures, along with a range of efficiencies from 5% to 20%, into equation (5) produces the results shown in Figure 2, which shows that \$3.00/W_p modules with high starting efficiencies require either greater increases in η or greater reductions in A than those with low starting efficiencies to reach the \$1.00/W_p goal. For example, Figure 2 indicates that the cost of a PV module with 15% efficiency can be reduced from \$3.00/W_p to \$1.00/W_p with no change in efficiency if ΔA = −\$300/m^2, or with an increase in efficiency to 20% (i.e., $\Delta \eta = 0.05$) if ΔA = −\$250/m^2.

Crystalline silicon PV modules have efficiencies in the 12% to 17% range and currently account for about 95% of annual PV production. With a theoretical maximum efficiency of about 29%, silicon PV module efficiencies might not increase more than 5%. If 15% is taken as a representative starting efficiency η_1 and $\Delta \eta$ is 5%, then η_2 is 20% and, by equation (1) for C_1 =\$3.00/W_p, A_1 is \$450/m^2. Figure 2 suggests that for this 5% increase in efficiency to yield cost-effective PV modules at \$1.00/W_p, A must decrease by \$250/m^2 — more than half — to \$200/m^2. With no change in efficiency whatsoever, A must decrease by \$300/m^2. Finally, even if module efficiency can be increased by a stunning 10%, A must still decrease by \$200/m^2. The situation, however, is not hopeless. Investigations into high-volume production methods have concluded that the cost reductions necessary to reach the \$1.00/Wp goal are attainable through a combination of measures including high-volume production, improved resource utilization (such as solar cell thick-

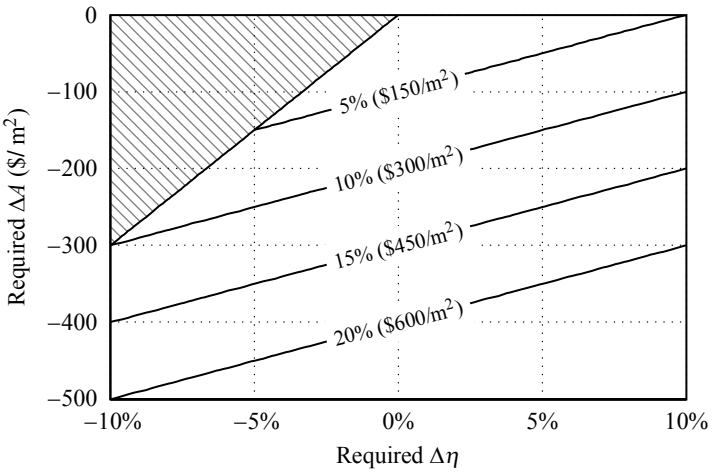

Figure 2: Required combination of ΔA and $\Delta\eta$ to reduce C by \$2.00/W_p for starting module efficiencies η_1 shown on contour lines and starting module cost C_1 of \$3.00/W_p. The hatched region denotes the impossible case where $\Delta\eta < -\eta_1$ (i.e., $\eta_2 < 0$).

ness reduction), increased solar cell efficiency, and greater automation of production processes [3, 4].

Thin film technologies such as amorphous silicon, cadmium telluride (CdTe), and copper indium diselenide (CIS) have been touted as low-cost alternatives that can eclipse crystalline silicon. Laboratory efficiencies approaching 20% for some thin-film technologies have raised hopes that modules of 15% efficiency can be commercially manufactured by 2020. Assuming a current efficiency of 10% at a cost of \$3.00/W_p, their area-related manufacturing cost A_1 is about \$300/m^2. By Figure 2, increasing the module efficiency to the desired 15% will require the area-related manufacturing cost to be cut in half to \$150/m^2; if the efficiency cannot be increased beyond 10%, the required reduction in manufacturing cost is \$200/m^2, or two thirds, for CIS modules to reach the \$1.00/W_p cost target.

Thus, the simple analytical model developed in this research can provide insight into the efforts required to make various PV technologies cost-effective. While thin-films have been highly touted for their low manufacturing costs, it is clear from this analysis that all PV technologies must reduce their current costs by at least half to two-thirds in order to become economical. This insight can be used to assess research and development options and further investigate which technologies have the best chance of becoming economically feasible.

4 Impact of PV Module Service Life on Cost and Efficiency Requirements

Calculations in the MYPP for the 2020 goals assume a 35-year service life. Because the service life of PV modules using thin-film technologies is uncertain at this time, the relationship between A and η for thin-film modules with a 20-year service life was determined. The requirements for the 20-year case were determined using version 0.9.9.4 of SAM [5], the model used by the Department of Energy to develop the requirements published in the MYPP. At the time of this work SAM was available only in limited release.

The 20-year case was modeled using the same assumptions used in the residential baseline case of the MYPP, save for a 20-year service life and 20-year financing period. Module efficiency was assumed to be 15%, the efficiency called for by the plan. Module cost was then adjusted to match the real levelized cost of electricity (LCOE) for the 35-year case. This resulted in a required retail module cost of \$0.34/W_p to \$0.73/W_p (compared to \$1.00/W_p to \$1.50/W_p for modules lasting 35 years). Assuming the 60% markup between factory and end-user used in the 35-year case, this corresponds to a direct manufacturing cost of \$0.21/W_p to \$0.46/W_p.

A revised version of Figure 1 appears in Figure 3 and depicts this difference. It shows that in order for PV modules with short service lives to compete with those having longer service lives they must be substantially less expensive. Calculations using SAM indicate that simply reducing service life from 35 years to 20 years while continuing to use a module cost of \$1.00/Wp to \$1.50/Wp increases the cost of electricity by approximately \$0.02/ kW·h. While that seems small compared to the cost of PV electricity today, it represents a 20% to 25% increase over the 2020 target price of \$0.08/ kW·h to \$0.10/ kW·h.

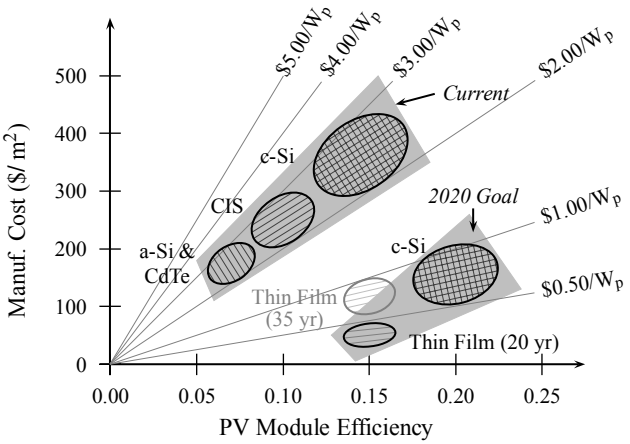

Figure 3: U.S. Department of Energy PV module cost goals for 2020, revised to reflect 20-year service life for thin-film modules.

5 Conclusions

The analytical model developed in this work shows that high solar cell efficiencies may be used to leverage area-related PV module cost in order to reduce power-related PV module cost, which is the predominant figure of merit for consumers and end-users purchasing PV modules. However, high efficiency cannot do it alone, and significant reductions in module manufacturing costs will also be required. Cutting the module manufacturing cost from \$3.00/W_p to \$1.00/W_p via efficiency alone would require tripling the power output — that is, efficiency — without incurring additional manufacturing costs. This is impossible for most technologies, extremely unlikely for the rest. Conversely, *all* existing commercial PV technologies can become cost-effective through manufacturing cost reductions, at least in theory. Increased efficiency simply reduces the magnitude of the required area-related cost reduction, as shown by the analytical model developed in this work. As a result, it is critically important that PV manufacturers in all technologies reduce area-related manufacturing costs. Thus, increases in area-related manufacturing cost A are counterproductive and, generally speaking, increases in efficiency should be accompanied by reductions in A if the goal of \$1.00/W_p manufacturing cost is to be realized.

Acknowledgements

The authors thank Dave Mooney, Steve Janzou, Mark Mehos, and the SAM development team for providing access and support for SAM.

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Photoluminescence Characterization of Phosphorous Gettering and Hydrogen Passivation in Multicrystalline Silicon Wafers

H. Sugimoto[a], M. Tajima[a], M. Dhamrin[b], K. Kamisako[b] and T.Saitoh[b]

[a]Institute of Space and Astronautical Science, Japan Aerospace Exploration Agency,
3-1-1 Yoshinodai, Sagamihara 229-8510, Japan
[b]Tokyo University of Agriculture & Technology, 2-24-16 Naka-cho, Koganei 184-8588, Japan
Tel & Fax: +81-42-759-8329, E-mail address: sugimoto@isas.jaxa.jp

Abstract

Effects of phosphorous gettering and hydrogen passivation on multicrystalline silicon wafers for solar cells were investigated by photoluminescence (PL) mapping and imaging. The averaged PL intensity became higher by the gettering and passivation. We confirmed that the crystallinity of the bottom wafer can be greatly improved. We also found that certain electrically non-active grain boundaries changed to active ones after the gettering, while the crystallinity of intra-grain areas was improved. Gettering and passivation were ineffective for defects related to dislocations.

1. Introduction

Phosphorous gettering (P-gettering) and hydrogen passivation (H-passivation) have recently become recognized as effective treatments to improve the quality of the multicrystalline Si (mc-Si) wafers for solar cells [1, 2]. For mc-Si solar cells, characterizing the grain boundaries and the intra-grain defects is essential to fabricate high conversion efficiency cells, because they act as the recombination center and degrade the cell performance. Although the effects of the P-gettering and the H-passivation on the mc-Si wafers have primarily been characterized by the averaged minority carrier lifetime, there are few reports about their effects on the grain boundaries and the intra-grain defects. Highly spatial resolved photoluminescence (PL) mapping of the latest mc-Si wafers has been performed by the authors [3, 4]. In the low minority carrier lifetime regions, the existence of intra-grain defects related to dislocations has been disclosed. We also confirmed that the grain boundaries did not primarily degrade the lifetime while the intra-grain defects cause extensive degradation. The effectiveness of P-gettering and H-passivation on these defects requires detailed clarification. In addition to PL mapping, PL imaging [5] is also a useful technique for characterizing the wafer quality. In this paper, we investigated the effects of P-gettering and H-passivation on the grain boundaries and the intra-grain defects by PL mapping and imaging.

2. Experimental Technique

We prepared three samples sliced horizontally from the top, center and bottom of a mc-Si ingot fabricated by the unidirectional solidification technique. They were boron doped with a resistivity ranging from 1.1 to 1.5 Ωcm, a thickness of 380 μm and a size of 4 x 4 cm^2. The sawing damage was etched off by HNO_3/HF solution.

PL mapping was obtained at room temperature using a system which had an accurate and fast X-Y stage with a position-repeatability as high as 0.3 μm and a maximum translation speed of 100 mm/s. The 532 nm line of a Nd:YVO_4 laser was used as an excitation source. Luminescent light was collected by an objective, passed through a spatial filter and band-pass filters with the transmission band of 1050–1230 nm, and then detected by a cooled photomultiplier. We took a whole wafer mapping of the intensity of

the band-edge emission with a spatial resolution of 100 μm. The excess carrier density was estimated to be from 5 x 10^{14} to 2 x 10^{15} cm^{-3}. For the PL imaging, we used a cooled CCD camera. The light excitation source was the LED array with a wavelength of 500 nm. Wafers passivated with silicon nitride (SiN_x) were used for the PL imaging. The power density of light excitation was about 50 mW/cm^2, and the excess carrier density was estimated to be from 2 x 10^{12} to 2 x 10^{14} cm^{-3}. The minority carrier lifetime was measured by the quasi-steady-state photoconductance (QSSPC) technique with an apparatus (Sinton Consulting WCT-100). Before the lifetime measurement, the surface was passivated by iodine in ethanol; the passivated layer was removed after the measurement.

For the experimental procedure, we first measured the lifetime by the QSSPC technique, and then performed the PL mapping. The P-gettering then proceeded at 1148 K for 30 min. After etching off the phosphorous diffusion layer, PL mapping was performed again; at this point we did not measure the lifetime in order to avoid the effects of the iodine passivation. Then, the H-passivation was carried out at 673 K for 15 min. Finally, the PL mapping and lifetime measurement were performed.

3. Results and Discussion

3.1 Changes in PL mapping before and after P-gettering and H-passivation

Photoluminescence mappings on the top wafer are shown in Fig. 1, where (a), (b) and (c) is as-grown, after the P-gettering and after the H-passivation, respectively. From the as-grown wafer, the dark-line PL patterns related to the dislocations [3] were obtained. We confirmed that the grain boundaries were not the active recombination center. The low PL intensity region on the periphery was due to the non-uniformity of the surface recombination velocity. PL intensity of the intra-grain areas increased after the P-gettering, and we found that certain grain boundaries became active recombination centers. The dislocation-related patterns hardly changed. After the H-passivation, the dislocation-related patterns and the active grain boundaries changed little, while the PL intensity of the intra-grain areas greatly increased. PL mappings on the center wafer represented a similar tendency, as shown in Fig. 2 (a)-(c). Figure 3 depicts the PL mappings on the bottom wafer. From the as-grown wafer, the bright-line PL patterns were obtained. We were able to see the dark-line core in the bright-line patterns by higher-resolution PL mapping. The width of the bright area was about 300 μm. The appearance of the bright-line pattern could be due to the high dopant distribution or to the gettering which occurred around the dark-line defects. After the P-gettering, the bright-line patterns vanished and only dark-line cores remained. We confirmed that the dark-line core was the grain boundary. The rate of increase of the PL intensity on the bottom wafer was higher than that of other wafers.

These findings show clearly that the crystallinity of the intra-grain areas can be improved by the P-gettering and H-passivation. However, certain grain boundaries which were not active recombination centers changed to active ones after the P-gettering. There is a possibility that the phosphor diffused deeply in these certain grain boundaries, and then the P-diffusion layer containing many gettered impurities remained after the etching. We also found that the P-gettering and H-passivation were ineffective for the dislocation- related defects.

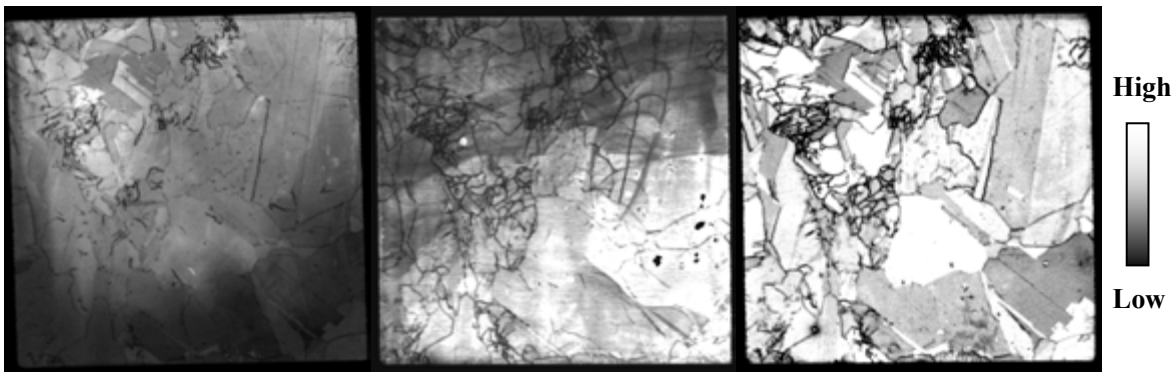

Fig. 1 PL mapping of top wafer: (a) as-grown (b) after gettering (c) after passivation. Whiter region indicates high PL intensity. Contrast of PL mapping was properly adjusted.

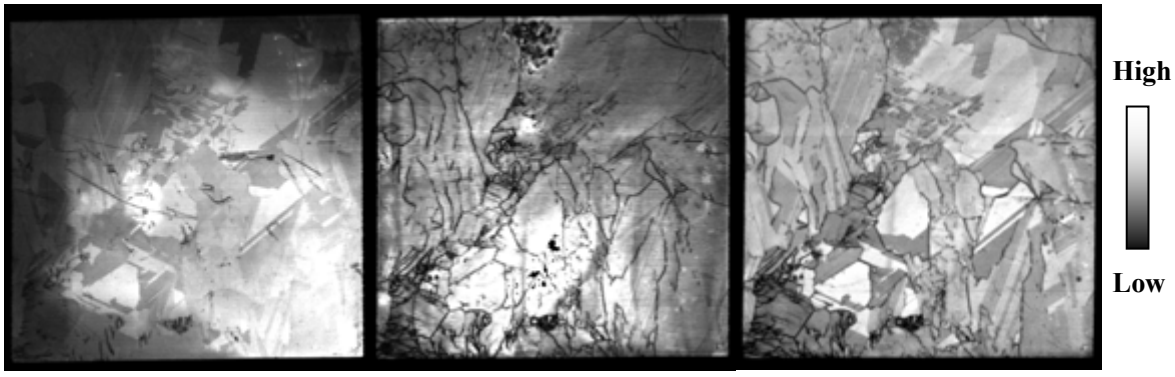

Fig. 2 PL mapping of center wafer: (a) as-grown (b) after gettering (c) after passivation.

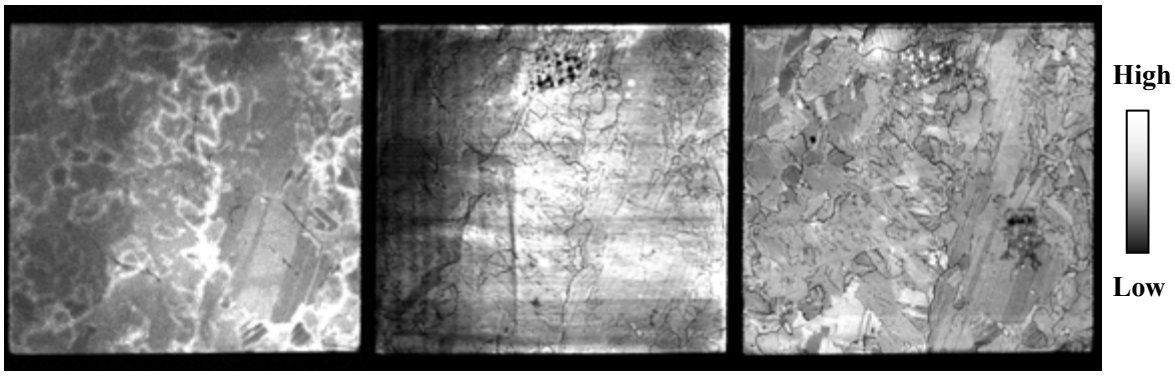

Fig. 3 PL mapping of bottom wafer: (a) as-grown (b) after gettering (c) after passivation.

3.2 Comparison between averaged lifetime and PL intensity

The changes in averaged PL intensity and the averaged lifetime after the P-gettering and H-passivation are illustrated in Fig. 4 (a) and (b), respectively. Although the lifetime of the center wafer was the highest of all, the top wafer had the highest PL intensity because of the difference of resistivity. The bottom wafer had the lowest PL intensity and lifetime, which indicated that it had poor crystallinity. The PL intensity of the top, center and bottom wafers became 1.4, 1.3 and 5.8 times higher after the P-gettering. We consider that this was because the bulk lifetime became high and the surface recombination

velocity became low. From our calculation, we estimated that the bulk lifetime of the top, center and bottom wafers became 1.8, 1.4 and 6.4 times higher, respectively. The surface recombination velocity seemed to change from about 1 x 10^4 to 8 x 10^3 cm/s. After the H-passivation, the PL intensity of the top, center and bottom wafers became 2.4, 3.0 and 3.2 times higher; this was mainly due to the surface passivation effect. The surface recombination velocity seemed to change from about 8 x 10^3 to 3 x 10^3 cm/s. From these facts, we confirmed that the quality of the bottom wafer can be greatly improved by the P-gettering and H-passivation.

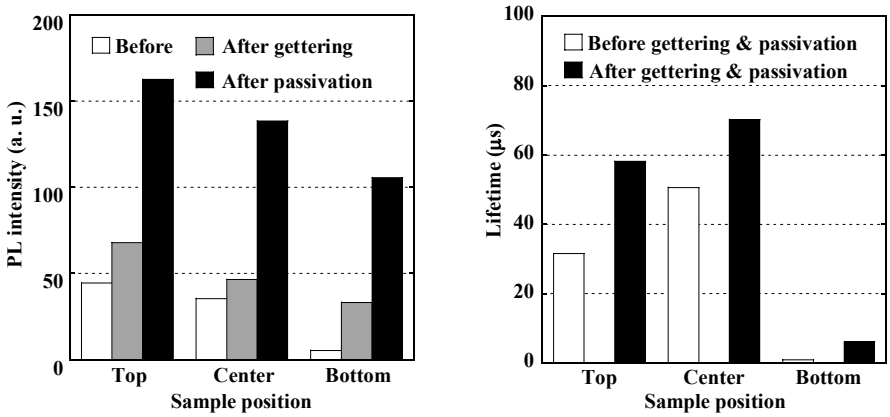

Fig. 4 Changes in (a) averaged PL intensity and (b) averaged lifetime after gettering and passivation.

3.3 PL imaging of P-gettered wafers

Photoluminescence image of the SiN_x passivated wafer after the P-gettering is shown in Fig. 5. We confirmed that the grain boundaries became the active recombination centers, while the non-gettered wafer had the non-active grain boundaries. The PL intensity of the intra-grain areas became higher than that of the non-gettered wafers. Although the data acquisition time of the PL imaging was faster than the PL mapping, the PL imaging was inferior in practical spatial resolution.

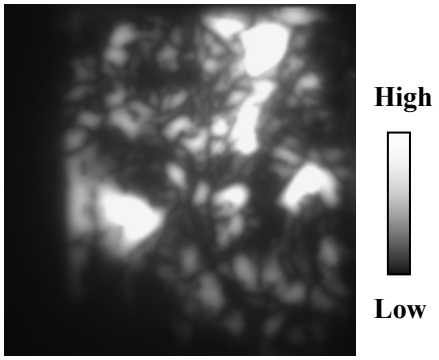

Fig. 5 PL image of SiN_x passivated wafer after P-gettering. (size: 5 x 5 cm, data acquisition time: 1 s)

4. Conclusion

In summary, the averaged PL intensity became higher by the P-gettering and the H-passivation. We confirmed that the quality of the bottom wafer can be greatly improved. We also found that the electrically non-active grain boundaries change to active ones following the P-gettering. The P-gettering and H-passivation were ineffective for the dislocation-related defects. We are confident that the present results will greatly contribute to the development of high quality mc-Si cells.

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Towards 3.5 grams / watt peak in BiThink Project

J.C. Jimeno, G. Bueno, R. Lago, I. Freire, L. Pérez, F. Recart, TiM-UPV/EHU (Spain)
J. Alonso, P. Sánchez-Friera, Isofotón, S.A. (Spain)
S. W. Glunz, G. Emanuel, R. Ruiz, A. Pohl, W. Wolke, M. Schubert, Fraunhofer ISE (Germany)
I. Gavilanes, M. Ezker, E. Zugasti, A. Turumbay, CENER (Spain)
H. Sato, J. Bragagnolo, NPC Europe GmbH (Germany), NPC America Corporation(USA)
P. M. Nasch, HCT Shaping Systems (Switzerland)
S. Ostapenko, A. Belyaev, W. Dallas, O. Polupan, USF (USA)
K. Albertsen, A. Shaikh, H. Kerp, J. Salami, Ferro Electronic Material Systems (The Netherlands, USA)

Abstract. BiThink is a project founded by the European Commission which target is to reduce the cost of PV silicon modules by developing a new technology based on bifacial cells and albedo modules. These bifacial cells are produced by an integral screen-printing process and using very thin silicon wafers. BiThink R&D activities cover the whole range from the slicing of silicon ingot to the lamination and testing of the module.

1. Introduction

BiThink is a project founded by the European Commission having transoceanic partners. The main BiThink's objective is to reduce significantly the cost of industrial PV silicon solar cells and modules. To this objective work has been focused on three different points:

- To use bifacial cells and albedo modules as a simple way to have more energy from the same silicon area without the use of optics or concentration
- To increase the number of sliced wafers per linear meter of silicon ingot
- To implement an efficient and simple manufacturing process, able to combine high mechanical yield values with reasonable cell efficiency

BiThink covers the whole chain of manufacturing solar modules, from the slicing of silicon ingots to the lamination of cells and testing of modules.

2. Bifacial cells and albedo modules

Bifacial solar cells and albedo modules were produced by Isofoton (patent from A. Luque, 1976) since 1981. These modules, with both active surfaces, are able to capture the light reflected by the surrounding areas to the PV system and convert it into electricity. Having a white painted floor or wall close to the PV modules the extra power, the albedo factor, would be over 30% of the conventional front incident light. This albedo factor would grow in cloudy climates or even be as large as 50% if a dihedron (floor plus wall) is used as reflective surfaces. Bifacial cells using a simple BSF structure present a symmetry in the photocurrent produced from rear or front illumination what ranges from 60% (for minority carrier diffusion lengths similar to the base thickness) to 100% for diffusion lengths over two times the base thickness, what is easily achievable on thin CZ n-type substrates.

The BSF bifacial structure is an excellent candidate to manufacture thin silicon solar cells. The lower coverage ratio of the contacts over both surfaces provides for low wafer stress values. Also the p+ emitter, which must be transparent, is made by boron diffusion introducing no surface stress. All these things result in a solar cell which is stress-free, and can be easily manufactured on thin silicon substrates. Finally, both textured surfaces provide an excellent light-trapping structure. Bifacial cells with thickness under 70 µm have been manufactured, using screen-printing techniques, without complicating the manufacturing process or the wafer handling.

3. Thin slicing of silicon ingots

Thin slicing of ingots is carried out by HCT Company using the Multi-Wire Slurry Slicing, technique, MWSS.. Figure 1 shows the record of cuts in this project, ranging from over 250 µm thick to lower than 100 µm. Wire diameters have been varied from 160 µm to 140 µm and pitch has been varied from 530 µm to 333 µm. It is remarkable that the Total Thickness Variation, TTV, which is a limiting variation in the lower achievable thickness, was independent of the final thickness of the wafer, as can be seen in figure 2.

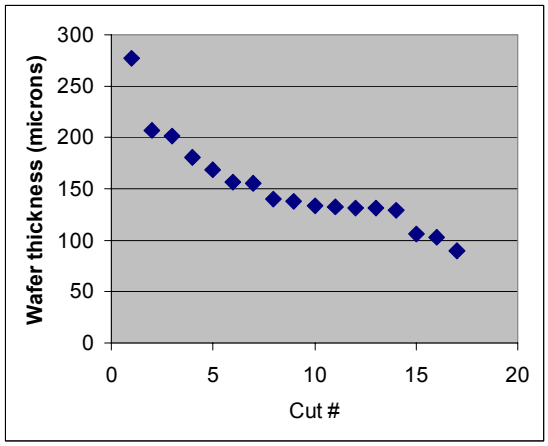

Figure 1. Cut summary

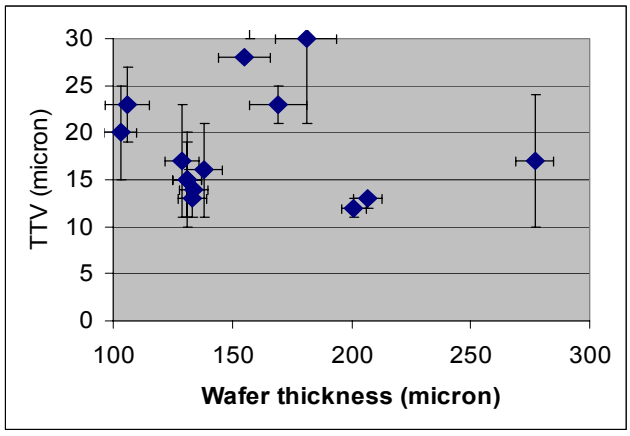

Figure 2. Total Thickness Variation vs. wafer thickness

The target of the project is to go from the current industrial value of 1800 wafers per linear meter of silicon ingot towards the range of 3500 – 4000 wafers per linear meter (w/m). An intermediate target of 2500 w/m has been reached from the very beginning of the project and current status is of 3000 w/m. A progression to 3500 w/m seems an achievable target, while 4000 w/m will require more substantial technology changes. Table I summarizes the progress of slicing technology in BiThink project.

		In production	BiThink 1st milestone	Current technology	Future technology
Wafer thickness	µm	**330**	**200**	**135**	**110**
Wire diameter	µm	160	160	160	140
Grit size	µm	15	15	15	10
Production yield	%	95	90	80(1)	80
Kerf loss	µm	198	198	198	178
Surface damage (1 side)	µm	23	23	23	15
Final wafer thickness	µm	285	155	90	80
Pitch average	µm	528	398	333	288
Raw material usage:					
wafer / cm		18.0	22.6	24.0	27.8
m^2 / kg		0.77	0.97	1.03	1.19

(1) This number is expected but not proven

Table I. Progress of slicing technology in BiThink project

4. Solar cell technology

Bifacial cells must be fabricated by a very simple and efficient process. That will give rise to high yield values and to a very robust process. Figure 3 shows the flowchart of cell processing. This process could be used over p or n type CZ or multi-crystalline silicon

Solar cell processing is based in screen-printing of dopants and electrical contacts. Screen-printing has been selected as base line technology for its low cost and its ability to be used in automated large production lines. However, having large efficiency values in screen-printed thin solar cells is not a trivial task. The main challenge is to produce a boron emitter without degrading the material properties and having low saturation currents after metallization. Close collaboration between Ferro, Fraunhofer ISE and TiM-UPV has been effective in this task. At the beginning of the project a low temperature (900ºC) short time process for boron diffusion resulted in p-type layers of around 0.15 µm. Contacting this layer by standard silver-based pastes results in high values in the junction recombination and very often in junction short-circuiting. A higher temperature processing yields 0.35 µm of junction deepth. The addition of extra components and reformulation of the silver-based paste has produced a relevant decrease in the junction recombination.

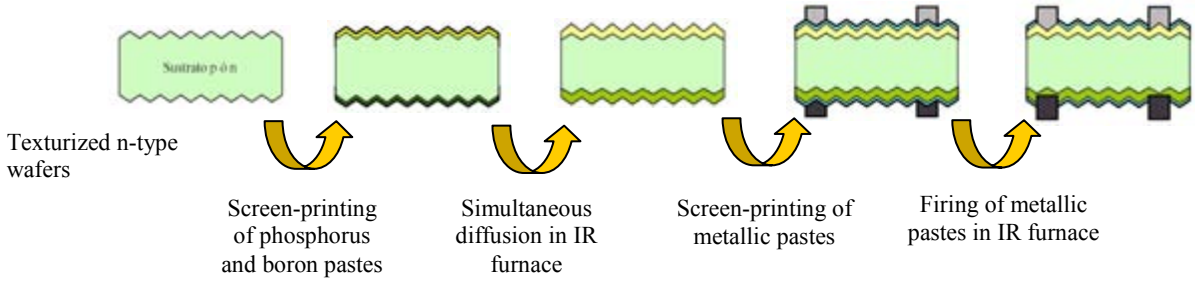

Figure 3. Manufacturing process of BSF bifacial solar cells

Current cell technology yields bifacial cells with efficiency under front side illumination greater than 15% and bifaciality values in the range of 60% if thin (lower than 130 μm) substrates are used. We anticipate that BiThink project will achieve 100% bifaciality and efficiency over 15.5%.

5. Yield and mechanical aspects

To maintain a high mechanical yield is a key task in BiThink project. To get this target the manufacturing process developed in BiThink only has four different kind of steps: chemical etch, screen printing of pastes, in line thermal processing or layer deposition and automatic loading and unloading of each system. Most critical steps are covered in BiThink project: CENER is working on evaluating handling conditions of thin wafers and in new chemical cabinets and carriers; NPC works in screen printers and automatic handlers. Results are very promising and currently wafers thinner than 100 μm could be printed without any yield reduction. A double-print process for thin lines with high aspect ratio was successfully tested resulting in contact lines of 24 to 30 μm height and 70 μm width, with no yield loss.

Increasing the mechanical yield will be based on a better knowledge of the mechanical behaviour of solar cells. BiThink is carrying out some work in mechanical modelling, mechanical strength of wafers in different process steps and early detection of mechanical defects. The Resonant Ultrasonic Vibration Technique, the stress detection technique developed by the University of South Florida, has been revealed as a powerful technique for the detection of cracks, both in CZ and multi-crystalline wafers. Resonant vibration is a function of the size, shape and crystallographic orientation of the wafer, but for a given technology it is possible to identify some resonant peaks having large stability between wafers. The simultaneous observation of three parameters from a chosen resonant peak: the resonant frequency, the amplitude of the vibration and the bandwidth, allows a clear identification of cracks of several millimetres in length. Work of the group at the University of South Florida runs quickly to a reduction of time for this crack detection that currently is in 2.6 seconds per CZ wafers. With this figures, or slightly lower, the RUV technique could be used for in-line detection of cracks and also in the optimization of automatic handling of solar cells in production lines.

The most critical defects causing the wafer breakage seem to be the surface damage, originated in the slicing process, and the periphery cracks due to mechanical stress in the solar cell processing. Both defects have been revealed to be detected by the RUV technique.

6. Results

Technology developed in BiThink project is demonstrating impressive numbers in low consumption of silicon: 3000 wafers can be obtained from a meter of silicon ingot and using a conservative 80% yield that means 1.06 m^2 of silicon wafers from a kilogram of silicon. Using the current BSF bifacial technology, with an efficiency of 15%, 60% bifaciality and using the lower albedo factor of 30%, gives a consumption of 4.3 grams/Wp without taking account the yield. Using the 80% of yield for the slicing process and 90% for the solar cell production this number is 5.9 g/Wp. Now, BiThink is running to 3.5 g/Wp.

Effect of single- and double-side PECVD SiN_x-induced Defect Hydrogenation in EFG Si

Kenta Nakayashiki, Vijay Yelundur, and Ajeet Rohatgi
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332

Sergei Ostapenko
Nanomaterials and Nanomanifacturing Research Center
University of South Florida, Tampa, FL 33620

Bala R. Bathey and Mark D. Rosenblum
SCHOTT Solar, Inc., Billerica, MA 01821

ABSTRACT

This paper reports on the systematic investigation of defect hydrogenation in EFG Si using a scanning photoluminescence (PL) technique. Cells fabricated with double-side hydrogenation process (PECVD SiN_x front and rear) showed no appreciable improvement in performance compared to those with standard fabrication process (SiN_x on the front and Al-BSF on the rear). After the double-side hydrogenation, SiN_x was removed from both sides and cells were completed with SiN_x on the front and Al-BSF on the rear. A scanning PL analysis on processed EFG Si wafers confirmed that double-side hydrogenation process neither improved bulk lifetime nor made the EFG Si materials more homogeneous relative to standard hydrogenation process. This suggests that sufficient hydrogen is able to penetrate Si from one side to hydrogenate most of the passivatable defects in the entire bulk.

INTRODUCTION

The cost of photovoltaic (PV) systems needs to decrease by about a factor of three to compete with traditional energy sources. Edge-defined film-fed grown (EFG) Si is a promising candidate for cost-effective PV systems because it eliminates the kerf loss and mechanical sawing process. However, as-grown EFG Si suffers from relatively high concentration of metal impurities, such as Fe and Ti, and structural defects, such as dislocations and grain boundaries. These defects lead to a very low as-grown carrier lifetime of 1-5 μs, which is not sufficient for producing high-efficiency cells. Therefore, it is necessary to enhance the carrier lifetime during the cell processing to reach the full potential of EFG Si for cost-effective PV. It has been shown in the literature that the plasma-enhanced chemical vapor deposited (PECVD) SiN_x-induced defect hydrogenation plays an important role in enhancing the carrier lifetime in mc-Si materials [1]. The implementation of PECVD SiN_x-induced defect hydrogenation in a rapid thermal processing unit has been shown to produce very high-efficiency 4 cm^2 ribbon Si solar cells (18.2% on EFG and 18.3% on String Ribbon Si) using photolithography front grid contacts [2],[3]. However, locally distributed unpassivated active defects still limit the cell performance [4]. Recently, Geiger et al. [5] observed a substantial scatter in carrier lifetime (<2 μs to >300 μs) within 5×5 cm^2 EFG and String Ribbon Si wafers after P diffusion gettering and microwave-induced remote hydrogen plasma processes using a spatially resolved lifetime mapping technique. In this study, an effort is made to improve the material homogeneity through the systematic investigation of single- and double-side PECVD SiN_x-induced defect hydrogenation by a combination of cell fabrication and scanning photoluminescence (PL) technique.

EXPERIMENT

In this study, 300 μm thick, B-doped 3-4 Ωcm EFG Si materials from SCHOTT Solar (Billerica, MA) were used. Large area (10×10 cm^2) EFG Si wafers were first cut into two pieces to ensure the identical crystallographic properties, as shown in Fig. 1(a). After the initial cleaning process, the samples were P diffused in a $POCl_3$ furnace to form 40-50 Ω/sq n^+ emitters. Sample set A (Cells 1-3) was processed using a standard fabrication sequence with single-side hydrogenation, and sample set B (Cells 4-6) was processed with double-side hydrogenation process. A SiN_x antireflection coating with a thickness of 800 Å and a refractive index of 2.0 was deposited on the front for set A and on the both side for set B. Set B was then annealed in a rapid thermal processing (RTP) unit at 750°C for 1 s with a temperature ramp-up rate of 75°C/s and a cooling rate of –40°C/s to inject hydrogen for defect passivation. The SiN_x layers were removed in a 10:1 H_2O:HF solution and another SiN_x layer was deposited on the front. Sample set A and B received a screen-printing of commercial Al paste (Ferro FX53-038) on the rear and Ag paste (Ferro CN33-455) on the front, followed by an anneal in an RTP unit to form Al-doped back surface field and Ag grid contacts. Cells were finally isolated into 2×2 cm^2 and forming gas annealed at 400°C for 10 min.

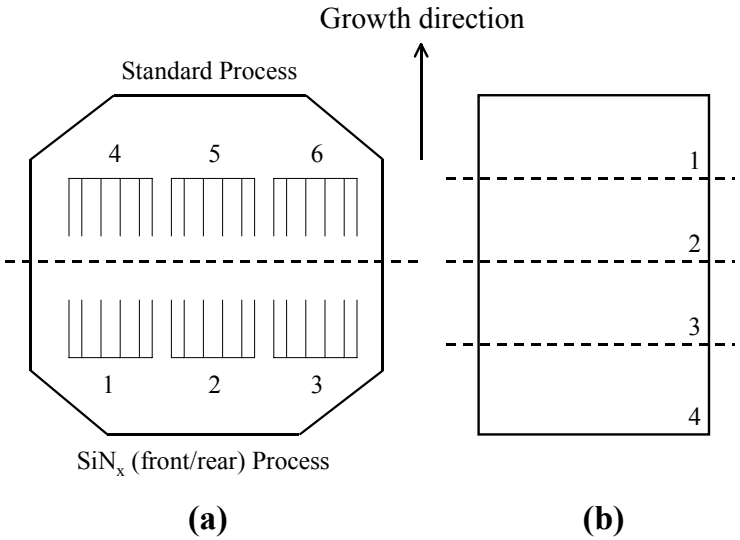

Figure 1: Schematic of EFG Si samples for (a) cell processing (cells 1-3 for standard process and cells 4-6 for intense hydrogenation process) and (b) PL measurements (1 as-grown, 2 P diffused and SiN_x on the front, 3 P diffused, SiN_x on the front and Al-BSF on the rear, and 4 P diffused and SiN_x on both side).

RESULTS AND DISCUSSION

The solar cell parameters were extracted by illuminated and shaded current-voltage (I-V) measurements. The average (15 cells on 5 wafers each) solar cell performance parameters are summarized in Table I. Surprisingly, there was no appreciable difference in cell performance between standard single- and double-side hydrogenation processes. This indicates that the nearly full effectiveness of defect hydrogenation process was achieved with SiN_x film deposited on the front only, and no appreciable enhancement was observed by injecting hydrogen from the rear side.

Table I: Average solar cell parameters for standard and intense SiN_x processes.

Process	**V_{OC} (mV)**	**J_{SC} (mA/cm^2)**	**FF**	**Eff. (%)**	**# of cells**
Standard	594	32.8	0.765	14.9	15
SiN_x (front/rear)	596	33.0	0.762	15.0	15

In order to support the effectiveness of PECVD SiN_x-induced defect hydrogenation, scanning photoluminescence (PL) measurements were performed on EFG Si materials subjected to single- and double-side hydrogenation. The PL spectrum was taken at room temperature using AlGaAs laser with a wavelength of 800 nm. For details of PL measurements, see [6] and [7]. Four small samples (5.0×2.5 cm^2) were cut from the same EFG wafer and prepared as follows: 1) unprocessed or as-grown, 2) P diffused and PECVD SiN_x on the front, 3) P diffused, PECVD SiN_x on the front and screen-printed Al on the rear, and 4) P diffused and PECVD SiN_x on the front and rear, as shown in Fig. 1(b). The P diffusion and SiN_x deposition conditions were kept same as described in previous section. Samples #2, 3, and 4 were annealed in an RTP unit at 750°C for 1 s for hydrogenation. After the thermal treatment, Al and SiN_x layers were removed in 2:1:1 H_2O:H_2O_2:HCl and 10:1 H_2O:HF solutions, respectively, and Al-BSF and P-doped n^+ layers were etched in 15:5:2 HNO_3:CH_3COOH:HF solution. The maps of PL intensity (band-to-band, I_{bb}, which is proportional to effective lifetime [6]) are shown in Fig. 2. The PL measurements were performed from the front as well as the rear side of the EFG samples to quantify the effect of defect passivation on bulk Si. The average values of PL intensity (I_{bb}) after each process step are summarized in Table II. Fig. 2 and Table II reveal that the combination of PECVD SiN_x on the front and Al-BSF on the rear produced maximum enhancement in PL response or carrier lifetime. In addition, there was no appreciable difference in the average PL response for single- and double-side hydrogenation. It is important to note that majority of the improvement came from single-side hydrogenation and Al-BSF. PL results are consistent with the cell results, which also showed no appreciable difference between the single- and double-side hydrogenation (Table I). This suggests that all the passivatable defects are passivated by hydrogen injected from the single-side SiN_x film. Therefore, additional injection of hydrogen from rear side does not play a role since the remaining defects are not affected by hydrogen. More research is needed to eliminate unpassivatable defects or enhance the effectiveness of SiN_x-induced defect hydrogenation in order to achieve a homogeneous distribution of carrier lifetime over the entire cell area.

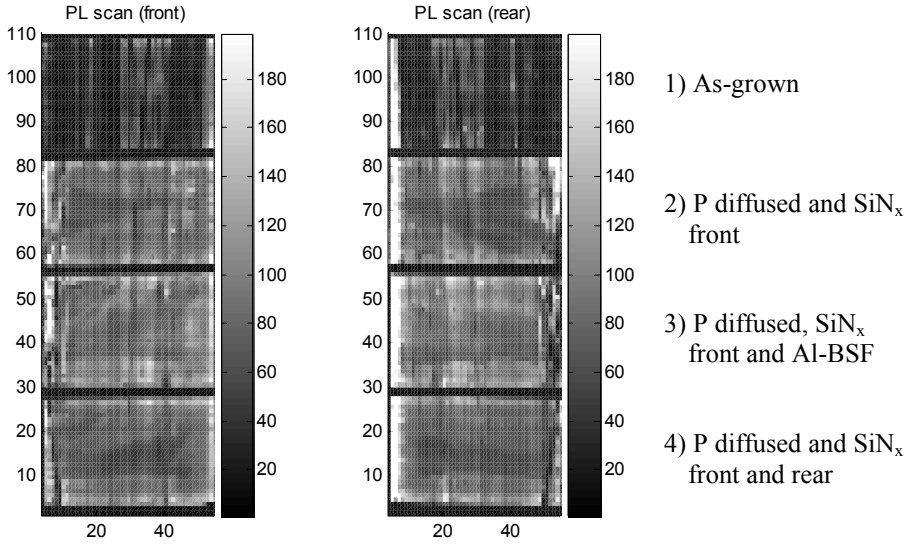

Figure 2: Front and rear PL scans (I_{bb}) of four EFG Si samples: 1) unprocessed or as-grown, 2) P diffused and PECVD SiN_x on the front, 3) P diffused, PECVD SiN_x on the front and screen-printed Al on the rear, and 4) P diffused and PECVD SiN_x on the front and rear.

Table II: Average values of PL intensities for I_{bb} in each step.

PL scan (I_{bb})	As-grown	P-diffused +SiN_x front	P-diffused +SiN_x front+Al-BSF rear	P-diffused +SiN_x front/rear
Front	27	77	88	75
Rear	36	84	91	78

CONCLUSIONS AND FUTURE RESEARCH

In this paper, single- and double-side SiN_x hydrogenation of EFG Si was investigated to improve the carrier lifetime and lifetime uniformity. There was no appreciable difference in the performance of cells fabricated with single- and double-side hydrogenation processes. This was consistent with the results of scanning PL measurements, which revealed that the injection of hydrogen from both side of wafer (front and rear) does not provide an enhancement in average carrier lifetime or PL intensity compared to sample with front side SiN_x only. This suggests that front side SiN_x hydrogenation is sufficient to passivate most of the passivatable defects in the entire 300 μm thick wafer. This also suggests that hydrogen injected from the front is able to reach the back side in sufficient quantity for defect passivation. However, PL maps show that there are still fair numbers of defects that are active. Further investigation is necessary to understand the remaining defects for achieving high-efficiency large-area EFG Si solar cells.

ACKNOWLEDGMENTS

The authors would like to thank Dr. Michael Stavola at Lehigh University for helpful discussions. This work was supported in part by the United States Department of Energy (Contract No. DE-FC36-00GO10600) and in part by the National Renewable Energy Laboratory (Contract No. AAT-2-31605-02).

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Investigation of the minority carrier lifetime before and after P diffusion and hydrogenation through SiNx:H layer deposition

Yongkook Park[1], M.C. Wagener[1], Jinggang Lu[1], N. Stoddard[2] and G.A. Rozgonyi[1]
[1]*North Carolina State University, Raleigh, NC 27695*
[2]*BP Solar, 630 Solarex Court, Frederick, MD 21703*

ABSTRACT
The minority carrier lifetime of cast multicrystalline silicon wafers was investigated before and after solar cell processing. For as-grown wafers, the lifetime is generally several μs, and had little change across different wafer locations. Currently it is believed that precipitates formed during the slow cooling following the growth are responsible for this phenomenon. For the processed wafer, some parts of the wafer showed enhanced lifetime, while other parts still showed the poor lifetime even though they were treated by P-diffusion gettering and hydrogenation. Secco etching suggested that the lifetime distribution of the processed wafers corresponds to the density distribution of dislocations and grain boundaries. It is suggested that the impurities released from precipitates during the annealing are gettered and hydrogen passivated effectively in the high lifetime regions involved in the low dislocation density regions, while for the low lifetime regions, the heavy dislocation networks seems to act as a barrier to gettering and hydrogen passivation.

I. INTRODUCTION
Multi-crystalline (mc)-Si solar cells occupy the largest portion of Si cell production and a considerable amount of mc-Si is composed of casted mc-Si. Drawbacks of cast mc-Si are that the nucleation of dislocations is caused by the excessive thermal stresses due to vertical temperature distribution during the growth and that impurities are incorporated into the ingot using lower-grade Si feedstock and silica crucibles. The distribution of dislocations is inhomogeneous because thermal stress exceeds the critical shear stress (CRSS) in grains of particular preferred orientations. Those with slip directions along the shear locally yield and relieve stress by local generation of dislocations [1]. Incorporated impurities are likely to form precipitates within the grains homogeneously as well as on GBs and dislocations heterogeneously resulting from the slow cooling rate of the solidification. Based on these facts, mc-Si includes structural defects such as dislocations (bundles of dislocations), GBs and impurities (impurity complexes, precipitates), which deteriorate the minority carrier lifetime significantly. For the sake of the enhancement in the lifetime, gettering and hydrogenation processes are applied to the solar cell substrate material. In this study, we explored what contributes to the enhancement in the lifetime after P-diffusion and hydrogenation in terms of defects and impurities.

II. EXPERIMENTAL
A pair of as-grown and P-diffused hydrogenated wafer was examined in this study. The wafers were adjacent in the brick and have the same grain structure. They were B doped with a concentration of ~10^{16}cm^{-3}, as determined from C-V measurements. The grain size

within a given wafer ranged from several millimeters to several tens of millimeters. Surface saw damage still remained on the as-grown wafer and it was polished before Al Schottky diodes were prepared on the surface for DLTS (Deep Level Transient Spectroscopy). Microwave PCD lifetime mapping was performed and during PCD mapping, the wafer was immersed in a 7% HF solution to passivate the surface for as-grown wafers. The step size used for generating the lifetime map was 0.5mm. A 904 nm GaAs laser with a Si penetration depth of ~30μm was used as a carrier injection source. After PCD mapping, the sample was Secco etched for 1 min. A scanned image was taken to record the dislocation and grain structure distribution for correlation with the lifetime distribution map in addition to Nomarski microscopy.

III. RESULTS AND DISCUSSION

The minority carrier lifetime measurements were carried out for the as-grown wafer and the wafer undergoing phosphorus diffusion and hydrogenation. The wafers were adjacent in the brick and have the same grain structure. In the case of the as-grown wafer, there is not much of spatial variance in the lifetime, while the processed wafer showed a relatively big deviation between high and low lifetime regions compared to the as-grown wafer. In addition, the lifetime of some portions (labeled H in Fig. 1(b)) of the processed wafer was enhanced during solar cell processing, while other regions (L in Fig. 1(b)) showed little improvement. Based on these observations, both the high lifetime region and the low lifetime region were Secco etched to investigate the dislocations and GBs densities as in Fig. 2. It was obvious that the high lifetime regions correspond to the low dislocations densities area and the low lifetime regions are involved in the dislocations networks. From this point, we can estimate the dislocations densities could play a dominant role in affecting the lifetime for the processed wafer. On the other hand, the fact that H and L regions of the as-grown wafer have almost the same lifetime even though there is difference in dislocations densities suggests that impurities or precipitates are likely to be responsible for this phenomenon.

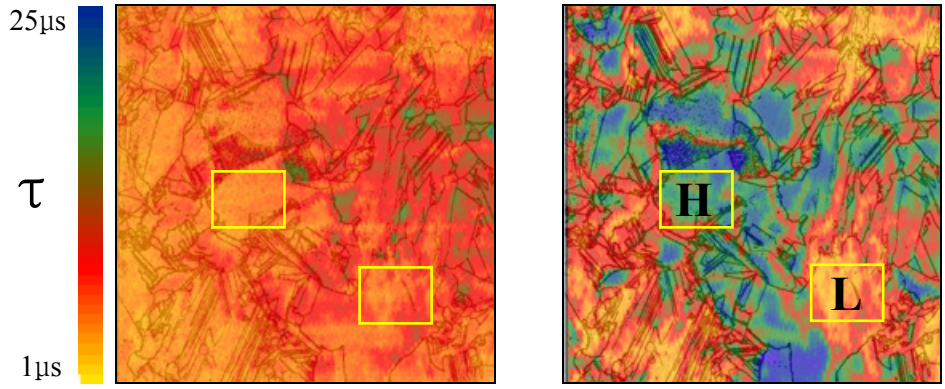
A DLTS study was performed to explore what kinds of impurities are present in the as-grown wafer and the processed wafer. At first, no DLTS peaks were detected in the as-grown wafer, which means the dissolved impurities concentrations are less than 2×10^{11} cm^{-3}. (The sensitivity of DLTS is given by the following equation

$$\frac{\Delta C}{C} = \frac{1}{2}\frac{N_T}{N_A}$$

where $\Delta C / C \sim 10^{-5}$ for our DLTS setup with N_A(boron doping level)=$10^{16}cm^{-3}$.)

Metal precipitates within the grains or at the defects sites are likely to exist due to the slow cooling rate during the growth.

Under the assumption that the metal precipitates prevail over the dissolved impurities, the sample from the as-grown wafer was annealed at 900°C for 30 min. to dissolve



(a) as grown wafer (b) the processed wafer

Fig. 1. Lifetime map and grain boundary structure overlay of one portion of a $5\times5in^2$ wafer

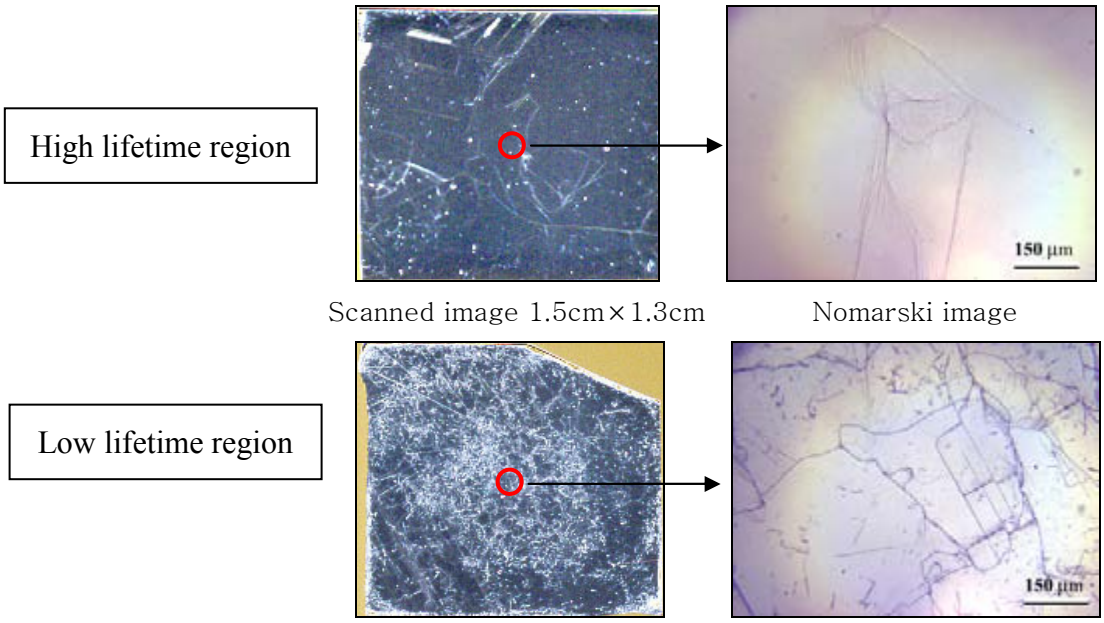
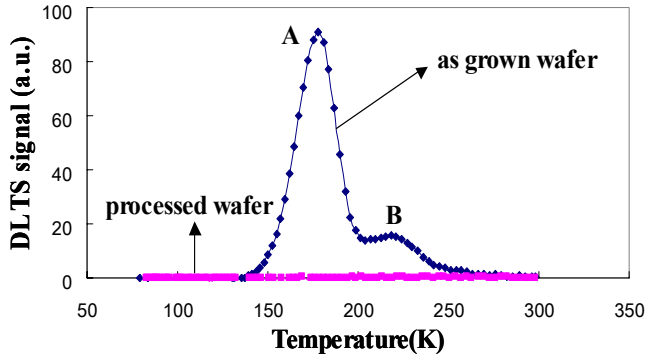


Fig. 2 Nomarski and scanned images of Secco etched high lifetime region (H) and low lifetime region (L)

the precipitates and then it was quenched. Afterwards, DLTS was done again for the identification of the incorporated impurities and two peaks are revealed. Currently, the lager peak (A in Fig. 3) is thought to be Cr-B pair [2]. The solubility limit of chromium at 900°C is about $10^{13}cm^{-3}$ and the ratio of Cr-B to Cr is close to one at room temperature under the boron concentrations are approximately $10^{16}cm^{-3}$. Based on this, the trap density resulting from the dissolved impurities at high temperature should be in the level of $10^{13}cm^{-3}$ in agreement with our DLTS results. The energy state of the chromium present in the interstitial site is above the middle of the band gap (E_c - 0.23eV) and this information can

be used in identifying the trap. For another small peak (B in Fig. 3), the identification is yet to be determined.

In case of the processed wafer, no peaks were detected. It is believed that this might be related to the gettering processes, and the cooling rate after co-firing. From the results of the lifetime change before and after processes and DLTS analysis, it can be inferred that impurities dissolved from precipitates are gettered in n+ regions by phosphorus diffusion gettering and passivated by hydrogen during annealing. (It is known that precipitates are difficult to getter by P diffusion gettering so they should be dissolved during annealing or gettering process.) It is believed that dislocations play a dominant role in affecting the gettering and passivation processes. This agrees with the etching results showing the relation between the dislocations density and the lifetime. The lifetime of heavy dislocation networks regions is little improved after processes, perhaps because dense dislocation network limits effective impurity gettering.



	A	B
E_A (eV)	$E_V + 0.266$	$E_V + 0.515$
σ_P (cm^{-2})	2×10^{-16}	1.4×10^{-15}
N_T (cm^{-3})	3×10^{13}	6×10^{12}
Identity	Cr-B	?

Fig. 3 DLTS spectra and peak assignment of the as-grown wafer after annealing and quenching, and the as-received processed wafer.

IV. CONCLUSIONS

Precipitates seem to be dominant in affecting the lifetime for as-grown wafer. For the processed wafer, it is believed that dissolved impurities during the annealing are gettered and hydrogen passivated so that the densities of the dislocations and GBs are responsible for the improved or poor lifetime. Further study is required to identify the impurities, and the behavior of the precipitates according to the annealing temperature and time, more detailed study of gettering and hydrogen passivation with the specific impurities are needed to fully understand the change in the lifetime before and after the processes.

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Low-cost, Low-cost, High-Throughput Emitter Formation Technologies Using a Ceramic Roller Hearth Metal-Free Diffusion Furnace for Crystalline Silicon Solar Cells

D.S. Kim[1], B. Rounsaville[1], A. Pandey[1], A. Ebong[1], V. Upadhyaya[1], A. Upadhyaya[1], K. Tate[1], V. Yelundur[1], A. Rohatgi[1], and J. Simpson[2],

[1]University Center of Excellence for Photovoltaics Research and Education
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332-0250
[2]SierraTherm Production Furnaces Inc, Watsonville, CA 95076

Abstract

A novel ceramic roller hearth furnace has been used for the emitter formation of c-Si solar cells to avoid metal contamination from a metal belt. A comparison of phosphorus doped emitters formed in a ceramic roller hearth furnace, a metal belt furnace, and a $POCl_3$ tube furnace is presented in this study. Emitters formed in the ceramic roller hearth and the metal belt furnaces used dilute phosphoric acid as a dopant source. Doping profiles, carrier lifetimes, and Joe values are compared. The results show that a carrier lifetime in excess of 300 μs can be maintained after the 45 Ω/sq emitter diffusion at 870°C in the ceramic roller furnace. The best solar cell with emitters formed in the ceramic roller furnace shows comparable V_{oc} and J_{sc} to the best cell with $POCl_3$ emitter. However the cell efficiency was 16.4% compared to the 17.2% $POCl_3$ cell due to lower fill factor. Limited data shows that optimization of the contact firing condition for the shallow emitter formed in ceramic furnace can lead to an efficiency comparable to the cell with $POCl_3$ emitter. Belt diffused emitters showed same belt-induced contamination when the uncoated wafer side is in direct contact with the belt during the diffusion.

Introduction

The formation of the p-n junction in c-Si solar cells strongly impacts the cell performance as well as the cell manufacturing cost. The emitter diffusion process in a conventional tube furnace involves deposition of P_2O_5 on the wafer using a liquid $POCl_3$ source followed by drive-in of phosphorus into the wafer. $POCl_3$ diffusion is widely used to form n^+ emitter, in spite of limitations in throughput and safety, because of low contamination and availability of equipment from the semiconductor industry. As the production capacity of c-Si solar cells increases and the cell thickness decreases, the demand for inline cell manufacturing processes will continue to grow rapidly. Inline manufacturing offers several advantages including the reduction of wafer breakage by minimizing wafer handling steps, lower cost processes, and the ease of automation. The inline emitter formation involves dopant coating followed by a drive-in. Spray coating of phosphoric acid in conjunction with drive-in in an IR metal belt furnace is frequently used in the PV industry for inline emitter formation process [1, 2]. However, the conventional metal belt furnace can lead to performance degradation due to metal contamination from the metal belt [3]. Although high-efficiency cells have been reported using metal belt furnace for emitter diffusion [4], the metal belt must be maintained or replaced regularly to reduce the risk of metal contamination.

In this study, we adapted a ceramic roller hearth furnace developed by SierraTherm Production Furnaces Inc. for dopant drive-in and inline emitter formation. This furnace is

equipped with ceramic rollers to avoid metal contamination from a metal belt. The ceramic roller hearth furnace requires less power consumption and no water cooling system since the ceramic rollers spin at stationary positions whereas the metal belt exchanges thermal energy between high temperature zones and room temperature. This may also lead to a more stable furnace temperature. In this study, contamination of c-Si wafers during heat treatment is studied by measuring the effective lifetime in silicon wafers before and after annealing in the ceramic roller furnace and in the metal belt furnace. In addition, a phosphorus emitter diffusion process for screen printed c-Si solar cells was developed using the new ceramic roller furnace with minimal lifetime degradation.

Experimental Method

In this study p-type (100), 1.3-2 Ω-cm, 5 in, pseudo square textured float zone (FZ) wafers were used for large area (149 cm^2) solar cell fabrication as well as the study of the emitter sheet resistance and the effective bulk lifetime as a function of process parameters. Small area cells (12 cm^2) were also fabricated on 4 inch, 1.3-2 Ω-cm p-type (100), FZ wafers. N-type, 500 Ωcm FZ wafers were used to measure the emitter saturation current density (J_{oe}). Saw damage on the as-cut wafers was removed by etching in 30% potassium hydroxide (KOH) solution for 3 minutes at 85°C followed by anisotropic etching in the mixture of KOH and isopropyl alcohol (IPA) for texturing. The textured silicon wafers were cleaned in 2:1:1 H_2O: H_2O_2: H_2SO_4 and 2:1:1 H_2O: H_2O_2: HCl solutions for 5 minutes followed by 3 minute DI water rinse after each cleaning. For inline diffused wafers, the surface of the wafer was oxidized in sulfuric acid (H_2SO_4) for 5 min to obtain hydrophilic surface prior to coating with phosphoric acid. The phosphoric acid was prepared by mixing commercial phosphoric acid (Aldrich, 99.9995%) with D.I. water and a solvent, which was used to enhance the coating uniformity on the textured surface. The phosphoric acid was coated on the one side of the wafers using a spin coater. We have successfully used a spray system to provide uniform coating of phosphoric acid, but the spin coater was adopted in this study to coat different size wafers in a simple way. The wafers coated with phosphoric acid were annealed at temperatures in the range of 870^{o}C – 1000^{o}C in a metal belt furnace and in the ceramic roller furnace (SierraTherm Inc.) that has eight heating zones. The temperature of each zone of the ceramic roller furnace was set independently to obtain uniform temperature from third zone to sixth zone. The drive-in time was controlled by adjusting the spin speed of ceramic rollers. Phosphorus diffusion was also performed in a $POCl_3$ furnace at 870°C for comparison. The phosphosilicate glass (PSG) was removed in a dilute HF solution after emitter diffusion. A SiN_x single layer antireflection coating with a thickness of 800 Å and a refractive index of 2.0 was deposited in a low-frequency (50 KHz) plasma-enhanced chemical vapor deposition (PECVD) reactor at 425 °C. The front and rear contacts were formed by screen-printing commercial Ag paste on front and Al paste on the back, followed by firing in the IR metal belt furnace. The process sequence is summarized in Fig. 1.

The carrier lifetimes in the wafers and emitter saturation current density (J_{oe}) of the diffused emitters were measured using Sinton's quasi-steady-state photoconductance (QSSPC) tool. Secondary ion mass spectroscopy (SIMS) analysis was performed to study the phosphorus doping profile after diffusion.

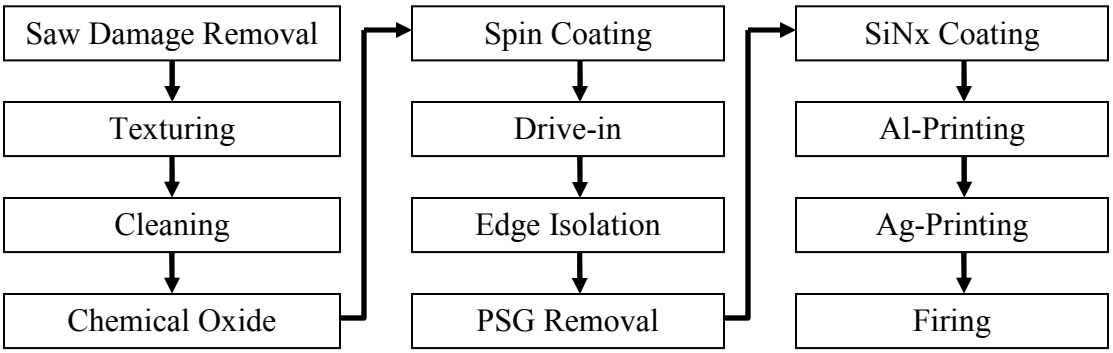


Fig 1. Process sequence for fabricating screen-printed solar cells with spray diffused emitter.

Properties of Emitters Diffused with Phosphoric Acid

Fig. 2 shows the SIMS doping profiles of diffused emitters at 870 ^{o}C in the ceramic roller furnace before and after PSG removal. The thick layer with high phosphorus and oxygen concentrations is associated with the PSG layer formed on the emitter surface. The emitter depth with sheet resistance of ~45 Ω/sq (870°C/20min) was about 0.4 µm, which is 0.1-0.2 µm shallower than $POCl_3$ emitter used in this study. When the diffusion time in the ceramic roller furnace at 870°C was reduced to 5 min, the emitter depth in the ceramic roller furnace decreased to 0.2 µm and the sheet resistance increased to 80 Ω/sq. Joe values for conventional emitters (45 Ω/sq.) and higher sheet resistance emitters (70-100 Ω/sq.) formed in the ceramic roller furnace and the $POCl_3$ tube furnace on textured and planar surfaces with SiNx surface passivation were determined by effective lifetime measurements. Table 1 shows that for a comparable sheet resistance and surface condition, the Joe of the emitters diffused in the ceramic roller furnace were comparable to those diffused in the $POCl_3$ tube. The Joe of 45 ohm/sq emitters formed in the ceramic roller furnace on textured wafers was 353 fA/cm^3, which corresponds to an open circuit voltage (Voc) of 655 mV assuming Jsc a of 35 mA/cm^2.

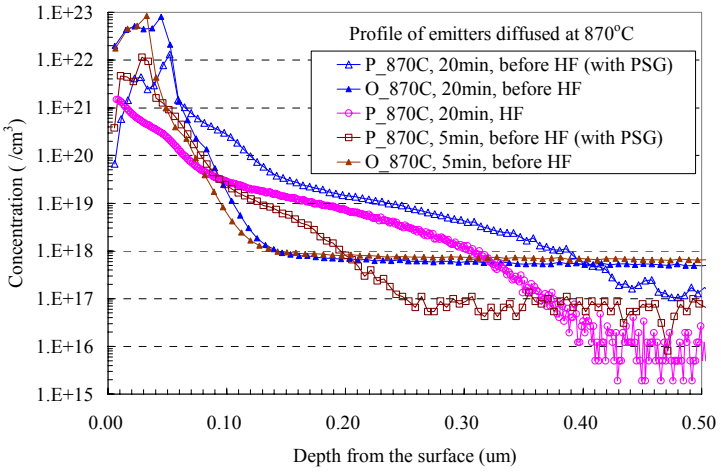


Fig. 2. SIMS profiles of phosphorus and oxygen before and after removal of PSG layer. The diffusion was performed in inline furnace at 870 ^{o}C for 20 min and 5 min using 4% H_3PO_4 as the dopant.

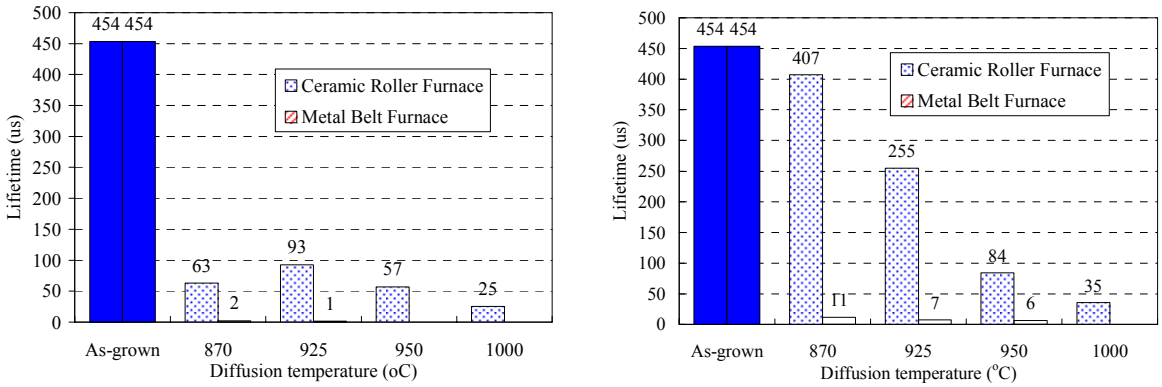
Table 1. Joe values of emitters diffused in the ceramic belt furnace. Phosphoric acid was used as a doping source.

Diffusion	Surface	Diffusion		Sheet Res. (ohm/sq)	Joe (fA/cm^2)	Voc Limit (mV)
		Temp. (^oC)	Time (min)			
Ceramic Roller	planar	870	20	45	256	663
Ceramic Roller	textured	870	20	45	353	655
Ceramic Roller	planar	870	5	72	219	667
Ceramic Roller	textured	870	5	83	319	657
POCl3 Furnace	textured	845	37	100	115	684
POCl3 Furnace	planar	870	37	45	244	664

Effect of thermal budget on the sheet resistance and the carrier lifetime in the ceramic roller furnace

The effective carrier lifetime in 2 Ω-cm bare FZ wafers was measured as a function of annealing temperature in the ceramic roller furnace with I_2/Methanol surface passivation. No dopant was applied in this experiment. Fig. 3 (a) shows that the average lifetime in the as-grown wafer decreased from 450 μs to 25 μs when the anneal temperature increased to 1000°C. For the metal belt furnace, the lifetime decreased to 1-2 μs with no dopant applied to the wafer (Fig.3(a)). It should be noted that the metal belt furnace used in this study is also regularly for Ag and Al contact firing. It appears that metal impurities diffuse into the silicon wafer during the annealing process in the metal belt, causing a degradation of the carrier lifetime. The results in Fig. 3 (a) show that the ceramic roller hearth furnace can also degrade the effective lifetime after annealing. However, at this time it is not clear if the decrease in lifetime is caused by impurities from the furnace or from the compressed air since high purity air was not used in this study. Lifetime difference between the metal belt furnace and ceramic roller furnace suggests that additional impurities from the metal belt can significantly reduced the bulk lifetime.

Nest, silicon wafers coated with phosphoric acid were annealed at the same temperatures in the ceramic roller furnace and the metal belt furnace to determine if the presence of dopant helps in gettering to preserve the lifetime. As shown in Fig. 3 (b), the lifetime was much higher when phosphoric acid was coated before the annealing, especially in the case of the ceramic roller furnace. When metal belt furnace is used, the lifetime improves by gettering but was still much lower than as-grown lifetime. The results in Fig. 3 (b) suggest that diffusion of phosphorus using phosphoric acid may getter the metal impurities from the silicon wafer to improve the carrier lifetime. The phosphorus gettering was not able to remove the metal impurities completely during the diffusion in the ceramic roller furnace, but it appears to have maintained a lifetime comparable to as-grown lifetime when the wafer was annealed at 870 ^oC for 6 min. Equally important is the fact that the diffusion temperature of 870 ^oC in the ceramic roller furnace can be used to form emitters with sheet resistances in the range of 45-90 ohm/sq by varying diffusion time from 4 to 20 min.



(a) (b)

Fig. 3 Lifetime in 2 Ω-cm FZ wafers as a function of annealing temperature. The wafers were annealed in the ceramic roller hearth IR furnace and the metal IR furnace. The diffusion time was set to 6 min for all temperatures. The phosphoric acid (4%) was coated on the front side in case of (b).

Effect of emitter formation technique on the cell performance

Screen printed solar cells with emitters diffused in $POCl_3$ tube furnace ($POCl_3$ Cell), metal belt furnace (Metal Belt Cell) and ceramic roller furnace (Ceramic Roller Cell), were fabricated using a process sequence shown in Fig. 1. The Ag paste and the contact firing recipe were optimized for the $POCl_3$ emitter, which has a deeper junction. The performance of best cell for each emitter is summarized in Table 2. The solar cells with emitters diffused with phosphoric acid yielded lower fill factor due to high series resistance. The best Ceramic Roller Cell showed higher Jsc than the best $POCl_3$ Cell due to shallower emitter. The Voc of the Ceramic Roller Cell was comparable to that of $POCl_3$ Cell. It is expected that the Ceramic Roller Cell can yield a comparable efficiency to the $POCl_3$ Cell if the Ag paste and firing recipe are optimized for the shallow emitter formed in the ceramic roller furnace. The $12cm^2$ Ceramic Roller Cells gave efficiency over 17 % when annealed in forming gas which improves the FF. The low V_{oc} and J_{sc} of the Metal Belt Cell are caused by the degradation in bulk lifetime during the emitter formation. Note that the metal belt furnace is routinely used for contact firing process and can introduce metal impurities into the wafer. We also found that the diffusion of metal impurities into the wafer can be reduced by coating phosphorus source on both sides of wafers before diffusion [3]. The lifetime dependence on diffusion method during the $POCl_3$ diffusion was also repeated by Schneider et al. [5]. This study shows that a combination of ceramic roller furnace and appropriate thermal budget can maintain a high lifetime with one side phosphoric acid coating.

Table 2. Performance of best cells with emitters formed in the $POCl_3$ tube furnace, the ceramic roller furnace, and the metal belt furnace. Two $12cm^2$ cells were annealed in forming gas.

Emitter Diff	Area (cm^2)	Sheet Res. (Ω/sq)	Voc (mV)	Jsc (mA/cm^2)	FF	Eff (%)
$POCl_3$ Furnace	149	45	625	34.9	0.787	17.2
Ceramic Roller	149	45	622	35.2	0.750	16.4
Ceramic Roller	12	38	624	35.5	0.767	17.0
Ceramic Roller	12	76	625	36.1	0.767	17.3
Metal Belt	149	45	600	33.8	0.724	14.7

Conclusions

A new phosphorus diffusion furnace with ceramic rollers has been developed and used in this study for the emitter formation of crystalline silicon solar cells with significantly reduced impurity contamination. The diffusion furnace features ceramic rollers that transport wafers into an open-ended IR- lamp heated furnace. In this study, a process has been developed for emitter formation using the ceramic roller diffusion furnace and low-cost phosphoric acid as the dopant source. It is found that the carrier lifetime decreases to <100 μs when the wafer is annealed in the ceramic roller furnace *without* the phosphoric acid dopant on the front side. However, >300 μs is achieved after diffusion at 870°C with phosphoric acid dopant source. In contrast the lifetime in the FZ wafers annealed in the metal belt furnace fell below 90 μs, with or without phosphoric acid coating on the front side. Emitters diffused in the ceramic roller furnace showed efficiencies as high as 16.4%. This efficiency is lower than the best cell (17.2%) formed with the $POCl_3$ emitter because of significant loss in FF, in spite of similar V_{oc} of 622 mV and higher J_{sc} of 35.19 mA/cm^2. This is because contact firing was not optimized for shallow emitter obtained in the ceramic roller furnace. The optimization of the contact firing can lead to cell efficiencies comparable to the cell with $POCl_3$ emitter. We conclude that the ceramic roller hearth furnace is a very promising tool that can substantially reduce impurity contamination during the emitter diffusion for crystalline silicon solar cells.

Acknowledgements

The authors would like to thank Bob Reedy at National Renewable Energy Laboratory for SIMS analysis.

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N-type silicon solar cell with Al back junction: results and modeling.

V. D. Mihailetchi, L. J. Geerligs, S. De Iuliis
ECN Solar Energy, P. O. Box 1, 1755 ZG Petten, The Netherlands
email: mihailetchi@ecn.nl

Abstract

We present results on n-type silicon cell process development based on the Al-back junction concept using low cost fabrication techniques. Excellent results have been obtained on floatzone silicon wafers with efficiency in excess of 16.4%. Moreover, model calculations allow us to identify the potential for further enhancement of the cell efficiency above 17.5% by improving front surface passivation. After some optimization, high efficiencies may be conceivable on n-type multicrystalline substrates as well.

Introduction

More than 90% of the commercial solar cells fabricated so far are based on p-type doped silicon material that was received from the electronic industry. Nowadays over 80% of the produced solar cells have a homogeneous emitter, a PECVD-SiN layer as antireflective coating, and screen printed contacts on both sides. For the backside, an aluminum paste is used to create a back surface field during the contact co-firing. Currently there is much interest in the development of low-cost industrial cell processing based on n-type (multicrystalline or monocrystalline) silicon wafers. This interest is based on several developments and findings, such as:

- High carrier lifetimes in n-type multicrystalline wafers, often significantly higher than in p-type wafers.
- Theoretical and experimental evidence for less recombination-active defects in n-type silicon [1].
- Tolerance of n-type silicon to high temperature processing with respect to p-type silicon [2].
- Shortage of silicon feedstock for the PV industry, and an unused potential supply of n-type silicon waste.
- New materials (ribbons, metallurgical feedstock) for which the above aspects favor n-type doping.
- Need for technology development towards very thin wafers and high cell efficiency, for which n-type silicon based solar cells may have advantages.

A few solar cells concepts based on n-type Si materials are under investigation. One of these concepts is the Al back-junction cell.

In this paper we present results on n-type cell process development based on the Al back-junction concept (also known as phostop, as introduced by Ebara [3]). The phostop represents a fast way, from industry side, to move from p-type to n-type substrates because of the possibility of maintaining the same process sequence. The only difference is that during the phosphorus diffusion step a front surface field is created instead of an emitter and during the contact co-firing the aluminum back junction is formed. Therefore this process has received much attention recently, on a process similar to the one we present here [4, 5] and on smaller size lab process [6, 7]. We developed the cell process on 148.5 mm^2 Float Zone (FZ) n-type monocrystalline silicon wafers, but results on 156.25 mm^2 industrial n-type multicrystalline silicon (mc-Si) wafers are also presented.

Cell Fabrication

The cell process we used is based on in-line processing for diffusion, co-firing, and on process steps which can be industrialized. The rear junction as well as the front surface field (FSF), anti-reflection coating (ARC), and the metallization, are based on industrial standard n^+np^+ process, as shown in Figure 1. It starts with a wafer thinning [8] to about 150-180 μm followed by an isotexture etch of the surface. Then the front-surface field is formed by phosphorus diffusion in an infrared conveyor belt furnace from a spin-on source, resulting in 50-55 Ω/sq. front surface field. After phosphorus glass removal the PECVD SiN anti-reflection coating was deposited on front, followed by rear side etch and edge isolation [5]. Subsequently, the silver grid was screen-printed on SiN front side, followed by screen-printing of Al on the whole rear side of the cell. Both contacts were co-fired in an infrared conveyor belt furnace, thus forming also the back junction.

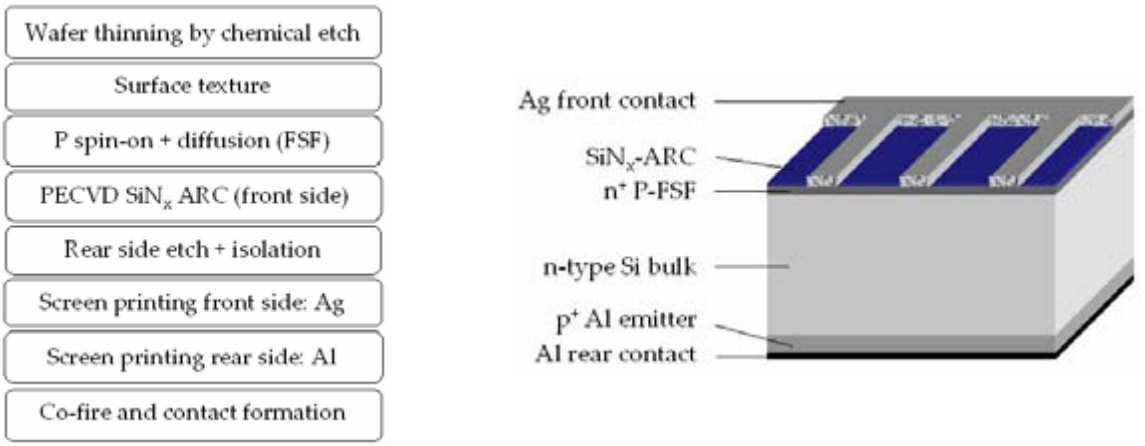

Figure 1. Process flow chart (left) and the layout of Al back junction solar cell (right).

Results and discussion

Table 1 summarizes the solar cell parameters of the best results obtained for mc-Si and FZ substrates. The highest efficiency of monocrystalline substrates is obtained for higher substrate resistivity (it is in fact nearly identical to the efficiency reached by Kopecek et al. [4] on similar substrates and with slightly different cell process). This is in agreement with model calculations [4,8], which show that, in order to benefit from the full potential of this type of solar cells, the wafer resistivity should be higher than 10 Ωcm (with a thickness of less than 200 μm). On the other hand it is important to know what limits the efficiency at lower substrate resistivity, especially for multicrystalline substrates. To understand this, we have investigated the internal quantum efficiency (IQE) of the cells from Table 1. Figure 2 (left) shows the experimental IQE (symbols) together with the PC1D fit (lines) using measured front doping profile and surface reflection, and assuming a constant Al doping profile for the rear junction. The relevant fit parameters for the modeling are the bulk lifetime and the front surface recombination velocity (SRV). Since for monocrystalline wafers the bulk lifetime is very high (>1 ms), it does not limit the IQE at lower wavelengths regime, where it is remaining completely determined by the SRV. The fit to experimental data reveals a SRV of $6(\pm1) \times 10^5$ cm/s for both monocrystalline wafers. Hence, the difference observed in IQE or in power conversion efficiency of monocrystalline wafers is accounted for only by the difference in their substrate resistivity. Such a good agreement between calculated and experimental data allows identifying SRV as the limiting parameter for solar cells efficiency based on monocrystalline substrates. Figure 2 (right) shows the model calculations of power conversion efficiency as a function of SRV. The starting point of this calculation was the experimental data of 16.4% efficiency cell. It is clear from the figure that an order of magnitude lower SRV would raise the efficiency above 17.5%. Work is currently under way to improve the passivation of phosphorus FSF of the Al back junction cell concept.

The bulk lifetime must be taken into account, however, when we analyze the current-voltage data of the multicrystalline wafers. The IQE fit of multicrystalline cell reveals the same SRV value as that obtained for monocrystalline cells, but with a considerable lower bulk lifetime of only 28 μs (as obtained from PC1D fit). It has been shown that the ratio of diffusion length and substrate thickness (L_d/d) must be higher than 2.5 to insure that the cell performance is not limited by the wafer quality [5]. Thus, to meet these conditions, the effective lifetime of the multicrystalline substrates must be higher than 130 μs. Hence, besides resistivity, the bulk lifetime is another important factor that limits the efficiency of n-type multicrystalline silicon solar cells with a rear side emitter.

Material	Resistivity [Ωcm]	Jsc [mA/cm^2]	Voc [mV]	FF [%]	η [%]
mc-Si	0.8	19.77	589	73.7	8.58
FZ	3.8	30.74	620	77.9	14.86
FZ	30	34.18	621	77.4	16.41

Table 1. Parameters of the best solar cells on n-type FZ and mc-Si substrates.

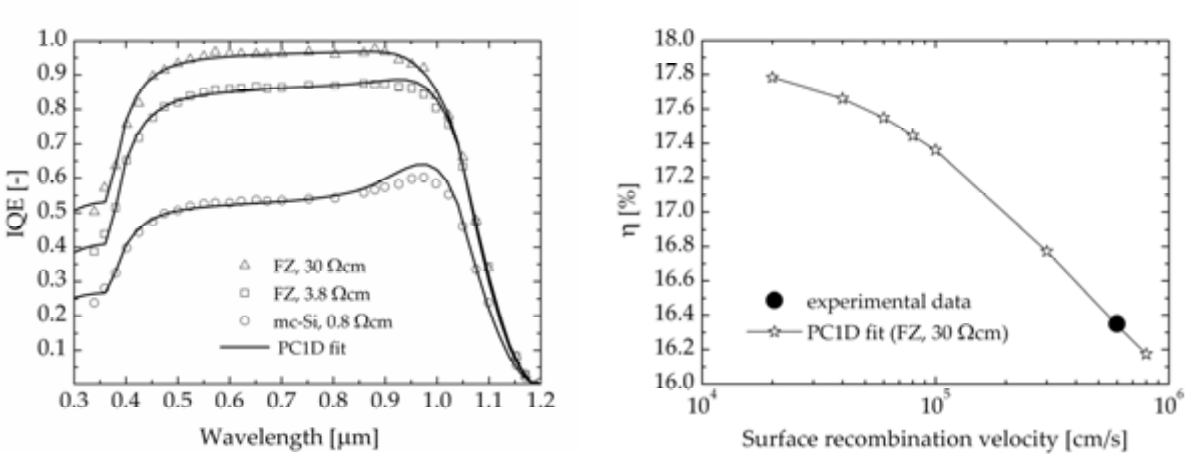

Figure 2. (left) Internal quantum efficiency (IQE) data of the solar cells from Table 1 (symbols) and its PC1D fit (lines), taking into account the measured front doping profile, surface reflection, wafer resistivity, and wafer thickness. The relevant fit parameters for the modeling are the bulk lifetime and front surface recombination velocity. (right) Calculated solar cell efficiency as a function of surface recombination velocity for an n-type FZ with a resistivity of 30 Ωcm. The parameters used in the calculation are those found by fitting the experimental data of Figure 2 (left). The increase in cell efficiency, due to an increase in J_{sc} and V_{oc}, is a result of a better front surface passivation.

It has been proven that a longer lifetime is obtained by increasing the wafer resistivity for multicrystalline substrates [9]; therefore, it would be important to know what could be the optimum resistivity to obtain the needed lifetime.

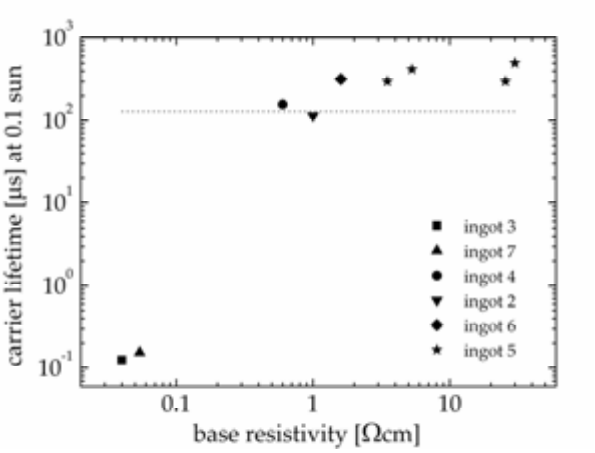

Figure 3. Effective minority carrier lifetime (symbols) as a function of base resistivity for various experimental n-type mc-Si ingots doped with As, Sb, or P (from their central parts). The effective lifetimes are measured using generalized Sinton QSSPC at an illumination level corresponding to 0.1 sun. The dotted line indicates the minimum lifetime required in order to guaranty that the cell performance is not limited by the wafer quality.

Figure 3 summarizes the effective minority carrier lifetime of various n-type multicrystalline ingots, measured using Sinton QSSPC at an illumination level corresponding to 0.1 sun. This illumination level approximately corresponds to the carrier density at the maximum power point of a cell. A sharp enhancement in lifetime, to values above 100 μs, is observed for wafer resistivity between 0.1 and 0.7 Ωcm. This is apparently in contradiction with the lifetime of 28 μs determined from the IQE of Figure 2 for the same base resistivity. However, the mc-Si wafer and cell suffer from spatially inhomogeneous lifetime distribution. Since the QSSPC method gives a locally averaged value for lifetime, the IQE lifetime, obtained by illuminating the entire cell, is the most realistic value. This is further supported by the light beam induced current (LBIC) scan of the mc-Si cell which shows a large variation in current density values on the whole cell, as is shown in Figure 4 (left). Partially

such an inhomogeneity was found to arise from a resistivity variation across the wafer, as shown by the resistivity scan of Figure 4 (right). We conclude that the lifetime inhomogeneity makes a significant difference in the solar cell performance [10]. Indeed, with higher resistivity and very homogeneous n-type mc-Si wafers, Kopecek et al. obtained cell efficiencies of 14.4% [4], and Cuevas et al. on small size 15.0% [6].

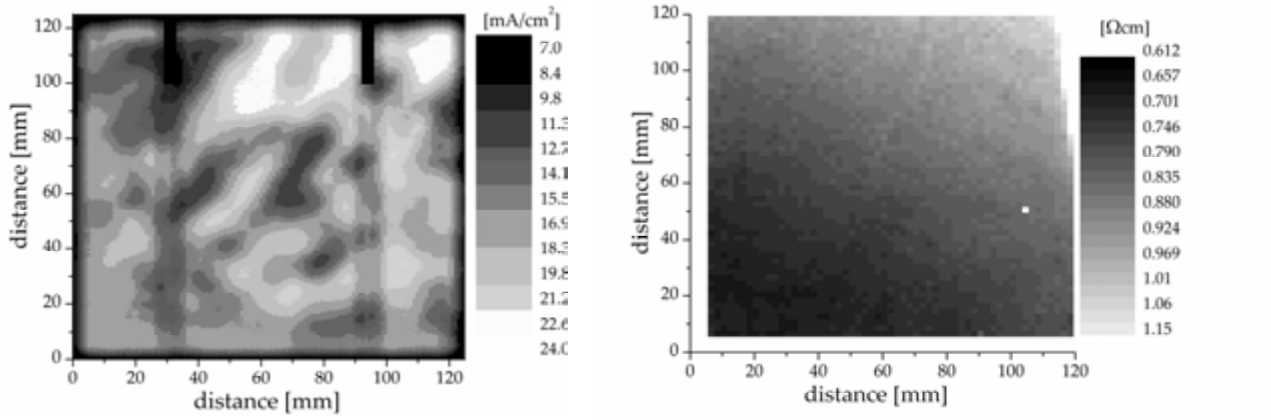

Figure 4. LBIC scan map (left) and bulk resistivity scan map (right) of the mc-Si of Table 1 (from the edge of the ingot). The resistivity scan was performed on an as-cut neighboring wafer.

Conclusion

We have demonstrated that a low cost process of fabricating n-type solar cells based on Al back junction concept leads to efficiencies up to 16.4% for monocrystalline substrates. Moreover, by improving the front surface passivation, efficiencies in excess of 17.5% could be realized, as demonstrated by our model calculations. High efficiencies may also be conceivable on n-type multicrystalline substrates after material optimizations, such as higher resistivity and increased lifetime homogeneity.

Acknowledgments

The authors would like to thank Radovan Kopecek and Thomas Buck for cooperation and stimulating discussions, and Ingo Röver and Karsten Wambach for cooperation and providing mc-Si wafers. This work was supported by SenterNovem as project no. 2020-04-11-11-001. The investigated mc-Si ingots were produced in the EC NESSI project, contract ENK6-CT-2002-00660, and the lifetime measurements of Fig. 3 were performed in the NESSI as well as the EC FOXY project, contract 019811(SES6). The content of this paper is the responsibility of the authors.

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Influence of Surface Roughness on the Accuracy of Dislocation Density Mapping by PVSCAN

Thurston Melson, Przemyslaw Rupnowski, and Bhushan Sopori
National Renewable Energy Laboratory
1617 Cole Blvd, Golden, CO 80401

ABSTRACT

Errors introduced by the surface roughness of commercial Si wafers, particularly ribbons, on the dislocation mapping are discussed. It is found that the error caused by the surface morphology of commercial ribbon-type wafers is only about ±10%. An important consequence is that ribbon samples can be mapped for dislocation distribution without a need for polishing.

INTRODUCTION

Dislocation mapping is an important tool for determining the quality of silicon wafers. Dislocation mapping has been greatly simplified by a new tool called PVSCAN, which rapidly measures dislocation distribution in a wafer. Typically, the sample is polished by CMP, then defect etched using the Sopori etch, and finally scanned under PVSCAN, which uses optical scattering from the etch pits to statistically count the dislocations. If the wafer is single crystal, CMP can be done quite easily. CMP can be somewhat tedious if the wafer is multicrystalline. Although we have developed procedures for damage-free polishing and minimizing grain-to-grain height variations, it is difficult to polish ribbon samples. Ribbon silicon samples typically have large thickness variations, and the material has greater hardness due to high concentrations of carbon. Therefore, it would be desirable to perform dislocation mapping of these wafers without the need for polishing. Because these wafers also have large surface roughness caused by growth striations and ridges of thickness variations caused by grain boundary solidification, it is not known how the surface morphology of such ribbon-based wafers will influence the accuracy of dislocation mapping by PVSCAN. We have carried out a detailed analysis to examine the effect of the surface morphology of as-grown ribbon samples on the accuracy of the dislocation measurements by PVSCAN. This paper presents the results of the study. We discuss experimental results and relate them to the theory of measurement by the PVSCAN.

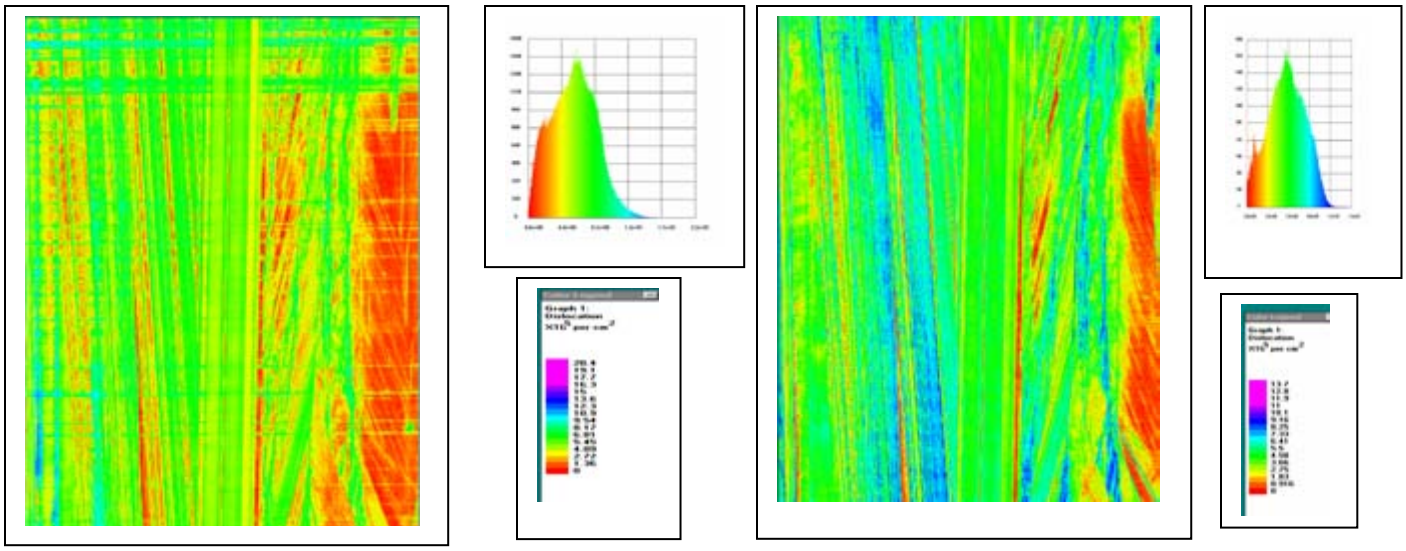
EXPERIMNTAL DETAILS

To determine the influence of surface roughness of the ribbons, we performed a variety of investigations using two types of ribbon-based substrates—from Evergreen Solar and Schott Solar. We carried out experiments to determine the surface morphology of as-grown ribbons, changes in the morphology upon defect etching, and the effects of the surface morphologies on defect counting. The following experiments were performed:

1. As-grown samples were defect etched and mapped. These samples were then polished using damage-free CMP, defect etched, and mapped again. These results were expected to show the error caused by absence of polishing.
2. A set of samples was defect mapped without defect etching. The results from this group of samples are expected to help in understanding various scattering from as-grown surface profiles and the maximum possible error one can have.
3. Samples of group 2 were defect etched and remapped. These results were expected to reveal changes in the relevant surface morphology of the samples by the defect etching.
4. Surface morphology was studied using a surface profilometer (Dektak), SEM, and optical microscopy.

RESULTS

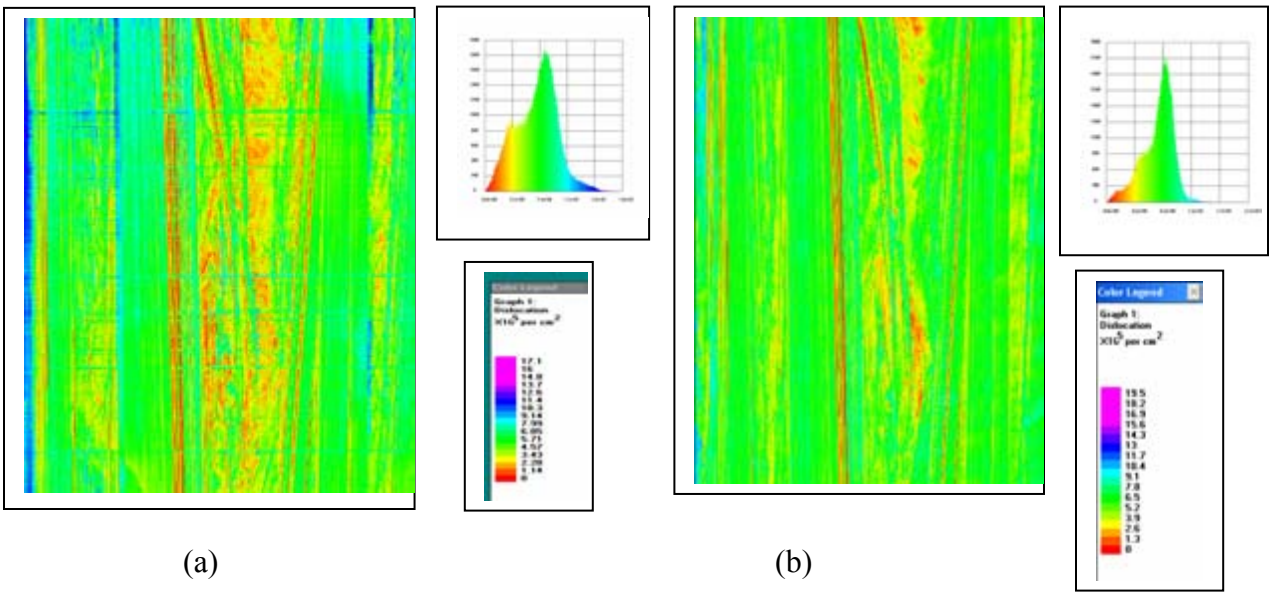
Figure 1 shows a typical example of dislocation maps of Evergreen Solar samples before and after polishing. The main difference between the unpolished and polished defect maps is absence of striations. The average dislocation density, $\langle N_d \rangle$ in cm^{-2}, obtained before and after polishing are 5.96 and 5.61 cm^{-2}, respectively. Also shown in Fig. 1 are color legends and dislocation distributions.



(a) (b)

Figure 1. (a) Defect map before polishing, Nd =5.96 x 10^5 cm^{-2}, and (b) after polishing Nd = 5.61 x 10^5 cm^{-2}.

Figure 2 is an example where the average defect density shows an increase upon polishing, from a value of 6.92 to 7.95 x 10^5 cm^{-2} . For all other cases, the changes in the defect density were in the range (see Table 1). The inference from these results clearly indicates that lack of polishing introduces error within ± 10%. This is very encouraging, but is quite counterintuitive.



(a) (b)

Figure 2. Defect maps (a) before polishing, $N_d = 6.92 \times 10^5$ cm^{-2} and (b) after polishing $N_d = 7.65 \times 10^5$ cm^{-2}.

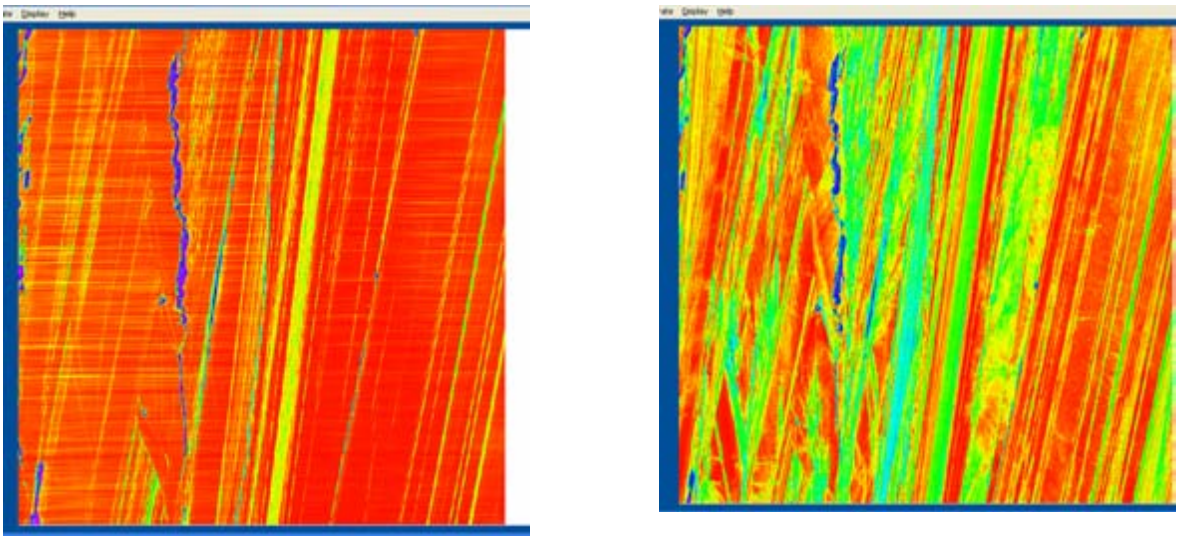


Figure 3. Sample 13 (2.9'' by 3.2'') (a) before etching, 1.85×10^5 cm^2, and (b) after etching 3.41×10^5 cm^{-2}.

Figure 3(a) shows a defect map of a ribbon sample without etching. It is seen that most of the ribbon appears to have zero effective dislocation density. This is desirable because the sample was not etched. However, there are regions of high dislocation density. Cumulatively, these regions contribute to an average dislocation density of 1.85×10^5 cm^{-2}. This value can be compared with dislocation density obtained after the same sample was defect etched and mapped. Figure 3(b) shows the defect map after etching. The average defect density was

3.41×10^5 cm^2. Similar values of <Nd> before and after etching were obtained for the whole set (see Table 2). From a comparison of the average dislocation density before and after etching, it would appear that there is an error of about 50%. This is not compatible with the results obtained before and after polishing. Clearly, etching leads to surface morphology in a way that PVSCAN does not (regard the scattering from such a surface as a signal caused by dislocations). Thus, it is important to examine the nature of surface roughness on the ribbons.

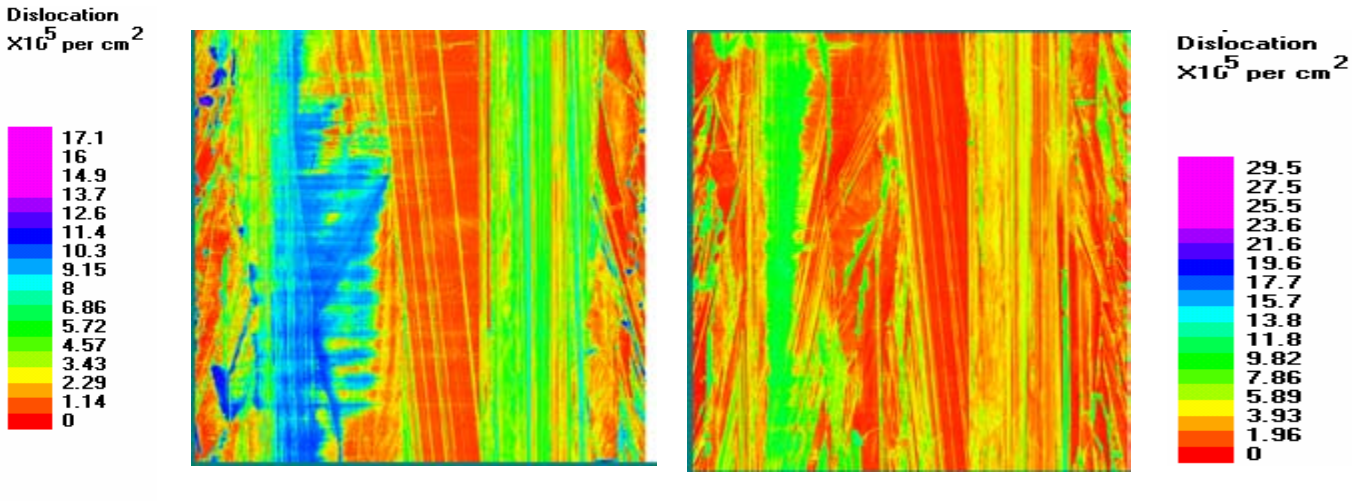


Figure 4. Ribbon (a) before polishing, Nd = $5.33\text{x}10^5$ cm^{-2}, and (b) after polishing Nd= $4.92\ \text{x}10^5$ cm^{-2}.

DISCUSSION

A similar study on unetched samples showed that as-grown surfaces have a large contribution toward defect counting. Figure 3 shows defect maps of an unetched sample before and after defect etching. This figure shows that the region that counts heavily as the dislocation contribution corresponds to the grain boundary ridge-like morphology. It is seen that the average dislocation density of the as-grown sample is $5.33\text{x}10^5$ cm^{-2}. Figure 3(b) shows the defect map after dislocation etching. The average value has increased to $3.42\ \text{x}\ 10^5$ cm^{-2}.

From the previous results, it may be concluded that defect etching provides two major contributions to the process of dislocation counting: (1) the contribution to the scattering from the dislocation etch pits, which increases upon defect etching, and (2) a decrease in the unwanted portion of the surface scattering that has a contribution toward dislocation counting.

NATURE OF ROUGHNESS OF RIBBON SURFACES

Ribbon surface has a morphology that is reminiscent of the crystal growth. In general we can categorize them into:

1. A fine-pitched, nearly periodic, grating-like structure, as seen in a micrograph of Fig. 5 a. Typical pitch of the structure is 7μm with an amplitude of ~ 1 μm This surface

perturbation appears to have a major effect on the dislocation signal. This structure is a result of surface relief in all ribbon technologies. Previous work has shown that this structure is related to the melt height and the growth speed. Our results show that this type of surface has a very pronounced effect on defect counting. It is, however, seen that Sopori etch actually smoothes this type of surface roughness. This effect can be seen clearly seen in Fig. 5. This figure shows optical micrographs of the same region of the sample before and after defect etching—it can be seen that the grating pattern is faded after etching. A similar quantitative result can be observed from Dektak traces (see next). Smoothing the grating-like pattern lowers the error in defect mapping.

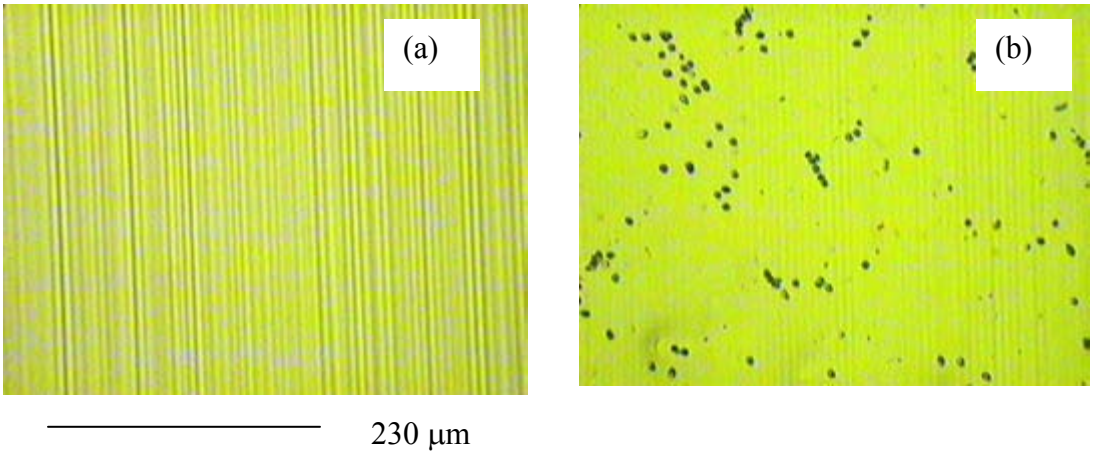
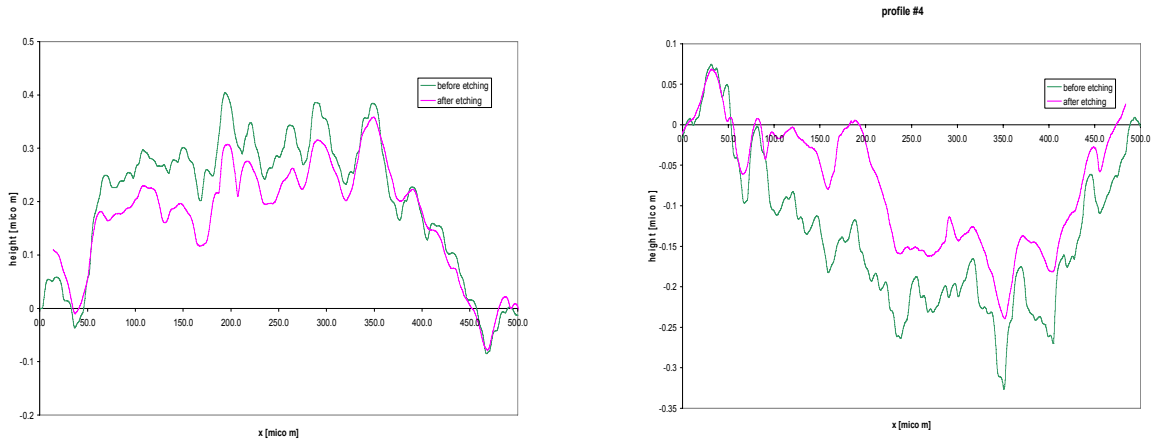


Figure 5. Optical micrographs of the grating-like pattern (a) before and (b) after defect etching. Defect etching smoothes the pattern.

2. Non-periodic striations with gentle slopes and rounded surfaces. Such a structure is believed to be caused by snapping of the melt and, in some cases, can be pseudoperiodic surface perturbation of large amplitude. Figures 6(a) and 6(b) show Detak traces of the surface profile of a ribbon in the same region before and after defect etching. By comparison, one can see that there is smoothing of the fine structure, whereas the large structure (of long spatial wavelength) does not change significantly. The effect of such surface morphology on the dislocation mapping can be also seen (in Figs. 1–3) as leading to an increase in the local defect density. However, this increase typically causes less than 10% error. Dektak data also exhibit changes in the surface morphology due to etchpits. In particular, the regions of high dislocation density can appear as troughs (see Fig. 6b)

2. A third type of surface structure often called a “ridge,” which appears at some grain boundary sites, in particular where several grains of different orientations meet. Figure 4a shows evidence of such a structure. The ridge formation is also accompanied by larger-scale surface geometry (generally a concave surface) that can have a significant effect on the defect imaging.



(a) (b)

Figure 6. Dektak traces from two samples taken (a) before and (b) after defect etching showing changes in the surface morphology.

Table 1. Average dislocation density measured for various samples before and after polishing.

Sample	<Nd> before polishing [10^5/cm^2]	<Nd> after polishing [10^5/cm^2]	Differ-ence [%]
1	5.96	5.61	6
2	6.92	7.65	-10
3	6.65	6.47	3
4	5.33	4.92	8

Table 2. Average dislocation density measured for various samples before and after defect etching.

Sample	<Nd> before etching [10^5/cm^2]	<Nd> after etching [10^5/cm^2]	Ratio of the two values
A	2.23	3.82	0.58
B	1.85	3.41	0.54
C	3.65	3.92	0.93
D	2.62	3.72	0.70
E	2.73	6.73	0.41

CONCLUSION

We have analyzed the effect of surface roughness on the error it can cause on defect counting by PVSCAN. Particular emphasis was placed on ribbon samples because they are difficult to polish. It is seen that ribbons have several types of roughness. The most important for defect mapping appears to be the higher spatial frequency, grating-like pattern. However, Sopori

etching causes a significant relief in this pattern. Consequently, we find that the error due to lack of polishing in the commercial ribbon samples is only about ± 10%.

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Cross-Sectioning a Finished Solar Cell for Detailed Characterization of Cell structure

Michael Speed, Manuel Romero, Bobby To, Helio Moutinho , Matt Page, and Bhushan Sopori

National Renewable Energy Laborites, Golden, Colorado 80401

ABSTRACT

An improved method for rapid, demountable, cross-sectioning of a large-area solar cell sample is described. The sample is encapsulated by wax in a chuck, which exposes the edge of the sample for CMP polishing. A controlled polishing scheme produces a flat, high-quality edge by a proper combination of pressure, slurry flow, and time. Major requirements for obtaining a high-quality edge for accurate characterization are described. This technique provides large-area cross-sections of a solar cell for evaluating various layers, and for study of such parameters as interface interactions, back-surface field, and EBIC.

INTRODUCTION

Development of solar cell fabrication processes requires detailed analyses of various interfaces as well as those of each of the layers. In most cases, this type of information is obtained on small-area samples, which are often fractured to observe various regions. We have developed a technique to cross-section large lengths of solar cells (or wafers at any step of the solar cell fabrication). This is a brief report of the technique and some results from different types of analytical methods.

CMP of a multi-layer, multicomponent sample is very difficult because each layer can have different polishing rate. The total polishing rate has mechanical and a chemical components. It is necessary to minimizing polishing rate variations by controlling mechanical and chemical polishing rates through pressure, slurry flow, time, and quality of the edge support.

METHOD

The various steps are illustrated below:

1. Samples are cut up to a length of 2 inches using a dicing saw

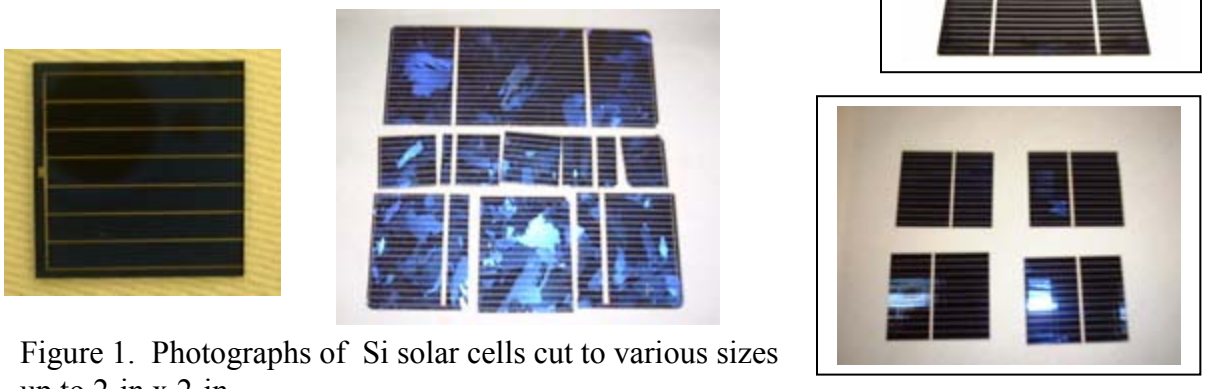


Figure 1. Photographs of Si solar cells cut to various sizes up to 2-in x 2-in.

2. The samples are mounted in a polishing chuck and polished on a semi-automatic polishing machine using Nalco slurry

a. Effect of meniscus formed on protruding sample

The wax forms a meniscus to properly support the sample, and prevent any round-off at the edges. Figure 2 illustrates meniscus formation, which results from melting wax and the capillary in which the sample is held.

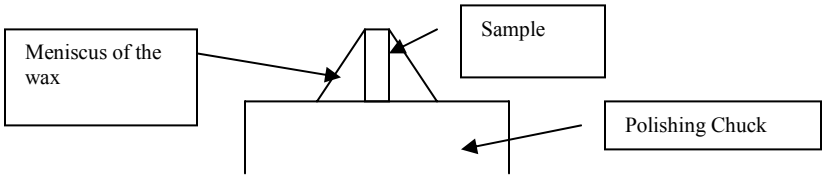


Figure 2. An illustration of sample protruding out of a polishing chuck, showing edge support provided by the meniscus formed by wax.

b. Effect of protruding length on polishing rate

The protruding length plays a key role in the quality of the finished cross-sectioned sample and as well controls the polishing rate. We mounted samples at different protruding length to determine the time required for polishing. Figure 3 shows that the polishing time is affected by the protruding length.

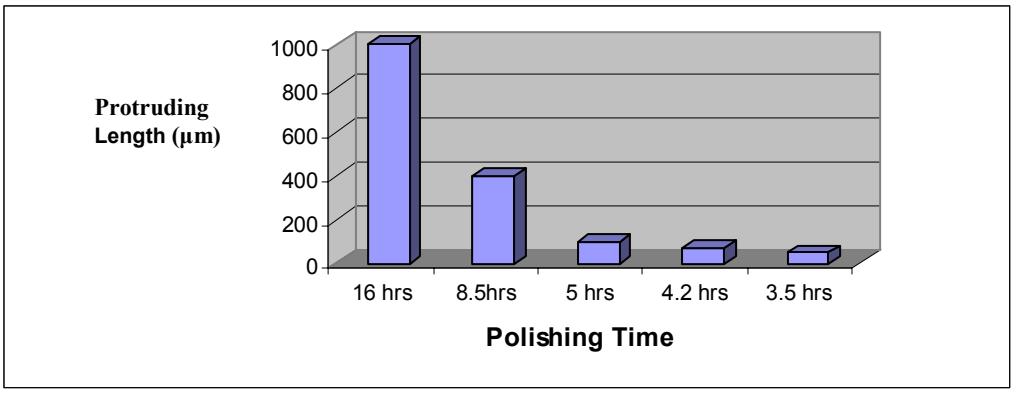


Figure 3. Polishing time as a function of protruding length.

Cross-sectioning large-area cells

Figure 4.

Photographs of sectioning chuck, sample mounting, and polishing

RESULTS/DISCUSSION

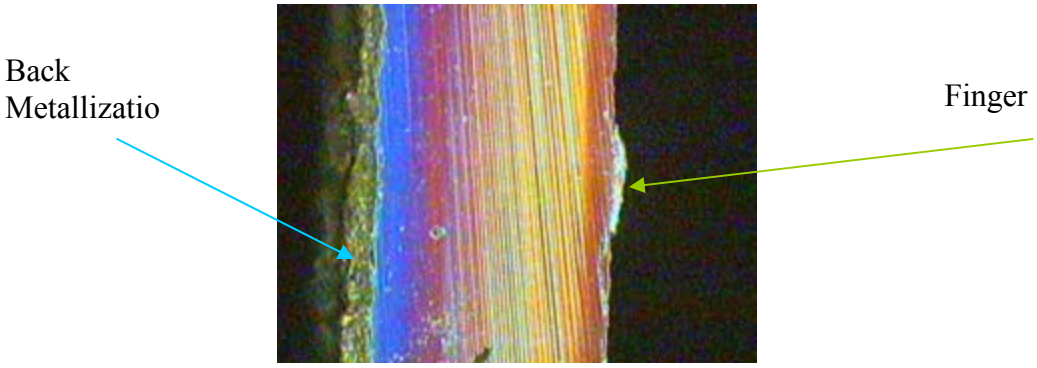


Figure 5. A photograph of a solar cell sample wax-encapsulated in the cross-sectioning chuck

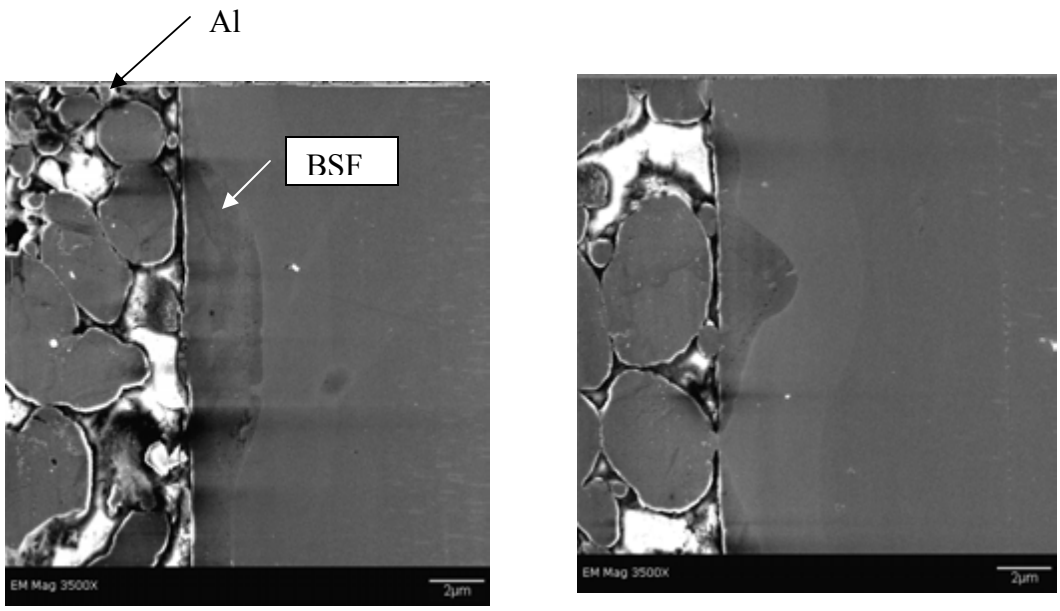


Fig. 6

Backside Al-alloyed, cross-sectioned cell showing large-grain Al, Si-Al alloyed, and the BSF regions.

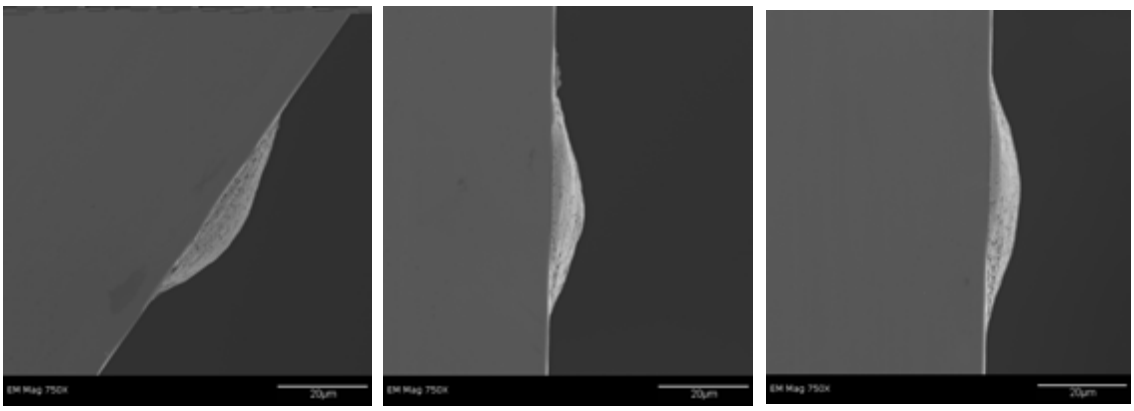
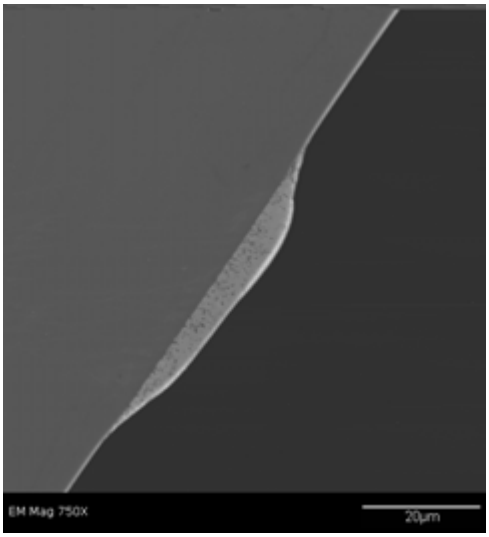


Fig. 7

SEM images of different grid lines on the same cross-sectioned cell



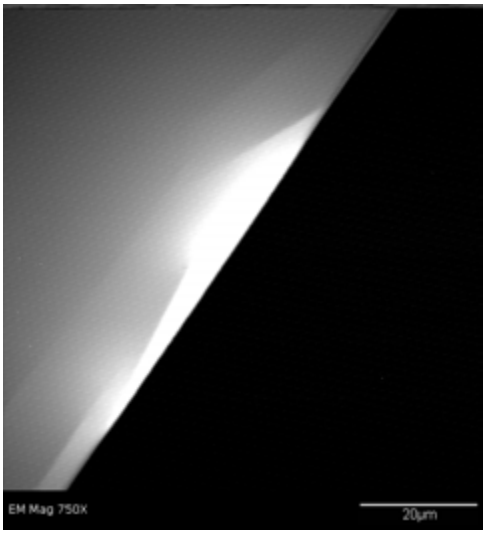


Fig.8

SEM (left) and EBIC (right) pictures of a Ag grid-line

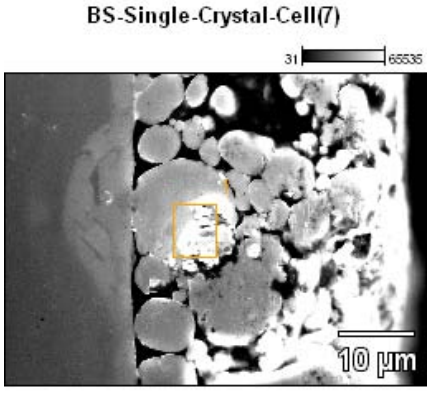
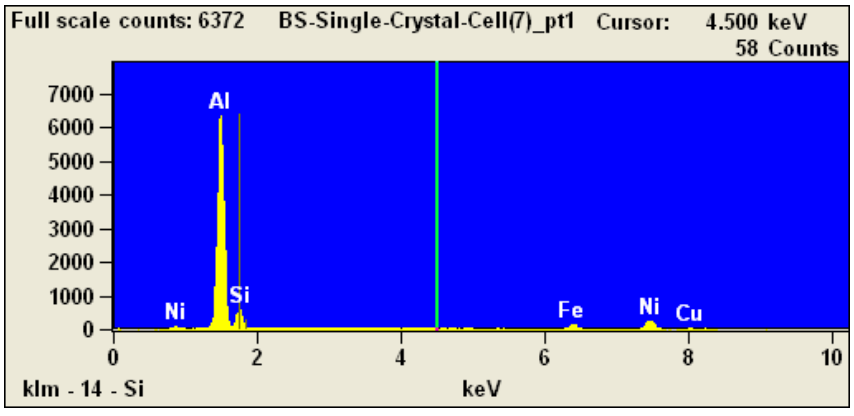


Fig. 9

Image Name: Sopori-Single-Crystal-Cell. **BACKSIDE ALUMINUM INTERFACE**

Accelerating Voltage: 15.0 kV

Magnification: 2000



REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ORGANIZATION.

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
August 2006	Conference Proceedings/Workshop	6-9 August 2006

4. TITLE AND SUBTITLE
16th Workshop on Crystalline Silicon Solar Cells & Modules: Materials and Processes; Extended Abstracts and Papers

5a. CONTRACT NUMBER
DE-AC36-99-GO10337

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
B.L. Sopori

5d. PROJECT NUMBER
NREL/BK-520-40423

5e. TASK NUMBER
WO97H299

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

8. PERFORMING ORGANIZATION REPORT NUMBER
NREL/BK-520-40423

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES

14. ABSTRACT *(Maximum 200 Words)*

The National Center for Photovoltaics sponsored the 16th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes held August 6-9, 2006 in Denver, Colorado. The workshop addressed the fundamental properties of PV-Si, new solar cell designs, and advanced solar cell processing techniques. It provided a forum for an informal exchange of technical and scientific information between international researchers in the photovoltaic and relevant non-photovoltaic fields. The Workshop Theme was: "Getting more (Watts) for Less ($i)". A combination of oral presentations by invited speakers, poster sessions, and discussion sessions reviewed recent advances in crystal growth, new cell structures, new processes and process characterization techniques, and cell fabrication approaches suitable for future manufacturing demands. The special sessions included: Feedstock Issues: Si Refining and Purification; Metal-impurity Engineering; Thin Film Si; and Diagnostic Techniques.

15. SUBJECT TERMS
photovoltaics; crystalline silicon; solar cells; module; materials and processes; manufacturing; new cell structures; cell fabrication; process characterization techniques; thin films;

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPHONE NUMBER (*Include area code*)
Unclassified	Unclassified	Unclassified	UL		

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18