March 2005 • NREL/SR-520-37738

Subcontractor Report

Large-Scale PV Module Manufacturing Using Ultra-Thin Polycrystalline Silicon Solar Cells

Annual Subcontract Report
1 October 2003–30 September 2004

J. Wohlgemuth and M. Narayanan
BP Solar
Frederick, Maryland

National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

Operated for the U.S. Department of Energy
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NREL Technical Monitor: Richard Mitchell

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PREFACE

This Annual Technical Progress Report covers the work performed by BP Solar for the period October 1, 2003 to September 30, 2004 under DOE/NREL Subcontract # ZDO-2-30628-03 entitled "Large-Scale PV Module Manufacturing Using Ultra thin Silicon Solar Cells". This is the second Annual Technical Report for this subcontract. The subcontract is scheduled to run from April 1, 2002 to November 30, 2005.

The following personnel at BP Solar have contributed to the technical efforts covered in this report.

Dinesh Amin
Roger Clark
Danny Cunningham
Bonnie Kinsey
Mohan Narayanan
Jean Posbic
Paul Schneider
John Wohlgemuth
Jay Miller
Fiore Artigliere
Joseph Creager
George Kelly
Timothy Koval
Andy Nguyen
William Poulin
Jay Shaner
Murray Bennett

BP Solar has been supported by subcontracts at the Automation and Robotics Research Institute at the University of Texas at Arlington (ARRI), the Physics Department at North Carolina State University (NCSU) and the Nanomaterials and Nanomanufacturing Research Center at the University of South Florida (USF).

ARRI staff that worked on the subcontract included:

Heather Beardsley
Raul Fernandez

NCSU work on the subcontract was performed under the direction of Professor Gerald Lucovsky.

USF work on the subcontract was performed under the direction of Dr. Sergei Ostapenko.

EXECUTIVE SUMMARY

The major objectives of this program are to continue the advancement of BP Solar polycrystalline silicon manufacturing technology. The Program includes work in the following areas.

- Efforts in the casting area to increase ingot size, improve ingot material quality, and improve handling of silicon feedstock as it is loaded into the casting stations.
- Developing wire saws to slice 100 μm thick silicon wafers on 290 μm centers.
- Developing equipment for demounting and subsequent handling of very thin silicon wafers.
- Developing cell processes using 100 μm thick silicon wafers that produce encapsulated cells with efficiencies of at least 15.4% at an overall yield exceeding 95%.
- Expanding existing in-line manufacturing data reporting systems to provide active process control.
- Establishing a 50 MW (annual nominal capacity) green-field Mega-plant factory model template based on this new thin polycrystalline silicon technology.
- Facilitating an increase in the silicon feedstock industry's production capacity for lower-cost solar grade silicon feedstock.

ACCOMPLISHMENTS

During the second year of the program there were significant accomplishments in each of the task areas.

- Formed a strategic partnership and demonstrated good yields and cell efficiencies using a mix of 25% solar grade silicon with 75% intrinsic silicon feedstock.
- Demonstrated casting of ingots > 300 kg.
- Modified the casting stations to reduce turn around time and maintenance requirements.
- Demonstrated the slicing of 110 μm thick silicon wafers.
- Demonstrated the use of thinner wire (140 μm versus 160 μm)
- Improved the glue used to mount the bricks for wafering.
- Demonstrated that the ARRI demounting prototype worked and identified a number of problems associated with handling ultra-thin wafers.
- Identified 2 vendors of wafer demounting equipment.
- Identified areas in the factory that must be modified for producing ultra-thin cells.
- Ran 225 μm wafers though the production line.
- Identified the process development necessary to implement iso-chemical texturing.
- Optimized the SiN process introduced during the first year of the program.
- Demonstrated potential efficiency gains using a selective emitter.
- Evaluated and qualified hot melt front paste as an alternative for standard screen print paste.
- Processed ultra-thin wafers through the cell line, evaluating several different process sequences.
- Implemented laminated-in protective bypass diodes in a number of commercial products.
- Demonstrated a 2.5 to 3% increase in output power using AR coated glass and qualified the glass through environmental testing.
- Demonstrated tabbing, stringing and lamination with ultra-thin solar cells.

- Utilized Scanning Acoustical Microscopy to observe cracks and micro-cracks in wafers, cells and partially processed cells.
- Implemented inline measurement of brick dimensions and of dark I-V for determining diode performance.

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1.0 INTRODUCTION

The goal of BP Solar's Crystalline PV Manufacturing R&D Project is to improve the Polycrystalline Silicon manufacturing facility, to reduce cost, improve efficiency and increase production capacity. Key components of the program are:

- Increasing ingot size;
- Improving ingot material quality;
- Improving material handling;
- Developing wire saws to slice 100 μm thick silicon wafers on 290 μm centers;
- Developing equipment for demounting and subsequent handling of ultra-thin silicon wafers;
- Developing cell processes using 100 μm thick silicon wafers that produce encapsulated cells with efficiencies of at least 15.4% at an overall yield exceeding 95%;
- Expanding existing in-line manufacturing data reporting systems to provide active process control;
- Establishing a 50 MW (annual nominal capacity) green-field MegaPlant factory model template based on this new thin polycrystalline silicon technology; and
- Facilitating an increase in the silicon feedstock industry's production capacity for lower-cost solar grade silicon feedstock

These goals are to be achieved while improving the already high reliability of today's crystalline silicon modules.

Three subcontractors are supporting BP Solar in this effort:

1. Automation and Robotics Research Institute (ARRI) of the University of Texas at Arlington to assist BP Solar in developing equipment for automated handling and demounting of ultra-thin wire saw wafers and assist in development of a model for the MegaPlant
2. North Carolina State University (NCSU) to support BP Solar in characterizing the effect of trapped charge at the silicon/anti-reflective (AR) coating interface and in determining how to improve the passivation of BP Solar cast polycrystalline silicon solar cells.
3. The Nanomaterials and Nanomanufacturing Research Center at the University of South Florida (USF) to develop a non-contact method for detecting cracks and micro-cracks in wafers, cells and partially processed cells.

The baseline for this PV Manufacturing R&D program is the polycrystalline process and production line as it existed at the conclusion of BP Solar's previous PVMaT Contract NREL # ZAX-8-17647-05 entitled "PVMAT Improvements in the BP Solar PV Module Manufacturing Technology". [1, 2] This baseline is described in more detail in Section 2.0.

The rationale behind this program was to identify specific areas in the baseline process where improvements in handling, process control or the process itself could significantly reduce cost, increase efficiency and/or improve capacity. The realization that feedstock silicon is becoming an increasing larger percentage of the overall cost lead to the incorporation of efforts to significantly reduce wafer thickness and to work with selected silicon feedstock manufacturers to secure a source of solar specific lower-cost solar-grade silicon feedstock.

BP Solar has identified two external vendors, who have provided large capacity casting stations for the expansion of the BP Solar Frederick casting facility. Material quality from these stations was shown to be equivalent to that made in the BP Solar baseline stations. Efforts during this program include increasing the ingot size and improving the material quality.

The development in the wire saw technology is to reduce wafer thickness in order to reduce cost and increase even further the number of wafers/cm of brick that can be cut, thereby reducing the amount of silicon necessary per watt of modules produced.

Work on cell processing is designed to increase the average cell efficiency to 15.4% (at Standard Test Conditions) for ultra-thin wafers while improving process control and reducing the overall module manufacturing cost. Areas of investigation include passivated AR coating, edge isolation, surface texturing, and selective emitter diffusion. In addition, those processes that are not compatible with processing of ultra-thin cells will be identified and modified.

Wafer and cell handling will become more critical as the thickness decreasing. ARRI is assisting BP Solar in identifying approaches to handling of ultra-thin wafers throughout the production line.

Improved measurement and control during processing should lead to improved yields and higher average cell efficiency. Three specific areas in the plant have been identified, where additional inline measurements are expected to significantly improve control of the process.

The second year's efforts will be discussed in detail in Section 3.0.

2.0 BASELINE PROCESS

BP Solar's Crystalline Silicon Technology is based on use of cast polycrystalline silicon wafers. The process flow at the end of NREL Contract # ZAX-8-17647-05 is shown in Table 1.

Table 1
Cast Polycrystalline Silicon Process Sequence

Casting
Of
240 Kg Brick Ingots

Wire Saw Wafering
270 μm thickness

Cell Process
All Print with Aluminum Back Surface Field (BSF)
&
Plasma Enhanced Chemical Vapor Deposition (PECVD) Silicon Nitride (SiN) AR

Module Assembly
Hot Bar Soldering for Tabbing and Stringing

Lamination
Fast Cure Ethylene Vinyl Acetate (EVA)

Finishing

The various segments of BP Solar's module manufacturing process as practiced at the beginning of this PV Manufacturing R&D program are described below.

Casting
BP Solar has purchased directional solidification equipment specifically designed for photovoltaics. In this process, silicon feedstock is melted in a ceramic crucible and solidified into a large grained semi-crystalline silicon ingot. The size of the cast ingot yields 25 – 12.5 cm by 12.5 cm bricks.

Wafering
During the previous PVMaT Programs BP Solar developed wire saw technology for cutting large area polycrystalline wafers and improved the performance by reducing the wire saw pitch to 450 microns with no loss in downstream yield, by separating and recycling the components of the wire saw cutting slurry, and by re-tooling older saws to increase their capacity by 40%.

Cell Process
The cell process sequence is based on the use of Thick Film Paste (TFP) metallization, where a commercially available screen-printed silver paste is applied as the current carrying grid on the front of the solar cell. This process has been designed to be as cost effective as possible. The high temperature process steps include: diffusion, firing of the front and back print pastes and PECVD deposition of a SiN antireflective (AR) coating.

During the previous PVMaT Program, BP Solar developed the cost effective PECVD SiN process. This process has now been implemented on all BP Solar screen print production lines.

Module Assembly

The first part of the module assembly sequence is to solder two solder plated copper tabs onto the front of the solar cells. BP Solar uses automated hot bar soldering machines to perform the tabbing operation. Tabbed cells are then soldered into strings using hot bar soldering equipment developed in the previous PVMaT program.

Module Lamination

The module construction consists of a low iron, tempered glass superstrate, EVA encapsulant and a Tedlar back sheet. The lamination process, including the cure, is performed in a vacuum lamination system. Then the modules are trimmed and the leads are attached. Finally, every module is flash tested to determine its STC power output.

3.0 PROGRAM EFFORTS

The following sections detail the progress made in each task during the second year of the program.

3.1 Silicon Feedstock Development

In this task, BP Solar is working with a strategic partner to develop a solar-specific lower-cost solar-grade silicon feedstock.

In the first experiment a small amount (~ 38 kg) of experimental solar grade material was produced by our strategic partner. The material was type tested and resistivity checked, giving 0.33-0.37 ohm-cm, p-type. The material was then processed through our standard silicon preparation and cleaning line. Prior to casting, a 38 kg reference ingot was grown in the test casting station using known good quality intrinsic feedstock doped to our standard resistivity range (1 to 2 ohm-cm) with boron dopant alloy. The test casting station was cleaned and turned around, and the 38 kg of solar grade (SoG) silicon was loaded into the station. All casting parameters were maintained from the intrinsic reference.

Both the reference ingot and the SoG ingot were then processed back to back through all the same equipment sets, sizing, wafering, surface etch, diffusion, SiN, and metallization. Cell test results are shown in Table 2 for a 1 in 6 sample set throughout the height of the ingot:

Table 2
Cell results for First Solar Grade Si Experiment

	Solar grade Si	Intrinsic Si
# of cells	55	52
Bulk resistivity (ohm-cm)	0.27-0.370	1.0-1.8
Efficiency (%)	11.5	14.6
Isc (A)	4.45	4.90
Voc (V)	603	607

The results reflect the lower base resistivity of the wafers, (0.27-0.30 ohm-cm for the SoG), and that there was no tuning or optimization on the cell line for this material.

In the second experiment a significantly larger amount (~ 100 kg) of experimental solar grade material was produced by our solar grade strategic partner. The material was pre-doped so that a 65% mix with intrinsic silicon would produce our targeted base resistivity range for further cell processing. A 38 kg total weight ingot was produced using a 65% mix. Immediately following this a 25% mix, 38 kg ingot (with the balance being intrinsic and dopant) was produced. Cells were made on both sets with the results given in Table 3. In all three cases the amount of silicon used to make cells was identical.

Table 3
Cell results for the Second Solar Grade Si Experiment

Silicon	Average Cell Efficiency (%)
Intrinsic	14.94
65% SoG	14.53
25% SoG	14.94

Based on these results, the decision was made to continue development of the material and move to larger tests of the 25% mix in the 240 kg ingot casting size.

In the third experiment, 60kg of experimental feedstock material were added to 180kg of intrinsic silicon along with dopant and cast in a Type A casting station. Initial test wafers by height in the ingot produced results that were comparable to the running line averages for standard material as indicated in Figure 1. Two test lots are circled in red and represent ~40 wafer lots surrounded by ~1100 wafer production lots in time sequence through testing.

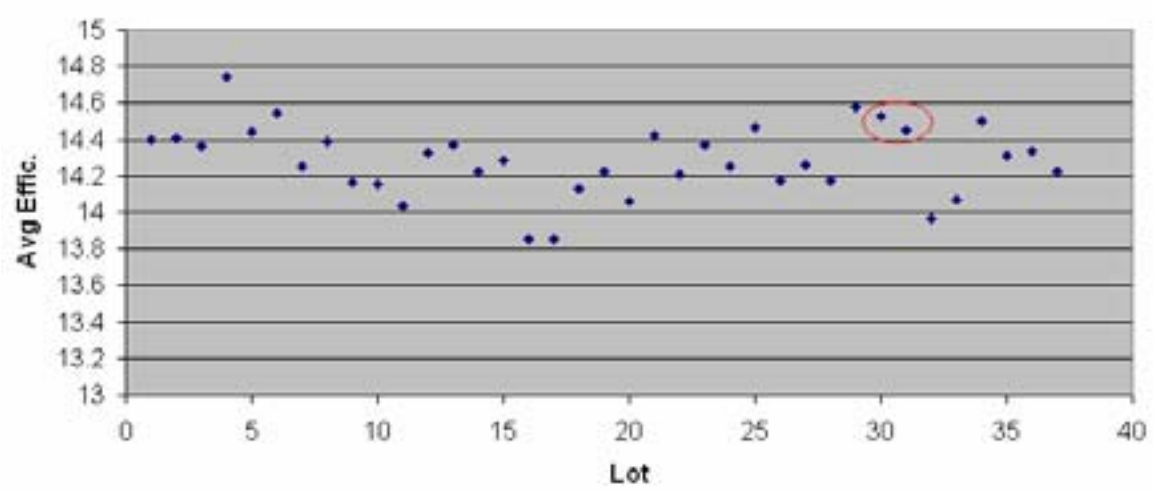


Figure 1: Lot Average Cell Efficiency for Standard and Test Silicon

Additional tests with the balance of this material produced over 6300 tracked wafers (lots 56198w1 through 56203w1) that showed similar bin distributions to production lots. The cell distributions are given in Figure 2. The two bolded lots 56189w1 and 56195w1 were of similar average efficiency, 56171w1 and 56172w1 were 0.3% higher in absolute efficiency for comparison.

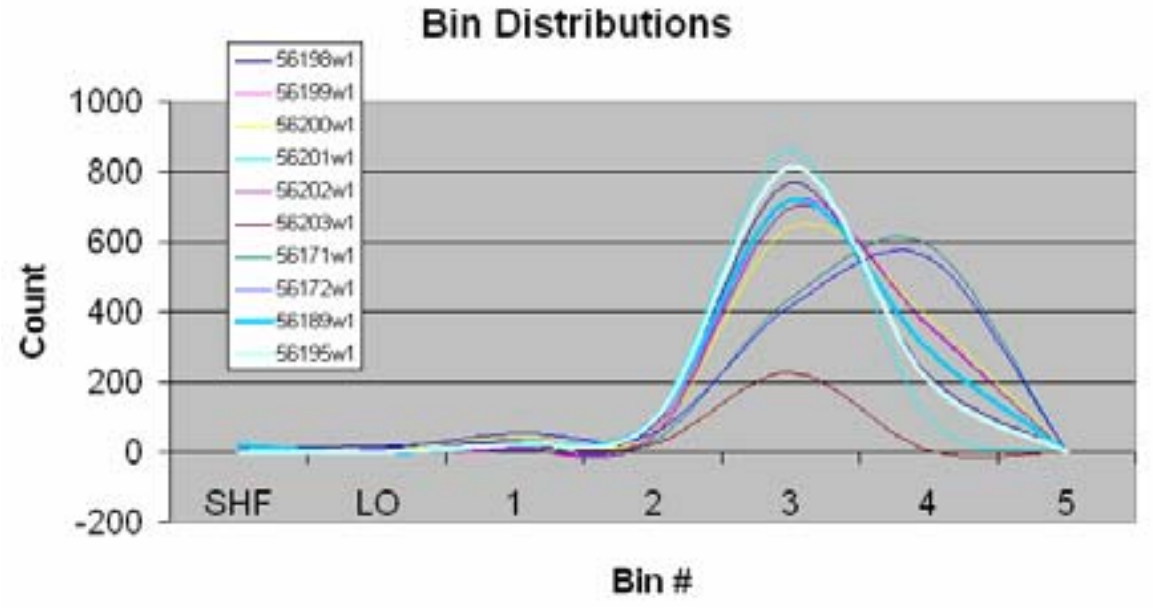


Figure 2: Cell Bin Distribution of Test Silicon Compared to Standard Silicon

With the success of this trial, we are planning a larger pilot demonstration.

3.2 Casting Development

In this task, BP Solar is investigating improvements in the casting process in order to increase ingot size, improve material quality and improve material handling.

3.2.1 Ingot Size Increase

BP Solar has designed and demonstrated a prototype casting station that can increase the cast ingot weight from the standard 240 kg to over 300 kg. The first extra large ingot was cast using 320 kg of Si feedstock. It resulted in an ingot with an average height of 28.8 cm as compared to the standard height of 21.9 cm. Figure 3 is a picture of a standard ingot and this taller ingot. From MW-PCD (microwave brick lifetime measurement), bricks showed 22-24cm of length with >2μs, our typical cut-off for useable silicon. Cell results from a single scribed outer brick show 24.1cm of panel grade cells and have peak efficiency across 20cm of the brick height. The graph of cell efficiency versus ingot position is shown in Figure 4.

Figure 3: Standard Ingot and Larger 320 kg Ingot

Casting of ingots larger than 240 kg has been demonstrated, 250 kg commonly, 265 kg in a trial set of 12 ingots, and two 320 kg ingots. However, there are several factors that limit complete production conversion to larger ingot size. A change of more than 10 kg from one size to the next necessitates a change in the release coating applied to the crucibles. Portions of the current tool set used to size the ingots into bricks also has a cut depth limitation, making complete conversion to larger ingot weights impossible without stranding capital assets. Currently a mix of 240 kg and 250 kg size are being used to optimize output. In the future, only tools capable of 250 kg+ sizes will be purchased. The manufacturer of Type A stations has also recommended a "do not exceed" weight of 280 kg, due to current mechanical design constraints on the internal and external drive components

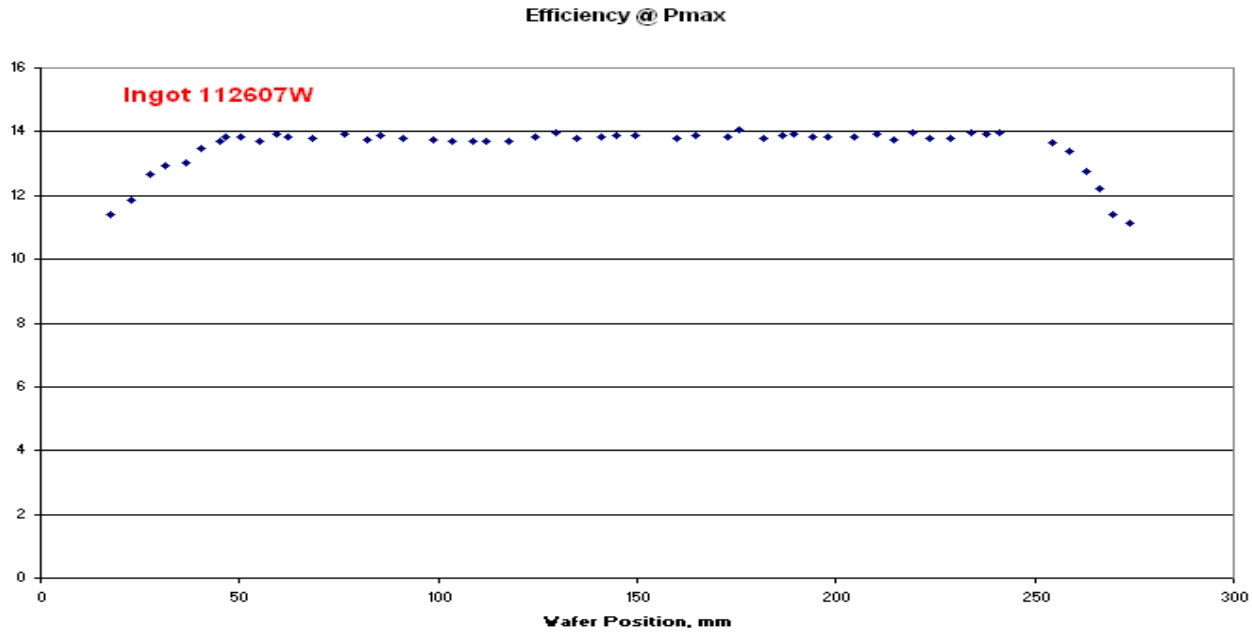


Figure 4: Cell Efficiency as a Function of Position in Large Ingot

3.2.2 Trace Gas Analysis

A Trace Gas Analyzer (TGA) was connected to a casting station during a casting run. A real-time chromatograph was recorded throughout the run, as well as concentration data (extracted from the chromatograph) every 858 seconds. A sample chromatograph is shown in Figure 5. The peaks from left to right are H_2, O_2, N_2, CH_4, CO, CO_2. This is the unscaled analog data from the TGA with successive 850 sec scans plotted front to back. Within the first two hours, peak clipping for N_2 and CO are visible.

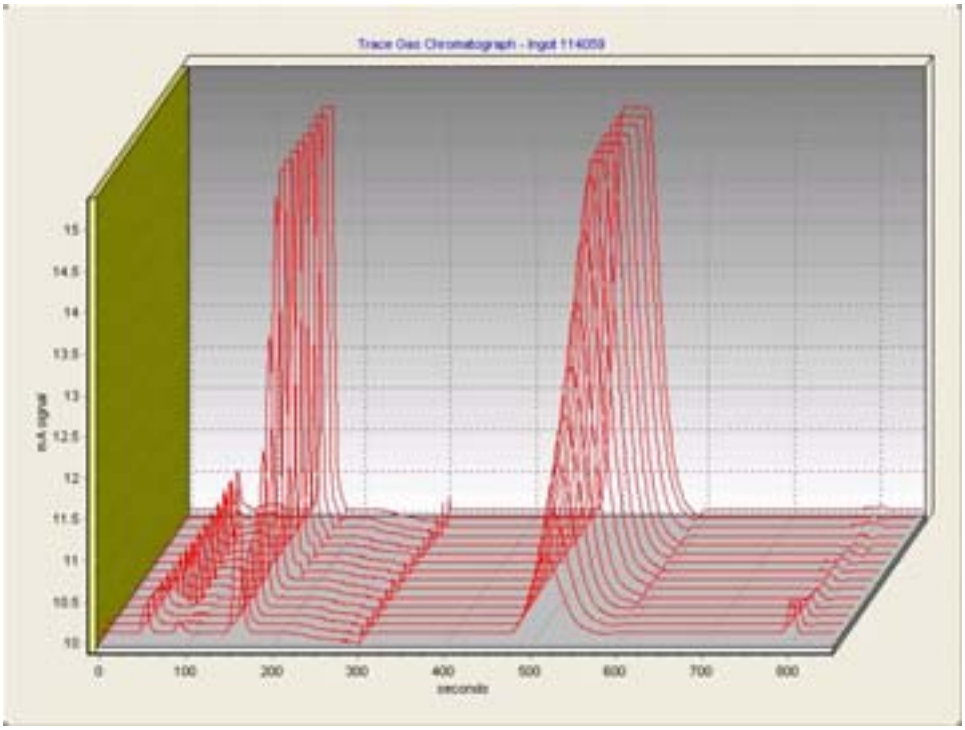


Figure 5: Chromatograph of Casting Run

The approximate concentration data throughout the run is plotted in Figure 6. These levels of contaminants are significant to the casting process and their concentration fluctuation timing can be correlated to relevant process conditions. The presence of hydrogen is not well understood.

With this data, we began to re-evaluate the results of some old experiments and looked to modify the physical set-up to look to reduce the level of contaminants circulating in the furnace and/or reduce the ingot's exposure to them.

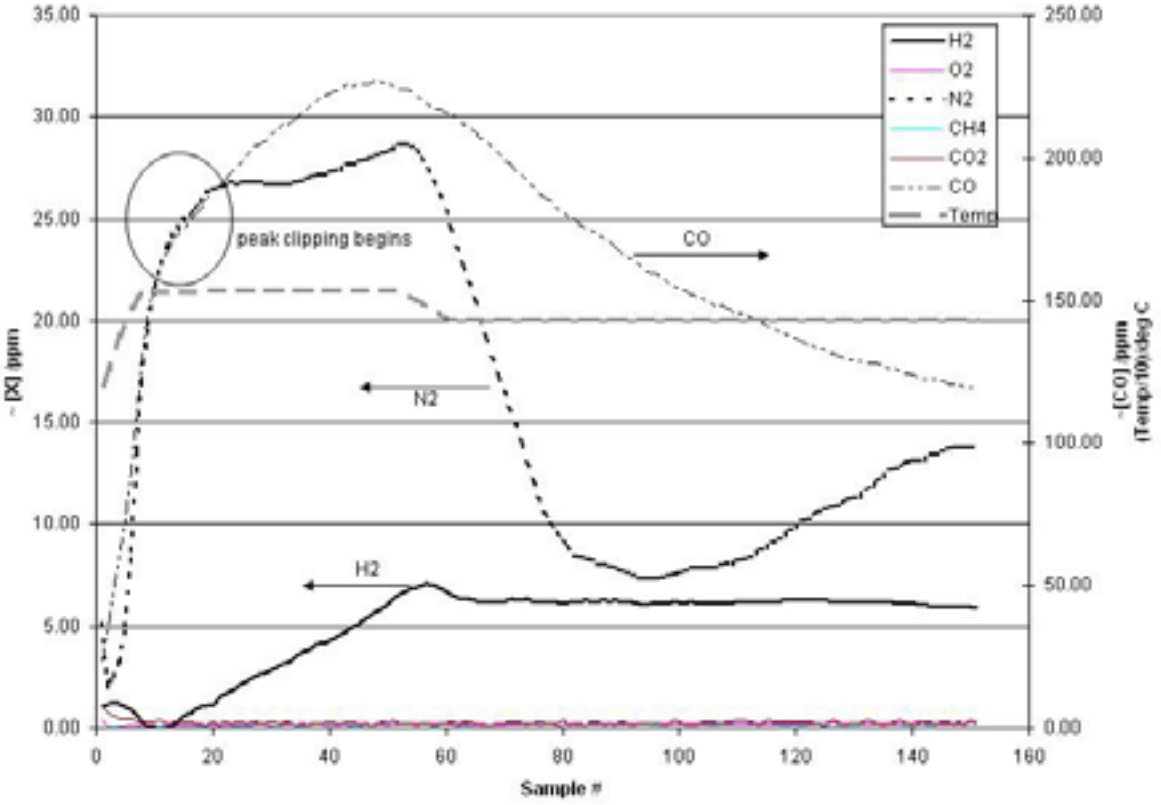


Figure 6: Concentration of Impurities during Casting Run

3.2.3 Equipment Improvements

During the program a number of improvements have been made in the construction of the casting chambers and of the supporting hardware inside. Specific improvements include:

- New ingot side plates were designed to eliminate a number of small fragile and expensive threaded connections with a mortise and tenon type construction. This reduced labor time and the number of parts that have to be stocked as well as reducing operator fatigue and increasing safety in handling.
- Redesign of the thermocouple feed-thru to reduce the number of fittings and add purge system to the vacuum seal.
- Design of a new crucible cover to improve gas flow around the ingot. The new crucible cover kept the top of the ingot clean and shiny as shown in Figure 7. Initial results indicate that the as cut brick lifetime was unaffected by the change.

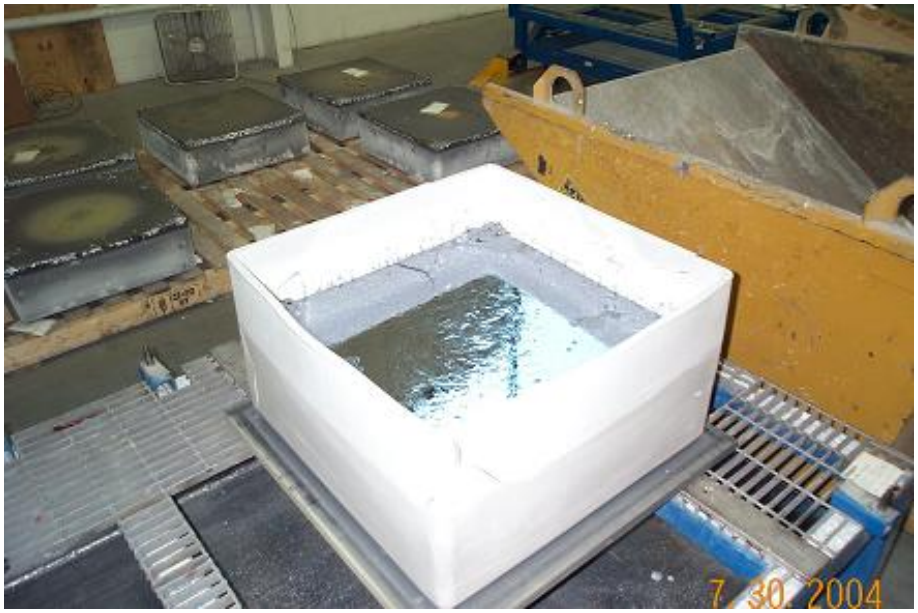


Figure 7: Clean, Shiny Ingot Surface from Experimental Cover

3.3 Thin Slicing of Silicon Wafers

In this task, BP Solar is developing a process to slice silicon wafers of 100 μm thickness on 200 μm centers.

During the first year of the program BP Solar was working with a vendor to develop a more durable slurry based on diamond grit. Diamond slurry is used in a number of industries as a cutting media. In the first experiments a standard slurry formulation was utilized. It was possible to cut the wafers, but the process was slow and the wafer surfaces were full of defects. Higher loads of diamond were evaluated, but did not improve the cut quality. It appears that while the slurry formulation is good for maintaining the diamond in suspension, it may not be optimum for transport on the wires into the cutting face. Work on diamond slurry has been terminated.

The wire saw effort using the standard silicon carbide slurry was much more successful. Wire saw guides were purchased which allowed us to cut wafers from 150 microns to 275 microns in a single wire saw run. We made two wire saw runs, obtaining about 500 wafers for each thickness. Wafers with thicknesses from 150 microns to 225 microns were then run through the cell line and in some cases the module assembly line, using standard operating procedures. These wafers are all thinner than our standard, which is 250 microns. These wafers were then used to identify handling problems in the remainder of the production line.

Wire guides were procured with grooves designed to cut 110 micron wafers using our standard 160 micron wire. For the test, a “conversion kit” was installed on the saw that included modified slurry nozzles and slurry deflectors. Thin wafer test slicing was completed in three runs on a 500 mm web and 300 mm wire guide in a production wire saw. Although the machines have the capability to do a maximum of about 180 cm of cutting length, the test runs were all lightly loaded to about 40 cm to simplify testing waferability at 110 microns. A full run of this thickness is also likely to present problems with motor loading and cooling load because of the increased cutting density (0.325 mm pitch versus 0.450 mm pitch).

Two runs of 12.5 cm wafers and a third of 15.7 cm wafers were completed. Cutting does not seems to be a large issue, but removal from the saw required that the web be cut off and pulled out prior to wafer extraction. The typical glue edge has insufficient strength at 110 micron width to securely hold the wafers and overcome the friction drag of web extraction, a problem that is exacerbated when the mounts are still warm from the cut. Figure 8 is a picture of one brick wafered at 110 microns with a centimeter ruler adjacent. Only near the beam are all wafers able to be seen, as the surface tension of the cleaning agents causes them to stick together.

Figure 8: Thin Wafer Comb as it came off of the Wire Saw

Once out of the saw, the mounts required some special attention to handling, but particularly in demounting and cassetting where breakage rates were high if standard handling techniques were used. These wafers are now being utilized for experiments in handling, as well as to develop optimized cell processes for ultra-thin wafers.

The amount of silicon used per wafer and therefore per kilowatt of PV produced can be reduced by using thinner wafers and by cutting with thinner wire. The first attempt at cutting with thinner wire utilized 140 micron wire instead of the standard 160 micron. The wire guides previous mentioned that allow us to cut wafers on 305 microns centers were utilized, resulting in wafers that are approximately 125 microns in thickness. This run was performed using standard production conditions except for reduced loading. The wire cut very well with no apparent problems related to wire thickness.

3.4 Wafer Demounting and Handling

In this task, BP Solar is developing processes and equipment for demounting and subsequent handling of very thin silicon wafers.

3.4.1 Wafer Demounting

BP Solar is developing processes and equipment for demounting of ultra-thin silicon wafers. This task is expected to result in integration of processes and equipment on the BP Solar production line for processing ultra-thin silicon wafers. In the present process sawn wafers, ~250 micrometers in thickness, still glued to the wire saw beam, are unloaded from the wire saw and soaked in solvent to remove the oil and slurry. Then, wafers, (still on the wire saw beam) are soaked in warm water to soften the epoxy bond. The operator then removes wafers from the beam by hand and loads them into cassettes. The wafers (in cassettes) are cleaned in a caustic based detergent solution and rinsed with DI water. Any remnants of glue stuck on the edges of the wafers get removed during the cleaning. The partial removal of the glue usually does not affect thicker wafers. However, mechanical removal of the glue can lead to the formation of micro-cracks in the wafers, which is not acceptable for ultra-thin wafer processing. Finally manual handling adds too much labor cost and when used on ultra-thin wafers will result in very high yield loss. Therefore an entirely new demounting and cleaning process and associated equipment are required.

The first step in development of a revised process is development of a glue compatible with ultra-thin wafers. In this task BP Solar evaluated a new glue (Blue Glue). Several bricks have been mounted using the Blue Glue. After the hot water soak the wafers separated from the glue as shown in Fig 9. (As opposed to the old glue which separated from the mounting plate, but remained stuck to the wafers.) The Blue Glue is scheduled for a full manufacturing trial. It is our plan to use Blue Glue for sawing of ultra-thin wafers.

BP Solar has taken two approaches to wafer demounting. One has involved a subcontract effort at ARRI, where they have built a wet wafer demounting prototype. This work will be described in detail below. The second has been to work with vendors of automated equipment. This effort is still ongoing with several potential vendors of wafer demounting equipment for standard thickness wafers, but none that will guarantee performance with ultra-thin wafers.

The initial ARRI prototype was described in detail in the first Annual Report of this contract[3]. ARRI investigated multiple methods for automated wet wafer demounting. The combination of vacuum / shearing has been consistently identified as the most promising for this particular scenario. Throughout phase I, ARRI built five generations of prototypes to achieve wet wafer coin stack demounting. The following items have been identified as most relevant to the success of the process:

- A special vacuum pump design is necessary to cope with minor fluid ingestion. Certain makes of venturi pumps can be easily modified for operation in this environment by removal of a cleaning filter.
- The vacuum cup material found to be optimal in terms of friction (soft silicone) is also compromised by presence of solvent; contact with a solvent must be avoided or minimized by thorough rinsing with water to prevent warping and loss of sealing. However, contact with the wire saw slurry has no deleterious effect on this vacuum cup material.
- The maximum shearing speed between wafers is limited by the high interfacial traction forces present, to a point where a single manipulator will not be able to perform both the singulation and cassette placement functions fast enough. However, with a “hand-over” operation after peeling the wafer from the stack, it is possible to achieve cycle times comparable to human handling (between 2 and 3 seconds per wafer).
- It has been found necessary to have a counter-rotating brush for most effective separation of the wafer.

Figure 9: Blue Glue trial – Glue releases from the wafer not the mounting beam

The Phase 1 prototype was successfully demonstrated with wafers that had been individually flushed with water and thus were free of solvent (vacuum held with no problems). Additional testing was performed with wafers soaked in slurry exactly as they come out of the wire saw machine (carefully demounted by hand). The intent was to see if the machine could singulate wafers that had not been exposed to solvent and that were heavily drenched in slurry. The prototype was successful in demounting under these conditions. Virtually no slurry ingestion into the vacuum system was observed, presumably due to the heavy viscosity of the fluid. Performance of the vacuum cups in peeling wafers from the stack was satisfactory; although the slurry might have lowered the traction from the vacuum cups, it also works to diminish interfacial frictional forces.

ARRI identified and successfully completed upgrades to the wet wafer demount prototype developed during Phase I of this program. The modified prototype was designed to be used for testing with ultra-thin 12.5 mm wafers. The prototype is shown in Figure 10.

Representatives from ARRI were onsite during the ultra-thin wafer testing to operate the wafer singulator system. The concept of the device involves using actuator controlled vacuum cups to engage the top wafer of the stack. After the cups have adhered to the top wafer, they are actuated forward to a position clear of the stack. During this process there is a bond between the wafers due to the presence of the viscous slurry. This causes multiple wafers to cling together and move forward as one unit. To prevent this, a rotating brush is placed such that the underside of the singulated wafers contact the brush. The

friction between the brush and the wafers forces all the wafers back onto the stack except for the top wafer which has been engaged by the vacuum cups. At this point the wafer is released and the vacuum cups are actuated back to the starting point. The wafer stack is indexed upward and the process is repeated. The singulator will be evaluated by its ability to operate under two conditions: the first involving slurry-coated wafers, and the second involving wafers that have undergone a solvent rinse.

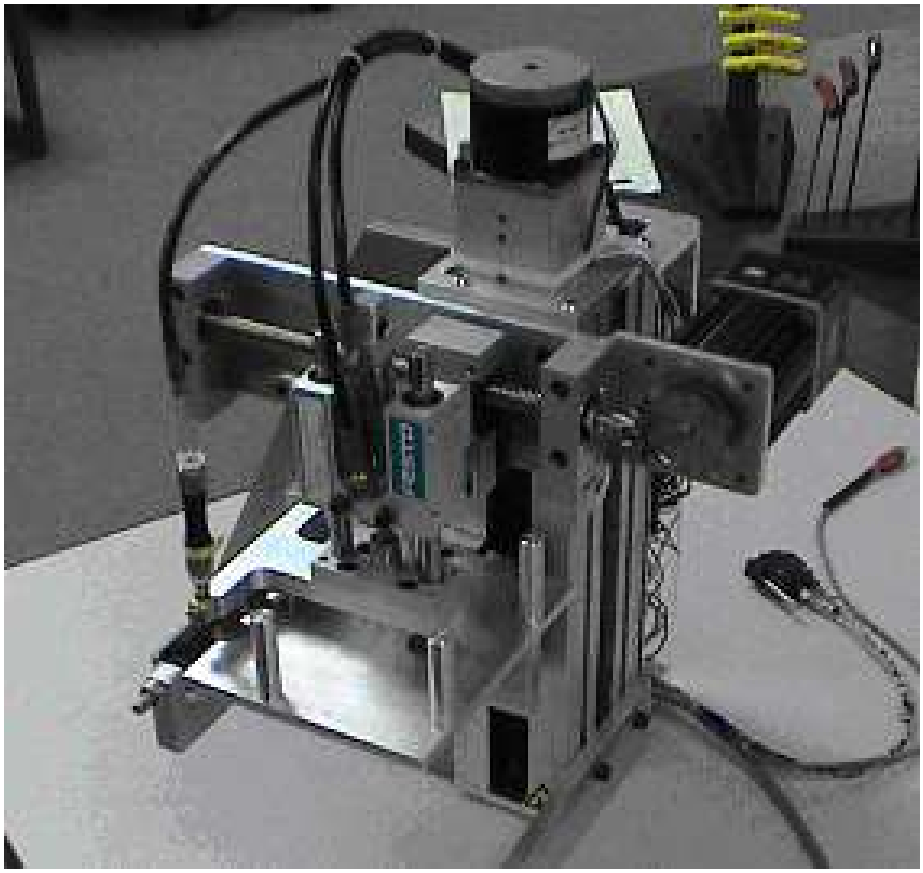


Figure 10: ARRI Wet Wafer Demounting Prototype

Performance with wafers directly from the comb, still slurry covered was not acceptable. It was noted that a setting period made the separation process more difficult as the slurry cooled and became more viscous. The rotating brush could not provide enough counterforce to overcome the slurry-induced bond between the wafers. The downward displacement of the vacuum cups was increased and the wafers were more firmly pressed against the brush. This resulted in increased friction between the wafer and the brush, but wafers began to consistently fracture. The yield of intact wafers was very low.

Since the Phase 1 tests, replacement suction cups allowed testing of solvent soaked wafers. The singulation device still required significant manual intervention, mainly due to difficult adjustment points for pick height, limited pick distance, and a preset indexing feature that was set to 250μm thickness so the stack advanced too far for each wafer extraction. These weaknesses were documented and sent back with ARRI for further improvement. Figure 11 shows the unit in operation.

Figure 11: ARRI Wet Wafer Singulation Prototype in Operation

3.4.2 Handling of Ultra-thin wafers

Once ultra-thin wafers are demounted from the wire saw comb, they must be handled through the production line and ultimately incorporated into PV modules. Once again BP Solar has taken a two pronged approach to solving this problem. The first approach has been to have ARRI work on "near-zero contact pressure" (NZCP) handling methods for ultra-thin cells and wafers. The second approach has been to run thinner than normal wafers through the cell line to determine which handling steps result in excess breakage and then to modify or eliminate those for future thin cell runs. Each of these approaches is discussed below:

ARRI Handling Effort

During the phase 1 effort (as reported in the First Annual Report[3]) ARRI reviewed wafer handling approaches and selected two methods, air levitation and electrostatic levitation for future evaluation.

Electrostatic handling holds much promise as an NZCP wafer handling method. Electrostatic *levitation* has been achieved mainly at the research level. It should be investigated further for critical non-contact operations. The electrostatic *chucking* (contact) method is already in use in semiconductor manufacturing, and is explained in more detail. An electrostatic manipulator can handle thin wafers in a contact-less manner using the "Direct Electrostatic Levitation and Propulsion (DELP)" technology (developed by Applied Electro-Optics Inc. of Mansfield, Massachusetts). The novel aspect of this manipulator is that it does not distort wafer's shape during the handling process. This is because that the force applied to the wafer is same as that of the wafer's gravity. Furthermore, the force is evenly distributed on a wafer. However, the horizontal motion of the wafer is not controlled by the electrostatic force and must be passively restricted either by mechanical stoppers or by lateral force.

Figure 12 shows a point-to-point wafer handling system using electrostatic levitation technology. The wafer being transported is a standard 12-inch diameter single crystal silicon wafer, which is suspended

under the levitation unit with a 400 micron gap. The levitation unit is mounted on a linear stage, which is driven by pressurized air.

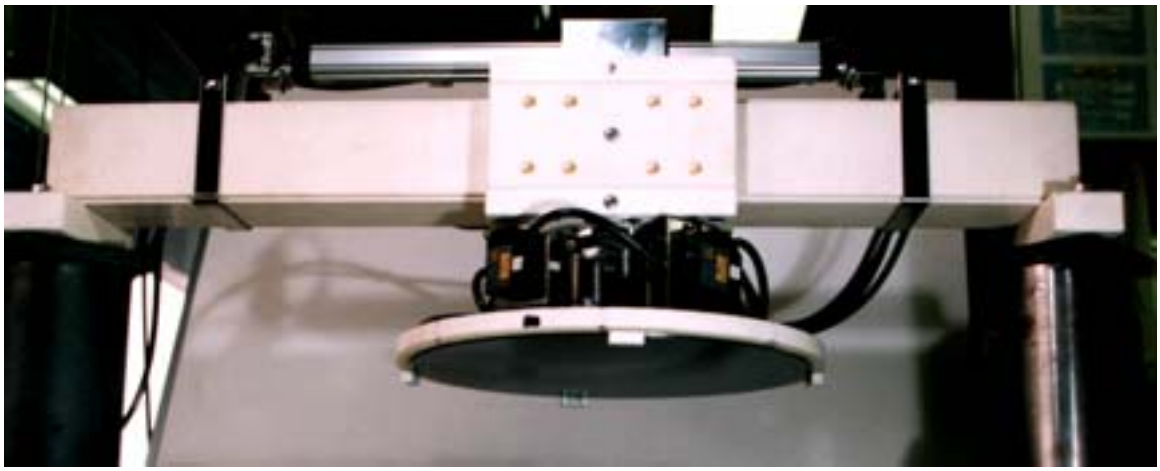


Figure 12: Electrostatic Wafer Levitation Device

The electrostatic chucking method has proven fully compatible with regular and thin wafers, but it was not as effective with processed cells, particularly when coupled through the front surface (target could be acquired and lifted, but would decouple easily with the application of a light external force). However, electrostatic field strength can be improved through more highly engineered dielectrics and higher voltages in order to retain this technology as an alternative.

The Air levitation work was described in detail in the first Annual Report[3]. Three prototypes were produced and evaluated. All are based on the principle of generating a horizontal stream of high-velocity air over the surface of the wafer to produce a vacuum; the air-stream is rendered horizontal either by direct impingement on the wafer or by the action of a flow-diverting valve.

Two of the designs are non-contact, with the wafer levitating as if on an "upside-down" air table, and the third exerts minimal contact to stabilize its horizontal motion. In order to evaluate the performance of the three nozzles, a series of tests were conducted. These tests involved the flow rate, noise output, and the lift capacity. The three nozzles exhibited similar behavior in that 8 psi was around the minimum pressure to lift the wafer off a surface and 9.2 psi produced an acceptable amount of lift to firmly hold the wafer in place. In the first test, the flow rate in standard liters per minute was measured. It was observed that the nozzle design yielded approximately twice the flow rate as the diffuser.

The radial diffuser and nozzles present promising new approaches to handling the wafers. The diffuser consumes less air than the other two but generates the lowest lift. The contact nozzle holds the wafer in place but the contact may not be compatible with some processes. The no-contact nozzle appears to be the best concept because it generates the most lift and consumes roughly the same amount of air as the contact nozzle. Robotic testing proved that the devices could adapt to a fast horizontal speed. Air consumption is lower than that required for standard vacuum cup systems, runs at lower pressures, and demands no special filtration requirements.

During Phase 2 preliminary experiments showed that the air levitation methods could be used to pick up ultra-thin (in this case 150 micron thick) wafers as well as fully processed solar cells and cells with tabs. Further work with air levitation wafer handling has been focused on specific areas within the BP Solar

process line. The first application was development of a handling tool to remove wafers from a SiN furnace.

The device works by forcing a high velocity stream of air over the surface of the wafer. This has two effects, the first is a vacuum created that generates a force into and perpendicular to the plate, the second is a planar force that is parallel to the wafer and consistent with the direction of the airstream. This levitates the wafer while simultaneously extracting it from the wafer boat.

In order for the device to work properly, it must be positioned at a precise height over the surface of the wafer. This is due to the fact that the vacuum draws the wafer into the plate until an equilibrium point is reached. If the gap is greater than this distance, the wafer will be pulled upward while it is still restrained by the buttons and the frictional forces resisting forward motion will be greatly increased. If the allowed gap is the same as the gap that exists during equilibrium, there will only planar forces acting on the wafer.

In order to allow for the proper spacing, grooves were machined into three sides of the face. This gives clearance room for the buttons which otherwise would protrude out and prevent the proper gap from being achieved. The grooves also aid in the alignment of the wafer. The device is shown in Figure 13.

Figure 13: Directional Airlev Plate

ARRI delivered the prototype directional airlev system to BP Solar. The prototype makes use of a "directional" airjet which not only levitates, but also imparts a horizontal biasing force to the wafer in order to dislodge it from underneath the holding buttons. The prototype is shown in the following Figures 14.

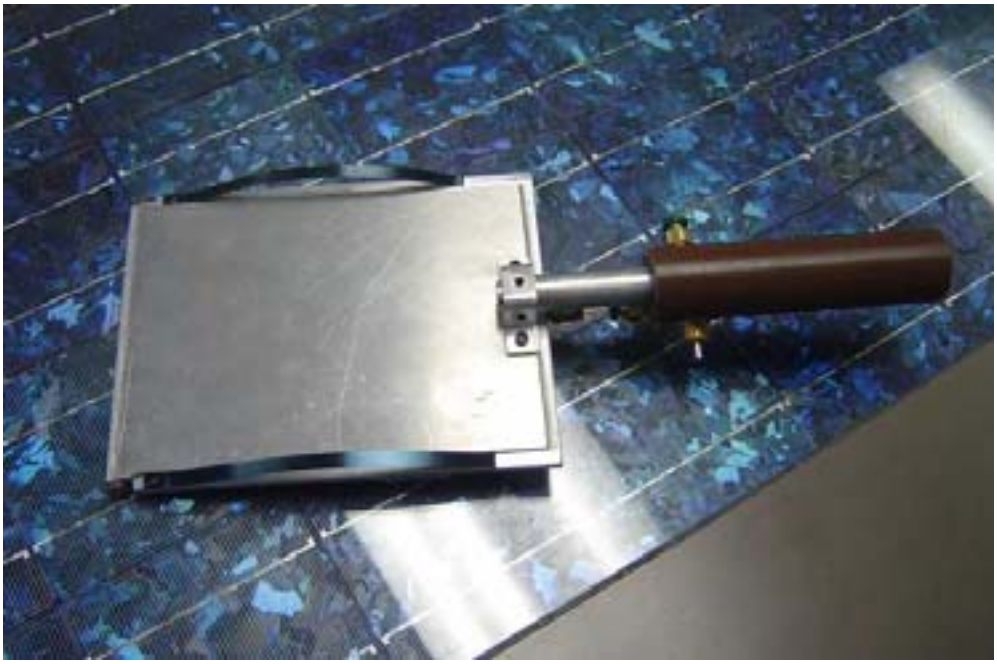


Figure 14: Airjet Pickup Tool

The Air-levitation Tooling has been evaluated for use as wafer pick up from silicon nitride graphite plate tooling in the SiN deposition equipment. The tool is not well suited for this purpose as the wafer is recessed in a pocket in the graphite plate. When the tool is activated to pick the wafer, the wafer moves rapidly across the 4 to 5 mm distance of pocket depth and tool offset and breaks.

The tool was also evaluated for performance in picking wafers and solar cells from stacks. Performance in picking a single wafer and releasing it to a stack was good. Careful alignment of the tool with the wafer is required. Performance in picking a wafer from a stack was poor. Wafers beneath the top wafer were carried along with the top wafer and eventually released to fall and break.

Efforts are now underway to develop an airlev tool for removing ultra-thin wafers from a belt. This is an important handling step in our cell process.

<u>In House Handling Efforts</u>
By running thinner than normal wafers though the cell line a number of ultra-thin wafer handling issues have been identified.

- When placed in cassettes for cleaning and etching, ultra-thin wafers tend to stick together after the wet processing. Because they are stuck together, the wafers do not rinse or dry correctly.
- Thinner wafers (175 and 200 microns), although weaker, are more flexible than 250 micron thick wafers. Some of the breakage appears to be more dependent on impact than on flexure.
- Some of the increased breakage of thin cells can be attributed to loaders and unloaders, which, though designed to be low impact, are in many cases slightly out of alignment.
- Carriers and cassettes are often slightly warped or distorted, resulting in wafer impact in situations where it should not occur.
- Conventional vacuum chuck depressions allowing manual (thumb and finger) pick-up have demonstrated wafer breakage with thin wafers.

After correcting a number of these issues, two pilot runs, each with about six thousand 225 micron thick wafers, have been processed through the cell and assembly lines. The mechanical yields in both cases were comparable to standard mechanical yields in both cell and assembly lines. There was no significant difference in efficiencies. A larger trial of 225 micron wafers is planned.

3.5 Cell Process Development

In this task, BP Solar is developing high efficiency cell processes for very thin silicon wafers (with the assistance of North Carolina State University). BP Solar is assessing the compatibility of the process cell process equipment to handle 100 μm thick wafers.

3.5.1 Texturing work

Effective surface texturing will be important to provide good light trapping in thinner cell designs. During the first year of the program two different approaches, Reactive Ion Etching (RIE) and Chemical Iso-Texture (ICT) were evaluated. The ICT process was chosen for future development as it resulted in greater efficiency gains and appears to be a lower cost process to implement. The impact of ICT on cell parameters is presented in Table 4.

Table 4: I-V characteristics comparing planar with ICT surface preparation

	FF	J_{sc}	V_{oc}	Eff.
	%	mA/cm²	mV	%
NaOH	76.3	31.2	615.9	14.6
Iso texture	76.6	33.2	614.1	15.6
Gain	0.3	**2.0**	-1.8	**1.0**

Two modules were fabricated – one with the ICT cells and the other with the baseline control cells. Module measurements indicate that there is a gain in I_{sc} of 4.2 % and power of 4.8 % relative (as shown in Table 5).

Table 5: I-V characteristics of the modules made from planar and ICT cells

Module	FF	I_{SC}	V_{OC}	P
	%	A	V	W
NaOH	74.5	4.98	22.2	82.5
Iso textured	75.0	5.19	22.4	86.5

During the second year of the program the development efforts included verification of the ICT process on larger groups of wafers and definition of the process specifications for implementation in manufacturing. The first attempts at texturing etching larger batches of wafers demonstrated that our standard wafer cleaning process was not conducive to producing a quality texture. The saw damage that results from wafering acts as a "seed" to initiate the texture etching. The amount of saw damage remaining after wafer cleaning will determine the quality of the texturing. The anti-foam additive in the detergent solution was found to contain KOH and BP Solar adds NaOH to the detergent to enhance cleaning and help remove the mounting glue. Both KOH and NaOH etch away some of the saw damage and so inhibit the iso-chemical texturing.

Three different wafer cleaning methods have been evaluated.

1. The first approach was to incrementally reduce the NaOH used to help remove the brick mounting glue. At 0% concentration the wafer surface appeared to be suitable for iso-texturing, however the wafers were not adequately clean and the glue was not removed. At .5% concentration the wafers were very clean and all of the glue was removed. The 1% solution also cleaned the wafers very well, however the resultant surface did not adequately iso-texture.
2. The glue manufacturer recommended a totally new detergent. This worked very well to both clean the wafers and remove the glue. The initial results indicated that this surface was okay for iso-texturing.
3. The final method tested was an acid etch solution suggested by University of Konstanz (UKN). This was found to remove the glue extremely well and quickly, however it did not clean the wafers at all.

Based on these experiments a larger trial was initiated using the new detergent. The modified cleaning solution produced very clean wafers and suitable surface characteristics (no removal of micro saw damage). However, there was not adequate removal of the brick mounting glue strips. The original small scale trial was run at a temperature that was 10^{o} C greater than specification, which seemed to assist in glue removal. Unfortunately the large production bath was not able to maintain this higher temperature so glue removal was inadequate. A number of different experiments were conducted in an effort to improve the glue removal including changing the resin-to-hardener ratio of the glue and using ultrasonic agitation in the cleaning tank. None of these helped very much to remove the glue. While this work was underway, a parallel effort to cut ultra-thin wafers had identified the wafering glue as an issue. As described in Section 3.4.1 a new glue was identified that releases from the silicon, not from the mounting beam. This new glue appears to have solved the wafer cleaning issue.

A number of ICT trials have been completed. They continue to demonstrate a 250 mA short circuit current gain on 12.5 cm by 12.5 cm cells or approximately 5%. However, in many of the experiments there has been a loss in fill factor (~ 1.5 %) and a lower open circuit voltage (~ 3 mV). In addition to lower fill factor and voltage, there is a higher percentage of shunted cells, which we believe is due to problems in edge isolation. Loss in FF is mostly driven by lower shunt resistance and rarely by higher series resistance. The series resistance was only slightly higher than for standard production. With a deeper diffusion there is an increase in FF. Further experiments are needed to confirm whether this is due to emitter damage, insufficient doping/diffusion into the rough surface or plasma etch damage to the emitter.

There was some concern that the doping prior to diffusion may not be providing a sufficient or uniform source of phosphorus on the ICT surface. This could either be due to the increased area of the textured surface or that a hydrophilic surface was required for vapor doping (typically HF is used to produce a hydrophobic surface). An experiment was run to compare HF versus HCl cleaning prior to diffusion, essentially to produce different surface conditions, not as a cleaning comparison. The cell data in Table 6 shows that a hydrophobic surface prior to doping is preferred for an ICT surface.

Table 6: Preclean of ICT Surfaces before Diffusion

Precleaning	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
HF	**14.82**	**5.306**	**0.597**	**73.1**
HCl	**14.61**	**5.278**	**0.594**	**72.8**

3.5.2 Silicon Nitride High Efficiency Process Development

During the first year of the program, silicon nitride equipment was installed and started operation in Frederick. Implementation of the SiN process in Frederick increased the average efficiency from approximately 12.8% up to 14.5% at the cell test level. Efforts during the second year have focused on process control and process optimization.

A number of experiments were conducted in an effort to understand the impact of input variables on SiN thickness and refractive index. The effects of pressure, total flow, flow ratio and transport speed were investigated. The effect of temperature variation was measured but only at a single setting of pressure, flows and transport speed. Power settings certainly affect index and thickness, but since uniformity is primarily controlled by power, the affect of power was not investigated. Table 7 presents our findings. For example, index increases as pressure increases, but decreases as transport speed increases. There is no interaction between pressure and flow ratio. There is an interaction between total flow and flow ratio; at higher total flow a lower SiH_4:NH_3 ratio is required to obtain a given index. Index increases and thickness decreases as temperature increases. Although this was measured at a single setting of flows, pressure and transport speed, we expect that it is likely true in general.

Table 7: Impact of Input Variables on SiN Thickness and Refractive Index

	Pressure	Total Flow	SiH_4:NH_3	Transport Speed
Refractive index	increases	increases	increases	decreases
Thickness	increases	increases	decreases slightly	decreases

A large number of experiments have been carried out to evaluate changes in refractive index and film thickness. In general neither the cell open circuit voltage or fill factor is affected by large changes in these parameters. The cell current does decrease slightly as the index increases, but some of this decrease is due to poorer index matching to air. When index matched to EVA/glass the decrease disappears at least until the films start becoming absorptive at very high indices.

Several experiments were conducted to evaluate the effect of flow rate on cell performance. In both cases the flow rate and pressure were varied over a significant range. Pressure had little impact on cell performance. However, the cell efficiency was improved by a statistically significant amount by reducing the flow rate. This efficiency gain has been demonstrated in several independent experiments and is always driven by improved short circuit current. However, lowering the flow rate reduces the deposition rate and therefore reduces the through put so it has not been implemented in manufacturing.

3.5.3 Selective Emitter

A selective emitter refers to a process where a deeper diffusion is formed under the metallization to reduce series resistance and a shallower diffusion is formed in the collecting field to improve current collection. By decoupling the metallization diffusion from the field diffusion, higher cell efficiencies are expected. In the process under development at BP Solar, a dopant grid is printed with slightly wider screen openings than the front metallization pattern. This allowed for the front paste to be printed within this lower sheet resistance selective emitter. The field emitter is then diffused with a much lower sheet resistance so the metal must stay within the deeper emitter to avoid shorting the junction. The results from one of the trials are given in Table 8. The selective emitter process resulted in an efficiency gain of 2.5%.

Table 8: Cell Results of Selective Emitter Experiment

Group	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Baseline	15.83	5.072	614.8	75.4
Selective Emitter 55 Ohm/sq field	16.21	5.019	621.4	77.3
Selective Emitter 65 Ohm/sq field	16.01	5.03	616.9	76.7

It was found that switching to a textured wafer surface, using the same dopant paste screens originally designed for planar surfaces, created severe spreading of the grid pattern. This produced a great deal of shading (loss of field emitter area) which is suspected to be the reason for the lower current in this experiment. Voc decreases slightly as the sheet resistance increased suggesting that the surface passivating effect of the SiN AR coating needs optimization. The front metal profile was developed for a 50 ohm/sq. junction. Optimization for a 30-35 ohm/sq. junction should further improve the FF.

Additional work was done to investigate the paste spreading issue. A higher viscosity dopant paste was tested. Little improvement was seen and it was difficult to work with. A matrix of screen parameters was tested. As a result, a much improved screen specification was determined which would hopefully be suitable for both textured and planar surfaces.

The new screens reduced the degree of spreading of the dopant paste, but did not eliminate it. Table 9 shows the printed dopant paste width after drying for the standard screens and the new finer mesh screens. The new screens reduced the spreading, but not enough to solve the problem. Cell results from this trial are given in Table 10. An overall cell efficiency gain of 1.2% was seen, with all major parameters (Isc, Voc and FF) all increasing.

Table 9: Width of Printed Dopant Paste

	Original Screen (mm)	Finer Mesh Screen (mm)
Planar Wafers	**0.42**	**0.28**
Textured Wafers	**0.93**	**0.74**

Table 10: Cell Results for Selective Emitter with New Screens

Group	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Baseline	**15.83**	**5.280**	**620**	**74.8**
Selective Emitter 55 Ohm/sq field	**15.91**	**5.229**	**619**	**76.0**
Selective Emitter 65 Ohm/sq field	**16.02**	**5.309**	**620**	**75.3**

The mesh/emulsion in the new screen is now at the limit. The only way to obtain thinner fingers is to reduce the line width of the pattern. At this point, it is not possible to do this, since printing on the alignment setup wafers must be done on a planar surface for good visibility. Reducing the line width enough to compensate for the spreading would cause the dopant grid on the planar surface to be narrower

than the metallization grid, which is printed directly on top and alignment would not be possible. A new technique was developed which consisted of two independent alignment marks that were totally decoupled from the grid pattern. This would make it possible to reduce the line width opening enough to compensate for the spreading. Once the process is developed into a production mode it should be possible to use an optical alignment scheme, which would eliminate the need for these setup wafers. A hot melt version of the dopant paste is currently in development. Hot melt should not suffer from the spreading of printed lines on a textured surface.

3.5.4 Cell Breakage

As the cell thickness is reduced the potential for breakage is likely to increase. Therefore we began a set of experiments to characterize wafer strength and causes of breakage. Using a 4–point biaxial flexure tester, we have demonstrated that the force required to break a 250 micron thick wafer averages about 7 Newtons and that about 95% - 97% of the wafers tested fall into a distribution which is roughly Gaussian and falls between 5N and 9N. The remaining 3% - 5% break at lower forces and may be contributing to breakage and hence yield loss in our cell processing line. Much of this group is already damaged before the test. We have found that chipped cells break much easier than wafers with no chips, as expected. Perhaps less expected is that this is true whether or not they break at the chip, and whether or not the chip is pointed or curved.

It has been proposed that a bending test be used as a 100 % screening on all incoming wafers to weed out those likely to break. A concern is that subjecting wafers to a low stress level to weed out the weak ones may weaken the wafers which survive. We tested this by splitting 50 wafers randomly into two groups. One group acted as controls and was untouched. The second group was stressed to 5N to screen out weak wafers. About 3% of the wafers broke at this stress level. All remaining wafers from both groups were then flexed in our tester until broken. The breaking force required on average for the pre-stressed group was the same as that for the control group. Hence low level stressing of the wafers has no effect on the strength of the wafers which survive this low level stressing.

3.5.5 Hot Melt Front Paste

An effort is underway to optimize, qualify and implement hot melt instead of screen print front metallization. Hot melt has several advantages over screen print:

- Hot melt ink has the capability of printing taller and finer lines than screen printing. Figures 15 and 16 show a comparison of screen print versus hot melt lines after firing.
- Hot melt ink solidifies immediately after the print, so can be processed and handled without the need to dry it in a furnace first as is required when using conventional wet inks.

Initial work with the hot melt ink involved developing printing parameters and refining ink formulations, using the same firing conditions as used for the standard screen printed paste. The results from one such experiment is shown in Table 11. The first group hot melt group was printed using our standard technique in which the squeegee travel is perpendicular to the direction of the fine grid lines. In the second group, we rotated the same screen 90 degrees and printed with the squeegee traveling parallel to the grid lines. Typically, this is considered to be the preferred technique, and it did result in a marked improvement in the appearance of the grid lines with the hot melt product. *(Under normal conditions, using conventional ink, we have not seen much difference in the cell performance as a function of screen orientation with respect to squeegee motion.)*

The results indicate that this hot melt material performed very well at our standard production firing condition, easily besting the standard production material. Compared to our baseline ink the best performance with the hot melt material was roughly 4% better in overall efficiency. This was based on improved FF and a higher Isc value. The Isc gain is driven by lower shadowing due to thinner grid lines. The FF improvement is driven by a combination of higher cross-sectional area in both the grid lines and

bus bar, with the possible addition of a reduction in contact resistance between the fired ink and the emitter layer. In this case, the improvement in Isc is slightly greater than we expected based on the reduction in shadowing due to the narrower grid lines.

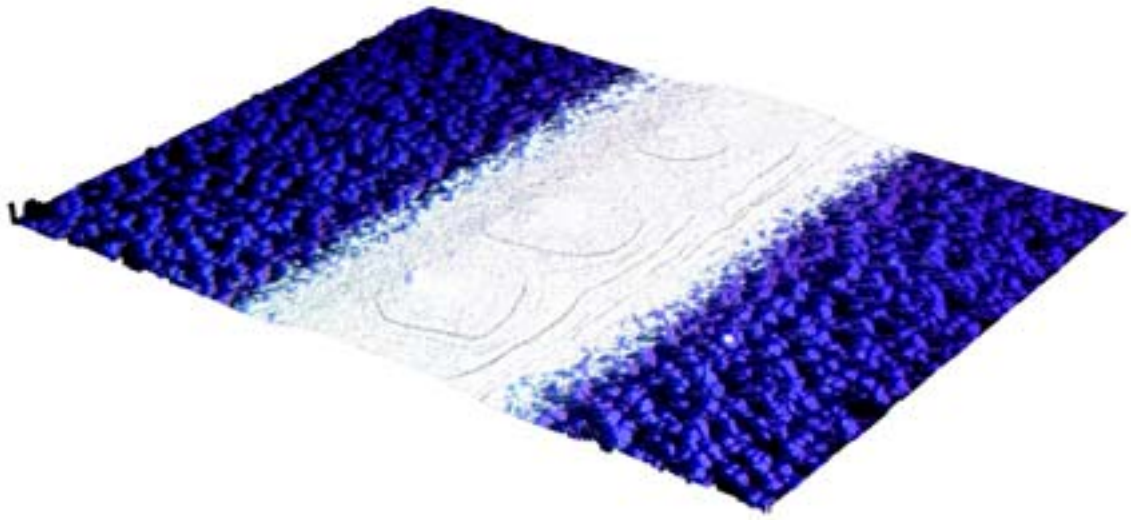


Figure 15: Standard paste deposition shown after firing using the 3D capabilities of the Syncroscopy system

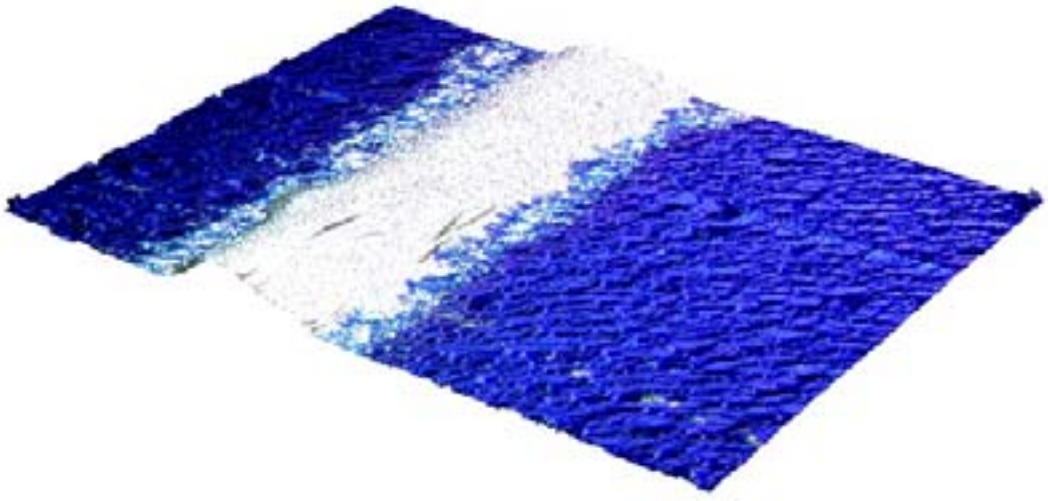


Figure 16: **Hot melt material shown after firing using the 3D model capabilities of the Syncroscopy system**

Table 11: Hot Melt Front Paste Trial

	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Screen Print Control	**13.33**	**4.796**	**590**	**73.6**
Hot Melt Across Grid	**13.85**	**4.881**	**593**	**74.8**
Hot Melt Parallel to Grid	**13.89**	**4.874**	**593**	**75.1**

The next step was to optimize the firing using the hot melt paste. A 3-factor Response Surface Methodology (RSM) experiment was performed in the same furnace that production uses for contact firing. In addition to the two standard factors (belt speed and peak temperature) we included a third factor that represented the "slope" of the zone temperatures within the spike zone. The trial indicated that our baseline firing condition was already very well tuned for the paste. Only one condition out of fifteen showed any promise of being better than the standard condition. Cell results are provided in Table 12. Figure 17 shows a plot of the 3 variables and the measured cell efficiencies.

Table 12: RSM Trial of Hot Melt Paste Firing Conditions

Group	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Standard	**14.92**	**5.145**	**608**	**74.6**
Seven	**15.03**	**5.137**	**608**	**75.1**
Nine	**14.75**	**5.105**	**607**	**74.4**
Ten	**14.75**	**5.097**	**607**	**74.5**

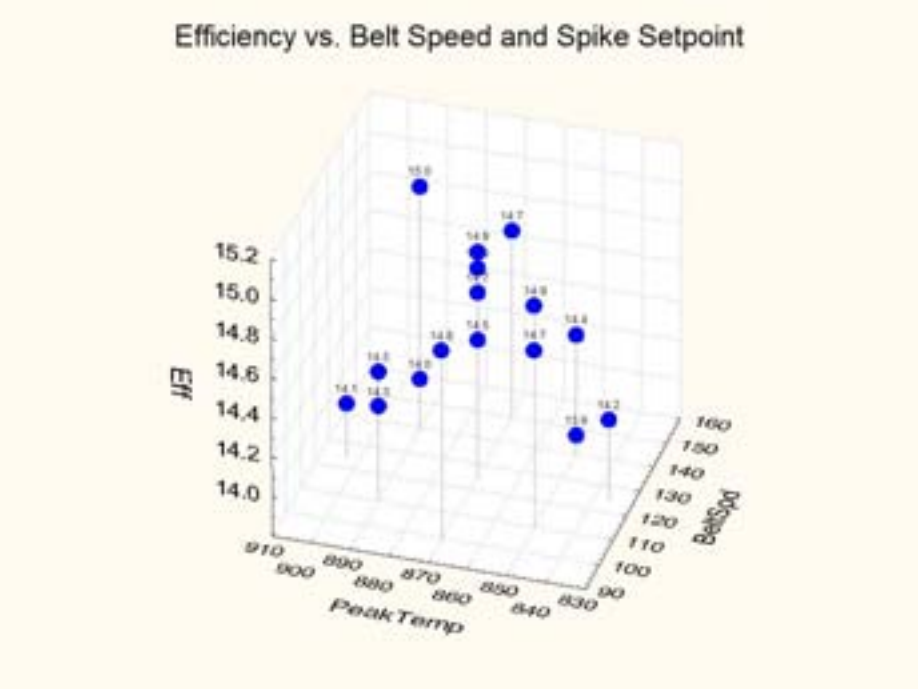


Figure 17: Cell Efficiency versus 3 Variables from RSM Trial of Hot Melt Paste Firing Conditions

Based on these results, the standard production firing condition was used to fabricate cells for qualification of the product. Sample of cells were tabbed on the standard automatic machines and pulled using our typical 45° angle. All of the solder joints had a pull in excess of our minimum specification of 0.5 lbs. Modules were then fabricated and subjected to our internal qualification tests including 500 thermal cycles and 1250 hours of damp heat. Hot melt front paste passed all of the tests with minimal power loss.

3.5.6 Thin Cell Process Development

All of the efficiency improvements discussed above particularly surface texturing, silicon nitride optimization, and the selective emitter will work at least as well with thin cells as with today's standard thickness. In addition, thin cells require work on the Back Surface Field (BSF)/back contact combination both because of its effect on the mechanical behavior of the cell as well as the fact that as the silicon gets thinner the back surface properties have a larger impact on cell performance. The standard Al paste back surface field causes a significant amount of bowing for standard thickness cells. With thin cells the bowing becomes excessive. So the thinner cells require the development of a new back surface process. Two different types of thin cell back processing are under study, low bow Al paste and a passivated back surface. The two concepts and experimental results on each is discussed below.

Low Bow Aluminum Paste

One of our paste vendors has developed an aluminum paste that is specifically formulated to reduce wafer bow after firing. This paste was initially evaluated on standard thickness cells where it duplicated the performance of our standard aluminum paste in terms of efficiency and yield. Modules made with these cells were subjected to our internal qualification tests including 500 thermal cycles and 1250 hours of damp heat. The new low bow Al paste passed all of the tests with minimal power loss.

The low bow paste was then evaluated using 115 micron thick wafers. No wafers broke during screen printing or firing, but about 30% of the wafers suffered edge chips in the screen printing process indicating that a change in handling will be necessary. The Low Bow paste resulted in a 4 mm bow in the wafers for the group processed with 0.008g/cm^2 of paste and a 3 mm bow for the group processed 0.007g/cm^2 as shown in Figure 18. The electrical results are shown in Table 13. The results were confused somewhat because of a far from optimum AR coating that resulted in a low short circuit current. However, the voltages and fill factors were reasonable, especially for the group processed with the larger amount of Al paste.

Table 13: Cell Results for Thin Cells with Low Bow Al Paste

Paste Amount (gm)	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
1.04	**11.7**	**3.58**	**591**	**0.72**
0.9	**10.8**	**3.55**	**590**	**0.68**

A second group of 115 micron wafers was processed into solar cells using the low bow Al paste. Based on the results of the first experiment the standard amount of paste 0.008g/cm^2 was used in all the groups. A variety of firing temperatures were utilized to determine if the thinner wafers have to be fired under different conditions than the standard thickness cells. The results are given in Table 14. None of the groups approach the efficiency values (~ 14.5%) normally achieved for 250 micron wafers. The best efficiencies were achieved using the standard firing temperature. These cells have considerably lower fill factor driven mostly by high series resistance. It is not clear at this time while the series resistance is higher for the ultra-thin cells.

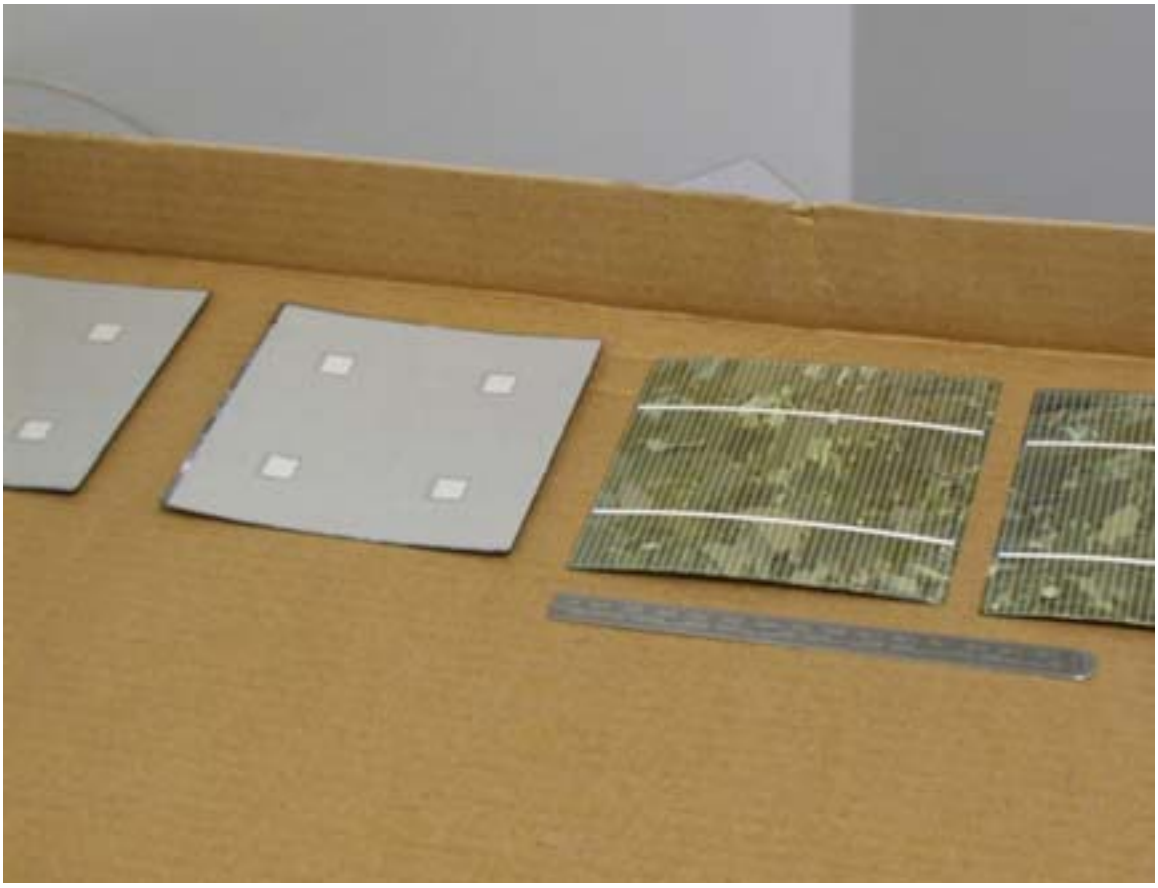


Figure 18: Thin Cell Bowing with low Bow Al Paste

Table 14: Ultra-thin Cells Processed with Low Bow Al Paste

Firing Conditions	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Low	**12.35**	**4.781**	**597**	**67.6**
Medium	**12.66**	**4.804**	**600**	**68.6**
High	**12.33**	**4.707**	**594**	**68.9**
Higher	**11.61**	**4.676**	**588**	**66.0**
Highest	**11.18**	**4.749**	**590**	**62.3**

Back Surface Passivation

If most of the area of the back surface can be well passivated high cell efficiency is possible. Since we already use PECVD SiN to passivate the front surface, it seemed logical to try using it to passivate the back with a fire through Ag paste grid (just like on the front).

The passivated back was first evaluated using 115 micron thick wafers. No wafers were broken, but about 20% of the wafers suffered corner chips in screen printing. No significant bow existed in the finished solar cells despite 115 micron wafer thickness. Electrical results for the Grid Back group were confused

by an un-optimized ARC resulting in low current. Voltage, series resistance and shunt resistance were fairly poor and were rejected by the cell test software as anomalous.
The second set of ultra-thin cells was fabricated with both SiN and a screen printed silver grid on the back. The results are shown in Table 15. None of these cells were particularly good. The best results were obtained with the lowest firing temperature. In all cases the fill factor was very low and the series resistance very high. The charge on the SiN may be of the correct sign to assist on the front, but to inhibit collection on the back.

Table 15: Ultra-thin Wafers Processed Using rear SiN Passivation and Ag Paste Grid

Firing Temperature	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Lowest	**10.14**	**4.378**	**574**	**63.0**
Lower	**9.66**	**4.383**	**572**	**60.2**
Low	**9.68**	**4.351**	**572**	**60.7**
Medium	**8.43**	**4.228**	**565**	**55.2**

3.6 Module Assembly

In this task, BP Solar is developing and demonstrating a module assembly process and the equipment suitable for very thin solar cells. This task is expected to result in an assembly process capable of producing framed, terminated PV modules using very thin cells at an overall yield exceeding 98%.

3.6.1 Laminated Diodes

Incorporation of bypass diodes is necessary in all but the smallest 12-volt modules. As cells get larger, the diodes must be able to carry the extra current produced by the larger cells. As modules get larger the number of diodes increases as a diode is required for every 12 to 24 cells, depending on the reverse behavior of the cell type. Indeed use of higher efficiency cells usually means fewer cells per diode. As we discussed in the First Annual Report, use of a laminated diode eliminates these external diode mounts and extra parts and the steps required to protect them from corrosion, and simplifies the circuitry. The laminated diode assembly consists of surface mount type Schottky diodes pre-assembled on a PC board coated with lead free solder. The cell matrix is connected to this laminated diode assembly, and the whole assembly is then encapsulated between the glass and the back sheet as routinely done on current PV laminates. The external diode connections are no longer required. In some cases this means a total elimination of enclosures and encapsulant filling.

The BP5170S module was selected as a pilot run candidate due to the complexity of its cell matrix layout. The old design required six diodes and three small potted junction boxes for each 72-cell module. Two pilot run trials were successfully conducted at two major BP Solar manufacturing sites: Madrid (Spain) and Frederick (USA). The laminated diode boards functioned properly in the pilot run samples and no performance deviations were recorded. A saving of 5 minutes in the assembly line was achieved. The diode board version of the BP 5170S was released to manufacturing and all 72 cell Saturn modules are being built with this technology.

A second product (BP3125) was then selected for release with the diode board. The BP3125 uses 15.7 cm by 15.7 cm multicrystalline cells. The large cell size results in high current levels (~ 8 Amp). There are no available axial lead diodes which can handle such high currents without exceeding the temperature rating of the junction box. The chip diode in the diode board was the only viable option. This product was piloted in our Australian plant and is now being built worldwide with laminated diode boards.

Several new products have now been or are in the process of being introduced with laminated diode boards. Efforts are underway to ultimately switch all BP Solar 72 cell modules to laminated diode boards.

3.6.2 Module Terminations

Presently BP Solar produces modules with two different junction boxes. One was the heritage Solarex box and the other was the heritage BP Solar box. In the First Annual Report we discussed the design, of a new junction box to replace the two now in use.

The new design incorporates the best features of both of the previous designs. Like the heritage BP Solar box, it has a hinged lid with captive screws, and the ability to accept a gasket around the edge of the lid for installation where IP 65 (watertight) rating is required. Like the heritage Solarex box, it has a solid bottom, which protects the module backsheet from accidental damage during installation of array wiring, as well as providing a better surface for adhering the junction box to the back of the module. Also, like the heritage Solarex box, it has knockouts which are compatible with either metric or English size conduit fittings.

During the second year of the program the new junction box was qualified through UL 1703, IEC 61215 and IP 65. Implementation will occur when the inventory of old style boxes has been depleted, probably in early 2005. Figure 19 shows the new box.

Figure 19: New Junction Box

3.6.3 AR Coated Glass

It is well known that use of an anti-reflective coating on the outer glass surface can increase the coupling of light into a PV module and therefore increase its conversion efficiency. While AR coated glass has been available for years, in the past these coatings were unable to survive long term exposure outdoors. Recent advances in glass coating technology have improved the ability of the coatings to survive the outdoor environment.

AR coated glass was obtained from three different vendors. Each of the AR coatings was formed in a different way.

1. Flabeg – porous SiO_2 formed by dipping[4];
2. Vendor 2 - deposited multi-layer films; and
3. Vendor 3 – etched coating.

In each case full sized modules, with either 36 (12.5 cm by 12.5 cm) cells or 72 (12.5 by 12.5 cm) cells, were fabricated along with controls using our standard low iron glass. Every effort was made to uniformly mix the cells into the modules.

Flash test results taken under Standard Test Conditions (1000 W/m^2, AM1.5 spectrum, 25° C) for the modules made using the Flabeg AR coated glass are shown in Table 16. The screen print multicrystalline silicon data is from ten test modules and ten controls. The Laser Grooved Buried Contact (LGBC) mono-Si data is taken from six test modules and six controls. The screen print mono-Si data is taken from three test modules and is compared to production data on a large number of modules. This glass produced a significant increase in power (2.5 to 3%) driven by higher short circuit current (2 to 2.6%) as expected for AR coated glass.

Table 16: Results for Flabeg AR Coated Glass

Cell Type	Glass Type	Voc (V)	Isc (A)	Pmp (W)	Improvement in Power
Screen Print Multi-Si	Control	43.42	4.963	156.3	
	Flabeg AR	43.46	5.098	160.5	2.7%
LGBC Mono-Si	Control	43.89	5.523	180.4	
	Flabeg AR	44.03	5.624	184.9	2.5 %
Screen Print Mono-Si	Flabeg AR	44.24	5.54	180.1	~3.0%

Glass from the other two vendors did not result in measurable gains above our standard glass. In both cases their un-AR coated glass produced significantly less power than our standard glass. Their AR coated glass resulted in approximately a 1% increase over their non-AR coated glass, but did not match the results from our standard glass. Measurements are now underway to determine why these other 2 types of AR coated glass did not produce the expected current gain.

The AR coating on the glass could change the module's energy rating by changing the spectral response or the angle of incidence response of the module. Several AR coated modules have been under test at our Homebush, Australia site and a third party site in Germany. In all cases the AR coated modules are producing about 5% more energy than the controls. Since the AR coated modules measured 2.5 to 3% higher at STC, the AR coated modules are producing at least 2 to 2.5% more energy than would normally be expected from the measured STC power.

Modules made using each of the three types of AR coated glass have been subjected to the IEC 61215 test sequence, particularly the long term exposures – thermal cycle, humidity-freeze and damp heat. All three of the AR coated glass types successfully passed the qualification tests without any evidence of degradation of the coatings. (Remember however, that the entire coating could be dissolved away and the resultant power loss would be less than the standard's acceptable level of 5 %.) One module that has been

under outdoor test for more than a year in Australia is also showing no evidence of degradation either in terms of power loss or visual change.

3.6.4 Module Performance Based on Cell Sorting Schemes

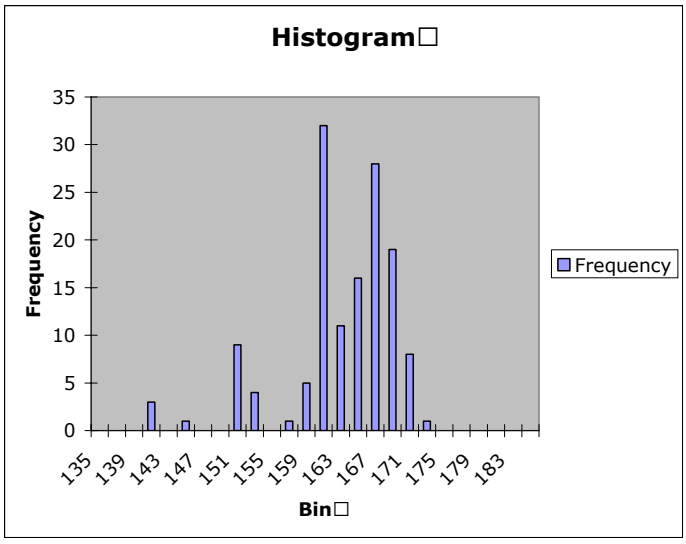
We have developed a model that manufactures "virtual" panels based on various cell sorting schemes. This was driven by a desire to optimize the module distribution resulting from the actual cell distribution. There have been several reports of achieving higher overall power due to better matching of the cell performance at the module level (less mismatch loss) by sub-binning using Ipmax.

The results of the modeling indicate essentially no benefit to the sub-binning schemes attempted so far as the power bins are reasonably narrow. We have seen that a large, open-ended power bin does not produce the high-end modules you can achieve by adding an additional bin at the upper end of the distribution.

These results are presented below as module distributions for roughly 10,000 cells. The data shows a histogram of module performance, along with the resultant power divided into two categories; modules > 165 Watts, and modules > 171 Watts. Note that this work was done for silicon nitride 12.5's. Figure 20 shows the results obtained using only 3 broad cell bins. Figure 21 shows the same cell distribution sorted into 4 bins. Introducing the 4th higher efficiency bin results in many more, higher power modules. The 3 bin system yields a combined wattage of 1541 Watts from 9 modules with power above 171 Watts, while the 4 bin system increases this number to 5321 Watts from a total of 31 modules with power above 171 Watts. However, note that the total power of the modules produced is virtually the same in the 2 schemes (22,504 Watts versus 22,508 Watts).

Technique:□ ***Frederick power bins (using only original 3), then test sequence***

Bin□	*Frequency*□	
135	0	0
137	0	0
139	0	0
141	3	423
143	0	0
145	1	145
147	0	0
149	0	0
151	9	1359
153	4	612
155	0	0
157	1	157
159	5	795
161	32	5152
163	11	1793
165	16	2640
167	28	4676
169	19	3211
171	8	1368
173	1	173
175	0	0
177	0	0
179	0	0
181	0	0
183	0	0
More	0	



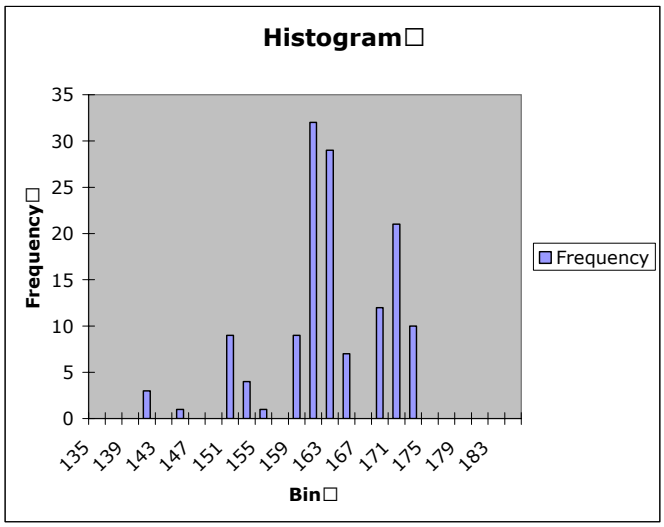
Total Module Power Product:	22504
Modules Watts of >165 Panels	12068
Modules Watts of >171 Panels	1541

Figure 20: Model Prediction of Module Output Using 3 Cell Bins

The numbers under the heading 'Bin' are the powers obtained from a 72 cell module. The numbers under the heading 'frequency' are how many modules fell in this power bin. So bin 163 would include all modules with power from 161.1 watts to 163 watts. In this case there were 11 modules in that power bin.

Technique: *Frederick power bins (including #4 @ 14.8), then test sequence*

Bin	Frequency	
135	0	0
137	0	0
139	0	0
141	3	423
143	0	0
145	1	145
147	0	0
149	0	0
151	9	1359
153	4	612
155	1	155
157	0	0
159	9	1431
161	32	5152
163	29	4727
165	7	1155
167	0	0
169	12	2028
171	21	3591
173	10	1730
175	0	0
177	0	0
179	0	0
181	0	0
183	0	0
More	0	



Total Module Power Product:	22508
Modules Watts of >165 Panels	8504
Modules Watts of >171 Panels	5321

Figure 21: Model Prediction of Module Output Using 4 Cell Bins

The numbers under the label 'Bin' are the powers obtained from a 72 cell module. The numbers under the heading 'frequency' are how many modules fell in this power bin. So bin 163 would include all modules with power from 161.1 watts to 163 watts. In this case there were 29 modules in that power bin.

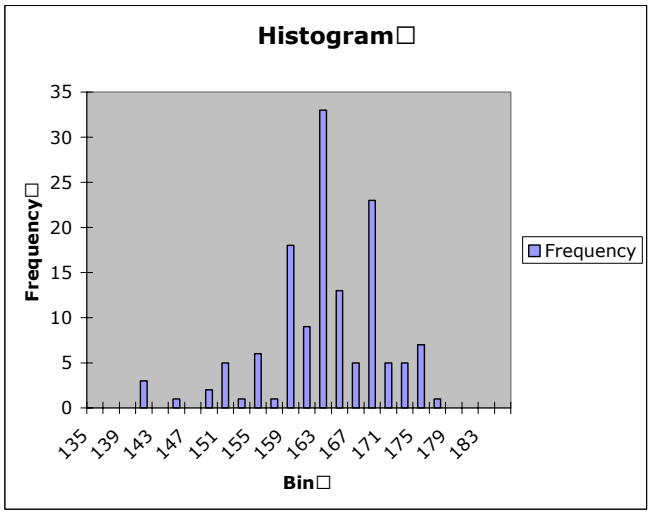
Figure 22 shows the same cell distribution sorted into 4 bins just like Figure 21. In Figure 22 however, the cells within a bin have been further sorted into sub-bins based on current at maximum power, Ipmax. Adding the sub-binning has very little impact on total module output power (22,508 Watts versus 22,540 Watts). On the other hand, sub-binning reduces the number of high power modules with power above 171 Watts from 31 modules producing 5321 Watts without sub-binning to 18 modules producing 3122 Watts with sub-binning. So there appears to be little reason to spend the extra effort to sub-bin the solar cells.

Today most of the modules produced by BP Solar have installed bypass diodes. When testing these modules on the solar simulator, the I-V curve often contains a bump at high current levels. When evaluating this in more detail, modules with bypass diodes tend to have higher short circuit current and lower fill factor than equivalent modules without bypass diodes. The explanation for this was that since cells had different short circuit current levels, those with the lowest currents were being driven into reverse bias and turning on the diodes. We decided to use our model to verify this.

Figure 23 shows the simulation of the I-V curve for a 72 cell module with bypass diodes. The model predicts the presence of the bumps in the I-V curve near short circuit current and models the increased Isc with reduced fill factor that we see in practice. The amount of effect on Isc and FF grows larger as the degree of mismatch within the cells increases. The good news is that this phenomena does not impact the measured peak power of the module at all.

Technique: *Frederick power bins (including #4 @ 14.8), then Ipmax*1.3, then test se*

Bin	Frequency	
135	0	0
137	0	0
139	0	0
141	3	423
143	0	0
145	1	145
147	0	0
149	2	298
151	5	755
153	1	153
155	6	930
157	1	157
159	18	2862
161	9	1449
163	33	5379
165	13	2145
167	5	835
169	23	3887
171	5	855
173	5	865
175	7	1225
177	1	177
179	0	0
181	0	0
183	0	0
More	0	



Total Module Power Product:	22540
Modules Watts of >165 Panels	9989
Modules Watts of >171 Panels	3122

Figure 22: Model Prediction of Module Output Using 4 Cell Bins with Ipmax Sub-binning

The numbers under the label 'Bin' are the powers obtained from a 72 cell module. The numbers under the heading 'frequency' are how many modules fell in this power bin. So bin 163 would include all modules with power from 161.1 watts to 163 watts. In this case there were 33 modules in that power bin.

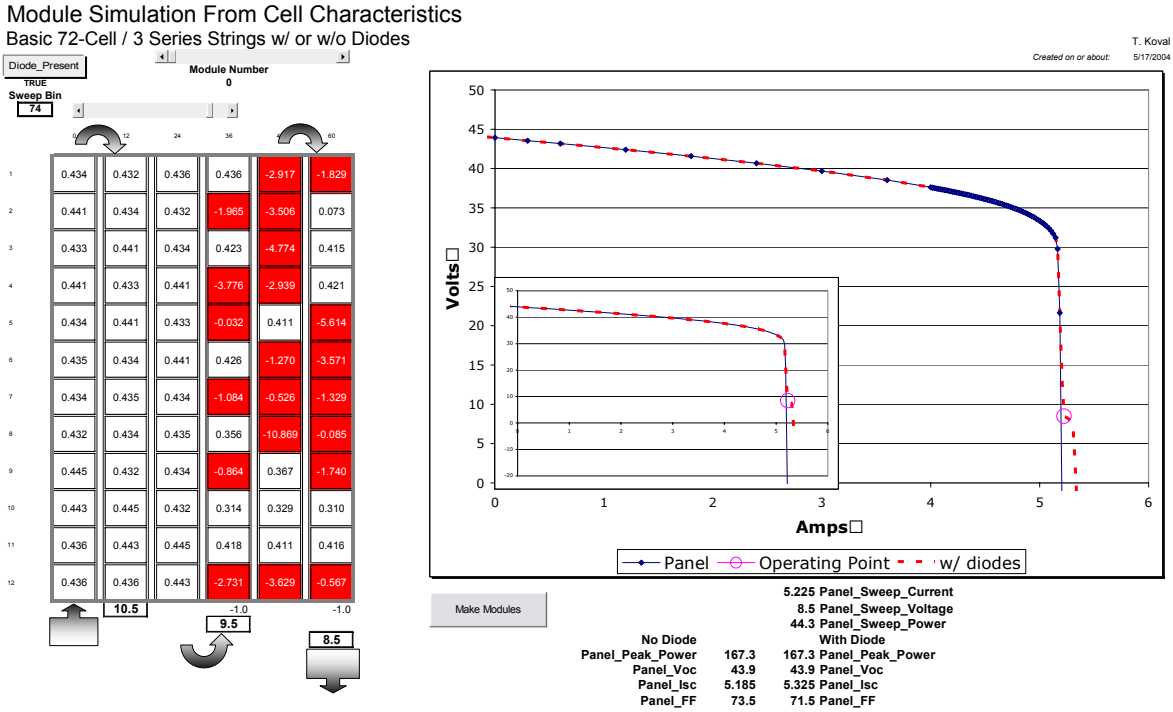


Figure 23: Simulation of By-Pass Diodes Turning on during I-V Testing

3.6.5 Interconnecting Ultra-Thin Cells

The major concern with module processing of ultra-thin cells has been the tabbing and stringing functions where individual cells are connected to the metallic tabbing ribbon. BP Solar traditionally uses hot bar resistive heating to solder the tabs onto the cells. We have a concern that this process may cause too much breakage when applied to ultra-thin cells. Therefore, while we will continue to evaluate the use of hot bar soldering for ultra-thin cells, we will also assess several alternate approaches including light soldering and conductive adhesives. The sections below will discuss each in turn.

Hot bar resistive solder robot machinery

A number of efforts are underway to better understand the hot bar process and then to modify it for application to ultra-thin cells. Control of pressure and rate of decent of solder heads/tips has been shown to be critical in reducing cell breakage when soldering with resistive hot bars. The rate of decent at impact was shown to have a significant effect on breakage. Therefore, tools to evaluate temperature, pressure and force at impact of hot bar solder tips were developed. Thermocouples bonded in the metal of the solder heads were used with chart recording hardware to study ramp rates and time above temperature. Load cells were used to record static weight of individual solder heads and to reduce variation induced by robot hardware friction. A force gage and load cell tool were developed to integrate solder head static weight and velocity upon impact. An example of the force (in Newtons) variation for several tabbing and stringing robots is shown in Figure 24.

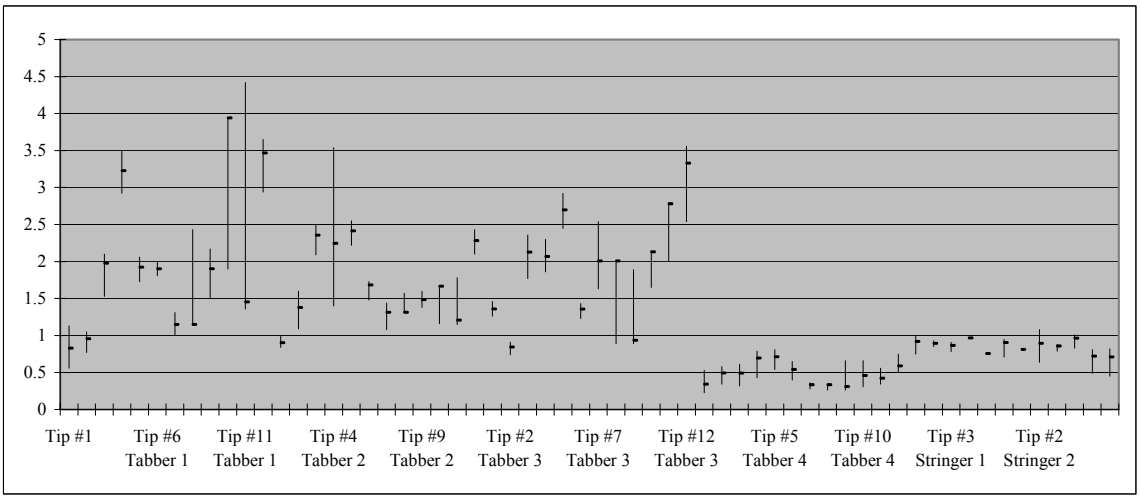


Figure 24: Force Applied by Hot Bar Tip While Making a Solder Bond

Structures to support the solar cell against the pressure of soldering have been incorporated into solar cell back pattern designs. Structures to support the previously assembled front interconnect ribbon during the solder assembly of tabbed solar cells into matrix strings have also been evaluated. Variations in the thickness of the soldered front interconnect has a significant (but small) effect on cell breakage in the stringer robots. Structures to cantilever the front ribbon unsupported result in high breakage. Structures to support the front ribbon only at points opposite stringer head pressure from the back are effective at reducing breakage.

Several groups of thinner cells have now been processed through the automated equipment in Frederick. In all cases the cells were 12.5 cm by 12.5 cm multicrystalline cells. The first group consisted of 200 μm thick solar cells. Of approximately 200 cells processed one was broken and 7 suffered edge chips. The broken one may be due to excess solder head pressure. The chips are more likely due to the handling

equipment, which we know must be modified for ultra-thin cells. The second group consisted of 175 μm thick cells. Out of 84 cells, none were broken and 2 suffered from edge chips. So it appears that the hot bar process can be applied to cells down to 175 μm in thickness.

Light Soldering

In this approach, light is used to heat the solder until it melts. This offers a non-contact method for making the solder bonds so there would be little or no pressure on the ultra-thin solar cell during the soldering process. We identified 3 vendors of light soldering equipment for solar cells and had each test BP Solar cells:

- GTI – Solders both sides at once; would not solder BP multicrystalline cells
- NPC – Solders both sides at once: soldered BP multicrystalline cells had poor adhesion
- ASCOR – Solders one side, then the other; soldered BP multicrystalline cells had good adhesion and passed qualification TC test (500 cycles).

A laboratory ASCOR light soldering unit has been ordered for experimentation with ultra-thin solar cells.

Conductive Adhesives

A second approach to reducing the stress of interconnection is to use conductive adhesives instead of soldering. We have looked at material from several vendors. The initial module performance is reasonable, matching the efficiency levels obtained using soldering. However, when small modules made with this process were subjected to qualification tests, they suffered significant power loss. The data is shown in Table 17. So after only 50 thermal cycles and 388 hours of damp heat 4 out of the 5 modules lost more power than the acceptance level of 5%.

Table 17: Environmental Testing of Conductive Adhesives

Test	P(Initial) (W)	P (Final) (W)	Change (%)
50 TC	**9.21**	**8.31**	**-9.8**
50 TC	**9.20**	**8.57**	**-6.8**
50 TC	**8.77**	**8.67**	**-1.1**
388 hr DH	**9.06**	**7.82**	**-13.7**
388 hr DH	**9.16**	**8.10**	**-11.6**

In the third year of the program we plan to evaluate conductive adhesives from several different vendors.

3.6.6 Modules with Ultra-thin Solar Cells

Module assembly of nominal 100 μm thick solar cells has been carried out on a laboratory scale at BP Solar under this contract. Modules have been made with multicrystalline silicon solar cells of 114mm x 114mm x 115 μm and with multicrystalline silicon solar cells of 125mm x 125mm x 115 μm. The module size in both cases was the conventional 36 (125mm x 125mm) cell size. The processing is described in the following sections.

Tabbing - Front interconnect ribbons of thickness 0.004 inch x width 0.070 inch width (the standard size for this module type) with lead free solder coating were soldered to the ultra thin cells by hand. The standard liquid flux used in production was utilized. For the first samples, hand soldering was used in order to evaluate soldering pressure, temperature, solder joint area, and sequence of solder joint position. Solder joints of small dimension were made intentionally to minimize stress on the ultra thin wafers. These dimensions were roughly equal to the solder joint dimensions of the front solder bonds made by the automated equipment on BP Solar commercial modules. In making each solder joint the silicon ultra-thin

cell was deflected or bowed in a concave fashion by the heat of soldering. Upon completion of five discrete solder joints on the length of both 125 mm cell front interconnects, the cell was warped about 3 mm. Occasional sounds of cracking of stressed silicon could be audibly detected as the soldered wafer cooled. This occurred for an estimated 2% or 3 % of the soldered solar cells. No evidence of damage could be detected on examination of these cells.

Stringing - Tabbed solar cells were arrayed in a composite material machined matrix jig to control string alignment and wafer spacing. Strings of 9 cells were made. Hand soldering as used for front tabbing as well as the same liquid flux were used for back stringing. The interconnect ribbons (previously applied to the front) were soldered to the back of the ultra-thin cells by hand. For the first samples hand soldering was used in order to evaluate the soldering pressure, temperature, solder joint area, and sequence of solder joint position. Solder joints of small dimension were made intentionally to minimize stress on the ultra thin wafers. These were roughly equal to the solder joint dimension of hand back soldering when done in production; however they are larger in area than the solder joints made by BP Solar production automation equipment. Four back solder joints were made on each of the ribbons.

Matrixing - Cells were arrayed in the matrixing jig with the back slightly convex; with finger pressure the tabbed cell was deflected flat into its alignment pocket and the interconnect ribbon was aligned and wet with flux. A solder joint was first made at the free end of the interconnect ribbon and subsequent joints were made moving toward the cell to be connected with. Again, as in front soldering there was a deflection of the finished soldered solar cell toward the concave position, with the result that the finished string was quite flat and free of bow. As the individual solar cells cooled after back soldering there was again some audible cracking in occasional cases.

Layup - Conventional BP385 module components were used for the construction of the module. Glass and EVA were prepared and the individual strings of ultra thin cells were picked up by hand at each end and lifted from the matrix jig and gently placed on the module layup. No breakage or cracking was detected during this process. Strings were aligned by hand and it was discovered that an error induced by hand at the matrix jig resulted in every other string bowing slightly toward the other. Strings, however did not touch and the error does not compromise the work.

Preassembled module bus bar sets from production were soldered in place into the end cells of the matrix using Teflon release paper to avoid damage to EVA. This soldering was done to the backs of those cells using the same tools and parameters as for stringing. There was no issue with this soldering, it was carried out as for back stringing with no breakage or signs of damage.

Conventional back EVA and special clear Tedlar backsheet (0.002 inch thick) were laid up on the assembled matrix without special precautions. The matrix remained quite flat as previously mentioned. The clear Tedlar was chosen to allow observation of the unusual grid back cell design and to allow defects (if present) to be observed.

Lamination - Lamination was carried out in a standard Spire clamshell laminator. The normal temperature for 36 cell modules with conventional cell thickness was used. A conventional lamination cycle of time and pressure was used. No damage was detected in the laminate after lamination and the pattern of interconnects and solder joints was normal.

Termination – The laminate was trimmed with a hot knife and electrical termination was performed using the conventional burn through technique. Two 12 gauge Multicontact cables were soldered to the bus bars to terminate the module. No diodes bypass were installed.

The laminate was electrically and mechanically tested before the junction box was installed. After framing a modified (top cut off to allow visual inspection) low profile junction box was installed using conventional material – an RTV adhesive and an epoxy pottant.

Framing – The module was framed in the normal manner using hot melt butyl and the standard cross section Al frame.

A back view of the completed module is shown in Figure 25. (The front looks like a standard module). The module was forward biased at 2 times short circuit current and inspected with the IR camera for cracks, hotspots and other signs of damage. An insignificant amount of damage was detected, similar in appearance to a module with conventional thickness solar cells. There were 2 or 3 cracked cells and a few minor hot spot solder joints, but nothing that would be considered a source of power loss or a potential source of future power loss. The measured output power of the module was low, but that was consistent with the quality of the cells used in it.

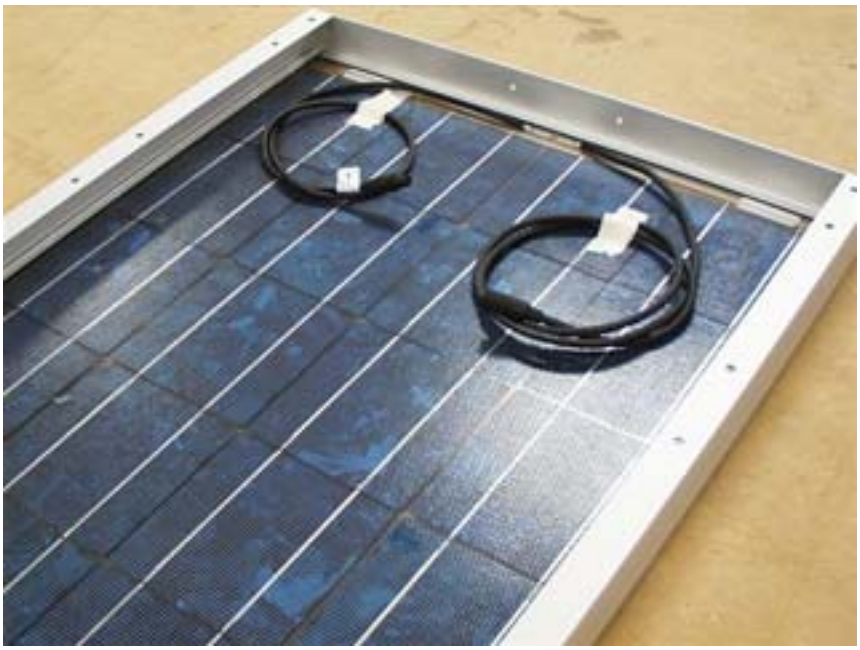


Figure 25: Back View of First Ultra-Thin Module

3.7 In-Line Process Control

In this task, BP Solar is incorporating active feedback from manufacturing processes into the in-line measurement system. BP Solar is working with the University of South Florida to develop a crack detection system.

3.7.1 Crack Detection

Wafer breakage during processing is a very high cost issue. This is particularly true when wafers fail during one of the print steps, generally resulting in several minutes of downtime while the operator cleans up the scattered parts and the wet paste. This is also a source of potential contamination. It is believed that wafers frequently fail at the print steps because they come into the process already cracked and the crack then fails when it is stressed during the process step. Wafer cracks can also cause electrical failure at cell or module test.

University of South Florida has been subcontracted to help in developing a system for crack detection. AT UCF they use the HS1000 HiSPEED™ Scanning Acoustic Microscope (SAM) by Sonix Inc. for surface morphology and structural (bulk) integrity evaluation. In SAM, a focused acoustic beam is scanned over the front and back surfaces of the wafer. The sound pulses are transmitted through the wafer and the reflection from the wafer interfaces is monitored. The ultrasonic pulses are generated by a high-frequency piezoelectric transducer. Electrical pulse from high voltage transmitter is converted to mechanical energy. This activation causes the transducer to vibrate at a specific frequency causing ultrasonic pulses to be transmitted from the transducer. These pulses travel through the material at the materials velocity and are reflected at the interfaces of the material it strikes. The ultrasonic energy does not travel well through air, so the wafers have to be placed in a coupling medium (deionized water bath). The system uses the pulse echo technique and operates at frequency up to 250 MHz. The pulses are repeated at the repetition rate of 20 KHz, so echoes from one pulse do not overlap those from the next. The returned echoes are received by the transducer and converted back to voltages. The voltage data is then sent to the receiver and is amplified and digitized (providing peak amplitude and phase).

The initial experiments were conducted with single crystal cells because a production yield problem with this cell type indicated that a significant fraction of these cells were susceptible to breakage. Figure 26 shows one of the cells as it was initially placed in the SAM system. The crack was initially ~1÷5mm in length, but it eventually propagated across the wafer leading to the wafer breakage, as shown in Figure 27. Figure 27 looks exactly like the IR image of the modules that incorporate these problem cells. The SAM system was able to see the small (micro-) crack Figure 26 that later lead to the break (Figure 27).

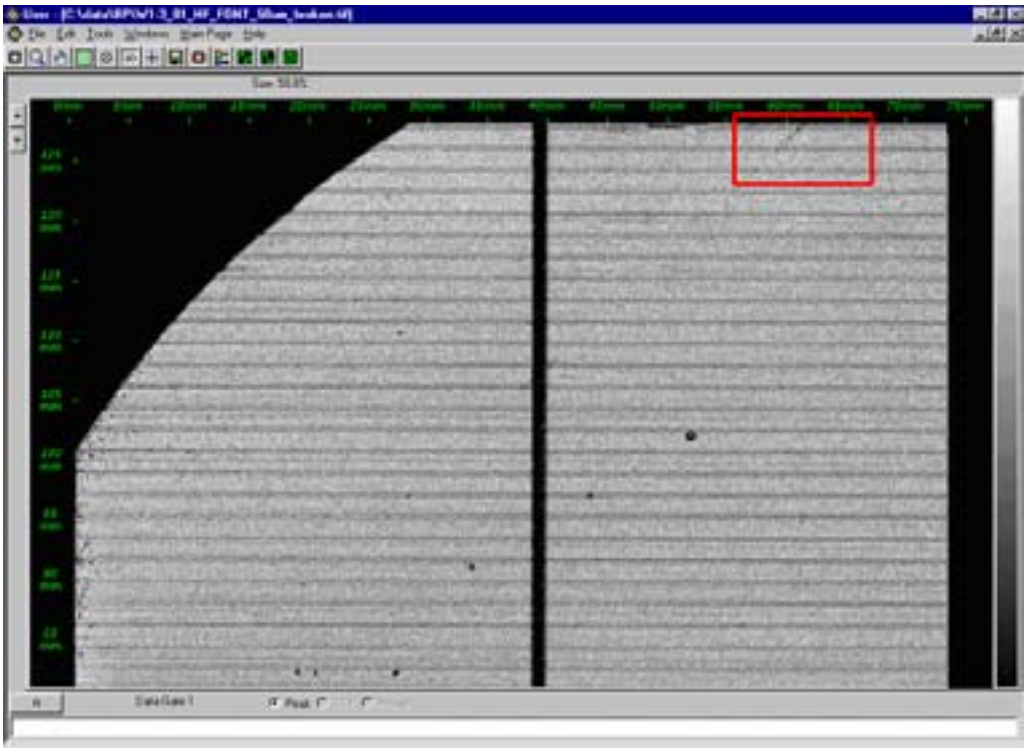


Figure 26: SAM image of the initial crack on the wafer captured in the red box

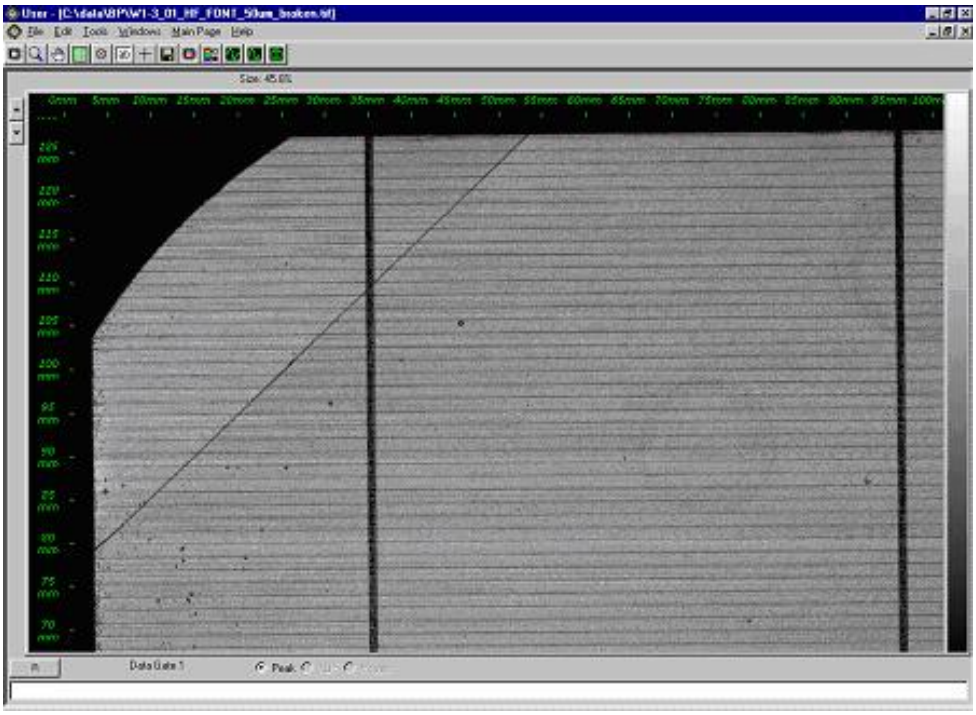


Figure 27: SAM image of the same area of the wafer as Figure 26 after stress. The initial crack had propagated across the wafer's corner causing it to break.

The SAM process was also able to identify internal cracks. An example is shown in Figure 28.

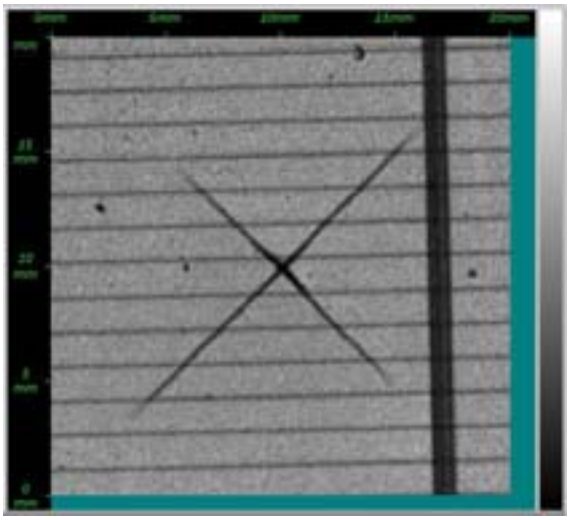


Figure 28: SAM image of STAR crack

BP Solar provided eight different sets of wafers to USF for scanning. The idea was to send wafers and partially processed cells in order to see if we could determine if one or several cell processes resulted in the formation of micro-cracks.

Each set initially contained 50 wafers. SAM mapping has been done on every single wafer from all eight sets. The wafers from first two sets were "as-delivered" wafers, but taken from different ingots. The wafers forming sets C through H are from various positions in the cell line. The results varied from zero

to 11 cracked or broken wafers/cells per group. SAM was an excellent research tool for determining which wafers are cracked. Specific lessons learned from this experiment are:

- Our wafer/cell packing was not adequate.
- There is a big difference in mechanical properties of wafers from different vendors.
- Several pieces of process equipment were identified as causing additional micro-cracks.
- The fewest micro-cracks were observed after laser grooving.
- Two groups of finished cells taken off of the line at different times, had significantly different numbers of cracks.

SAM has proven to be an accurate method for identifying cracks and micro-cracks in wafers and partially processed solar cells. In this case it provided BP Solar with information about where cracks and micro-cracks were first occurring and therefore has provide valuable information to assist in reducing breakage and increasing yield.

However, each SAM wafer measurement took 20 minutes for sample set-up and data collection. This is clearly not an inline production process. The data from this effort was very useful as the sample set evaluated by SAM can now be used to calibrate and verify the accuracy of any new methods developed for crack detection.

The next phase of the program will be to develop a rapid procedure using resonance ultrasonic vibrations to diagnose the mechanical quality of full-size Si wafers and solar cells

3.7.2 In-Line Measurements

Three specific areas have been selected for implementation of active feedback into the production line. The three areas will be discussed below.

Brick Measurements

As part of QA procedures to maintain overall dimensional control for our multicrystalline wafer product, prior to wafering, the bricks of silicon are measured for both lateral size and orthogonal skew. This procedure has been done manually in the past requiring substantial handling and movement of bricks to complete the series of measurements with digital calipers and squareness tool with a dial indicator. In an attempt to reduce handling to facilitate increased production volume and increased brick size (weight), an inline, single-station measurement tool was designed, constructed, and implemented in production.

The station utilizes five non-contact laser measurement heads, four long-range heads for dimensional check with a resolution of 10μm and a fifth for the orthogonal check with a resolution of 1μm. The heads are placed such that each measurement is opposed to a defining bearing surface that sets the zero surface. All five measurements are taken simultaneously and displayed at the proper precision to the operator on a readout panel. The display color has been set to display red for out of spec condition, yellow for marginal, and green for a pass condition. The displays are also capable of digital data output to allow for automatic data collection into our quality system. The system is shown in Figure 29.

Quantity of Dopant

One critical process parameter is the amount of phosphorous dopant deposited onto the wafer surface. Historically this has been measured and the data recorded manually. This process is being upgraded to make both the measurement and the recording of the data automatic.

Figure 29: Brick Measurement System

Diode Integrity

The standard flash test I-V curve will identify a shorted bypass diode. However, it will not tell whether the diode is operational nor whether it is actually electrically connected into the circuit. To determine if the diode is installed and working properly, BP Solar has implemented a dark reverse current measurement of every module type manufactured with a bypass diode. If the diodes are installed and operating correctly the reverse current will flow through them so the voltage drop will be minimal. If the diodes are not installed or operating correctly the reverse current will have to flow through the cells so there will be a much higher reverse voltage drop.

3.8 MegaPlant Design

In this task BP Solar is developing a 50 MW (annual nominal capacity) green-field MegaPlant factory model template based on a new thin polycrystalline silicon product line. This template shall include the fully integrated, very thin wafer, high efficiency processes developed in the other tasks of this program, and will be used for evaluating equipment and labor requirements as well as manufacturing costs.

ARRI is supporting BP Solar in this activity. The objective of the ARRI effort is to develop a decision support tool that will aid the economic justification of ultra-thin photovoltaic (PV) cell production. This decision support tool will consist of a discrete-event simulation model coupled with embedded activity-based costing mechanisms. This dynamic model of a PV module production facility encompasses the entire span of foundry operations, wafer cutting, cell production, and module assembly (figure 30). The immediate application of this tool will be to access the economic viability of shifting to ultra-thin cell production and module assembly. This technology shift will require a new class of continuous flow cell production technologies. It is also anticipated that cell breakage rates will increase as a result of the reduced thickness of the cell. The model will be used to construct activity-based cost predictions for conventional module production and the proposed ultra-thin cell technologies. Sensitivity models will also be constructed for the impact of cell breakage rates on product production costs.

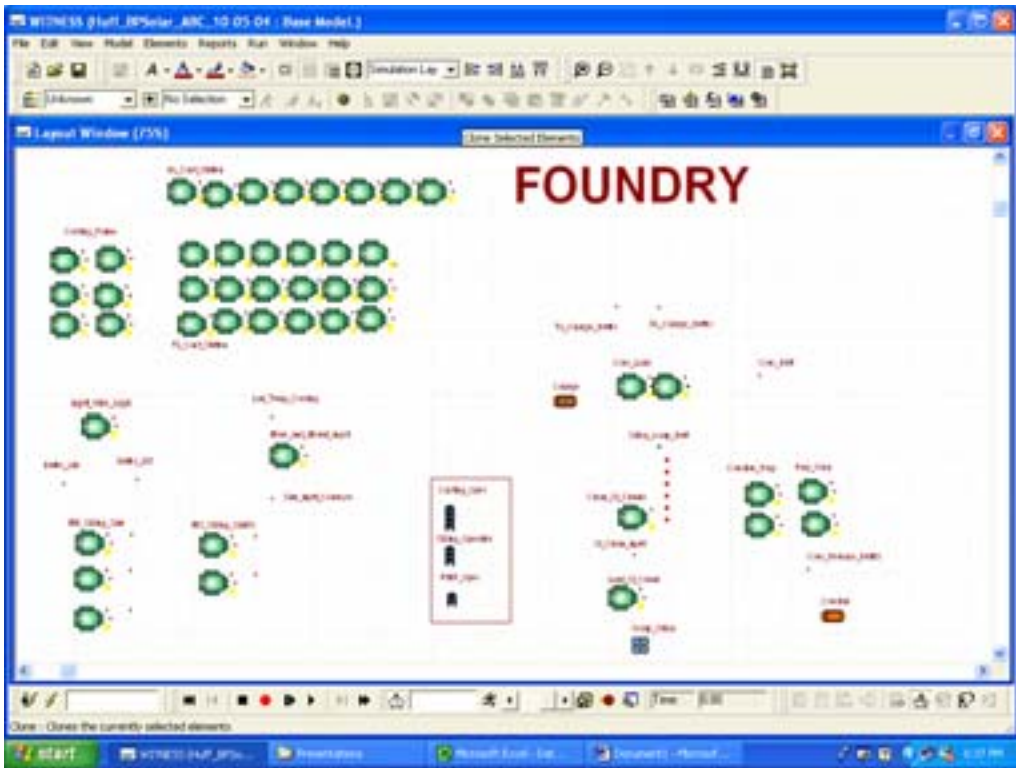


Figure 30: A section of the discrete-event simulation model depicting foundry operations

A secondary objective was to develop a maintainable tool that can be used with minimal knowledge of discrete-event simulation and proprietary simulation software languages. This will be accomplished by providing a front end spreadsheet for the model which can be maintained by BP Solar Personnel. Under this strategy, the internal structure of the model is specific to a given production facility but system resource levels, cycle times, and unit resource costs can be specified through a series of worksheets (figure 31).

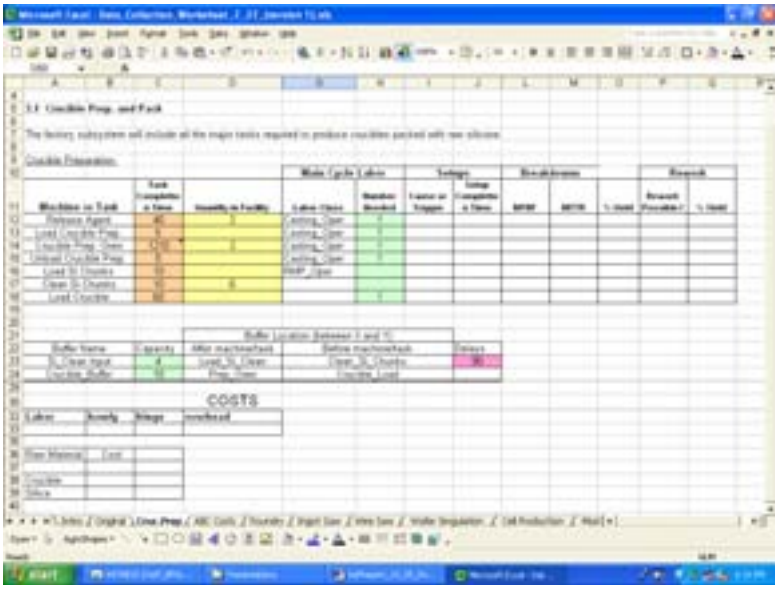


Figure 31: Example Data Entry Worksheet

A multi-phase plan has been adopted for this effort. The following activities outline the steps that are being followed:

- Define model objectives and requirements
- Understand current operations and collect model input data.
- Define a conceptual modeling approach.
- Construct an "As-Is" simulation model of current PV production activities.
- Verify and validate the performance of the "As-Is" model.
- Use the model to predict current module production costs.
- Access the tool's ease of use and maintainability.
- Understand and model the proposed "To-Be" ultra-thin cell production methods.
- Construct a "To-Be" simulation model of the ultra-thin cell production methods.
- Verify and validate the performance of the "To-Be" model.
- Predict ultra-thin cell product costs and perform yield cost sensitivity analysis.
- Use the tool to support economic justification of ultra-thin cell production technologies.
- Maintain the tool for additional analysis activities.

These tasks will generally be performed in the order listed above although iterations through the process steps may be required as the development of the modeling tool advances. This is particularly true for the model construction and verification tasks where the facility models will be built and tested in an iterative process.

Currently the base functional model of the "As-Is" production operations is being completed. Labor resource constraints and a credible PV Module Production Demand Generator still need to be added to this model. Once the base model is complete, we will verify that the model's performance is consistent with the current BP Solar Frederick Facility production levels.

A data entry worksheet has been constructed and it has been verified that it can be used to drive the simulation model. After the base functional model provides consistent the activity-based costing constructs will be added that will allow us to predict the production cost of the various PV module components throughout their manufacturing cycle.

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630 Solarex Court
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14. ABSTRACT *(Maximum 200 Words)*

The major objectives of this program are to continue the advancement of BP Solar polycrystalline silicon manufacturing technology. The program includes work in the following areas: Efforts in the casting area to increase ingot size, improve ingot material quality, and improve handling of silicon feedstock as it is loaded into the casting stations; developing wire saws to slice 100-μm-thick silicon wafers on 290-μm centers; developing equipment for demounting and subsequent handling of very thin silicon wafers; developing cell processes using 100-μm-thick silicon wafers that produce encapsulated cells with efficiencies of at least 15.4% at an overall yield exceeding 95%; expanding existing in-line manufacturing data reporting systems to provide active process control; establishing a 50-MW (annual nominal capacity) green-field Mega-plant factory model template based on this new thin polycrystalline silicon technology; facilitating an increase in the silicon feedstock industry's production capacity for lower-cost solar-grade silicon feedstock.

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