

# **Experiments Involving Correlations Between CdTe Solar Cell Fabrication History and Intrinsic Device Stability**

D. Albin, T. McMahon, T. Berniard, J. Pankow,  
and R. Noufi  
*National Renewable Energy Laboratory*

S. Demtsu  
*Colorado State University*

*Prepared for the 31<sup>st</sup> IEEE Photovoltaics Specialists  
Conference and Exhibition  
Lake Buena Vista, Florida  
January 3–7, 2005*



**NREL**

**National Renewable Energy Laboratory**  
1617 Cole Boulevard, Golden, Colorado 80401-3393  
303-275-3000 • [www.nrel.gov](http://www.nrel.gov)

Operated for the U.S. Department of Energy  
Office of Energy Efficiency and Renewable Energy  
by Midwest Research Institute • Battelle

Contract No. DE-AC36-99-GO10337

## NOTICE

The submitted manuscript has been offered by an employee of the Midwest Research Institute (MRI), a contractor of the US Government under Contract No. DE-AC36-99GO10337. Accordingly, the US Government and MRI retain a nonexclusive royalty-free license to publish or reproduce the published form of this contribution, or allow others to do so, for US Government purposes.

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Available electronically at <http://www.osti.gov/bridge>

Available for a processing fee to U.S. Department of Energy and its contractors, in paper, from:

U.S. Department of Energy  
Office of Scientific and Technical Information  
P.O. Box 62  
Oak Ridge, TN 37831-0062  
phone: 865.576.8401  
fax: 865.576.5728  
email: <mailto:reports@adonis.osti.gov>

Available for sale to the public, in paper, from:

U.S. Department of Commerce  
National Technical Information Service  
5285 Port Royal Road  
Springfield, VA 22161  
phone: 800.553.6847  
fax: 703.605.6900  
email: [orders@ntis.fedworld.gov](mailto:orders@ntis.fedworld.gov)  
online ordering: <http://www.ntis.gov/ordering.htm>



# Experiments Involving Correlations Between CdTe Solar Cell Fabrication History and Intrinsic Device Stability

David Albin<sup>1</sup>, Tom McMahon<sup>1</sup>, Tracie Bernard<sup>1</sup>, Joel Pankow<sup>1</sup>, Samuel Demtsu<sup>2</sup>, and Rommel Noufi<sup>1</sup>

<sup>1</sup>National Renewable Energy Laboratory, Golden, CO 80401

<sup>2</sup>Colorado State University, Fort Collins, CO 80523

## ABSTRACT

An orthogonal full-factorial design was used to study the effect of CdS and CdTe layer thickness, oxygen ambient during vapor CdCl<sub>2</sub> (VCC) and the use of nitric-phosphoric (NP) acid as a pre-contact etch on the initial and stressed performance of CdS/CdTe small-area devices. The best initial device efficiency (using thinner CdS, thicker CdTe, no oxygen during VCC, and NP etch) also showed poor stability. Increasing the CdS thickness significantly improved stability with only a slight decrease in resulting initial performance. All devices used a thin margin of CdTe around the perimeter of the backcontact that was shown to significantly reduce catastrophic degradation and improve overall test statistics. The latter degradation is modeled by the formation of a weak-diode/low shunt resistance localized near the edge of finished devices. This shunting is believed to occur through the CdS/CdTe interface, rather than along the device edge, and is exacerbated by thinner CdS films.

## INTRODUCTION

The success of photovoltaics as a viable source of renewable energy will be achieved by balancing performance, cost, and reliability. To date, much of the current knowledge regarding polycrystalline thin film devices has focused on optimizing initial performance. In this work, we present empirical optimization experiments specifically designed to study the balance between performance and stability.

### Device Fabrication

The technique used to fabricate CdS/CdTe devices have been previously described [1]. The basic structure is that of a superstrate design in which light passes through a transparent glass/tin-oxide superstrate, where it is then absorbed in the n-(CdS)/p-(CdTe) heterojunction structure. For this study, the chemical-bath deposited CdS layer thickness was varied by adjusting the time of growth (3 levels; 34, 37, and 41 m; corresponding to approximate film thicknesses of 60, 80, and 100 nm). The close-spaced sublimated (CSS) CdTe thickness was similarly controlled using deposition time (2 levels; 8 and 11  $\mu$ m). After the CdTe deposition, the finished structure was subjected to VCC at 400 °C in a oxygen/helium ambient (2 levels; 0 torr O<sub>2</sub>/500 torr He and 100 torr O<sub>2</sub>/400 torr He).

Prior to the backcontact step, CdTe surfaces are typically treated with a NP etch in order to promote the formation of a Te-rich layer and to remove surface oxides [2,3]. In this study, devices were made with and without this pre-contact etch. Backcontact fabrication concluded with application of a relatively thick layer (~50 – 100  $\mu$ m) of graphite paste containing Cu<sub>x</sub>Te and HgTe dopants followed by a similarly thick, final conducting layer of Ag paste. A narrow (~1 mm) margin of CdTe surrounding the perimeter of the dopant/Ag paste contact was used. This feature was previously reported by use to drastically reduce edge leakage and shunting [4]. In addition, such a structure also improves stress data repeatability results among similarly processed devices by reducing statistically sporadic nature of shunting.

### Experimental Set-up

A 3x2x2 full factorial experimental design was used for this study. This design allows for screening both main as well as interaction effects between process variables. Each of the 24 experimental points was replicated twice by defining two devices per substrate resulting in 48 individual cells. Multiple linear regression models for open-circuit voltage ( $V_{oc}$ ) in volts, short-circuit current density ( $J_{sc}$ ) in mA/cm<sup>2</sup>, fill-factor (%FF), and efficiency ( $\eta$ %) after initial fabrication and after stress testing were generated from these orthogonal designs and subsequently compared with actual data using simple residual analysis.

Accelerated stress testing consisted of heating cells uniformly to a temperature of 100°C while illuminating them through the glass side with a solar-matched spectrum (filtered Xenon source) at one-sun irradiance. Devices were allowed to naturally bias themselves at open-circuit voltage. Devices were placed within machined aluminum holders that were heated from below using a Cu-heat riser placed on a regulated hot plate. Uniformity among all samples was measured using embedded thermocouples and determined to be  $\pm 5^\circ\text{C}$  during the course of the test.

Current density-voltage (JV) measurements were performed under both dark and illuminated (calibrated 1-sun) conditions. Transients were reduced in light-soaked (stressed) samples by storing devices in the dark for 12-24 hrs at 25°C prior to JV scans. Stress measurements were made after light soaking for 4.25, 30, 119, 195, 408, and 693 hrs.

## EXPERIMENTAL RESULTS

Multiple linear regression models were generated from the orthogonal experiments using the SAS software package JMP. Regressions were performed using datasets corresponding to unstressed, and stressed (stress time = 693 hrs) devices. The regression models for the unstressed devices were extremely well correlated with actual performance data. Figure 1 shows the correlation between actual and predicted device  $V_{oc}$  and a residual plot as a function of sample run.

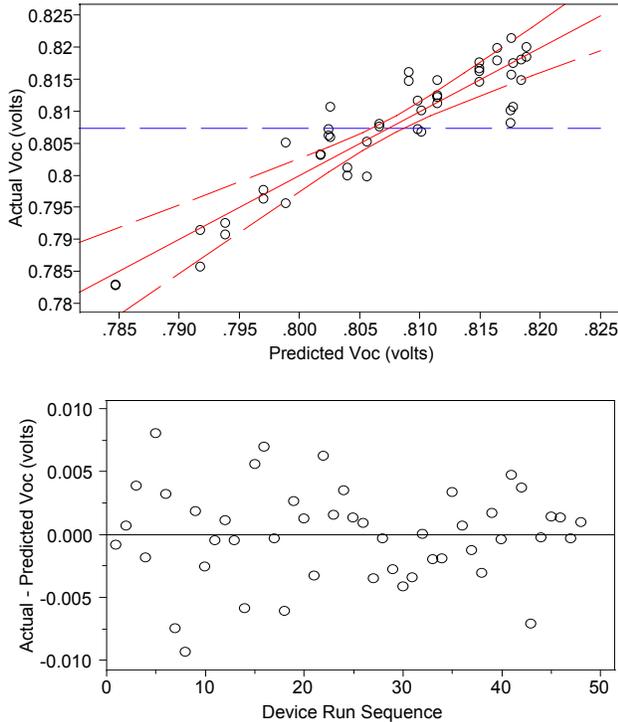


Fig. 1. Top Figure shows correlation between regression model predicted and actual  $V_{oc}$ . Dashed lines show 95% confidence intervals for the mean of the effect. Bottom figure shows residuals (Actual – Predicted values) vs. device run sequence.

Due to the necessity of using a single CdS film for 8 CdTe devices, total randomization of experimental points was not possible. Rather, devices were fabricated in the sequence of using ever-thicker CdS films. The residual plot above shows that the accuracy of the model improved as CdS film thickness increased (higher run sequence). This characteristic was also observed for the stressed dataset correlations.

The magnitude variation in residuals among  $V_{oc}$ ,  $J_{sc}$ , FF, and  $\eta\%$  for the unstressed data was less than  $\pm 10$  mV,  $1 \text{ mA/cm}^2$ , 3%, and 1% respectively. In addition, reproducibility among replicated devices was also measured and found to be surprisingly good.

Process interactions were studied within the context of the regression models for unstressed devices. When NP etch was used, the highest efficiency devices were made using the thinnest CdS, thickest CdTe, and zero

oxygen during the VCC process. At these process combinations, the predicted and actual  $V_{oc}/J_{sc}/FF/\eta\%$  values were 0.819/23.2/67.9/12.9 and 0.819/23.3/68.6/13.1 respectively. When NP etch was absent, the highest initial efficiency devices also used the same processing combination. The predicted and actual parameters in this case were again in excellent agreement, 0.810/22.97/59.2/11.0 and 0.809/23.2/58.9/11.1 respectively. In both NP and non-etched devices, the oxygen level present during the VCC process affects the sensitivity of the process to variations in CdS window layer thickness. As oxygen is reduced, the performance of devices became less sensitive to variations in the CdS window layer thickness.

Regression models of the stressed cells after 693 hrs of light soak at  $100^\circ\text{C}$  were not as well-correlated as the initial performance datasets but were nevertheless adequate for data interpretation. Table 1 presents the actual degradation data (showing mean %Change in Efficiency) sorted from least to most degradation as a function of the 24 experimental processing variations. Also shown in this table is the corresponding mean initial device efficiency. For the most stable cells, degradation values effectively represent stabilized levels, i.e., cells optimized for stability approach an asymptotic level beyond which appreciable degradation no longer occurs.

CdS Thk	CdTe Thk	VCC Ambient	Etch	Initial Eff(%)	%Change Efficiency
41	11	0	NP	12.50	-8.36
34	11	100	NP	12.52	-9.05
37	11	0	NP	12.40	-9.11
41	11	100	NP	11.88	-9.75
37	8	100	NP	12.46	-10.52
37	11	100	NP	11.87	-10.59
41	8	100	NP	10.90	-11.16
34	8	100	NP	11.47	-11.45
37	8	0	NP	12.25	-11.65
41	8	100	none	10.02	-25.19
41	8	0	none	9.88	-28.92
41	8	0	NP	12.02	-32.23
34	8	0	none	10.47	-34.66
41	11	100	none	10.50	-35.14
34	8	100	none	11.18	-35.57
41	11	0	none	10.67	-35.83
37	11	0	none	11.10	-37.13
37	8	0	none	10.08	-37.48
37	11	100	none	10.60	-38.41
34	8	0	NP	12.07	-42.68
37	8	100	none	10.84	-45.02
34	11	0	none	11.06	-61.76
34	11	100	none	10.68	-64.18
34	11	0	NP	13.07	-87.03

Table 1. Degradation Data Measured at  $t = 693$  hrs.

Statistically, the best reproducibility among replicated pair devices was observed when the CdTe film was thicker, and particularly, when NP was used. As the CdTe thickness decreased, reproducibility was not as good. For

the thick CdTe case with NP, the combination of thin CdS and no  $O_2$  during the VCC process resulted in the worst stability of all devices (mean degradation of  $-87\%$ ). When  $O_2$  was introduced, the stability improved considerably (up to  $-9.0\%$  mean degradation). The benefit of using  $O_2$  during VCC for thin CdS devices is shown in Figure 2(a). This behavior was also observed in the case when NP was absent though it was not as strong. As shown in Figure 2(b), the reproducibility in degradation for thin CdS devices (both with and without  $O_2$  during VCC) was not as good as shown for the NP etched examples in Figure 2(a). As shown in both figures, when the CdS is thickest (the heavy lines), stability was determined primarily by whether the CdTe was etched or not. With NP etch, degradation approaches the asymptotic stabilized level more rapidly. The amount of oxygen used during the VCC process for thick CdS devices had little impact on stability.

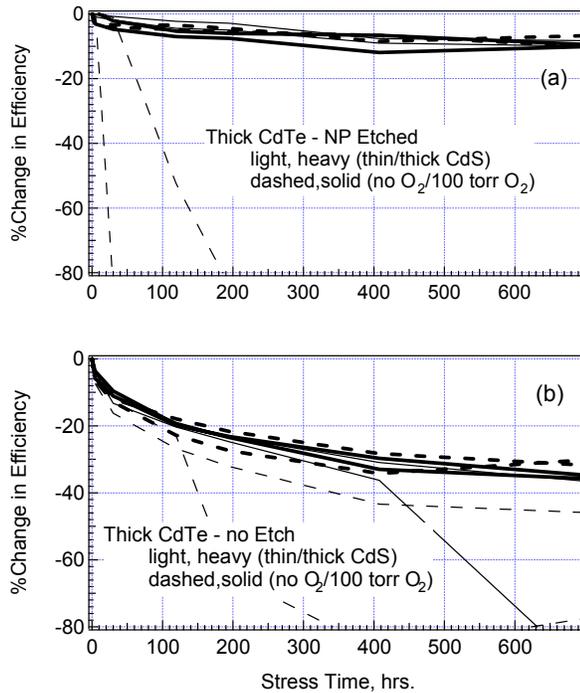


Fig. 2. Stability of thick CdTe devices with (a) and without (b) NP etch

Comparing the unstressed and stressed datasets resulted in an interesting observation. The highest initial efficiency (actual and predicted) yielded the least stable device. However, by increasing the CdS thickness from 60 nm to 100 nm, a significant improvement in stability was obtained with only a slight drop in performance. The predicted efficiency at  $t=0$  was observed to drop to only 12.63% (actual mean level of 12.5%). The corresponding degradation improved to a modeled level of  $-11.8\%$  (actual mean level of  $-8.4\%$ ).

The major impediment to correlating processing with stability was the tendency for identically processed devices to suddenly exhibit large variations in degradation rate. This behavior was due to a significant increase in shunting. During earlier experiments, such behavior was com-

monplace. For example, Figure 3 shows how such an effect can rapidly destroy the statistical significance of stress testing. In this subset, 14 out of 48 devices (indicated by the X's) showed this type of "catastrophic" degradation within the first 1000 hrs of stress testing (nearly a 30% occurrence rate).

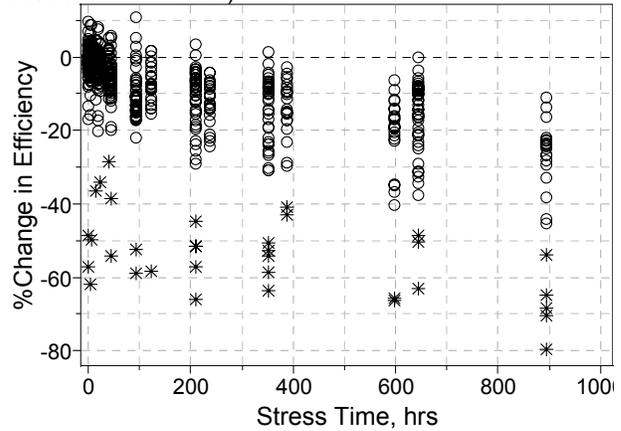


Fig. 3. Early degradation rate data plagued by high incidence of shunt-related defects.

In these early devices, the edge was defined by cutting perpendicularly through the backcontact pastes to the tin-oxide front contact using a razor blade. This approach favors the physical contact between these layers which are only separated by the active-layer film thickness of  $\sim 8\text{-}10$   $\mu\text{m}$ . Such a "non-margined" structure was recently shown to favor leakage currents [4]. By introducing a thin ( $\sim 1$  mm) margin of CdTe around the perimeter of the backcontact we were able to effectively increase the potential shunting path length by a factor of 100. With this modification, shunting was reduced significantly. A plot similar to Figure 3, but using the new "margined" cell structure shows only 7 such failures out of a sample of 66 devices. Of these 7 cells, 6 used thin CdS (not a process variable for the set shown in Figure 3).

Visual examination of the backcontact definition for these 7 devices revealed regions where the metal paste had visibly extended over the edge of the dag+ dopant paste and was in direct contact with the CdTe surface *but not the tin-oxide front contact* (these extensions were still margined). Auger electron spectroscopy analysis of the CdTe surface between these protrusions and the actual CdS/CdTe device edge did not detect any Ag eliminating possible surface migration as the reason for shunting. These results, as well as the observation that 6 of the 7 devices used thin, 60 nm CdS (the one exception using 80 nm CdS) strongly suggests shunting has occurred perpendicularly through the device, rather than simply down the CdS/CdTe edge. Previously, metal atom chains were used to make switchable memory devices in a-Si [5]. Recently, the concept of such chains as a breakdown mechanism in thin-film device junctions was proposed by Karpov, et al. [6]. According to this model, the energy barrier for homogeneous shunt nucleation across a dielectric layer like CBD CdS should decrease linearly with decreasing layer thickness. This may be the reason why our thin CdS devices fail with stress testing.

Infrared imaging of degraded but margined devices using thin CdS were used to study catastrophic shunting observed during stress testing. Figure 4 was recorded at 1.2 volts forward-bias (6.0 mA) and clearly shows the presence of bright spots distributed both within the cell interior as well as at the bottom right corner. These bright spots are believed to be due to either local variations in emissivity or, more interestingly, the evolution of heat associated with either resistive or diode recombination processes. Such spots have also been observed in reverse-bias, where diode recombination current joule loss is not expected.

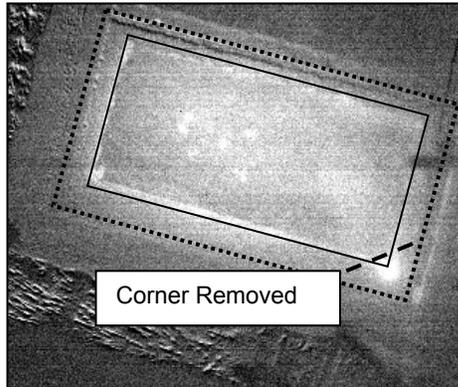


Fig. 4. Infrared Image of a Shunted Device. Dashed line indicates the approximate boundary of the CdTe margin.

The corner bright spot is the location of one of the before-mentioned overlaps of the Ag backcontact directly on the CdTe surface. When this area is physically removed (re-defined), most of the initial cell performance is recovered. The experimental JV curves corresponding to the unstressed, stressed, and re-defined cell are shown as the open circles in Figure 5. The performance of this cell initially, after degradation, and after redefinition was 13.1%, 1.3%, and 11.6% respectively.

A 10-diode Pspice model with the ability to adjust diode quality factor  $A$ , reverse-saturation current density  $J_0$  ( $\text{mA}/\text{cm}^2$ ), and series,  $R_s$ , and shunt,  $R_{sh}$ , resistance ( $\text{ohms}\cdot\text{cm}^2$ ) was used to simulate the observed experimental data (Figure 5)

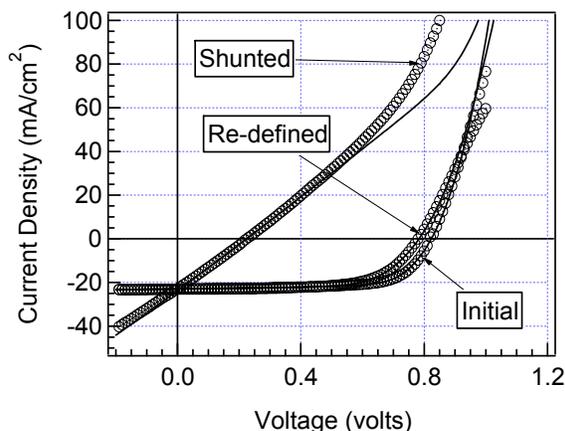


Fig. 5 Initial, stressed (shunted), and redefined J-V data for the device shown in Figure 4.

Such series-distributed diode models generate more physically sensible values for  $J_0$  and  $A$  relative to models that utilize single, "lumped circuit" equivalents and allow for modeling spatially localized variations in device characteristics. The simulation fits are shown as the solid lines in Figure 5. The 10-diode fit for the initial case was made using  $J_0 = 1.2\text{e-}11$ ,  $A = 1.72$ ,  $R_{sh} = 5\text{K}$ , and  $R_s = 0.5$ . The shunted case was modeled as a single highly shunted, "weak-diode" with  $J_0=1\text{e-}02$ ,  $A=1.8$ ,  $R_s=0.5$ , and  $R_{sh}=0.5$  in parallel with 9 slightly weakened diodes with  $J_0=1\text{e-}10$ ,  $A=1.8$ ,  $R_s=0.95$ , and  $R_{sh}=5\text{K}$ . By removing the single "weak diode" (e.g., leaving only 9 slightly weakened diodes), the simulation easily fit the re-defined experimental data shown in Figure 5.

## CONCLUDING REMARKS

The slight gain in initial performance associated with using the thinnest CdS films (~60 nm) was more than negated by significant problems with stability as measured by open-circuit, 100 °C light-soak stress testing. Stability problems with thin CdS films were attributed to the formation of weak-diodes and shunting through the CdS/CdTe interface rather than along the cell edge. Such behavior may be verification of the thickness-dependent shunt nucleation model proposed by Karpov, et al [5]. Process variations, in this case, the use of oxygen during the VCC step and thicker CdTe allowed for the use of thinner CdS.

## ACKNOWLEDGEMENTS

We acknowledge the support of the U.S. Department of Energy under Contract No. DE-AC36-99G010337.

## REFERENCES

1. D. Rose, D.F. Hasoon, R. Dhere, D. Albin, R. Ribelin, X. Li, Y. Mahathongdy, T. Gessert, P. Sheldon, "Fabrication procedures and process sensitivities for CdS/CdTe solar cells," *Prog. Photovolt: Res. Appl.* 1999; **7**: 331-340.
2. D. Levi, D. Albin, and D. King, "Influence of Surface Composition on Back-contact Performance in CdTe/CdS PV Devices," *Prog. Photovolt: Res. Appl.* 2000; **8**: 591-602.
3. D. Albin, D. Levi, S. Asher, A. Balcioğlu, and R. Dhere, "Precontact Surface Chemistry Affects on CdS/CdTe Solar Cell Performance and Stability," *28th IEEE PVSC*, 583 (2000).
4. T.J. McMahon, T.J. Bernard, and D.S. Albin, "Non-linear Shunt Paths in Thin-Film CdTe Solar Cells", accepted and to be published in *J. Appl. Phys.*
5. P.G. LeComber, A.E. Owne, W.E. Spear, J. Hajto, A.J. Snell, W.K. Choi, M.J. Rose and S. Reynolds, "The switching mechanism in amorphous silicon junctions," *J. Non-Cryst. Sol.* **77 & 78**, 1373 (1985).
6. V.G. Karpov, D. Shvydka, and Y. Roussillon, "E<sup>2</sup> phase transition: Thin-film breakdown and Schottky-barrier suppression", *Phys. Rev. B*, **70**, 155332 (2004).

# REPORT DOCUMENTATION PAGE

*Form Approved*  
OMB No. 0704-0188

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Executive Services and Communications Directorate (0704-0188). Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

**PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ORGANIZATION.**

<b>1. REPORT DATE (DD-MM-YYYY)</b> February 2005		<b>2. REPORT TYPE</b> Conference Paper		<b>3. DATES COVERED (From - To)</b> 3-7 January 2005		
<b>4. TITLE AND SUBTITLE</b> Experiments Involving Correlations Between CdTe Solar Cell Fabrication History and Intrinsic Device Stability				<b>5a. CONTRACT NUMBER</b> DE-AC36-99-GO10337		
				<b>5b. GRANT NUMBER</b>		
				<b>5c. PROGRAM ELEMENT NUMBER</b>		
<b>6. AUTHOR(S)</b> D. Albin, T. McMahan, T. Berniard, J. Pankow, S. Demtsu, and R. Noufi				<b>5d. PROJECT NUMBER</b> NREL/CP-520-37426		
				<b>5e. TASK NUMBER</b> PVA54301		
				<b>5f. WORK UNIT NUMBER</b>		
<b>7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)</b> National Renewable Energy Laboratory 1617 Cole Blvd. Golden, CO 80401-3393				<b>8. PERFORMING ORGANIZATION REPORT NUMBER</b> NREL/CP-520-37426		
<b>9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)</b>				<b>10. SPONSOR/MONITOR'S ACRONYM(S)</b> NREL		
				<b>11. SPONSORING/MONITORING AGENCY REPORT NUMBER</b>		
<b>12. DISTRIBUTION AVAILABILITY STATEMENT</b> National Technical Information Service U.S. Department of Commerce 5285 Port Royal Road Springfield, VA 22161						
<b>13. SUPPLEMENTARY NOTES</b>						
<b>14. ABSTRACT (Maximum 200 Words)</b> An orthogonal full-factorial design was used to study the effect of CdS and CdTe layer thickness, oxygen ambient during vapor CdCl <sub>2</sub> (VCC) and the use of nitric-phosphoric (NP) acid as a pre-contact etch on the initial and stressed performance of CdS/CdTe small-area devices. The best initial device efficiency (using thinner CdS, thicker CdTe, no oxygen during VCC, and NP etch) also showed poor stability. Increasing the CdS thickness significantly improved stability with only a slight decrease in resulting initial performance. All devices used a thin margin of CdTe around the perimeter of the backcontact that was shown to significantly reduce catastrophic degradation and improve overall test statistics. The latter degradation is modeled by the formation of a weak-diode/low shunt resistance localized near the edge of finished devices. This shunting is believed to occur through the CdS/CdTe interface, rather than along the device edge, and is exacerbated by thinner CdS films.						
<b>15. SUBJECT TERMS</b> PV; layer thickness; intrinsic device stability; solar cells; fabrication history; nitric-phosphoric (NP); small-area; backcontact;						
<b>16. SECURITY CLASSIFICATION OF:</b>			<b>17. LIMITATION OF ABSTRACT</b>  UL	<b>18. NUMBER OF PAGES</b>	<b>19a. NAME OF RESPONSIBLE PERSON</b>	
<b>a. REPORT</b> Unclassified	<b>b. ABSTRACT</b> Unclassified	<b>c. THIS PAGE</b> Unclassified			<b>19b. TELEPHONE NUMBER (Include area code)</b>	