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Advances in the In-House CdTe Research Activities at NREL

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Advances in the In-House CdTe Research Activities at NREL

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ABSTRACT

NREL in-house CdTe research activities have impacted a broad range of recent program priorities. Studies aimed at industrially relevant applications have produced new materials and processes that enhance the performance of devices based on commercial materials (e.g., soda-lime glass, SnO_2:F). Preliminary tests of the effectiveness of these novel components using large-scale processes have been encouraging. Similarly, electro- and nano-probe techniques have been developed and used to study the evolution and function of CdTe grain boundaries. Finally, cathodoluminescence (CL) and photoluminescence (PL) studies on single-crystal samples have yielded improved understanding of how various processes may combine to produce important defects in CdTe films.

1. Objectives

In-house CdTe device research at NREL addresses a broad range of issues important to the Solar Energy Technologies Program [1]. These range from developing novel processing alternatives for industry to understanding causes and evolution of major defect species in CdTe thin-film material.

2. Technical Approach

This paper highlights three different study areas presently ongoing within the NREL CdTe device activity. The first area investigates the use of soda-lime glass in conjunction with the novel processes used to produce NREL's world-record-efficiency CdS/CdTe devices. The second area involves the use of conductive atomic-force microscopy (C-AFM) and near-field scanning optical microscopy (NSOM) to study grain-boundary delineation during pre-contact chemical surface treatments, and the effects of grain boundaries on photocurrent collection, respectively. The third investigation area studies evolution of luminescence spectra within typical CdS/CdTe devices, as well as resulting from controlled diffusion of likely contact species.

3. Results and Accomplishments

Studies of CdS/CdTe device fabrication on soda-lime glass substrates have used commercial SnO_2-coated substrates (e.g., Tec. 15 or Asahi with texture). After cleaning, these are sputter coated with a zinc-tin-oxide buffer layer and an oxygenated nanocrystalline CdS layer (CdS:O). Both layers are deposited at room temperature using r.f. magnetron sputtering. Further details are provided elsewhere [2]. Table 1 shows that performance of devices produced on these substrates is 14% or higher. The reasons for this high performance are attributed to a combination of benefits from incorporation of the ZTO and CdS:O layers. These include: enhanced ability to optimize $CdCl_2$ treatment due to improved sub-layer adhesion, reduced diffusion of Te into CdS:O compared to polycrystalline CdS, the ability to use a thinner CdS layer without open circuit voltage (V_{oc}) loss, and reduced shunting through CdS layer.

Table 1. NREL CdS/CdTe Devices on Soda-Lime Glass

Cell #	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Effic. (%)	Area (cm^2)
1*	829	23.4	72.5	14.0	1.001
2*	829	23.5	74.1	14.4	0.923
3*	831	23.3	72.2	14.0	1.027
4*	823	23.2	74.3	14.2	0.917
5*	830	23.4	73.7	14.2	1.062
6**	821	23.3	73.9	14.1	1.298

NREL confirmed total area measurements.
* Cells deposited onto Tec. 15 glass.
**Cell deposited onto Asahi-coated glass.

Potential industrial impacts embodied by these small-area device demonstrations include the production of modules with efficiency of >12%. Therefore, efforts have proceeded rapidly to transfer these technologies to our main industrial partner. Transfer activities have included numerous visits, transfer of sputtering-target recipes and quality criteria, and characterization of materials produced outside of NREL based on NREL processes.

Studies using nano-probe techniques have investigated the result of pre-contact chemical treatments, as well as helped determine the relative extent of intragrain vs. grain-boundary photocurrent generation. Figure 1 shows the topography (AFM) and corresponding conductive atomic-force microscopy (C-AFM) images of the surface of a CdTe/CdS solar cell following a bromine/methanol etch. The brighter areas in the right image indicate that higher conductivity grain boundary regions result from preferential etching. In contrast, nitric-phosphoric acid etching creates a conductive layer across the entire surface [3].

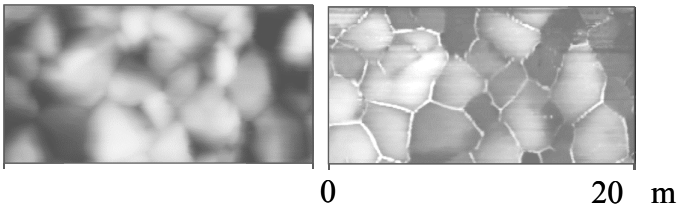

Figure 1. Left: Topographic AFM image of a CdTe film after $CdCl_2$ treatment and bromine etch. Right: Simultaneously acquired C-AFM image showing enhanced grain-boundary conductivity.

The C-AFM analysis suggests that grain boundaries near the back contact could reduce total contact resistance by effectively increasing the contact area. However, the analysis does not indicate how grain boundaries could effect photocurrent generation. To investigate this, a novel application of NSOM has been used to examine nano-scale variations of photocurrent generation/collection in an actual working device [4]. In this technique, a very small spot of 635-nm light is scanned through the ZnTe:Cu layer of a CdS/CdTe/ZnTe:Cu/Ti device that has been prepared with the following considerations: First, studies have shown that depletion in a CdS/CdTe device can be controlled by the amount of Cu diffusion from a ZnTe:Cu contact [5]. Specifically, thin layers of ZnTe:Cu yield a device with the entire CdTe layer depleted. These completely depleted devices do not demonstrate high-performance because, for typical CdTe thicknesses of ~3-5 µm, inadequate Cu diffusion results in an CdTe acceptor concentration too low for high V_{oc}, and the electric field is too small for high current. However, completely depleted devices have the attribute that carriers generated at the back during backside illumination can be collected. The second consideration is to photolithographically define small holes through the Ti outer metallization while retaining the ZnTe:Cu layer.

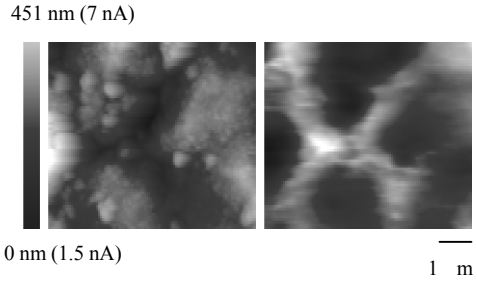

Figure 2. Left: AFM image of polycrystalline CdTe/CdTe/ZnTe:Cu solar cell. Right: Simultaneously acquired NSOM image.

Figure 2 shows NSOM analysis of these devices revealing photocurrent collection five times greater when the NSOM tip is positioned above grain boundaries, suggesting that the local field at grain boundaries assists charge collection. We believe this type of analysis could help explain the high performance of many types of polycrystalline devices.

The above investigations indicate significant progress toward understanding the functional aspects of thin-film CdS/CdTe device operation. However, NREL CdTe research activities have also expanded to include fundamental studies with a goal of understanding the semiconductor defects that form during typical device processing. These defects are, in large part, responsible for resulting junction formation. Some of the more important defects that have been studied are related to Cu. Figure 3 shows cross-sectional CL analysis indicating that the location within the device of broad-band luminescence (~1.4-1.55 eV), as well as its energy dependence, depends on processes [6]. More recent (and lower-temperature) PL analysis, following controlled diffusion of Cu into single-crystal CdTe samples, has provided further insight regarding this broad-band luminescence. Figure 4 shows that temperature-dependent PL reveals a zero-phonon line at 1.456 eV for Cu-diffused, single-crystal CdTe samples when the sample temperature is <50 K. Further, this same PL transition is observed in both NREL and First Solar thin-film CdTe material - even prior to any $CdCl_2$ or Cu-contacting processes. Studies are ongoing, but preliminary analysis suggests the formation of a previously unreported defect that may be a donor [7].

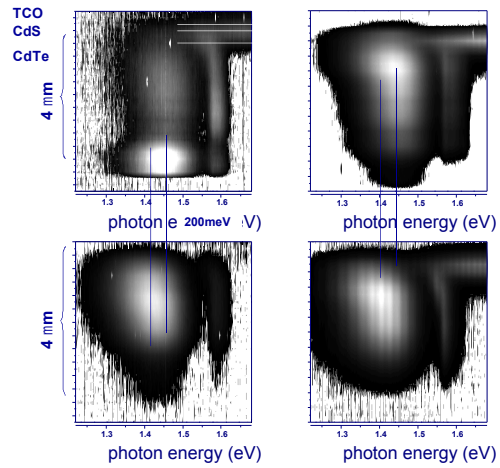

Figure 3. Cross-sectional CL at 77 K for NREL (left two maps) and First Solar (right two maps) material before (top) and after

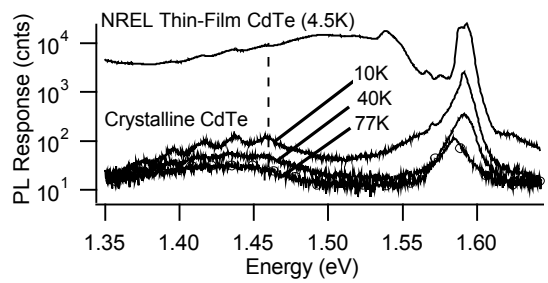

Figure 4. PL showing 1.456 eV zero-phonon emission and related LO phonons for both crystalline and thin-film CdTe samples.

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