

Process R&D for CIS-Based Thin-Film PV

**Annual Technical Report
January 2003–January 2004**

D.E. Tarrant and R.R. Gay
*Shell Solar Industries
Camarillo, California*



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NREL Technical Monitor: H.S. Ullal

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Preface

Shell Solar Industries (SSI), formerly Siemens Solar Industries has pursued the research and development of CuInSe₂-based thin film PV technology since 1980. At the start of subcontract activities with NREL, SSI had demonstrated a 14.1% efficient 3.4 cm² active-area cell, unencapsulated integrated modules with aperture efficiencies of 11.2% on 940 cm² and 9.1% on 3900 cm², and an encapsulated module with 8.7% efficiency on 3883 cm² (verified by NREL).

SSI began a 3-year, 3 phase cost-shared subcontract (No. ZN-1-19019-5) on May 1, 1991 with the overall project goal of fabricating a large area, stable, 12.5% aperture efficient encapsulated CIS module by scaleable, low-cost techniques on inexpensive substrates. Subcontract accomplishments were facilitated by addressing module reproducibility issues using small area test devices and mini-modules. Statistical process control disciplines were adopted to rigorously quantify process reproducibility. SSI addressed uniformity and reproducibility of absorber formation, interactions of the substrate with the absorber, and performance losses near interconnects. Subcontract accomplishments included demonstration of encapsulated module efficiencies that were at that time the highest reported mini-module efficiencies for any thin film technology (encapsulated 12.8% efficient mini-module on 68.9 cm² and an NREL-verified 12.7% efficient unencapsulated circuit on 69 cm² with a prismatic cover), demonstration of a champion large area (3860 cm²) encapsulated module efficiency of 10.3% (verified by NREL) that was the first thin film module of its size to exceed the 10% efficiency level, and delivery to NREL of a one kilowatt array of large area (~3890 cm²) approximately 30 watt modules [1].

From September 1995 through December 1998, SSI participated in a 3-year, 3 phase cost-shared TFPPP subcontract (No. ZAF-5-14142-03). The primary objective of this subcontract was to establish reliable high-throughput, high-yield thin film deposition processes in order to make CIS a viable option for the next generation of photovoltaics. Outdoor testing, accelerated environmental testing, and packaging development progressed throughout all phases of this subcontract. During Phase 1, SSI rigorously demonstrating process reproducibility and yield for a 10x10-cm monolithically interconnected "mini-module" baseline process and demonstrated a 13.6% aperture area efficient mini-module (verified by NREL). During Phase 2, SSI demonstrated the need to replace an existing large area reactor with a reactor based on a more direct scale-up of the baseline reactor, built a new large area reactor, and demonstrated comparable performance for the mini-modules baseline and 28x30-cm circuit plates. SSI developed products and prototype large area modules using a new package designed to integrate small circuit plates into larger modules. A one kilowatt array of Cu (In,Ga)(S,Se)₂ modules was delivered to NREL replacing a previously installed array based on an older absorber formation technology without sulfur incorporated in the absorber (Cu(In,Ga)Se₂). This array demonstrated significant improvements in efficiency and the temperature coefficient for power. SSI introduced two new 5-watt (ST5) and 10-watt (ST10) CIS-based products designed for use in 12 V systems, and NREL confirmed a new world-record efficiency of 11.1% on a SSI large area (3665 cm²) module. During subcontract Phase 3, substrate size was scaled from ~30x30 cm to ~30x120 cm and good process control was demonstrated with an average efficiency of 10.8%. Commercial product samples were delivered to NREL and a second set of ~30x120 cm modules (32 modules totaling ~1.2 kW) was delivered to the NREL Outdoor Test Facility. The NREL

measured average efficiency at standard test conditions of 11.4% was at that time the highest large area efficiency for any thin-film technology and NREL confirmed a world-record 11.8% large area (3651 cm²) efficiency for the champion module [2].

From August 1998 through November 2001, SSI participated in a 3-year, 3 phase cost-shared TFPPP subcontract (No. ZAF-5-14142-03). The primary objectives of this “Commercialization of CIS-Based Thin-Film PV” subcontract were to scale-up substrate size and to increase production capacity of the baseline CIS module process while introducing CIS-based products. These objectives were pursued to demonstrate fabrication of efficient and stable thin-film modules made by scaleable, manufacturable, low-cost techniques. An additional mid- to longer-term objective was to advance CIS based thin-film technology thereby assuring future product competitiveness by improving module performance, cost per watt produced, and reliability. Throughout this subcontract, SSI capabilities were leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics. SSI’s approach to this work was to apply design of experiment and statistical process control methodologies. Siemens Solar was the first company in the world to start production of PV modules based on CIS thin-film technology and this major milestone in the development of PV was recognized by R&D Magazine by awarding the prestigious R&D 100 Award to the Siemens Solar family of CIS solar modules. NREL, the California Energy Commission and SSI shared this award. SSI expanded the CIS product line in 1999 to include 20-Watt “ST20” modules and 40-Watt “ST40” modules. Also during the first subcontract phase, a record-breaking efficiency of more than 12% was verified by NREL for an ST-40 module. This result in 1999 far surpassed the DOE year 2000 goal for a commercial CIS module above 10%. During the second subcontract phase, SSI delivered 20 ST-40 large area modules, all with efficiencies over 11%, to meet the subcontract deliverables defined as large area modules with efficiencies over 10%. The average efficiency based on a Gaussian fit to the main portion of the circuit plate efficiency distribution was increased from 10.8% prior to this subcontract to 11.6% for this subcontract period. These advancements were due to continuous improvement of all process along with particular attention to process research for two critical processes – CIS formation in new large area reactors and the quality of molybdenum deposited in new high capacity sputtering equipment. Process development improved adhesion, decreased breakage, addressed control of raw materials, and decreased failures associated with patterning. Further R&D of all CIS processes for part size and capacity scale-up was pursued during the third subcontract phase. Major accomplishments included addressing process issues for implementation of high quality high throughput Mo deposition and patterning, high throughput precursor deposition, and higher throughput reaction of the precursor. Circuit plate production capacity was increased by more than an order of magnitude from the beginning of this subcontract while circuit and module efficiencies were steadily improved. The second subcontract milestone – to achieve a pilot production rate of 500 kW per year by the end of subcontract – was first achieved in March of 2001 [3].

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Summary

Compared to traditional wafer-based crystalline silicon technologies, monolithic integration of thin film solar cells can lead to products of comparable performance but with significant manufacturing advantages: lower consumption of direct and indirect materials, fewer processing steps and easier automation. Monolithic integration is required to achieve these advantages since this eliminates multiple process steps and handling operations during both formation of the absorber and during module assembly. The basic module elements for all thin-film technologies (alloys of amorphous silicon, cadmium telluride and CIS) are the same; the module elements are a circuit-glass/cover-glass laminate, a frame, and a junction box. The basic circuit elements are also very similar; they each have a base electrode, an absorber, a junction, a top electrode and three patterning steps for monolithic integration. While the details of these module elements or equivalent module elements differ, the basic cost structures are very similar on an area-related basis. Since the cost per unit area is the same, the cost per watt is inversely proportional to the module efficiency. CIS cells and monolithically integrated modules have demonstrated the highest efficiencies of any candidate thin-film technologies; therefore, CIS is expected to have the lowest manufacturing cost/watt.

The primary objectives of this subcontract are to:

- Address key near-term technical R&D issues for continued CIS product improvement
- Continue process development for increased production capacity
- Develop processes capable of significantly contributing to DOE 2020 PV shipment goals
- Advance mid- and longer-term R&D needed by industry for future product competitiveness including improving module performance, decreasing production process costs per watt produced, and improving reliability
- Perform aggressive module lifetime R&D directed at developing packages that address the DOE goal for modules that should last up to 30 years while retaining 80% of initial power

Outstanding progress has been made in the initial commercialization of high performance thin film CIS technology. During this subcontract period, predictability of SSI's CIS process was demonstrated by continuously executing the process while increasing throughput. Cumulative production for 2002 exceeded 1 MW - about twice the production rate for 2001. Capacity in 2003 increased to somewhat below 3 MW per year and production for 2003 was just over 1.2 MW per year. Introducing a new product accounts for the main difference between production and capacity. The laminate efficiency distribution for 2003 peaked at 11.0% with a full width of only 11% of the average. This distribution is nominally the same as the distribution for 2002 but with an approximately 33% increase in large area laminate production volume. The following quote from the EERE Multi-Year Technical Plan (MYTP) recognizes previous SSI accomplishment, "After two decades of R&D, CIS is being introduced to the market, with prototype modules made by Shell Solar (Camarillo, CA) consistently reaching efficiencies greater than 11%—beating a goal set in the last PV Subprogram 5-year plan by more than a year." Again at least a year in advance and with production modules rather than champion modules, recent SSI accomplishments far exceed the 2003 DOE EERE Multi-Year Technical Plan technical target of 8% module conversion efficiency for thin-film modules.

Dramatic increases in line yield were achieved by improved production protocols and by addressing disparate special causes for process variation. Line yield increased from about 60%

in 2000 to about 85% in 2002. This high line yield was maintained during 2003. NREL confirmed a champion 12.8% aperture area conversion efficiency for a large area (3626 cm²) CIS production module. Process R&D during this and previous subcontract periods, both at SSI and in collaboration with NREL teams, has demonstrated the potential for further performance improvements. This 12.8% efficient champion module demonstrated the potential to meet the 2007 MYTP technical target of 12% module conversion efficiency.

Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules with multiple prototype package designs have undergone testing for over fourteen years. However, field failures have also been observed. Field failure mechanisms related to particular package designs and errors during production have been clearly identified. Additional circuit plate or packaging process variables may have affected durability during particular production timeframes; when losses have been observed, the losses correlated with date of deployment or prototype module configuration. Losses are not inherent to CIS; multiple past and present module deployments have demonstrated stability.

SSI is developing “glass/glass” packages that eliminate the TPAT backsheet used in present products. The primary advantage is decreased packaging costs. Simplification of the package and decreased operating temperature are additional potential advantages. Prototype glass/glass packages for individual 40W circuit plates have passed accelerated tests, including the damp heat test. This package incorporates an edge seal developed in collaboration with the National Thin-Film PV Module Reliability Team. Development of the 40W glass/glass packages is being extended to a new 80W product made using two nominally 40W circuit plates laminated to a common front sheet.

SSI independently and in conjunction with TFPPP team activities has pursued improved understanding of CIS processes and devices. Extending this work, options for minimizing or eliminating transient effects have been demonstrated during this subcontract period. The importance of transient effects is primarily related to production rather than long-term outdoor stability; thermally induced transients are not observed in the field despite daily and seasonal changes in module temperature. Transient effects are an important issue for production since they complicate all activities related to measurements: product ratings, definition of measurement protocols, accelerated testing, etc. Thicker CdS decreases transients while partial electrolyte soaks apparently have no long term effect. Studies of sulfur content variation during the reaction process indicate significantly decreased transients for lower sulfur content relative to the present baseline. Samples purposely fabricated with low sodium content were much more sensitive to thermal exposure. However, there was no apparent correlation between transient effects and sulfur or sodium levels for the relatively small position dependence within a reactor. Modifying CdS thickness and the sulfur content is expected to decrease transient effects.

These production R&D results, production volume, efficiency, high line yield and advances in understanding, are a major accomplishment. The demonstrated and maintained high production yield is a major accomplishment supporting attractive cost projections for CIS. Process R&D at successive levels of CIS production has led to the continued demonstration of the prerequisites for commitment to large-scale commercialization. Process and packaging R&D during this and previous subcontract periods has demonstrated the potential for further cost and performance improvements. SSI's thin-film CIS technology is poised to make very significant contributions to DOE/NREL/NCPV long-term goals - higher volume, lower cost commercial products.

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Introduction

Overview

Multinary $\text{Cu}(\text{In,Ga})(\text{Se,S})_2$ absorbers (CIS-based absorbers) are promising candidates for reducing the cost of photovoltaics well below the cost of crystalline silicon. CIS champion solar cells have exceeded 19% efficiency for devices fabricated at NREL [4]. Small area, fully integrated modules exceeding 13% in efficiency have been demonstrated by several groups [5]. Record breaking efficiencies of over 12% for a commercial large area module have been verified by NREL [6]. Long-term outdoor stability has been demonstrated at NREL by $\sim 30 \times 30$ cm and $\sim 30 \times 120$ cm SSI modules which have been in field-testing for over fourteen years. Projections based on current processing indicate production costs well below the cost of crystalline silicon [5].

Compared to traditional wafer-based crystalline silicon technologies, new thin film technologies yield products of comparable performance but with significant advantages in manufacturing [5, 7]:

- Lower consumption of direct and indirect materials
- Fewer processing steps
- Easier automation

Lower consumption of direct and indirect materials results in part from the thin-film structure for the semiconductor used to collect solar energy. All three of these manufacturing advantages are in part due to an integrated, monolithic circuit design illustrated in Figure 1. Monolithic integration eliminates multiple process steps that are otherwise required to handle individual wafers and assemble individual solar cells into the final product.

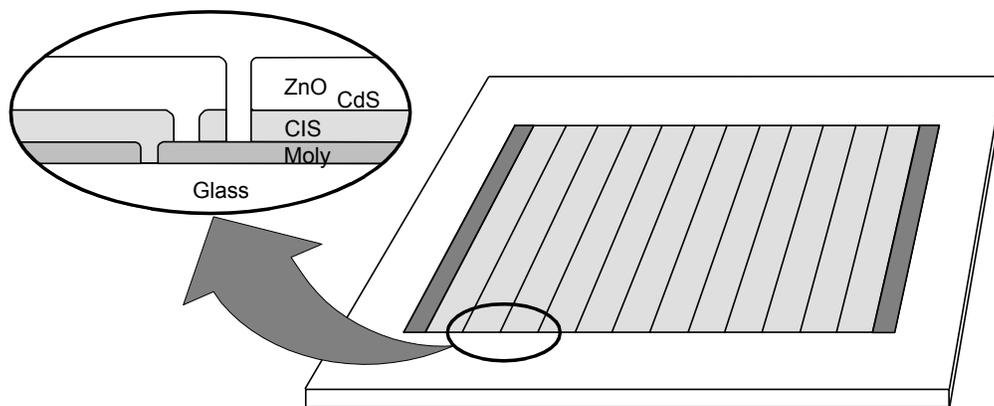


Figure 1. Structure of SSI's monolithically integrated thin-film circuits.

A number of thin film photovoltaic technologies have been developed as alternatives to the traditional solar cells based on crystalline silicon wafers [5]. The technologies with the greatest potential to significantly reduce manufacturing costs are based on alloys of amorphous silicon (a-Si), cadmium telluride (CdTe), CIS, and film silicon (Si-film). These photovoltaic thin film technologies have similar manufacturing costs per unit area since all share common elements of design and construction:

- Deposition of typically three layers on a suitable substrate – window/electrode, absorber, and back electrode
- Patterning to create monolithically integrated circuit plates
- Encapsulation to construct modules

Cost per watt is a more appropriate figure of merit than cost per unit area [5]. All thin film technologies have similar manufacturing costs per unit area since they all use similar or equivalent deposition, patterning, and encapsulation processes. About half of the total module cost – material, labor, and overhead – originates in the encapsulation scheme which is for the most part independent of the thin film technology. Costs for alternative encapsulation schemes are typically similar or even higher. The average efficiency of large, ~30x120 cm modules in pilot production at Shell Solar is approximately 11%. This performance is at the lower end of the range for products based on crystalline silicon. The lowest cost per peak watt will result from the technology with the highest efficiency, CIS technology, since most thin film technologies have similar cost per unit area.

SSI CIS Process

Most photovoltaic products are designed for 12-volt or higher applications, but the output voltage of an individual solar cell is typically about 0.5 volts. Wafer-based technologies build up the voltage by connecting individual solar cells in series. In contrast, CIS circuits are fabricated monolithically (Figure 1); the interconnection is accomplished as part of the processing sequence to form the solar cell by alternately depositing a layer in the cell structure and patterning the layer using laser or mechanical scribing.

The structure of a SSI CIS solar cell is shown in Figure 2. The full process to form CIS circuit plates, including monolithic integration, is outlined in Figure 3. This process starts with ordinary sodalime window glass, which is cleaned and an SiO₂ barrier layer is deposited to control sodium diffusion and improve adhesion between the CIS and the molybdenum (Mo) base electrode. The Mo base electrode is sputtered onto the substrate. This is followed by the first patterning step (referred to as “P1”) required to create monolithically integrated circuit plates – laser scribing to cut an isolation scribe in the Mo electrode. Copper, gallium and indium precursors to CIS formation are then deposited by sputtering. Deposition of the precursors occurs sequentially from two targets in an in-line sputtering system, first from a copper-gallium alloy target (17 at% Ga) and then from a pure indium target. CIS formation is accomplished by heating the precursors in H₂Se and H₂S to form the CIS absorber. Beginning at room temperature, furnace temperature is ramped to around 400°C for selenization via H₂Se, and ramped again to around 500°C for subsequent sulfidation via H₂S, followed by cool-down to room temperature. This deposition of copper and indium precursors followed by reaction to form CIS is often referred to as the two-stage process. A very thin coating of cadmium sulfide (CdS) is deposited by chemical

bath deposition (CBD). This layer is often referred to as a “buffer” layer. A second patterning step (P2) is performed by mechanical scribing through the CIS absorber to the Mo substrate thereby forming an interconnect via. A transparent contact is made by chemical vapor deposition (CVD) of zinc oxide (ZnO). This layer is often referred to as a “window layer” or a transparent conducting oxide (TCO). Simultaneously, ZnO is deposited on the exposed part of the Mo substrate in the interconnect via and thereby connects the Mo and ZnO electrodes of adjacent cells. A third and final patterning step (P3) is performed by mechanical scribing through the ZnO and CIS absorber to isolate adjacent cells.

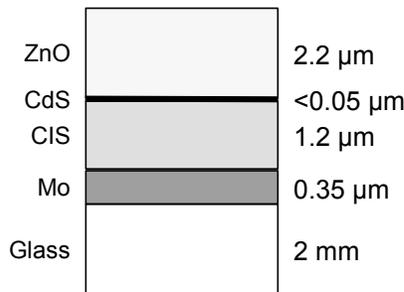


Figure 2. SSI's CIS cell structure (not to scale).

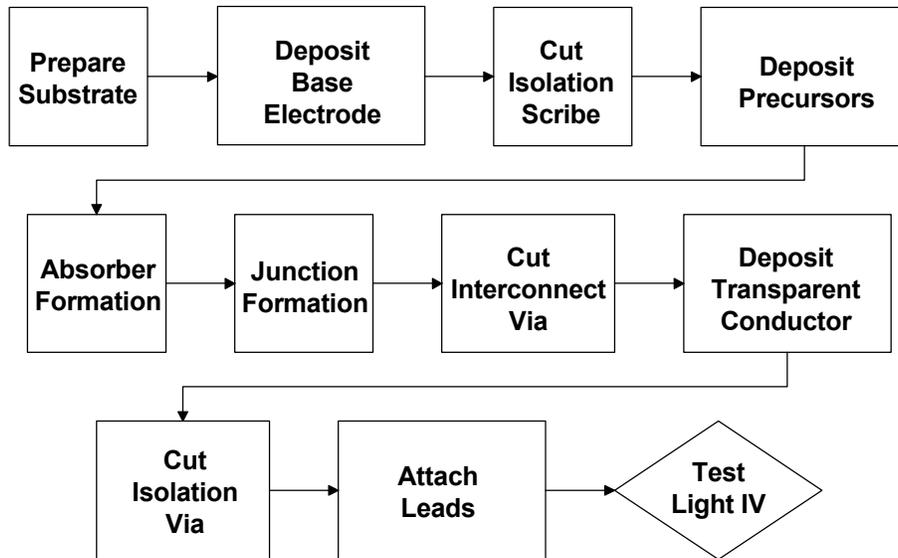


Figure 3. SSI CIS Circuit Processing Sequence.

The CIS-based absorber referred to in this report is composed of the ternary compound CuInSe_2 combined with sulfur and gallium to form the multinary compound Cu(In,Ga)(S,Se)_2 . Gallium and sulfur are not uniformly distributed throughout the absorber but the concentrations are graded; hence, this structure is referred to as a “graded absorber.” The graded absorber structure is a graded Cu(In,Ga)(Se,S)_2 multinary with higher sulfur concentration at the front and back and

higher Ga concentration at the back. Elemental profiles typical of the SSI graded absorber structures are presented in Figure 4. Efficiency, voltage, and adhesion improvements have been reported for the SSI graded absorber structure [1, 8, 9].

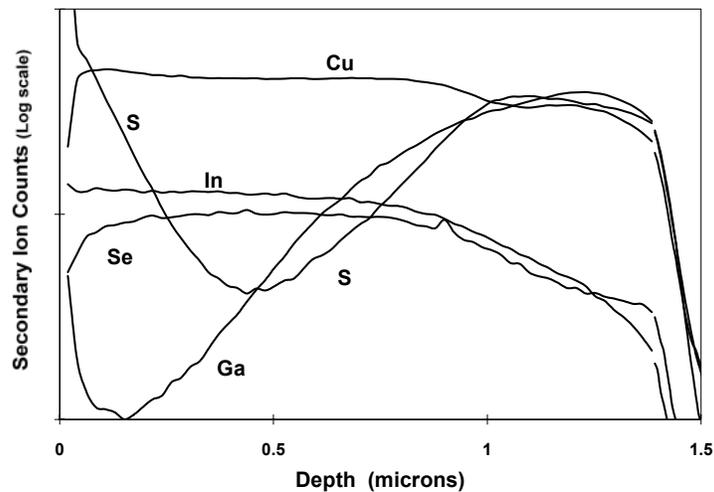


Figure 4. Typical elemental profile for the SSI graded absorber (SIMS from NREL).

Figure 5 illustrates the module configuration used for prototypes and products during this subcontract period. EVA is used to laminate circuit plates to a tempered cover glass and a Tedlar/polyester/Al/Tedlar (TPAT) backsheet provides a hermetic seal. Aluminum extrusions are used to build frames for the modules. In addition to providing a hermetic seal, the combination of the TPAT backsheet and the offset between the circuit plate and the frame provides electrical isolation from the frame.

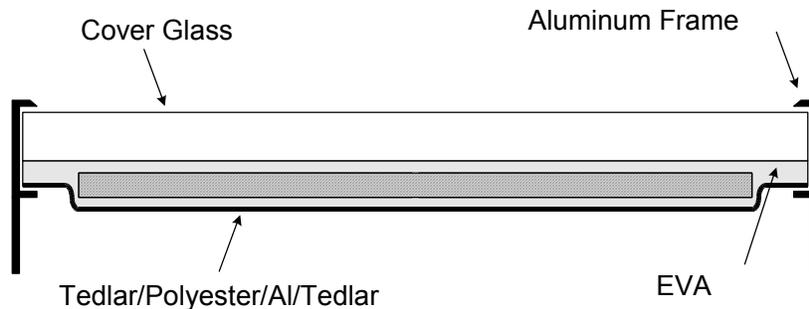


Figure 5. Single circuit plate module configuration with a TPAT backsheet.

SSI's CIS processing facility produces nominally 1x4 ft. circuit plates for production and process R&D. Full size 1x4 ft. circuit plates are used for ST40, 40W product. Smaller modules in the ST series of products are cut from circuit plates with the same design. Processing through all CIS device fabrication and monolithic integration process steps is the same for full size 1x4 ft. and smaller modules.

SSI's R&D Approach

From the industrial perspective, the full process sequence anticipated for use in large-scale production must be mastered and rigorously demonstrated. The SSI research approach is composed of two main elements:

- Experimentation and development using device structures that exercise all aspects of large area module production [10]
- Application of statistical process control (SPC) as the discipline to rigorously quantify process reproducibility, and application of statistical methods such as analysis of variation (ANOVA) to rigorously quantify experimental results [11, 12].

Process predictability is a prerequisite for commercialization of thin-film PV since product performance ratings, yields and costs must be known before committing to produce products. Also, process predictability is essential for proper interpretation of process development efforts since experimental results may be ambiguous or misleading if compared to an unpredictable baseline process. SSI has adopted SPC methodologies because SPC was developed to rigorously quantify process reproducibility and process capability; the essence of SPC is predictability. Equally significantly, SPC provides the measure of systematic progress as processes are developed. Communication of this progress is typically best expressed in the language of the SPC discipline [13]. For example, process characterization results are demonstrated to be “statistically significant” based on knowledge of process repeatability measured using the SPC discipline and compared to a predictable baseline process. Confidence in the appropriate interpretation of experimental results is gained through application of statistical methods such as ANOVA to demonstrate statistically significant results.

Subcontract Activities and Milestones

Background

The purpose of the Thin-Film Photovoltaics Partnerships Program (TFPPP) is to accelerate the progress of thin film solar cells and module development as well as to address mid and long-term research and development issues. The long-term objective of the TFPPP is to demonstrate commercial, low-cost, reproducible, high yield and robust modules of 15% aperture-area efficiency. Furthermore, this research is directed at making progress toward this objective by achieving interim goals in thin film module efficiencies; cell and module processing; cell and module reliability and the necessary fundamental research needed to build the technology base that supports these key areas. Participation in the National R&D Teams is paramount to the success of this project. The DOE/NREL/NCPV strategy in undertaking this R&D effort is to maintain the good coupling between laboratory results from fundamental materials and processes research to manufacturing R&D, pilot-line operation, and early entry of advanced thin-film PV products to the ever-growing worldwide marketplace.

The purpose of this subcontract, as part of the Technology Partners Category, is to accelerate the progress of thin film solar cell and module development as well as to address mid and long-term research and development issues by achieving aggressive interim goals in thin film module

efficiencies; cell and module processing; cell and module reliability; and in the technology base that supports these key areas.

Objectives

The primary objectives of this subcontract are to:

- Address key near-term technical R&D issues for continued CIS product improvement
- Continue process development for increased production capacity
- Develop processes capable of significantly contributing to DOE 2020 PV shipment goals
- Advance mid- and longer-term R&D needed by industry for future product competitiveness including improving module performance, decreasing production process costs per watt produced, and improving reliability
- Perform aggressive module lifetime R&D directed at developing packages that address the DOE goal for modules that should last up to 30 years while retaining 80% of initial power

Milestones

SSI shall perform each of the above tasks with the goal of meeting the following targets:

- Scale the substrate size from 1 ft. x 4 ft. to approximately 2 ft. x 5 ft. by the end of the subcontract.
- Achieve pilot production rates of 9,000 kW per year by the end of the subcontract.
- Demonstrate commercial, low-cost, reproducible, high yield and robust module process that achieve the DOE goal for 15% aperture-area efficiency
- Deliverables for the subcontract include CIS-based products and representative modules delivered to the NREL Module Testing Team for outdoor testing and evaluation.

Deliverables

SSI will deliver 10 representative CIS-based module products at the end of each phase of the subcontract.

SSI will deliver 10 representative CIS modules to the NREL Module Testing Team by the end of each phase of the subcontract.

Technical Review

Capacity and Product Line Expansion Overview

Production and process R&D have been based on nominally 1x4 ft. circuit plates for the ST40, 40W product. Smaller products and R&D samples have typically been cut from these circuit plates. The module configuration with a TPAT backsheet illustrated in Figure 5 has been used for production of four product sizes, with and without frames, and for R&D. During this subcontract period three additional configurations have been used for process, capacity and packaging R&D: circuit plates designed for a nominally 40W glass/glass package, two nominally 40W circuit plates laminated to a common tempered glass front sheet forming a “ST80” and minimodules. R&D results based on using these packages are reported for a range of R&D efforts from absorber formation studies to packaging studies. An overview of these configurations is given in advance of reporting on R&D results since results for these variants are not unique to one topic and appear in multiple technical sections of this report – Process R&D, National CIS R&D Team, Package Development.

Most production infrastructure, with the exception of absorber formation reactors, is compatible with larger circuit plates - up to nominally 2x5 ft. Overall capacity increases can be achieved by increasing the substrate size; however, reviewing this approach in light of recent process developments has led to the conclusion that substrate size scale up may not be the only or best route to increasing capacity. Production capacity increases have been achieved through process development to increase the number of substrates processed in a reactor batch. This process development addressed tendencies toward increased warping and poorer adhesion for larger substrate loads. Increased capacity by stacking reactors one over another, using the floor space that would normally be required for one reactor, has also been demonstrated. Higher power products can be fabricated using multiple circuit plates rather than larger circuit plates; prototype modules using two 1x4 ft. circuit plates have been built. Increasing the substrate size is an option that has potential value and will continue to be considered, particularly as a longer-term option. However, substrate size scale up may not be the best short-term approach to increasing capacity.

SSI is now developing “glass/glass” package designs that eliminate the TPAT backsheet primarily to decrease packaging costs. Simplification of the package and decreased operating temperature are additional potential advantages. Figure 6 is a sketch comparing the present production package and a single circuit plate glass/glass package. In addition to decreased cost, simplification of the package may increase yield. Decreasing the operating temperature will lead to higher efficiency for modules in the field.

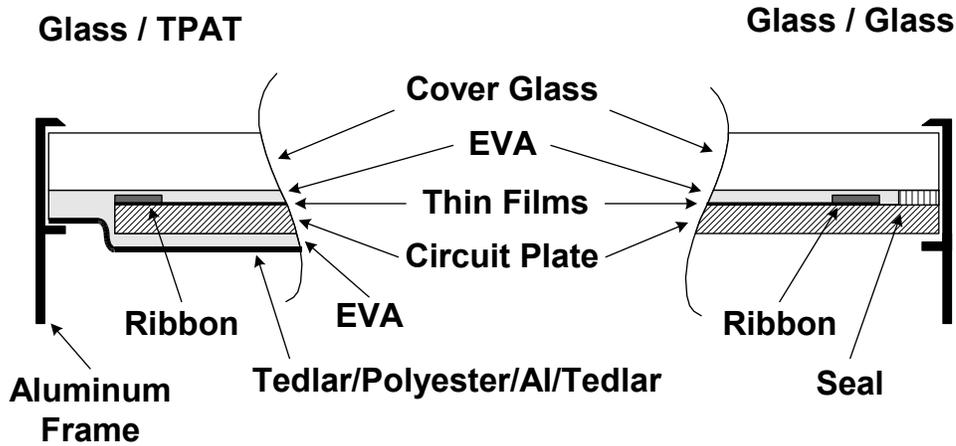


Figure 6. Present and future package designs.

Progress toward developing and testing glass/glass packages using a single 40W circuit plates will be reported. These results are being extended to a new 80W product (ST80) made using two nominally 40W circuit plates laminated to a common tempered glass front sheet. More detail on this design is discussed in the Package Design section of this report. The product may be available in both framed and unframed versions.

SSI studied and began production of a new product. The product is a 6cm by 6cm minimodule with a plastic encapsulant for consumer applications (Figure 7). This new product may expand near-term and long-term capacity scale-up options for the SSI CIS manufacturing.

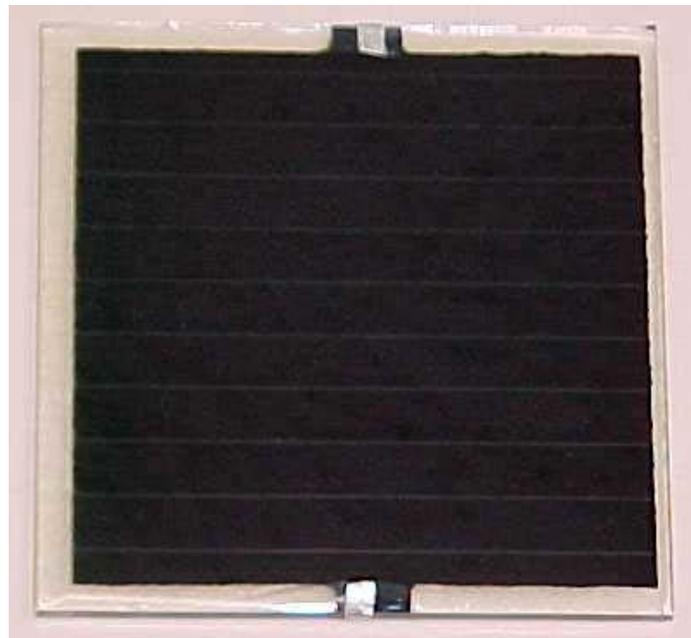


Figure 7. Potential 6cm by 6cm minimodule for consumer applications

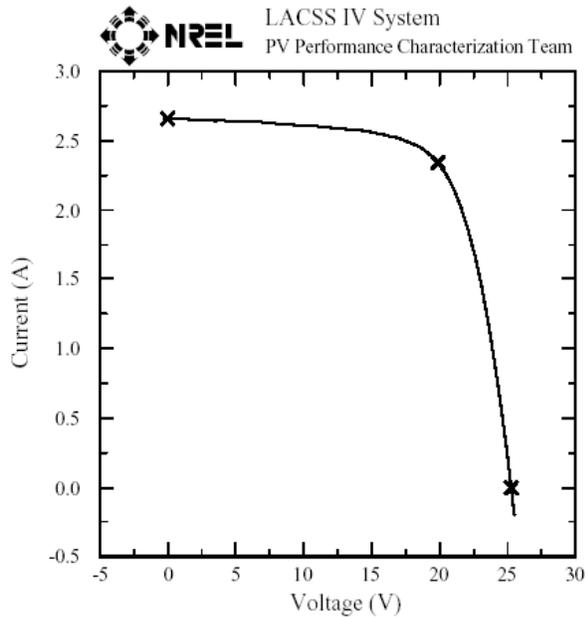
There are additional benefits for development work using minimodules. For example, reactor position dependence studies can be augmented with increased spatial resolution. Minimodules are created on the same size, nominally 1x4 ft., circuit plate used for power modules. Patterning for monolithic integration is asymmetric; patterning for the positive buss is different from patterning for the negative bus. Only one set of positive and negative bus bars are created for 40W circuit plates. Smaller circuit plates with both busses can be created by dicing the larger plates perpendicular to the long dimension. Dicing the larger plates parallel to the long dimension would create subsections without the required positive and negative busses. Therefore, a 1x4 ft., 40W circuit plate only accommodates exploring position dependence along the long dimension. Minimodule circuit plates allow position dependent mapping in both dimensions since bus bar structures are repeated across the short dimension. Also, minimodule process development for increased capacity parallels or augments process development for power modules. Regarding packaging, process development to define environmental packages for minimodules, which have unique requirements, have led to new understanding of general packaging issues and to new process options.

As with power module measurement, transient effects are very important for minimodule production since they complicate accelerated testing, analysis for process definition, definition of measurement protocols, analysis of process predictability, interpretation of experimental test results, and understanding of device structures. Recent efforts have included addressing transient effects while developing the capabilities necessary to measure each minimodule in a few seconds.

Process R&D

Performance and Capacity

During this subcontract period NREL confirmed a champion 12.8 percent aperture area conversion efficiency for a large area (3626 cm²) CIS module (Figure 8). The aperture area for this champion module was defined by taping off the approximately 1 cm inactive boarder surrounding the monolithically integrated CIS circuit in a ST40, 40W, production module. Other than definition of the aperture area, this module is simply one module from the upper end of the production distribution for standard modules.



	Module	per Cell	
Eff	12.8		%
Pmax	46.5		W
Voc	25.3	0.601	V
Isc	2.7		A
Jsc		30.8	mA/cm ²
FF	69.2		%
Area*	3626	86.3	cm ²
Cells	42		

* Aperture area - including interconnect loss

Figure 8. Champion ST40 module from the upper end of the production distribution

Figure 9 is the production distribution for approximately twenty one thousand ~1x4-ft. laminates produced during 2003. The average efficiency of this distribution is 11.0%. A Normal distribution fit to the main portion of the distribution yields a standard deviation of 0.60%. Over 88% of this production output is over 10% efficiency. This distribution is nominally the same as the distribution for 2002 but with an approximately 33% increase in production volume.

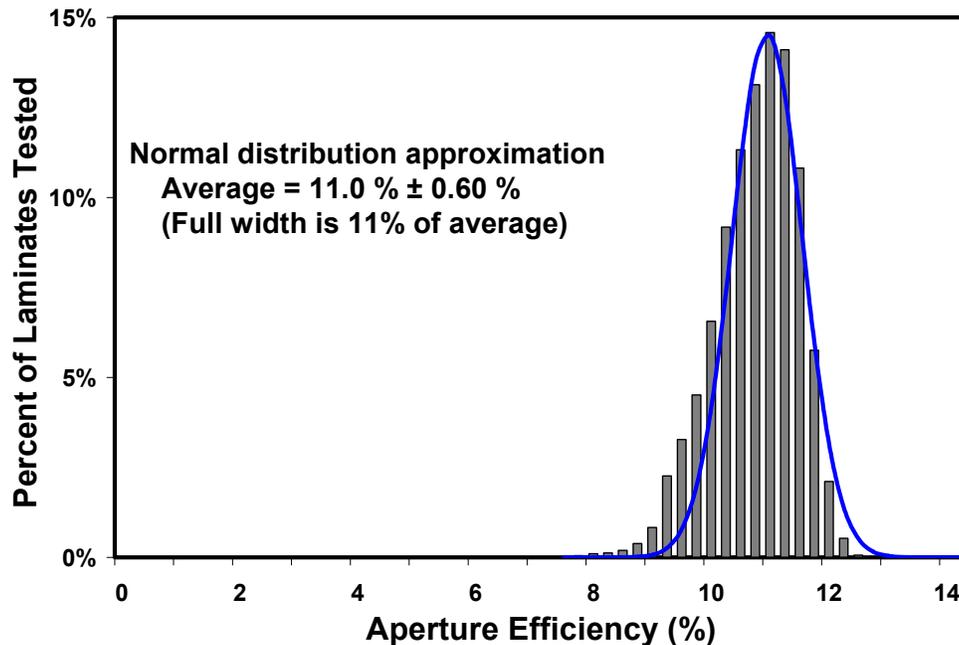


Figure 9. Production distribution for 1x4-ft. laminates produced during 2003

Historical production rates and the production rate achieved during 2003 are charted in Figure 10. Prior to 2003, the data is for ST40, 40W product and smaller modules in the ST series of products produced from the same circuit plate design. Data for 2003 includes production data for the new 6cm by 6cm minimodule consumer product. SSI 2003 capacity was somewhat less than 3 MW per year whereas production for 2003 was just over 1.2 MW per year. Introducing the new product accounts for the main difference between production and capacity. Significant differences between capacity and production are expected to continue as new products are introduced and while capacity is increased.

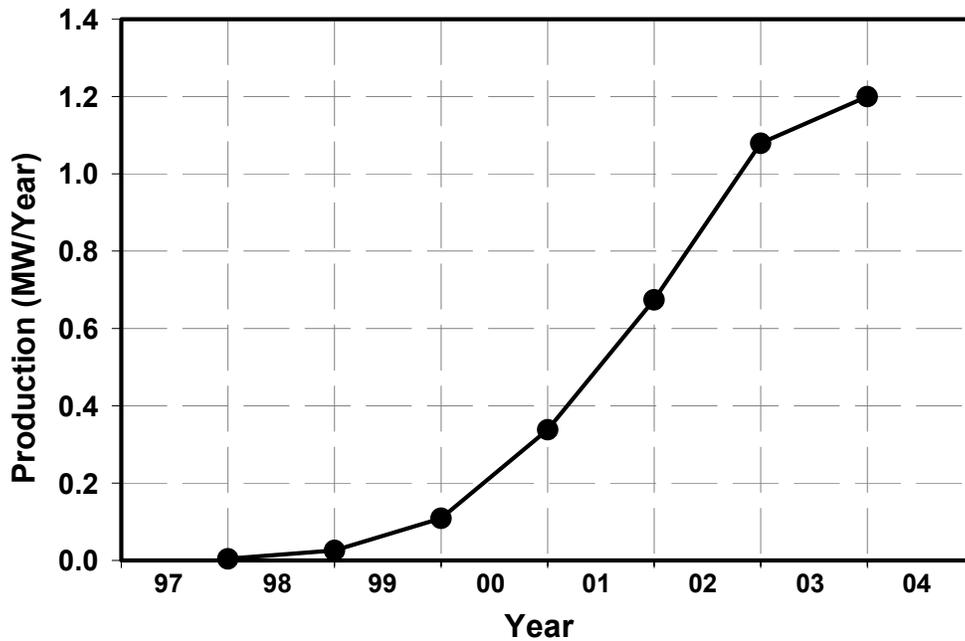


Figure 10. Historical production rate including the first phase of this subcontract (2002).

During this subcontract period, capacity growth through improvements in production equipment, processes and procedures were considered for all products. Equipment utilization improvements and process changes for decreased process time were implemented for base electrode deposition, precursor deposition, absorber reaction, buffer deposition, ZnO deposition and patterning steps.

As reported in the previous annual report, dramatic increases in CIS line yield have been demonstrated [14, 15]. Line yield is defined as the ratio of two areas – the area of product produced divided by the area of glass started through the production line. This is total yield including both electrical yield and mechanical yield through all processing required to produce products. Line yield has increased from about 60% in 2000 to about 85% in 2002. Figure 11 illustrates yield improvements over approximately the last four years. These advancements were due to continuous improvement of multiple processes. This major accomplishment supports attractive cost projections for CIS.

- Decreased peeling related to ZnO deposition
- Decreased loss of process runs by improving infrastructure for higher capacity and yield

Cell gridding and IV and QE measurements were performed by the Battelle/Pacific Northwest National Laboratory group headed by Dr. Larry Olsen (PNNL). These tasks supported subcontract work on efficiency improvements, transient studies and substrate size and capacity scale-up. Procedures and fixtures have been developed to create gridded devices on sections diced from patterned production circuit plates. This approach, measuring samples directly from the power module production line with minimal additional unique processing, is pursued to obtain results that are directly relevant to production processes. PNNL set up the infrastructure necessary for gridding and measurements. An initial group of 25 devices was selected to verify procedures and measurements. Total area efficiency results were lower than expected (Figure 12) due to somewhat low measured current density ($\sim 26 \text{ mA/cm}^2$). Variation in J_{sc} accounts for most of the variation in Eff. Otherwise, the cell to cell consistency of V_{oc} and FF was good (V_{oc} - avg. 0.586, std. dev. 0.020, FF - avg. 0.586, std. dev. 0.020).

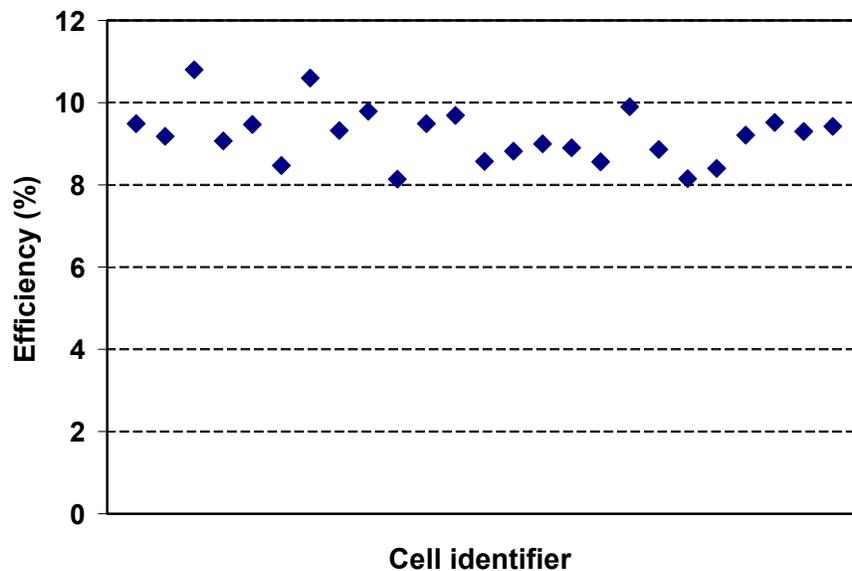


Figure 12. Initial cell measurements results with lower than expected Eff.

Samples from this group and Si control devices were sent to NREL for measurements and are now used for calibration. A second set of samples was sent to PNNL and two devices from this group were also sent to NREL for calibration measurements. As indicated in Table 1, agreement within 5% of NREL measurements was achieved for all IV parameters.

Table 1. PNNL measurements relative to NREL measurements.

Cell I.D.	Voc (V)	Jsc mAcm ²	FF	Eff
03-B2-2.5	1.03	0.95	0.96	0.95
03-B2-7.5	1.01	0.98	0.98	0.97

After developing capabilities for gridding and measuring cells on circuit plates for power modules, SSI requested that PNNL change to grids and hardware for generating and measuring SSI’s production of new minimodule products. This was accommodated and another set of minimodules was sent to PNNL for gridding and measurement verification.

Another group of samples measured at PNNL was selected to characterize the spatial uniformity of a production circuit plate. Figure 13 illustrates the position of “slices” and cells used to characterize a nominally 1x4 ft. circuit plate.

Seven “slices”, (see Figure 13) nominally the same as 5W, ST5 product, were made and measured at SSI to map performance parallel to the long dimension of a 1x4 ft. circuit plate - front to back in a reactor. Samples for cell measurements at PNNL were selected to duplicated this sub-module slice data and sample the potential vertical position dependence within the reactor – top to bottom in the illustration.

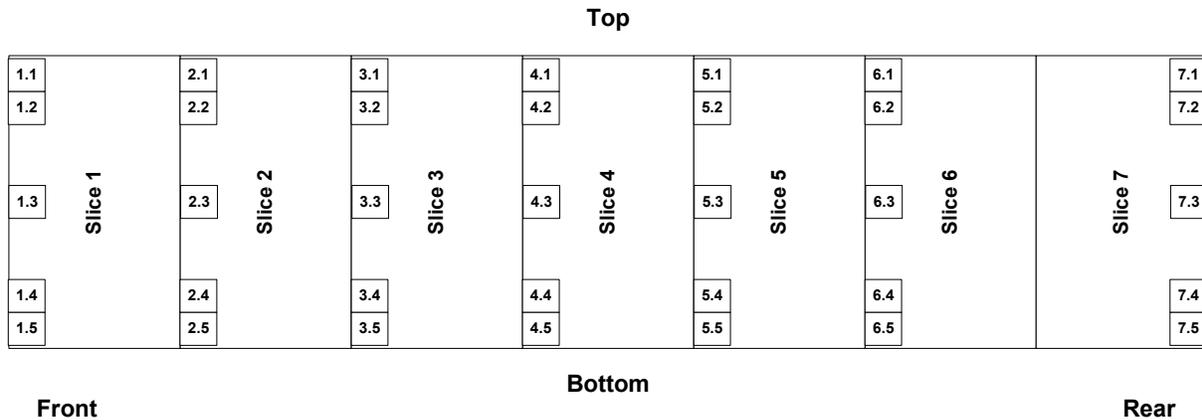


Figure 13. Sub-module slice and cell positions on a nominally 1x4 ft. circuit plate.

A 1x4 ft. circuit plate that was expected to be uniform based on experience with sub-module measurements was selected for mapping at PNNL. Sub-module and cell IV data are presented in Figure 14 through Figure 17. The size of the sample set, particularly for QE measurements, is smaller than planned because hand dicing led to poor control of sample size and interference with the fixturing for grid deposition. Solid diamonds represents slice data (referred to in the legend as “ST5”). Connected open circles represent the data for cells from one slice where the top to bottom dependence is plotted from left to right (relative positions in the charts are maintained even when there is missing data). Trend lines are included when a position dependent correlation (other than flat) was found to be statistically significant at the 95%

confidence level. For Voc, there is minimal variation with position for both dimension and good correlation between slice and cell results.

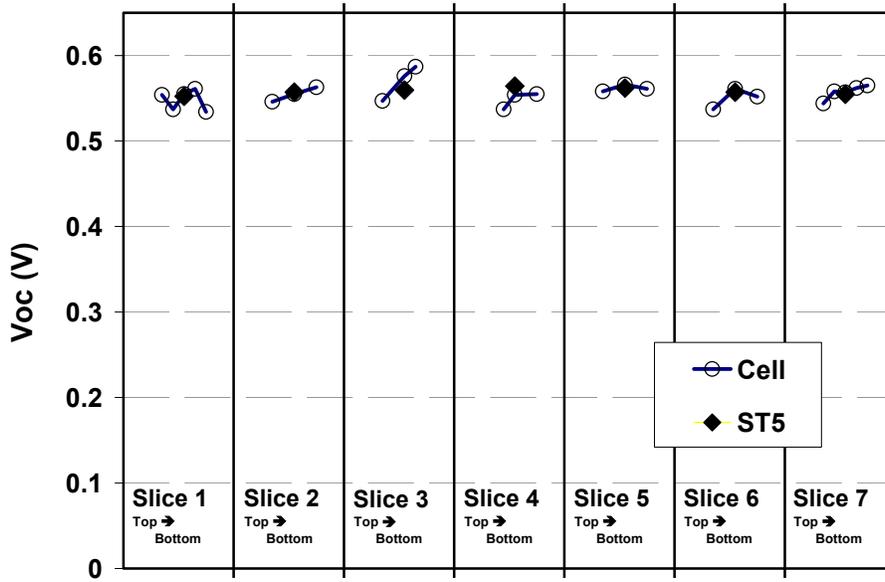


Figure 14. Sub-module slice and cell Voc versus position - front to back and top to bottom in a reactor.

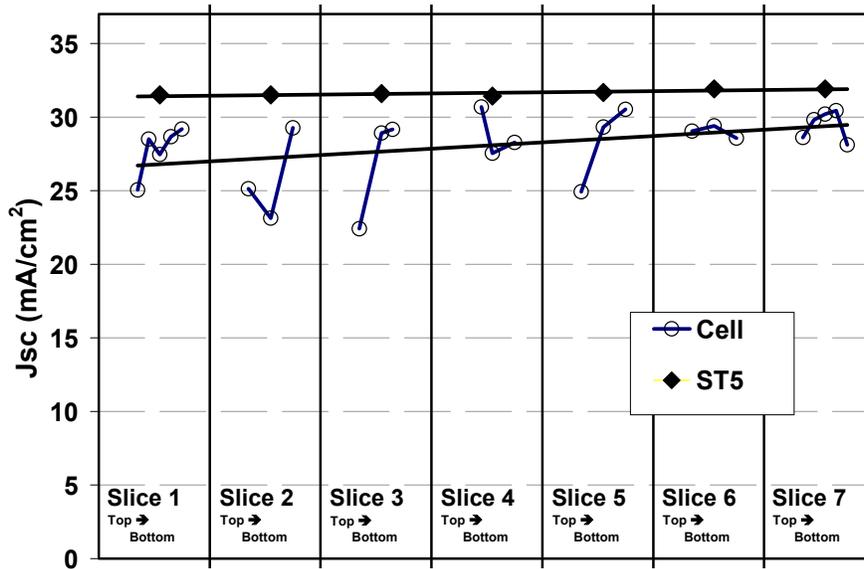


Figure 15. Sub-module slice and cell Jsc versus position - front to back and top to bottom in a reactor.

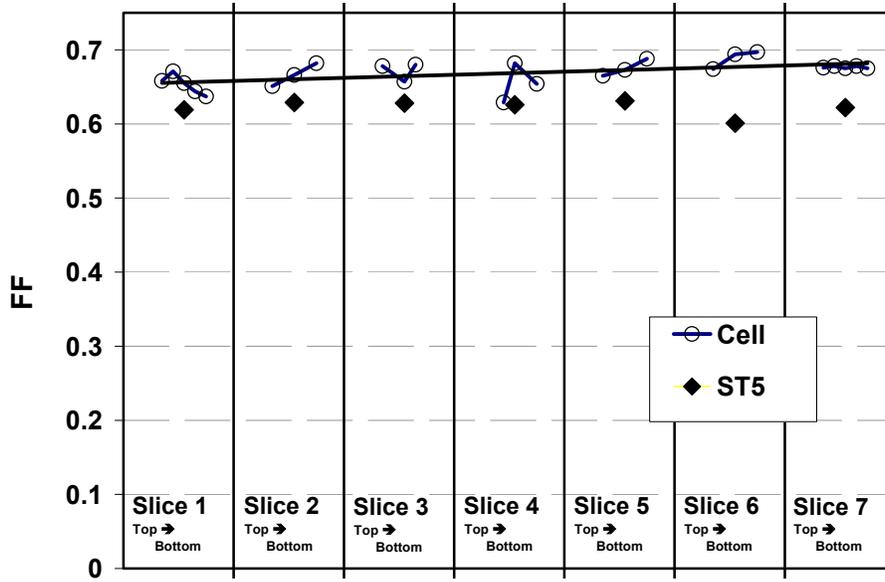


Figure 16. Sub-module slice and cell FF versus position - front to back and top to bottom in a reactor.

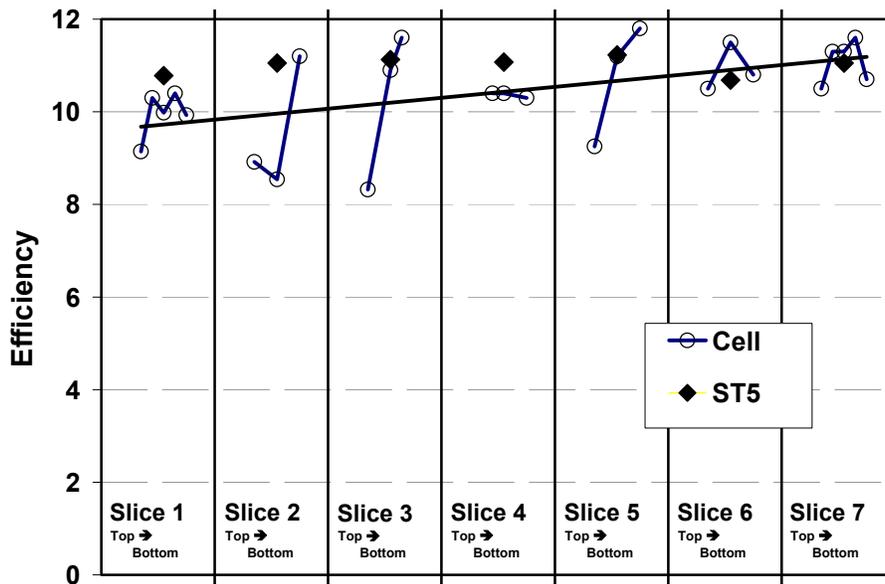


Figure 17. Sub-module slice and cell Eff versus position - front to back and top to bottom in a reactor.

Cell data exhibits significant within-slice variability in Jsc with a span of about 16% of the average. This may be a top to bottom i.e. edge to center to edge trend in Jsc. However, this variability can not be identified as a statistically significant trend because of the limited size of the sample set and the added complexity when considering corners and sides in addition to a

potential top to bottom dependence. An 8.5% front to back position dependence for cell Jsc is a statistically significant trend even without the ability to compensate for the high top to bottom variability. A 3.6% front to back position dependence for cell FF is a statistically significant trend. A 12.6% front to back position dependence for cell Eff is a statistically significant trend and is consistent with the contributions from Jsc and FF.

The only statistically significant position dependent trend for slice data is a very small, 1.5%, front to back trend in Jsc. In addition, the FF for interconnected slices is consistently lower than for cells by about 7.5%. Although it may exist, the front to back change in FF observed for cells is not statistically verifiable for slices. Because of the small data set, slice FF data that is particularly low relative to other slices (probably as the result of module integration or local issues) can not be eliminated to further explore this potential position dependence.

It is appropriate to consider trends in any parameter for separate cell and slice measurements. It is also appropriate to compare the absolute value of Voc and FF for cells and slices measured at different times using different equipment. However, comparing the absolute value of Jsc and Eff for cells and slices is particularly problematic. With this preface and support from quantum efficiency data that is presented later, the IV data for cells and slices imply the following:

- Minimal change in Voc with position, front to back and top to bottom, implies that the back of the absorber layer, the front of the absorber, the CdS buffer and the ZnO are quite uniform over this 1x4 plate.
- Jsc varies from front to back (~8.5%) implying an electrooptical variation in the absorber.
- There appears to be a top to bottom (or edge to center to edge) variation in Jsc that is at least as significant as the front to back dependence; however, the character and consistency of this variation can not be statistically verified or quantified using this data set.
- The small but statistically significant variation in Jsc for slices is the result of a front to back variation in absorber properties that is partially masked by series connection. The larger top to bottom i.e. edge to edge variation is also masked.
- The small front to back variation in FF for cells probably also exists for slices but this can not be statistically demonstrated for this data set.
- The front to back FF trend for slices and the potential implications for module Eff is unimportant in comparison with the approximately 7.5% lower FF for interconnected slices. Although other issues related to cell integration into modules could explain part of this variation, a significant portion of the lower FF is possibly due to top to bottom variability in current density (~16%).
- Even for a relatively uniform 1x4, local performance improvements on the order of 7% to 12% (based only on Jsc and FF trends rather than more problematic data) are possible for further improvements in uniformity. The edge to center to edge variability is more important than the front to back variation.

Normalized Quantum efficiency data obtained for a subset of the cells indicates performance variations for slices in two wavelength ranges - long and short wavelengths relative to the peak at about 620 nm (Figure 18). Performance variations for the extreme slice positions, for slice 1 and slice 7, are displayed in Figure 19 and Figure 20. This data illustrates variation in the QE peak, the front to back QE variation and an additional systematic edge to center to opposite edge variation in peak QE. Statistical analysis of these three zones in the QE data was done based on the peak QE and two integrals - the integral (with unity flux per wavelength) of QE above 620 nm and a similar integral below 620 nm. The results for the long and short wavelength regions are displayed in Figure 21. Variation in the peak QE and the QE at long wavelengths is well correlated with position while there is no correlation for short wavelengths.

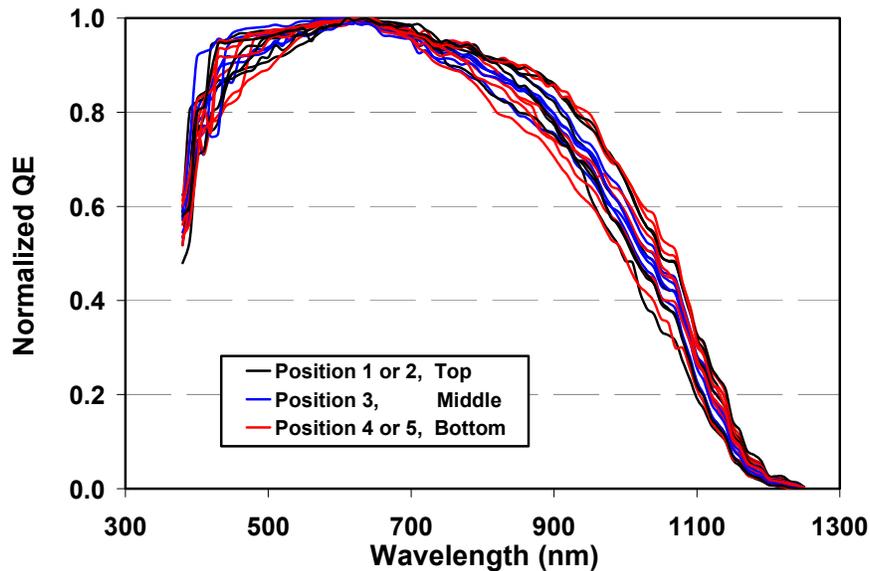


Figure 18. Normalized quantum efficiency.

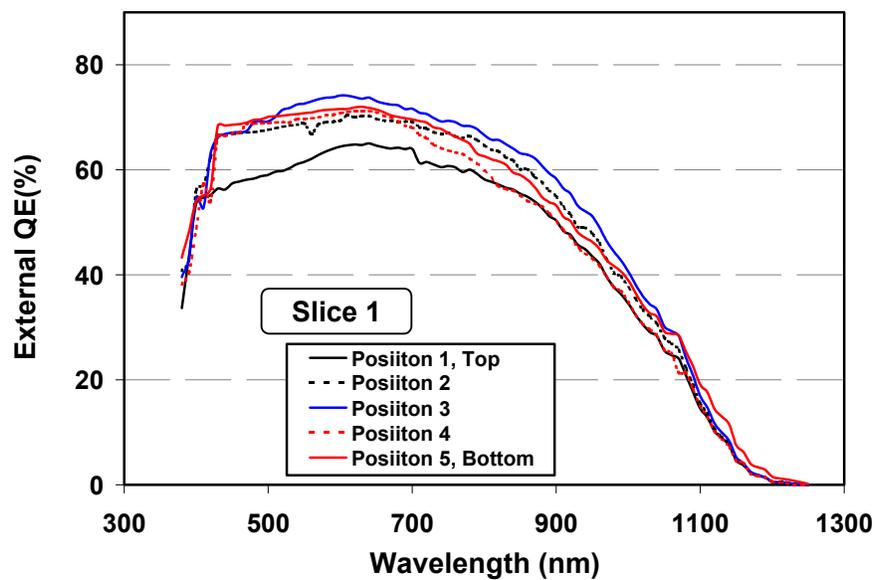


Figure 19. External quantum efficiency for Slice 1.

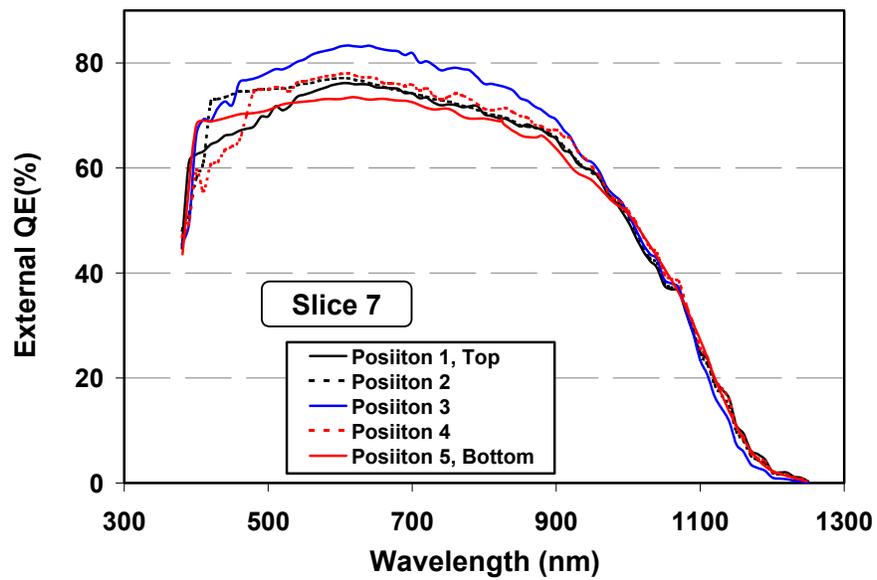
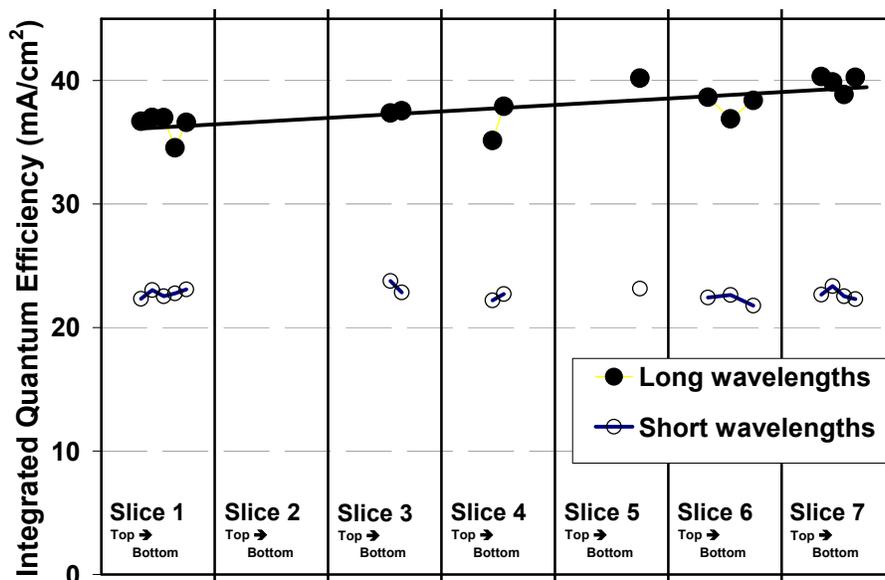


Figure 20. External quantum efficiency for Slice 7.



**Figure 21. Cell response above and below 630nm
- front to back and top to bottom in a reactor.**

The intercept on the energy axis of the square of quantum efficiency versus photon energy is taken as a measure of optical bandgap. This bandgap data is actually a qualitative measure of device structure since the measured bandgap is a convolution of the affects of absorption and collection through the varying bandgap structure of absorbers. Previous experience indicates that the primary variation is in the sulfur profile; however, the Ga profile can also be effected.

The data used to determine bandgap for all cells and the linear interpolations determined for the highest and lowest bandgaps are displayed in Figure 22. A vary narrow range in the bandgap corresponds to a relatively large differences in QE throughout the long wavelength range. This is consistent with a graded structure where the QE depends more strongly on the region with the lowest bandgap in the absorber structure rather than on the graded regions.

The bandgap is well correlated with long wavelength QE, peak QE, Jsc (Figure 23), Eff and position (Figure 24) but is not correlated with the short wavelength QE. This indicates that the front to back variation in Jsc is due to elemental profile variation in the absorber. Correlation with the peak QE indicates that variation in the absorber that has a significant impact on long wavelength QE also degrades the full spectrum QE (this is not necessarily the sole source of an impact on the full spectrum QE). This may be due to a lower elemental gradient and thereby lower field or degradation of overall transport properties.

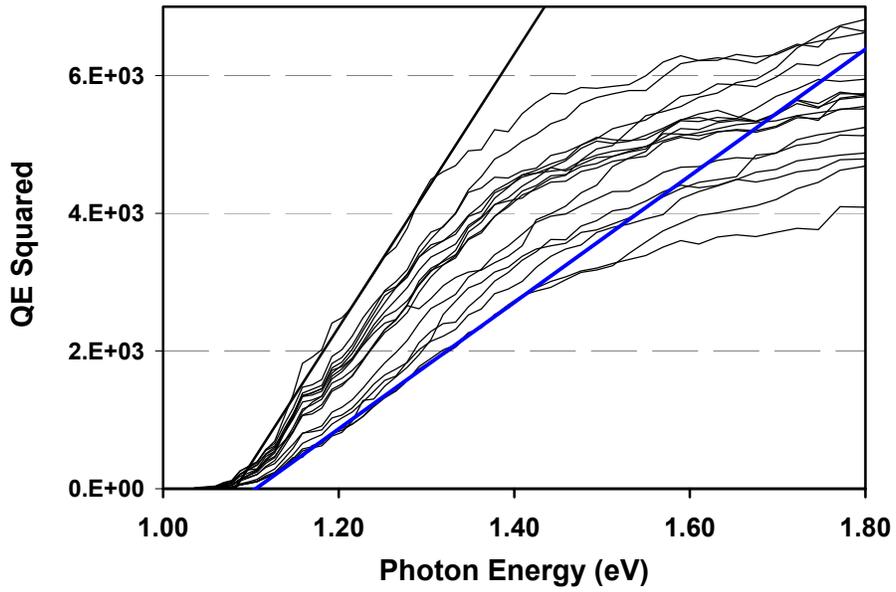


Figure 22. Breadth of long wavelength QE performance and the linear interpolations used to determined the highest and lowest bandgaps.

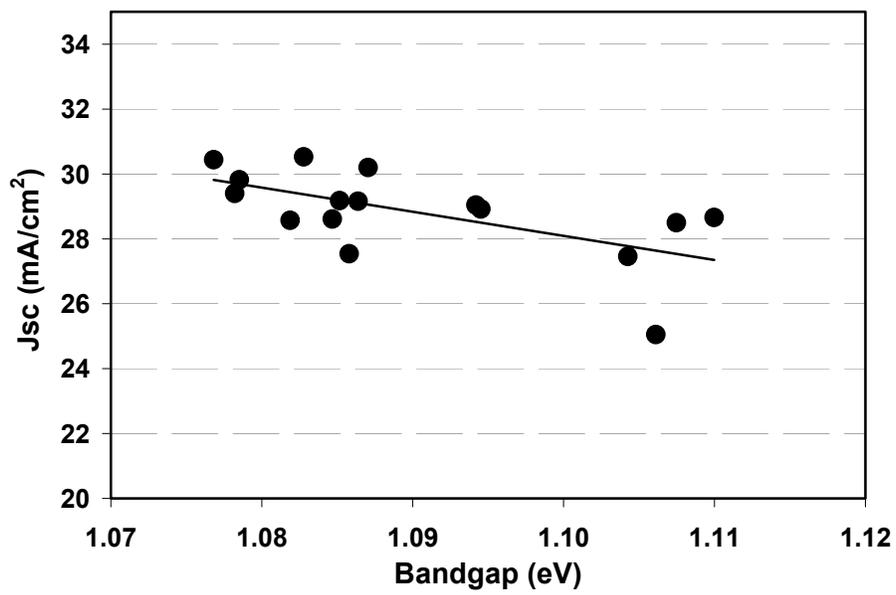


Figure 23. Correlation between bandgap and Jsc.

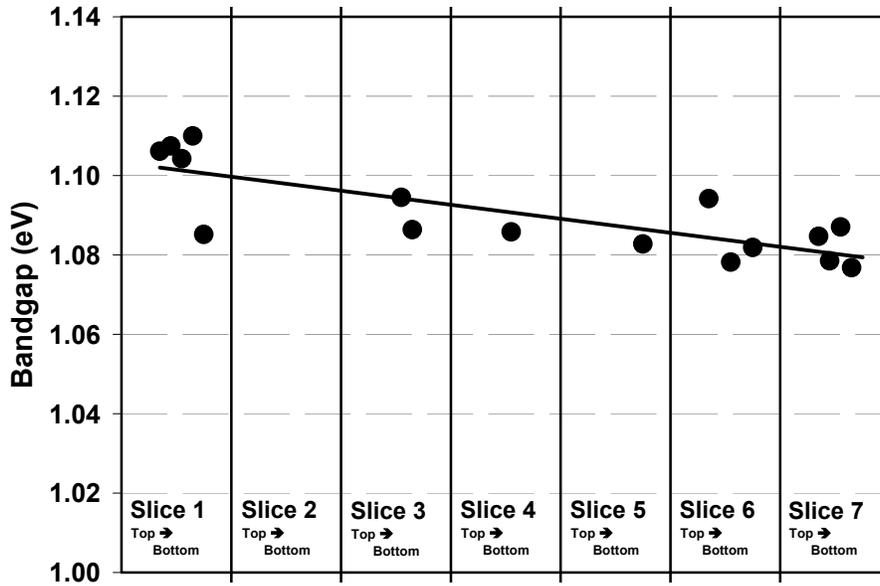


Figure 24. Correlation between bandgap and position - front to back in a reactor.

Although there is not adequate data available for a statistical analysis, the QE data for Slice 7 (Figure 20) and to a lesser degree the QE data for Slice 1 (Figure 19), indicates that the peak QE is degraded at the edges relative to the center. This degradation occurs without a large change in bandgap (Figure 19) or a change in bandgap that is even counter to the front to back changes (Figure 20). The front to back and the edge to center to opposite edge variations are distinct and superimposed. Therefore, the edge to center to opposite edge variation is likely a degradation of overall transport properties rather than a lower elemental gradient and thereby lower field. The front to back variation is related to differences in elemental profiles while the edge to center to edge variation is likely related to the impact of different conditions within the reactor on overall transport properties.

It is important to note that the variations discussed in these studies are already expressed in the reported production data – both efficiency distributions (Figure 9) and yield data (Figure 11). The efficiency distribution is already narrow (full width of about 11% of the average). Identifying and addressing issues determined in these studies will allow improvement over already record results.

Transient effects

SSI is pursuing process R&D to decrease or eliminate transient effects. This is to address issues that are primarily related to production rather than long-term outdoor stability. Although field failures associated with particular production timeframes, package designs and errors during production have been clearly identified, there is no evidence that transient effects, with relatively short time constants, impact intrinsic stability or long-term outdoor durability. Thermally induced transients are observed after exposure to high temperatures in the dark during accelerated environmental testing. Thermally induced transients are not observed in the field

despite daily and seasonal changes in module temperature. This is entirely reasonable since the magnitude of thermally induced transients during accelerated testing decreases when testing is done with illumination, known transient effects are temperature dependent and the module temperatures reached for actual deployment are less than the temperatures defined for accelerated testing.

However, transient effects are an important issue for production since they complicate all activities related to measurements: product ratings, definition of measurement protocols, accelerated testing, analysis for process definition, analysis of process predictability, interpretation of experimental test results, interpretation of outdoor test results, and analysis for understanding of device structures. For example, measurements after a thermal stress are typically made after a two-hour outdoor exposure when conditions allow exposure over 1/3 sun. This timeframe provides significant but incomplete recovery and the degree of recovery depends on weather conditions. Variability in the exposure introduces some uncertainty in the measurements that must be compensated for in experimental design. The two hours exposure is an awkward extension of measurement time when many modules need to be measured for production or R&D.

SSI independently and in conjunction with TFPPP team activities has pursued improved understanding of transient effects. Transient effects are difficult to quantify since the magnitude and time constant for transient effects are dependent on processing, handling, light exposure history and measurement protocols. Significant progress has been made through NREL TFPPP teaming activities. Team accomplishments that have been previously reported included:

- Characterization of transient effects
- Definition of a repeatable measurement methodology for systematic study of transient effects
- Demonstration that some potential causes for the effect are not dominant and directed efforts accordingly
- Improved understanding of the effect and CIS devices
- Demonstrated and communicated that transients are important to consider when measuring CIS
- Demonstrated long term stability for normal operating conditions
- Demonstrated process approaches that influence this effect and may eventually mitigate or eliminate the effect, particularly buffer layers and “partial electrolyte” treatments (solutions used during buffer layer deposition)
- Defined areas for future study

Investigation of the impact on transient effects for several processes steps and processing conditions have continued during this subcontract period:

- Environmental exposure between process steps - Reducing the exposure to ambient humidity before and after the CdS deposition significantly reduces lamination transients.
- Buffer layer variations - Thicker CdS decreases transients while partial electrolyte soaks apparently have no effect.

- Reactor process parameters – Studies for limited variations in process parameters, such as the degree of sulfidation, indicate a dependence on this absorber formation parameter.
- Positions within reactors – Initial results indicate that transients can be, but are not necessarily, dependent on position within a reactor.
- Differences between reactors
- Higher lamination temperature leads to larger magnitude reversible changes in device parameters, particularly FF.
- Various coatings on circuit plates before lamination that are typically used to inhibit moisture ingress may also influence the magnitude of transient effects.

The following expands on some of these studies.

Transients effects were analyzed for samples from multiple baseline absorber formation runs made in four reactors. As seen in the following photograph of a reactor for 1x4-foot circuit plates, Figure 25, a group of substrates is loaded in a carrier, placed into the tube reactor, and processed as a batch. The position of 1x4 circuit plates within the reactors was explored by selecting a central plate and a plate from near the outside of the carrier. The dependence on position within the reactor parallel with the long edge of a 1x4 circuit plate, from the door (front) to the rear of the reactor, was explored by dicing each 1x4 into seven “slices” – each a monolithically integrated sub-module. The end and center slices were laminated while sections of other slices were used for ICP analysis. Each laminate was subjected to nominally 1,000 hours at 85°C and ambient humidity. These simplified accelerated test conditions for laminates have been found to predict behavior through standard high humidity accelerated testing for package designs that provide good protection from water vapor ingress.

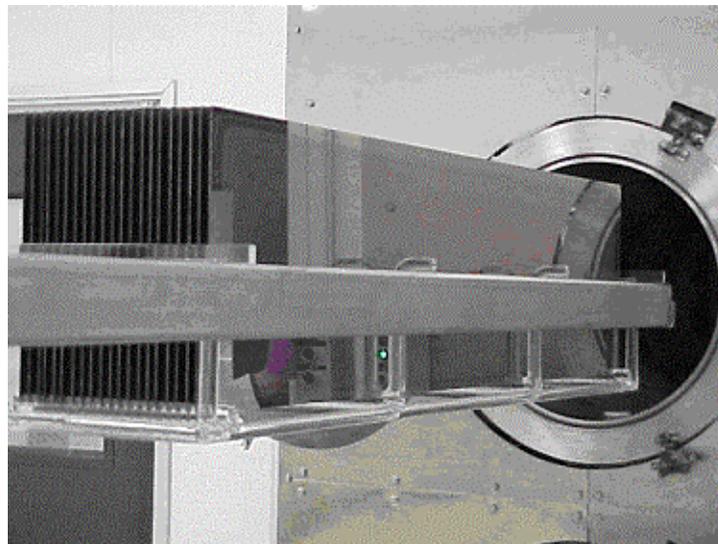


Figure 25. Reactor for 1x4-foot circuit plates.

IV measurements before and after these accelerated test conditions were made after 2 hours of outdoor exposure at over 1/3 sun. This light exposure provides partial recovery from processing or accelerated testing induced transients and was taken as the standard light exposure history state to characterize the degree of thermally induced transients for these investigations. A correlation is assumed, but not demonstrated, between this method of characterizing transients and the power retained after accelerated testing and long term light exposure to fully reverse transient losses.

Results indicate differences between reactors and differences with position within the reactors that ranged from minimal to significant. Typical of transient effects, differences in power were dominated by differences in FF. Post thermal exposure data normalized to pre-exposure data for reactors with minimal and significant thermally induced transients are plotted in Figure 26 and Figure 27. In general for all reactors, the door end introduces smaller thermally induced transients than the rear. Similarly, smaller thermally induced transients are generally observed for circuit plates from the outside of the carrier. For limited studies, there was no apparent correlation between sulfur or sodium levels and the relative position dependence of transient effects.

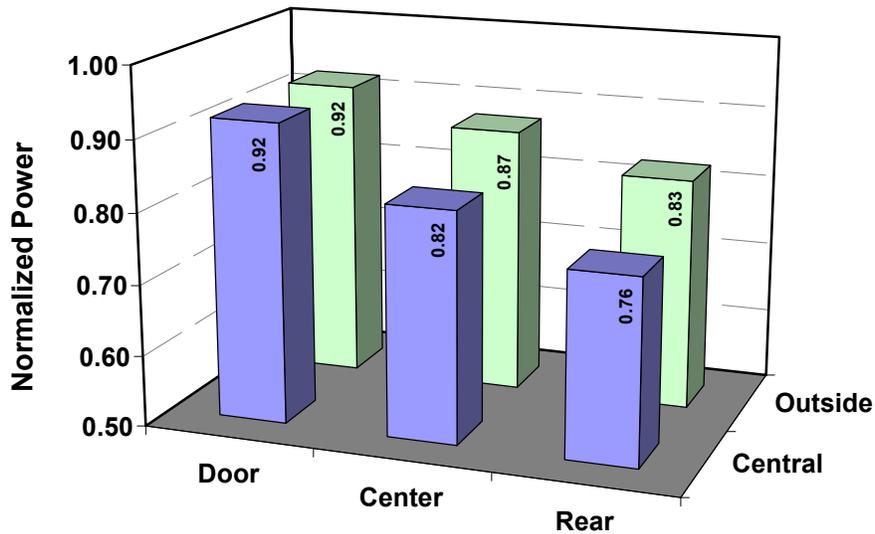


Figure 26. Position dependence of transient effects - reactor with significant variation.

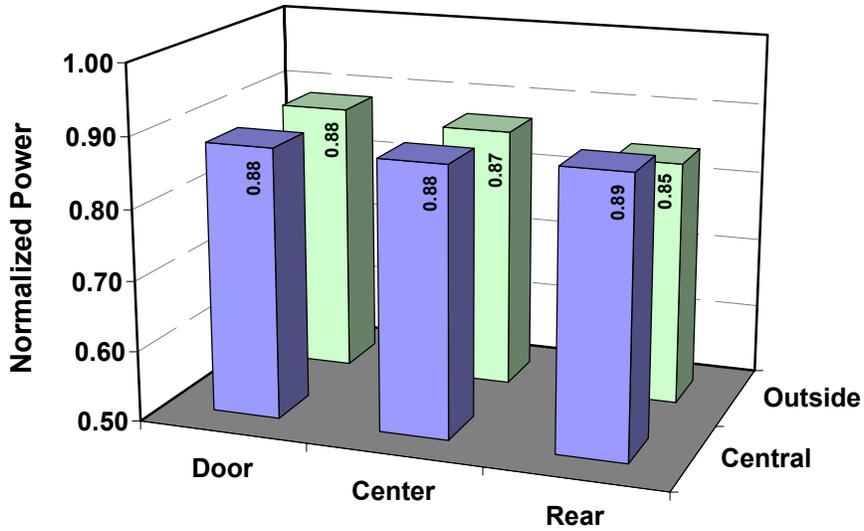


Figure 27. Position dependence of transient effects - reactor with minimal variation.

The impact of purposely varied sulfur content on transient effects was also explored. Performance versus time at 85°C and ambient relative humidity was tracked for a small number of circuit plates processed using baseline H₂S concentration, 25% of the baseline concentration and 200% of the baseline concentration (Figure 28).

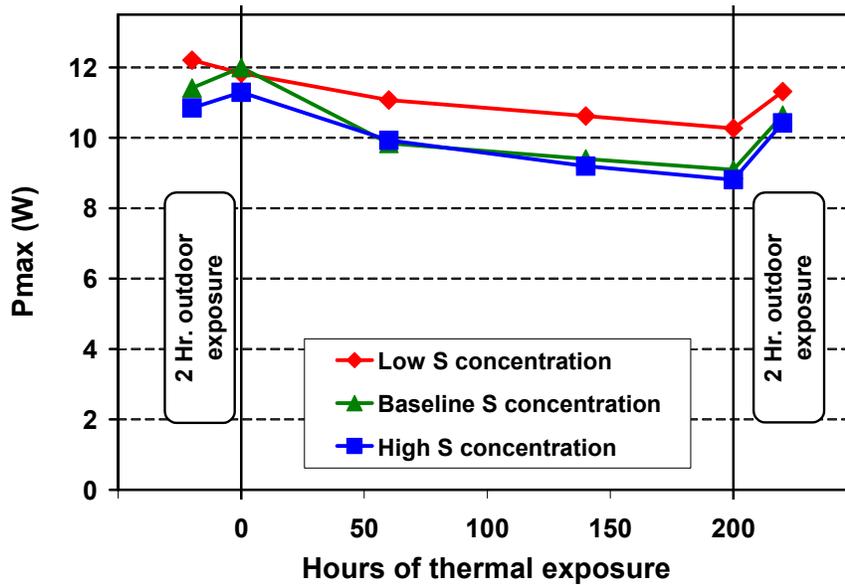


Figure 28. Impact of sulfur content on transient effects.

In contrast with the other two process and typical results, circuit plates processed with 25% of the baseline H₂S concentration declined with outdoor exposure prior to the thermal exposure.

Therefore, the starting point chosen for normalization determines the relative stability of the circuit plates in this test. Choosing the measurement after lamination and 2-hour outdoor exposure for normalization, as is typically done, indicates that the circuit plates processed with a lower sulfur content perform better through thermal exposure. There is no indicated difference between the processes for normalization to the measurement before the outdoor exposure measurement. Modifying the sulfur content may utilize a process degree of freedom to minimize if not eliminate transient effects.

The impact of purposely varied sodium content on transient effects was also explored during this subcontract period. Performance after an extended exposure at 85°C was compared for samples fabricated with low sodium (about an order of magnitude lower than typical) and samples from the previously discussed experiment to explore the dependence on position within reactors. ICP analysis was used to determine sodium concentrations. For the relatively small variations in nominal sodium concentration with reactor position, post thermal exposure data normalized to pre-exposure data indicated a weak trend in thermally induced transients with sodium concentration that could not be statistically verified at the 95% confidence level. Samples purposely fabricated with very low sodium content were much more sensitive to thermal exposure; however, the initial efficiency was also very low and the significance of this result or a comparison with baseline material is uncertain.

As with power module measurement, transient effects are very important for minimodule production since they complicate all activities related to measurements. Subcontract efforts have included addressing transient effects while developing the capabilities necessary to measure each minimodule in a few seconds.

National CIS R&D Team

Prior to and during this subcontract phase SSI contributed to TFPPP National CIS R&D Team activities. Summarizing results for all of the extensive team member activities is not attempted in this report since the expertise for most team activities resides with the team members. Instead, the following experiments are summarized as examples of teamwork where SSI has had major involvement in sample preparation or data analysis.

Vasilis Fthenakis, head of the National Photovoltaic Environmental, Health and Safety Assistance Center at Brookhaven National Laboratory, visited SSI on May 29. A review of SSI's process was supplied in advance and Vasilis toured the CIS facilities. The tour emphasized safety systems and Vasilis reviewed the "Process Hazard Analysis Photovoltaics Checklist" that he developed for the Photovoltaics community.

In sample exchanges related to TFPPP team activities, device performance has varied for SSI absorber with buffer and ZnO depositions by NREL or IEC. Consistent good performance for the same sample set has been obtained for SSI absorbers with CVD and ZnO deposited by SSI. During this subcontract period, Kannan Ramanathan provided the team with a summary of related information and new photoluminescence data indicating a difference in the peak PL signal for devices completed by SSI and NREL.

Kannan Ramanathan and Raghu Bhattacharya at NREL have made progress on depositing CBD ZnS buffer layers on SSI absorbers. SSI supplied baseline absorber layers to NREL, NREL deposited the ZnS buffer layers, CVD ZnO was deposited at SSI, gridding and measurements were done at NREL. Good small area devices have been fabricated with one CBD ZnS deposition and no subsequent anneal whereas both multiple depositions and an anneal were previously required. Multiple devices with efficiencies over 11% have been fabricated on SSI absorbers that produce 14% devices with a CdS buffer layer. Mixed results were obtained for annealing at 200°C.

Samples of SSI absorbers from standard production processes and samples with process variations were sent to Sally Asher, NREL, for analysis. Comparing results will aid process development at SSI and will likely advance the fundamental understanding of CIS-based materials and devices. Rather than requesting specific measurements, SSI and NREL are collaborating on the best surface and bulk measurements to characterize the samples and differences between the samples. SIMS elemental profile data, including analysis of Na, is of particular interest for developing understanding of the impact of elemental profiles on device performance – both efficiency and transient effects. Samples with CdS, without CdS and with thicker CdS were included in the sample set to explore the impact of CdS deposition on surface properties and performance. Another area of interest is characterization of dark spots. Initial results indicated that elemental profiles are nearly identical for the dark spots and “typical” areas. Although dark spots do not have a significant impact performance, they are a cosmetic issue and should be eliminated.

SSI has supplied minimodules and various configurations of 10x10 cm samples for work on barrier coatings by Larry Olsen’s group at PNNL. The possibilities for this technology range from alternative encapsulation options for consumer products with minimal environmental protection requirements to enabling low cost PV products with very long lifetimes. These barrier coatings were originally designed for flat organic light emitting diode (OLED) panel displays that are very sensitive to water vapor and oxygen ingress. As discussed in his paper presented at the most recent National Center for Photovoltaics and Solar Program Review Meeting, initial results are very encouraging [16]. As seen in Figure 29, comparing IV characteristics for coated and uncoated circuit plates that went through accelerated environmental test cycles indicates protection of circuit plates from moisture ingress. This protection can be defeated if the conformal coating is interrupted by steps in the thin films, debris from cutting samples and handling, and surface features that are sometimes associated with dark spots on SSI circuit plates. Although cost estimates have not been obtained, the cost of these vacuum deposited multiple layer coatings may be prohibitive. Fewer layers or other potential process variations may provide adequate protection and be cost effective.

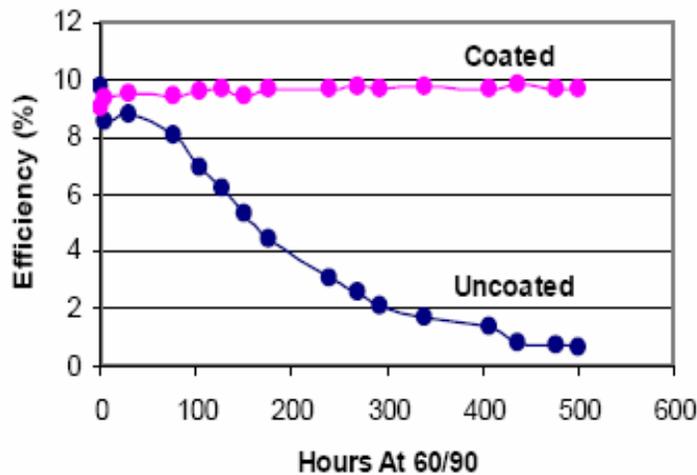


Figure 29. Comparison of accelerated testing results for coated and uncoated minimodules. (From L. Olsen, et al., “Barrier Coatings For Thin Film Solar Cells”, National Center for Photovoltaics and Solar Program Review Meeting – 2003)

Additional team activities included:

- As discussed above, SSI independently and in conjunction with TFPPP team activities has pursued improved understanding of transient effects
- SSI deposited CVD ZnO on multiple sets of samples with experimental buffer layers from Larry Olsen, WSU.
- Dale Tarrant attended the National CIS R&D Team Meeting, NREL Visitor's Center, January 30-31, 2003 and presented a talk on the status of CIS R&D at SSI. Actual and projected production capacity, yield and cost data were presented. General plans for glass/glass packaging were also discussed.
- Steve Voss attended the National Thin Film Module Reliability Team Meeting "Failure Mechanisms", February 27-28, 2003 at Florida Solar Energy Center and presented a talk titled “Accelerated Environmental Testing of Shell Solar CIS”.
- Steve Voss attended the National Thin Film Module Reliability Team Meeting, Sandia National Laboratory, September 18 and 19, 2003 and presented at talk titled “Thermal and Field Stability of Shell Solar CIS”
- SSI supplied samples to Larry Olsen’s group at PNNL for testing multi layer barrier coatings – discussed above.
- SSI carried out UV exposure testing for devices with barrier coatings from PNNL that were previously exposed to high humidity accelerated testing.
- About 60 Mo coated 10x10 cm glass substrates were sent to Seokhyun Yoon, a graduate student working with Tim Anderson at the University of Florida, for CIS studies in conjunction with TFPPP team activities.

- About 40 Cu(In,Ga)(S,Se)₂ absorber layers on 10x10 cm glass substrates were sent to Tim Anderson at the University of Florida, for laser processing experiments in conjunction with TFPPP team activities.
- SSI supplied Mo coated 10x10 cm glass substrates to Angus Rockett, University of Illinois, for CIS studies in conjunction with TFPPP team activities.
- SSI deposited CVD ZnO on multiple sets of samples experimental absorbers for Unisun.
- SSI patterned Mo coated glass was supplied to Unisun.
- SSI supplied absorbers to Kannan Ramanathan for experiments varying CdS process parameters at NREL with SSI baseline ZnO depositions. The goal is to understand fill factor and open circuit voltage differences for SSI absorbers processed at SSI, NREL and IEC.
- NREL representatives Sally Asher, Kannan Ramanathan, Carl Osterwald and Harin Ullal visited SSI on June 10, 2003. The primary topic was working with NREL with emphasis on learning about environmental issues by deploying modules in multiple environments. SSI will provide materials as appropriate for NREL “baselining” activities associated with developing tools or accelerated tests that predict long term performance.
- Mini-modules gridded and measured at PNNL and the associated data were sent to Kannan Ramanathan, NREL, to explore the possibility of doing similar gridding on sections of monolithically integrated modules at NREL. These minimodules were then passed on to David Albin, NREL, as the beginning of “baselining” activities at NREL for environmental studies.

Package Development

Outdoor testing

Experience indicates that intrinsic stability and long-term outdoor durability of CIS modules can be assured through packaging development. Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules with multiple prototype package designs have undergone testing for over fourteen years. However, field failures have also been observed. Losses are not inherent to CIS since multiple past and present module deployments, typically in 1 kW arrays, have demonstrated stability.

When losses have been observed, a range of module performance, including no losses, have been observed. Some failure mechanisms related to particular package designs and errors during production have been clearly identified. Other subjective observations imply that additional circuit plate or packaging process variables may have affected durability during particular production timeframes. As discussed in the previous annual report, if losses were observed, the losses are best correlated with date of deployment or prototype module configuration. Results have demonstrated the proof of concept for stability and long-term outdoor durability. Lower cost package approaches are available but require development.

As discussed in a previous section, transient effects complicate all activities related to measurements, in particular the interpretation of outdoor test results and measurements related to package development. It is difficult to make conclusive statements about correlations or casual relationships between transient effects and other observations because the magnitude and time constant for transient effects are dependent on processing, handling, light exposure history and measurement protocols. However, the best data to date indicates that, although field failures associated with particular production timeframes, package designs and errors during production have been clearly identified, there is no evidence that transient effects impact long-term outdoor stability. Thermally induced transients are not observed in the field despite daily and seasonal changes in module temperature.

SSI installed and dedicated a 245 kW CIS thin film array on the roof of one of its manufacturing building (Figure 30). The system covers more than 31,000 square feet and contains 6144 modules. Installed with support from the CEC rebates, SSI receives economic benefits from the power produced by the installation. Environmental and economic benefits of PV are showcased by this array and it is an example of the use of CIS for SSI customers.



Figure 30. SSI's new 245 kW CIS thin film array.

An innovative systems design approach for the CIS array was employed to evaluate a new modular array support structure for flat commercial roofs and to evaluate optimization of array output based on utility rate schedules. The support structure is a modular design for simplified installation and utilizes inexpensive light gauge cold-formed steel c-channels. Roof penetrations are minimized even with an open-rack design that allows for cooling. The robust structure is capable of withstanding 80 mph winds and meeting zone 4 earthquake resistance requirements. System design is optimized by comparing tilt and azimuth dependent hourly and seasonal array output with local utility rate schedules.

SSI received a test report titled “Siemens CIGSS 1kW System PVUSA Power Rating Performance” from Jill Adelstein, NREL (attached). Data acquisition began on November 18, 1998 for this third 1kW array of prototype modules. The system is comprised of 28 modules with an average efficiency of 11.4% at STC. A linear fit to PVUSA power rating versus time data indicates degradation at a rate of about 3.4% per year.

Reasons for the degradation in this array, actually some modules in this array, have been at least partly explained by studies of this array and other prototype module arrays deployed by SSI during the timeframe that this array was deployed. As discussed in the most recent annual report, the presence of any significant loss in this array is best correlated with module configuration or date of deployment. Some failure mechanisms, such as improper use of lay-up tape and dirt buildup for wide frames, have been clearly identified. Other subjective observations imply that additional circuit plate or packaging process variables effected long-term stability for pre-production modules produced in the timeframe when wider frames, as for this array, were standard. A range of array performance from improvement through losses is observed for the timeframe where arrays might show significant losses. Also, within the arrays that show losses, particularly this array, there is a range of module performance including no significant loss.

As Phase I deliverables, SSI shipped 60 modules to NREL for use by the TFPPP “Outdoor Testing and Monitoring of Thin Film Modules in Hot and Humid Climates” program. After characterization at NREL, these modules will be deployed at the Florida Solar Energy Center. An additional set of 60 modules, as Phase II deliverables, will be sent to NREL for this program and deployed at Texas A&M.

Glass/Glass Package Development

Progress toward developing glass/glass packages has been made using 40W circuit plates. New packages are required to pass accelerated environmental tests such as the damp heat test - an exposure for 1,000 hour at 85°C and 85% relative humidity. No detectable humidity ingress occurs during damp heat testing of the current SSI products with a TPAT backsheets. However, humidity penetration during accelerated tests was observed during testing of initial glass/glass package designs [17]. Very promising results have now been demonstrated for prototype packages with an edge seal developed in collaboration with the new NREL sponsored National Thin-Film PV Module Reliability Team. Prototype 40W circuit plates packages incorporating this edge seal have passed accelerated tests, including the damp heat test.

Various package design options were explored including variation in edge seal type, edge seal width, EVA thickness and lead routing. In addition to a barrier to humidity ingress, the edge seal chosen solved problems during lamination; breakage of the circuit plate due to compression of the laminate edges was eliminated. This allowed simplification of the process by eliminating the need for fixturing during lamination and allowed the use of thinner EVA thereby reducing materials cost.

Testing of new package designs has included exploring the importance of the frame. No detectable humidity ingress occurs during damp heat testing of current framed products. However, unframed laminates made using the present production design with a TPAT backsheets

do not perform well through high humidity accelerated testing. In addition to a moisture barrier, the frame may keep the laminate and interfaces under compression. This is not the case for the glass/glass package under development; there is no statistically significant difference between framed or unframed laminates exposed to high heat and high humidity or unframed laminates exposed to high heat.

Results from these studies of the importance of the frame also provide a potential explanation for some field failures. As reported in the previous annual report, destructive testing found that tape used during lay-up for lamination was at times used improperly and that this was potentially the cause for some field failures. Even when used properly, this tape leaves depressions bordered by thicker than normal regions in the TPAT/EVE/glass structure at the edge of laminates – where the frame captures the laminate. These regions may be the equivalent of unframed sections of the present production module design with a TPAT backsheets that, without a frame, did not perform well through high humidity accelerated testing. These regions may interfere with the frame providing a moisture barrier or keeping the laminate and interfaces under compression.

Experiments have been conducted to explore the effects of lamination temperature and EVA gel content on thermal stability i.e. transient effects. Measurements were made before and after accelerated testing at elevated temperature followed by a two-hour light exposure. No statistically significant effects were observed for laminations temperatures of 120, 130 and 140°C with gel contents targeted at 65% and 80%.

Progress developing and testing glass/glass packages using single 40W circuit plates are being extended to a new higher power product, the ST80. Figure 31 is a sketch of the proposed ST80 glass/glass package. Two nominally 40W circuit plates are laminated to a common tempered glass front sheet. Laser edge deletion, removal of all films forming an approximately 1 cm border, provides electrical isolation from the frame. The edge seal developed in collaboration with the new NREL sponsored National Thin-Film PV Module Reliability Team is used at the perimeter of both plates.

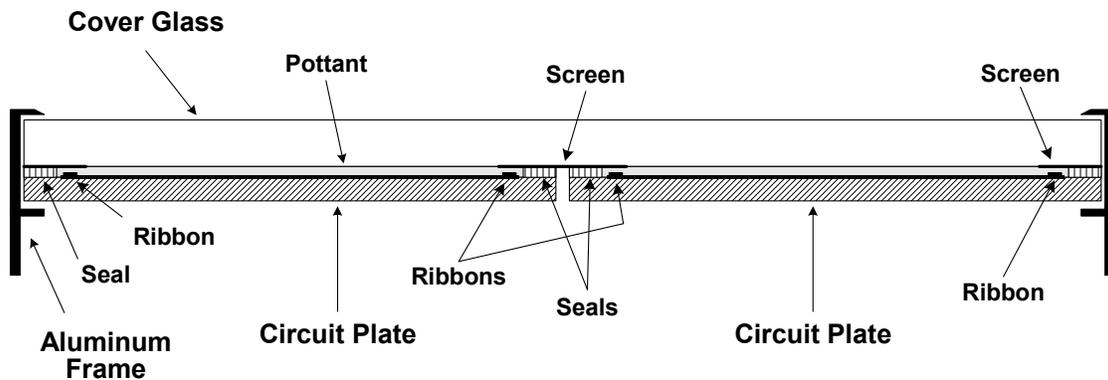


Figure 31. Proposed ST80 glass/glass package.

Figure 32 illustrates the layout of the circuit plates, buss bar ribbons and a printed circuit board (PCB) that connects the circuit plates and routes power to a junction box on the back of the module. A screen in front of the ribbons, Figure 31 and Figure 32, is included to achieve an aesthetically pleasing uniform black appearance.

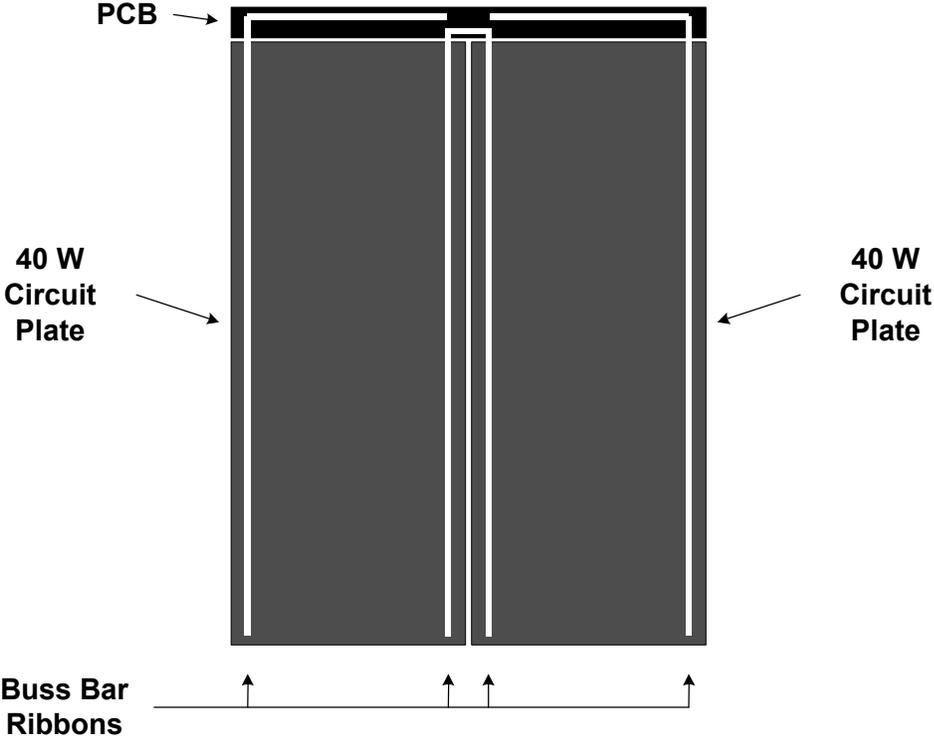


Figure 32. Lay-up of two circuit plates.

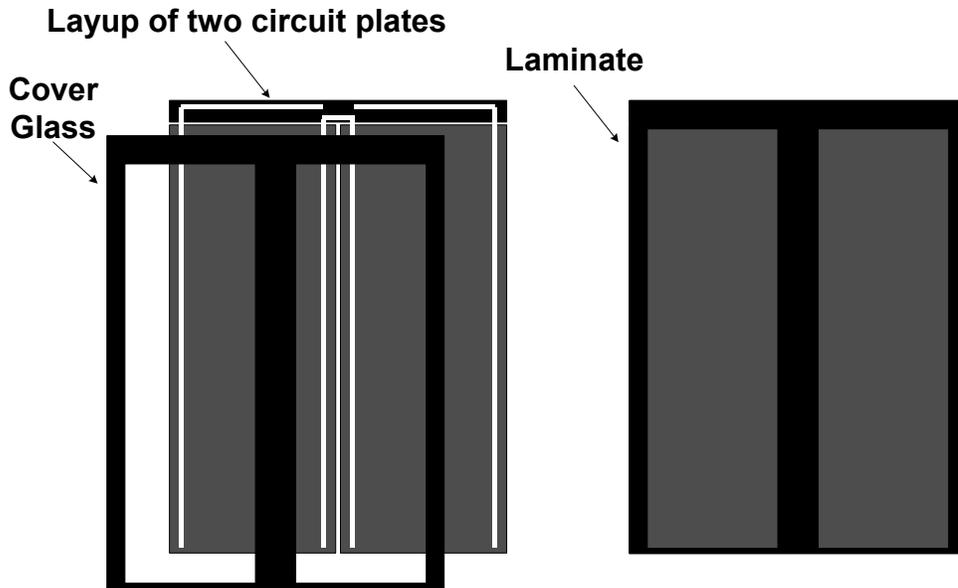


Figure 33. A cover glass with screen achieves an uniform black appearance.

Package process development for minimodules led to the discovery of a corrosion mechanism in minimodules that may also be a consideration for some low cost and very long lifetime power module package options. Corrosion of the Mo in the area of ZnO patterning is observed because minimodule package approaches do not protect the circuit from water vapor ingress as well as package designs for power modules. This corrosion is observed if both the ZnO and CIS are removed, as is done during mechanical patterning. However, corrosion does not occur if only the ZnO is disrupted and the CIS remains largely intact.

Alternative patterning strategies that were previously developed to avoid near-interconnect adhesion problems are applicable to the minimodule corrosion issue [1]. These patterning approaches were not previously adopted since preferable changes in other absorber formation processes solved the near-interconnect adhesion problems. Some of the alternative patterning approaches included deposition of an insulator over part of the interconnect and subsequent deposition of ZnO over the insulator. A class of materials tested as potential insulators was found to suppress ZnO growth. This led to new patterning approaches based on growth suppression rather than patterning the ZnO. One of these approaches was effective in addressing the current minimodule corrosion issue since the CIS remains intact (Figure 34). In addition, this type of approach may be valuable for alternative large area package designs if a similar corrosion mechanism occurs that is not seen for present designs.

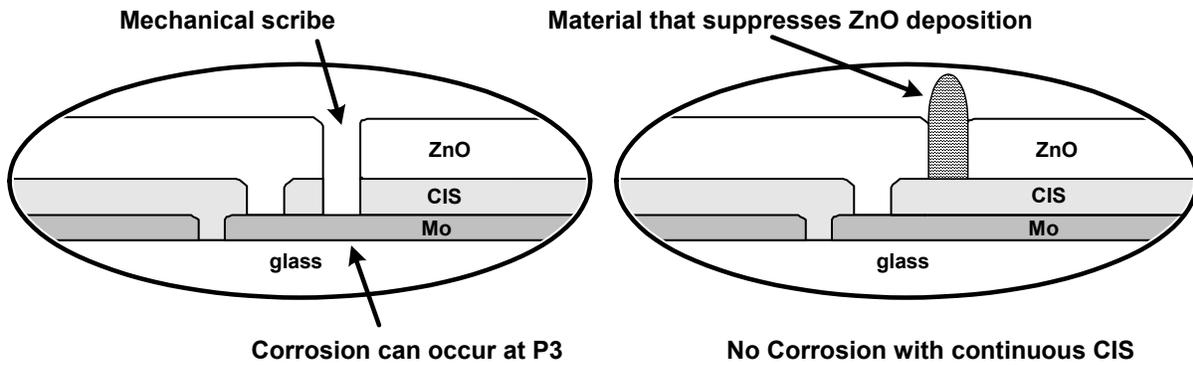


Figure 34. Corrosion avoided when P3 is formed by suppression of ZnO growth rather than mechanically.

Additional results:

- Previously discussed results indicating differences in transients depending on the position of 1x4 circuit plate within reactors.
- Improvements in the dehumidification of cabinets used to hold racks of circuit plates before and after CdS deposition increase the laminate fill factor probably due to decreasing transients.
- Hi-pot testing has illuminated potential problems with arcing between the leads and the circuit plate electrode materials.
- Modifications to the package design to avoid arcing are being explored.

Conclusions

Outstanding progress has been made in the initial commercialization of high performance thin film CIS technology. The following are highlights of accomplishments during this subcontract period:

- Executing the CIS process continues to demonstrate process predictability.
- Cumulative production for 2002 exceeded 1 MW - about twice the production rate for 2001. SSI 2003 capacity was about 3 MW per year whereas production for 2003 was just over 1.2 MW per year. Introducing the new product accounts for the main difference between production and capacity.
- Average laminate efficiency for 2003 was 11.0% with a full width of only 11% of the average. This distribution is nominally the same as the distribution for 2002 but with an approximately 33% increase in production volume.
- Line yield increased from about 60% in 2000 to about 85% in 2002. Maintenance of this high line yield was demonstrated during 2003.
- Process R&D during this and previous subcontract periods, both at SSI and in collaboration with NREL teams, has demonstrated the potential for further cost performance improvements: minimization of transients, increased efficiency and improved packaging.
- Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules with multiple prototype package designs have undergone testing for over fourteen years.
- Field failure mechanisms related to particular package designs and errors during production have been clearly identified. Additional circuit plate or packaging process variables may have affected durability during particular production timeframes; when losses have been observed, the losses correlated with date of deployment or prototype module configuration.
- Prototype glass/glass packages for individual 40W circuit plates have passed accelerated tests, including the damp heat test. This package incorporates an edge seal developed in collaboration with the National Thin-Film PV Module Reliability Team.
- Developing and testing of 40W glass/glass packages is being extended to a new 80W product made using two nominally 40W circuit plates laminated to a common front sheet.

Further device and production R&D can lead to higher efficiencies, lower cost, and longer product lifetime. Production volume, efficiency and yield data supports attractive cost projections for CIS. Prerequisites for commitment to large-scale commercialization have been demonstrated at successive levels of CIS production. Remaining R&D challenges are to scale the processes to even larger areas, to reach higher production capacity, to demonstrate in-service durability over longer times, and to advance the fundamental understanding of CIS-based materials and devices with the goal of improvements for future products. SSI's thin-film CIS technology is poised to make very significant contributions to DOE/NREL/NCPV long-term goals - higher volume, lower cost commercial products.

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