

Novel Power Electronics Systems for Wind Energy Applications: Final Report

**Period of Performance:
August 24, 1999 – November 30, 2002**

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EXECUTIVE SUMMARY

The objective of this work was to develop new approaches to the power electronics of variable-speed wind power systems, with the goal of improving the associated cost of energy. Of particular importance is the converter efficiency at low-wind operating points, where these systems typically operate. Developing converter approaches that maintain high efficiency at partial power, without sacrificing performance at maximum power, is desirable, as is demonstrating an approach that can use emerging power component technologies to attain these performance goals with low projected capital costs.

In this report, we show that multilevel conversion is an approach that can meet these performance requirements. In the wind power application, multilevel conversion proves superior to conventional converter technologies because it is scalable to high power and higher voltage levels, it extends the range of high converter efficiency to lower wind speeds, and it allows superior low-voltage fast-switching semiconductor devices to be used in high-voltage high-power applications. In addition, multilevel conversion reduces switching loss without the need for additional silicon area (thereby improving efficiency at both full load and partial load), and it reduces size of filter inductors. Although the major disadvantages of multilevel conversion are the complexity of its control and its bus bar interconnections, these issues can be addressed using ongoing advances in microprocessor technology.

Attempts by other authors to address the complexity of power interconnections and bus bar construction have been largely unsuccessful or limited in application. We have addressed this issue by proposing a new family of multilevel matrix converters that are modular in design, require simple power interconnections and bus bar configurations, and exhibit high efficiency and good semiconductor switch utilization. We believe that this approach is well-suited to the variable-speed wind power application, where it can improve the cost of energy, and that it can be scaled to higher voltage and power levels. The proposed converters are fundamentally different from known matrix converters, as well as from known multilevel converters, but they combine the positive features of both. We have used simulation to confirm the successful operation of the basic configuration of the proposed new converters.

At first, controlling the proposed converters appears to be quite complex and daunting. But we have also derived a new control algorithm—single-capacitor space vector modulation—that is relatively simple to apply and understand. This approach is, in some sense, optimal, in that it minimizes the circulating currents between capacitors, allowing the converter to operate with relatively high direct power (leading to low conduction and switching loss). Using space vector modulation leads to compatibility with field-oriented control. We believe that this approach also allows the issue of control of DC capacitor voltage levels to be addressed in a relatively simple manner.

We constructed a working prototype system to prove the validity of the converter and of the proposed control algorithm. At 50-kVA output and 50- to 100-kHz switching frequency, the specific cost of the insulated gate bipolar transistors that we purchased was \$7.03/kVA. We have fabricated modular switch cells using a printed circuit board approach for power interconnections. A Motorola PPC555 microcontroller provides the control functions, and we have developed basic core codes to implement the proposed single-capacitor space vector modulation algorithm. The microcontroller is interfaced to the switch modules via complex programmable logic devices and flash memory, and the detailed codes for these devices are documented in the appendices of this report. We have also designed and fabricated filter magnetics. The specific cost of the Metglass inductors that we constructed was \$33.00/kVA for a 10-kHz

switching frequency. This cost could be significantly reduced by increasing the switching frequency or by using multilevel operation at rated load, or both. We have documented the operation of the converter system at a switching frequency of 50 kHz at several operating points.

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1.0

Introduction

1.1 GOALS AND APPROACH

Figure 1-1 illustrates two common approaches to variable-speed wind power generation. In each of these, an alternating current–alternating current (AC–AC) power electronics system interfaces with and converts the variable-voltage variable-frequency AC appearing at generator terminals to the constant-voltage constant-frequency AC of the utility system. To fully realize the potential of variable-speed generation to harvest the energy available over a wide range of wind speeds, all elements of the system must be designed to operate with high efficiency over the entire operating range. Because a typical wind generation system may operate at a fraction of rated power most of the time, attaining high efficiency at light load is critical for reducing the cost of energy (COE) in these systems. This requirement distinguishes the wind power application from nearly all other applications where efficiency at light load is usually much less important than other considerations, such as the efficiency at full load. Although previous work (Erickson, R.; Al-Naseem, O.; Changtong, K. (1999)) has been devoted to optimizing the design of the wind turbine and the machine to meet this requirement, much less work has focused on similar optimization of the power electronics. Furthermore, typical off-the-shelf converters exhibit poor efficiency at light loads. In previous work, (Al-Naseem, O.; Erickson, R.; Carlin, P. (February 2000)) we modeled the losses in a conventional direct current (DC) link system to understand the physical mechanisms that cause this behavior in switching converters. The objectives of the work described in this report were to develop and demonstrate a new approach to the power electronics technology of wind power systems, an approach that addresses these issues and is suited to the unique requirements of these systems.

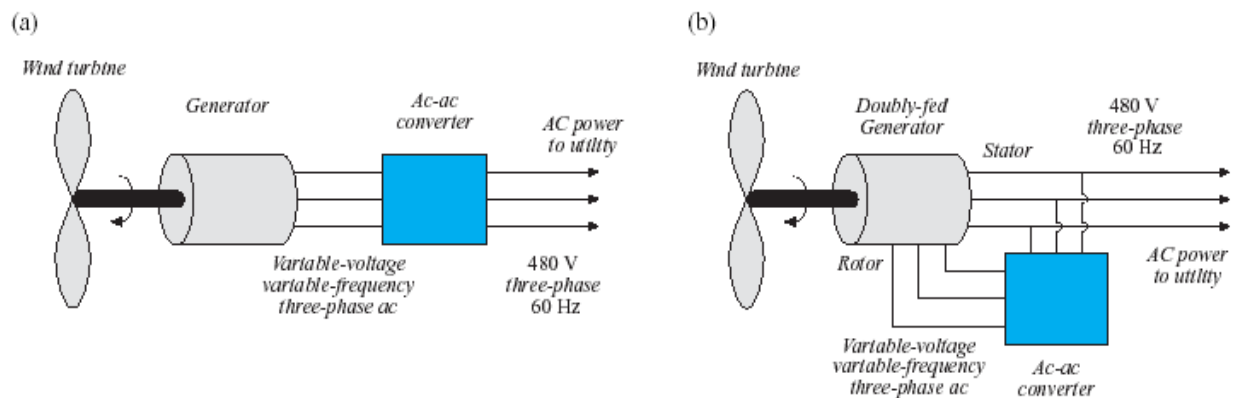


Figure 1-1. Major elements of typical wind power systems: (a) with permanent-magnet or singly-fed induction generator, (b) with doubly-fed induction generator.

In this work, we first applied the results of previous work (Erickson, R.; Al-Naseem, O. (November 2001)) on developing an experimentally verified model of converter losses in wind power applications with a goal of understanding the major origins of losses. These results are summarized in Section 1.2.1. Second, we assessed the state of relevant technologies and their rates of advance, to project the likelihood that they could substantially improve the performance of future AC-to-AC conversion systems for wind power applications. We briefly summarize this assessment below in this section. Third, we considered approaches used to improve converter performance in other applications, and proposed multilevel conversion as a solution well-suited to the requirements of wind power. Next, we developed a new converter that is a hybrid of multilevel and matrix technologies, and that we believe exhibits advantages over previously known multilevel or matrix converter technologies. These results are discussed in Sections 1.2.3 and 1.3, as well as in Chapter 2. Then we modeled and analyzed the proposed new multilevel matrix converter, to develop a practical control strategy and to prove the validity of the converter. Chapter 3 presents these results. Finally, we carried out experimental work to construct and demonstrate a working converter that exhibits high efficiency over a wide range of operating points. In addition to demonstrating the validity of the proposed new family of converters, this experiment also attempts to demonstrate the feasibility of operation with a high switching frequency of 50 kHz, which would reduce the size and cost of reactive filter elements, allow modular construction on printed circuit boards, and attain controlled wave forms of high quality. Chapter 4 gives the details on the modular 50-kW converter.

1.1.1 About Power Electronics Technology

Moore's Law is widely celebrated within the field of electrical engineering. The cofounder of Intel, Gordon Moore, predicted the periodic doubling, and hence exponential growth, of the number of transistors in digital integrated circuits. This has led to today's microprocessors, which have tremendous capability and complexity with relatively low cost. The advance of silicon technology continues to outpace that of all other major technologies.

The technological development of power semiconductor devices has also been very rapid, although not as fast as that of digital silicon technology. Nonetheless, the evolution of power silicon devices greatly outpaces that of other technologies relevant to power electronics. Specifically:

- Magnetics and capacitor technologies have evolved relatively slowly, with only minor incremental improvements in magnetics materials seen over the past 20 years. The incremental improvements in high-current capacitor technologies have had a relatively small impact on the field of power conversion.
- Microprocessor, microcontroller, and gate array technologies have developed very quickly. This enables sophisticated, complex control algorithms to be employed in complex switching converters.
- Power semiconductor technologies have evolved rapidly as well. Recent high-speed low-voltage insulated gate bipolar transistors (IGBTs; 600–900 V, f_s up to 100 kHz); high-voltage medium-speed IGBTs and HVIGBTs (up to 4500 V, f_s up to 1–10 kHz, depending on construction); and high-voltage low-speed gate turn-off thyristors (GTOs) and gate-controlled thyristors (GCTs; 4500 V and higher, f_s up to 1 kHz) are resulting in new power conversion applications with increased functionality and performance.
- Electronic packaging and manufacturing technologies have developed quickly. Highly complex circuitry can be assembled by machine at low cost and high reliability. To some extent, these

technologies can be applied to the power stages of converters, although the voltage and current levels are limited.

This suggests that research and development (R&D) efforts in the power electronics area should take advantage of the increasing capabilities of semiconductor devices, to improve the performance, cost, and functionality of switching converters in wind power applications. Complexity of a given approach is not necessarily a disadvantage; indeed, it may be possible to exploit microcontroller and packaging technologies to attain the desired improvements. Converters that employ more, smaller transistors (with the same total silicon area) are feasible to build, and may exhibit improved functionality or performance without increased cost. Furthermore, it is reasonable to project that the cost of semiconductor devices, including IGBTs and other devices, will decrease in the future; however, similar decreases in the costs of magnetics and capacitors are unlikely to occur without a major breakthrough. This suggests that, in the long term, we should attempt to reduce the size and cost of reactive elements by using silicon, rather than the opposite.

Power semiconductor devices are loss-limited by their packages. For example, an IGBT that is rated at 100 A may be usable only up to 50 A before it fails as a result of excess temperature rise within the silicon. Minimizing switching losses (as well as all other losses) within the transistor can allow it to conduct currents closer to its maximum rating, thereby reducing the cost per rated kVA of the silicon.

Low-voltage power semiconductors generally exhibit much better characteristics than high-voltage devices. They have much faster switching speeds, resulting in lower switching losses. This translates into improved AC wave form quality, as well as in reduced size of reactive elements. Within a given family of devices, low-voltage devices tend to have substantially lower forward-voltage drops than high-voltage devices, all other factors being equal. Low-voltage devices therefore have lower conduction losses, and they cost less per kVA. However, the type of device and its design details also have a strong impact. The power metal oxide semiconductor field effect transistor (MOSFET) is a majority-carrier device whose forward-voltage drop increases very rapidly with rated voltage. These devices are superior to other devices at voltages below 400 V. They are commonly employed in commercial products that have switching frequencies in the range from hundreds of kilohertz to several megahertz. IGBTs are single-injection minority-carrier devices with forward-voltage drops that are superior to MOSFETs at voltages above 400 V. They are available in switched-mode (up to 100 kHz, 900 V), third- or fourth-generation (1–20 kHz, 600–1700 V), and HVIGBT (a few kilohertz, up to 4500 V) technologies. MOSFETs and IGBTs can both be directly paralleled, and the current shared between chips. GTOs and GCTs are double-injection minority-carrier devices with forward-voltage drops superior to those of HVIGBTs, and their voltage ratings approach those of semiconductor-controlled rectifiers (SCRs). However, the switching speeds of GTOs and GCTs are restricted to below 1 kHz. These latching devices have a four-layer structure similar to that of the SCR, but they require a modern fabrication process to achieve the required fine feature size that allows gate control of their turn-off transistors. They cannot be paralleled without adding external circuitry to force current sharing between devices; for this reason, they are not constructed as modules of paralleled small chips, but rather as single devices that fill an entire silicon wafer.

The available magnetics materials fall into three categories. Low-frequency laminations are very inexpensive but are generally restricted to applications involving low frequencies such as 60 Hz. Laminated steels can be employed at somewhat higher frequencies, at a substantial increase in cost. These materials also exhibit the highest saturation flux densities (1.5 to 2.0 T), which further reduces their cost. Amorphous alloys such as Metglas (Metglas®, Inc.) are useful for frequencies of several kilohertz, and

exhibit saturation flux densities nearly as high as those of laminated steels. However, the cost of Metglas is very high—roughly an order of magnitude higher than laminated steel. As a result, the gain in reduced inductor value that accrues from increasing the switching from a few hundred hertz to a few kilohertz is not accompanied by reduced inductor cost because the material required is expensive, unless other ways of filtering the switching harmonics can be found. Consequently, several kilohertz becomes an awkward choice for the switching frequency of a converter that includes filtering of the switching harmonics. Ferrite materials exhibit greatly reduced core losses, and are useful for switching frequencies in the 20-kHz to 1-MHz range. Because their saturation flux densities are greatly reduced (0.3 to 0.5 T), they lead to the need to use large and expensive elements unless the switching frequency is sufficiently high. To achieve competitive costs using ferrite inductors, switching frequencies of roughly 100 kHz or above are required.

The loss mechanisms of magnetic devices can be divided into the broad categories of core loss and copper loss. Copper loss depends on the winding current, which means that it decreases with decreasing load current. Core loss depends primarily on the magnitude of the AC voltage applied to a winding, so core loss tends to be less dependent on load current.

1.2 EFFICIENCY VERSUS WIND SPEED

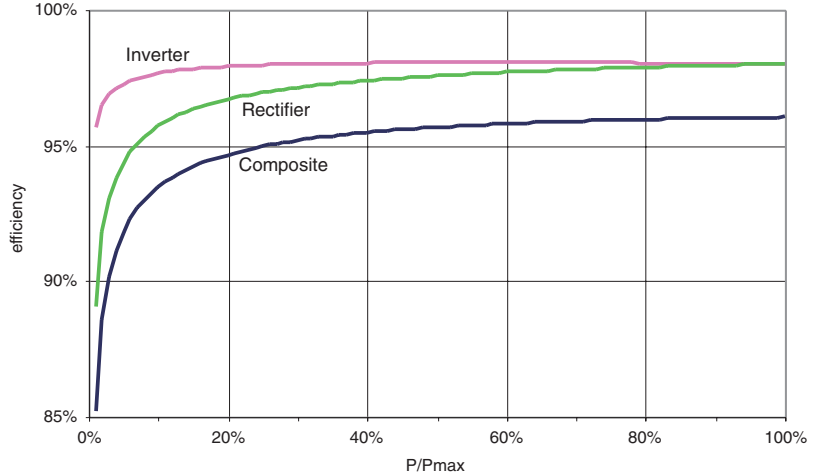
Researchers have now recognized that achieving high efficiency under low wind conditions is crucial to variable-speed designs (Fingersh and Robinson 1997). Because typical wind systems operate at low wind most of the time, the COE can be substantially improved by improving the system efficiency in low wind conditions. The requirement for high efficiency at low power and low speed is unique to the wind power field, and off-the-shelf converters do not satisfy the needs of wind power.

1.2.1 Origins of Poor Efficiency at Low Wind Speed

It is common practice to optimize the design of a DC link converter system at rated conditions. This lowers the cost of the system by minimizing the component stress and loss under worst-case conditions. For example, in a variable-speed motor drive, the motor voltage is chosen to be equal to the utility voltage under rated (full power and speed) conditions. The DC link voltage is slightly greater than the peak line-line utility voltage. These typical choices minimize the voltages and currents applied to the semiconductor devices under these conditions, and allow semiconductor devices that have minimum size and capital cost to be selected. A secondary effect of this practice is that the efficiency of the system is diminished at reduced speed and voltage.

We modeled the efficiency curves for a DC link system in our previous project (Erickson, Al-Naseem, and Changtong 1999), and the results are illustrated in Figure 1-2. In this system, the DC link voltage is fixed, and is slightly greater than the peak line-to-line voltage of the utility. As a result, the inverter operates with high efficiency because the utility voltage and the DC link voltage are close in value. The voltage that the synchronous machine produces is also close in value at maximum wind speed, but it decreases as the wind speed decreases. Under low wind conditions, the reduced voltage produced by the synchronous machine causes the rectifier to “work harder” in stepping up the voltage, with a greater proportion of indirect power. In the rectifier portion of the DC link system, the indirect power consists of energy that is first stored in the inductor and later released to the DC link. In contrast, direct power consists of power that flows directly

Figure 1-2. Efficiency of the inverter, rectifier, and composite converter system of a DC link converter system that interfaces a variable-speed synchronous generator to the AC utility. For this plot, the generator voltage was assumed to vary as the square of the power.



from the generator to the DC link, without going through the intermediate step of storage in the inductor. Direct power must pass through only the upper semiconductor devices in the circuit of Figure 1-3; indirect power must pass through both the upper and lower devices of the bridge. This means that indirect power conversion incurs additional loss. The indirect power is increased when the peak line-line voltage differs substantially from the DC link voltage. The reduced rectifier efficiency at low generator voltages, then, can be explained through increased conduction loss, even without fixed losses.

The concept of indirect power is well understood in the power electronics literature (see, for example, Wolaver 1969, along with Kassakian, Schlecht, and Vergese 1991). For example, in the boost converter of Figure 1-3, if the transistor switch is always off (duty cycle = 0), the output voltage is equal to the input voltage. No power conversion takes place within the converter, and power equal to the direct power flows from the input to the output. If the transistor switches with some nonzero duty cycle, energy is stored in the inductor when the transistor conducts. When the transistor is off, the stored energy within the inductor is released to the output; during this interval, the voltage developed in the inductor rides on top of the input

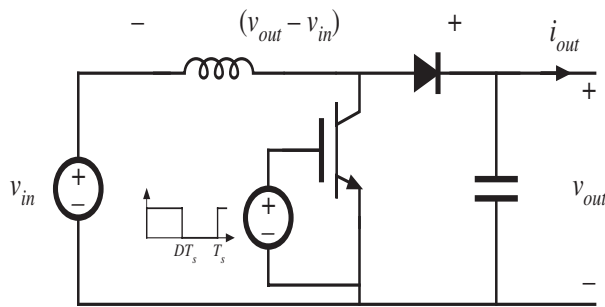
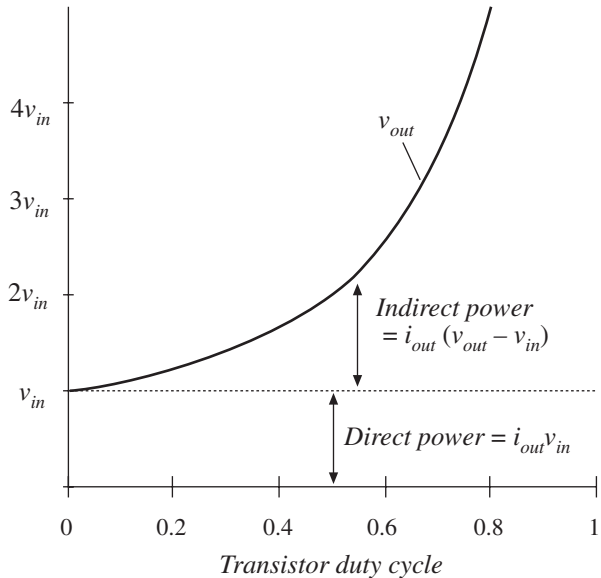


Figure 1-3. Direct and indirect power in a boost converter



voltage to produce the output voltage. The indirect power is equal to the power that is alternately stored in the inductor and then released to the output. When the input and output voltages are close in value, the indirect power is also very small. At such operating points, the transistor voltage and current stresses are relatively low compared to the output voltage and current, and the converter efficiency is high. In effect, the converter must work to convert only the indirect power, and in this sense the converter transistors are rated for a fraction of the total load. The boost, buck, DC link, and matrix converters are examples of circuits that can have substantial direct power components. Converters that do not contain DC voltage and current paths between the input and output terminals, such as the buck-boost converter, all transformer-isolated converters, and many resonant converters, can process power only through indirect means. These converters generally will operate with higher semiconductor stresses and lower efficiency. The increased proportion of indirect power at low wind accounts for the reduced efficiency of the rectifier in Figure 1-2.

When converters have fixed losses, or losses that are only weakly dependent on loading conditions (such as some mechanisms of switching loss and core loss), disabling one or more parallel-connected converters under low wind conditions can improve efficiency. Because the fixed losses are reduced, the remaining converter operates at a point exhibiting higher efficiency. Such an approach can increase the light-load efficiency of the inverter in the DC link system of Figure 1-2. However, we can see that there is very little to be gained from such an approach, as the inverter efficiency does not vary by much except at very low power levels.

Disabling parallel-connected rectifiers at light load does not necessarily improve the system efficiency. For example, suppose that the system operates at 20% of maximum load power, corresponding to some value of wind speed and generator voltage. If the rectifier consisted of two parallel-connected rectifier circuits, each rectifier would operate at 20% of its maximum power, and yield the efficiency shown in Figure 1-2. Turning off one of these rectifier circuits would cause the remaining rectifier circuit to operate at 40% of its rated power, but the generator voltage would be unchanged. Figure 1-2 cannot be used to determine the efficiency in this case, because the rectifier operating point (determined by both voltage and power) does not coincide with any points on the plot. Indeed, the near-independence of the inverter efficiency with power suggests that the rectifier efficiency is more dependent on voltage than on power (note that in this DC link system, the DC link voltage and the utility voltage are both fixed, so the terminal voltages of the inverter do not vary with wind speed). Therefore, the approach of disabling parallel-connected rectifiers at light load would probably have little effect on system efficiency.

1.2.2 Redesign of DC Link

We might attempt to mitigate the light-load efficiency problem by changing the design of the converter and the choice of operating points, such that the generator voltage is equal to the utility voltage at some reduced speed condition. This could be accomplished by increasing the generator volts/rpm ratio or decreasing the utility voltage. This has the effect of shifting the maximum efficiency point of the converter system to a lower wind speed. The efficiency in Region II (peak power tracking regime) is improved, at the expense of the efficiency in Region III (operation at fixed rated power).

The problem with this approach is the converter behavior at maximum power (for example, in Region III, where the generator voltage will substantially exceed the utility voltage). Relative to a more traditional design, this approach requires increased semiconductor ratings because it is suboptimal at rated power.

Specifically, there are two cases:

1. If light-load efficiency is improved by increasing the generator volts per rpm, the semiconductor voltage ratings must be increased to withstand the increased DC link voltage at maximum speed. This necessitates using larger, more expensive devices. As the generator voltage and DC link voltage increase, the switch duty cycles will be scaled back. The same converter would be capable of producing more power if the utility voltage were higher.
2. If light load efficiency is improved by reducing the utility voltage, the utility currents will be increased so that rated power is maintained. This leads to increased current in the converter elements, with commensurate increased ratings and cost. Again, the same converter would be capable of producing more power if the utility voltage were higher.

In either case, the cost of the converter is substantially increased because of the increased rated-load stresses and losses that result from increased indirect power. For example, if the generator voltage is equal to the utility voltage at half speed, the size and cost of the converter is approximately doubled. This would lead to a serious penalty in the COE, which is likely to negate any gains in COE brought about by the improved light-load efficiency. We believe that this is a poor approach for wind power systems.

1.2.3 Multilevel Conversion Is a Solution

The example given in Section 1.2.2 illustrates that the optimization of the full-load converter design must not be compromised by attempts to improve the partial-load efficiency. Further, it should be apparent that the basic DC link circuit is incapable of simultaneously meeting the requirements of partial-load efficiency and economical design at rated load. It is somewhat disappointing that the light-load efficiency is less than the full-load efficiency, especially in view of the fact that a converter could be built that would exhibit higher efficiency at light load (even using less silicon!), if only the operating point could be better optimized. This suggests that we need to reconfigure the converter to optimize efficiency over a wider range of operating points.

Such reconfigurable converters are indeed possible. They require finer control of the silicon (which adds complexity), so that the power conversion mechanisms can be effectively reconfigured and better optimized at a wide range of operating points. For example, high-current IGBT and MOSFET modules are composed of many individual transistor chips, mounted on a common thermal substrate and packaged into one module. The individual chips are typically rated at 30 to 100 A each. The same chips are available in smaller packages with lower current ratings, and are also available individually in TO-247 or similar packages. The cost is primarily a function of the total silicon area within the package. So we might elect to employ (a) one large device, or in its place (b) several smaller devices. The biggest disadvantage of option (b) is its higher parts count, with possible higher manufacturing cost and lower yield. However, we can deal with this by using up-to-date manufacturing techniques, such as modularity and machine-fabricated printed circuit boards. Option (b) also requires more complex control, which can be accomplished by exploiting today's sophisticated microcontrollers.

Using multilevel converters is a reconfiguration approach that can improve the efficiency of the rectifier at light load. At low input voltages, these circuits can be operated in a multiplier mode that attains a high ratio of output to input voltage, maintaining efficiencies close to the values attained with high input voltage.

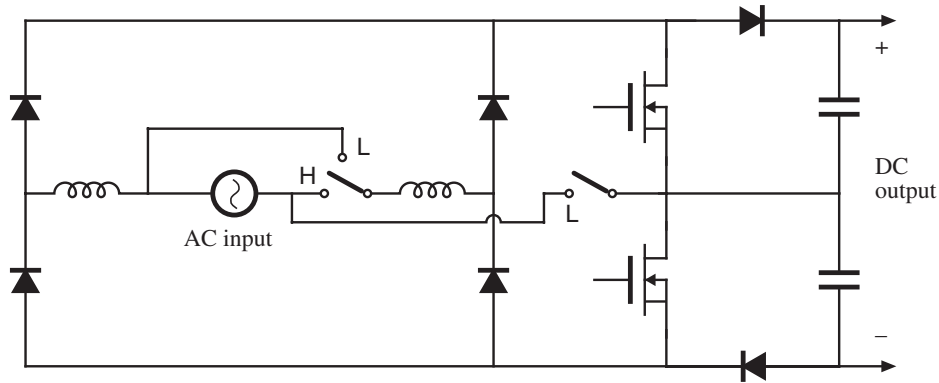


Figure 1-4. Single-phase boost PWM rectifier with switches to reconfigure the converter, resulting in optimized efficiency over a wide range of AC input voltages. The converter operates in three-level doubler mode at low AC input voltage (Maksimovic and Erickson 1995).

Figure 1-4 shows an example of such a converter. This converter is a single-phase pulse-width modulated (PWM) rectifier based on the boost converter. At high input voltage (with the switches in the positions marked “H”), the circuit functions as a traditional boost converter with the MOSFETs switching on and off at the same time. The DC output capacitor is split so that each capacitor voltage is half of the DC output voltage. The maximum MOSFET voltages are clamped to a capacitor voltage. For operation at low input voltage, the switches are moved to the positions marked “L.” The converter then operates in doubler mode, with three-level wave forms. The experimental data of Figure 1-5 is taken from Maksimovic and Erickson (1995).

We can see that reconfiguring the converter for three-level operation in doubler mode leads to a substantial improvement in efficiency. In the plots of Figure 1-5, the AC input voltage is varied while the load power is held constant. This is a single-phase example, but it correctly illustrates the concept and behavior in the

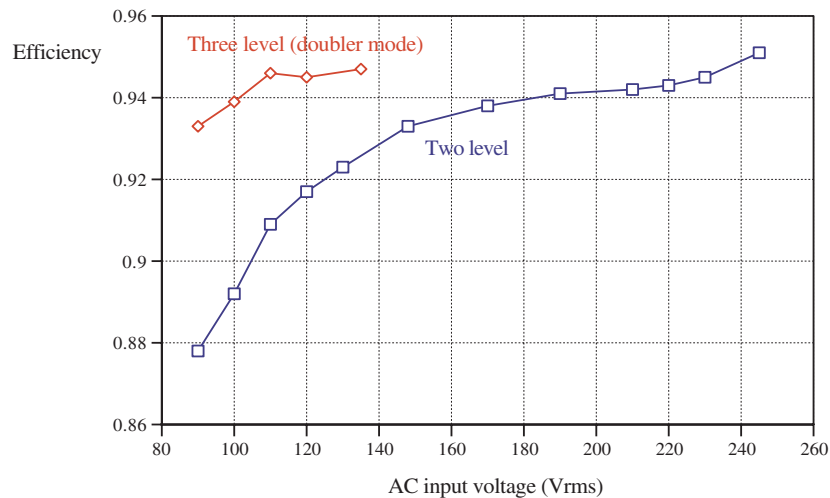


Figure 1-5. Experimentally measured improvement of efficiency in the reconfigurable PWM boost rectifier of Figure 1-4

three-phase case. When configured for high AC line-voltage operation, the circuit functions as a conventional boost converter with two-level switching. The increased conduction and switching losses at low input voltage lead to decreased efficiency. At low AC line voltage, the reconfiguration of the converter for three-level doubler operation leads to reduced losses, which correspond to a lower effective DC link voltage with correspondingly higher efficiency. In the universal-input rectifier application, the converter must produce full output power even when the AC line voltage is low; this led to a need to reconfigure not only the semiconductors but also the magnetics. Because full power at low generator voltage is not required in the wind power application, simpler approaches that do not attempt to reconfigure the magnetics could be employed.

Efficiency of a wind power system at low generator voltage can be improved merely by incorporating multilevel switching. Figure 1-6 shows an example of one phase of a conventional three-level inverter or rectifier. The DC link is divided in half, and DC capacitors are each charged to half of the DC link voltage. The maximum voltage applied to the transistors is clamped to one capacitor voltage. In previous work (Erickson, Al-Naseem, and Changtong 1999; Carlin 2000), the efficiency of this system was extensively modeled, including the effects of multilevel switching using the same devices and loss models.

Figure 1-6. Conventional three-level DC link inverter. One phase is illustrated.

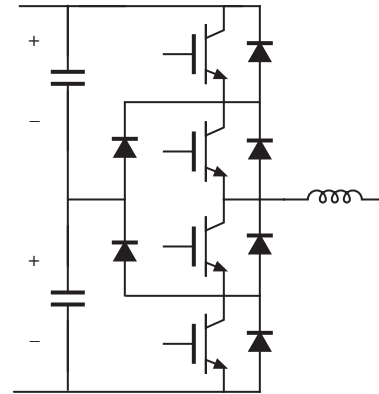


Figure 1-5 illustrates the improvement in efficiency that can be attained by changing from two-level to three-level switching. The efficiencies of the PWM rectifiers, PWM inverters, and composite systems are compared for conventional DC link systems. The switching losses and conduction losses of all semiconductor elements are modeled in detail. Losses of the reactive elements are not included. Figure 1-7(a) shows the efficiency of the conventional system, which has two-level switching; this plot is identical to Figure 1-2. The reduced efficiency at light load is dominated by the rectifier losses. Figure 1-7(b) is the efficiency of a three-level system that employs the same semiconductor elements and uses identical models of the switching and conduction losses. We can see that:

- The efficiency at full load is improved. This alone may justify using multilevel switching, because it improves the energy capture of the system. Even though the full-load point involves operating in Region III where the maximum hub power is limited, the improved efficiency of the converter still implies that more of this limited power is actually output to the utility. Higher efficiency at rated load power also implies improved reliability and reduced heat sink size.
- The efficiency at light load is improved, and the knee of the efficiency curve is shifted to the left. Effectively, the range of power levels over which the high full-load efficiency is maintained is extended by a factor of approximately two (i.e., the value of P/P_{max} at the knee is reduced by 50%).

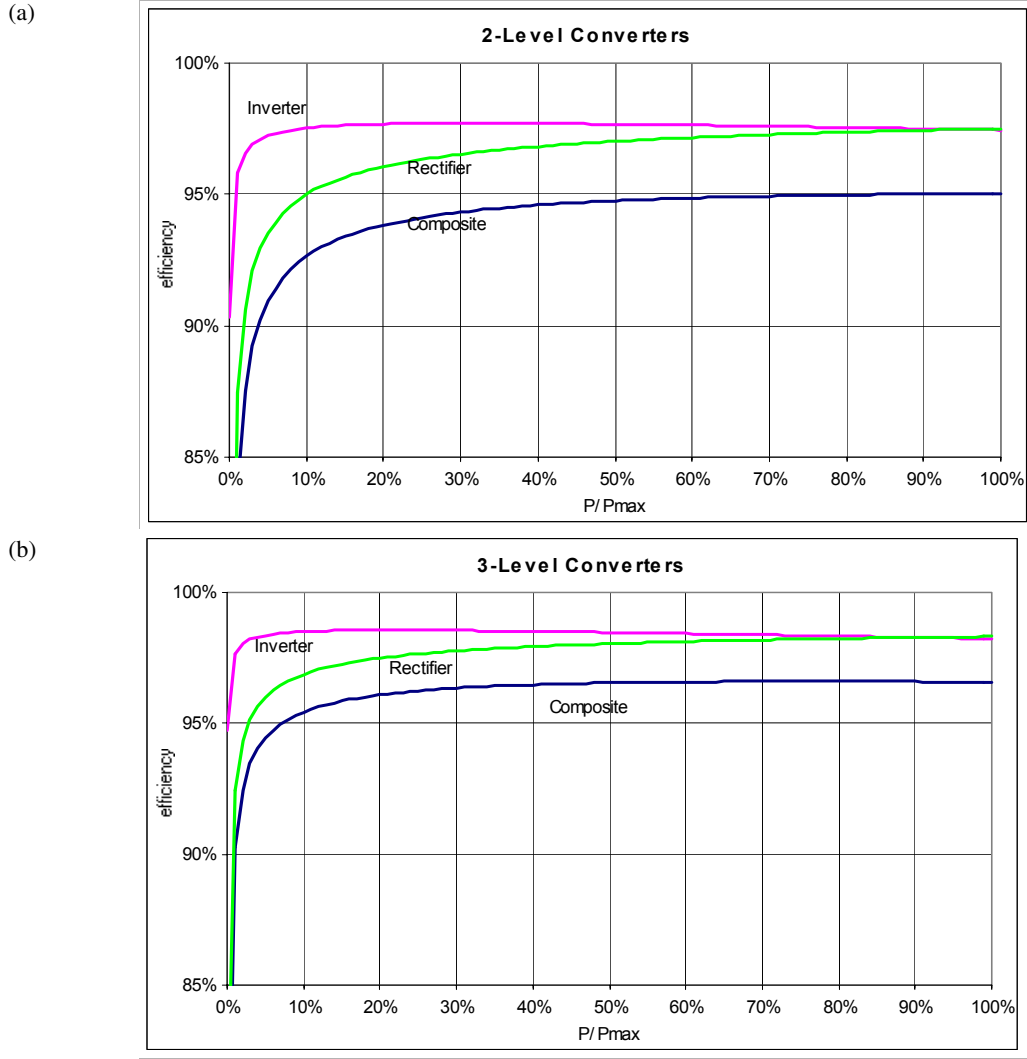


Figure 1-7. Effect of multilevel switching on the efficiency curves of a DC link converter system in a wind power application: (a) conventional two-level converter, (b) a three-level converter that employs the same devices

The three-level converter of Figure 1-7(b) operates with all voltages doubled (compared with the two-level case), so the rated power P_{max} is doubled. However, the switching losses are not doubled because the dominant sources of switching loss are induced by the diode reverse recovery process and the IGBT current tailing process. Each process can be expressed by equations of the form

$$P_{sw} = Q(\Delta v) f_s \tag{1-1}$$

where Q is the integral of the IGBT current during the switching transition (equal to the diode recovered charge and the area of the IGBT current tail, respectively); Δv is the blocking voltage of the IGBT (equal to the DC link voltage in the two-level case, and half of the DC link voltage in the three-level case); and f_s is the switching frequency. Equation 1-1 is numerically the same for both converters of Figure 1-7, but the

output power is doubled in the three-level case. The three-level case, then, exhibits significantly higher efficiency. In addition, this switching loss is distributed over twice as many IGBTs in the three-level converter, which implies that each individual IGBT endures less loss. Because IGBTs are thermally limited by their packages, reduced switching loss implies that additional conduction loss can be tolerated. In other words, the same IGBTs can be operated at higher current levels, the rated power of the converter could be increased, and the capital cost per rated kVA can be reduced.

The results of Figure 1-7 further suggest that resonant conversion or soft-switching techniques, such as the auxiliary-resonant commutated-pole approach (Bernet and Teichmann 1997), may not be necessary. Resonant conversion and soft switching are approaches to reducing switching loss, but come at the expense of increased conduction loss and increased silicon area. Using multilevel switching also achieves reduced switching loss, but without the penalty of increased silicon area.

The results summarized in Figure 1-7 constitute a controlled simulation, backed by an experimentally verified loss model, that objectively shows how multilevel switching can ultimately improve the partial-load efficiency of the converter in a wind power system relative to a conventional two-level DC link system. The results summarized in Figure 1-5 constitute measured laboratory efficiency curves of similar reconfigurable PWM boost rectifiers. We can conclude that multilevel switching is indeed a real, practical solution to the problem of poor efficiency at partial load.

A modulation technique for control of DC link multilevel converters at reduced voltage magnitudes is described in Tolbert, Peng, and Habetler (2000). However, this reference does not address the effect of the described approach on converter efficiency.

1.3 MULTILEVEL CONVERSION

Multilevel conversion has attracted significant attention as a way to construct a relatively high-power converter using many relatively small power semiconductor devices (Nabae, Takahashi, and Akagi 1981; Bhagwat and Stefanovic 1983). Multilevel switching involves using additional voltage levels in the switched wave forms; for example, in Figure 1-8, conventional two-level switching is compared with three-level switching. This approach has the advantages of reduced switching loss and reduced harmonic content of output AC wave forms. The peak voltages applied to the semiconductor devices are clamped to capacitors with DC voltages that can be controlled via feedback. When the input and output voltage magnitudes differ significantly, it is also possible to reduce the conduction losses using multilevel

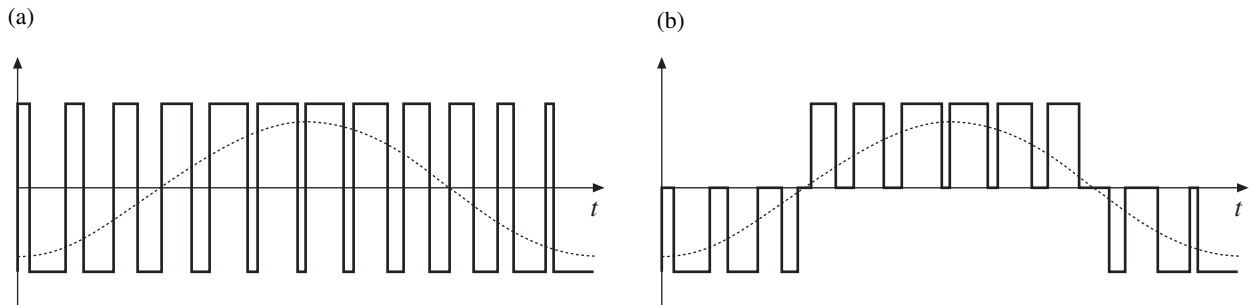


Figure 1-8. Comparison of PWM wave forms for (a) conventional two-level switching, and (b) three-level switching

techniques as shown in Section 1.2.3; this property could improve the energy capture of variable-speed wind power systems. Although multilevel conversion requires a higher packaging and parts count, the total silicon area can, in principle, be reduced because of the lower device voltage ratings. Higher performance is attained, although at the expense of increased control and complexity.

1.3.1 Known Multilevel Converters Based on DC Link Topology

Multilevel extensions to the conventional DC link topology are now well accepted in the literature. Figure 1-6 depicts one phase of a three-level converter. The DC link capacitor is split into multiple series-connected capacitors. The converter control system regulates the voltages of these capacitors, so that they share the total DC link voltage evenly. Each semiconductor device is rated to block the voltage across one of the capacitors. Figure 1-9 illustrates a complete DC link rectifier/inverter system based on four-level converters. Three-level and five-level converters have found significant industrial application and are extensively described in the literature (see, for example, Nabae, Takahashi, and Akagi 1981; Bhagwat and Stefanovic 1983; Manjrekar and Lipo 1998; Tolbert and Peng 1998; Cengelci et al. 1998; Tolbert, Peng, and Habetler 2000). Multilevel converters appear well-suited for medium-voltage high-power AC drives (Tolbert and Peng 1998; Cengelci et al. 1998), and a variety of power semiconductor devices can be employed (Manjrekar and Lipo 1998).

A number of control techniques are applicable to multilevel conversion. For example, slow switches can be used, which switch at the line frequency or at a low multiple of the line frequency (Nabae, Takahashi, and Akagi 1981; Bhagwat and Stefanovic 1983); this approach is appropriate when GTOs or GCTs are employed. In such cases, multilevel converters generate AC wave forms of higher quality (reduced harmonic content), relative to the wave forms of an equivalent two-level square-wave converter. The switching frequency can also be increased using PWM to further improve the wave form quality—this is appropriate when faster devices such as IGBTs are employed. Popular methods for generating the modulated gate drive signals include techniques that are based on analog carrier wave forms, in addition to digital techniques that employ space vector modulation (SVM).

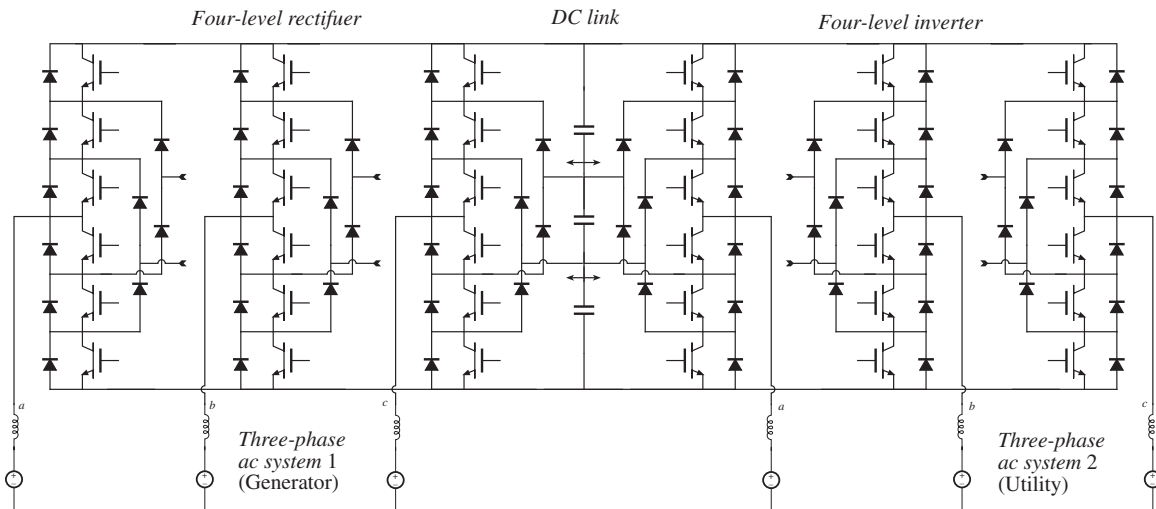


Figure 1-9. DC link converter system based on four-level converters

As we noted previously, multilevel conversion leads to reduced switching loss according to Equation 1-1, because of the reduced change in transistor voltage (Δv) during each switching transition. This same mechanism also allows the size of filter magnetics to be reduced, because the magnitude of the voltage applied across the filter inductors is reduced. For example, the required inductance in a three-level converter is approximately half the value required in a two-level inverter, if all other quantities are kept constant. We should note that the fast risetimes of the voltages applied to machines by PWM converters have been implicated in the premature failure of winding insulation (Mefti et al. 1997; Mefti et al. 1998; Rendusara and Enjetic 1998), and that common-mode currents generated by converter switching wave forms have been implicated in the premature failure of machine bearings (Busse et al. 1997). For this reason, it is advisable to include filtering between the converter and the machine, and filter size, cost, and efficiency become issues. Some filtering between the converter and the utility is also necessary, to meet regulations on electromagnetic interference and harmonic content. This filtering may also be realized using discrete magnetic elements. Finally, using inductors allows better regulation of the currents in parallel-connected converters, so that accurate sharing of currents in modular systems can be achieved. Thus, multilevel conversion can accrue the added benefits of reduced switching loss and reduced magnetics size.

1.3.2 Known Multilevel Converters Based on Voltage-Clamped Switch Cells

As the number of levels is increased, the bus bar structures of multilevel DC link converter systems can become quite complex and difficult to fabricate. This problem can be solved by using the simple voltage-clamped switch cell illustrated in Figure 1-10 (Peng and Lai 1995; Lin, Chien, and Lu 1999). This circuit locally clamps the voltages applied to the semiconductor devices to the value V . This switch cell is capable of producing the instantaneous voltages $+V$, 0 , and $-V$, when the devices conduct, and is capable of blocking voltages of magnitude less than V when all of the devices are off. Figure 1-11 depicts one phase of a multilevel inverter that employs three of these switch cells. Three of the circuits illustrated in Figure 1-11 could be connected in wye to obtain a three-phase converter. This circuit is modular in form, and the bus bar structures need only be simple H-bridge configurations. Controlling this system is relatively simple.

The difficulty with the approach of Figure 1-11 is that the voltage sources V of each switch cell must generate the average power supplied by the inverter, and hence floating sources of DC power are required. It has been suggested in the literature that this could be an appropriate configuration for solar-array inverters, with the voltage sources V replaced by solar panels. Investigators have also suggested that the voltage sources V could be realized using transformer-isolated DC power supplies (Peng and Lai 1995;

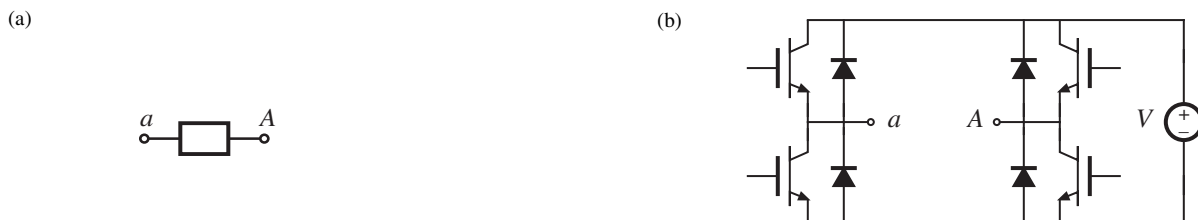
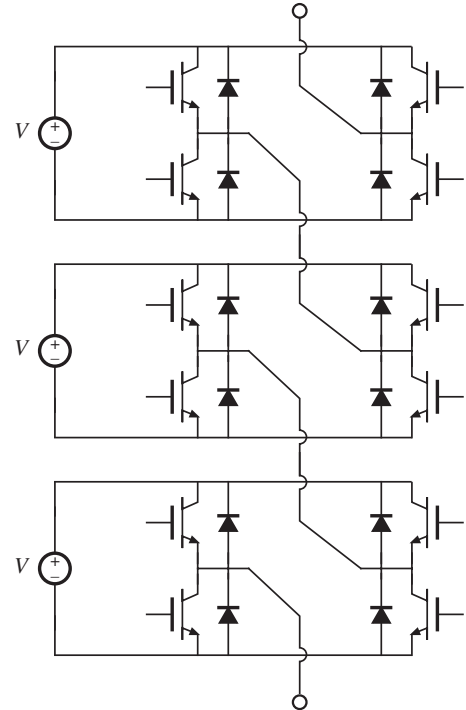


Figure 1-10. Voltage-clamped switch cell: (a) switch cell symbol, (b) schematic diagram

Figure 1-11. A multilevel converter that employs the switch cell of Figure 1-10. One phase is shown.



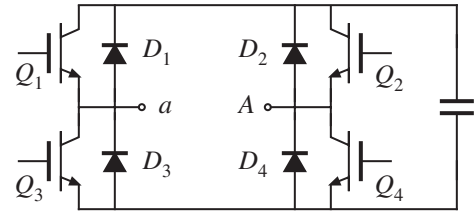
(Lin, Chien, and Lu 1999). However, such isolated power supplies must operate with 100% indirect power, resulting in increased transistor stress and reduced efficiency compared with other approaches such as the DC link or matrix converter. In consequence, this approach exhibits high cost and poor performance. Thus, there has been an unmet need for a multilevel converter that employs simple switch cells based on the H-bridge, and that does not require floating sources of DC power.

1.3.3 Proposed New Multilevel Matrix Converters Based on the Matrix Topology

In this project, we developed a new approach for AC-to-variable-AC conversion that is based on simple H-bridge switch cells, and that overcomes the problems associated with the power stages of previously known multilevel converters. Using a matrix configuration eliminates the need for the voltage sources V to supply average power, so these voltage sources can be replaced with simple capacitors. The bus bar structures and the power stage of the proposed converter are therefore relatively easy to construct. Because isolated DC–DC converters are not needed, high efficiency and low total switch stress can be attained. We also believe that the proposed new converter is the first known approach to attaining multilevel operation in a matrix configuration.

The proposed new family of converters employs the voltage-clamped H-bridge configuration shown in Figure 1-12. This circuit resembles the cell of Figure 1-10, except that the DC voltage source is replaced by a capacitor. Figure 1-13 illustrates a basic configuration of the proposed new converter family. Nine of the switch cells of Figure 1-12 are connected in a matrix configuration, between the AC input (i.e., the generator output) and the AC output (the utility). In this matrix configuration, the DC capacitors of the switch cells are alternately charged and discharged, so no source of DC power is needed. This results in a simple modular structure.

Figure 1-12. Switch cell employed in proposed new family of multilevel matrix converters. No source of DC power is needed, and transistor voltages are clamped to a DC capacitor voltage.



Chapter 2 gives details of the proposed new approach to multilevel matrix conversion. This approach is fundamentally different from the conventional matrix converter (Alesina and Venturini 1989; Huber and Borojevic 1995) in several respects. It is capable of both increasing and decreasing the voltage magnitude and frequency, while operating with arbitrary power factors. The peak semiconductor device voltages are locally clamped to a DC capacitor voltage, whose magnitude can be regulated. Multilevel switching is used to synthesize the voltage wave forms at both the input and output ports of the converter. In the basic configuration of Figure 1-13, the converter operates with two-level switching at rated speed, and can switch to three-level operation at low speed to increase the efficiency. The modular structure can be scaled to higher voltage and power levels by connecting additional switch modules in each leg of the matrix; this could allow use of low-voltage high-performance semiconductor devices in a high-voltage high-power application. Such a converter would be capable of higher order multilevel switching, with commensurate gains in efficiency and cost.

The proposed new converters require a larger number of discrete devices than conventional approaches such as the DC link system. However, because the devices have smaller silicon area, they are less expensive. Rather than packaging multiple silicon chips into a single high-current module (as in the conventional approach), the chips could be individually packaged and controlled. With the same silicon area and cost, greater control flexibility becomes possible. Further, the proposed new converters effectively utilize their semiconductors, so that high efficiency and low silicon cost are maintained.

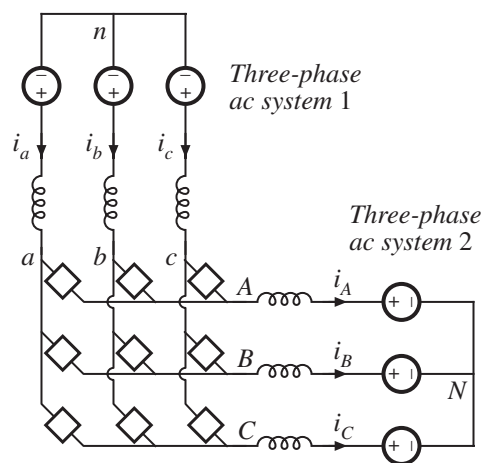


Figure 1-13. Basic configuration of the proposed new family of matrix converters.

Chapter 3 describes the control of a basic version of the proposed new family of matrix converters. We show that space vector control techniques can be adapted to control the input and output wave forms of the converter simultaneously. We can also see that the capacitor voltages of the switch cells can be stabilized using the appropriate control measures. Simulations confirm the operation of the basic form of the new matrix converters. We developed a relatively simple algorithm for implementing space vector control of the proposed new converter, which is also described in Chapter 3.

Construction of a laboratory converter is described in Chapter 4. To demonstrate the viability and performance of the proposed new approach, we have developed a system based on fast-switching IGBTs. The objective is to demonstrate the best performance that we can. Modular H-bridge switch cells are constructed on printed-circuit boards, and the system is controlled by a Motorola PPC555 microcontroller. This chip is interfaced through a digital bus structure, complex programmable logic devices (CPLDs), and flash memory containing the control algorithm, to the gate drive circuitry of each H-bridge. The key to this technology is implementing the control. We have demonstrated a working prototype that operates with space vector control. Although the control algorithm is complex, it can be manufactured cheaply—one simply duplicates the programming of the flash memory and CPLDs.

In addition to demonstrating the validity of the proposed new converters, we are further attempting to demonstrate the feasibility of operating at relatively high switching frequencies (50 to 100 kHz) at these power levels. As we discussed earlier, multilevel conversion results in reduced switching loss (and distribution of the remaining switching loss over a larger number of devices), without incurring the penalty in silicon area or conduction loss that is found in resonant approaches. Our laboratory prototype operates at a switching frequency of 50 kHz, and further increases may be possible if the gate drivers are improved. The proposed converters may find use in variable-speed AC drives, variable-speed wind power generation, and other polyphase AC-to-AC applications. They address the issues of variable-speed wind power, and can take advantage of the substantial and ongoing advances in power semiconductors, packaging, and microcontroller technology.

2.0

New Multilevel Matrix Converters

2.1 PROPOSED NEW FAMILY OF CONVERTERS

A basic configuration of the proposed new multilevel matrix converter is shown in Figure 2-1 (Erickson and Al-Naseem 2001). Superficially, the converter resembles a conventional matrix converter through its use of a matrix of nine four-quadrant switch cells. However, the switch cells are realized as illustrated in Figure 2-2. Each cell resembles the cells of Figure 1-10 except that the cells do not require sources of DC power, and hence the DC voltage sources may be replaced by capacitors. The transistors and diodes within each cell are clamped to the DC capacitor voltage V_{cap} , which can be regulated to a known DC value. As with the switch cell of Figure 1-10, this switch cell is capable of producing the instantaneous voltages $+V_{cap}$, 0, and $-V_{cap}$ when the devices conduct, and is capable of blocking voltages of magnitude less than V_{cap} when all the devices are off. Using switch cells based on the H-bridge circuit allows for simple modular construction.

The use of four transistors in the switch cell of Figure 2-2 allows the average current to be doubled, relative to a conventional matrix converter whose four-quadrant switches are realized using two transistors and two diodes. This is true because the currents conducted by the IGBTs are thermally limited, and with proper control, the current stresses can be spread over all four devices in Figure 2-2. The proposed converter, then, effectively utilizes the silicon of the devices, and its silicon cost per kVA is competitive with other

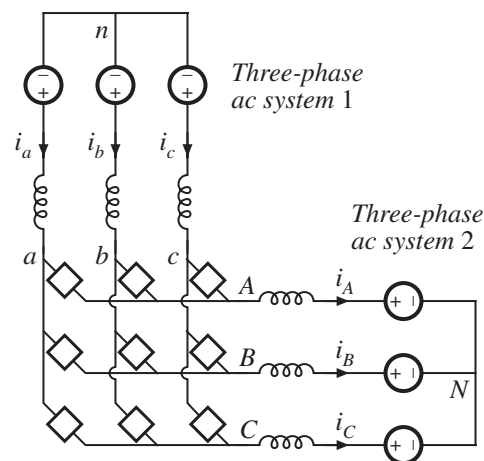


Figure 2-1. Basic configuration of the proposed new family of matrix converters

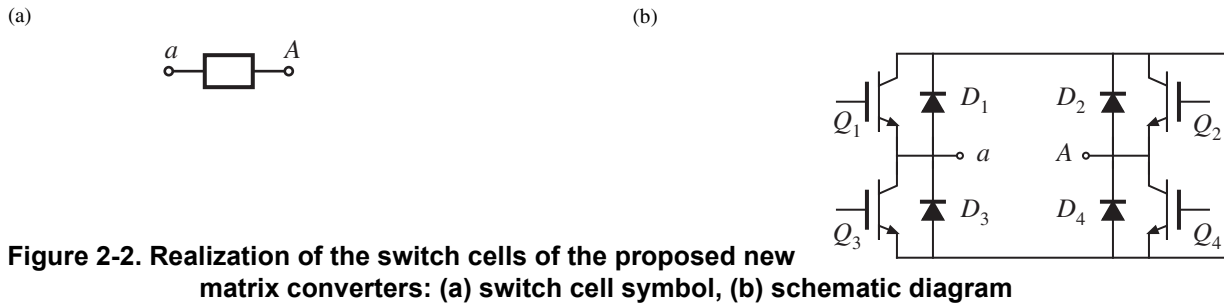


Figure 2-2. Realization of the switch cells of the proposed new matrix converters: (a) switch cell symbol, (b) schematic diagram

approaches such as the DC link or the conventional matrix converter. However, rather than paralleling many silicon chips within a few large packages, the proposed approach employs the same silicon with more and smaller packages. This allows finer control of the wave forms, leading to the potential for improved performance over a wide range of operating points.

The basic circuit of Figure 2-1 is capable of limited multilevel operation. The semiconductor devices must be rated at least as large as the peak applied line-to-line voltage, with an appropriate additional safety factor. Given such devices, the converter can operate with only two-level switching when the input and output voltages are equal to their full rated values. However, when one (or both) of the voltages are sufficiently reduced, the converter can be controlled to operate with three-level switching, without exceeding the voltage ratings of the devices, by reducing the capacitor voltages. In a wind power application, the proposed converter can operate with two-level switching at rated wind speed, and three-level switching at low wind speed. The converter is capable of both increasing and decreasing the AC voltage magnitude, and can interface two asynchronous AC systems with arbitrary power factor. Both the input and the output ports are inductive in nature; these inductors may be physical discrete elements, or they may be inductances of other system elements such as machine winding or transformer leakage inductances, among others.

The number of voltage levels can be increased. Figure 2-3 illustrates a multilevel version of the proposed matrix converter family, in which each branch of the switch matrix contains two series-connected switch cells. Each switch cell is again realized using the voltage-clamped H-bridge circuit shown in Figure 2-2. This converter is capable of producing three-level operation (i.e., three levels of line-neutral voltage, or five levels of line-line voltages) at the full rated operating point, with sharing of voltage stresses among the switch cells. This approach allows the terminal voltages to be increased without changing the voltage ratings of the semiconductor devices. The number of levels can be further increased when the input and/or output voltage is reduced.

The circuit of Figure 2-3 can be extended to allow three or more switch cells per branch. Thus, the proposed new family of matrix converters is composed of polyphase AC-AC converters having input and output ports (each port made up of several phases) that are inductive in nature, with a matrix of switch cells that serve as conducting branches from each input phase to each output phase. Each branch includes one or more switch cells. Each switch cell is composed of an H-bridge circuit with a DC capacitor.

We are employing IGBTs as the switching elements within the switch cells, as illustrated in Figure 2-2(b),

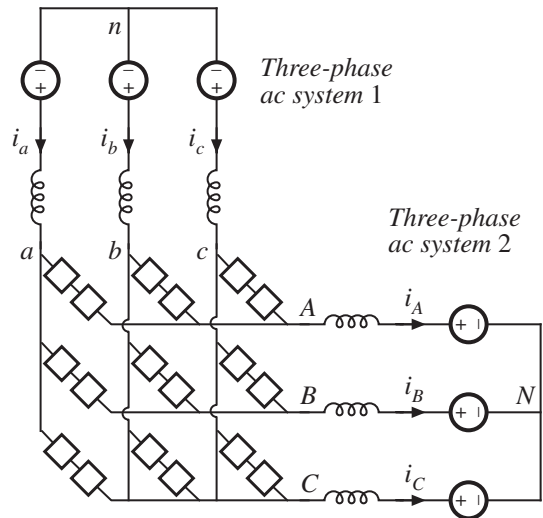


Figure 2-3. A new multilevel matrix converter containing two of the switch cells of Figure 2-2 in each branch of the switch matrix

and we are attempting to operate these devices with switching frequencies in the 10-kHz to 100-kHz range. This high switching frequency reduces the size and cost of the reactive elements of the converter (i.e., the filter inductors and the DC capacitors). However, it is possible to employ other types of switching devices as the switch elements, including MOSFETs, bipolar junction transistors (BJTs), GTOs, and GCTs. In addition, the switches can be operated at lower frequencies such as several kilohertz, several hundreds of hertz, or the utility frequency. The design engineer typically selects the device type and switching frequency, based on application requirements. We should note that, even when the switching frequency is low, multilevel switching can reduce the magnetics size (relative to a two-level switching approach that has the same switching frequency).

The proposed multilevel matrix converter synthesizes the input and output voltage wave forms by switching the known DC capacitor voltages of the switch cells. This operation differs from that of the conventional matrix converter in which voltage wave forms are synthesized on one side, and current wave forms on the other. Because of the symmetry of the converter, step-up and step-down of the voltages are possible.

In the basic configuration of Figure 2-1, the converter consists of nine branches that each consist of a switch cell as depicted in Figure 2-2. To avoid interrupting the six inductor currents, exactly five branches must conduct current at any instant in time. It is important to avoid the cross-conduction and shoot-through currents that can occur when the transistors of six or more branches conduct (although in some special cases, it is possible to allow more than five branches to conduct). However, turning off the transistors of five or more branches does not cause a calamity, because the antiparallel diodes can conduct current and provide a path along which the inductor currents can flow. Energy stored in the inductors is then transferred to the capacitors of the switch cells. One simple method for coordinating the switching transitions is to first turn off all transistors that are to be switched off, and then after a short delay, turn on the transistors that are to be switched on (“break before make” operation). Other soft-switching schemes are also possible (Bernet and Teichmann 1997).

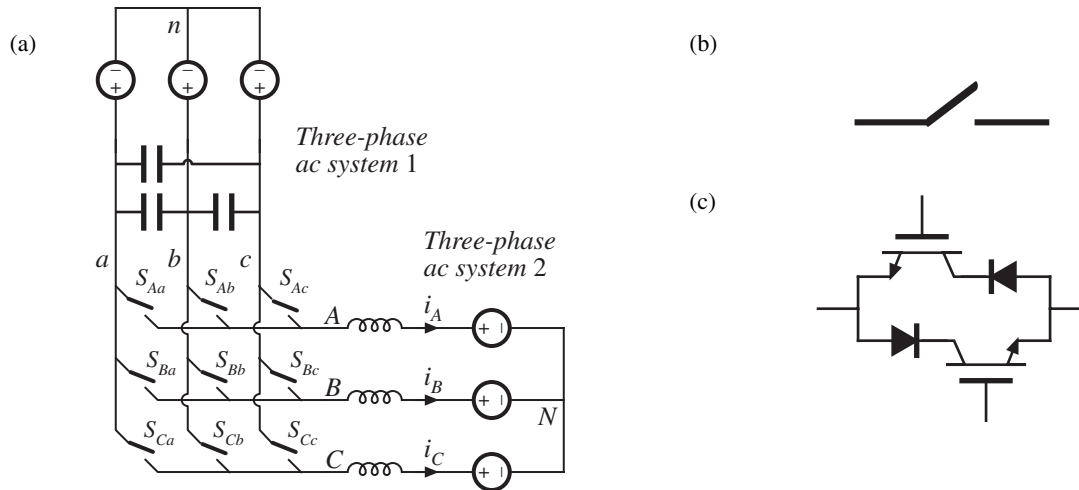


Figure 2-4. The conventional matrix converter: (a) schematic, (b) symbol for four-quadrant switches employed here, and (c) realization of four-quadrant switch using IGBTs and diodes

2.2 COMPARISON WITH CONVENTIONAL MATRIX CONVERTER

Table 2-1 summarizes several significant ways in which the proposed new converters differ from conventional matrix converters. For reference, the conventional matrix converter is illustrated in Figure 2-4. First, the conventional matrix converter can only step down (“buck”) the voltage, with a maximum output voltage magnitude of 0.866 times the input voltage magnitude. Alternatively, if the input and output terminals are reversed, the conventional matrix converter can only step up (“boost”) the voltage, with a minimum output voltage magnitude of 1.15 times the input voltage magnitude. In a wind power application, this constraint means that the generator voltage must not exceed 0.866 times the utility voltage magnitude. Applications that employ off-the-shelf machines are seriously limited by this constraint, because the machines are precluded from operating at rated voltage. The proposed matrix converters are

Table 2-1. Comparison of Conventional Matrix Converter with Proposed New Family of Converters

	Conventional Matrix Converter	Proposed New Matrix Converters
Voltage Conversion Ratio V_{out}/V_{in}	Buck only: $V_{out} < 0.866 V_{in}$	Buck-boost: $0 < V_{out} < \infty$
Switch Commutation	Coordination of 4-quadrant switches	Simple transistor plus freewheeling diode
Bus Bar Structure	Complex	Modular and simple
Multilevel Operation	No	Possible
Utility-Side Filter Elements	AC capacitors	Inductive
Machine-Side Filter Elements	Inductive	Inductive

capable of buck–boost operation, and suffer no such constraint; in this regard, their performance is similar to that of the DC link system.

In the conventional matrix converter, the switching of the four-quadrant switches must be carefully coordinated. This is accomplished by independent control of the antiparallel transistors within each four-quadrant switch (Alesina and Venturini 1989; Huber, Borojevic, and Burany 1989; Oyama et al. 1989). Such control is entirely feasible; nonetheless, note that it introduces an additional level of complexity in the controller. The proposed new matrix converters do not exhibit this behavior. Instead, the switching transitions represent simple commutations of a transistor and freewheeling diode, similar to the DC link converter.

The bus bar structures of conventional matrix converters, as well as of multilevel converters based on the DC link system, are quite complex. To avoid excessive voltage transients during the switching transitions, it is necessary to minimize the parasitic wiring and bus inductance in all circuit loops that carry AC currents with substantial high-frequency switching components. In recent commercial practice, this has been accomplished through bus bar structures that resemble multilayer printed circuit boards, and that often have built-in capacitors between some of the layers. Whenever a high-frequency transient current flows in a bus bar, the identical current flows in the opposite direction through an adjacent or overlapping bus bar. The magnetic fields of the currents in the two bus bars nearly cancel, and parasitic inductance is minimized. This minimizes the voltage transient applied to the semiconductor switch, reduces the need for snubbers and their associated loss, and improves reliability. In the matrix converter, it is necessary to overlap the bus bars of all nine switches, switch branches, and the three AC-side capacitors. In multilevel converters based on the DC link approach, the bus bars of all transistors, diodes, and capacitors must overlap. Very few manufacturers are able to fabricate such complex bus bar systems. In the proposed new family of matrix converters, only the bus bars within the H-bridge switch cells themselves must overlap. The modularity of the proposed converter considerably simplifies its physical construction.

That modularity also results in a path for directly scaling the design to higher voltage and power levels. Given a working design for the basic configuration of Figure 2-1, the power stage voltage and power levels can be increased by a factor of n by inserting $(n - 1)$ additional identical switch modules in each branch of the matrix. The power stage elements are otherwise unchanged. All that is needed is modification of the controller to properly switch the additional modules. We should point out that this type of scaling maintains the cost per rated kVA of the converter, provided that the cost of interconnections between modules can be kept sufficiently low.

In addition, we are attempting to construct switch modules using printed circuit boards instead of bus bars. Such construction has the further benefit of allowing automated fabrication of the circuitry, with reduced cost. The feasibility of this approach is a function of the voltage and current levels of the switch modules. We believe that 480-V 50-A (AC rms) switch modules are quite feasible using this approach, and higher ratings may be possible.

To the best of our knowledge, extensions of the conventional matrix converter to multilevel operation have not been proposed and are not known. However, as noted above, multilevel operation of the new family of matrix converters can be achieved.

Finally, the conventional matrix converter requires AC capacitors to be used at the high-voltage side of the converter. This configuration implies that exactly three switch branches conduct during each subinterval.

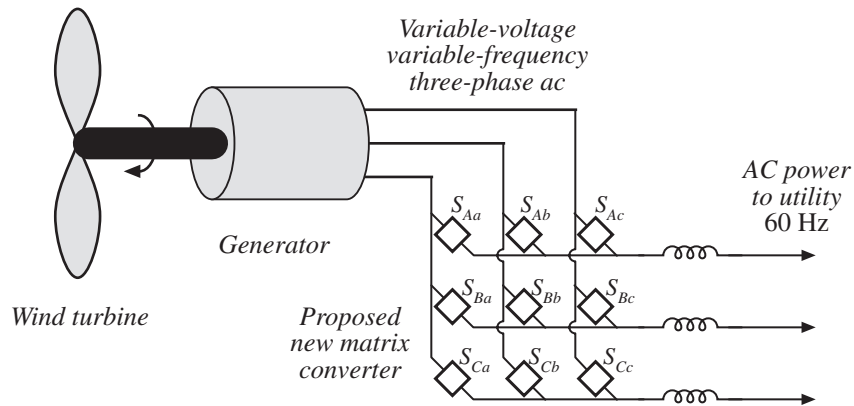


Figure 2-5. A variable-speed wind power system incorporating the basic version of the proposed new family of matrix converters

In contrast, the proposed converters employ inductive elements on both sides of the converter, and require five conducting branches during each subinterval. No AC capacitors are needed. We can see, then, that the basic operations of the two matrix converter approaches are fundamentally different.

2.3 IMPLEMENTING THE PROPOSED CONVERTERS IN WIND POWER APPLICATIONS

Figure 2-5 illustrates the use of the basic version of the proposed new family of matrix converters in a variable-speed wind generation application. For this example, the wind turbine is mechanically coupled to the shaft of a synchronous machine, either directly or through a gearbox. The magnetic excitation of the synchronous machine may be generated by a permanent magnet, or by a current flowing in a field winding. The synchronous machine produces variable-frequency variable-voltage AC. The converter interfaces this generator output to the constant-frequency constant-voltage utility system. At rated power and rated generator voltage, the converter operates with two-level voltage wave forms. When the generator voltage falls below a threshold, the converter is operated with three-level wave forms, thereby improving the efficiency under low wind conditions. Any of the well-known methods for controlling the machine may be employed, such as field-oriented control. In the system illustrated in Figure 2-5, the machine winding inductances are relied on to filter the switched wave forms produced by the converter; as an alternative, discrete inductors may be placed between the converter and machine. Also, discrete inductors are illustrated between the converter and utility in Figure 2-5; these inductors may be eliminated and the inductances inherent in the utility system (such as transformer leakage and distribution line inductances) can be relied on to filter the switched wave forms produced by the converter.

Figure 2-6 illustrates the employment of another member of the proposed new family of matrix converters in a similar variable-speed wind generation application. In this case, the converter functions with three-level operation at full power. Under light wind conditions, the modulation control strategy is altered to improve the efficiency; the converter may then operate with either three-level or five-level wave forms. Our previous discussion of realization of the generator-side and utility-side inductors also applies to this

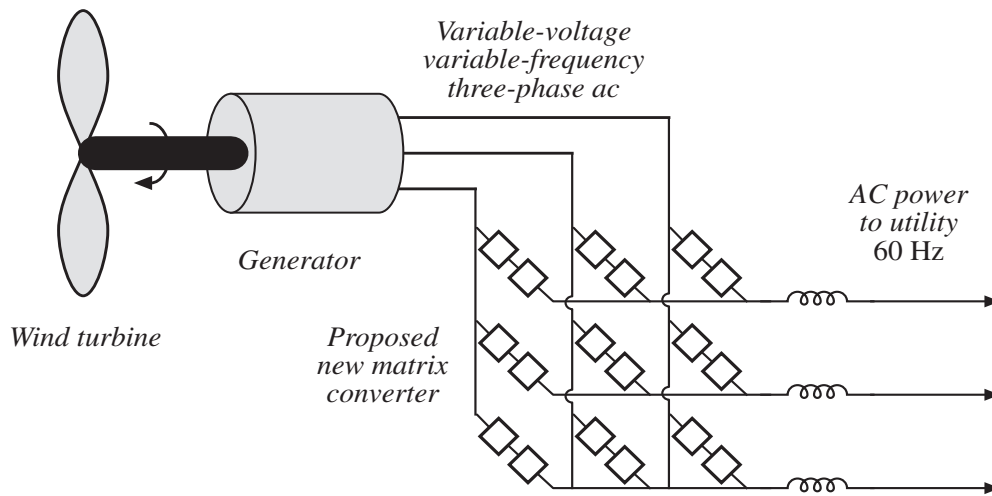


Figure 2-6. A variable-speed wind power system that incorporates the new multilevel matrix converter shown in Figure 2-3

system. Each branch of the matrix may contain one, two, or more switch cells.

In Figure 2-7, we depict the employment of one of the proposed new matrix converters in a similar wind generation system that incorporates a doubly fed machine as its electromechanical generator. The stator is directly connected to the utility; the rotor is interfaced through the converter to the utility. Again, we can

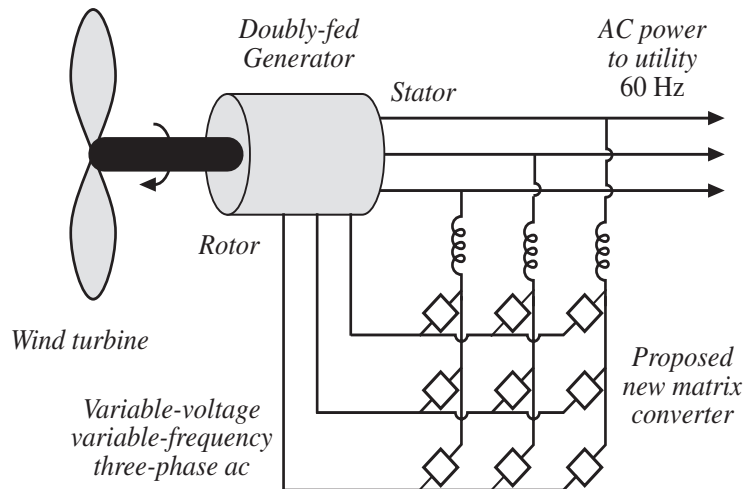


Figure 2-7. Using the basic member of the proposed new family of matrix converters in a wind power system that employs a doubly fed machine

choose to employ either discrete inductors or rely on other system inductances to filter the wave forms at the utility side and rotor side of the converter. Each branch of the matrix may contain one, two, or more switch cells.

3.0

Control of New Multilevel Matrix Converter

3.1 INTRODUCTION

The controller of the proposed multilevel matrix converter must perform two major tasks:

1. Maintain fixed voltage (charge regulation) across all midpoint capacitors.
2. Synthesize input and output voltage wave forms.

Control that simultaneously accomplishes these two tasks is demonstrated here. The SVM technique is extended to the case of controlling the input and output voltage wave forms of the proposed converter; at the same time, the controller regulates the capacitor voltages. In addition to offering a general analysis of the problem, we describe a relatively simple control strategy.

First, we must understand which switch states are allowable, and how the choice of switch states affects the terminal voltages of the matrix. The rules governing operation of the switch matrix are developed in Section 3.2, and we found that there are 19,683 valid combinations of switch states. These were sorted and tabulated in the Appendix of the Year 2 report. (Erickson, R.; Angkititrakul, S.; Al-Naseem, O.; Lujan, G. (January 28, 2002) “Novel Power Electronics Systems for Wind energy Applications,” *Year 2 Report*.)

The large number of combinations is at first quite daunting, and the resulting complexity can obscure the underlying physical behavior of the converter. Furthermore, it is possible that the DC capacitor voltages of the switch cells could exhibit instabilities—a capacitor that is charged from the input during one subinterval should transfer the charge to the output during a following subinterval. Yet such behavior is not guaranteed, and a control strategy could possibly charge one capacitor, then discharge another, leading to voltage imbalances and instabilities. However, these obstacles can be overcome by using the SVM technique and by choosing switch states that minimize converter complexity and guarantee capacitor charge balance.

The SVM technique is extended to the proposed new matrix converter in Section 3.3. In Section 3.3.1, we briefly review of the prior art and present clear definitions of relevant terminology. The space vectors attainable with the basic version of the proposed new family of converters are listed in Section 3.3.2. The basic configuration is capable of three-level switching under limited circumstances. In Section 3.3.3, we describe the application of SVM to the basic configuration. Finally, we present the simulation results in Section 3.3.4. These results show that the SVM technique can indeed be used in the proposed new converter, to generate input- and output-balanced three-phase wave forms of arbitrary frequency,

magnitude, and power factor. Further, the simulations demonstrate that it is indeed possible to control and stabilize the DC capacitor voltages of all nine switch cells. Although the simulation package employs the SVM technique, it does so in a somewhat brute-force manner, employing searches through the tables of the above referenced Appendix. Nonetheless, the simulations confirm the operation of the proposed converter.

We describe a significant improvement in Section 3.4. By carefully studying the allowed switch states and the SVM scheme, we found that only one capacitor must be charged and discharged during a given switching period. This effectively precludes the issue of capacitor voltage imbalances. It also allows simple regulation of the DC capacitor voltages, one at a time, through control of the converter input and output powers. For example, if the input power is reduced while the output power is maintained, the difference is supplied by the capacitor and the capacitor voltage decreases. With the proposed control strategy, some of the input power is transferred directly to the output. The remainder is alternately stored in a specific DC capacitor and is then discharged to the output. The simplicity of this approach leads to much greater understanding, as well as to tractable analytical results. This strategy can be employed whenever the generator voltage is greater than the utility voltage divided by the square root of three. Consequently, it is applicable (for example) to operation of a variable-speed wind generator with synchronous machine in Region III (constant power) and in part of Region II (peak power tracking). At lower voltages, an alternate approach involving simultaneous charging or discharging of two or more capacitors is required. It is also possible to apply the proposed new converter and control strategies to other wind generator systems, such as those incorporating doubly fed machines.

The limitation that only one capacitor participates in the power conversion process during a given switching period is not only a simplification, but it is also in some sense optimal. During a given switching period, some of the input power (the “direct power”) is transferred directly to the output terminals. The remainder of the input power (the “indirect power”) goes through the intermediate process of being first stored in a capacitor and then later released to the output. The indirect power invariably incurs more loss than the direct power, improving efficiency when the indirect power is minimized (Wolaver 1969; Kassakian, Schlecht, and Vergese 1991). The simultaneous participation of multiple capacitors in the power conversion process may imply that additional indirect power circulates between the capacitors, leading to reduced efficiency.

We summarize the proposed control system in Section 3.5.

3.2 SWITCH STATES

In this section, we present an analysis of the basic configuration of the proposed new multilevel matrix converter, in which one switch cell is used for each branch of the matrix converter. The term “branch” refers to a connection between one input phase and one output phase using one or more switch cells. For example, branch Aa refers to a connection between phase A and phase a , using (for the basic configuration) switch cell S_{Aa} . Figure 3-1 shows a simplified circuit schematic of the multilevel matrix converter.

Switch cells S_{Aa} , S_{Ab} , S_{Ac} , S_{Ba} , S_{Bb} , S_{Bc} , S_{Ca} , S_{Cb} , and S_{Cc} are realized using H-bridges with DC capacitor voltages as described in the previous chapter, and operate as four-quadrant switches. In addition, they are capable of applying their DC capacitor voltages across their terminals. As with the conventional matrix converter, the operation of the new matrix converter has special constraints. First, because of the existence of inductors, current must flow continuously through the input and output phases. The operation of the switch cells, then, must never result in an open circuit applied to an input or output phase. Second, the converter branches must never conduct in a way that forms a closed loop within the switch matrix. Third, to avoid high voltage stresses on the semiconductor devices and to allow antiparallel diodes to be used within the switch cells, the total voltage applied across an open switch cell must never exceed the magnitude of the DC capacitor voltage within the open cell. These constraints imply that the converter must operate with exactly five branches conducting at any instant, and also further limit the allowed combinations of conducting switch cells. With nine branches in the switch matrix, and with one switch cell per branch (for the basic configuration of the proposed converter), there are 81 cases of branch connections to connect the three input phases to the three outputs. There are three general rules for operating the novel multilevel matrix converter:

1. There is exactly one and only one conducting path between any two phases.
2. If any phase on one side (i.e., input side or output side) has two conducting branches (i.e., is connected to two phases from the other side), there must be exactly one other phase from the same side having two conducting branches. The third phase must be connected directly to one conducting branch.
3. If any phase on one side (i.e., input side or output side) has three conducting branches (i.e., connected to all phases from the other side), the other two phases from the same side must each have one and only one conducting branch.

Table 3-1 summarizes the configurations and possible number of branches that may be used to connect a set of three input phases to a set of output phases. The sum of connected branches is always equal to five. Table 3-2 shows a detailed listing of the first 27 cases, from a total of 81 cases, of branch connections used in the novel multilevel matrix converter. In this table, the three left-most columns show which input phases are connected directly through conducting branches to which output phases. From left to right, columns

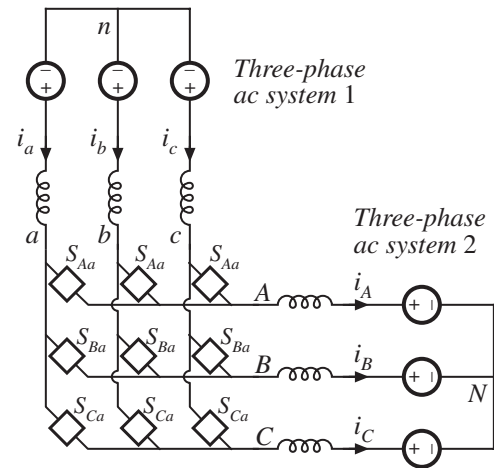


Figure 3-1. Basic configuration of the proposed multilevel matrix converter

Table 3-1. Configurations of Branch Connections

Phase A or Phase a	Phase B or Phase b	Phase C or Phase c
1 branch	1 branch	3 branches
1 branch	2 branches	2 branches
1 branch	3 branches	1 branch
2 branches	1 branch	2 branches
2 branches	2 branches	1 branch
3 branches	1 branch	1 branch

4–12 show the status of each of the nine branches of the converter. The number “1” denotes a conducting branch and “0” denotes an open-circuited branch. Results similar to those of Table 3-2 may be obtained for the remainder of the 81 cases of branch connections by rotating only one set of three phases, either input or output, by 120° and 240°.

	A	B	C
a			
b			
c			

Figure 3-2. Matrix used to test for validity of Figure 3-3 branch connections

To graphically test for the validity of a switching combination, we can construct a matrix as shown in Figure 3-2. The graph resembles the Karnaugh map used for logic design. The upper row entries are labeled A, B, and C to represent phases A, B, and C at one side of the multilevel matrix converter. The left column squares are labeled a, b, and c to represent phases a, b, and c at the other side of the multilevel matrix converter. Now, draw an “X” mark inside any five squares to represent a closed branch. Leave the other squares empty to represent open branches. A closed branch combination is valid if and only if there is no set of four “X’s” forming a square or rectangle. Such a forbidden case of four squares represents a closed loop of

connected branches, linking two phases at one side of the converter to another two phases at the other side of the converter. The loop thus formed could result in shorting of DC capacitors within the loop switch cells. Figure 3-3 gives some examples of valid and invalid branch switch combinations.

In addition to varying the branch connections, control can be asserted by varying the switch states within the switch cells of conducting branches. Each switch cell has two nodes, at the midpoints between the switches of each half bridge, where the cell is connected to the remainder of the converter. These nodes are denoted X and Y. The capacitor internal to the switch cell is charged to voltage V_{cap} . There are a number of possibilities for selection of these switch states:

- State 1: The voltage V_{cap} is applied between nodes X and Y, with node X being positive with respect to node Y. When the current flowing into node X is positive, diodes will conduct the current and the capacitor is charged. When the current flowing into node X is negative (i.e., the current flows out of node X), two transistors must be turned on, and the capacitor is discharged.

Table 3-2. First 27 Cases of Possible Branch Connections

Phase			Branch connections								
A	B	C	(1 = connected, 0 = not connected)								
is connected to phases			Aa	Ab	Ac	Ba	Bb	Bc	Ca	Cb	Cc
a	a	abc	1	0	0	1	0	0	1	1	1
a	b	abc	1	0	0	0	1	0	1	1	1
a	c	abc	1	0	0	0	0	1	1	1	1
b	a	abc	0	1	0	1	0	0	1	1	1
b	b	abc	0	1	0	0	1	0	1	1	1
b	c	abc	0	1	0	0	0	1	1	1	1
c	a	abc	0	0	1	1	0	0	1	1	1
c	b	abc	0	0	1	0	1	0	1	1	1
c	c	abc	0	0	1	0	0	1	1	1	1
a	ab	ac	1	0	0	1	1	0	1	0	1
a	ab	bc	1	0	0	1	1	0	0	1	1
a	ac	ab	1	0	0	1	0	1	1	1	0
a	ac	bc	1	0	0	1	0	1	0	1	1
a	bc	ab	1	0	0	0	1	1	1	1	0
a	bc	ac	1	0	0	0	1	1	1	0	1
b	ab	ac	0	1	0	1	1	0	1	0	1
b	ab	bc	0	1	0	1	1	0	0	1	1
b	ac	ab	0	1	0	1	0	1	1	1	0
b	ac	bc	0	1	0	1	0	1	0	1	1
b	bc	ab	0	1	0	0	1	1	1	1	0
b	bc	ac	0	1	0	0	1	1	1	0	1
c	ab	ac	0	0	1	1	1	0	1	0	1
c	ab	bc	0	0	1	1	1	0	0	1	1
c	ac	ab	0	0	1	1	0	1	1	1	0
c	ac	bc	0	0	1	1	0	1	0	1	1
c	bc	ab	0	0	1	0	1	1	1	1	0
c	bc	ac	0	0	1	0	1	1	1	0	1

	A	B	C
a	X	X	
b	X	X	
c			X

INVALID

	A	B	C
a	X	X	X
b			X
c			X

VALID

	A	B	C
a	X	X	
b			
c	X	X	X

INVALID

	A	B	C
a			X
b		X	X
c	X		X

VALID

	A	B	C
a	X		X
b	X		X
c			X

INVALID

	A	B	C
a	X		
b		X	X
c	X		X

VALID

	A	B	C
a	X		X
b			X
c	X		X

INVALID

	A	B	C
a	X	X	X
b	X		
c	X		

VALID

Figure 3-3. Examples of valid and invalid branch connections

- State 2: The voltage V_{cap} is applied between nodes X and Y , with node Y being positive with respect to node X . When the current flowing into node X is positive, transistors must be turned on to conduct the current, and the capacitor is discharged. When the current flowing into node X is negative (i.e., the current flows out of node X), two diodes are forward-biased, and the capacitor is charged.
- State 3: Nodes X and Y are shorted together. This can be accomplished by turning on either the upper transistors or the lower transistors of the H-bridge. In either case, one transistor and one diode will conduct. It is advantageous to alternate the conducting devices, so that conduction losses are distributed evenly over the devices.
- State 4: In this state, all devices are off, and the switch cell does not conduct. The switch cell is capable of blocking voltages applied between terminals X and Y that are less than or equal to the DC capacitor voltage V_{cap} . If a larger voltage is applied, diodes within the switch cell will become forward-biased, and the cell will revert to state 1 or 2.

We can see, then, that there are three possible states for each conducting switch cell. In the basic configuration of the new multilevel matrix converter, exactly five switch cells conduct at any given instant. Therefore, there are $3^5 = 243$ possible combinations of switch states for a given branch connection. As shown above, there are 81 possible branch connections. This leads to $243 \cdot 81 = 19,683$ combinations of switch states and branch connections in the proposed converter. However, not all of these combinations are valid, and most of them can be generated by rotation of the input and/or output phases of previously generated combinations. The Appendix of the Year 2 report.(Erickson, R.; Angkititrakul, S.; Al-Naseem, O.; Lujan, G. (January 28, 2002) “Novel Power Electronics Systems for Wind energy Applications,” *Year 2 Report*.) includes a listing of combinations. This appendix is ordered first by the branch connections of Table 3-2, and then by the individual switch states.

Figure 3-4 shows an example of three different switching combinations, for the choice of branch connection having branches Aa , Ba , Ca , Cb , and Cc conducting, and branches Ab , Ac , Bb , and Bc open (disconnected). Branch Aa uses switch cell S_{Aa} , branch Ba uses switch cell S_{Ba} , and so on. This figure also shows that it is possible to obtain five different line-to-line voltage levels from the basic configuration of the new multilevel matrix converter, having only one switch cell per branch. The DC capacitor voltages of the switch cells, V_{cap} , are each set to +240 V. The configuration of Figure 3-4(a) produces 0 V for all line-to-line voltages on both sides of the converter. This is done by operating all switch cells of the connected branches in state 2. Of course, the same result can be obtained in other ways, such as by operating all switch cells in state 3 as shorts. Figure 3-4(b) illustrates what happens when one switch cell (S_{Cc}) is changed to state 3. The converter then produces three-level line-to-line output voltages of -240 V, 0 V, and +240 V. Figure 3-4(c) illustrates the result of changing switch cell S_{Cc} to state 1. The line-to-line output voltages are now -480 V, 0 V, and +480 V. By alternating between the three device-switching combinations of Figure 3-4, the new multilevel matrix converter could produce five-level line-to-line voltage wave forms with voltage levels at -480 V, -240 V, 0 V, 240 V, and 480 V at one side of the converter.

As we noted previously, when in state 4 the switch cells can block voltages that are less than or equal to the DC capacitor voltage V_{cap} of the cell. This imposes another constraint on the choice of switching combinations. To avoid applying voltages exceeding V_{cap} across an open switch cell (state 4), the set of three-phase line-to-line voltages on one side of the converter must remain at zero whenever the set of instantaneous line-to-line voltages of the other side exceeds V_{cap} . For example, in the device-switching

UTILITY SIDE

GENERATOR SIDE

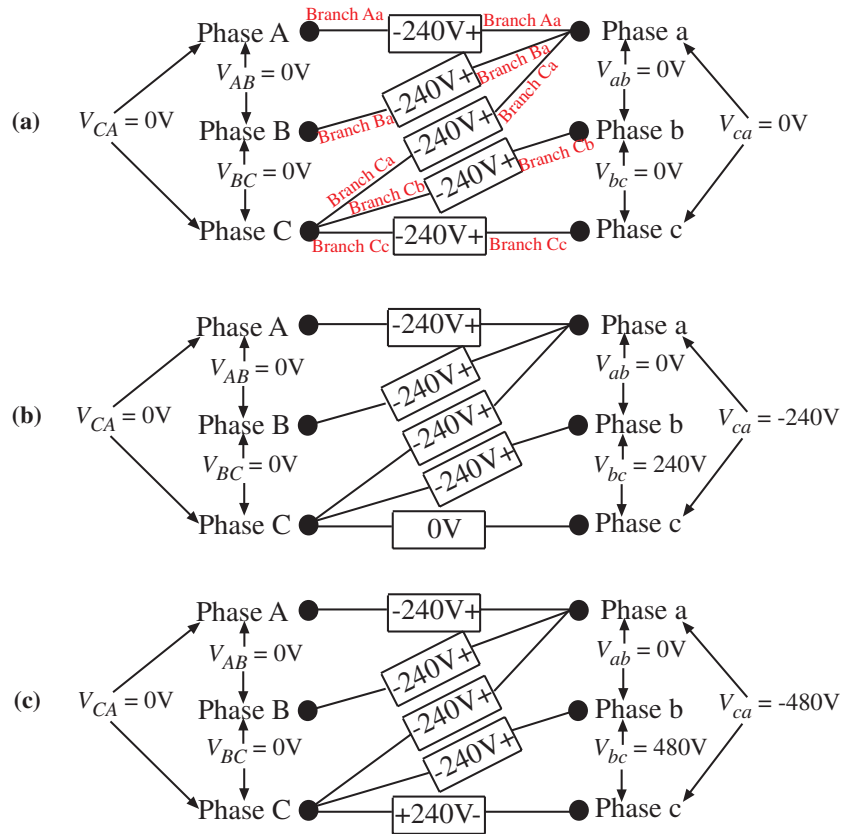


Figure 3-4. Three different switching combinations, each for the same choice of branch connections. The resulting line-to-line input and output voltages are shown.

combination of Figure 3-4(c), the utility sides of the converter line-to-line voltages are each equal to zero, while the line-to-line voltages of the generator side exceed the voltage $V_{cap} = 240$ V. It can be verified that the switch cells of all open branches block voltage magnitudes equal to V_{cap} .

Figure 3-5 shows an example of a disallowed device-switching combination in which voltage stresses are tripled for each of the switch cells that are in state 4. In other words, a nonconducting switch cell is required to block voltage magnitudes greater than V_{cap} . In this case, $3V_{cap}$ is applied across each

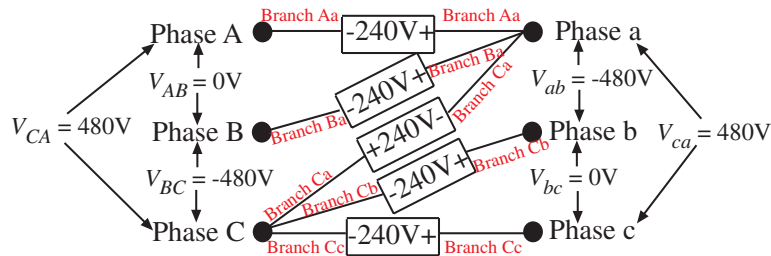


Figure 3-5. Disallowed switching combination, having line-to-line voltages of magnitude $2V_{cap}$ simultaneously at the input and output ports. The nonconducting switch cells must block voltages of $3V_{cap}$.

nonconducting switch cell. As we explained previously, this would forward-bias diodes within the switch cell, changing the conduction state from state 4 to states 1 or 2. This switching combination, then, does not work. Therefore, combinations that require switch cells to block voltages greater than V_{cap} are not allowed. Examining all possible switching combinations reveals that this excludes all switching combinations having line-to-line voltages of $2V_{cap}$ on one side, and nonzero voltages on the other side. However, combinations having at least one line-to-line voltage of $2V_{cap}$ on one side with zero voltages on the other side are allowed; one such example is Figure 3-4(c).

The discussion of the previous paragraph admits the possibility that the basic version of the new multilevel matrix converter may be able to operate with multilevel switching under low wind conditions. As we discussed in Chapter 2, this may lead to improved efficiency at low wind. The capacitor voltages would be reduced by a factor of one-half when the generator voltage is sufficiently less than half of the utility voltage. It would then be possible to use multilevel switching to step the generator voltage up to the (reduced) DC capacitor voltage, and still interface to the full-magnitude utility voltage.

3.3 SPACE VECTOR CONTROL

SVM is one attractive approach to controlling the novel multilevel matrix converter. In this section, we present an overview of the SVM technique, and include a detailed explanation of how to adapt SVM in the control of the new multilevel matrix converter. We describe a relatively simple control algorithm that both implements space vector control and also allows for control of the DC capacitor voltages.

3.3.1 Review of d - q Transformation and SVM Techniques

Originally used to analyze three-phase AC machines, space vector control is now adopted to control three-phase power electronic converters. SVM has recently gained popularity as an alternative to conventional PWM techniques for controlling three-phase converters. The major reason for this lies in SVM's ability to control the operation of the entire converter through modulation between the converter space vectors in the d - q reference frame. Furthermore, SVM can be performed to result in minimum switching of semiconductor devices. This reduction in device switching consequently reduces switching loss in the SVM-controlled converter.

SVM is based on the transformation of a three-wire three-phase system into a simpler two-coordinate systems without loss of information (Huber, Borojevic, and Burany 1989). As only two phases are independent in the three-phase converters we consider here, we can simplify the analysis of the three-phase systems by transforming the three phases into an equivalent two-phase d - q reference frame using the following d - q transformation:

$$\mathbf{v}(t) = \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} \cos(0) & \cos\left(\frac{2\pi}{3}\right) & \cos\left(\frac{4\pi}{3}\right) \\ \sin(0) & \sin\left(\frac{2\pi}{3}\right) & \sin\left(\frac{4\pi}{3}\right) \end{bmatrix} \begin{bmatrix} v_{ab}(t) \\ v_{bc}(t) \\ v_{ca}(t) \end{bmatrix} \quad (3-1)$$

In rotating machine theory, it is customary to transform three-phase systems into equivalent two-phase systems in this manner. Additionally, it is common practice to perform a second transformation that converts the rotating stator wave forms into a frame of reference that is stationary with respect to the rotor. This removes the time-dependence of steady-state wave forms:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} \quad (3-2)$$

The transformation of Equation 3-2 is useful for control of the three-phase line currents, but is not directly used in space vector control. It should be noted that this second transformation is not included in Equation 3-1; hence, in steady state the quantities $v_d(t)$ and $v_q(t)$ are sinusoids. The vector $\mathbf{v}(t)$ of Equation 3-1 can be represented in complex form as follows:

$$\vec{v}(t) = v_d(t) + jv_q(t) \quad (3-3)$$

This form appears similar to a phasor, except that the time dependence of the sinusoids is still retained. Equation 3-3 represents a complex space vector. When the space vector lies on the positive direct axis (i.e., when v_q is zero and v_d is positive), the line-to-line voltage $v_{ab}(t)$ attains its maximum positive value.

In space vector control of a three-phase converter, the complex space vectors produced by each valid switch state are tabulated. Producing a sinusoidal output that corresponds to a rotating complex space vector is desirable, and this is achieved through PWM of the complex space vectors generated by converter switch states.

For example, consider the conventional voltage-source inverter of Figure 3-6. There are eight valid switch states for this converter, in which exactly one switch per phase conducts. These switch states are listed in Table 3-3, along with the resulting line-to-line output voltages. Evaluating Equation 3-1 for each switch state leads to the transformed two-phase voltages listed in the table.

When the two-phase voltages of Table 3-3 are plotted as space vectors according to Equation 3-3, we obtain the space vector diagram shown in Figure 3-7. We can see that, in addition to the zero vector, six space vectors are evenly spaced around a circle of radius $\sqrt{3}V_{dc}$. These vectors represent the instantaneous voltages that can be produced by the switch network.

It is usually desirable to produce balanced three-phase sinusoidal output voltages. In the space vector domain, this corresponds to producing a space vector of constant amplitude, which rotates at the desired frequency. To minimize the low-frequency harmonics, PWM is used to produce average space vectors that

Figure 3-6. Conventional DC–3 ϕ AC voltage-source inverter

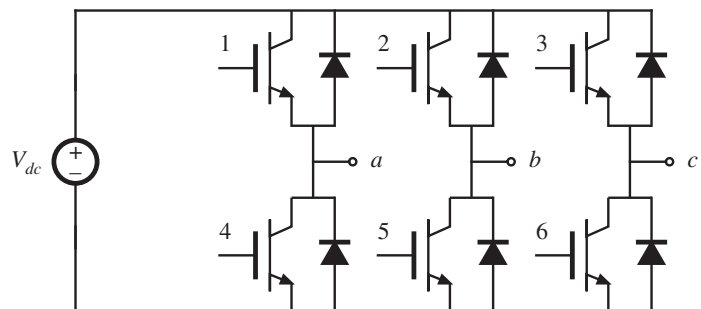
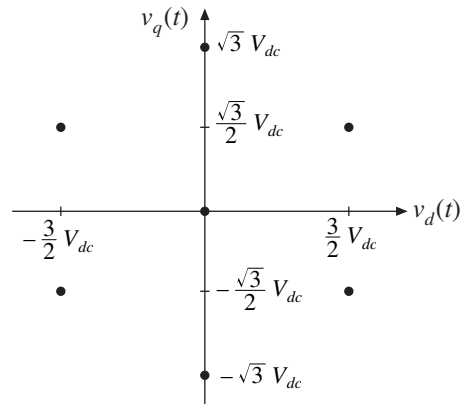


Table 3-3. Space Vectors, Voltage-Source Inverter Example

Conducting switches	v_{ab}	v_{bc}	v_{ca}	v_d	v_q
123 or 456	0	0	0	0	0
156	V_{dc}	0	$-V_{dc}$	$\frac{3}{2}V_{dc}$	$\frac{\sqrt{3}}{2}V_{dc}$
264	$-V_{dc}$	V_{dc}	0	$-\frac{3}{2}V_{dc}$	$\frac{\sqrt{3}}{2}V_{dc}$
345	0	$-V_{dc}$	V_{dc}	0	$-\sqrt{3}V_{dc}$
126	0	V_{dc}	$-V_{dc}$	0	$\sqrt{3}V_{dc}$
234	$-V_{dc}$	0	V_{dc}	$-\frac{3}{2}V_{dc}$	$-\frac{\sqrt{3}}{2}V_{dc}$
315	V_{dc}	$-V_{dc}$	0	$\frac{3}{2}V_{dc}$	$-\frac{\sqrt{3}}{2}V_{dc}$

Figure 3-7. The seven space vectors that can be generated by the conventional voltage-source inverter

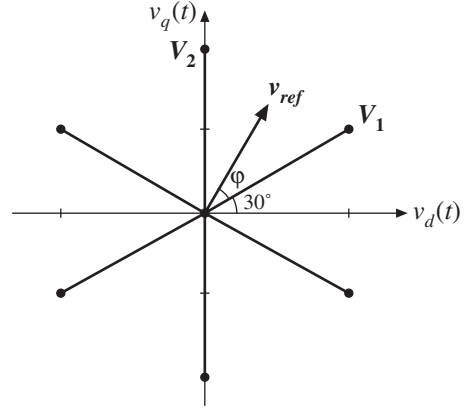


lie between the points illustrated in Figure 3-7. For example, suppose that we wish to generate the following balanced three-phase line-to-line voltages:

$$\begin{aligned}
 v_{ab}(t) &= V_m \cos(\omega t) \\
 v_{bc}(t) &= V_m \cos(\omega t - 120^\circ) \\
 v_{ca}(t) &= V_m \cos(\omega t - 240^\circ)
 \end{aligned}
 \tag{3-4}$$

By substitution into Equation 3-1, we find that these voltages correspond to a two-phase voltage representation of

Figure 3-8. At some time t , the desired space vector $v_{ref}(t)$ lies between space vectors V_1 and V_2 that can be generated during single switch states by the inverter circuit.



$$v_{ref}(t) = \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} \cos(0) & \cos(120^\circ) & \cos(240^\circ) \\ \sin(0) & \sin(120^\circ) & \sin(240^\circ) \end{bmatrix} \begin{bmatrix} V_m \cos(\omega t) \\ V_m \cos(\omega t - 120^\circ) \\ V_m \cos(\omega t - 240^\circ) \end{bmatrix} = \begin{bmatrix} \frac{3}{2} V_m \cos(\omega t) \\ \frac{3}{2} V_m \sin(\omega t) \end{bmatrix} \quad (3-5)$$

which constitutes a space vector of constant amplitude $1.5V_m$, rotating at angular frequency ω .

At a given time t , the desired space vector $v_{ref}(t)$ can be represented as a linear combination of the space vectors of Figure 3-7. For example, consider the case illustrated in Figure 3-8. At the given time, the desired space vector $v_{ref}(t)$ lies between the space vector V_1 (which is generated by turning on switches 1, 5, and 6) and space vector V_2 (generated by turning on switches 1, 2, and 6). Hence $v_{ref}(t)$ can be expressed as follows:

$$v_{ref} = d_1 V_1 + d_2 V_2 + d_0 V_0 \quad (3-6)$$

where V_0 is the zero vector (generated by turning on switches 1, 2, and 3 or 4, 5, and 6), and where

$$d_1 + d_2 + d_0 = 1 \quad (3-7)$$

This representation is illustrated in Figure 3-9. Vector addition is used to express v_{ref} in terms of V_1 , V_2 , and the zero vector V_0 . Equation 3-6 suggests a way to use PWM to generate a three-phase output voltage whose average value follows a given three-phase reference: switch between space vectors V_1 , V_2 , and V_0 with duty cycles d_1 , d_2 , and d_3 , respectively. The average values of the three-phase output voltages will then follow v_{ref} .

It remains to solve the vector diagram of Figure 3-9 to find the duty cycles d_1 and d_2 . The diagram of Figure 3-9 is sketched in more detail in Figure 3-10. A dashed line that is orthogonal to V_1 is extended from V_1 to v_{ref} . By solution of the right triangle formed by this line and the v_{ref} vector, we find that the length of the dashed line is:

$$V_{ref} \sin \phi \quad (3-8)$$

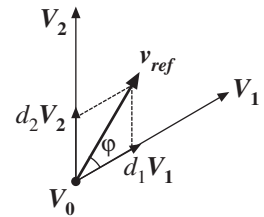


Figure 3-9. Expressing v_{ref} as a linear combination of V_1 , V_2 , and V_0

where V_{ref} is the magnitude of the vector v_{ref} . Figure 3-10 also illustrates a $30^\circ-60^\circ-90^\circ$ triangle (dashed lines). Solution of this triangle leads to:

$$V_{ref} \sin \varphi = d_2 V_2 \sin 60^\circ \quad (3-9)$$

where V_2 is the magnitude of the vector V_2 . Solution for the duty cycle d_2 and simplification of the result yields

$$d_2 = \frac{V_{ref}}{V_2 \sin 60^\circ} \sin \varphi = \frac{2}{\sqrt{3}} \frac{V_{ref}}{V_2} \sin \varphi \quad (3-10)$$

This is the equation used to select the duty cycle d_2 . A similar analysis leads to the following equation for the duty cycle d_1 :

$$d_1 = \frac{V_{ref}}{V_1 \sin 60^\circ} \sin (60^\circ - \varphi) = \frac{2}{\sqrt{3}} \frac{V_{ref}}{V_1} \sin (60^\circ - \varphi) \quad (3-11)$$

Given the above solutions for d_1 and d_2 , the remaining duty cycle d_0 can be found by solving Equation 3-7:

$$d_0 = 1 - d_1 - d_2 \quad (3-12)$$

Thus, in each 60° sector of Figure 3-8, the reference vector is expressed as a linear combination of neighboring space vectors. PWM according to Equations 3-10 through 3-12 generates the desired average space vector.

Although the above analysis is applied to the conventional voltage-source inverter, the results can be generalized to other converter circuits as well.

3.3.2 Space Vectors Attainable with the Basic Configuration of the New Converter

We can use the process described in the last section to find all possible voltage space vectors synthesized by the new multilevel matrix converter. Using the $d-q$ transformation procedure of Equation 3-1 and the three-phase line-to-line voltages of the possible device-switching combinations summarized in Section 3.2, we find that each side of the multilevel matrix converter can generate a total of 19 different voltage space vectors. In other words, each device-switching combination can place the input side, as well as the output side, into one of the 19 different voltage space vectors. The input-side voltage space vector may be different from the output-side space vector for a particular device-switching combination.

Figure 3-11 shows the space vector diagram of one side of the proposed multilevel matrix converter. The voltages are expressed with respect to the DC capacitor voltage V_{cap} . The null voltage space vector $(0, 0)$ resides in the center of the space vector diagram. The null space vector corresponds to the device switching combinations that generate three-phase voltages with amplitudes of zero. There are also six voltage space vectors with magnitude equal to $\sqrt{3}V_{cap}$. These correspond to device switching combinations that produce three-phase line-line voltages with amplitudes equal to and not exceeding V_{cap} ; the phases of these vectors coincide with the positive and negative peaks of the line-to-neutral voltages. This inner ring of space vectors is identical to the voltage-source inverter space vectors of Figure 3-7. The SVM technique we described in the previous section can be extended to apply here, using only this inner ring of space vectors.

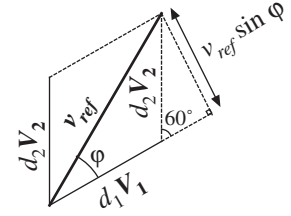
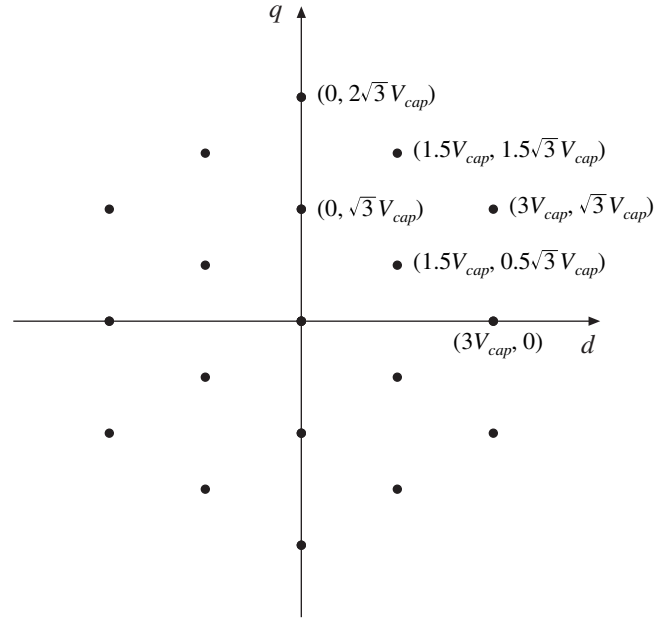


Figure 3-10. Magnified view of Figure 3-9, used to solve for duty cycles

Figure 3-11. Attainable voltage space vectors for the basic configuration of the proposed multilevel matrix converter. Values are labeled in the first quadrant; other quadrants are symmetrical.



The remaining 12 voltage space vectors, which have magnitudes greater than $\sqrt{3}V_{cap}$, correspond to device-switching combinations that result in three-phase voltages with amplitudes greater than V_{cap} . In fact, the different magnitudes of voltage space vectors represent the different voltage levels in which the new multilevel matrix converter can synthesize. Recall from Section 3.2 that if the amplitude of the three-phase voltages at one side of the multilevel matrix converter exceeds V_{cap} , the voltages at the other side of the converter must remain at zero to maintain a maximum blocking voltage of V_{cap} across the devices of all open switch cells (i.e., to avoid forward-biasing the diodes of nonconducting switch cells). In consequence, the 12 high magnitude voltage space vectors do not find useful application when near-rated voltage appears at both input and output (i.e., at rated wind speed). However, when operating with one side at substantially reduced voltage, which would be the case in a variable-speed wind generator at low wind, the outer ring of 12 space vectors can be employed to attain multilevel switching in the basic converter configuration. This would require that the capacitor voltage V_{cap} be reduced at these operating points. We believe that this would allow the benefits of multilevel switching (i.e., improved efficiency at low wind) to be achieved in the basic configuration depicted in Figure 3-1.

3.3.3 Space Vector Control of Proposed Converter

We can now apply the conventional space vector control method of Section 3.3.1 to the proposed new converter, using the space vectors of Figure 3-11. At a given instant in time, the desired reference space vectors for the generator and utility sides of the converter are given. Each reference space vector lies within one of the 60° sectors defined in Figure 3-8; this defines the choice of space vectors V_1 and V_2 for the input and output sides of the converter. For each side, the duty cycles d_0 , d_1 , and d_2 are computed using Equations 3-10 through 3-12. The switching period is then divided into five subintervals, with timing arranged such that both input and output are driven with the correct duty cycles and space vectors.

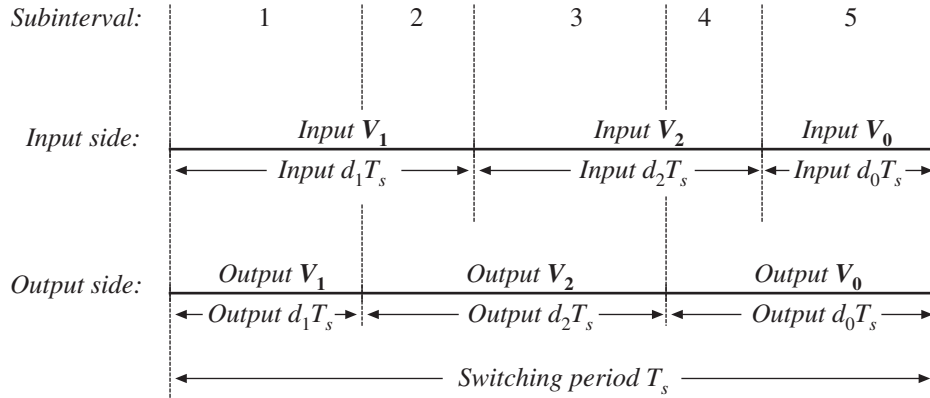


Figure 3-12. Space vector control of proposed new matrix converters: dividing the switching period into five subintervals, for the example of Section 3.3.3.

Figure 3-12 gives an example. The input and output sides are driven with their respective space vectors and duty cycles as described above. Because the input- and output-side duty cycles are different, the switching of the input- and output-side space vectors occurs at different times. We can see that five distinct subintervals occur during each switching period. In the example of Figure 3-12, the input and output sides are each driven with their respective V_1 space vectors during the first subinterval. We can search the tabulated list of switch combinations to select a valid combination of switch states that leads simultaneously to the desired input and output space vectors for this subinterval. During the second subinterval, the output side has switched to its V_2 space vector; the input side remains at its V_1 space vector. Again, we can search the list and select one of the switch combinations that yields this combination of input- and output-side space vectors. The process repeats for the following subintervals. We should note that the order of the subintervals is arbitrary, and that it may be advantageous to sequence the input- and output-side space vectors differently. Considerable optimization is possible, through careful selection of the switch states and through sequencing of the subintervals, and we cover one such strategy in Section 3.4.

3.3.4 Simulation Results

To demonstrate the operation of the proposed new matrix converter, and to verify the feasibility of space vector control and control of the capacitor voltages, we developed a simulation program. This program was written using Microsoft Visual Basic 6 and runs on the PC. We have delivered a CD containing the program to NREL, but present the details of the algorithm used in the simulation program here. Simulation results are obtained showing satisfactory operation of the multilevel matrix converter at different operating points. Plots were obtained for the generator and utility line-to-line voltages and phase currents. Furthermore, the simulator provides harmonic analysis to show the magnitudes of various harmonics of the generated SVM voltage wave forms. These results prove the feasibility of constructing converters using the simple switch cell based on the H-bridge, in which the DC voltage is provided by a capacitor rather than a DC source that supplies average power.

Initially, the main objective was to write a program to determine the possible 19,683 device-switching combinations, sort them, store them into a lookup table, and transform the voltages synthesized by the device-switching combinations into $d-q$ space vector coordinates. We entered all 81 cases of branch connections into the simulation program code manually. Each case of branch connection was an independent subroutine that was called by the main program. A loop was incorporated within each subroutine to account for the different device-switching combinations in the branch connection. The results are described in Sections 3.2 and 3.3, as well as in the previously mentioned appendix of the Year 2 report.

After determining the 19,683 possible device-switching combinations, the next objective was to apply SVM to synthesize three-phase AC voltages on the generator and utility sides of the new matrix converter. The simulator algorithm for this function is as follows:

- Read the instantaneous generator- and utility-side voltages. The rate at which these voltages are read constitutes the switching frequency.
- Perform $d-q$ transformation of these voltages into a space vector diagram. Two sets of $d-q$ coordinates are deduced; one for the generator-side voltages and another for the utility-side voltages.
- Derive space vector duty ratios for the SVM as described above.
- Divide each switching period into several subintervals.
- Search for a device-switching combination to synthesize the generator- and utility-side wave forms for the first switching period subinterval.
- Increment the time and search for a device-switching combination to synthesize the generator- and utility-side wave forms for the next switching period subinterval, repeating until the switching period is complete. The number of switching period subintervals defines the resolution of the PWM duty ratios. More subintervals leads to more resolution.
- Read another set of instantaneous generator- and utility-side voltages, and repeat the above steps.

Using SVM, the converter is able to successfully synthesize PWM voltage wave forms whose fundamental components match the desired references. Indeed, this can be done using only one branch connection, which included only 243 device-switching combinations. However, such operation does not guarantee that the DC capacitor voltages will remain stable.

The next task was to operate the multilevel matrix converter while maintaining capacitor voltages at a fixed DC level (approximately 240 V for the example we give in this section). The capacitor charge depends not only on the modulation scheme, but also on the applied terminal currents. Therefore, the generator- and utility-side phase currents must be modeled in this task, to determine the change in capacitor charge during each subinterval. The converter state space equations are integrated by the program, to compute capacitor charge and voltage levels.

Each device combination has its own reduced state matrix \mathbf{B} , as explained in Al Naseem (2001). Given the values of the phase currents, the branch currents may be computed using the inverse of matrix \mathbf{B} . For this reason, we added code to the simulation program to find the inverse of matrix \mathbf{B} for each different branch connection. The simulator then searches for the device-switching combinations that produce the desired input and output voltages. Next, each searched device-switching combination is tested to determine whether it can maintain the capacitor voltages within a $\pm 5\%$ variation from the desired 240 V. If a searched device switching combination cannot maintain the capacitor voltages within the $\pm 5\%$ set limit, a search for another device-switching combination is performed. If no adequate device-switching combination is found, the $\pm 5\%$ limit is incremented by one to $\pm 6\%$. This process may repeat until the

limit reaches $\pm 12\%$. If an adequate device-switching combination is found, the limit is decremented by one. This process repeats until the limit falls back to $\pm 5\%$. If the limit reaches $\pm 12\%$, and there are still no valid device-switching combinations, the simulator searches for any random device-switching combination that can return the capacitor voltages to within their original $\pm 5\%$ limit. Although this random device-switching combination does not follow the space vector control algorithm, and hence does not synthesize the appropriate input and output voltages, its effect on distortion of the synthesized wave forms is negligible because it occurs for a short time. This is confirmed through harmonic analysis of the synthesized wave forms up to the 26th harmonic order. Furthermore, device gating signal times during a single switching period were allowed to be divided (if necessary) into randomly nonconsecutive time intervals. This added more flexibility in finding a device-switching combination that produces the appropriate voltages while regulating the capacitor voltages.

The algorithm we described above is not intended to be a practical control approach for on-line converters. Instead, it is intended to prove that the converter can work, and can perform the required power conversion functions while maintaining the DC capacitor voltages. With this algorithm, the multilevel matrix converter has been shown to function properly, producing the expected voltage and current wave forms. Plots of generator- and utility-side wave forms are generated by the simulator and are included in the list below to show the ability of the multilevel matrix converter to operate at various operating points and with universal input and output power factors. The simulator also generates plots of the harmonic spectrum of utility-side line-to-line voltage v_{AB} and generator-side line-to-line voltage v_{ab} . The simulation program also provides plots of variations in capacitor voltages to prove the feasibility of regulating the capacitor charge. Switch cell states are also displayed in a plot showing the operation of the SVM and capacitor charge regulation controls. In addition to the produced wave forms, the simulator also generates text files describing the exact operation of the multilevel matrix converter during simulation run time.

- **Simulated operating point 1:** Utility side: 240 V, 60 Hz, 11 A, unity power factor. Generator side: 240 V, 25 Hz, unity power factor. Switching frequency: 1 kHz. Figure 3-13 shows simulator-generated wave forms for three-phase AC utility voltages at 240 V and 60 Hz, and with currents at 11 A at unity power factor. Figure 3-14 shows the harmonic spectrum of utility-side line-to-line voltage v_{AB} . Notice the high magnitudes of harmonics in the vicinity of the 18th harmonic. These harmonics represent sidebands of the 1-kHz switching frequency. Figure 3-15 shows the generator-side voltages and currents. The PWM wave forms are line-to-line voltages and the sinusoids are phase currents. Figure 3-16 shows the harmonic spectrum of the generator-side line-to-line voltage v_{ab} , Figure 3-17 shows the regulated capacitor voltages, and Figure 3-18 shows the switch cell states during converter operation. We can see that the converter does indeed produce the required terminal wave forms at this operating point, while maintaining control of the nine DC capacitor voltages. Note that we chose the low switching frequency of 1 kHz for this simulation so that the details of the switching could be easily seen; the actual choice of operating point is an engineering design choice that would normally be based on the switching speeds of available semiconductor devices.
- **Simulated operating point 2:** Utility side: 240 V, 60 Hz, 11 A, unity power factor. Generator side: 240 V, 25 Hz, unity power factor. Switching frequency: 20 kHz. This simulation illustrates the effect of increasing the switching frequency; the converter otherwise operates under the same conditions as in operating point 1. Figure 3-19 shows simulator-generated wave forms for the three-phase AC utility wave forms at this operating point. Figure 3-20 shows the harmonic spectrum of the utility-side line-to-line voltage v_{AB} . Because of the increased switching frequency, the harmonics of Figure 3-14 are not present here; rather, they are shifted to 20 kHz and its sidebands, and are easier to filter using smaller

size magnetics. Figure 3-21 shows the generator-side voltages and currents, and Figure 3-22 shows the harmonic spectrum of generator-side line-to-line voltage v_{ab} . The regulated capacitor voltages for this modulation approach are plotted in Figure 3-23, and the switch states are given in Figure 3-24.

- **Simulated operating point 3:** Utility side: 240 V, 60 Hz, 11 A, unity power factor. Generator side 60 V, 6.25 Hz, unity power factor. Switching frequency: 1 kHz. This simulation illustrates converter operation at reduced generator voltage. Figure 3-25 shows simulator-generated wave forms for three-phase AC utility voltages at this operating point, and Figure 3-26 shows the harmonic spectrum of utility-side line-to-line voltage v_{AB} . As with simulated operating point 1, the low 1-kHz switching frequency leads to substantial harmonics in the vicinity of the 18th harmonic; these could again be eliminated by increasing the switching frequency. Figure 3-27 shows the generator-side voltages and currents, and Figure 3-28 shows the harmonic spectrum of generator-side line-to-line voltage v_{ab} . The capacitor voltages and switch states are plotted in Figures 3-29 and 3-30, respectively.
- **Simulated operating point 4:** Utility side: 240 V, 60 Hz, 11 A, 0.5 power factor. Generator side: 240 V, 25 Hz, unity power factor. Switching frequency: 1 kHz. This simulation illustrates operating the converter while supplying reactive power to the utility. Figure 3-31 shows simulator-generated wave forms for three-phase AC utility voltages at this operating point. We can see that the simulation algorithm sometimes selects unusual switching combinations (only when necessary) to return the capacitor voltages back to within $\pm 5\%$ of the desired regulated value. Similar voltages appear also in the generator-side wave forms. Such behavior can be avoided by using the control scheme described in the next section. Figure 3-32 shows the resulting harmonic spectrum of utility-side line-to-line voltage v_{AB} . The generator-side voltages and currents are illustrated in Figure 3-33, with the voltage spectrum given in Figure 3-34. The capacitor voltages and switch states are plotted in Figures 3-35 and 3-36, respectively.
- **Simulated operating point 5:** Utility side: 240 V, 60 Hz, 11 A, 0.5 power factor. Generator side 60 V, 6.25 Hz, 0.5 power factor. Switching frequency: 1 kHz. This final simulation illustrates operation with nonunity power factor at both the utility and generator sides of the converter, and with reduced generator voltage. Figure 3-37 shows simulator-generated wave forms for the three-phase AC utility voltages at this operating point, and Figure 3-38 shows the harmonic spectrum of the utility-side line-to-line voltage v_{AB} . The generator-side voltages and currents are illustrated in Figure 3-39, and the generator line-line voltage spectrum is given in Figure 3-40. Regulation of the capacitor voltages and control of the switch states are illustrated in Figures 3-41 and 3-42, respectively.

In summary, we developed a computer simulation program specifically for the proposed new matrix converter. The simulator is useful for analyzing the operation of the converter at different operating points. It derives all possible device combinations and stores them into arrays. Then, it operates the converter with a given set of three-phase input and output voltages, currents, frequencies, and power factors. Within the simulation program, control of the new converter is achieved through SVM, in which three-phase AC voltages are transformed to the $d-q$ reference frame and compared with a set of space vectors before modulation. Using the derived device-switching combinations, the simulation program synthesizes the three-phase input and output voltage wave forms and also regulates the capacitor DC voltages in a band within $\pm 5\%$ to $\pm 12\%$ of the desired DC capacitor voltage. The extensive simulation results show that the proposed new matrix converter can function at different operating points while maintaining constant capacitor voltages. No cases of operational deficiency were encountered. Additional simulations under other operating conditions are given in Al Naseem (2001).

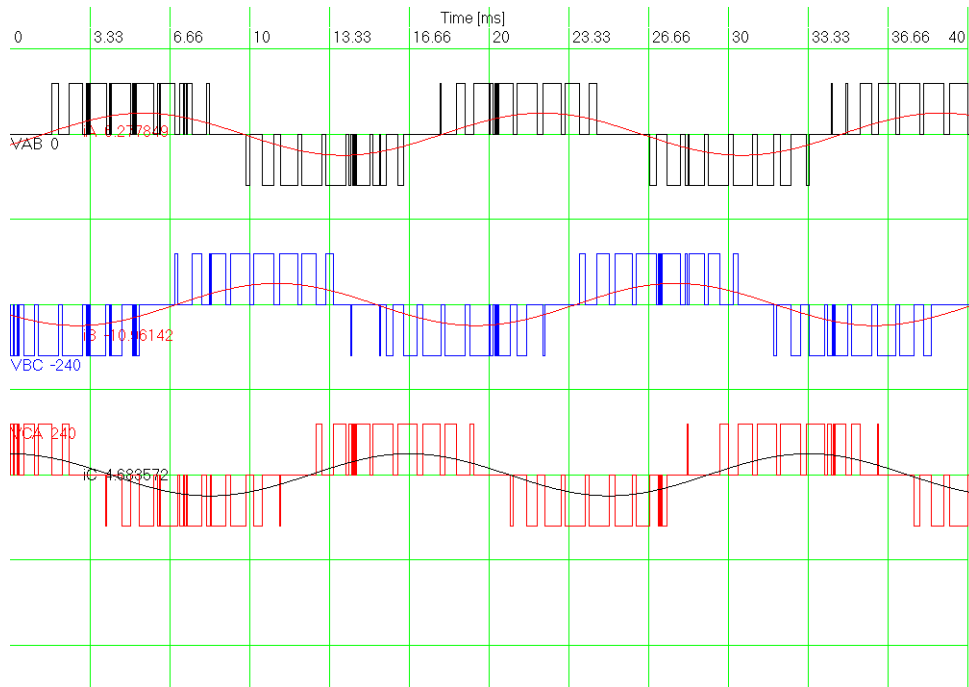


Figure 3-13. Simulated utility-side wave forms, operating point 1

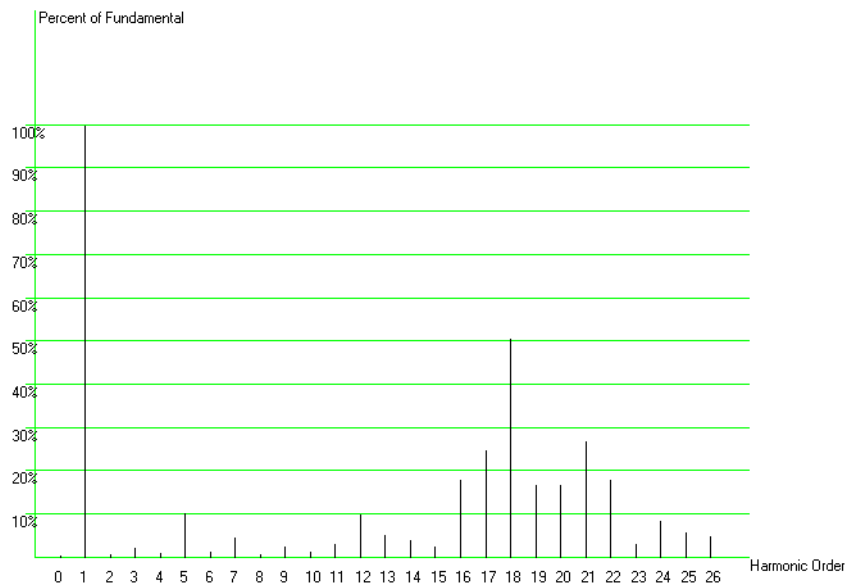


Figure 3-14. Harmonic spectrum of utility-side line-line voltage wave form, operating point 1

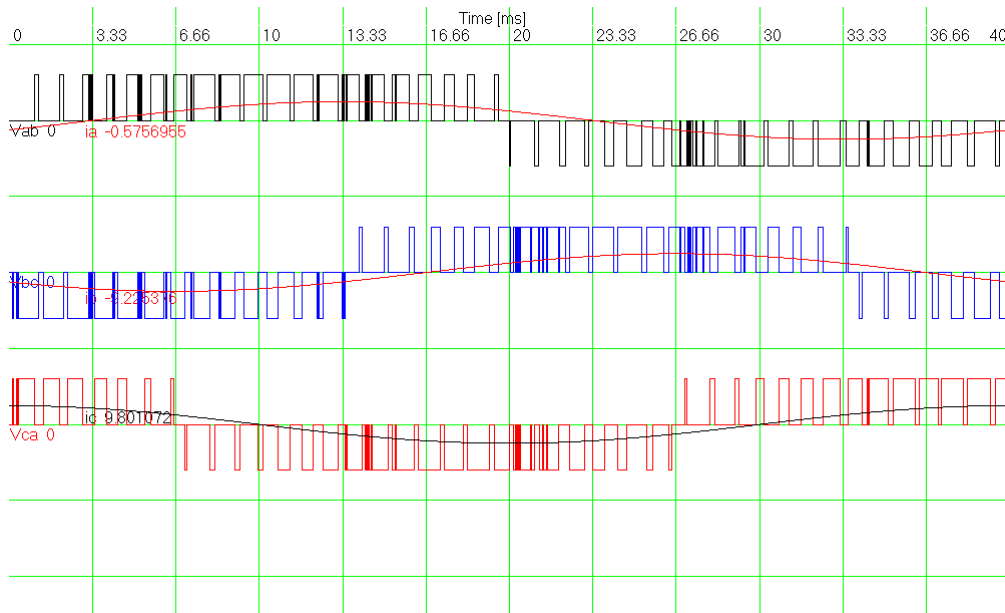


Figure 3-15. Simulated generator wave forms, operating point 1

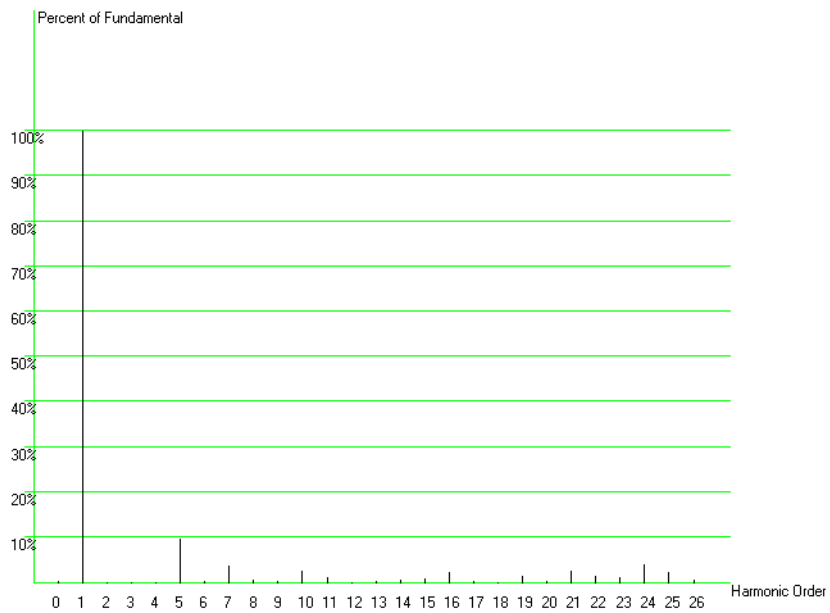


Figure 3-16. Harmonic spectrum of generator-side line-line voltage, operating point 1

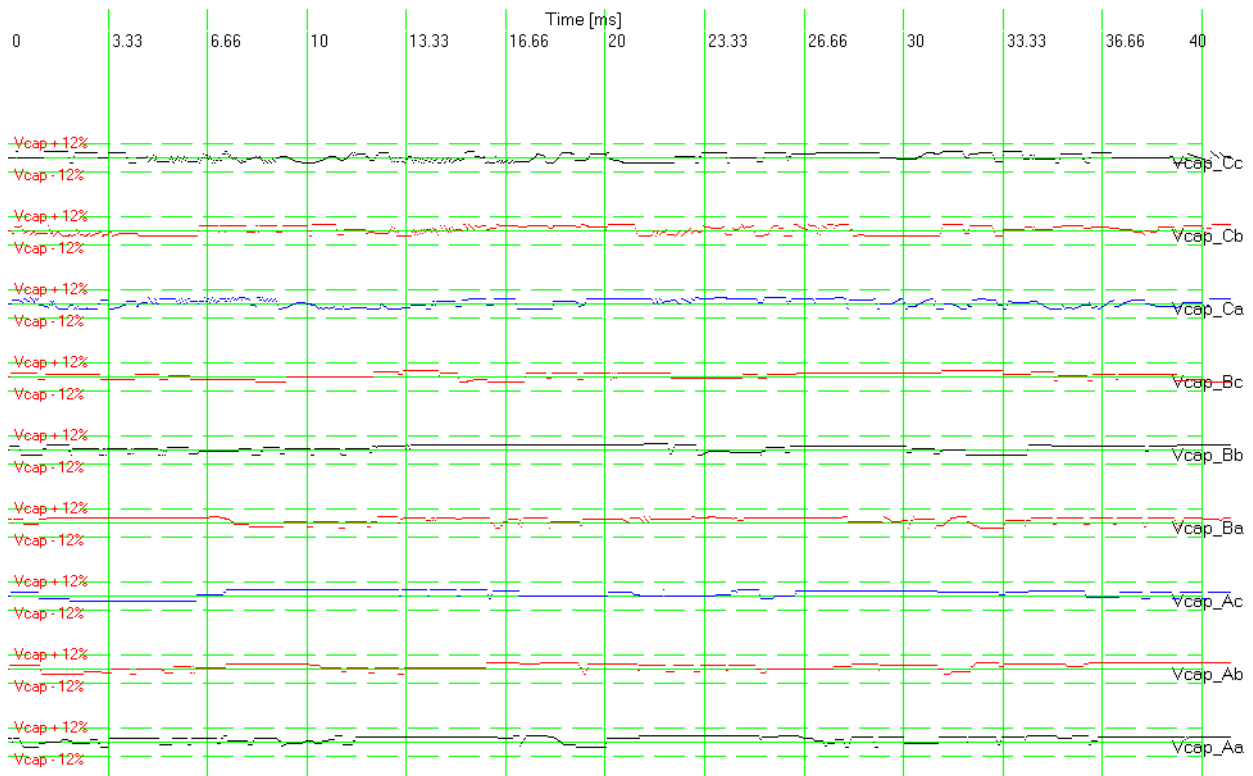


Figure 3-17. Capacitor voltages of the nine switch cells, operating point 1. The nominal voltage and the $\pm 12\%$ regulation band are labeled.

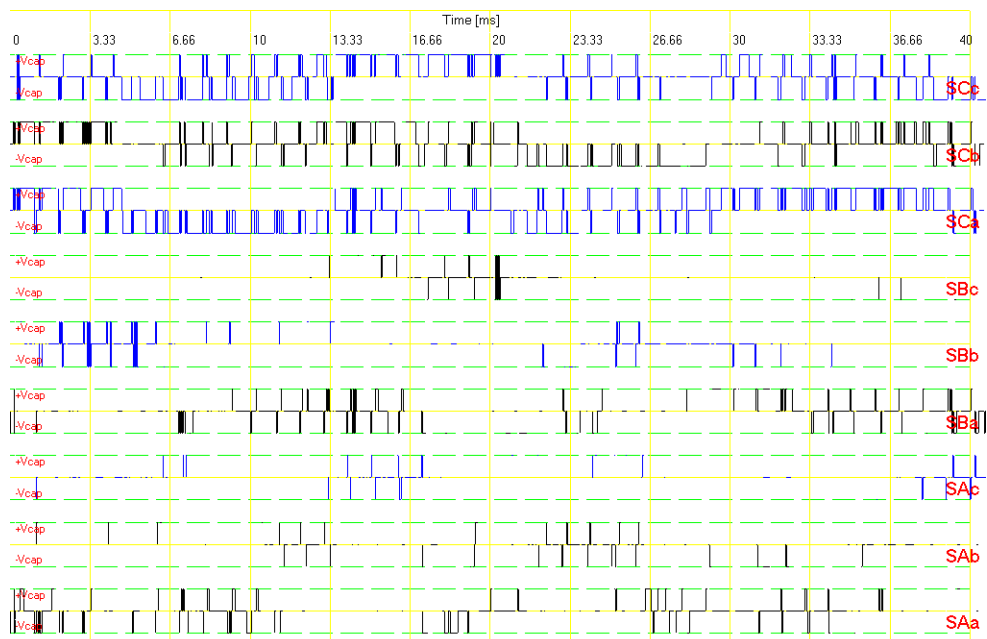


Figure 3-18. Switch states for each of the nine switch cells, operating point 1. Each switch cell may be open-circuited (no line), short-circuited (line at 0 V), or may connect the capacitor to the AC output terminals of the cell (line at $+V_{cap}$ or $-V_{cap}$).

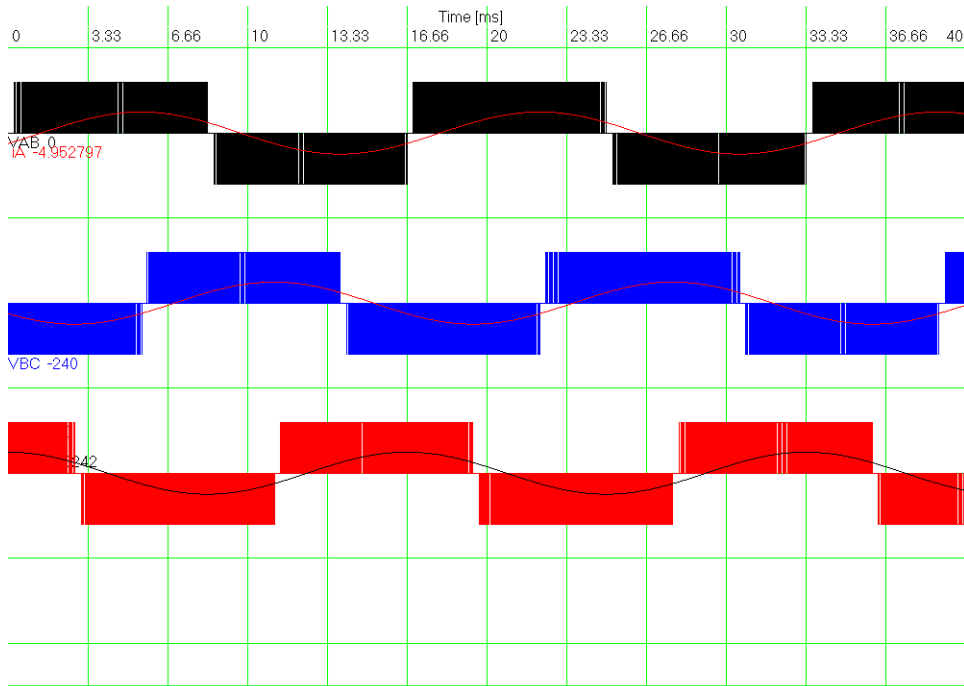


Figure 3-19. Simulated utility-side wave forms, operating point 2. The phase currents and PWM line-line voltages are shown.

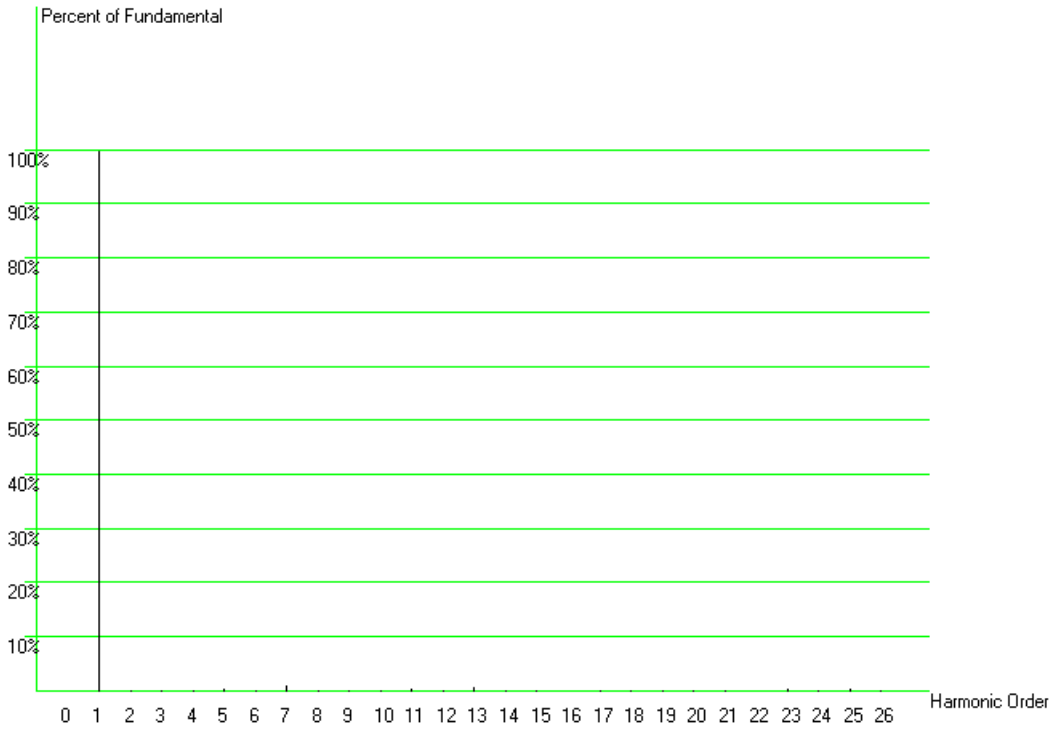


Figure 3-20. Harmonic spectrum of utility-side line-line voltage wave forms, operating point 2

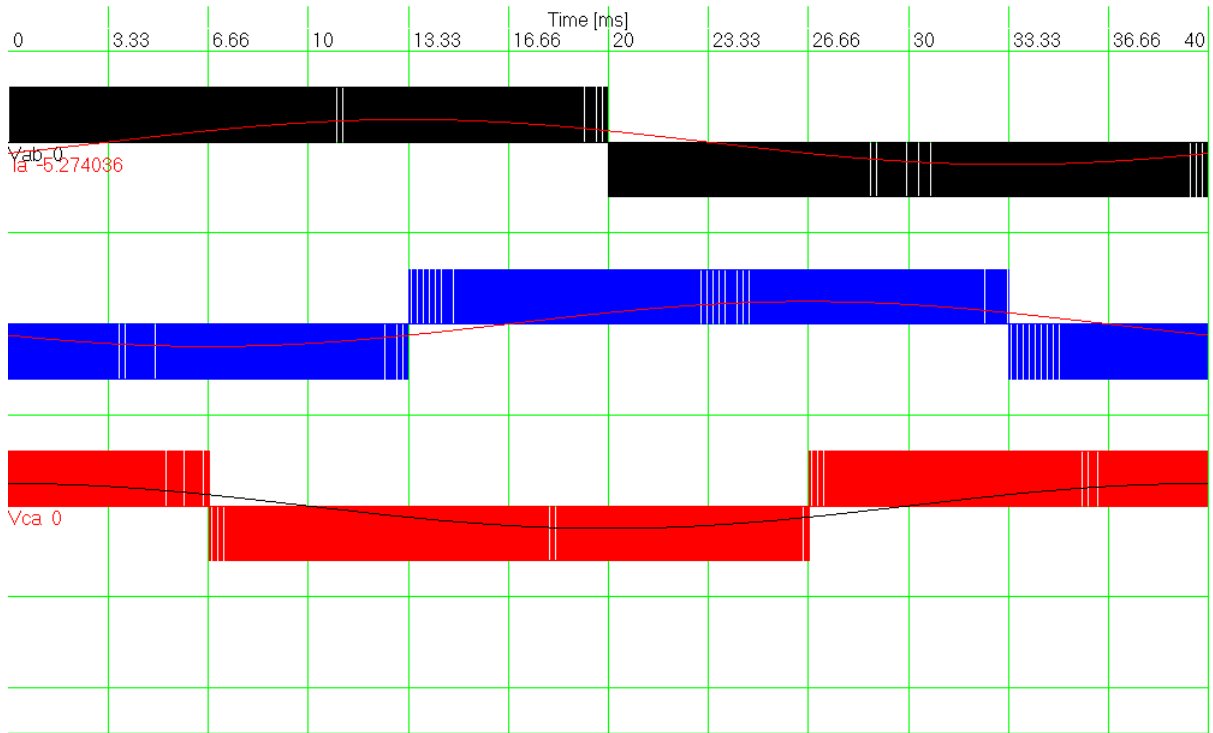


Figure 3-21. Generator-side phase currents and line-line voltages, operating point 2

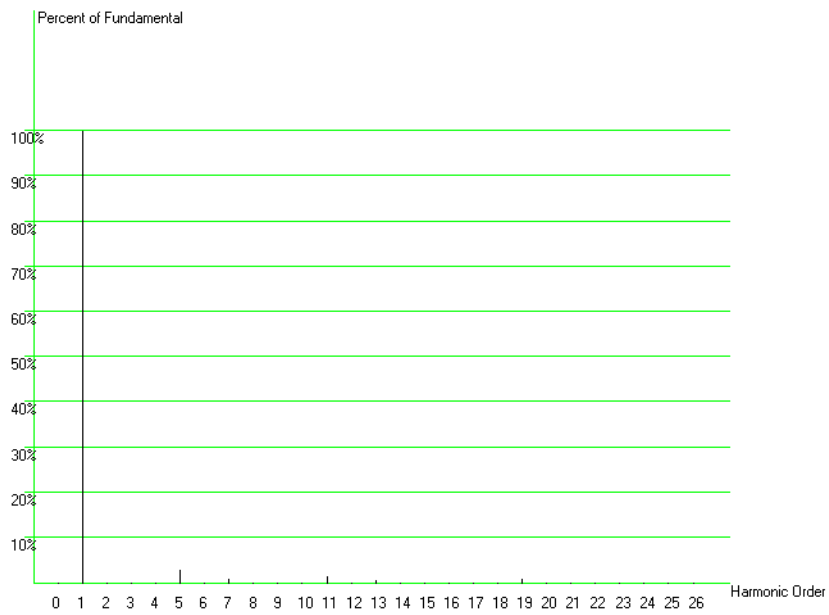


Figure 3-22. Harmonic spectrum of generator-side line-line voltage v_{ab} , operating point 2.

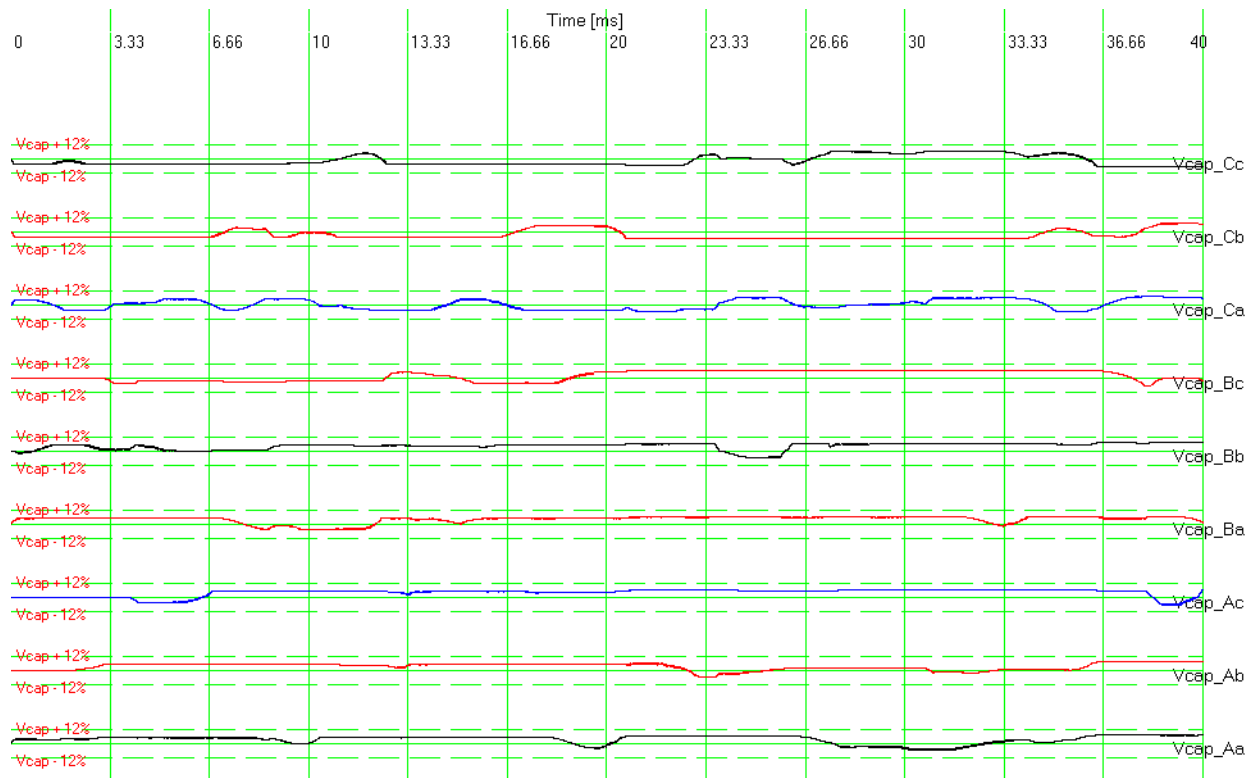


Figure 3-23. Capacitor voltages of the nine switch cells, operating point 2. The nominal voltage and the $\pm 12\%$ regulation band are labeled.

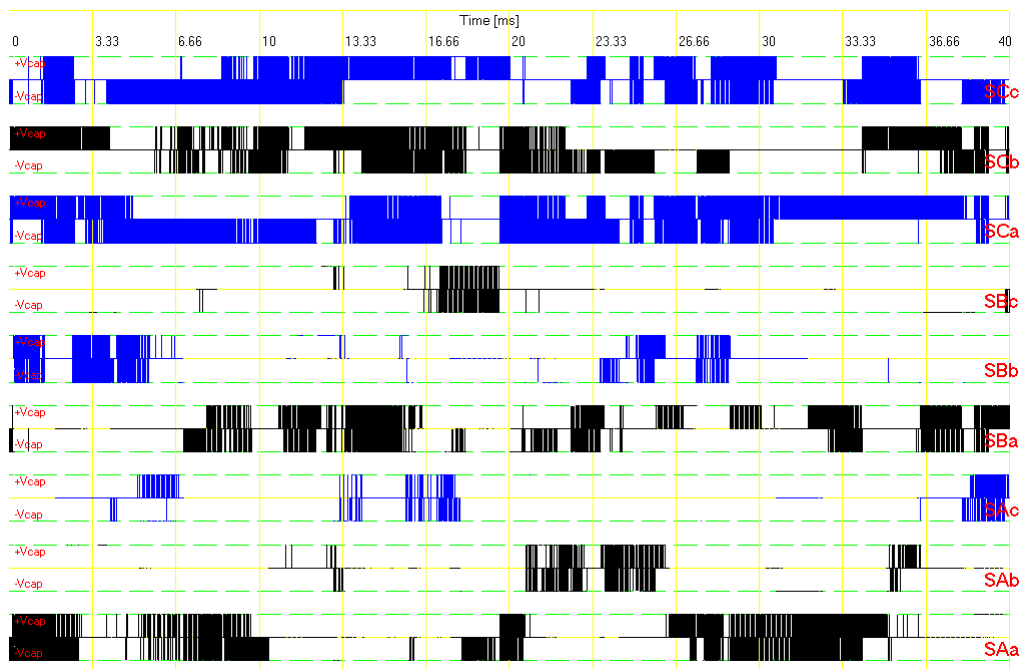


Figure 3-24. Switch states for each of the nine switch cells, operating point 2

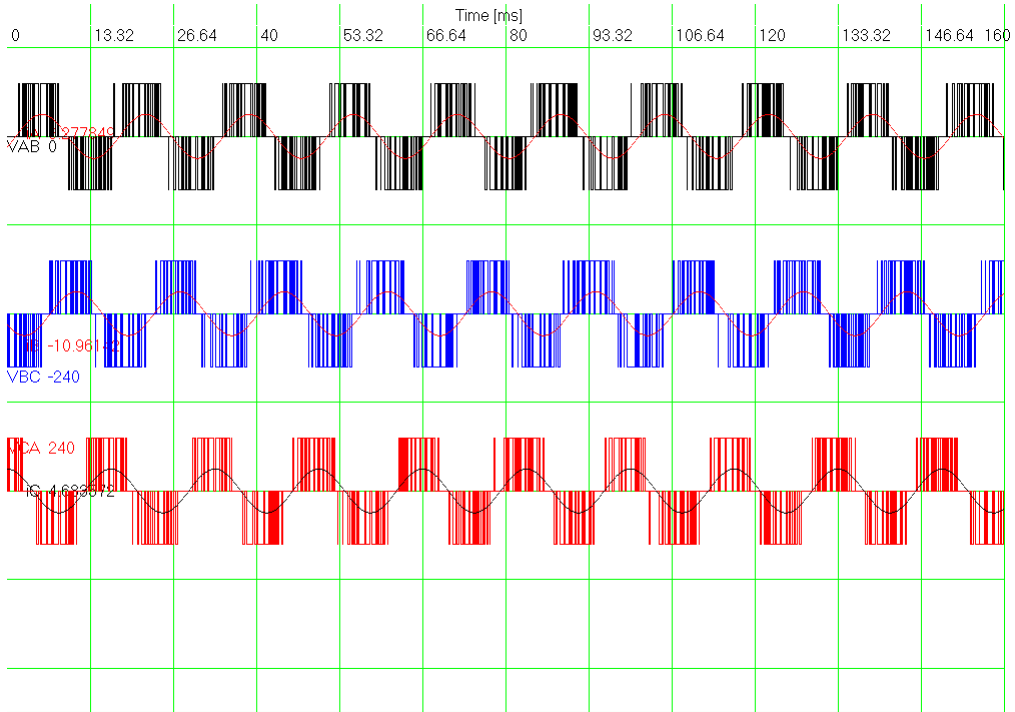


Figure 3-25. Simulated utility-side wave forms, operating point 3

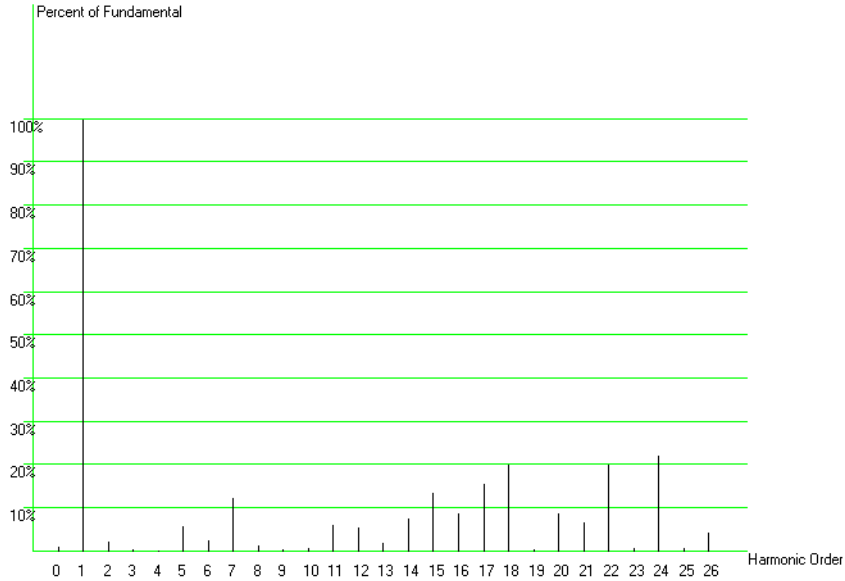


Figure 3-26. Harmonic spectrum of utility-side line-line voltage wave form, operating point 3

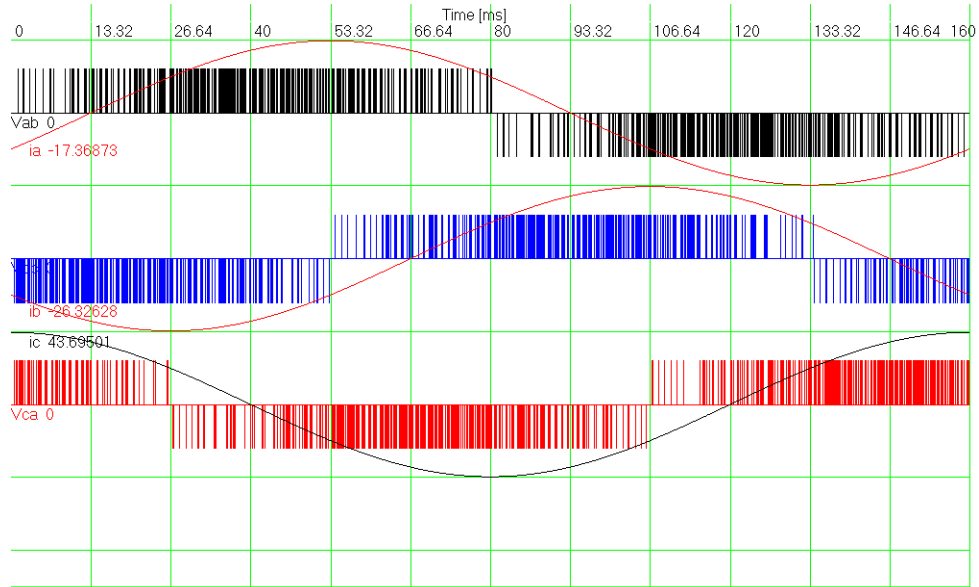


Figure 3-27. Simulated generator wave forms, operating point 3

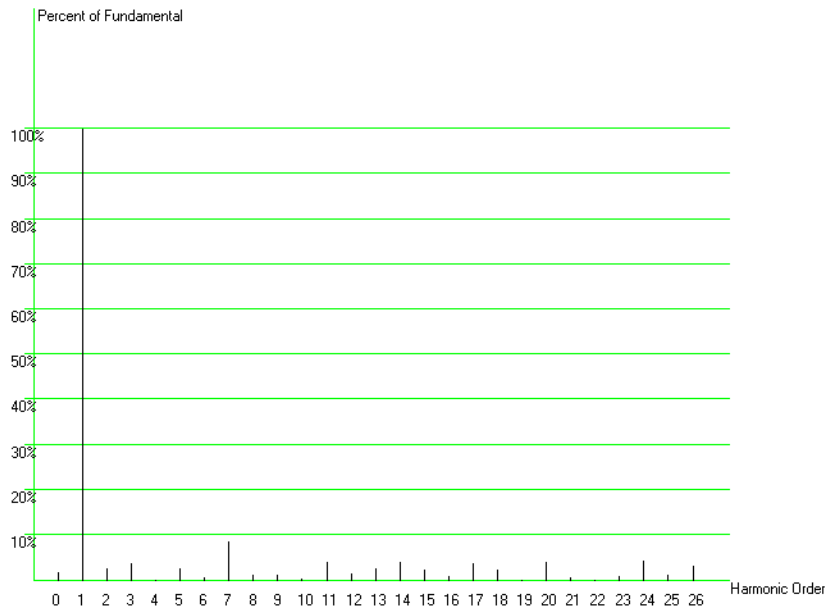


Figure 3-28. Harmonic spectrum of generator-side line-line voltage, operating point 3

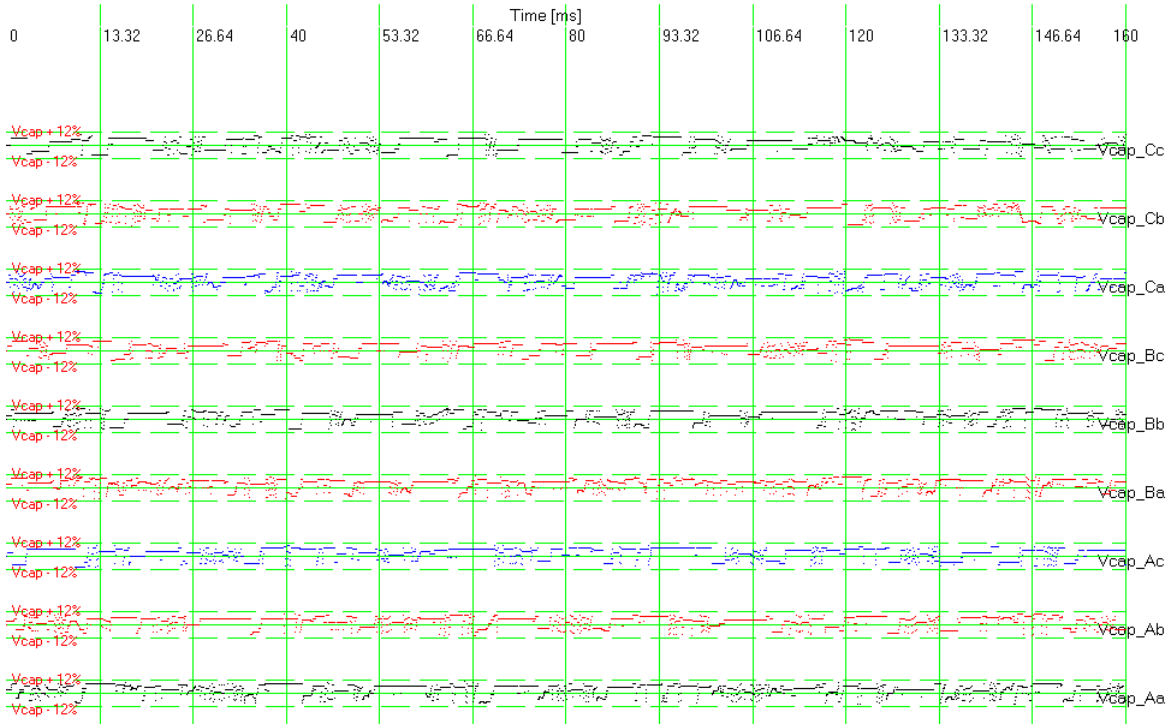


Figure 3-29. Regulation of capacitor voltages, operating point 3

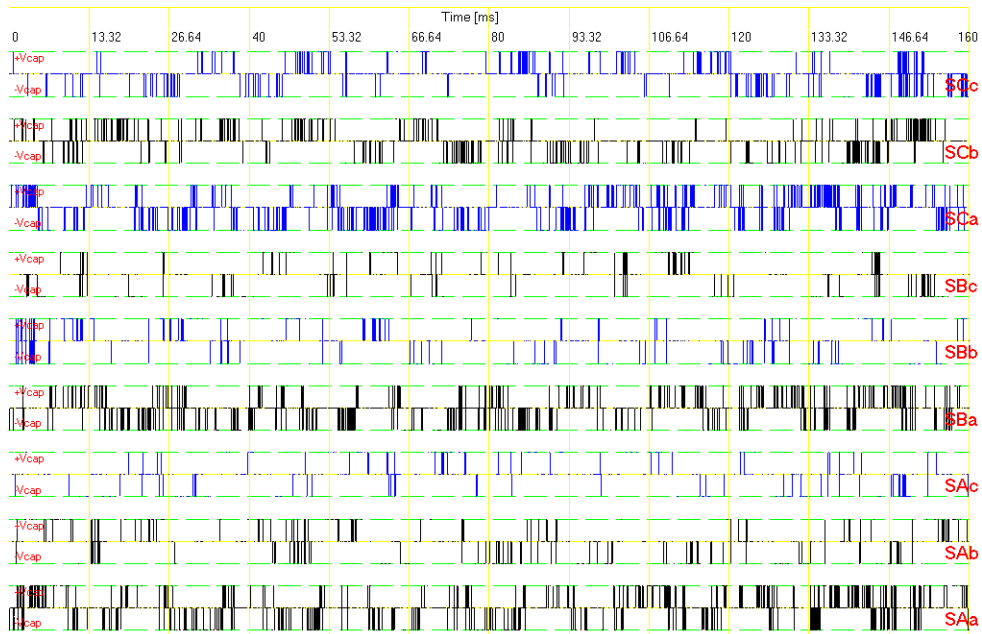


Figure 3-30. Switch states for the nine switch cells, operating point 3

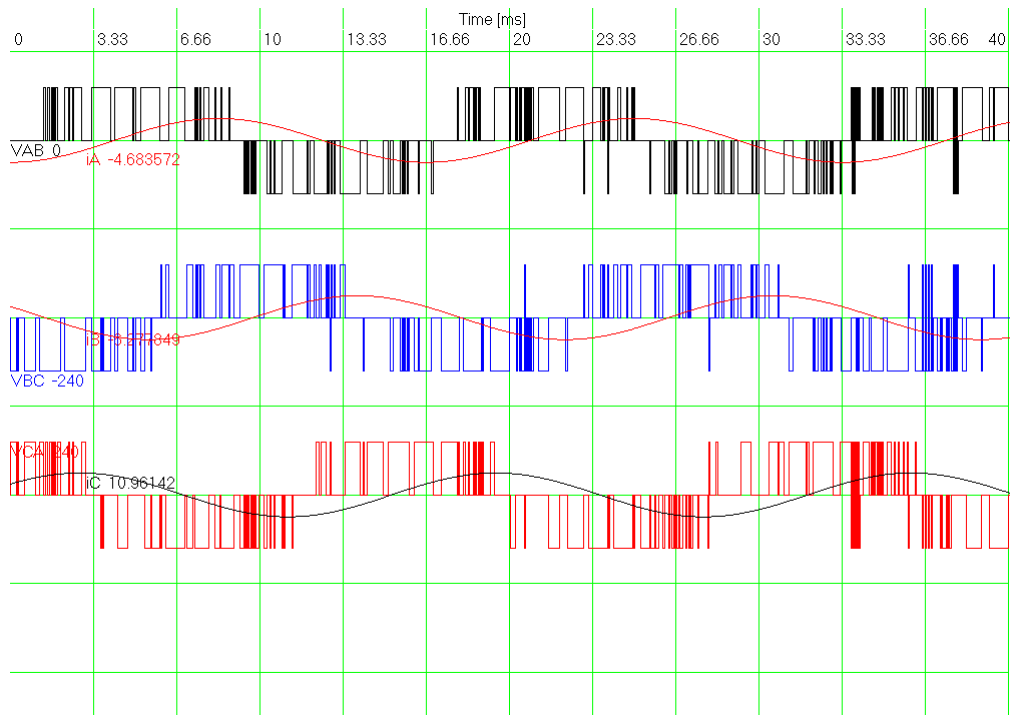


Figure 3-31. Simulated utility-side wave forms, operating point 4

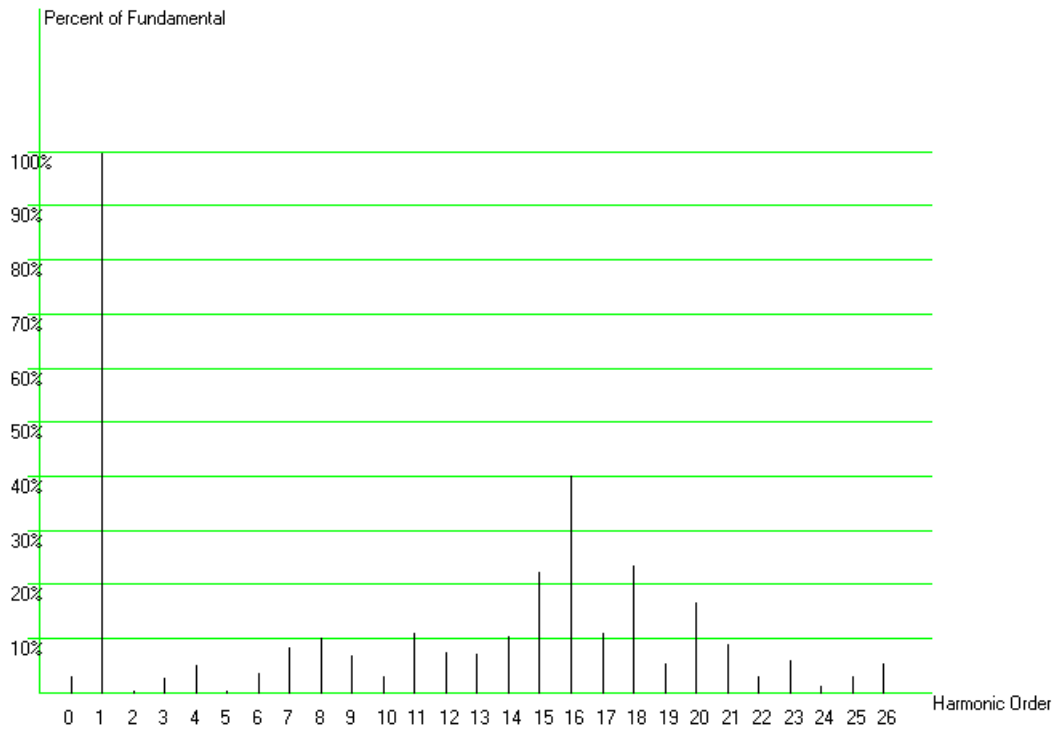


Figure 3-32. Harmonic spectrum of utility-side line-line voltage, operating point 4

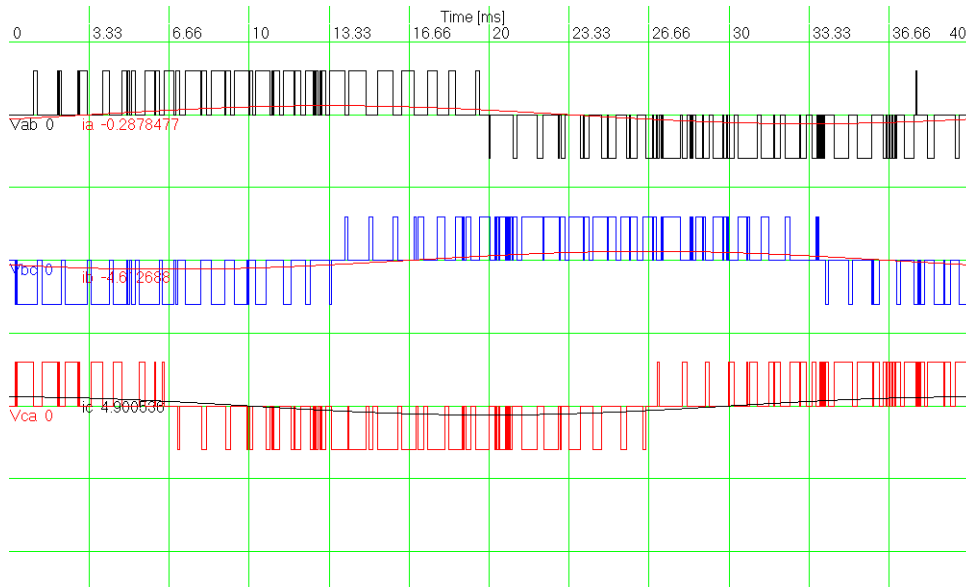


Figure 3-33. Generator-side currents and line-line voltages, operating point 4

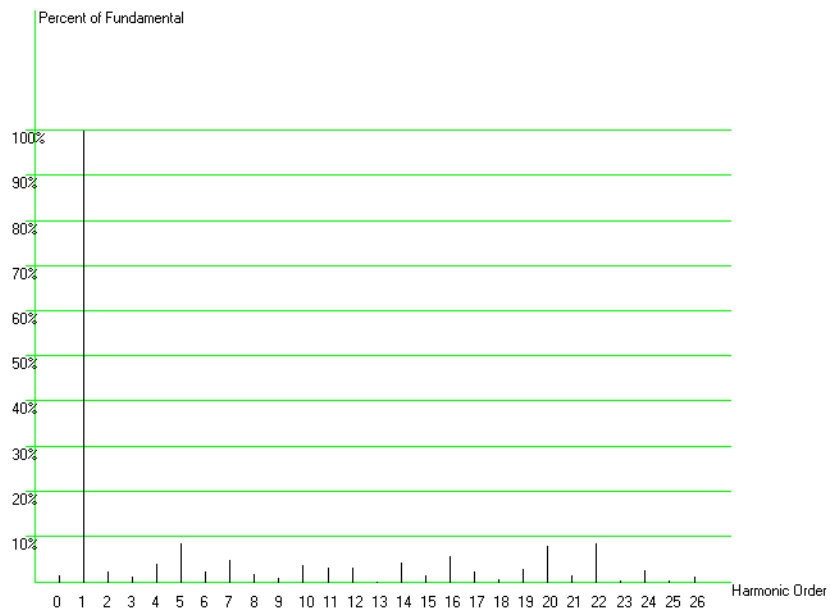


Figure 3-34. Harmonic spectrum of generator-side line-line voltage, operating point 4

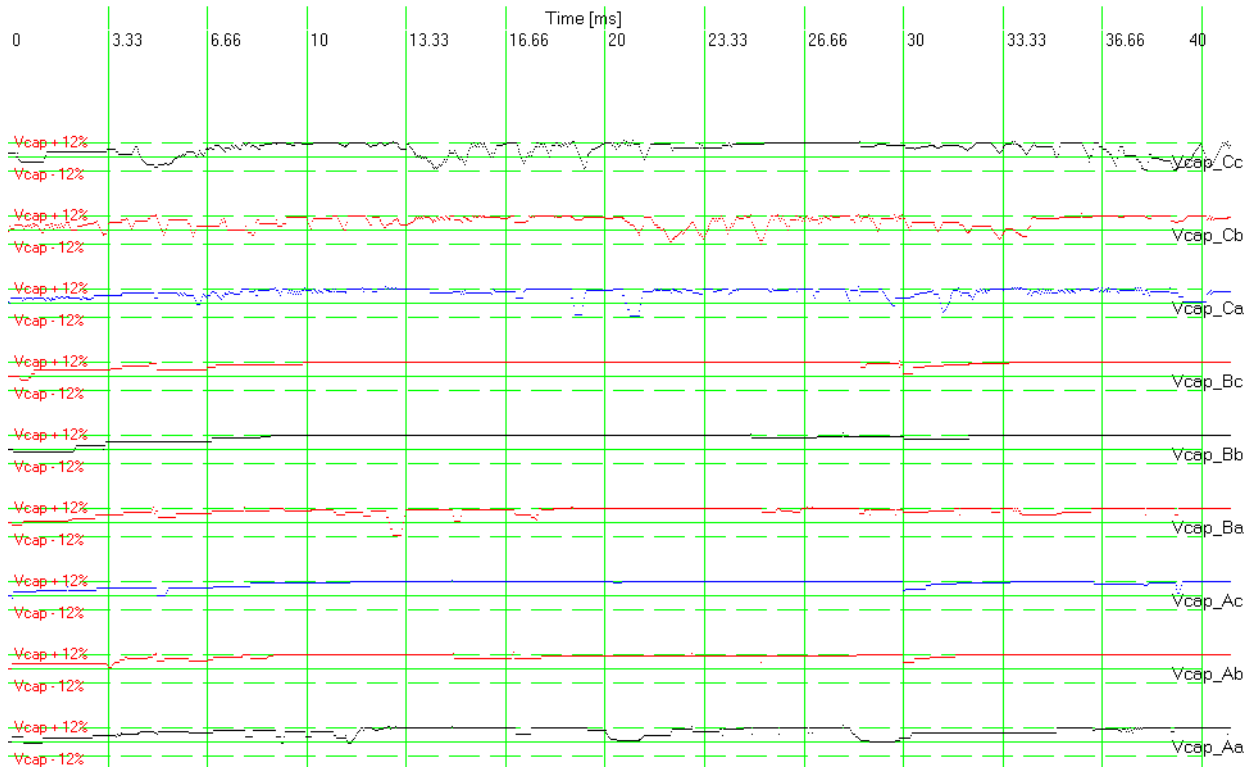


Figure 3-35. Regulation of capacitor voltages, operating point 4

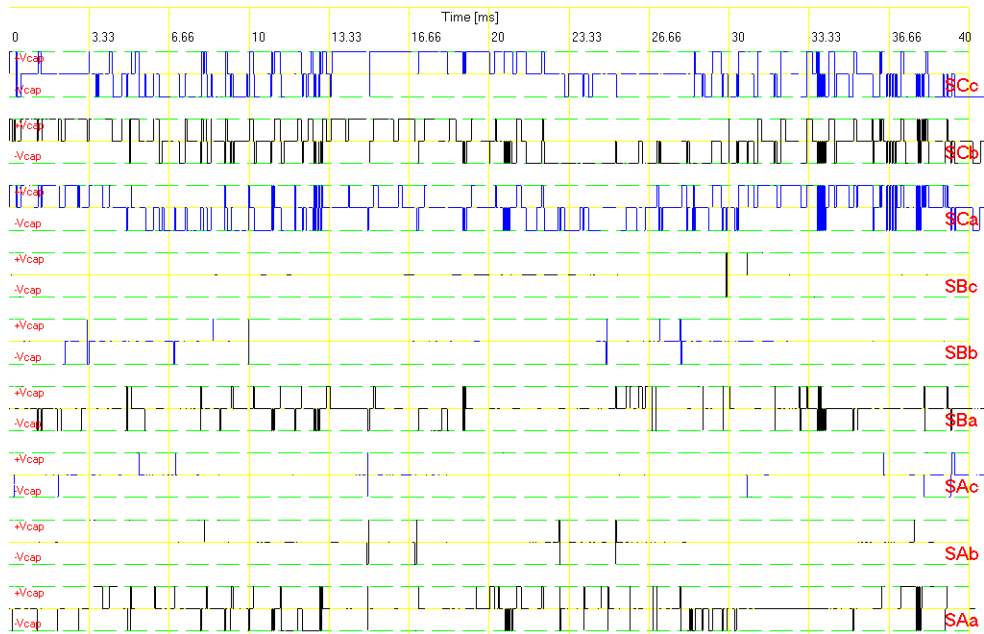


Figure 3-36. Switch states of the nine switch cells, operating point 4

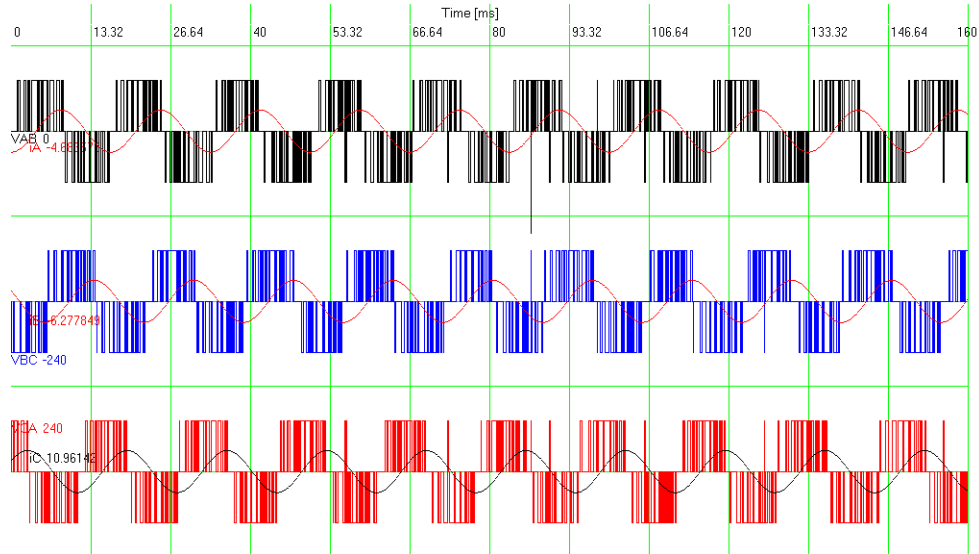


Figure 3-37. Simulated utility-side wave forms, operating point 5

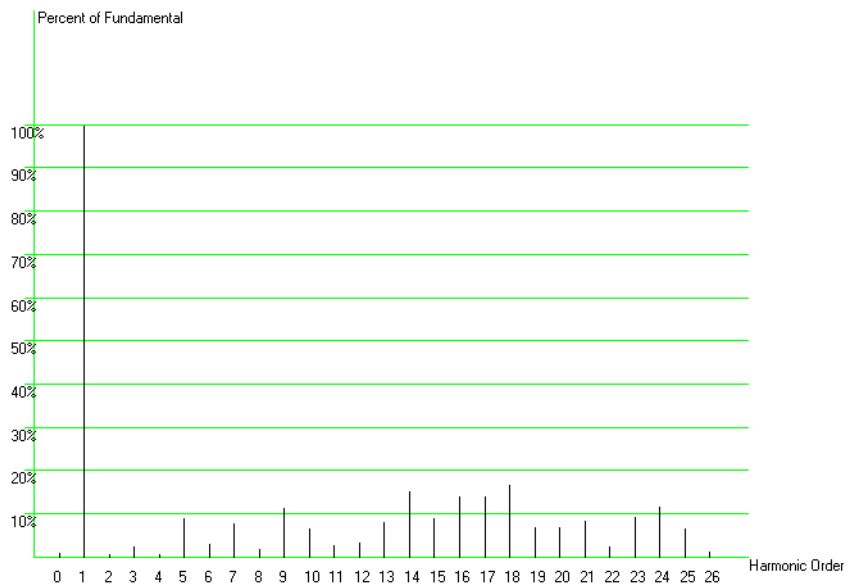


Figure 3-38. Harmonic spectrum of utility-side line-line voltage, operating point 5

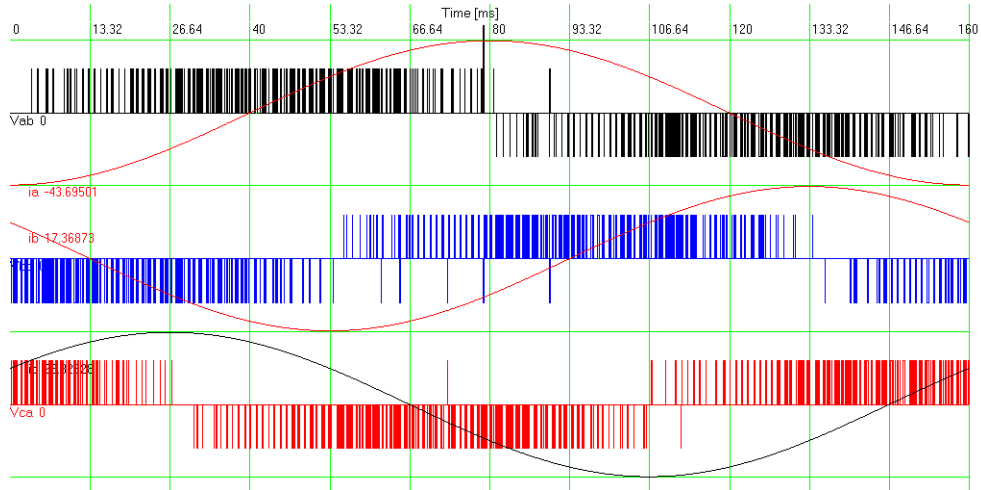


Figure 3-39. Generator-side wave forms, operating point 5

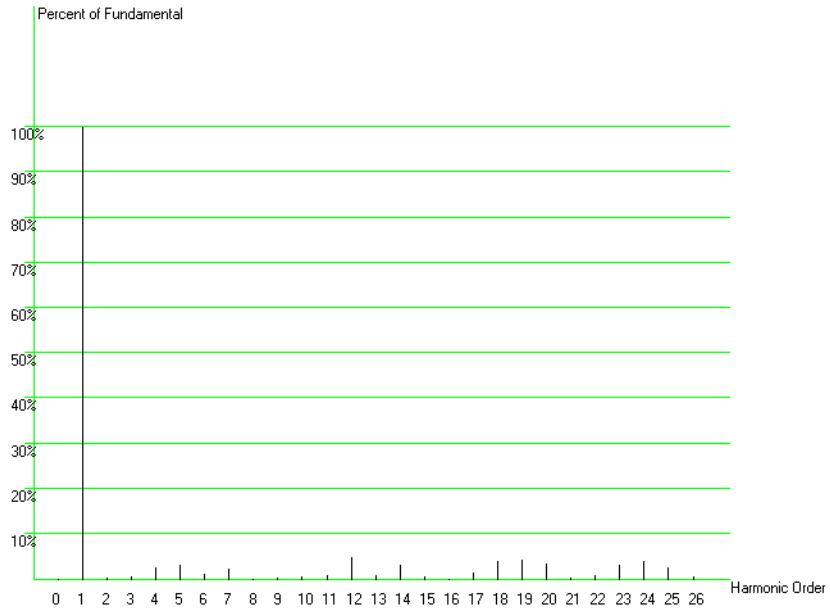


Figure 3-40. Spectrum of generator-side line-line voltage, operating point 5

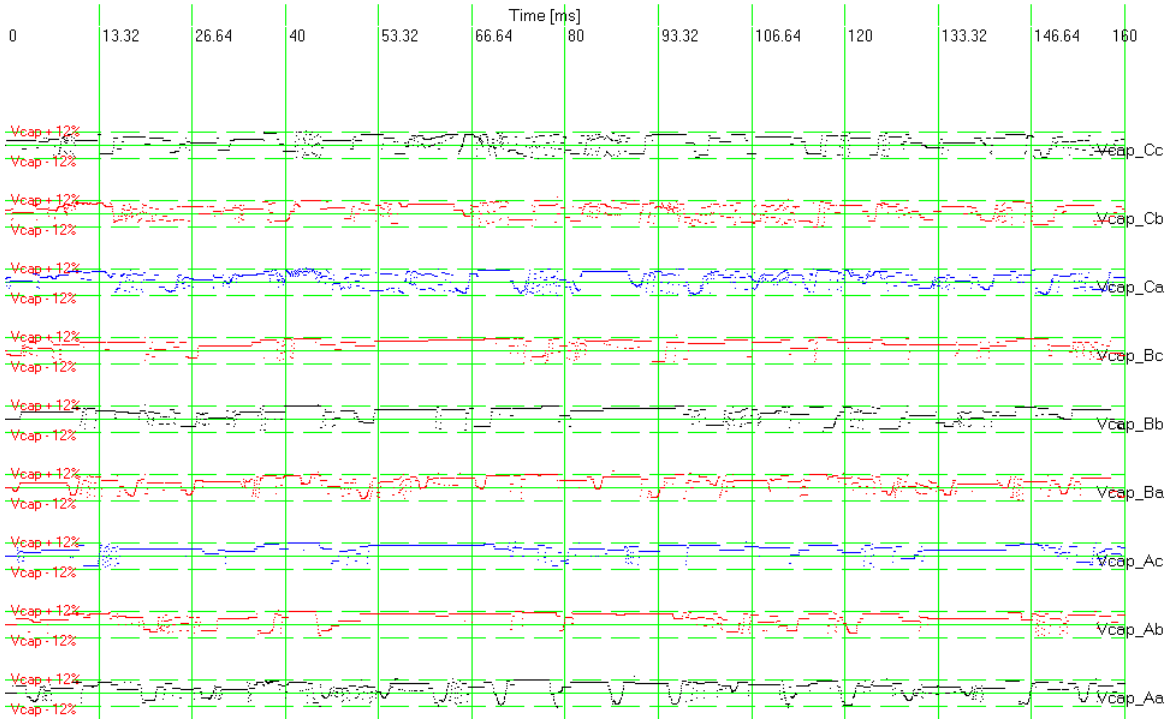


Figure 3-41. Capacitor voltages of the nine switch cells, operating point 5

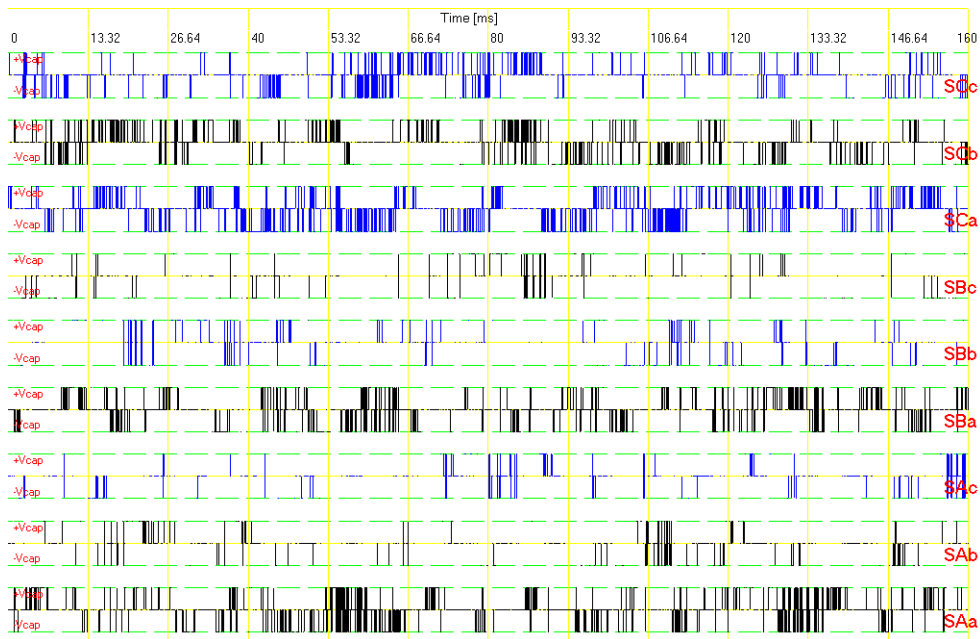


Figure 3-42. Switch states for each of the nine switch cells, operating point 5

3.4 A BASIC CONTROL STRATEGY

The simulator's brute-force control approach described in the previous section is successful in demonstrating the feasibility of the proposed new converter, as well as in showing that it is indeed possible to employ capacitors (rather than sources of DC power) in the DC buses of multilevel converters that incorporate H-bridges. However, this approach is not practical for real-time control of the proposed converter, because the search routines require unacceptably long times to complete. Further, such an approach does not yield the insight necessary to model and design the converter.

The proposed converter can be controlled through a variety of algorithms, and we describe one practical strategy in this section. This algorithm is relatively simple and is easy to model and implement. It allows the capacitor voltages to be modeled and also allows relatively high efficiency of power transfer through the module. With this algorithm, each switching period involves transfer of energy from the input to the output terminals, either directly or through a single capacitor. By avoiding the use of multiple capacitors during a switching period, the circulation of currents between multiple capacitors is minimized. In addition, the possibility of capacitor voltage imbalances is minimized.

We have found that it is possible to apply the SVM algorithm of Equations 3-10 through 3-12 in the proposed matrix converter, while charging and discharging only one capacitor during each switching period, whenever the following requirement is met:

$$\sqrt{3} \geq \frac{\text{Generator voltage}}{\text{Utility voltage}} \geq \frac{1}{\sqrt{3}} \quad (3-13)$$

Note that because the converter is symmetrical, it can both step up and step down the voltage, and can work with the source and load interchanged. This symmetry is reflected in Equation 3-13.

3.4.1 An Example

The control strategy is explained here with reference to the example illustrated in Figure 3-43. This example is (arbitrarily) taken to be at an instant in time when the input- and output-side reference space vectors lie at the positions illustrated. When the input reference voltage space-vector lies between space-vectors 3 and 4 as illustrated, the SVM technique involves modulation between input-side space vectors V_3 , V_4 , and V_0 , according to Equations 3-10 through 3-12 with duty cycles d_3 , d_4 , and d_0 , respectively. Likewise, the SVM technique for the output side involves modulation between output-side space vectors V_1 , V_6 , and V_0 , according to Equations 3-10 through 3-12, with duty cycles d_1 , d_6 , and d_{0-out} , respectively. This SVM strategy requires that the switching period be divided into five subintervals as shown in Figure 3-44. Each of these subintervals is defined by a choice of input- and output-side space vectors.

We next search the Appendix of the previously mentioned Year 2 Report to find switch combinations that lead to the required input- and output-side space vectors for each subinterval. Selecting switch combinations that involve only one capacitor is desirable. In Figure 3-45, the possible single-capacitor choices are listed. We can see that capacitor C_{Aa} (the capacitor of the switch cell connected between input

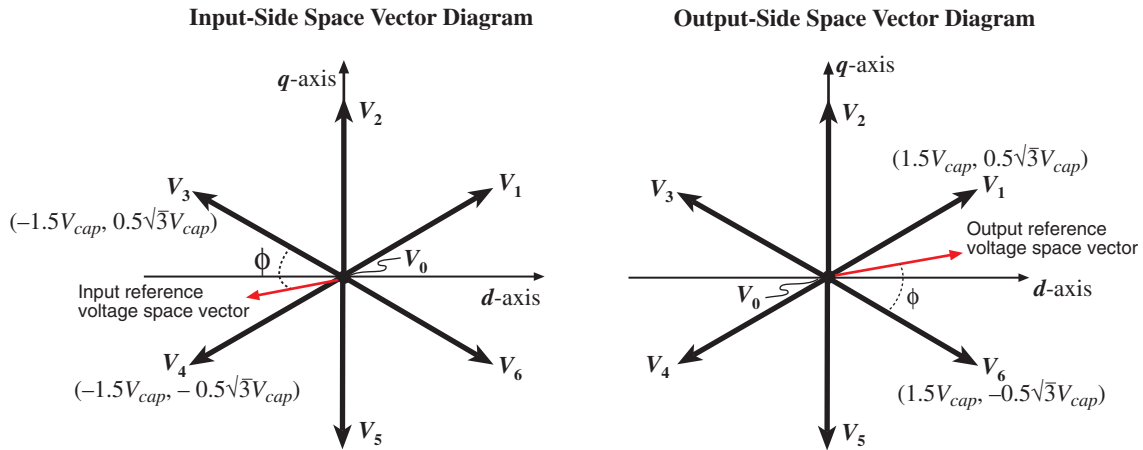


Figure 3-43. Control example, at an instant in time when the input- and output-side reference space vectors lie as shown

phase *A* and output phase *a*) can be employed for every subinterval. Hence, for this switching period, we can select switching combinations that use only C_{Aa} , to obtain a simple and efficient transfer of energy while maintaining capacitor charge balance. Note that this result is dependent not only on the input and output space vectors, but also on the relative order of the intervals.

The resulting circuit configurations for each of the five subintervals are illustrated in Figure 3-46(a). The switch network connected between input phase *A* and output phase *a*, consisting of a H-bridge and a DC capacitor, is controlled to short-circuit its AC output terminals during the first subinterval, and to present its DC capacitor voltage V_{cap} to its output terminals during the remaining four subintervals. The other eight switch networks are either short-circuited or open-circuited during each of the subintervals. These circuits lead to the input and output terminal voltage wave forms of Figure 3-46(b). For some of the subintervals, the required space vectors can be obtained in multiple ways. For example, during the first subinterval (in which all input and output phases are shorted together), any or all switch elements can be turned on, as long as all phases are shorted together. Similar comments apply to the circuits for the second and fourth subintervals in Figure 3-46.

Figure 3-44. The proposed modulation scheme employs five subintervals per switching period.

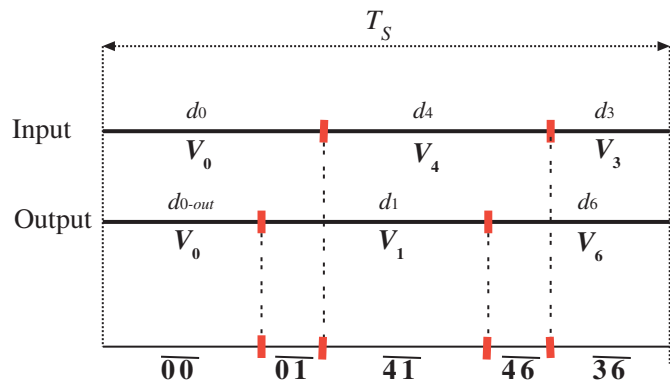


Figure 3-45. Searching for a single-capacitor modulation scheme

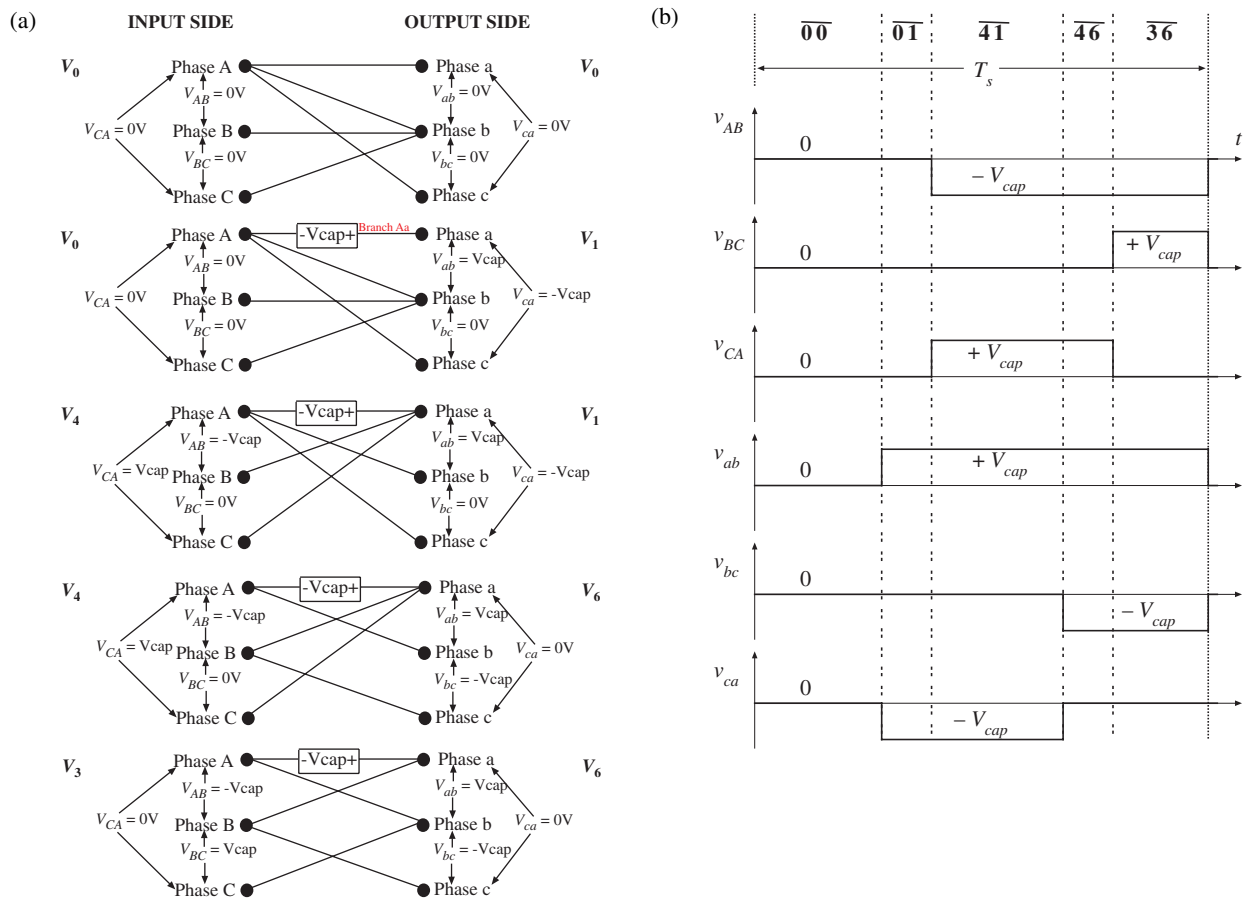
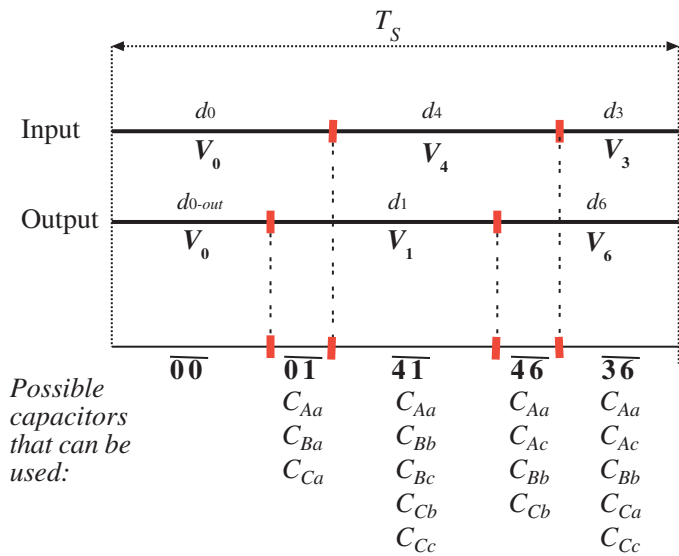


Figure 3-46. Results for the example of Figures 3-42 to 3-44: (a) Switch combinations for each of the five subintervals. The input- and output-side space vectors for each subinterval are also listed. (b) The resulting input and output voltage wave forms.

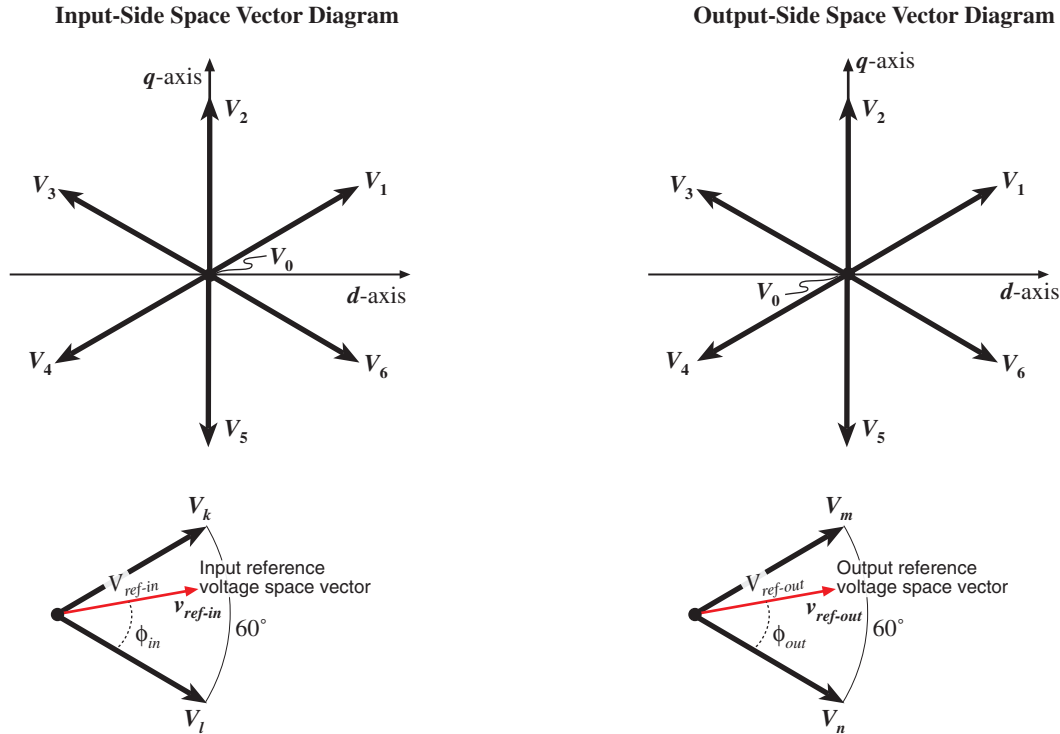


Figure 3-47. Input- and output-side SVM for the algorithm of Section 3.4.2

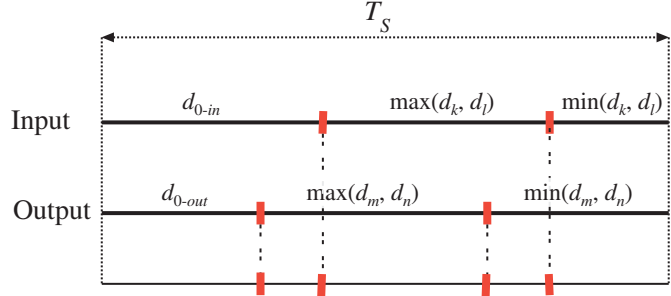
Similar results can be obtained when the input and output reference space vectors lie in other parts of the d - q plane. Provided that Equation 3-13 is satisfied, for each combination of input-side and output-side reference space vector locations, one of the DC capacitors of the nine switch networks assumes the role of capacitor C_{Aa} in the above example. As time progresses and the reference space vectors rotate, each of the nine capacitors participates (one per switching period) in the power conversion process of the converter. The switch combinations for these cases can be viewed as rotations (or interchanging) of the phases in Figure 3-46(a).

3.4.2 An Algorithm

The control strategy of the above example is formally generalized here, to control the basic form of the proposed converter using a single DC capacitor during each switching period. The algorithm is valid whenever Equation 3-13 is satisfied.

We are given reference voltage space vectors for the input and output sides, \mathbf{v}_{ref-in} and $\mathbf{v}_{ref-out}$, respectively. These vectors have magnitudes V_{ref-in} and $V_{ref-out}$, respectively. Further, the input-side reference space vector \mathbf{v}_{ref-in} lies between two of the input-side vectors that can be produced by the converter: V_k and V_l . Likewise, the output-side reference space vector $\mathbf{v}_{ref-out}$ lies between two of the output-side vectors that can be produced by the converter: V_m and V_n . Figure 3-47 illustrates the general situation. The input- and output-side duty cycles are now computed using Equations 3-9 through 3-12, as follows. For the input side, we

Figure 3-48. Ordering the subintervals, space vector control algorithm of Section 3.4.2



obtain

$$\begin{aligned}
 d_{0-in} &= 1 - M_{in} \sin(60^\circ + \phi_{in}) \\
 d_k &= M_{in} \sin(\phi_{in}) \\
 d_l &= M_{in} \sin(60^\circ - \phi_{in}) \\
 M_{in} &= \frac{2}{\sqrt{3}} \frac{V_{ref-in}}{V_{cap}}
 \end{aligned} \tag{3-14}$$

Here, M_{in} is the input-side modulation index, V_{cap} is the DC capacitor voltage of the switch cell, and the quantities V_{ref-in} and ϕ_{in} are as defined in Figure 3-46. Likewise, for the output side, we obtain

$$\begin{aligned}
 d_{0-out} &= 1 - M_{out} \sin(60^\circ + \phi_{out}) \\
 d_m &= M_{out} \sin(\phi_{out}) \\
 d_n &= M_{out} \sin(60^\circ - \phi_{out}) \\
 M_{out} &= \frac{2}{\sqrt{3}} \frac{V_{ref-out}}{V_{cap}}
 \end{aligned} \tag{3-15}$$

The subintervals are then ordered as illustrated in Figure 3-48.

We next select the capacitor that participates in the energy conversion process during this switching period, (performing the role of capacitor C_{Aa} of the previous example). First, we compare the duty cycles d_{0-in} and d_{0-out} , to determine which is smaller. From Equations 3-14 and 3-15, we can see that the side having the larger modulation index, and hence higher voltage, will usually exhibit the smaller d_0 . In a typical wind generation system, this may most often be the utility side. However, the phase angles ϕ_{in} and ϕ_{out} also play a role, and may change the conclusion under some circumstances. For the side having the smaller d_0 , we identify the converter space vector that is nearest to (i.e., within $\pm 30^\circ$ of) the reference space vector. We should also note that, when the reference space vector coincides with one of the converter space vectors V_1, V_2, \dots, V_6 , the corresponding line-to-neutral voltage $v_{an}, -v_{cn}, v_{bn}, -v_{an}, v_{cn}, -v_{bn}$, attains its peak positive value. The capacitor should be in a switch cell connected to the corresponding phase.

For example, suppose that d_{0-in} is greater than d_{0-out} . We therefore examine the output-side reference space vector $v_{ref-out}$. Suppose that $v_{ref-out}$ lies within $\pm 30^\circ$ of converter space vector V_3 , and hence the output-side line-to-neutral voltage $v_{bn}(t)$ is within $\pm 30^\circ$ of its peak positive value for the output AC line cycle. We will thus select one of the three capacitors connected to output phase b : either C_{Ab}, C_{Bb} , or C_{Cb} .

We next examine the other side of the converter—the side having the larger d_0 —to narrow the choice to a single capacitor. We select the phase having polarity opposite the selected phase of the first side, and having the largest magnitude. For the above example, the selected output phase b has positive polarity, so

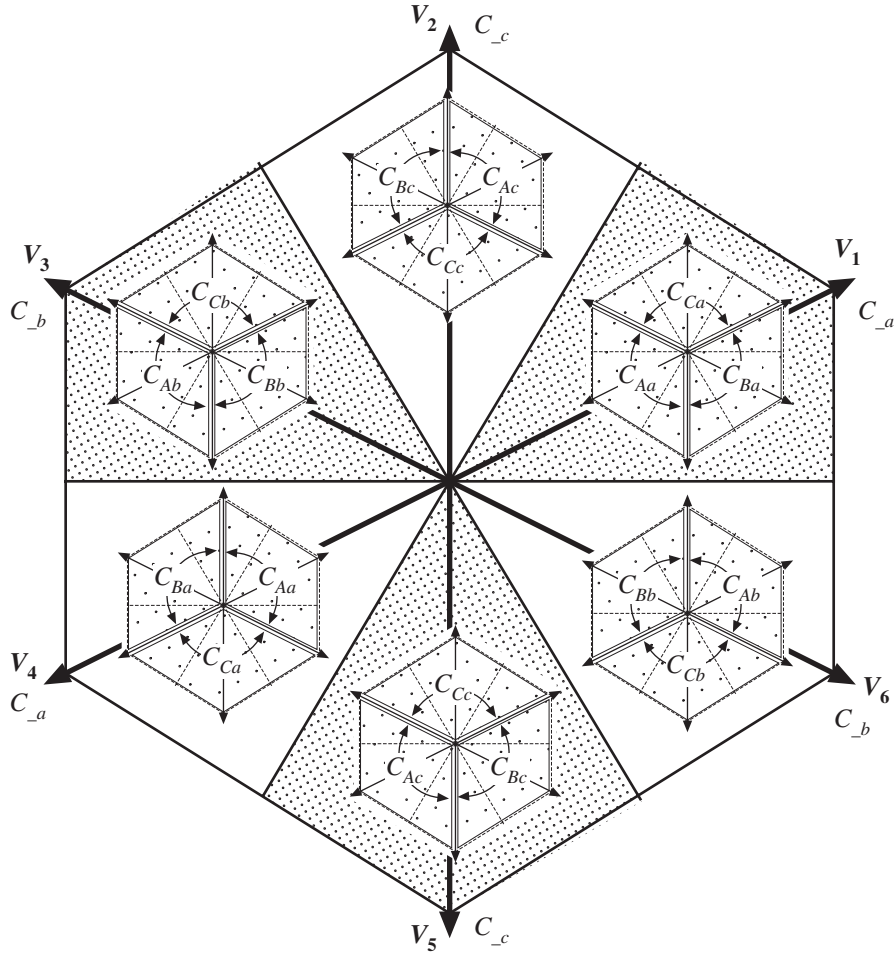


Figure 3-49. Summary of capacitor choice for the algorithm of Section 3.4.2. The case when $d_{0-out} < d_{0-in}$ is illustrated. The large (outer) space vector diagram represents the output side, with 60° segments. When the 60° segment is shaded, the positive side of V_{cap} is applied to the respective output terminal. The smaller superimposed space vector diagrams represent the input side, with 120° segments. The case $d_{0-out} > d_{0-in}$ is symmetrical, with the input and output sides interchanged.

we should select the input-side phase that is negative with the largest amplitude. Three of the six converter space vectors correspond to negative polarities: V_2 , V_4 , and V_6 correspond to $-v_{CN}$, $-v_{AN}$, and $-v_{BN}$, respectively. We select the converter space vector that lies closest to (i.e., within $\pm 60^\circ$ of) the reference space vector. For example, if the input-side reference space vector lies between converter space vectors V_4 and V_5 , it is closest to converter space vector V_4 (of vectors V_2 , V_4 , and V_6), and so input phase A exhibits the most negative line-to-neutral voltage. Therefore, we would select capacitor C_{Ab} .

Having chosen a capacitor for the given switching period, the SVM then proceeds with the timing illustrated in Figure 3-48. The switching combinations will be similar to those of Figure 3-46(a), but possibly with rotation of the input and output phases, and possibly with the polarity of V_{cap} reversed.

The process for selecting the capacitor is summarized in Fig 3-49. The large circle represents the space vector diagram of the converter side having the smaller d_0 . This circle is divided into six 60° regions, each

of which lie within $\pm 30^\circ$ of a converter space vector, as described above. Within each region is a smaller circle that represents the space vector diagram of the converter side that has the larger d_0 ; these smaller circles are divided into 120° regions that lie within $\pm 60^\circ$ of the appropriate converter space vectors. The capacitors for each combination of input-side and output-side regions are labeled.

During a given switching period, control can be exerted on the voltage of the capacitor that is used during that period, by controlling the converter input and output power. If the input power is less than the output power, the difference will be supplied by the energy stored in the capacitor. Consequently, if we wish to adjust the capacitor voltage, we can change the ratio of input to output power, which is accomplished by changing the reference space vectors for the input and output sides.

3.4.3 Three-Level Modulation

The SVM schemes we have discussed so far are two-level schemes, in which the input and output line-to-neutral voltages can attain one of two levels. The resulting line-to-line voltages can attain three levels. For the basic configuration of the proposed new matrix converter, only two-level modulation can be used when the input and output voltages are close in magnitude. However, three-level switching is possible in the basic configuration when the input and output voltages are sufficiently different; an example is at low wind speeds where the generator voltage is sufficiently smaller than the utility voltage. In versions of the proposed new matrix converters that contain two or more switch cells per branch, modulation with three or more levels is possible even when the input and output voltage magnitudes are the same.

In this section, three-level modulation of the basic configuration of the proposed new matrix converter is described. The SVM method is applied, using all 19 possible voltage space vectors of Figure 3-11. The basic equations are stated, and limits on the modulation index are given. These schemes require that two or more capacitors participate in the power conversion process during each switching period. So far, we have not addressed the issue of capacitor selection or capacitor voltage control for this case, so only the basic space vector control equations are given.

Three-level modulation in the basic configuration of the proposed new matrix converter is useful in a wind generation application when the generator voltage is lower than the utility voltage by a factor of $1/(\sqrt{3})$:

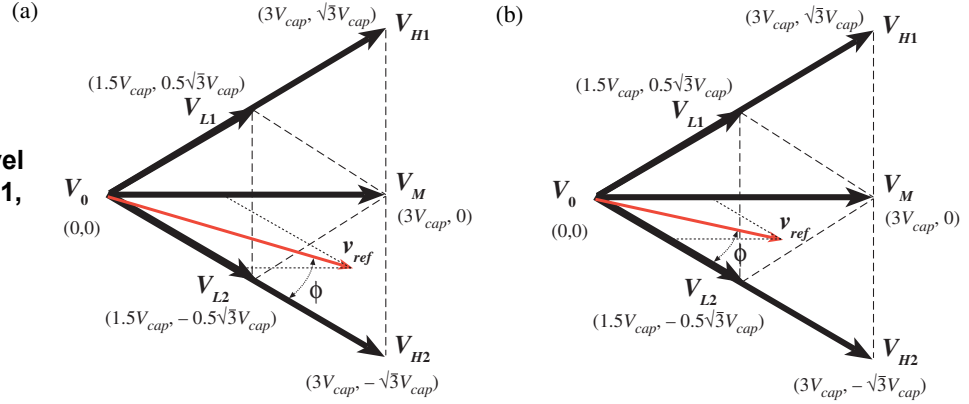
$$\frac{\text{Generator voltage}}{\text{Utility voltage}} < \frac{1}{\sqrt{3}} \quad (3-16)$$

Under this condition, we can reduce the DC capacitor voltages of the switch cells, to a value between two-thirds and one-half of the peak utility voltage, depending on the generator voltage. We could then operate the generator side with two-level modulation, and the utility side with three-level modulation. The reduced capacitor voltage leads to effectively higher modulation index on the generator side, with higher duty cycles and reduced loss.

For the side that operates with three-level modulation (e.g., the utility side), the modulation index is again defined as

$$M = \frac{2}{\sqrt{3}} \frac{V_{ref}}{V_{cap}} \quad (3-17)$$

Figure 3-50. Three-level modulation: (a) case 1, (b) case 2



where V_{ref} is again the magnitude of the reference voltage space vector, and V_{cap} is the DC capacitor voltage. For three-level operation,

$$1 < M < 2 \quad (3-18)$$

In other words, the reference voltage space vector lies between the inner and outer rings of Figure 3-11.

Two cases can occur. The first case is illustrated in Figure 3-50(a). Modulation occurs between the low-magnitude space vector V_{L2} , the intermediate-magnitude space vector V_M , and the high-magnitude space vector V_{H2} , with duty cycles d_{L2} , d_M , and d_{H2} , respectively. We can express the reference vector v_{ref} in terms of the space vectors V_{L2} , V_M , and V_{H2} :

$$\begin{aligned} v_{ref} &= d_{L2}V_{L2} + d_{H2}V_{H2} + d_MV_M \\ \text{with } d_{L2} + d_{H2} + d_M &= 1 \end{aligned} \quad (3-19)$$

Solution of the geometry of Figure 3-49(a) leads to the following expressions for the duty cycles:

$$\begin{aligned} d_M &= M \sin(\phi) \\ d_{H2} &= -1 + M \sin(60^\circ - \phi) \\ d_{L2} &= -2 - M \sin(60^\circ + \phi) \end{aligned} \quad (3-20)$$

The second case is illustrated in Figure 3-50(b). Modulation occurs between the two low-magnitude space vectors V_{L1} and V_{L2} , and the intermediate-magnitude space vector V_M . The solution for the duty cycles in this case is

$$\begin{aligned} d_M &= -1 + M \sin(60^\circ + \phi) \\ d_{L1} &= 1 - M \sin(\phi) \\ d_{L2} &= 1 - M \sin(60^\circ - \phi) \end{aligned} \quad (3-21)$$

A key limitation to the use of three-level modulation in the basic configuration of the proposed matrix converters is the fact that, whenever an intermediate- or high-magnitude space vector is employed at one side of the converter, the zero vector must be employed at the other side. This means that high average voltages cannot be generated at one side unless low voltages appear at the other side. Nonetheless, this is indeed the case when the generator voltage is low, as in low-wind conditions in a system employing a permanent-magnet synchronous generator. We now believe that it is feasible to switch to this mode of control whenever Equation 3-16 is satisfied. Therefore, the control strategies of Sections 3.4.2 and 3.4.3

should be sufficient to cover the entire range of generator voltage magnitudes, from zero to the utility voltage.

3.5 PROPOSED CONTROL SYSTEM

The overall converter control system employs space vector control to maintain the machine and utility currents at the desired magnitudes and phase angles. The capacitor voltages within the H-bridges are regulated by controlling the reference input and output reference space vectors, as we noted previously. This approach also provides a convenient framework for field-oriented control of the generator, if desired. A block diagram is given in Figure 3-51, and further details are given in Chapter 4.

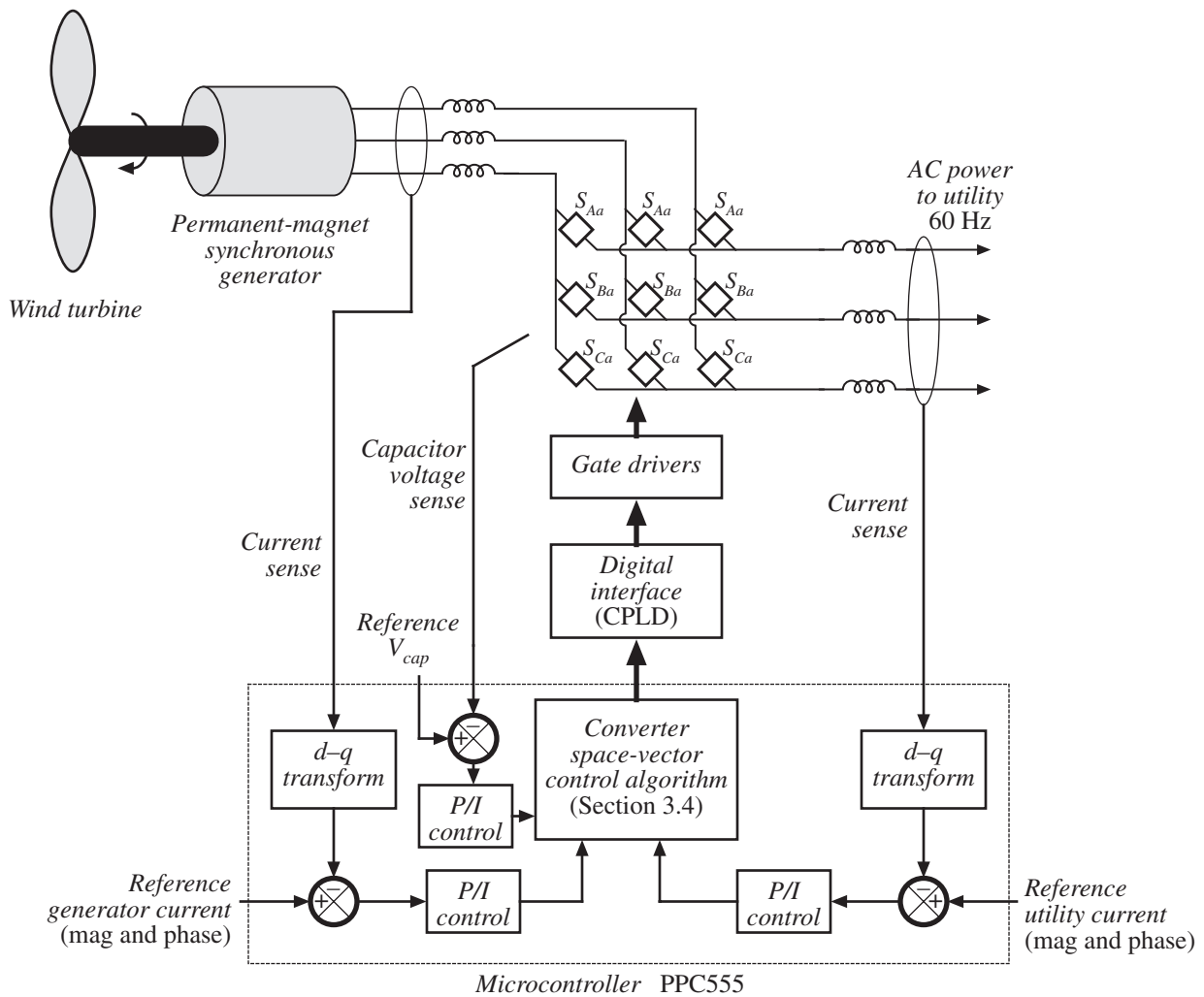


Figure 3-51. Block diagram of proposed controller

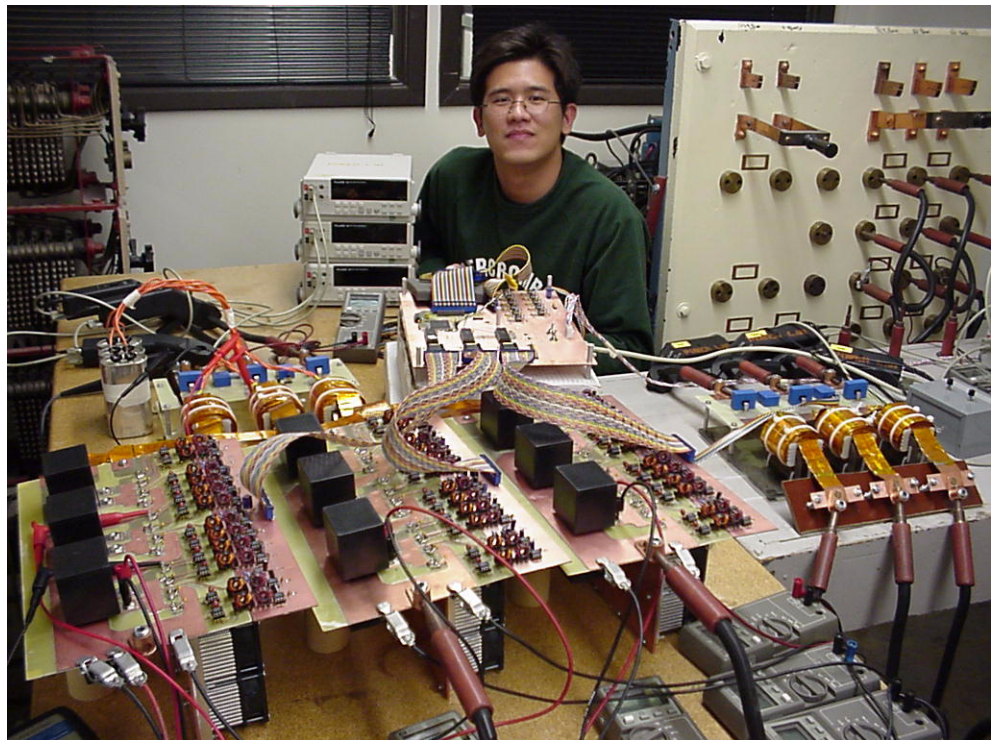
4.0

Prototype Development

4.1 INTRODUCTION

To demonstrate the validity of the proposed new converter, and to provide data and experience about its performance, we are constructing the laboratory prototype diagrammed in Figure 3-51 and photographed in Figure 4-1. This prototype is rated at 240 V at both its input and output terminals, and we believe that it should be capable of operating at approximately 50 kVA. It includes internal DC bus voltages of 400 V, and will use 600 V IGBTs. Later increase of the voltage to 480 V could be accomplished either by using 1200-V IGBTs, or by doubling the number of switch cells in a multilevel arrangement such as that depicted in Figure 2-3. The approach taken is to construct the switch cells using printed circuit boards, which can be manufactured by automated methods. This requires high-current traces on the boards; nonetheless, the current levels are commensurate with the values found in other power supply applications such as voltage regulator modules (VRMs) for high-speed microprocessors. The power stage components were constructed early on in the experimental portion of this project. We believe that the modular architecture of the proposed converter allows up-to-date manufacturing techniques to be employed to construct a high-

Figure 4-1.
Graduate research
assistant
Siththipong
Angkititrakul and
the prototype
converter system



performance converter that can be scaled up to the power levels required of near-future wind power applications.

The key challenge in this approach is developing and implementing practical control algorithms. Existing microelectronics technology, specifically the technology of complex gate arrays, memory, and microcontrollers, is a powerful resource that can be applied to this task. However, knowledge of how to apply this technology to control the proposed converter is lacking. The key results of the second half of this project have been (1) the development of algorithms for controlling the basic version of the proposed converter, described in the previous chapter, and (2) the hardware implementation of the algorithms using CPLDs, flash memory, and a microcontroller system. The hardware implementation of the control system, including the power stage elements, the microprocessor controller, and the logic interface and control circuitry, is documented in this chapter. We also report on the system's measured performance.

4.2 SWITCH MODULES AND POWER ELEMENTS

We have constructed power stage modules that contain three H-bridge switch cells per printed circuit board. The copper-clad boards use 10 mil copper, which can conduct at least 50 A (rms) per inch of trace width. Figure 4-2(a) is a photograph of the three boards, with a close-up of one switch cell given in Figure 4-2(b). The isolated gate driver circuitry can be seen along the lower side of each board. The square black objects are the polypropylene capacitors that maintain the DC bus voltages of the switch cells. Input and output connections to the filter inductors appear at the left and right sides of the boards.

The heat sinks and IGBTs are mounted on the bottom side of the boards. Figure 4-3 includes a photograph of the IGBTs, mounted on a copper heat spreader. Heat sinks and fans are mounted on the opposite side of the heat spreader. Figure 4-4 is a side view of the module. The heat sinks and fans are conservatively rated, and are sufficient to cool the 50-kW system even if the efficiency is as low as 90%.

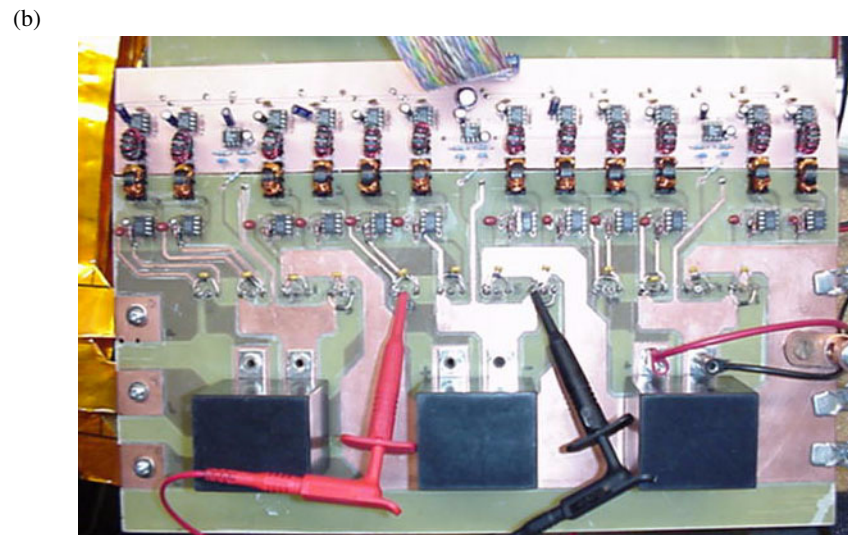
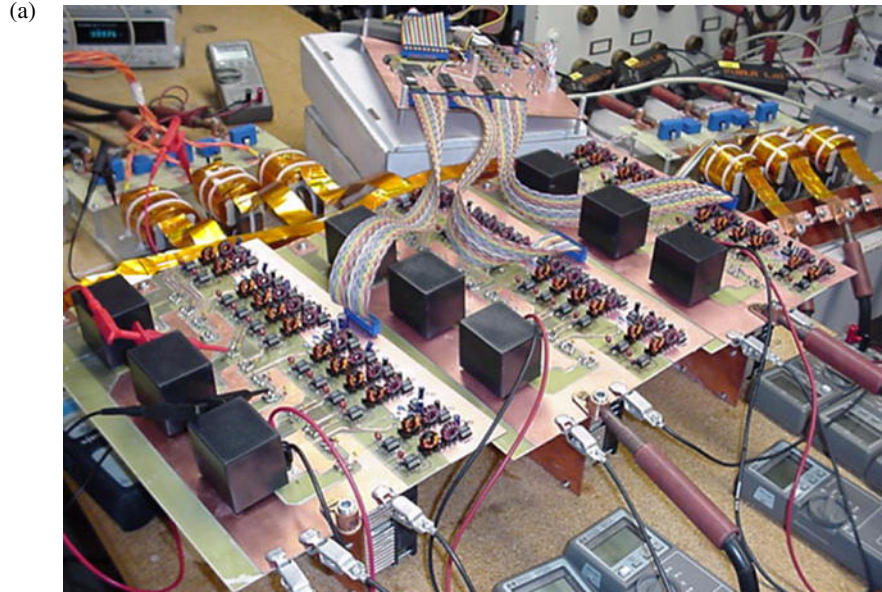
4.2.1 IGBT Devices

The prototype employs 600-V “SMPS Series” *n*-channel IGBT devices, Intersil part # HGTG30N60A4D (Intersil Corporation, Milpitas, California.) The TO-247 packages include antiparallel “hyperfast” diodes. The data sheet ratings are

- Collector-to-emitter voltage 600 V
- Continuous collector current 60 A
- Pulsed collector current 240 A.

We purchased these devices for \$9.76 each, in an under-100 quantity. Our prototype employs 36 of these devices, for a total power silicon cost of \$351.36. If the converter meets our goal of producing a rated power of 50 kVA, the cost per kVA of the power silicon is \$7.03/kVA. This figure is consistent with our earlier estimates of IGBT costs in wind system inverters (Erickson, Al Naseem, and Changtong 1999). We would expect that this cost would decrease in a manufacturing environment where the devices are purchased in larger quantities.

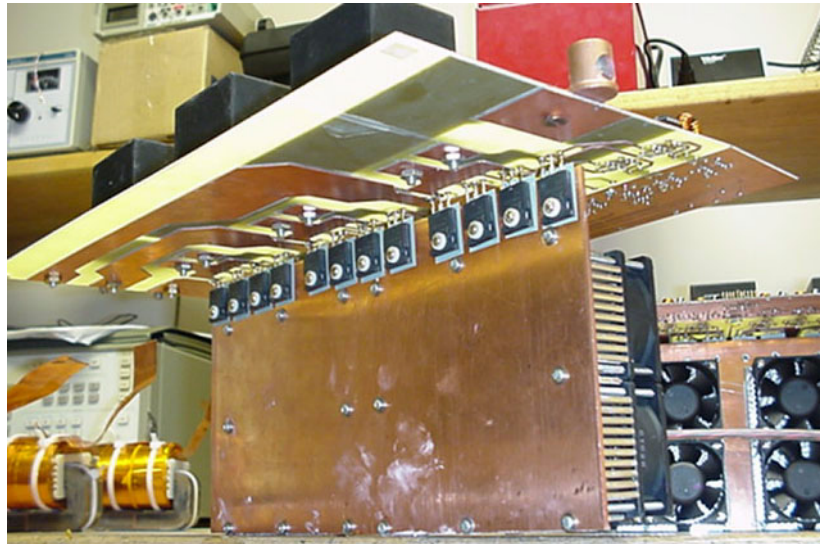
Figure 4-2. Power stage modules, top view: (a) three printed-circuit boards each contain three H-bridge switch cells, for a total of nine switch cells and (b) close-up of one switch cell. Isolated gate drivers, DC capacitors, and input and output phase connectors can be seen. IGBTs and heat sinks are mounted on the bottom side of the board.



The prototype employs 400-V DC buses in each switch cell, and hence the IGBT voltages are derated by a factor of 67%. The data sheet continuous collector current rating of 60 A is based on a case temperature of 110°C, and 75 A continuous rating is possible if the case temperature is maintained below 90°C. However, maximum currents under actual operating conditions depend on the total loss within the package, including switching loss. The data sheet also notes that these devices can be used in PWM DC–DC converters at frequencies up to 300 kHz if the current is limited to 30 A. We expect that these devices should operate reliably in our application at currents greater than 30 A, and it may be possible to approach 60 A.

If the converter operates at 50 kVA and 240 V_{rms}, the per-phase inductor currents will be equal to 120 Arms. This phase current will divide between three branches of the switch matrix, and additionally between two paths within each switch cell. We believe that the IGBTs should be able to handle the current with a comfortable safety margin. One goal of the experimental research is to establish a reasonable limit

Figure 4-3. Bottom side of printed circuit board, showing IGBTs mounted on copper heat spreader



for the output current that can be produced using IGBTs of a given rating; our estimate of 50 kVA for these devices may be conservative. Actually, the devices in this converter should be capable of producing more than 100 kVA of rated output power if the switching loss is sufficiently low. This would reduce the specific cost of the power silicon to approximately \$3.50/kVA. However, we should note that the specific costs of the reactive elements described in the next two sections are substantially higher than the cost of the power silicon. For this reason, it is worthwhile to increase the switching frequency; this increases the silicon cost while reducing the costs of the reactive elements, and can reduce the overall cost of a system that includes discrete filtering.

The switching frequency of our laboratory prototype has been limited primarily by the capabilities of the microcontroller and the algorithm implemented in the logic interface circuitry, as described in Section 4.3. As we have debugged the prototype and improved our design, we have been able to increase the switching



Figure 4-4. Side view of two printed circuit boards. Heat sinks and fans can be seen, mounted on the copper heat spreaders. The black rectangular objects are the DC polypropylene capacitors.

frequency from 1 kHz, to 10 kHz, and recently to 50 kHz. The switching frequency is now limited by the layout and the gate driver integrated circuits (ICs). In the continuation project, we propose to further improve the design so that the switching frequency is limited by the capabilities of the IGBTs. This would allow experimental data to be collected on the trade-off between IGBT cost and reactive element cost, enabling the power stage design to be optimized.

4.2.2 DC Bus Capacitors

The capacitors employed in the DC buses of the switch cells were initially 2 μF polypropylene devices, rated for operation as snubbers in IGBT inverters. They are Cornell Dubilier part #SCD205K122A3Z25 (Cornell Dubilier Electronics, Inc., Liberty, South Carolina), with the following ratings:

- Voltage 1200-V DC
- dv/dt 400 V/ μs
- Equivalent series resistance 4 m Ω
- Current 30.1 Arms.

The dimensions of these capacitors are: width = 1.8 in (2.6 cm), length = 2.2 in (5.6 cm), height = 2.0 in (5.1 cm). Given their high voltage ratings, these capacitors could also be employed in 480-V (or higher) applications having an 800-V DC bus voltage and a switching frequency of 100 kHz.

Because the switching frequency of this prototype so far has been substantially below 100 kHz, it was necessary to increase this capacitance. The prototype now employs two 4.7- μF 600-V capacitors, Cornell Dubilier part #SCD475K601A3Z25, each having the dimensions of the 2- μF capacitor we described above.

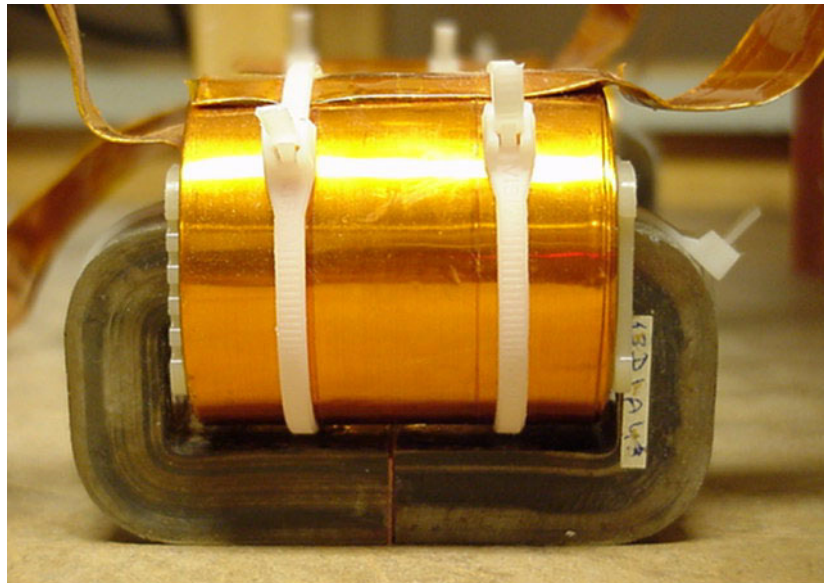
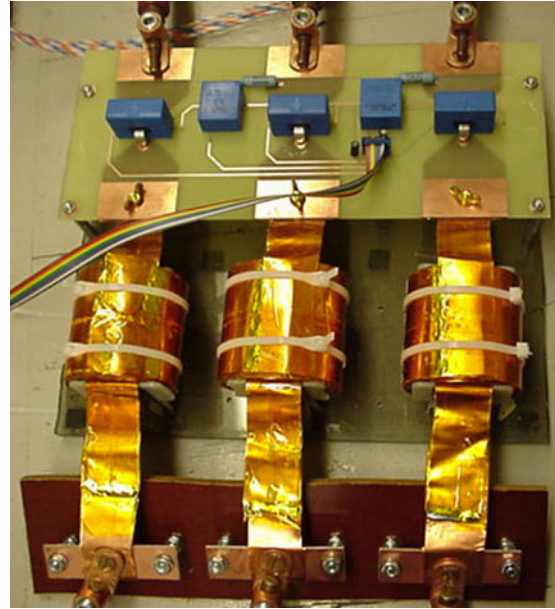
4.2.3 Filter Inductors

The prototype includes filter inductors at both the generator side and the utility side. The three input inductors are shown in Figure 4-5. All six inductors are identical, and preliminary versions have been built to the following specifications:

- Inductance: 0.2 mH
- Saturation current: 50 A
- Winding: 26 turns of 8-oz copper foil
- Air gap: 1.64 mm
- Core material: iron-based Metglas (Metglas®, Inc.) amorphous alloy cores, $B_{max} = 1.4$ T
- Core size: Applied Micro Circuits Corporation (AMCC; San Diego, California) AMCC63
- Dimensions: height = 10.2 cm; width = 5.2 cm; length = 3.0 cm
- Core cross-sectional area: 3.9 cm².

We paid \$54.82 for each AMCC63 Metglass core. Six cores are required if we want to provide filtering of the input and output currents. These inductors are suitable in size for a 15-kVA converter that operates at a

Figure 4-5. Filter inductors. Top: input-side inductors, one per phase. The input voltage and current sensors can also be seen at the top of the photo. Bottom: close-up of one inductor.



switching frequency of 10 kHz. The cost of the copper is relatively small. Hence, the cost per kVA of these Metglas filter magnetics is approximately \$33.00/kVA, which threatens to dominate the cost of the power electronics. Again, there is some cost break for purchasing these cores in high volume, but the potential reduction in cost is only 20% to 30%. Unless the cost of Metglas undergoes a major reduction, it would appear that we should search for a different approach.

Using Metglas is appropriate at switching frequencies up to 10 kHz. For switching frequencies approaching 100 kHz, ferrite may be a better solution. It has the potential to substantially reduce the size and cost of the filter magnetics. The above design is limited to peak AC phase currents of 50 A, and hence will not allow operation at 50-kVA rated power. We intend to first investigate the upper limit on switching frequency that our design allows, and then redesign the inductors as appropriate. Note that, in the DC–DC converter field, reductions in magnetics size of more than an order of magnitude are observed as the

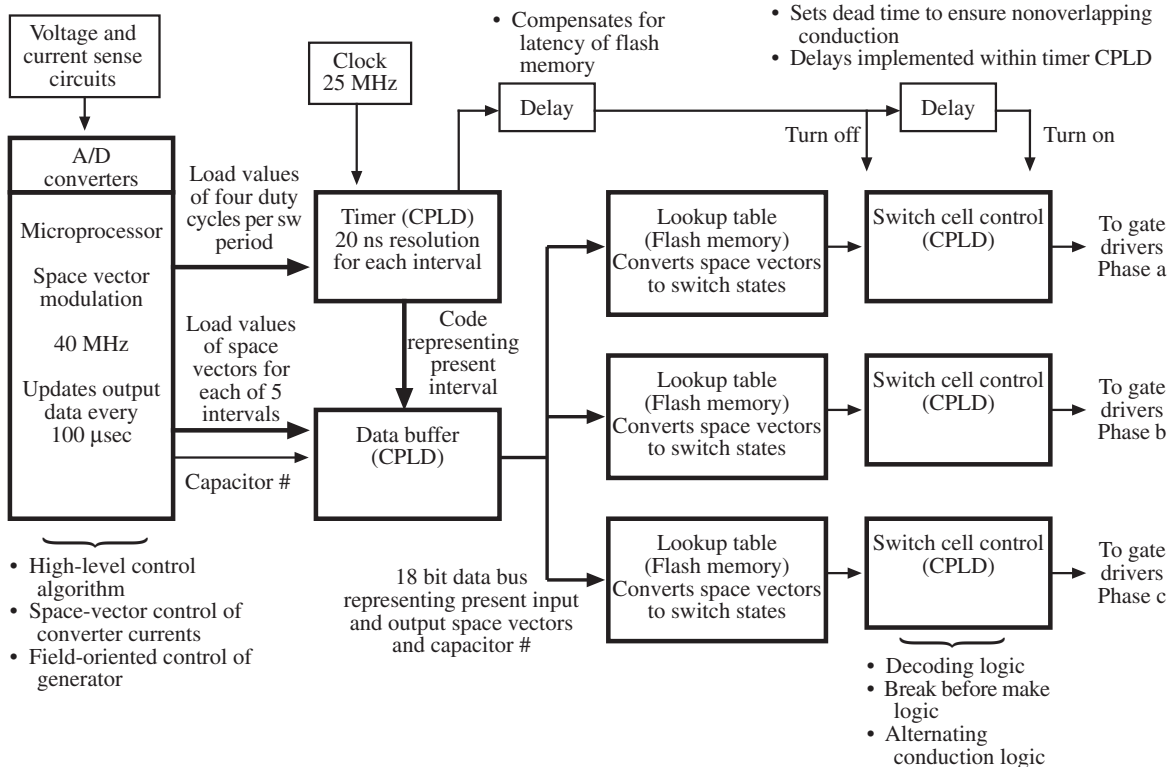


Figure 4-6. Block diagram of the control system hardware

switching frequency is increased from 20 kHz to 250 kHz (Erickson and Maksimovic 2001), and ferrite is the most common core material.

4.3 CONTROL CIRCUITRY

Figure 4-6 is a block diagram of the control system hardware. The utility and generator voltages and currents are sensed by Hall effect devices, and are digitized using analog-to-digital converters (ADCs). The microcontroller transforms these into d - q coordinates. The DC capacitor voltages of the nine switch cells are also measured using differential amplifier circuits, and digitized using ADCs. The microcontroller performs the SVM algorithm described in Sections 3.4 and 3.5, and commands the switching of the semiconductor devices. The microcontroller is interfaced to the switch cells through complex programmable logic devices (CPLDs); in our current system, there are five CPLDs and three flash memory chips. The CPLDs are addressable by the microcontroller, and store the current state of all switches. In addition, the state of all switches during the next subinterval can be loaded into the CPLDs. At the beginning of a subinterval, the microcontroller commands the CPLDs to change their outputs to the new states, which causes the IGBTs to switch.

To avoid cross conduction of the IGBTs during their switching transitions (which would lead to momentary shorting of the DC bus voltages through the IGBTs), the turn-off transitions of the IGBTs occurs first. In other words, those IGBTs that were previously on, but will be turned off, are switched first. After a controllable delay (the 200-ns block illustrated in Figure 4-6), the turn-on transitions are triggered

(i.e., the IGBTs that were previously off, but will be turned on, are switched). The outputs of the CPLDs are connected through isolated gate driver chips to the IGBTs.

4.3.1 Microcontroller

The microcontroller is a Motorola Power PC device, the PPC555 (Motorola, Austin, Texas). The microcontroller system includes A-to-D converters, digital outputs, timers, and other elements. It operates at a 40-MHz clock frequency. Figure 4-7 is a photograph of the microcontroller board connected to the PC development system.

The microcontroller implements a general routine to select the capacitor based on the locations of the input- and output-side reference space vectors, as described in Section 3.4.2. It then implements the space vector control algorithm based on the choice of capacitor. So far, only two-level control has been implemented.

The microcontroller includes a periodic interrupt timer (PIT) that activates the A-to-D converters and the calculation flow of the microcontroller. In the present implementation, this timer is set to interrupt every 100 μ s. In consequence, the microcontroller provides an updated choice of space vectors every 100 μ s (i.e., at a 10-kHz rate). This rate is limited by the speed of the microcontroller and the efficiency of its programming.

The length of the switching period is determined by the CPLDs, and need not coincide with the 10-kHz microcontroller rate. In our current prototype, the switching frequency is equal to 50 kHz; this allows the sizes of the reactive elements to be better optimized according to the capabilities of the power semiconductor elements, rather than the microcontroller speed. Each switching period of 20 μ s is further divided into five subintervals, as illustrated in Figure 4-8. These five subintervals are determined by the choice of input and output space vectors, as well as the respective duty cycles. In the current implementation, the input and output space vectors requiring the smaller duty cycles are output first,

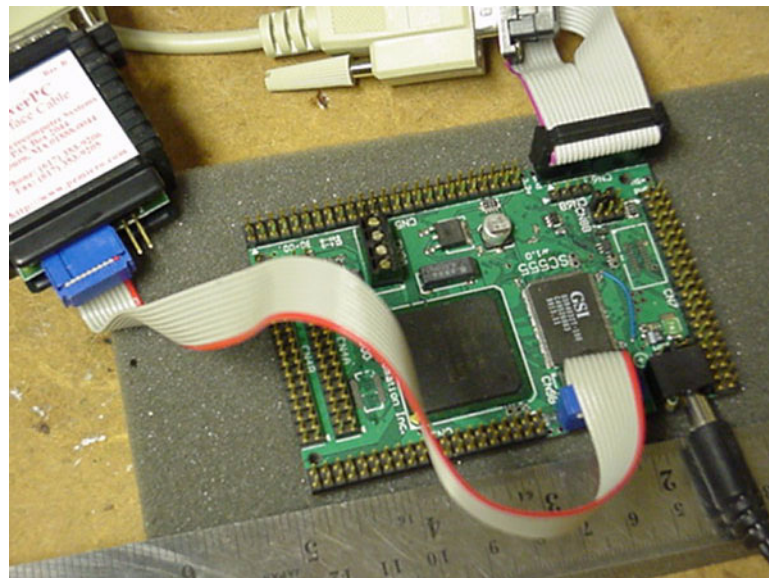


Figure 4-7. Microcontroller board

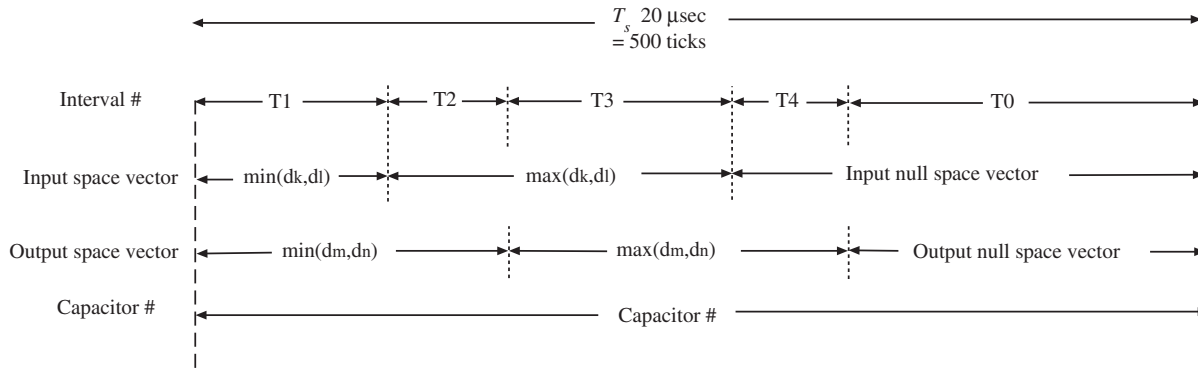


Figure 4-8. Timing details: each switching period is divided into five subintervals

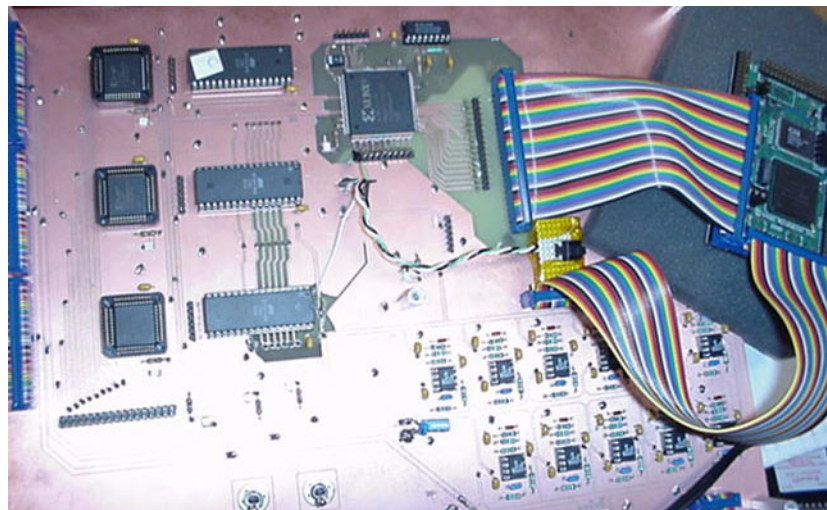
followed by the space vectors needing the longer duty cycles, followed by the null space vectors. Because the switching frequency is faster than the microcontroller update rate, the CPLDs use the same data over multiple switching periods.

The input and output space vectors for each subinterval are coded and sent through the I/O port of the microcontroller to the CPLDs, which latch the data. In addition, the number of clock ticks for each subinterval are also output to the timer CPLD. In the current prototype, each 20- μs switching period is divided into 500 ticks, so the five subinterval lengths are controlled with a resolution of 40 ns.

4.3.2 Complex Programmable Logic Devices

Five CPLDs are used in the prototype; these could be combined into one large device if desired. These CPLDs implement the functions of timing and PWM, buffering the data from the microcontroller and decoding the data to drive the IGBT gates of each switch cell. In addition, these devices interface the lookup tables (stored in flash memory) that store the control algorithms. The CPLDs and flash memory constitute the heart of the converter control system, and their development has constituted the bulk of the project work over the last year. Figure 4-9 is a photo of the CPLD board. We describe each of these

Figure 4-9. Printed circuit board containing the CPLDs. The microcontroller can be seen to the right side. To the left of the ribbon cables are the timer CPLD, the three flash memory chips, and the three switch cell control CPLDs. The data buffer CPLD is on the bottom side of the board. Differential amplifiers for sensing the DC capacitor voltages can be seen below the ribbon cables.



elements in detail below, and code listings are given in Appendix B. The “timer CPLD” controls the durations of the subintervals. A Xilinx XC95216 chip is used (Xilinx, Inc., San Jose, California). A logic diagram is given in Figure 4-10. This CPLD latches five sets of nine-bit data from the microcontroller into its buffers; these data represent the number of clock ticks for the length of each subinterval. The clock ticks are generated by an external 25-MHz (40-ns) clock.

A double-buffering scheme allows the converter switching frequency to differ from, and be asynchronous with, the microcontroller data rate. The first data buffer, Buffer1, interfaces with the I/O port of the microcontroller. This buffer is addressed by the microcontroller, and latches the subinterval length data for the next update of this data. The second data buffer, Buffer2, latches the subinterval length data that are currently being used. An update signal controls the transfer of data from Buffer1 to Buffer2. This signal is generated within the timer CPLD. It is asserted only when all new data values are valid within Buffer1, and the converter is in subinterval T0 (when the input and output operate with the null space vector—see Figure 4-8). This approach avoids glitches by ensuring that subinterval lengths are not updated in the middle of a switching period.

An interval counter keeps track of the current subinterval number (0 to 4). This count drives two multiplexers that output the lengths of the current and next subintervals. The first multiplexer, Mux1, provides the length of the current subinterval to an incremental counter that times the interval. At the end of the subinterval, a turn-off pulse is generated that commands on-to-off IGBT switching transitions to occur. After a controllable delay, a second pulse is generated, which initiates off-to-on IGBT switching transitions. The second multiplexer, Mux2, provides the length of the upcoming subinterval to a comparator. This length is compared with a controllable minimum pulse width that is currently at 1.2 μ s. If the commanded interval length is less than the minimum limit, the subinterval is skipped. This minimum pulse width is needed to prevent glitches caused by gate delays and flash memory latency.

Figure 4-10. Block diagram of the timer CPLD

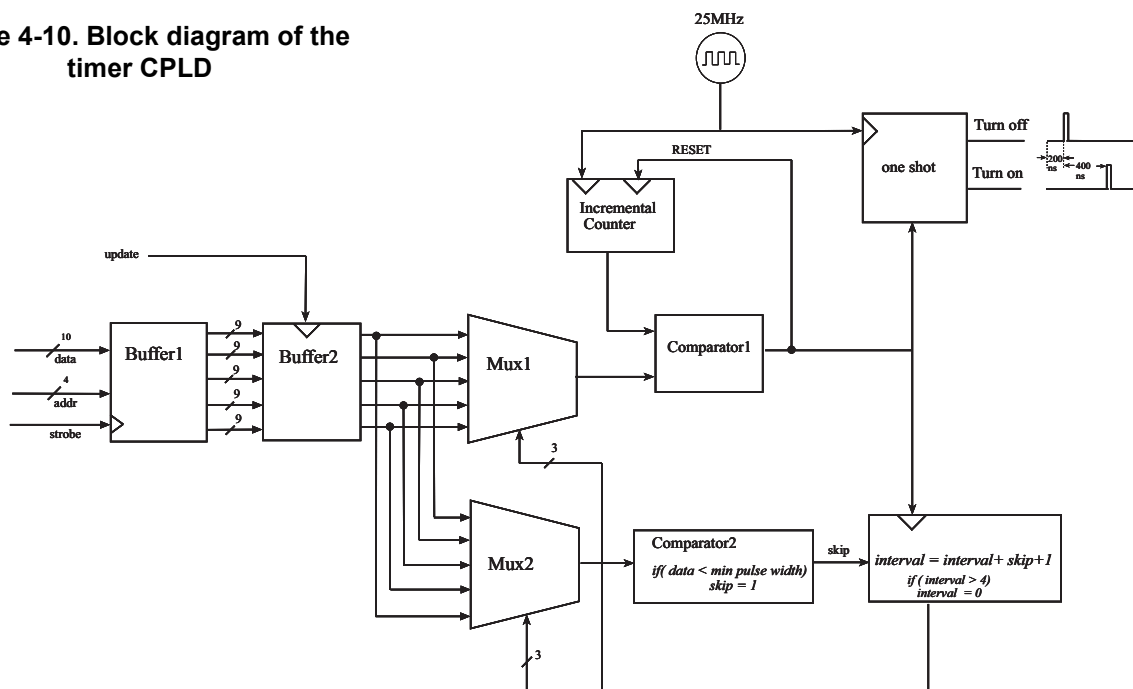


Figure 4-11. Block diagram of the data buffer CPLD

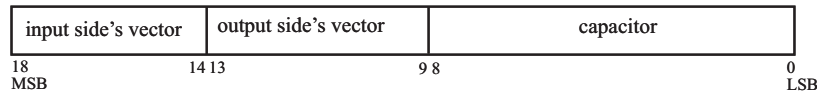
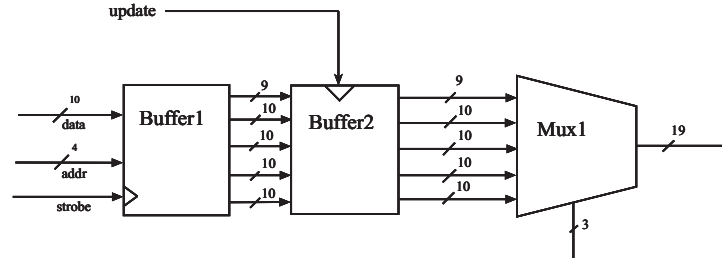


Figure 4-12. Bit pattern for the output of the data buffer CPLD

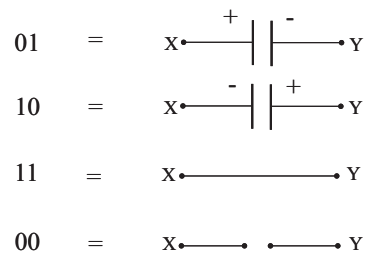
The “data buffer CPLD” stores the input and output space vectors for each subinterval. A block diagram is given in Figure 4-11. As with the timer CPLD, a double-buffering scheme is employed so that the microcontroller and power stage can operate asynchronously. The update command from the timer CPLD controls the transfer of data between these two buffers. In addition, a multiplexer feeds the correct space vector information for the current subinterval to the flash memory.

The capacitor employed in the current switching period is represented by a nine-bit word. A high bit indicated that the corresponding capacitor is employed. Bit [0] refers to the capacitor in branch *Aa*; Bit [8] refers to the capacitor in branch *Cc*. Our current control scheme employs only one capacitor per switching period, meaning that exactly one bit will be high during a given switching period. However, the encoding scheme admits future control schemes that employ multiple capacitors during a given switching period.

The input- and output-side space vectors for each subinterval are represented by five bit words. The words can represent all 19 space vectors in the stationary *d-q* reference frame, so ten bits are needed for each subinterval. The output of the data buffer CPLD is a 19-bit word that represents the capacitor, input-side space vector, and output-side space vector for the current subinterval. The assigned mapping of these bits is diagrammed in Figure 4-12.

A “lookup table” decodes the input and output space vector data for the current subinterval, and provides logic signals that command each switch cell. Each phase employs a 512-kB flash memory chip. Each of these chips contains the data for the three switch cells that are connected to the same input phase. The input (address lines) of the table are the space vector and capacitor data defined in Figure 4-12. The output of the table includes two bits per switch cell, which represent the state of the switch cell as illustrated in Figure 4-13. Each chip, then, produces six bits of output data, and the remaining two bits are unused.

Figure 4-13. The output of the lookup table includes two bits per switch cell, which represent the conducting state of the switch cell as shown here.



The lookup table is the heart of the control scheme. Appendix A lists the entries in the lookup table for our prototype, employing a single-capacitor control scheme. Invalid inputs, such as combinations involving multiple capacitors or invalid space vectors, result in a zero output that turns off all IGBTs. Multiple capacitor control schemes could be accommodated by simply reprogramming this table.

The “switch cell control CPLDs” take the outputs of the lookup tables, and provide appropriate logic signals to the inputs of the individual gate drivers. In the prototype, we chose to implement one of these per board; that is, one per input phase. These CPLDs are relatively small Xilinx XC9572 devices. These circuits accept the turn-on and turn-off signals from the timer CPLD, along with the coded switch cell state data from a lookup table.

There are two ways to realize the 11 conducting states of a switch cell—both upper IGBTs can conduct, or both lower IGBTs can conduct. To distribute the conduction losses between devices, the switch cell control CPLDs contain R-S flip-flops that alternate the conduction path between these two choices.

The schematic of this CPLD circuitry is diagrammed in Figure 4-14. This figure also summarizes the truth table for the decoding logic.

4.3.3 Gate Driver Circuitry

Design of the gate driver circuitry for PWM inverters continues to be problematic, in spite of the efforts of engineers in the power electronics field over many decades. A floating drive is required, which can maintain any duty cycle from zero to one for an extended length of time. This circuitry usually requires a floating power supply that is referenced to the emitter/source/cathode of the transistor. The current rating of the driver must be adequate not only to switch the IGBT quickly enough, but also to source or sink the current that flows in the gate-to-collector capacitance when the collector voltage changes. Reliable operation with a driver having a given current capability requires that the collector dv/dt be limited. In practice, this is accomplished by limiting the switching speed of the IGBTs, and by operating with a known maximum capacitor voltage. In addition, it is now common practice to employ a substantial negative voltage to bias the gates of IGBTs in the off state.

An additional issue is the generation of common-mode noise, usually through the interwinding capacitances of the transformers that transmit the gate drive signals and power for the driver circuitry. Even with careful transformer design, common-mode filters may be needed to avoid disrupting the control circuitry. Common-mode noise also increases directly with the collector dv/dt , so that noise levels worsen as the input voltage is increased.

A final issue is the cost of the gate driver circuitry, relative to the cost of the IGBTs themselves. If the cost of an IGBT is equal to the cost of its driver circuitry, the semiconductor cost per kVA is effectively doubled. We would probably be willing to spend \$10 or \$20/IGBT on the circuitry to drive \$100 IGBTs, but only one tenth as much to drive \$10 IGBTs. Consequently, it is worthwhile to devote engineering effort to designing reliable and inexpensive gate driver circuitry, as well as to optimizing switch module size, such that the total semiconductor (IGBT plus driver) cost per kVA is minimized.

D_IN1(1:0) is coded 2-bits signal represents switch cell state

SVM_decoder

Input		Output			
D_IN	L	4	3	2	1
00	X	0	0	0	0
01	X	1	0	0	1
10	X	0	1	1	0
11	0	0	0	1	1
11	1	1	1	0	0

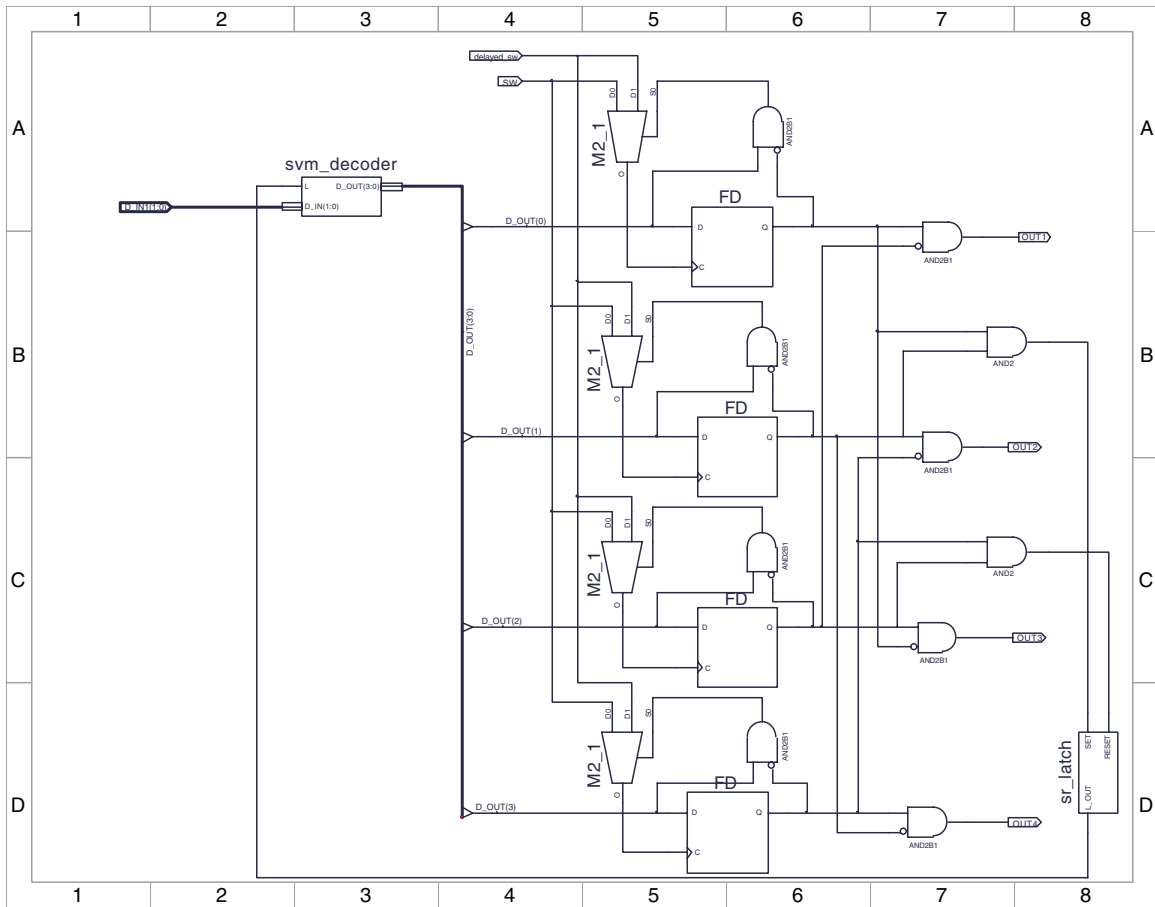
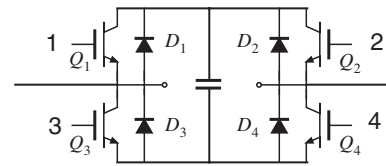
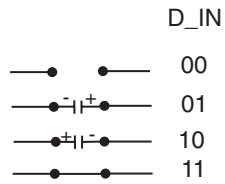


Figure 4-14. CPLD internal circuitry to decode states of switch cell

We considered a number of approaches for implementation of the gate driver circuitry. Isolated or high-side driver circuits used in DC–DC converters are usually not suitable for inverter application such as this one, because of the limits on maximum or minimum duty cycle imposed by a gate drive transformer or a bootstrap power supply. Gate drive circuits that employ an optoisolator for transmission of the gate drive logic signal avoid this issue, and also avoid the problem of common-mode noise being transmitted through a signal transformer. However, these circuits require a floating power supply, which has a transformer of its own that can lead to substantial common-mode noise as well. Commercial gate driver modules are available from companies such as SEMIKRON (Nurnberg, Germany). These often have nice features, but are limited in speed (with propagation delays of one or several microseconds) and can cost almost as much as the devices they are intended to drive. They also include internal floating power supplies and can have common-mode noise issues.

Yet another option is the use of commercially available chipsets that transmit both the logic signal and the floating power through a common transformer. An input-side IC generates a high-frequency AC voltage for the transmission of power through a small high-frequency transformer. This signal is also modulated by the gate drive logic signal. An output- (IGBT-) side IC rectifies the voltage on the secondary of the transformer, yielding the power supply for the output-side circuitry. This IC also demodulates the signal to recover the gate drive logic command, and drives the gate of the IGBT. These chipsets are available from several manufacturers, such as Unitrode/Texas Instruments (TI; Dallas, Texas).

For this project, we chose the Unitrode/TI UC3724/3725 eight-pin isolated gate driver/transmitter chipset. These devices are inexpensive relative to the modules mentioned above, and have short propagation delays (tens of microseconds). A small ferrite toroidal core was employed in the high-frequency transformer for each gate. An additional small common-mode filter was placed in series with the primary of each transformer. These devices were able to drive the Intersil HGTG30N60A4D IGBTs at switching frequencies up to 50 kHz, and with capacitor voltages exceeding 150-V DC. However, at 200 V DC the thermal limits of these devices is exceeded, and converter operation becomes unreliable. This is currently the active constraint that limits the voltage and power throughput of the converter prototype, and efforts to overcome this limit are currently under way in a follow-on project.

We should also note that TI recently discontinued the UC3724/3725 chipset, and other parts must be designed into new products. We can conclude that IC manufacturers have had difficulty in designing gate driver chips or modules that can compete economically with discrete gate driver designs.

4.4 EXPERIMENTAL RESULTS

We tested the prototype in our laboratory as illustrated in Figure 4-15. A three-phase variac provides a 60-Hz, variable 0- to 440-V three-phase source that drives the input of the converter. Five-ohm resistors (not shown) were placed in series with the variac output, to limit the current under fault conditions. These resistors are for prototype testing purposes only, and would not be part of the final system. The output of the converter was connected to a resistive load. The input-side utility voltages were sensed, so that the input-side reference space vector is derived from the 60-Hz utility voltages. For this experiment, we have programmed this reference space vector to be in phase with the 60-Hz input, but to have controllable magnitude.

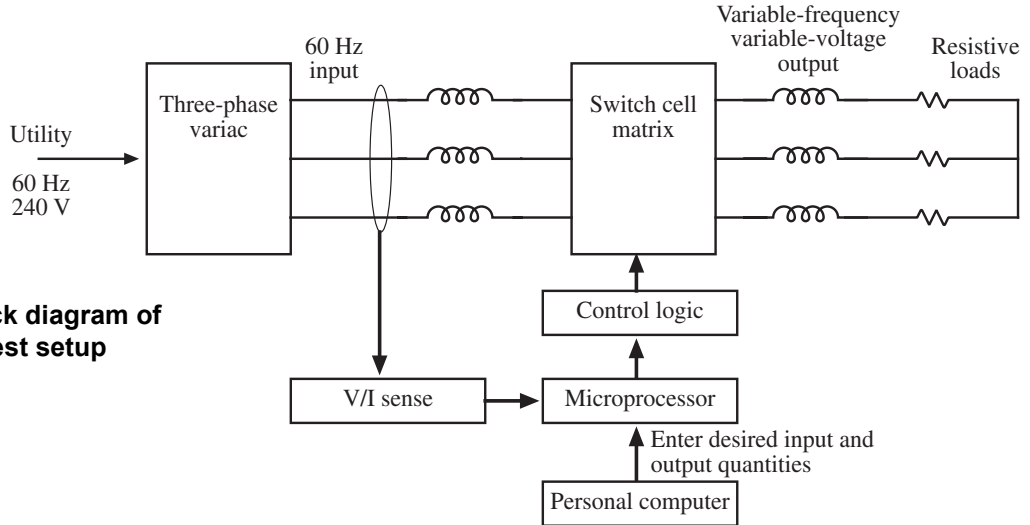


Figure 4-15. Block diagram of laboratory test setup

Although we have included sensor circuits that can monitor all DC capacitor voltages, no control of these voltages has been implemented in our existing control algorithms. Such control could be implemented in the future.

The output reference space vector can be chosen arbitrarily in software. We are able to select the output frequency, magnitude, and phase through programming of the microcontroller. Sensors have also been constructed for measuring all input and output voltages and currents; these are intended for implementing input and output current control in the future.

The prototype system has been tested at a variety of operating points. Here, we present data for three different choices of output frequency, input and output voltage, and/or power. Next, we summarize the current status of the experimental prototype.

4.4.1 Case 1

The controller was programmed to produce an output frequency of 20 Hz, with the following modulation indices:

$$M_{in} = \frac{2V_{ref-in}}{3V_{cap}} = 0.63 \tag{4-1}$$

$$M_{out} = \frac{2V_{ref-out}}{3V_{cap}} = 0.57 \tag{4-2}$$

Input and output wave forms are illustrated in Figure 4-16. At this operating point, the capacitor voltage V_{cap} is approximately 150 Vdc. The top trace, trace 1, is the line-to-line voltage that appears at the input (60-Hz) side of the switch matrix. This PWM voltage switches between zero, $+V_{cap}$, and $-V_{cap}$, with a switching frequency of 50 kHz. Trace 2 is a similar line-to-line voltage that appears at the output (20-Hz) side of the switch matrix. Traces 3 and 4 are the resulting currents that appear in an input-side and an output-side inductor, respectively.

Figure 4-16. Input and output wave forms, Case 1. Trace 1: input-side line-line PWM voltage wave form, at 200 V/div. Trace 2: output-side line-line PWM voltage wave form, at 200 V/div. Trace 3: input-side phase current, at 5 A/div. Trace 4: output-side phase current, at 5 A/div. Horizontal scale: 10 ms/div.

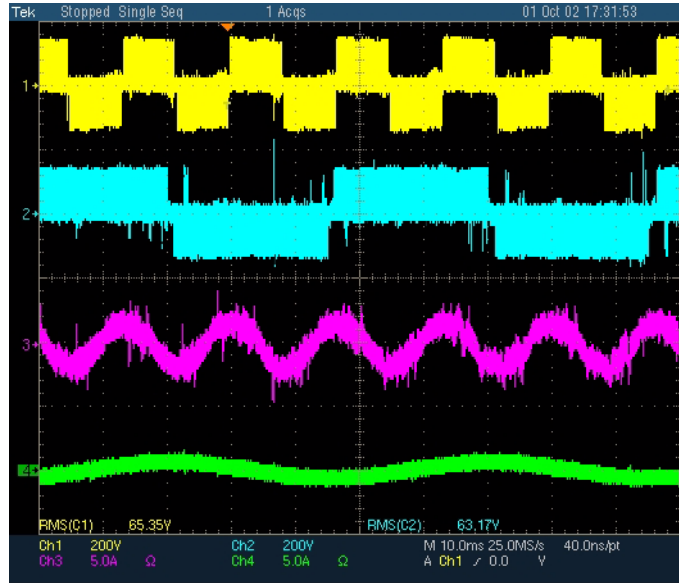


Figure 4-17. Output (20-Hz) line-to-line voltage wave forms for Case 1. Trace 1 (yellow): PWM voltage at the output of the switch network. Trace 2 (blue): load voltage, after filtering by L - C output low-pass network.

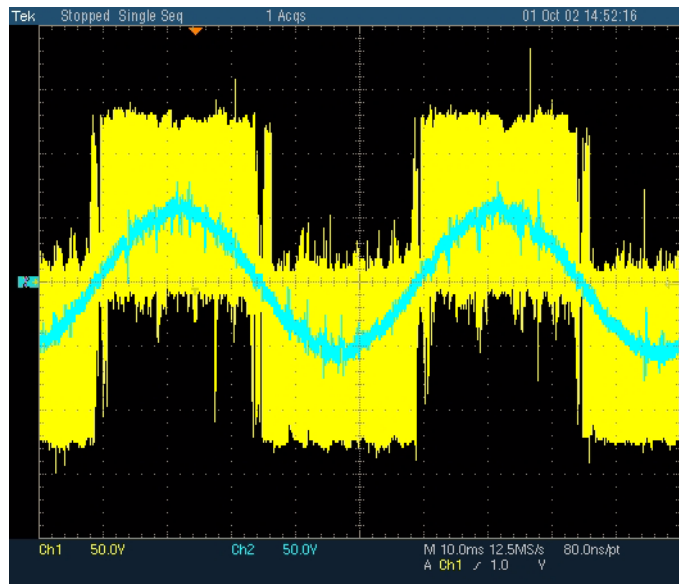


Figure 4-17 illustrates the output voltage produced at this operating point. Trace 1 is the PWM line-to-line voltage that appears at the output of the switch network, and is similar to Trace 2 of Figure 4-16. Although some high-frequency noise is present, we can see that the low-frequency component is a high-quality sinusoid that has low distortion.

Figure 4-18 illustrates the voltage across one of the DC capacitors. Trace 2 (blue) is the capacitor voltage, equal to approximately 125 V in this example. Trace 1 (yellow) is AC output (20-Hz) voltage, the same wave form as Trace 2 of Figure 4-17. Figure 4-19 is a similar plot that illustrates the variations of the capacitor voltages of two different switch cells. The top half of the screen shows the two DC capacitor voltages; the lower half of the screen shows the same wave forms with an expanded time scale. The capacitor voltage is not regulated by the controller. We can see that the average capacitor voltages tend to

Figure 4-18. Variation of DC capacitor voltage, without active control. Trace 1 (yellow): filtered load voltage. Trace 2 (blue): DC capacitor voltage. Both traces have scales of 50 V/div.

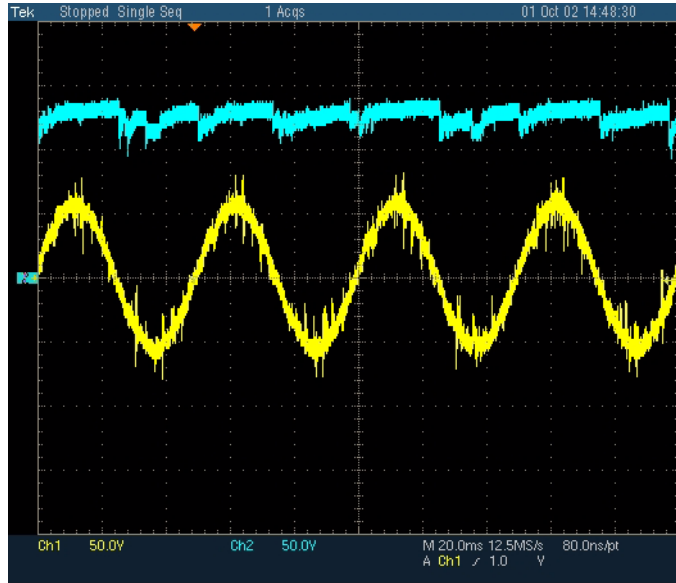
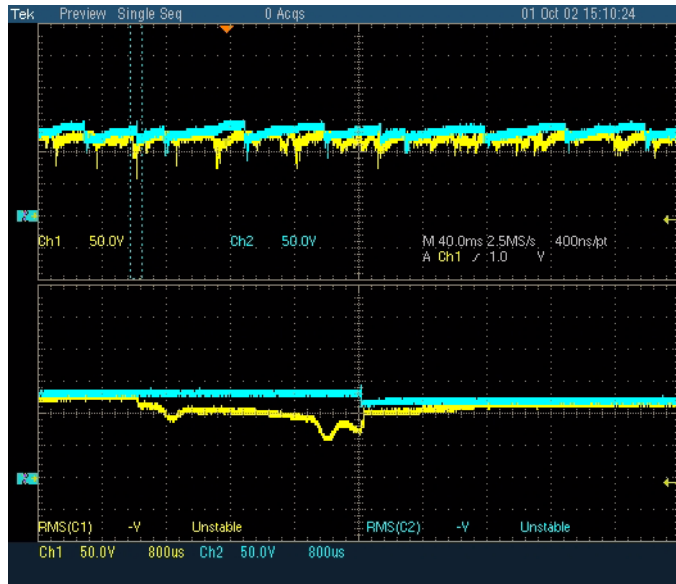


Figure 4-19. The DC capacitor voltage wave forms of two different switch cells. Trace 1 (yellow) and Trace 2 (blue) are both set to scales of 50 V/div with the same ground reference level. The upper half of the screen illustrates the measured wave forms, at 40 ms/div. The lower half of the screen shows the same wave forms at 800 μ s/div, between the cursors.



remain balanced between switch cells, and do not require active control. We would expect this to be true for the current experiment employing a single-capacitor control scheme and a resistive load, by analogy with the DC link case. However, we expect that when a generator is interfaced to the infinite-bus utility, regulation of the DC capacitor voltage will be necessary. The capacitor voltages should still remain balanced between switch cells. We also expect that independent regulation of the individual capacitor voltages will be necessary when multiple-capacitor/multilevel control schemes are employed.

Figures 4-18 and 4-19 also illustrate that there is some moderate amount of voltage ripple on the DC capacitors. In spite of the relatively small capacitance of the polypropylene capacitors, the magnitude of the 50-kHz voltage ripple is quite small. This is achieved through the high 50-kHz switching frequency. The dominant component of voltage ripple has a relatively low period of tens of milliseconds. This ripple

is caused by several factors, including the inability of the gate drivers to adequately drive the IGBTs, energy recovered from layout-induced ringing, and noise-induced false triggering of the drivers. In the lower half of Figure 4-19, we can see that Trace 1 decays in voltage for several milliseconds until, at the center of the screen, the IGBTs associated with the capacitor of Trace 2 are turned on to apply the Trace 2 capacitor voltage. Charge is then quickly transferred from the Trace 2 capacitor to the Trace 1 capacitor. Although this mechanism tends to equalize the capacitor voltages across switch cells, it is a relatively inefficient process. If the associated currents are large enough, they could even lead to failure of the IGBTs. We have been able to reduce this voltage ripple by improving the gate drive circuitry, and we believe that further improvements are possible with even better gate drivers.

4.4.2 Case 2

Case 2 illustrates that the converter can change the line frequency arbitrarily. The 60-Hz utility input is changed to a 120-Hz output. The modulation indices are $M_{in} = 0.63$ and $M_{out} = 0.58$. The input and output PWM line-to-line voltages and line currents are illustrated in Figure 4-20, and the output voltage wave forms are depicted in Figure 4-21. Again, the switching frequency is 50 kHz.

4.4.3 Case 3

Case 3 illustrates boosting the voltage magnitude. The modulation indices are $M_{in} = 0.50$ and $M_{out} = 0.63$. The DC capacitor voltages must be greater than or equal to the larger of the peak input and output line-to-line voltages. The 60-Hz input is converted to a 30-Hz output, and the switching frequency is again 50 kHz. The input and output wave forms are shown in Figure 4-22, and Figure 4-23 contains an expanded view of the output PWM voltage and filtered load voltage.

Figure 4-20. Input and output wave forms, Case 2. Trace 1: input-side line-line PWM voltage wave form, at 200 V/div. Trace 2: output-side line-line PWM voltage wave form, at 200 V/div. Trace 3: input-side phase current, at 5 A/div. Trace 4: output-side phase current, at 5 A/div. Horizontal scale: 4 ms/div.

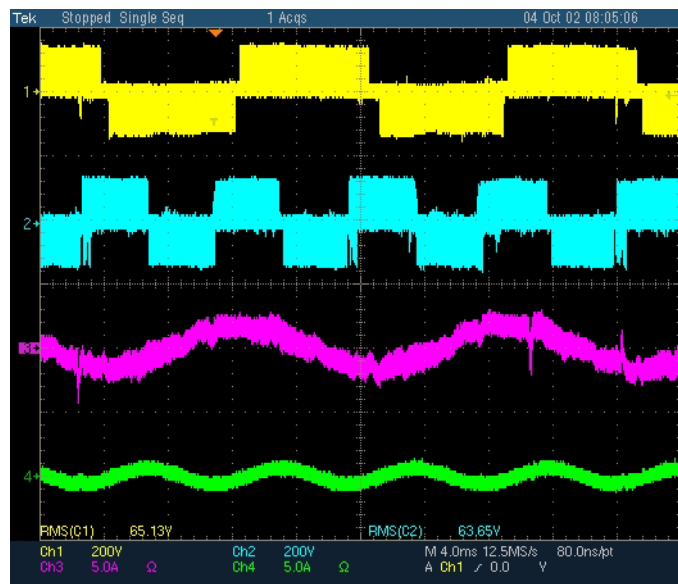
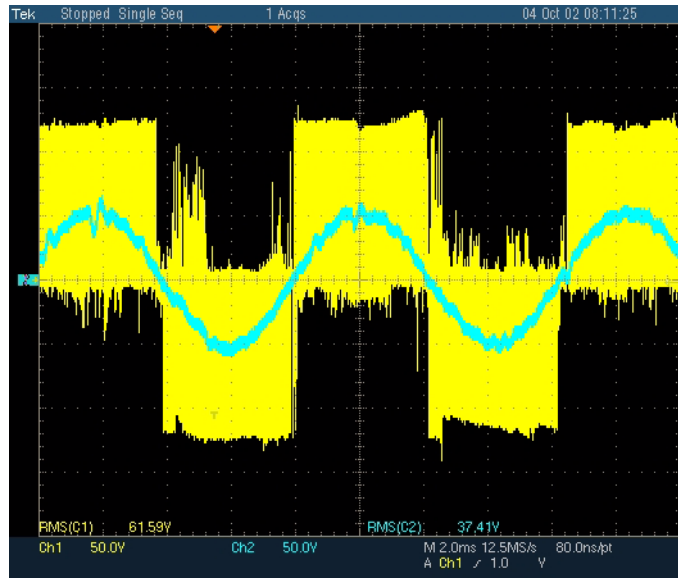


Figure 4-21. Output PWM line-to-line voltage wave forms, case 2. Trace 1 (yellow): PWM line-to-line voltage, 50 V/div. Trace 2 (blue): line-to-line voltage across load, after L - C low-pass filter, at 50 V/div. Horizontal scale: 2 ms/div.



4.4.4 Documentation of Switching Frequency

Figure 4-24 illustrates the 50-kHz switching of the IGBTs and diodes. Line-to-line voltages at the input and output sides of the switch matrix are shown. Note that the switching period is indeed equal to 20 μ s. Figure 4-24(b) shows the wave forms near the zero crossing of the average line-to-line input voltage. The upper trace remains at zero for ten switching periods. This occurs because the computed duty cycle is less than the minimum limit, and hence switching is suppressed. Also note that, because the microprocessor updates its control output at a 10-kHz rate, the same duty cycles and space vectors are employed for five switching periods before being updated.

Figure 4-22. Voltage and current wave forms, case 3. Trace 1 (top, yellow): PWM line-to-line voltage at input of switch network, 200 V/div. Trace 2 (blue): PWM line-to-line voltage at output of switch network, 200 V/div. Trace 3 (purple): input phase current, 5 A/div. Trace 4 (green): output phase current, 5 A/div.

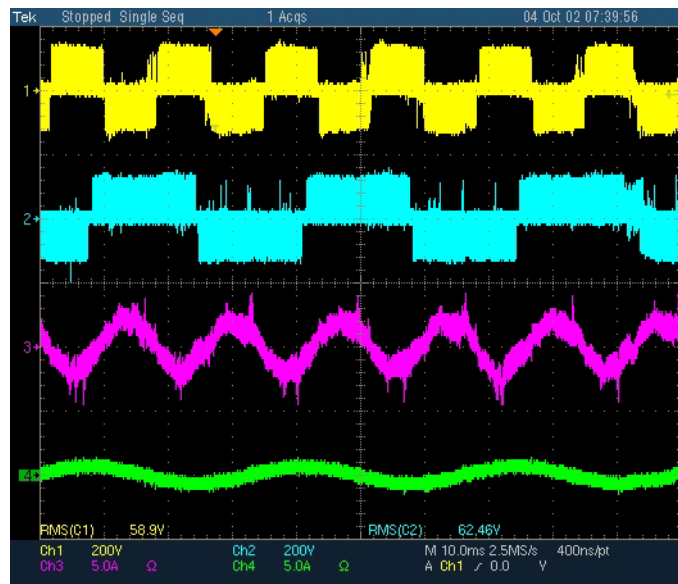


Figure 4-23. Output voltage wave forms, at 10 ms/div, for case 3. Trace 1 (yellow) is the line-to-line PWM wave form at the output side of the switch network. Trace 2 (blue) is the filtered voltage across the resistive load. Both voltages are displayed at 50 V/div.

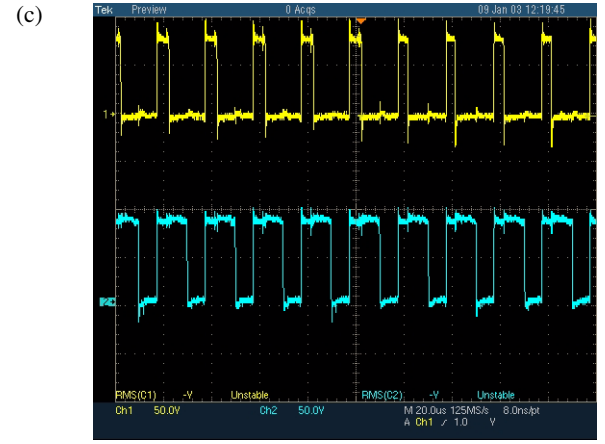
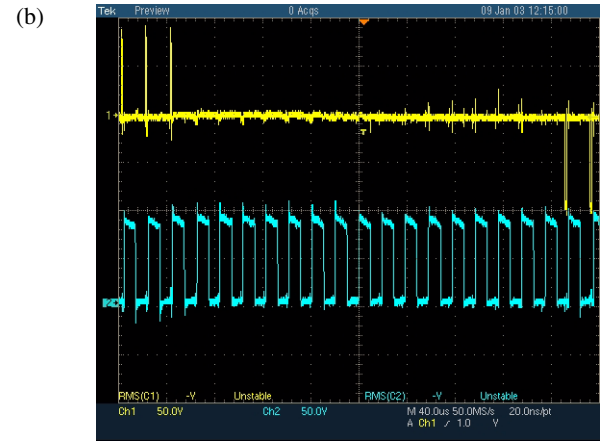
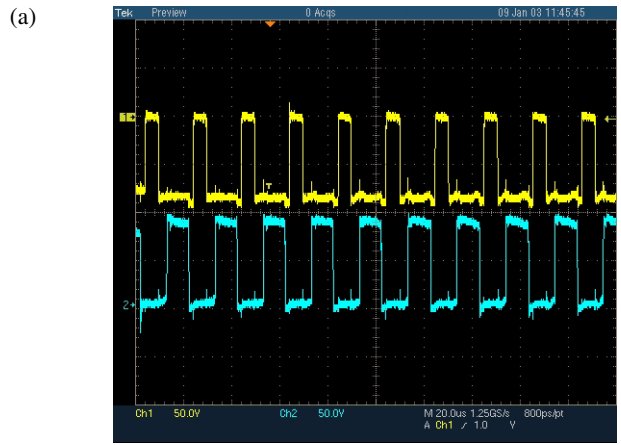
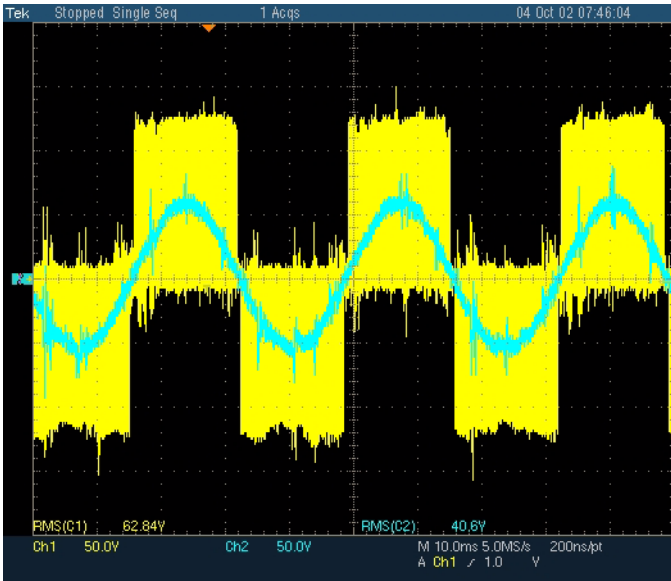


Figure 4-24. Input and output PWM line-to-line voltages, at three different points on the AC line wave form: (a) 50-kHz modulation, time scale 20 μ s/div; (b) 50-kHz modulation near the zero crossing of the input voltage wave form, time scale 40 μ s/div; (c) 50-kHz modulation, time scale 20 μ s/div.

4.4.5 Summary

The laboratory experiment proves that the proposed new modular matrix converter is valid and operates as claimed. Space-vector control of both the input and output side has been implemented, to convert a given three-phase input into a three-phase output of given desired frequency, magnitude, and phase. With the single-capacitor control scheme, we observed that the capacitor voltages naturally remained balanced and stable. The converter operated with an IGBT switching frequency of 50 kHz; the asynchronous control update rate of the microcontroller was approximately 10 kHz.

Although considerable engineering effort has been expended to develop and implement a suitable control scheme, the controller can be easily reproduced. Standard gate arrays and flash memory contain the heart of the control system; these are merely programmed as detailed in the appendices of this report.

Additional work is needed in the gate drive circuitry, before operation at rated voltage and power can be demonstrated. This would allow the converter efficiency to be measured and effective utilization of the power semiconductor devices to be demonstrated.

5.0

Summary

5.1 KEY RESULTS—CONVERTER EFFICIENCY

In the previous project, we developed an experimentally verified model of switching converter losses in wind power applications. This model predicts diode and transistor conduction losses, as well as switching losses caused by diode-stored charge and IGBT current tailing. In this project, we used the model to conclude that losses associated with the rectification process dominate the performance of converter systems in wind power applications. Further, we showed that multilevel conversion can address these identified efficiency issues, leading to improved performance and energy capture. We published a paper describing this result (Al-Naseem, Erickson, and Carlin 2000), and also generated a patent disclosure (Erickson, Al-Naseem, and Fingerish (May 2003)).

Ph.D. student Osama Al-Naseem participated in this work.

5.2 KEY RESULTS—NEW MULTILEVEL MATRIX CONVERTERS

We have derived a new type of multilevel matrix converter with unique properties that appear well-suited to wind power applications:

- Basic converter can switch to multilevel operation at low speed
- Potential low cost of modular bus bar structures
- Higher efficiency over wide speed range
- Scalability to higher voltage and power levels using relatively small, high-performance semiconductor devices.

We have developed control algorithms for the new converter, including a new control algorithm that is relatively simple, employing a single capacitor in the energy conversion process during each switching period. We have shown that controlling the basic operating mode of the converter is feasible using this algorithm. In addition, it enables modeling of the converter efficiency and dynamics, a topic to be pursued in the future.

In addition, we have developed a program to simulate the new matrix converter with simultaneous space vector control and capacitor DC voltage control. With this program, we demonstrated the basic operation of the converter, to prove that the converter is valid and can operate with arbitrary voltage conversion ratio and power factors. We published a paper describing these results (Erickson and Al-Naseem 2001), as well as a Ph.D. thesis (Al-Naseem 2001) and a patent disclosure (Erickson and Al-Naseem (May, 2003)).

Ph.D. students Osama Al-Naseem and Sitthipong Angkititrakul, as well as B.S./M.S. student Giancarlo Lujan, have participated in this work.

5.3 KEY RESULTS—LABORATORY DEMONSTRATION

We have constructed a working laboratory prototype that proves the validity of the basic version of the proposed new converter. It also proves that the proposed control algorithm works as claimed. This algorithm is implemented using programmable logic devices and a lookup table residing in flash memory. The converter switches at 50 kHz, and the power stage elements are interconnected using printed circuit boards with 10 mil copper traces. In this experiment, the DC capacitor voltages maintained stable values without active control. The new matrix converter was shown to be capable of both increasing and decreasing the AC voltage magnitude.

5.4 FUTURE WORK

Recommended future work includes:

- Improving gate drive circuitry, so that full-power operation can be demonstrated and efficiency can be measured.
- Demonstrating three-level operation at low speed in the laboratory. This would require developing new control algorithms for three-level operation and for regulation of the individual capacitor voltages.
- Configuring the device as a wind generator by connecting the converter between a variable-voltage variable-frequency AC machine and the utility.
- Increasing the number of switch modules to demonstrate the feasibility of scaling the proposed new converter to higher voltage and power levels. This would involve extending the control algorithms, constructing additional power stage and control elements, and testing and measuring performance.

6.0

References

- Alesina, A.; Venturini, M. (January 1989). "Analysis and Design of Optimum Amplitude Nine-Switch Direct AC–AC Converters." *IEEE Transactions on Power Electronics* (Vol 4:No 1); Institute of Electrical and Electronic Engineers; pp. 101-112.
- Al-Naseem, O.A. (April 2001). *Modeling and Space Vector Control of a Novel Multilevel Matrix Converter for Variable-Speed Wind Power Generators*. Ph.D. Thesis. Boulder, CO: University of Colorado.
- Al-Naseem, O.; Erickson, R.; Carlin, P. (February 2000). "Prediction of Switching Loss Variations by Averaged Switch Modeling." *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*; Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA; pp. 242–248.
- Bernet, S.; Teichmann, R. (1997). "The Auxiliary Resonant Commutated Pole Matrix Converter for DC Applications." Presented at the *Twenty-eighth Annual IEEE Power Electronics Specialists Conference, Part 2 of 2*, PESC Record – Institute of Electrical and Electronic Engineers Annual Power Electronics Specialists Conference, St. Louis, CA, USA, June 23-26, 1997; pp. 1225-1231.
- Bhagwat, P.; Stefanovic, V. (November–December 1983). "Generalized Structure of a Multilevel PWM Inverter." *Proceedings IEEE Transactions on Industry Applications*, Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA (IA-19:6); pp. 1057–1069.
- Busse, D.; Erdman, J.; Kerkman, R.; Schlegel, D.; Skibinski, G. (March–April 1997). "System Electrical Parameters and Their Effects on Bearing Currents." *Proceedings IEEE Transactions on Industry Applications* (33); Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA; pp. 577–584.
- Cengelci, E.; Enjeti, P.; Singh, C.; Blaabjerg, F.; Pederson, J. "New Medium-Voltage PWM Inverter Topologies for Adjustable-Speed AC Motor Drive Systems." *Proceedings IEEE Applied Power Electronics Conference (APEC'98)*; Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA; pp. 565–571.
- Erickson, R.; Al-Naseem, O. (November 2001). "A New Family of Matrix Converters," *IEEE Industrial Electronics Society Annual Conference (IECON '01)*, IECON Proceedings (Industrial Electronics Conference), 27th Annual Conference of the IEEE Industrial Electronics Society, v2, Nov.29-Dec.2 2001, Denver, CO.
- Erickson, R.; Al-Naseem, O.; Changtong, K. (1999). *Energy Efficiency Analysis of Wind Turbine Electric Generators and Electric Components, Final Report*. NREL Contract No. XCX-8-17222-01. Golden, CO: NREL.
- Erickson, R.; Maksimovic, D. (2001). *Fundamentals of Power Electronics*, Second Edition, Kluwer Academic Publishers, Dordrecht, The Netherlands, p. 576.

Erickson, R.; Al-Naseem, O.; Fingersh, L. (5/30/03). *Variable-Speed Wind Power System with Improved Energy Capture via Multilevel Conversion*. Patent disclosure.

Erickson, R.; Al-Naseem, O. (5/30/03). *Multilevel Matrix Converter*. Patent disclosure.

Fingersh, L.J.; Robinson, M. (January 1997). "Effects of Variable Speed and Drive Train Component Efficiencies on Wind Turbine Energy Capture." *Proceedings ASME Wind Energy Symposium*; Jointly published by the AME and American Institute of Aeronautics and Astronautics (AIAA), Reno, NV; pp. 264–270.

Huber, L.; Borojevic, D.; Burany, N. (1989). "Voltage Space Vector Based PWM Control of Forced Commutated Cycloconverters." *Proceedings IEEE Industrial Electronics Society Annual Conference (IECON '89)*; 15th Annual Conference of IEEE Industrial Electronics Society – IECON '89, Part 1, Nov. 6-10 1989, Philadelphia, PA, USA, Institute of Electrical and Electronic Engineers, Los Alamitos, CA, USA; pp. 106–111.

Huber, L.; Borojevic, D. (November–December 1995). "Space Vector Modulated Three-Phase to Three-Phase Matrix Converter with Input Power Factor Correction." *Proceedings IEEE Transactions on Industry Applications* (31:6); Nov. – Dec. 1995, IEEE Transactions of Industry Applications, Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA; pp. 1234-1246.

Kassakian, J.; Schlecht, M.; Vergese, G. (1991). *Principles of Power Electronics*. Boston, MA: Addison-Wesley.

Lin, B.; Chien, Y.; Lu, H. (July 1999). "Multilevel Inverter with Series Connection of H-Bridge Cells," *Proceedings IEEE International Conference on Power Electronics and Drive Systems (PEDS'99)*; Proceedings of the 1999 3rd IEEE International Conference on Power Electronics and Drive Systems (PEDS'99), July 27-29, 1999, Kowloon, Hong Kong, Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA; pp. 859–864.

Maksimovic, D.; Erickson, R. (1995). "Universal-Input High-Power-Factor Boost Doubler Rectifiers." *Proceedings IEEE Applied Power Electronics Conference; Conference Proceedings – IEEE Applied Power Electronics Conference and Exposition – APEC*; Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA, March 5-9, 1995; pp. 459–465.

Manjrekar, M.; Lipo, T. (February 1998). "A Hybrid Multilevel Inverter Topology for Drive Applications." *Proceedings IEEE Applied Power Electronics Conference (APEC'98)*; Proceedings of the 1998 13th Annual Applied Power Electronics and Exposition, APEC'98 Part 2 of 2, Feb. 15-19, 1998, Anaheim, CA, USA, Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA, pp. 523–529.

Mefti, M.; Sung, J.; Bell, S.; Skibinski, G. (October 1997). "Effect of Surge Voltage Risettime on the Insulation of Low Voltage Machines Fed by PWM Converters." *Proceedings Industry Applications Society Annual Meeting*; IAS Annual Meeting (IEEE Industry Applications Society), v1, 1997, Proceedings of the 1997 IEEE Industry Applications Conference 32nd IAS Annual Meeting, Part 1 of 3, Oct. 5-9, 1997, New Orleans, LA, USA. Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA, pp. 239–246.

Mefti, M.; Sung, J.; Bell, S.; Skibinski, G. (November 1998). "Impact of IGBT/PWM Drive on Low Voltage Motor Windings—Part 2: Test Results." *Power Conversion and Intelligent Motion*; pp. 30–42.

Nabae, A.; Takahashi, I.; Akagi, H. (September–October 1981). “A New Neutral-Point Clamped PWM Inverter.” *IEEE Trans. Industry Applications* (IA-17:5); pp. 518–523.

Oyama, J.; Higuchi, T.; Yamada, E.; Lipo, T. (1989). “New Control Strategy for Matrix Converter.” *Proceedings IEEE Power Electronics Specialists Conference*; Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA; pp. 360–367.

Peng, F.Z.; Lai, J.S. (1995). “A Multilevel Voltage-Source Inverter with Separate DC Sources.” *Proceedings IEEE Industry Applications Society Annual Meeting*; Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA; pp. 2541–2548.

Rendusara, D.; Enjeti, P. (November 1998). “An Improved Inverter Output Filter Configuration Reduces Common and Differential Modes dv/dt at the Motor Terminals in PWM Drive Systems.” *Proceedings IEEE Transactions on Power Electronics* (13:6); Institute of Electrical and Electronic Engineers, Piscataway, NJ, USA; pp. 1135–1143.

Tolbert, L.; Peng, F. (February 1998). “Multilevel Converters for Large Electric Drives,” *Proceedings IEEE Applied Power Electronics Conference (APEC’98)*; Electrical and Electronic Engineers, Piscataway, NJ, USA; pp. 530–536.

Tolbert, L.; Peng, F.; Habetler, T. (July 2000). “Multilevel PWM Methods at Low Modulation Indices.” *Proceedings IEEE Transactions on Power Electronics* (15:4); Electrical and Electronic Engineers, Piscataway, NJ, USA; pp. 719–725.

Wolaver, D. (January 1969). *Fundamental Study of DC to DC Conversion Systems*. Ph.D. thesis. Boston, MA: Massachusetts Institute of Technology.

APPENDIX A

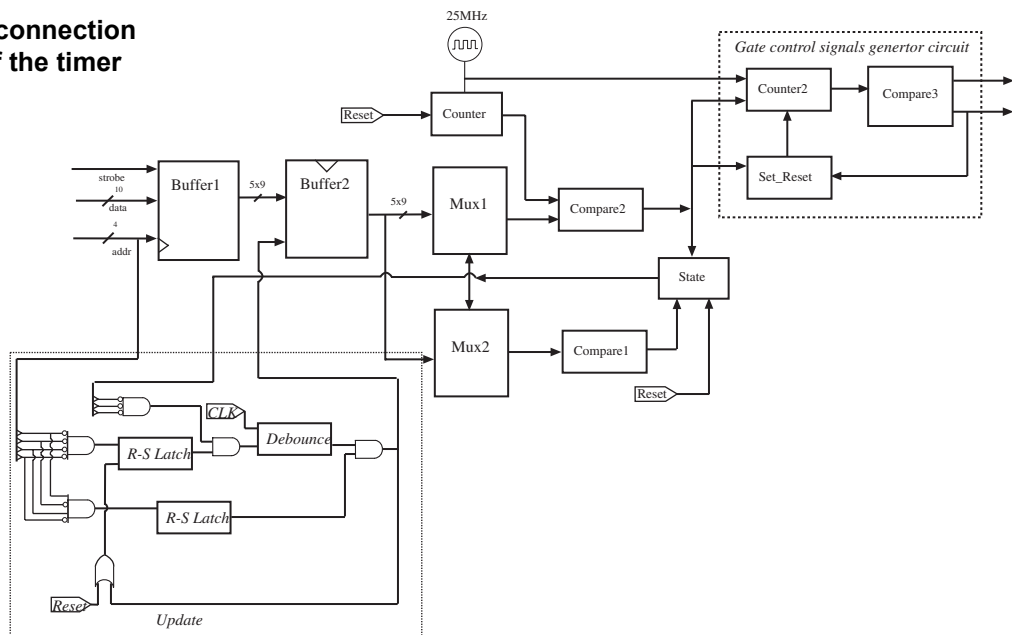
CPLD PROGRAMMING

This appendix documents the details of the programming of the CPLDs. The Xilinx CPLDs were designed using the Xilinx ISE development system. Individual logical blocks were specified via the Verilog hardware description language. High-level connections between blocks were made using the ISE schematic editor. Chapter 4 gives a high-level description of the timer CPLD, the data buffer CPLD, and the switch cell control CPLD, and the details are described here.

A.1 TIMER CPLD

This CPLD receives asynchronous duty-cycle data from the microcontroller, and controls the timing of the switching frequency and duty cycles. It also implements the turn-on and turn-off delays that ensure nonoverlapping conduction of the IGBTs. The logical blocks of the timer CPLD and their interconnections are diagrammed in Figure A-1.

Figure A-1. Interconnection of the blocks of the timer CPLD



A.1.1 Buffer1

Buffer1 is a register composed of D-type flip-flops, whose function is to receive and store data transmitted by the microcontroller. This block is also able to alter the data, as necessary to eliminate the narrow pulse width problem of the gate driver circuitry. Buffers 1 and 2 implement asynchronous handshaking between the microcontroller and the CPLD, allowing the switching frequency to be independent of the microcontroller update rate.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```
module buffer1(read,data,sel,T0_i,T1_i,T2_i,T3_i,T4_i);
    input read;
    input [9:0] data;
    input [3:0] sel;
    output [8:0] T0_i,T1_i,T2_i,T3_i,T4_i;
    reg [8:0] T0_i,T1_i,T2_i,T3_i,T4_i;

always @(posedge read)
begin
    case(sel)
        4'b0110 :begin
            if (data[8:0] <=15)
                T1_i <= 0;
            else if (data[8:0] > 15 && data[8:0] < 30)
                T1_i <= 30;
            else
                T1_i <= data[8:0];
        end
        4'b0111 :begin
            if (data[8:0] <=15)
                T2_i <= 0;
            else if (data[8:0] > 15 && data[8:0] < 30)
                T2_i <= 30;
            else
                T2_i <= data[8:0];
        end
        4'b1000 :begin
            if (data[8:0] <=15)
                T3_i <= 0;
            else if (data[8:0] > 15 && data[8:0] < 30)
                T3_i <= 30;
            else
                T3_i <= data[8:0];
        end
        4'b1001 :begin
            if (data[8:0] <=15)
```

```

        T4_i <= 0;
    else if (data[8:0] > 15 && data[8:0] < 30)
        T4_i <= 30;
    else
        T4_i <= data[8:0];
    end
4'b1010 :begin
    if (data[8:0] <=15)
        T0_i <= 0;
    else if (data[8:0] > 15 && data[8:0] < 30)
        T0_i <= 30;
    else
        T0_i <= data[8:0];
    end
endcase
end
endmodule

```

A.1.2 Buffer2

The Buffer2 registers latch the data previously received by Buffer1 from the microcontroller. The data in Buffer2 are used by the remainder of the timer CPLD; these data can change only at the conclusion of a switching period, and are guaranteed to be consistent and valid during each complete switching period.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```

module buffer2(update,T0_i,T1_i,T2_i,T3_i,T4_i,T0,T1,T2,T3,T4);
    input update;
    input[8:0] T0_i,T1_i,T2_i,T3_i,T4_i;
    output[8:0]T0,T1,T2,T3,T4;
    reg[8:0] T0,T1,T2,T3,T4;

    always @(posedge update)
    begin
        T0 <= T0_i;
        T1 <= T1_i;
        T2 <= T2_i;
        T3 <= T3_i;
        T4 <= T4_i;
    end
endmodule

```


A.1.3 Mux1

Mux1 is a logical multiplexer that supplies the number of ticks in the current subinterval. It selects the timer output data of Buffer2 based on the current state (i.e., based on the subinterval number).

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```
module mux1(state,T0,T1,T2,T3,T4,ref);
    input[2:0] state;
    input[8:0] T0,T1,T2,T3,T4;
    output[8:0] ref;
    reg[8:0] ref;

    always @(state or T0 or T1 or T2 or T3 or T4)
    begin
        case(state)
            3'b000: ref = T0;
            3'b001: ref = T1;
            3'b010: ref = T2;
            3'b011: ref = T3;
            3'b100: ref = T4;
            3'b101: ref = 0;
            3'b110: ref = 0;
            3'b111: ref = 0;
        endcase
    end
endmodule
```

A.1.4 Mux2

Mux2 is a multiplexer that functions in a manner similar to Mux1. However, its output data corresponds to the next state.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```
module mux2(state,T0,T1,T2,T3,T4,next_ref);
    input[2:0] state;
    input[8:0] T0,T1,T2,T3,T4;
    output[8:0] next_ref;
    reg[8:0] next_ref;

    always @(state or T0 or T1 or T2 or T3 or T4)
    begin
        case(state)
```

```

        3'b000: next_ref = T1;
        3'b001: next_ref = T2;
        3'b010: next_ref = T3;
        3'b011: next_ref = T4;
        3'b100: next_ref = T0;
        3'b101: next_ref = 0;
        3'b110: next_ref = 0;
        3'b111: next_ref = 0;
    endcase
end
endmodule

```

A.1.5 Compare1

This logical block compares the data from Mux2 to the minimum pulse width, limited by the gate driver circuit. If the next subinterval length is less than minimum pulse width, the timer circuit skips the next subinterval.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```

module compare1(next_ref,zero);
    input[8:0] next_ref;
    output zero;
    reg zero;

    always @(next_ref)
    begin
        if(next_ref <= 15)
            zero = 1;
        else
            zero = 0;
    end
endmodule

```

A.1.6 Compare2

The logical block Compare2 takes the data from Mux1 and compares it with the counter output. The output of this block triggers termination of the current subinterval.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```

module compare2(ref,count,count_done);
    input[8:0] count,ref;

```

```

        output count_done;
        reg count_done;

always @(count or ref )
begin
    if(count == ref)
        count_done = 1;
    else
        #10 count_done = 0;
end
endmodule

```

A.1.7 Counter

This logical block is a basic nine-bit counter circuit, which counts down each subinterval. This counter is clocked by the external 25-MHz clock signal.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```

module counter(RESET,CLK,count);
    input RESET,CLK;
    output[8:0] count;
    reg[8:0] count;

always @(posedge RESET or posedge CLK)
begin
    if(RESET == 1)
        count = 0;
    else
        count = count + 1;
end
endmodule

```

A.1.8 State

This module is a state machine that keeps track of the subinterval number.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```

module state(change,skip,RESET,state);
    input change,skip,RESET;
    output [2:0] state;
    reg[2:0] state;

```

```

always @(posedge change or posedge RESET)
begin
    if (RESET == 1)
        state = 3'b000;
    else
        begin
            if(skip == 1)
                case(state)
                3'b000: state = 3'b010;
                3'b001: state = 3'b011;
                3'b010: state = 3'b100;
                default: state = 0;
                endcase
            else
                case(state)
                3'b000: state = 3'b001;
                3'b001: state = 3'b010;
                3'b010: state = 3'b011;
                3'b011: state = 3'b100;
                default: state = 0;
                endcase
            end
        end
end
endmodule

```

A.1.9 Gate Control Signal Generator with Dead Time Control

This logical block is a set of modules for generating turn-on and turn-off gate driver signals.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```

module counter2(ch,CLK,enable,count);
    input ch,CLK,enable;
    output[3:0] count;
    reg[3:0] count;

    always @(posedge ch or posedge CLK)
    begin
        if(ch == 1)
            count = 0;
        else
            if(enable)
                count = count + 1;
    end
end

```

```

endmodule

module compare3(count,turn_off,turn_on);
    input[3:0] count;
    output turn_off,turn_on;
    reg turn_off,turn_on;

always @(count)
begin
    if(count == 5)
        turn_off = 1;
    else
        turn_off = 0;
    if(count == 10)
        turn_on = 1;
    else
        turn_on = 0;
end
endmodule

```

```

module set_reset(SET,RESET,ENABLE);
    input SET,RESET;
    output ENABLE;
    reg ENABLE;

always @(posedge SET or negedge RESET)
begin
    if (SET == 1)
        ENABLE = 1;
    else
        ENABLE =0;
end
endmodule

```

A.1.10 Update

This logical block controls the handshaking between the asynchronous microcontroller and the CPLDs. Specifically, it allows the data to be transferred from Buffer1 to Buffer2 only at the end of a switching period, so that the timer circuit uses the same set of data for one complete switching period. Without this block, the duty cycles can change in the middle of a switching period, resulting in glitches in the power wave forms.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```

module debounce(D_in,RESET,CLK,Q_out);
    input D_in;
    input RESET;
    input CLK;
    output Q_out;
    reg q1, q2, q3;

always @(posedge CLK or posedge RESET)
if (RESET == 1)
begin
q1 <= 1'b0; q2 <= 1'b0; q3 <= 1'b0;
end
else
begin
q1 <= D_in; q2 <= q1; q3 <= q2;
end

assign Q_out = q1 & q2 & !q3;

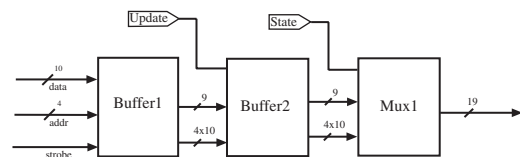
endmodule

```

A.2 DATA BUFFER CPLD

The data buffer CPLD receives asynchronous space vector and capacitor data from the microcontroller. It supplies the stored data for the current subinterval to the inputs of the flash memory. This circuitry operates in a manner similar to the corresponding blocks of the timer CPLD. The logical blocks of the data buffer CPLD are illustrated in Figure A-2.

Figure A-2. Interconnection of the blocks of the data buffer CPLD



A.2.1 Buffer1

Buffer1 is composed of sets of D-type flip-flop that receive data from the microcontroller.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```

module buffer1(read,data,sel,Cap_i,C1_i,C2_i,C3_i,C4_i); //C0_i = 10'b0 by default
    input read;
    input [9:0] data;
    input [3:0] sel;
    output [8:0] Cap_i;

```

```

        output [9:0] C1_i,C2_i,C3_i,C4_i;
        reg [8:0] Cap_i;
        reg [9:0] C1_i,C2_i,C3_i,C4_i;

always @(posedge read)
begin
    case(sel)
        4'b0001 :Cap_i <= data[8:0];
        4'b0010 :C1_i <= data;
        4'b0011 :C2_i <= data;
        4'b0100 :C3_i <= data;
        4'b0101 :C4_i <= data;
    endcase
end
endmodule

```

A.2.2 Buffer2

Buffer2 contains sets of registers that hold the space vector and capacitor data for all of the switching subintervals. It uses the “update” signal from the timer CPLD to initialize data transfer from Buffer1.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```

module buffer2(update,Cap_i,C1_i,C2_i,C3_i,C4_i,Cap,C1,C2,C3,C4); //C0_i = 10'b0 by default
    input update;
    input [8:0] Cap_i;
    input [9:0] C1_i,C2_i,C3_i,C4_i;
    output [8:0] Cap;
    output [9:0] C1,C2,C3,C4;
    reg [8:0] Cap;
    reg [9:0] C1,C2,C3,C4;

always @(posedge update)
begin
    Cap <= Cap_i;
    C1 <= C1_i;
    C2 <= C2_i;
    C3 <= C3_i;
    C4 <= C4_i;
end
endmodule

```

A.2.3 Mux1

Mux1 is a logical multiplexer that supplies the space vectors and capacitor(s) for the current subinterval. It selects the output data of Buffer 2 based on the current state (i.e., based on the subinterval number supplied by the timer CPLD).

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)

```
module main2(state,Cap,C1,C2,C3,C4,d_out);
    input[2:0] state;
    input[8:0] Cap;
    input[9:0] C1,C2,C3,C4;
    output[18:0] d_out;
    reg[18:0] d_out;

    always @(state or Cap or C1 or C2 or C3 or C4)
    begin
        case(state)
            3'b000: d_out <= {10'b0,Cap};
            3'b001: d_out <= {C1,Cap};
            3'b010: d_out <= {C2,Cap};
            3'b011: d_out <= {C3,Cap};
            3'b100: d_out <= {C4,Cap};
            3'b101: d_out <= 19'b1111111111111111111;
            3'b110: d_out <= 19'b1111111111111111111;
            3'b111: d_out <= 19'b1111111111111111111;
        endcase
    end
endmodule
```

A.3 SWITCH DECODER CPLD

Details of this CPLD are illustrated in Figure 4-13. The svm_decoder logical cell was generated using Verilog, and is documented below. The remainder of the circuitry was specified using the ISE schematic editor, and is documented in Figure 4-13. In our prototype, there are three switch cells per circuit board, so each physical-switch-decoded CPLD contains the circuitry of Figure 4-13 replicated three times.

A.3.1 Svm_decoder

This logical block decodes the two-bit data output from flash memory into the states of the four IGBTs of a switch network.

- HARDWARE DESCRIPTION LANGUAGE (VERILOG)


```
module sw_decoder(D_in,L,D_out);
    input L;
    input[1:0] D_in;
    output[3:0] D_out;
    reg[3:0] D_out;

    always @(D_in or L)
    begin
        casex({D_in,L})
            3'b00x: D_out <= 4'b0000;
            3'b01x: D_out <= 4'b1001;
            3'b10x: D_out <= 4'b0110;
            3'b110: D_out <= 4'b0011;
            3'b111: D_out <= 4'b1100;
            default: D_out <= 4'b0;
        endcase
    end
endmodule
```

APPENDIX B

FLASH MEMORY TABLE

This appendix documents the details of the flash memory table. This table is the heart of the control algorithm. It accepts inputs that denote the input and output space vectors, and the capacitor(s) to be used, and produces outputs specifying the switch states of the nine switch networks. The table entries described in this appendix implement the two-level single-capacitor control scheme we described in the body of the report. However, the architecture is able to handle three-level control that employs multiple capacitors per switching period, so that future control algorithms can be accommodated by simply reprogramming the flash memory. A high-level description of the current programming is given in Chapter 4, and the details are described here.

The lookup table receives data from the data buffer CPLD. The input data are 19 bits wide, with the bits defined as illustrated in Figure B-1.

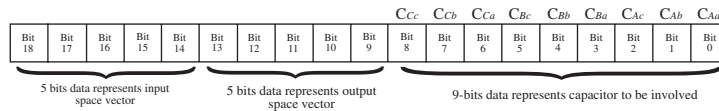


Figure B-1. Assignment of bits in input (address lines) words to flash memory

Each 19-bit word is divided into three groups: the input-side space vector, the output-side space vector, and the choice of capacitor(s). Given these three data groups, the lookup table outputs the switch state for each of the nine switch cells.

The groups representing the input-side and output-side space vectors each use 5 bits of data to represent all possible 19 space vectors, numbered from 0 to 18, in the basic nine-switch-network configuration for the converter. In the current prototype, the lookup table memory chips include data that represent space vectors 0 through 6, for two-level modulation. For any space vector that exceeds this range, the corresponding outputs are all programmed at “00,” which causes all IGBTs to be turned off.

The last 9 bits of data specify which capacitor is employed in the current subinterval. Each capacitor is represented by 1 bit, in the order defined in Figure B-1. The bit is asserted to “1” when the corresponding capacitor is connected through conducting switches to the remainder of the converter. In the current version of the control algorithm, in which only one capacitor is employed during each switching period, only 1 of 9 bits can be “1”. Setting more than one capacitor bit to “1” causes the table to output all zeroes.

For a given combination of input space vector and output space vector, not all 9 capacitors can be employed. This means that any combination that includes an invalid choice of capacitor is also programmed to turn off all IGBTs.

The state of each switch cell is represented by 2 bits of data. In the prototype, we used three 512-kB flash memory chips. Each chip has data for three switch cells connected to the same input phase. Thus, each chip uses 19 bits of input data from the data buffer CPLD as the memory address lines, and gives 6 bits of output data for 3 switch cells.

The complete lookup table comprises the rest of this appendix.

Address (hex)	Input SV	Output SV	Capacitor	S_{Cc}	S_{Cb}	S_{Ca}	S_{Bc}	S_{Bb}	S_{Ba}	S_{Ac}	S_{Ab}	S_{Aa}
0x00001	00000	00000	000000001	11	11	11	11	11	11	11	11	11
0x00002	00000	00000	000000010	11	11	11	11	11	11	11	11	11
0x00004	00000	00000	000000100	11	11	11	11	11	11	11	11	11
0x00008	00000	00000	000001000	11	11	11	11	11	11	11	11	11
0x00010	00000	00000	000010000	11	11	11	11	11	11	11	11	11
0x00020	00000	00000	000100000	11	11	11	11	11	11	11	11	11
0x00040	00000	00000	001000000	11	11	11	11	11	11	11	11	11
0x00080	00000	00000	010000000	11	11	11	11	11	11	11	11	11
0x00100	00000	00000	100000000	11	11	11	11	11	11	11	11	11
0x00201	00000	00001	000000001	11	11	00	11	11	00	11	11	10
0x00208	00000	00001	000001000	11	11	00	11	11	10	11	11	00
0x00240	00000	00001	001000000	11	11	10	11	11	00	11	11	00
0x00404	00000	00010	000000100	00	11	11	00	11	11	01	11	11
0x00420	00000	00010	000100000	00	11	11	01	11	11	00	11	11
0x00500	00000	00010	100000000	01	11	11	00	11	11	00	11	11
0x00602	00000	00011	000000010	11	00	11	11	00	11	11	10	11
0x00610	00000	00011	000010000	11	00	11	11	10	11	11	00	11
0x00680	00000	00011	010000000	11	10	11	11	00	11	11	00	11
0x00801	00000	00100	000000001	11	11	00	11	11	00	11	11	01
0x00808	00000	00100	000001000	11	11	00	11	11	01	11	11	00
0x00840	00000	00100	001000000	11	11	01	11	11	00	11	11	00
0x00A04	00000	00101	000000100	00	11	11	00	11	11	10	11	11
0x00A20	00000	00101	000100000	00	11	11	10	11	11	00	11	11
0x00B00	00000	00101	100000000	10	11	11	00	11	11	00	11	11
0x00C02	00000	00110	000000010	11	00	11	11	00	11	11	01	11
0x00C10	00000	00110	000010000	11	00	11	11	01	11	11	00	11
0x00C80	00000	00110	010000000	11	01	11	11	00	11	11	00	11
0x04001	00001	00000	000000001	11	11	11	11	11	11	00	00	01
0x04002	00001	00000	000000010	11	11	11	11	11	11	00	01	00
0x04004	00001	00000	000000100	11	11	11	11	11	11	01	00	00
0x04202	00001	00001	000000010	11	11	00	11	11	00	00	01	11
0x04204	00001	00001	000000100	11	11	00	11	11	00	01	00	11
0x04208	00001	00001	000001000	11	11	00	11	11	10	00	00	11
0x04240	00001	00001	001000000	11	11	10	11	11	00	00	00	11
0x04404	00001	00010	000000100	11	00	00	11	00	00	01	11	11
0x04408	00001	00010	000001000	11	00	00	11	00	10	00	11	11
0x04410	00001	00010	000010000	11	00	00	11	10	00	00	11	11
0x04440	00001	00010	001000000	11	00	10	11	00	00	00	11	11
0x04480	00001	00010	010000000	11	10	00	11	00	00	00	11	11
0x04601	00001	00011	000000001	11	00	11	11	00	11	00	11	01
0x04604	00001	00011	000000100	11	00	11	11	00	11	01	11	00
0x04610	00001	00011	000010000	11	00	11	11	10	11	00	11	00
0x04680	00001	00011	010000000	11	10	11	11	00	11	00	11	00
0x04801	00001	00100	000000001	00	00	11	00	00	11	11	11	01
0x04810	00001	00100	000010000	00	00	11	00	10	11	11	11	00

0x04820	00001	00100	000100000	00	00	11	10	00	11	11	11	00
0x04880	00001	00100	010000000	00	10	11	00	00	11	11	11	00
0x04900	00001	00100	100000000	10	00	11	00	00	11	11	11	00
0x04A01	00001	00101	000000001	00	11	11	00	11	11	11	00	01
0x04A02	00001	00101	000000010	00	11	11	00	11	11	11	01	00
0x04A20	00001	00101	000100000	00	11	11	10	11	11	11	00	00
0x04B00	00001	00101	100000000	10	11	11	00	11	11	11	00	00
0x04C02	00001	00110	000000010	00	11	00	00	11	00	11	01	11
0x04C08	00001	00110	000001000	00	11	00	00	11	10	11	00	11
0x04C20	00001	00110	000100000	00	11	00	10	11	00	11	00	11
0x04C40	00001	00110	001000000	00	11	10	00	11	00	11	00	11
0x04D00	00001	00110	100000000	10	11	00	00	11	00	11	00	11
0x08040	00010	00000	001000000	00	00	10	11	11	11	11	11	11
0x08080	00010	00000	010000000	00	10	00	11	11	11	11	11	11
0x08100	00010	00000	100000000	10	00	00	11	11	11	11	11	11
0x08202	00010	00001	000000010	11	11	00	00	00	11	00	01	11
0x08204	00010	00001	000000100	11	11	00	00	00	11	01	00	11
0x08210	00010	00001	000010000	11	11	00	00	01	11	00	00	11
0x08220	00010	00001	000100000	11	11	00	01	00	11	00	00	11
0x08240	00010	00001	001000000	11	11	10	00	00	11	00	00	11
0x08404	00010	00010	000000100	11	00	00	00	11	11	01	11	11
0x08420	00010	00010	000100000	11	00	00	01	11	11	00	11	11
0x08440	00010	00010	001000000	11	00	10	00	11	11	00	11	11
0x08480	00010	00010	010000000	11	10	00	00	11	11	00	11	11
0x08601	00010	00011	000000001	11	00	11	00	11	00	00	11	01
0x08604	00010	00011	000000100	11	00	11	00	11	00	01	11	00
0x08608	00010	00011	000001000	11	00	11	00	11	01	00	11	00
0x08620	00010	00011	000100000	11	00	11	01	11	00	00	11	00
0x08680	00010	00011	010000000	11	10	11	00	11	00	00	11	00
0x08801	00010	00100	000000001	00	00	11	11	11	00	11	11	01
0x08808	00010	00100	000001000	00	00	11	11	11	01	11	11	00
0x08880	00010	00100	010000000	00	10	11	11	11	00	11	11	00
0x08900	00010	00100	100000000	10	00	11	11	11	00	11	11	00
0x08A01	00010	00101	000000001	00	11	11	11	00	00	11	00	01
0x08A02	00010	00101	000000010	00	11	11	11	00	00	11	01	00
0x08A08	00010	00101	000001000	00	11	11	11	00	01	11	00	00
0x08A10	00010	00101	000010000	00	11	11	11	01	00	11	00	00
0x08B00	00010	00101	100000000	10	11	11	11	00	00	11	00	00
0x08C02	00010	00110	000000010	00	11	00	11	00	11	11	01	11
0x08C10	00010	00110	000010000	00	11	00	11	01	11	11	00	11
0x08C40	00010	00110	001000000	00	11	10	11	00	11	11	00	11
0x08D00	00010	00110	100000000	10	11	00	11	00	11	11	00	11
0x0C008	00011	00000	000001000	11	11	11	00	00	01	11	11	11
0x0C010	00011	00000	000010000	11	11	11	00	01	00	11	11	11
0x0C020	00011	00000	000100000	11	11	11	01	00	00	11	11	11
0x0C201	00011	00001	000000001	11	11	00	00	00	11	11	11	10
0x0C210	00011	00001	000010000	11	11	00	00	01	11	11	11	00

0x0C220	00011	00001	000100000	11	11	00	01	00	11	11	11	00
0x0C240	00011	00001	001000000	11	11	10	00	00	11	11	11	00
0x0C401	00011	00010	000000001	11	00	00	00	11	11	11	00	10
0x0C402	00011	00010	000000010	11	00	00	00	11	11	11	10	00
0x0C420	00011	00010	000100000	11	00	00	01	11	11	11	00	00
0x0C440	00011	00010	001000000	11	00	10	00	11	11	11	00	00
0x0C480	00011	00010	010000000	11	10	00	00	11	11	11	00	00
0x0C602	00011	00011	000000010	11	00	11	00	11	00	11	10	11
0x0C608	00011	00011	000001000	11	00	11	00	11	01	11	00	11
0x0C620	00011	00011	000100000	11	00	11	01	11	00	11	00	11
0x0C680	00011	00011	010000000	11	10	11	00	11	00	11	00	11
0x0C802	00011	00100	000000010	00	00	11	11	11	00	00	10	11
0x0C804	00011	00100	000000100	00	00	11	11	11	00	10	00	11
0x0C808	00011	00100	000001000	00	00	11	11	11	01	00	00	11
0x0C880	00011	00100	010000000	00	10	11	11	11	00	00	00	11
0x0C900	00011	00100	100000000	10	00	11	11	11	00	00	00	11
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0x0CD00	00011	00110	100000000	10	11	00	11	00	11	00	11	00
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0x10280	00100	00001	010000000	00	01	11	00	00	11	11	11	00
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0x10500	00100	00010	100000000	01	11	11	00	11	11	11	00	00
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0x14201	00101	00001	000000001	00	00	11	11	11	00	11	11	10
0x14208	00101	00001	000001000	00	00	11	11	11	10	11	11	00
0x14280	00101	00001	010000000	00	01	11	11	11	00	11	11	00
0x14300	00101	00001	100000000	01	00	11	11	11	00	11	11	00
0x14401	00101	00010	000000001	00	11	11	11	00	00	11	00	10
0x14402	00101	00010	000000010	00	11	11	11	00	00	11	10	00
0x14408	00101	00010	000001000	00	11	11	11	00	10	11	00	00
0x14410	00101	00010	000010000	00	11	11	11	10	00	11	00	00
0x14500	00101	00010	100000000	01	11	11	11	00	00	11	00	00
0x14602	00101	00011	000000010	00	11	00	11	00	11	11	10	11
0x14610	00101	00011	000010000	00	11	00	11	10	11	11	00	11
0x14640	00101	00011	001000000	00	11	01	11	00	11	11	00	11
0x14700	00101	00011	100000000	01	11	00	11	00	11	11	00	11
0x14802	00101	00100	000000010	11	11	00	00	00	11	00	10	11
0x14804	00101	00100	000000100	11	11	00	00	00	11	10	00	11
0x14810	00101	00100	000010000	11	11	00	00	10	11	00	00	11
0x14820	00101	00100	000100000	11	11	00	10	00	11	00	00	11
0x14840	00101	00100	001000000	11	11	01	00	00	11	00	00	11
0x14A04	00101	00101	000000100	11	00	00	00	11	11	10	11	11
0x14A20	00101	00101	000100000	11	00	00	10	11	11	00	11	11
0x14A40	00101	00101	001000000	11	00	01	00	11	11	00	11	11
0x14A80	00101	00101	010000000	11	01	00	00	11	11	00	11	11
0x14C01	00101	00110	000000001	11	00	11	00	11	00	00	11	10
0x14C04	00101	00110	000000100	11	00	11	00	11	00	10	11	00
0x14C08	00101	00110	000001000	11	00	11	00	11	10	00	11	00
0x14C20	00101	00110	000100000	11	00	11	10	11	00	00	11	00
0x14C80	00101	00110	010000000	11	01	11	00	11	00	00	11	00
0x18008	00110	00000	000001000	11	11	11	00	00	10	11	11	11
0x18010	00110	00000	000010000	11	11	11	00	10	00	11	11	11
0x18020	00110	00000	000100000	11	11	11	10	00	00	11	11	11
0x18202	00110	00001	000000010	00	00	11	11	11	00	00	01	11
0x18204	00110	00001	000000100	00	00	11	11	11	00	01	00	11
0x18208	00110	00001	000001000	00	00	11	11	11	10	00	00	11
0x18280	00110	00001	010000000	00	01	11	11	11	00	00	00	11
0x18300	00110	00001	100000000	01	00	11	11	11	00	00	00	11
0x18404	00110	00010	000000100	00	11	11	11	00	00	01	11	11

0x18408	00110	00010	000001000	00	11	11	11	00	10	00	11	11
0x18410	00110	00010	000010000	00	11	11	11	10	00	00	11	11
0x18500	00110	00010	100000000	01	11	11	11	00	00	00	11	11
0x18601	00110	00011	000000001	00	11	00	11	00	11	00	11	01
0x18604	00110	00011	000000100	00	11	00	11	00	11	01	11	00
0x18610	00110	00011	000010000	00	11	00	11	10	11	00	11	00
0x18640	00110	00011	001000000	00	11	01	11	00	11	00	11	00
0x18700	00110	00011	100000000	01	11	00	11	00	11	00	11	00
0x18801	00110	00100	000000001	11	11	00	00	00	11	11	11	01
0x18810	00110	00100	000010000	11	11	00	00	10	11	11	11	00
0x18820	00110	00100	000100000	11	11	00	10	00	11	11	11	00
0x18840	00110	00100	001000000	11	11	01	00	00	11	11	11	00
0x18A01	00110	00101	000000001	11	00	00	00	11	11	11	00	01
0x18A02	00110	00101	000000010	11	00	00	00	11	11	11	01	00
0x18A20	00110	00101	000100000	11	00	00	10	11	11	11	00	00
0x18A40	00110	00101	001000000	11	00	01	00	11	11	11	00	00
0x18A80	00110	00101	010000000	11	01	00	00	11	11	11	00	00
0x18C02	00110	00110	000000010	11	00	11	00	11	00	11	01	11
0x18C08	00110	00110	000001000	11	00	11	00	11	10	11	00	11
0x18C20	00110	00110	000100000	11	00	11	10	11	00	11	00	11
0x18C80	00110	00110	010000000	11	01	11	00	11	00	11	00	11

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14. ABSTRACT (Maximum 200 Words) The objective of this work was to develop new approaches to the power electronics of variable-speed wind power systems, with the goal of improving the associated cost of energy. Of particular importance is the converter efficiency at low-wind operating points. Developing converter approaches that maintain high efficiency at partial power, without sacrificing performance at maximum power, is desirable, as is demonstrating an approach that can use emerging power component technologies to attain these performance goals with low projected capital costs. In this report, we show that multilevel conversion is an approach that can meet these performance requirements. In the wind power application, multilevel conversion proves superior to conventional converter technologies because it is callable to high power and higher voltage levels, it extends the range of high converter efficiency to lower wind speeds, and it allows superior low-voltage fast-switching semiconductor devices to be used in high-voltage high-power applications.					
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