August 2003 • NREL/SR-560-34635

Subcontractor Report

DG Power Quality, Protection and Reliability Case Studies Report

GE Corporate Research and Development
Niskayuna, New York

National Renewable Energy Laboratory

1617 Cole Boulevard
Golden, Colorado 80401-3393

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Contract No. DE-AC36-99-GO10337

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NREL Technical Monitor: B. Kroposki

Prepared under Subcontract No. NAD-1-30605-01

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1. Executive Summary

As distributed generation (DG) hardware becomes more reliable and economically feasible, there is a trend to interconnect DG units to the existing utilities to serve different purposes and offer more possibilities to end-users, such as—

- improving availability and reliability of electric power
- peak load shaving
- energy cost savings
- selling power back to utilities or other users
- reactive power compensation
- mitigation of harmonics and voltage sag

However, a wide range of system issues arise when DG units attempt to connect to the electric power system (EPS). Major issues regarding the interconnection of DGs include protection, power quality, and system operation. These issues are barriers that limit the penetration of DGs into the EPS.

Future electric power systems should be versatile and flexible so electric energy can be freely generated, transmitted, distributed, and consumed. This program will develop requirements that support the definition, design, and demonstration of a DG-EPS interconnection interface box that allows DG sources to be interconnected to the EPS in a manner that provides value to the end user without compromising reliability or performance. The first major task of this program is to study the DG-EPS interconnection issues using a GE-designed virtual test bed (VTB). The VTB is a simulation platform suite that includes EPS, DG, and load models. This report summarizes various DG-EPS interconnection cases that were studied by conducting simulations utilizing the VTB. The results from these case studies will enable us to make recommendations for improvement to the IEEE P1547 standard as well as provide inputs to the design of the interconnection interface box.

Some key findings from these initial studies of the impact of DG-EPS interconnect are:

- Widespread penetration of DGs at the load appears to be benign with respect to system response to bulk system disturbances.
- With significant levels of DG penetration, it will be difficult to avoid detraction from EPS voltage regulation performance. While IEEE P1547 presently requires that a DG not cause the EPS voltage to all outside of the prescribed regulation range, achieving this goal may become increasingly difficult using conventional approaches. EPS voltage regulation performance problems due to DG can be mitigated if there is integrated control of system voltage and reactive power management. IEEE P1547 may need to incorporate provisions where the reactive power output of the DG is controlled by the EPS operator.
- Simultaneous tripping of DGs in a system dependent on the DG output can result in widespread and severe voltage problems. Presently, IEEE P1547 is biased in favor of fast tripping in order to rapidly detect and eliminate inadvertent islands. There may need to be further consideration of the fine balance between island avoidance and making the system vulnerable to voltage collapse.
- Anti-islanding schemes (of the type studied in this project) appear to be effective at destabilizing islands containing multiple DGs and loads with relatively complex dynamics while having little impact on system response to bulk system disturbances. This is a highly complex subject, and further investigation is highly desirable.
- Inverter-type DGs will have significant beneficial impact on flicker caused by system loads, only if they have a voltage regulation function or if they have a control scheme where they are operated as controlled voltage sources (i.e., as virtual synchronous generators).
- Modern inverter-based DGs do not contribute to system fault current beyond the pre-fault operating current level. However, the current contribution of the DG system to a single phase fault may be greater than the three phase case which conflicts with IEEE P1547 requirement that ground fault current contribution of a DG shall not be greater than 100% of the fault current contribution of the DG to a three phase fault. This is because the DG is a nearly ideal current source for the positive sequence, but is generally a constant impedance or voltage source for the zero sequence. Both are desirable characteristics, and the result reveals that the wording of IEEE P1547's single-phase to three phase fault current ratio requirement is more appropriate for conventional rotating generators. The wording of this requirement needs additional consideration with respect to its consistency with inverter-based applications.
- Take-aways for future DG designs:
  - Single phase Sandia Anti-islanding scheme can be effectively extended to 3 phase DG

systems;
  - Inverter based DGs will have significant beneficial impact on flicker only if they include a voltage regulation function;
  - Transformer-less DGs should pay special attention to zero-sequence impedance design so an effective ground can be provided.
  - DG voltage regulation functionality may be beneficial in reducing the impact of DG penetration on EPS voltage regulation performance. However, local control may not be sufficient and a system level voltage control approach may be necessary in many applications.
  - DG voltage regulation may reduce the effectiveness of active anti-islanding schemes.
  - Unbalanced grid will cause ripple power and current distortion of the DG, a filter can minimize this effect.
- The GE-designed interconnect interface box will address some of the issues identified above, such as integrated control of system voltage; reactive power management; and communication to a supervisory level to manage microgrid power exchange.

2. Introduction

2.1 OBJECTIVE

The objective of this report is to summarize various DG-EPS interconnection cases that studied the power quality, protection and reliability issues. The GE designed VTB, a simulation platform suite that includes EPS, DG and load models as described in the *Models and Virtual Test Bed* report,[1] was utilized to conduct simulations for the studies.

2.2 TECHNICAL APPROACH

The set of simulations run on the VTB were based on a case list compiled by the team from various brainstorming sessions, IEEE P1547 Draft Standard for interconnecting Distributed Resources with Electric Power Systems, Edison Electric Institute Distributed Resource Task Force Interconnection Study, and literature searches.

The analysis was focused on determining the impact of DGs on power system performance, and the impact of power system events on the operation of DGs. Investigations were designed to test DG behavior on progressively more complex systems. The progression starts with individual DGs, then moves on to multiple DGs embedded in realistic power systems. Finally, impacts of DG on entire bulk power systems are explored. The full range of VTB capability was used in these investigations. Multi-phase, point-on-wave simulations with very detailed representations of DGs were used to investigate local phenomena and to validate large system simulations.

The cases studied are grouped into two categories: power quality case studies and protection and reliability case studies.

The power quality case studies include:

- Voltage regulation
- DG design considerations to meet power quality requirements
  - Harmonics
  - Flicker
  - DC current injection
  - Grounding
  - Unbalanced grid

The protection and reliability case studies include:

- Transient response and fault behaviors
  - Capacitor switching
  - Fault Behaviors
- Reclosing
- Anti-islanding studies
- Power systems dynamics and stability

3. Power Quality Case Studies

A major issue related to interconnection of distributed resources onto the power grid is the potential impacts on the quality of power provided to other customers connected to the grid. Attributes which define power quality include:

- ***Voltage regulation***—The maintenance of the voltage at the point of delivery to each customer within an acceptable range.
- ***Flicker***—The repetitive and rapid changes of voltage, which has the effect of causing unacceptable variations in light output and other effects on power consumers and their equipment.
- ***Voltage imbalance***—The grid voltage does not have identical voltage magnitude on each phase, and a 120° phase separation between each pair of phases.
- ***Harmonic distortion***—The injection of currents having frequency components which are multiples of the fundamental frequency.
- ***Direct current injection***—A situation which can cause saturation and heating of transformers and motors, and can also cause these passive devices to produce unacceptable harmonic currents.

Case studies, using generic models, have been performed to illustrate the potential impacts of distributed generation on these various aspects of power quality. For some of these categories, the studies evaluate the effects as a function of DG penetration, allowing a quantitative understanding of the situations where DG may have a significant impact on power quality. While some of the case studies pertain equally to inverter-based and conventional rotating DG, the primary focus of this investigation is the inverter-based devices.

3.1 VOLTAGE REGULATION

A primary objective of distribution system design is to supply customers at a voltage which is within a prescribed range. The relevant standard, ANSI C84.1, specifies two voltage ranges: Range A, covering normal operation, and a wider Range B for infrequently-occurring circumstances. Many public utility regulatory authorities have codified the ANSI C84.1 requirements, and can impose sanctions on utilities for providing customers with out-or-range voltages.

Normal variations in load, and DG operations, fall into the category covered by Range A. The service voltages for Range A, as specified by ANSI C84.1, are to be between 114 V and 126 V, on a 120 V base (0.95 p.u.–1.05 p.u.). The service voltages are at the customer service entrance. Thus, the lower limit of the primary feeder voltage must be maintained above 95% of nominal to account for transformer and secondary service cable voltage drops under full-load conditions. Generally, this requires that the minimum primary feeder voltage be maintained above at least 98% of nominal.

Distribution system voltage regulation design is based on relatively predictable daily and seasonal changes in loading. In general, loading on the various sections of a feeder follow relatively similar patterns. Without DG, power flow is always unidirectional, and monotonically decreasing in real power (kW) magnitude with increasing distance from the substation. The addition of DG to a system, however, can radically shift power flow patterns and make them unpredictable. Interconnection policies and regulations may allow DG operators to export power into the grid, or cease export, at will. Depending on the spatial relationship of loads and DG, power flow can increase or decrease along a feeder. Net power flow can potentially reverse over a portion of the feeder, or even over the entire feeder if DG production exceeds the load present at that time. These load flow variations can make it difficult to maintain adequate voltage regulation. Also, the unconventional load flow patterns can cause distribution system voltage regulation devices, such as step voltage regulators, load tapchangers, and switched capacitor banks to respond inappropriately.

Extensive case studies have been performed to assess the potential impact of DG on distribution feeder voltage profiles. The studies used, as a base, typical distribution system designs which provide acceptable voltage regulation at all points on the feeder (spatially) and over the full range of feeder load level (temporally). Distributed generation penetration was increased and the impact on voltage regulation was observed. From these case studies, generalized conclusions were reached.

The studies have been performed considering both generic models of a single radial distribution feeder with uniformly distributed load, and a more complex and irregular system comprising two radial feeders from a common substation. The complex, irregular system model is the "P2" system as defined in the *Models and Virtual Test Bed* report,[1] and will not be described further in this report. The simple feeder models are described below.

3.1.1 Generic radial feeder models and cases for voltage regulation analysis

The voltage regulation cases are a full matrix of combinations of the following:

- Feeder design
- Load level
- DG penetration
- DG spatial location
- Scenarios of load growth relationship to DG deployment
- DG local voltage regulation strategy.

Base feeder designs

The simple radial feeder models include design variations typically encountered in practical distribution systems. The models include a:

- Shorter radial 12.47 kV feeder, four miles in circuit length, representing a heavily loaded urban or dense suburban situation
- Longer eight-mile radial feeder (also 12.47 kV) representing a typical lower load density situation (suburban or rural)

The eight-mile feeder model includes step voltage regulators (SVR) and capacitor banks to provide a valid voltage profile in the base, no-DG condition. Where applied, SVRs were located at the 50% point of the feeder length. The four-mile feeder represents a more rudimentary design, and does not have voltage regulators or feeder capacitor banks to control the voltage profile. Both feeder models include regulation of the substation voltage at the source end of the feeder, including load-drop compensation (LDC) strategies in many cases.*

The first half of each feeder has per-mile impedances typical of a 400 Ampere 12.47 kV overhead feeder line. The second half has typical impedances for a 200 Ampere capacity line. The line impedances are summarized in Table 1. Reductions of line capacity, for feeder sections remote from the substation, is a typical design practice.

DG deployment

Voltage regulation was analyzed for the following DG spatial locations:

- Distributed uniformly along the feeder
- Lumped at the beginning of the feeder
- Lumped at the middle of the feeder
- Lumped at the end of the feeder

The rated outputs of the DG were scaled to evaluate the impact of penetration levels ranging from zero to 100%. In this study, the DG penetration is defined in as ratio of the sum of the DG output ratings for all DGs on the feeder, divided by the base feeder peak load.

Feeder loading

The peak load in the base (no DG) condition of all the radial feeder designs is 7 MW, with loads uniformly distributed along the length of the feeder. All system design and DG penetration variation cases were tested at both peak load and at a minimum loading level of 30% of peak. The load power factor was 0.85 at peak load, and 0.95 at minimum load.

A focus of this study was on the changes in the distribution system voltage regulation performance as the amount of DG in the system is increased. The voltage regulation performance of each feeder design was tested with two different load change with DG penetration scenarios:

- The DG is added to the existing system, with no offsetting change in load level (7 MW for 1 p.u. load).
- The DG and an equivalent incremental load is added to the system (Thus for 100% penetration, at peak load, there would be 14 MW of load connected to the feeder with 7 MW supplied by the grid and 7 MW supplied by the DG).

The DG installations were modeled operating at rated output, regardless of the load level. This reflects the possibility that DG operators, if allowed,

Table 1 Generic feeder model impedances

	First half		Second half		Total feeder	
Generic feeder model	R (Ω)	X (Ω)	R (Ω)	X (Ω)	R (Ω)	X (Ω)
4-mile feeder	0.5	1.0	0.8	1.4	1.3	2.4
8-mile feeder	1.0	2.0	1.6	2.8	2.6	4.8

* Load drop compensation is a voltage strategy where the voltage setpoint maintained by the substation load tapchanger or a feeder step voltage regulator (SVR) is adjusted in proportion to the real and reactive current flow at that point. If current were constant along the feeder, the effect of the LDC is to hold the voltage constant at an arbitrary, remote location elsewhere on the feeder. For example, if all of the load were lumped at the end of a feeder, and the proportionality constants of the LDC were 50% of the real and reactive impedance of the feeder, voltage would remain constant at a point halfway along the feeder.

Table 2 Feeder designs case table

Base design	Design variation	Substation LTC Control: Voltage setpoint	Substation LTC Control: Load drop compensation settings R (Ω)	Substation LTC Control: Load drop compensation settings X (Ω)	Substation LTC Control: Load drop compensation settings Voltage limit	Capacitor banks[1] kVAr rating	SVR Control: Voltage setpoint	SVR Control: Load drop compensation settings R (Ω)	SVR Control: Load drop compensation settings X (Ω)	SVR Control: Load drop compensation settings Voltage limit	DG Voltage regulation[2]
Case 1: 4 mile feeder	1.1	1.05	no LDC		fixed	0	no SVR				secondary
	1.2	1.04	0.30	0.60	1.05	0	no SVR				secondary
	1.3	1.05	0.00	0.00	1.05	varied[3]	no SVR				secondary
Case 2: 8 mile feeder	2.1	1.01	0.75	1.50	no limit	900	no SVR				secondary
	2.1	1.02	0.60	1.10	1.05	1200	no SVR				secondary
Case 3: 8 mile feeder	3.1	1.02	0.50	1.00	no limit	900	1.01	1.01	1.01	no limit	secondary
	3.2	1.03	0.25	0.50	1.05	900	1.01	1.01	1.01	1.01	secondary
	3.3	1.03	0.25	0.50	1.05	900	1.01	1.01	1.01	1.01	primary

1. Capacitor banks of these three-phase ratings were applied at the 20%, 40%, 60%, and 80% points along the feeder length
2. Location of the voltage regulated by DG.
3. Capacitor banks were added having the total kVAR rating equal to the incremental reactive load demand created by the changes in peak feeder load with DG penetration. Total kVAR was divided into banks located at the 20%, 40%, 60%, and 80% points along the feeder length

may make maximum usage of their generation assets and export power into the grid if not needed for local loads. Thus, for penetrations exceeding the minimum feeder load, the net power flow of the feeder will be reversed at light load.

DG local voltage regulation

For each case, simulations were performed with two voltage regulation assumptions:

- The DG is operated at unity power factor.
- The DG attempts to regulate the voltage at the secondary of its distribution transformer to 1.0 p.u., using a regulator with a 5% droop. The DG reactive power output is limited to 0.9 power factor, both leading and lagging.

For one series of cases, the DG voltage regulation strategy was modified such that the DG attempts to regulate the primary side voltage, with the same droop and within the same reactive output limits.

Case table

Table 2 summarizes the feeder designs studied along with the load drop compensation (LDC) settings used, and the location (primary or secondary voltage) regulated by the DG in the sub-cases where the effect of DG voltage regulation was investigated. Note that, for each line in Table 2, a total of 1,536 loadflow simulations were performed. This is illustrated by the case tree structure shown in Figure 1.

3.1.2 Generic feeder voltage regulation results

Voluminous results were generated by this study. The main body of this report summarizes overall observations and conclusions, and the specific case results are relegated to appendices.

Each case generated a voltage profile plot such as shown in Figure 2. Per-unit voltage levels are shown as a function of distance along the feeder, with the substation (source) end as zero distance. The global measure of voltage regulation performance is the voltage range between the minimum voltage at any point on the feeder, at any point in the load level range, and the maximum voltage at any point or load level. Note that these two points will usually not correspond to the same location or load level. If this global maximum and minimum are within the 0.98–1.05 p.u. range, then the voltage regulation is

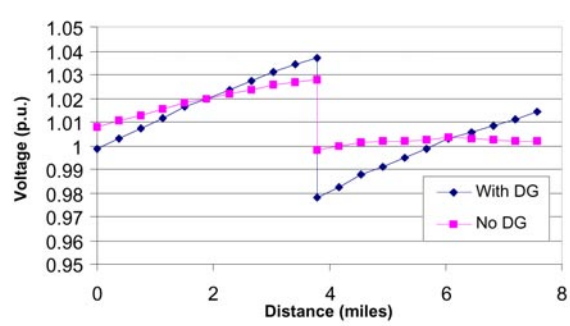


Figure 2. Typical voltage profile plot.

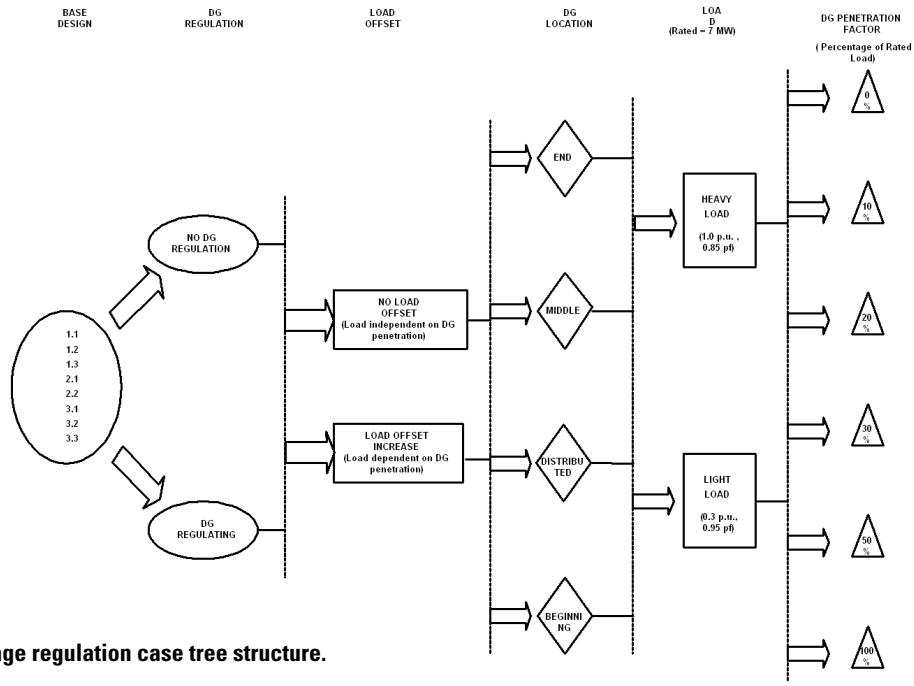


Figure 1. Voltage regulation case tree structure.

acceptable. As DG penetration level is increased, the global voltage range will change, usually widening. A plot, such as that shown in Figure 3, can be made of the global voltage range band as a function of DG penetration. This plot clearly illustrates the impact of DG penetration on distribution system voltage regulation performance. The solid lines in this plot indicate the voltage range with the DG operating at 100% of rated output. The DG, however, may operate at any power level or be off line. Therefore, if the voltage maximum or minimum without the DG (0% penetration) is more limiting, this no-DG condition establishes a wider voltage range. This is shown as a broken line, labeled "Ref Min" and "Ref Max" on the plots. Appendix A provides the global voltage range plots for all cases analyzed.

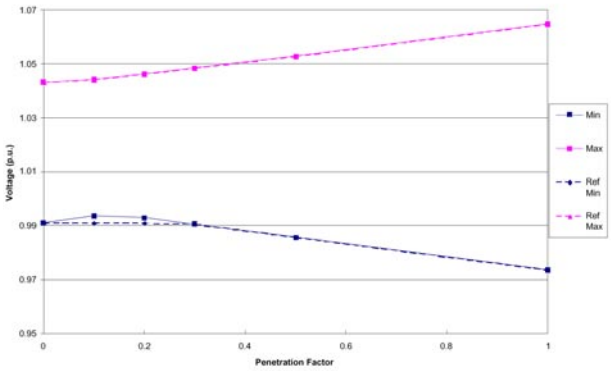


Figure 3. Typical global voltage range versus DG penetration.

The global voltage range plots, however, often do not indicate the root cause for the voltage range excursions. A narrative, case-by-case discussion of generic feeder study case results is provided in Appendix B. This case narrative includes a number of voltage profile plots, similar to that in Figure 2, to illustrate significant findings of the cases.

3.1.3 P2 system study[1]

In addition to the generic single-feeder analyses described above, additional study was made of an example distribution system having multiple feeders sourced from common substation, irregular distribution of loads and DG, and a more complex topology which included laterals from the radial feeders. This system is the "P2" system as described in the Virtual Test Bed Final Report. This system model represents a system which has evolved to become dependent on the installed DG. Unlike the generic feeder studies described earlier, this system is not designed such that the voltage profiles are adequate without the DGs.

Loadflow analysis of the P2 system over a range of load conditions produce results consistent with results obtained in the previously-described generic single-feeder analyses. Voltage profiles for the P2 cases are provided in Appendix C.

The P2 system, as noted earlier, has a high penetration of DG. At peak load, the output of the DGs account for over 40% of the total active power load on the distribution system. For such a high penetration of DG, the contribution of active power

becomes a major factor in managing the load profile. As would be expected, a completely passive or decoupled approach to managing the DGs can create difficulties.

The importance of the DG contribution at peak load is shown in the following two figures. Figure 4 shows the P2 system at peak load, with the five DGs on-line and delivering rated power. The largest DG, located at bus G2-2, also is delivering reactive power – as would be expected of device of this size. The figure shows a satisfactory voltage profile on both feeders.

When all of the DGs are removed, but the loads and the balance of the distribution feeder are kept with the same configuration, the distribution system has major problems. Figure 5 shows this condition. The voltage has dropped to unacceptably low levels on about half of the load buses in the system. The voltages near to where the large DG at bus G2-2 had been connected are extremely low. This extreme case illustrates the obvious reality that when DGs become a major source of power on a system, then arbitrarily removing them from service (for any reason, economic or technical) can cause serious problems. The customer at bus G2-2 in particular serves to make this point. The relatively large load at the bus is normally served by the DG there. When that DG is removed, but the load is not modified accordingly, the voltage at that customer and at all of the customers in the immediate vicinity are significant affected.

The appendix includes a sequence of load/voltage profiles showing the impact of the DGs as the load varies from this peak condition down to 20% of peak. In these cases, the DGs maintain their rated output. When the load drops to 40% and lower, all of the power requirements of the distribution system are satisfied by the DGs, and the excess is exported to the grid.

One potential impact of the power flow reversal that occurs when the DGs exceed the local power requirements on the feeder, is to confuse step voltage regulators (SVRs). Many radial distribution feeders are actually configured as loops with a normally open point. If the normal source for a feeder is unavailable (e.g., the feeder breaker is out for maintenance), the open point can be closed and the feeder can be fed in the reverse direction from another feeder, as illustrated in Figure 6. The SVR at location A must now regulate the downstream side voltage at location B, instead of the normal downstream side at location C. To automate this control logic change, some SVRs used on open-loop distribution feeder systems have power flow sensing logic which shifts the control scheme when the power flow reverses. This control feature is based on the assumption that power flows from the grid down to loads on the receiving side. Further, the SVR logic assumes that the grid is the strong or stiff side, and that the voltage is to be regulated on the receiving or downstream side.

If the flow reverses due to DG output exceeding local load requirements, SVRs with this type of logic will switch their controls to regulate the voltage on the grid side, rather than the feeder side. The SVR control will then become unstable and will run to its regulating limit, depressing the voltage on the side away from the distribution substation. This behavior is shown in Figure 7. The voltage on feeder 2 beyond the SVR is unacceptable in this case. The profile with a correctly operating SVR for this condition is acceptable (as shown in Appendix C).

This regulator instability cannot be easily corrected using local information. Communication of feeder sectionalizing switch and breaker status to

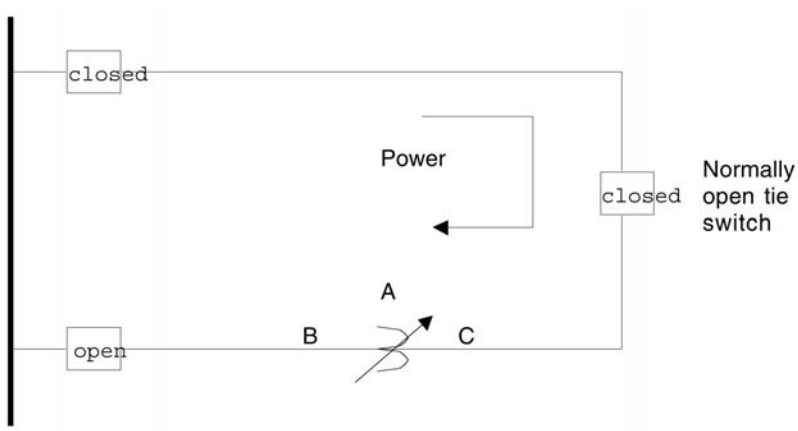


Figure 6. Open loop radial feeder topology.

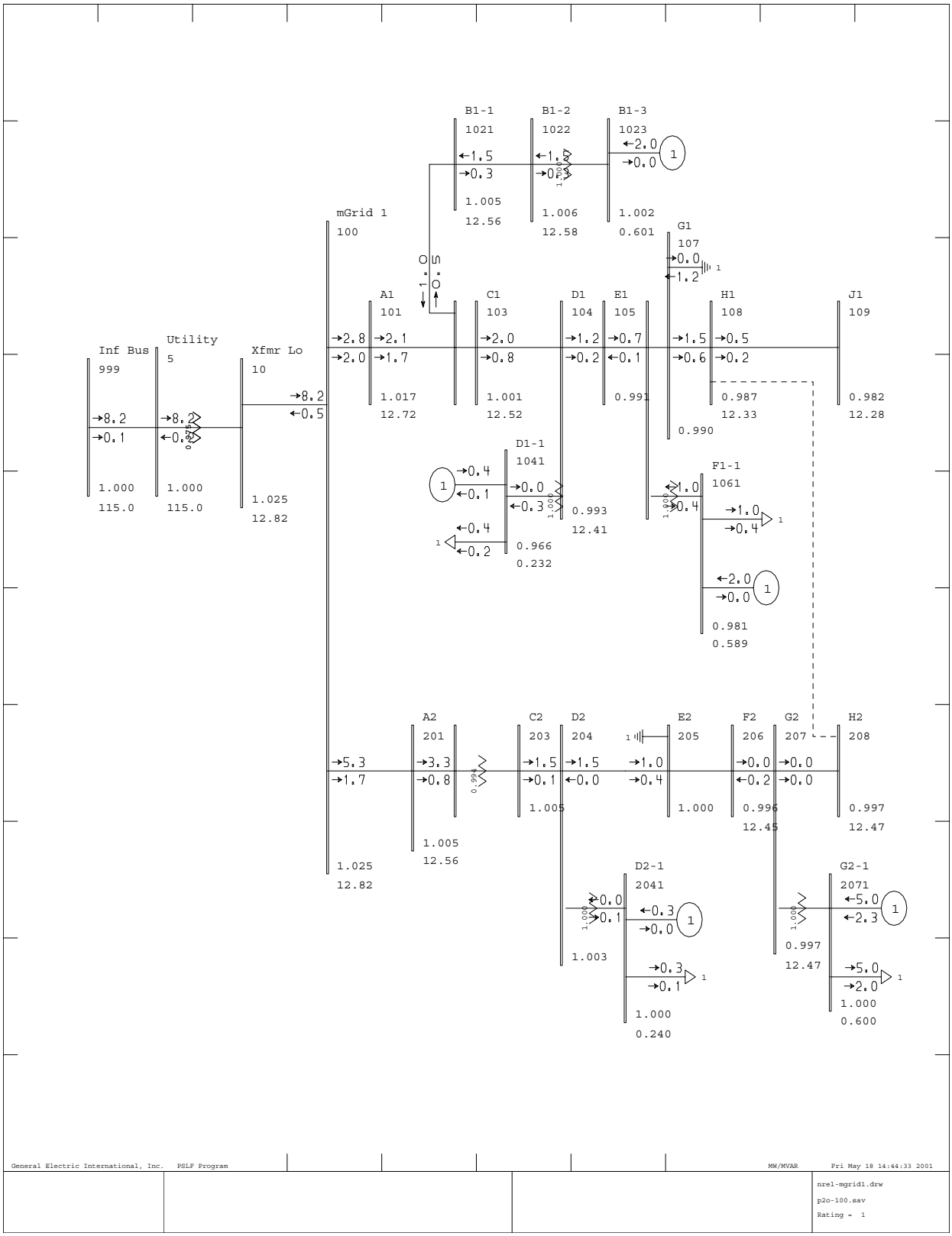


Figure 4. P2 System at peak load with all DGs operating.

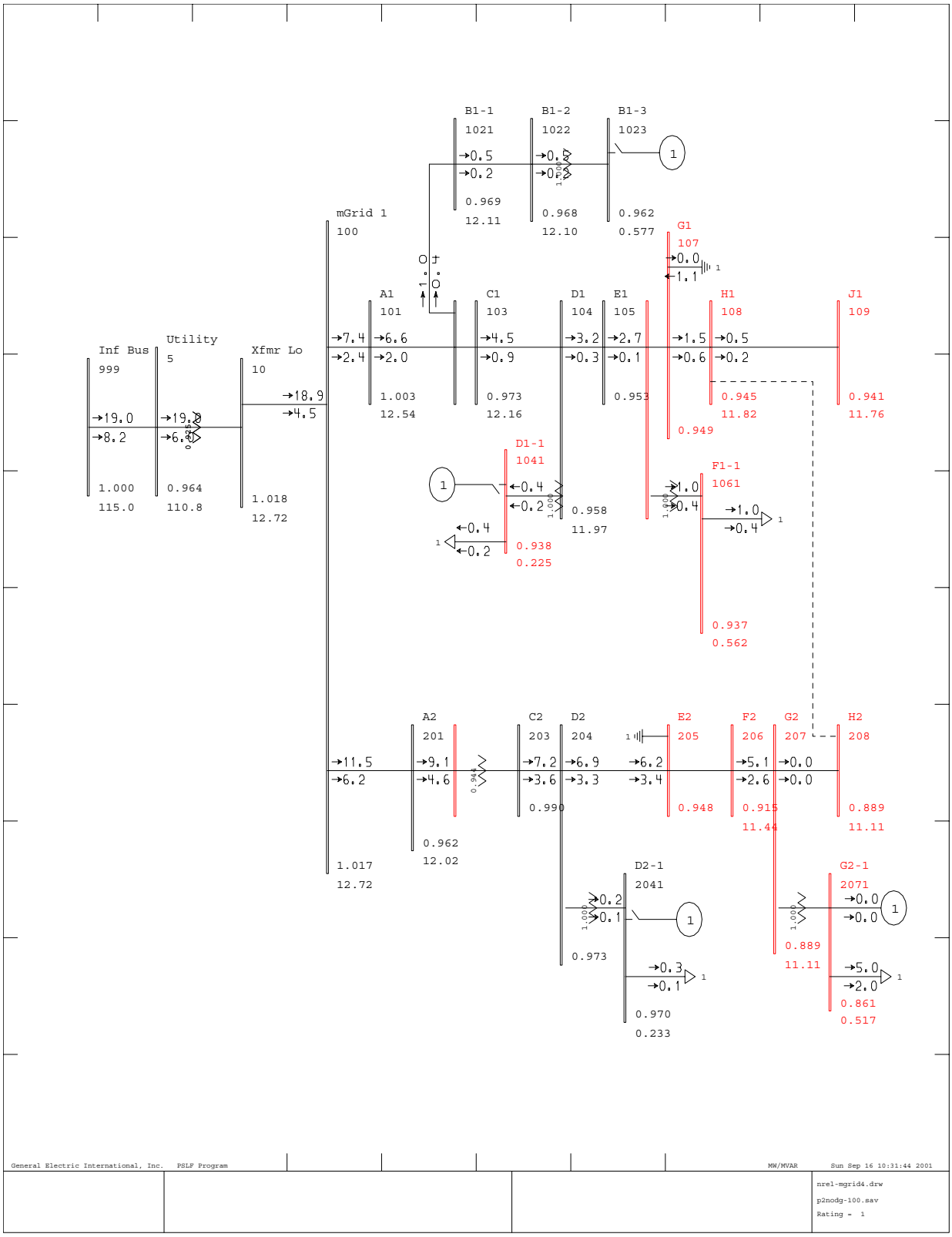


Figure 5. P2 System at peak load with no DGs operating.

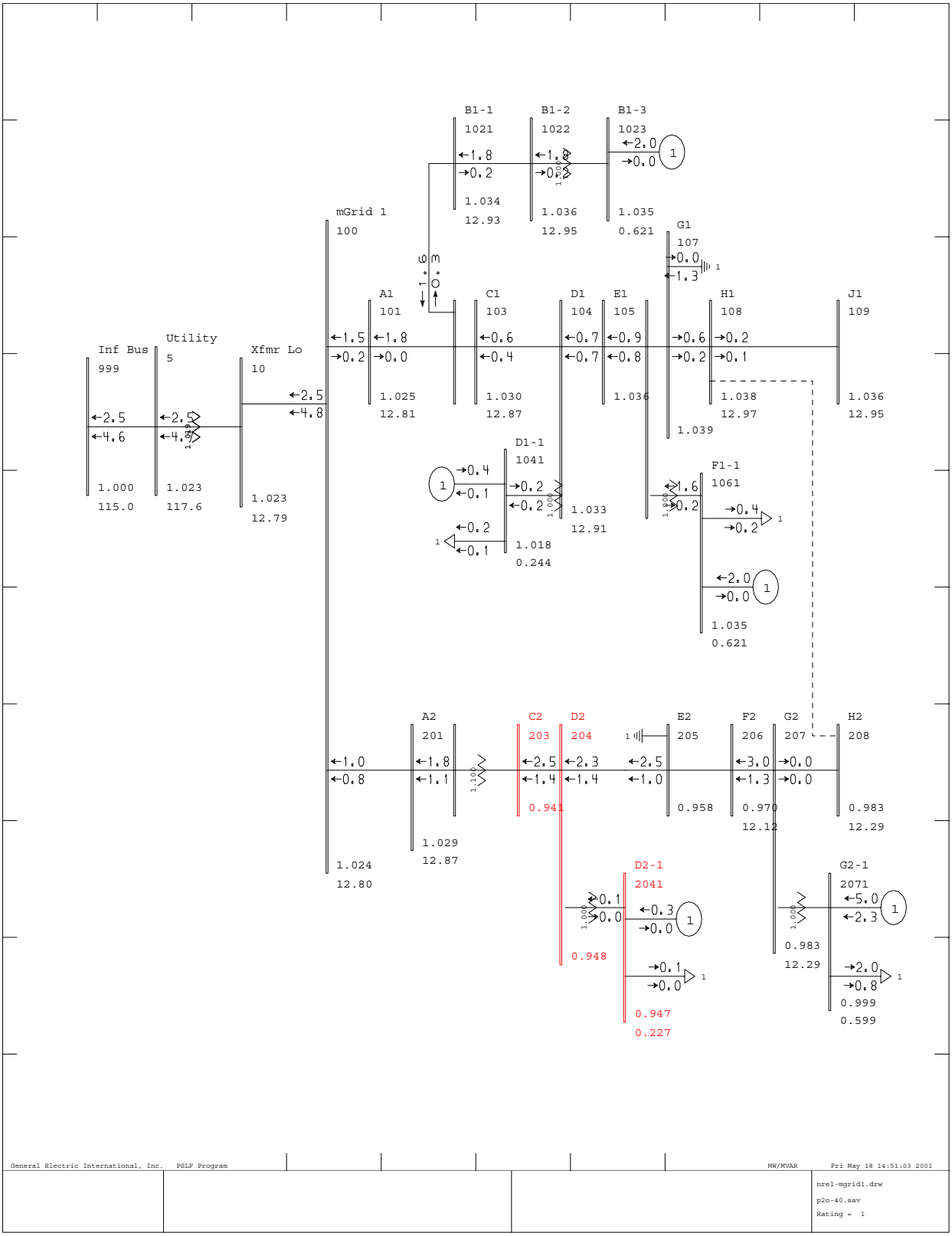


Figure 7. P2 System at 40% Load with unstable SVR.

the SVR is probably necessary, which can be an expensive requirement if a communication infrastructure or distribution automation system is not available.

3.1.4 Summary of significant voltage regulation issues

Overvoltages due to reverse power flow

The voltage at the substation end of a feeder is typically regulated to a value which allows for the normal voltage drop along the feeder, such that the voltage at the remote end of the feeder is within the acceptable range at full load. At a give point on the feeder, if the downstream DG output exceeds the downstream feeder load, there is an increase in feeder voltage with increasing distance. If the substation-end voltage is held to near the maximum allowable value, voltages downstream on the feeder can exceed the acceptable range.

The threshold of penetration where this line-rise overvoltage becomes an issue depends on how the DG and load are distributed on the feeder. With uniformly distributed load, and the DG lumped at the remote end of the feeder, the DG output need only be half of the current feeder load (typically 30% of peak), or about 15% penetration, for the remote end voltage to exceed the substation voltage. This issue is most significant when the DG is lumped at the end of the line, and is not an issue when the DG is lumped at the beginning of the feeder. With DG distributed uniformly along the feeder, the line-rise overvoltage begins to be a significant issue when penetration exceeds 50%. These penetration thresholds are for a feeder without fixed reactive compensation installed on the feeder. Where fixed capacitor banks are used, the light-load overvoltage problem will be exacerbated and penetration thresholds will be somewhat less.

Interaction with LTC and SVR controls

Load drop compensation (LDC), typically used on load tapchanger (LTC) and step voltage regulator (SVR) controls, adjust the voltage setpoint based on locally-measured real and reactive current flow. In a distribution system without DG, it can generally be assumed that the current flow at these control devices follows the same trends as the current at other points downstream of their location. Thus, LDC settings can be calculated which give adequate regulation at all points on the feeder.

The presence of DG can cause localized changes in flow patterns which are not reflective of the general trend on the feeder. As a result, the LTC or SVR can be set such that a good voltage profile is not obtained. If a large DG is exporting power at a location immediately downstream from a voltage regulating device with LDC, current flow through the device may be greatly reduced or even reversed. As a result, the device will not provide enough voltage boost, and voltages at downstream locations may drop below the acceptable range.

At light loads with high LDC settings, reversed power flow can cause the voltage setpoint to be below the acceptable range, subjecting loads immediately downstream of the LTC or SVC to be subjected to an undervoltage condition.

These LDC interaction problems generally occur for a penetration of 30% to 50%. The threshold penetration, however, can be less if the DG is lumped immediately downstream of the LTC or SVR.

As shown in the P2 case with light (20%) load, it is possible for an SVR with a “reverse power sensing” algorithm to incorrectly shift its control objective and become unstable. This can result in severely out-of-range voltages on a feeder system.

Effectiveness of voltage regulation by DG

Early drafts of the P1547 standard did not allow a DG to regulate voltage, effectively requiring operation at a constant power factor or reactive power output. While later drafts of this standard does allow voltage regulation, it is generally perceived to be unwise to attempt grid voltage regulation with a DG.

All scenarios in the generic feeder study were performed with and without voltage regulation by the DG. The DG regulation effectiveness modifying the primary feeder voltage was limited, however, due to the following practical assumptions:

- The DG reactive power was limited to 0.9 pf leading or lagging.
- The voltage regulator had a 5% droop, meaning that the voltage must be 5% from the setpoint for the DG to reach full reactive output.
- The DG is connected to the primary feeder through the impedance of a distribution transformer.

The impact of allowing the DG to regulate voltage was found to be mixed. In many cases, DG voltage regulation minimized or eliminated feeder voltage regulation problems caused by the penetration of DG. In many other cases, regulation of the local voltage by DG was ineffective in counteracting the impact of DG penetration on feeder voltage regulation. In a significant minority of cases, DG regulation of local voltage introduced as aggravated feeder voltage regulation problems, primarily by interaction with system voltage regulation devices such as SVRs.

Addition of load with DG

It might appear that addition of feeder load, matched by an equal offsetting DG capacity, does not have a system impact. This may not be the case for the following reasons:

- The DG may be operated at full capacity while its associated load is at a low value in order to reap the economic benefits of exporting power to the grid. This can result in overvoltages due to line voltage rise due to reversed power flow, and undervoltages due to interaction with LDC schemes on LTCs and SVRs.
- Matching load and DG kW does not mean that reactive power requirements are met by the DG. DGs are often operated at unity power factor, or even slightly leading, for maximum production economy and also to minimize the chance of inadvertent islanding. Meeting increased load demand with DG not supplying the incremental loads' reactive power requirements places the reactive demand on the utility system. This can result in undervoltage conditions, or even overvoltage conditions due to interaction with LDC schemes.
- DG may not be located at the same location on a feeder where incremental load is added. This can cause local aberrations in the power flow, affecting voltage profiles over the whole feeder.
- There may be situations where the DG or DGs are off line with the load connected. This can result in widespread voltage problems in a system dependent on the DG. It is possible for a single system event, such as a voltage dip, to simultaneously trip all connected DGs. Also, certain economic conditions, such as a spike in natural gas prices, might also cause a large number of DGs to not be operated.

While DG might be viewed as a means to avoid distribution system investment to meet future load growth, it cannot eliminate this investment need entirely. Public policy, regulations, and utility tariffs need to be designed which appropriately assign the incremental costs of distribution system infrastructure improvements needed to support the interconnection of self-generating loads.

Recommendations for voltage regulation improvement

The underlying cause for DG-induced voltage regulation issues is the autonomous operation of various voltage regulation devices in a distribution system. LTC and SVR controls operate with local information, with the assumption that the local information is a reflection of the performance elsewhere in the system. A DG generally has the ability to supply or consume reactive power, which can be used to help regulate system voltage. The DG, however, would normally respond only to local voltage conditions. This response can be detrimental to voltage regulation elsewhere on the system, particularly if the DG is located near to a distribution system voltage regulation device. The ultimate solution is an integrated control approach where DG reactive power output is used to assist overall feeder voltage regulation, and system voltage regulation devices (LTCs, SVRs, and switched capacitor banks) are controlled using more complete information, including the voltage profile throughout the system and the status and output of connected DGs. Implementation of such a scheme, however, requires a communication infrastructure not currently available in most distribution systems.

3.2 DG DESIGN CONSIDERATIONS TO MEET POWER QUALITY REQUIREMENTS

Power electronic DGs bring along with them a number of concerns that are critical to the quality of power in the utility system:

- Unlike rotating machine based generators, power electronic DGs have the capability of injecting subsynchronous current and DC into the grid. Distorted current injected by the DG can lead to aberrant operation and damage neighboring equipment.
- Presence of DGs can cause customer complaints due to flicker in lighting loads. Proper control of the DG can lead to reduction of flicker.
- Emerging power electronic inverter topologies used in DG applications can lead to grounding issues that have not been considered in traditional utility grounding studies.
- Unbalanced grid voltage can impact power quality depending on the DG inverter control strategy.

These issues which have a substantial impact on power quality are addressed in this section.

3.2.1 Current distortion from power electronic DG

All power electronic equipment create current distortion that can impact neighboring equipment. These concerns and impact can be classified according to the dominant frequency component of the distortion current.

- ***Subsynchronous current distortion***—This can be caused by a change in reference to the DG and by nonlinearities in PWM power converters. DG current control using methods such as bang-bang modulation can lead to significant

subharmonic content in the output current. Low and very low frequency content in the waveforms can lead to low frequency current injection and flicker. These issues are discussed in section 3.2.2 and 3.2.3.

- ***Harmonics of the fundamental frequency***—High power electronic equipment and equipment based on conventional line commutated power converters have a large harmonic content. High frequency, PWM power converters are capable of injecting relatively clean waveforms into the grid. One concern for DG application is that some anti-islanding algorithms purposely inject low frequency harmonics into the grid to detect islanding situations. The THD can become fairly significant depending on the settings of these algorithms. The recommended practice commonly referred to for harmonic limits of power electronic equipment is IEEE519.[3] The DG designer should ensure that the power converter meets these recommendations.
- ***Switching frequency harmonics***—These are inherently present at the output of the PWM inverter due to the on-off control of the power converter switches. An LC filter is typically used to filter the switching frequency harmonics. Care has to be taken in the DG design so that there is no poorly damped resonance caused by the filter capacitance and the grid impedance. Passive damping or active damping through appropriate control of the DG can prevent this resonance.
- ***High frequency distortion***—Signals in the range higher than 150kHz is considered EMI, which can be of conducted or radiated type. Circuit parasitic factors, materials and packaging, gate drive design and other factors that are not easily controlled by the designer can affect the EMI characteristic.[4] EMI filters can be used to reduce EMI emissions and improve susceptibility. DG vendors are obligated to ensure that the design of their equipment meets FCC standards

3.2.2 Flicker concerns for DG

Light flicker is a human sensation to luminous fluctuations and variations. Flicker is an old subject that is dated back to 1891—only four years after the AC power distribution concept was demonstrated. The luminous fluctuation could be periodic or non-periodic. It is a quite complex problem to quantify because it links both the objective and subjective aspects of the phenomenon.[5]

On the objective side, the fluctuation of the luminous output of a lamp depends on—

- The input AC voltage fluctuation; and
- Lamp type and ballast circuit for the lamps.

The AC line voltage fluctuation is normally the root cause of light flicker, especially for incandescent lamps. Therefore, a voltage flicker limit is necessary to confine the light flicker. The lamp types and their driving circuits determine luminous fluctuations in response to the AC line voltage fluctuation. For instance, the luminous fluctuation of an incandescent lamp is more sensitive to a low frequency voltage fluctuation (e.g., 5–15 Hz) than that of a fluorescent lamp. A 60 W 230 V incandescent lamp has a time constant of 19ms, while it is 28ms for a 120V incandescent light bulb, and less than 5 ms for a typical fluorescent lamp.[6]

Excessive light flicker can be very irritating to human eyes and causes customer complaints. On the subjective side, the human perception, including eye and brain response and brain storage effect are involved. The sensitivity of human eye to flicker is not uniform. First of all different people have different sensitivities. Also, not all of light flickers with the same luminous fluctuation magnitude produce the same irritating result to humans. The human eye tends to be more sensitive to periodic flicker than non-periodic flicker and the most sensitive periodic flicker frequency is around 8.8 Hz. This makes flicker measurement fairly complicated and statistical studies are called for.

What flicker means to DG systems

Flicker is an important power quality issue. Excessive flicker will cause customer complaints. For a DG system running in standalone mode (islanded), the disturbances of loads, such as start and stop of an air-conditioner, refrigerator, compressors, washing machines and cook-top, cause sudden load current changes to the DG inverter. In turn, these sudden current changes cause voltage drops due to the output impedance of the inverter, and thus, its AC output voltage will fluctuate causing light flicker. In standalone mode, the key to reducing voltage flicker is to reduce the output impedance of the PCS. The lower output impedance of the PCS calls for faster control dynamics and large transient current capability. They can be relatively easily examined in the models and through simulation.

In grid parallel mode, flicker is less of a problem since the grid supports the AC voltage. However, the flicker problem may still take place for a weak line. In this case the flicker is also associated with

the DG inverter control loop design. The main control parameters that impact flicker are:

- Loop damping—which controls voltage overshoot/undershoot
- Set-point limits and reference changes in output power
- Walk-in rates (i.e., rate of change limits for reference or load changes)
- Voltage support by DG VAR injection

Flicker due to energy source fluctuations

Fluctuations in the power delivered by a DG have the potential to cause flicker in the power system in a fashion very similar to that caused by load fluctuations. DGs may impose unwanted power fluctuations on the host power system (the local EPS or the grid) when two conditions are satisfied:

- The energy source (e.g., the wind turbine or fuel cell) has some mechanical (or chemical) fluctuations in power output, and
- The electrical equipment (e.g., the dc bus and inverter) does not have sufficient energy storage to smooth out these fluctuations.

When these two conditions occur, the power fluctuations must pass on to the system. One example of such mechanical power fluctuations is that which occurs in wind turbines when the blades pass the wind shadow of the supporting tower. When this occurs, the shaft torque experiences a momentary drop and real power output of the wind turbine generator will exhibit a periodic oscillation. This particular phenomenon can present a significant challenge in wind applications.

Specification of voltage flicker limit

Voltage flicker measurement and flicker limit specifications are difficult to define due to the reasons mentioned above. Fortunately IEEE and IEC standards provide some guidance.

IEEE standards

The P1453 Flicker Task Force voted to adopt the IEC methodology in 1998. The IEC 1000-4-15 standard has been modified to accommodate North American 120 V power systems.[6,7] This will allow full coordination with IEC 61000-4-15. The voltage flicker limits are represented by two flicker curves – borderline of visibility and borderline of irritation. These curves are also called the "GE Flicker Curve" since they are based on studies conducted by GE starting in 1921, updated in 1930s and then again in 1950.[5] This curve provides percentages for voltage fluctuation limits assuming a certain repetition rate for the transient event.[8] However, the difficulty is that the voltage fluctuation percentage alone does not reflect the true light flicker, let alone the human perception. For instance, a lamp or the human eye may not respond to a very narrow yet higher voltage fluctuation than indicated in Figure 8. The curve also does not address voltage fluctuation at non-periodic rates. Therefore, a more

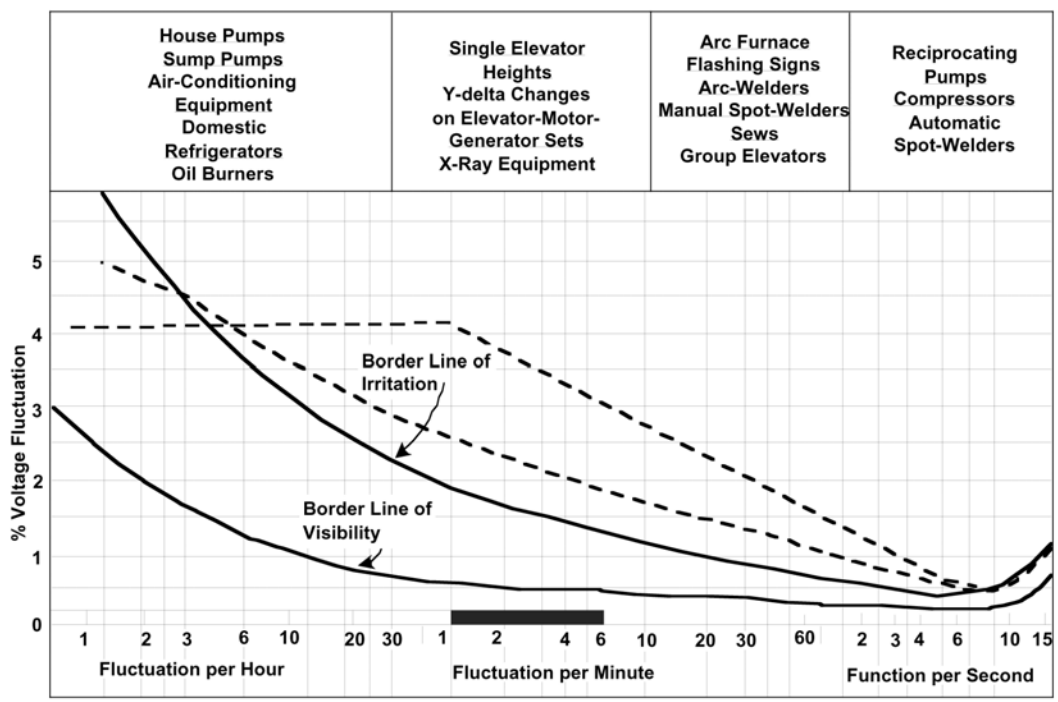


Figure 8. Flicker sensitivity curves—EC 555-3 (1982).

sophisticated method to quantify the voltage flicker is needed.

IEC Standards

(IEC Std. 61000-4-15, IEC Std. 61000-3-3, and IEC Std. 61000-3-5) IEC standards specified a flicker meter, which is a comprehensive way to measure voltage flickers.[9–11] The flicker meter is specified in IEC 1000-4-15 (originally IEC 868); the voltage flicker limit for equipment with rated current less than 16A is specified in IEC 1000-3-3; and the limit for equipment with larger than 16A rated current is specified in IEC 1000-3-5. The IEC flicker meter is a sophisticated measurement methodology considering lamp response, human eye and brain response, human brain storage effect, etc. Although the original limit and the lamp response function are derived based on 230 V 60 W incandescent light bulb, different lamp transfer functions can be easily included. IEEE-P1453 task force is considering to adopt this methodology and modify the limit and lamp transfer function based on the 120 V 60 W incandescent light bulb to fit North American power systems.

Flicker performance of the P2 system

This section presents illustrative simulation results from the P2 system. The potential impact of DG on local flicker problems due to load fluctuations is examined. Then, the potential for fluctuations of the DG energy source to cause flicker is shown. The relative behaviors of inverter based DGs compared to rotating DGs are shown.

DG impact on load-induced flicker

Figure 9 shows the system response from the P2 system when it is subjected to a disturbing load. In this case, the one large load at bus G2-1 on the P2 system is disturbing the feeder. The load exhibits periodic steps in active power order. This behavior is representative of a number of types of disturbing loads, an arc welder being a good example and a common cause of flicker on commercial and residential distribution feeders. For these cases the load pulsations are periodic, at a rate of 0.6 Hz. The three traces in Figure 4 are all voltages at the D1 bus in the P2 system. The voltage traces represent three different conditions for the P2 system:

- No DGs (blue trace with stars)
- Inverter type DGs (red trace with circles)
- Rotating type DGs (green trace with crosses)

The results of this test are consistent with the overall characteristics of the two classes of DGs. The voltage deviations at bus D1 (and all other points in the distribution system) occur at time of the load pulsation. The voltage fluctuation for the no DGs case is 0.46%. This level of fluctuation would be well above the threshold of visibility at this frequency, and would be near the threshold of irritation for frequencies in the approximate range of 3–8 Hz.

The addition of inverter type DGs at the five locations in the system has a slight beneficial impact on the flicker, with the amplitude of the voltage deviation being slightly decreased to 0.36%. The voltage traces shown are for a load bus that is served by a small DG. The difference in voltage performance at other buses in the system not served by DGs is less. The interaction of the DG with voltage deviation is minimal. The DG behaves as a nearly perfect current source under these conditions, as expected.

The addition of the rotating type DGs has a substantial beneficial impact on flicker. The amplitude of the voltage deviation is reduced to about 0.08% - a roughly 80% improvement. This substantial benefit is because the rotating DGs, unlike the inverter based DGs, increase the short circuit strength of the distribution system. Again, the improvement at other buses, not served by DGs is less. A complete set of results for this case is included in Appendix D.

A further investigation of potential DG impact on flicker is presented in Figure 10. In this case, the DGs have been provided with a voltage control function. Provision of voltage is readily achievable technically (and a requirement for isolated operation). The traces in Figure 10 correspond to the same three conditions as in Figure 9. Of the three traces, only the inverter-type DG trace shows a significant difference in performance. As the previous case showed, the inverter type DG has relatively little inherent response to the voltage flicker. However, the controls of the inverter can be made very fast.

In this case, the amplitude of the voltage flicker is reduced to about 0.16%: a dramatic improvement. This is consistent with expectation. In large power systems subject to voltage flicker, e.g. steel mills or auto fabrication factories, the standard practice for flicker mitigation when increasing short circuit strength is not possible, is to provide voltage control with power electronics. The most common power electronic device in present practice is the static var compensator or SVC. Recently, however, the use of SVCs is being supplanted by voltage source inverter based devices, which the power industry has termed 'STATCOMs' (for static compensators). Inverter based DGs, when provided with a voltage regulator function, are nearly functionally identical to STATCOMs. Thus, providing this capability has very substantial beneficial impact

on the dynamic voltage performance of the distribution feeder.

The voltage behavior of the rotating DGs in Figure 10 is nearly identical to that in Figure 9, the case without voltage regulation. This reflects the fact that the speed of response of rotating DGs is limited by machine time constants, not the controls. Rotating DGs provide flicker benefit mostly because of increased short circuit strength. This performance cannot be appreciably altered by controls. The complete results from this case are included in Appendix D.

In summary, these cases illustrate a few key points about DG impact on load induced flicker:

- Rotating equipment, including DGs, increases short circuit strength and therefore improves flicker performance,
- Additional control of rotating equipment is relatively ineffective at further improving flicker performance
- Inverter based DGs operating in a constant-current mode without a voltage regulation function have a very slight inherent benefit on flicker performance,

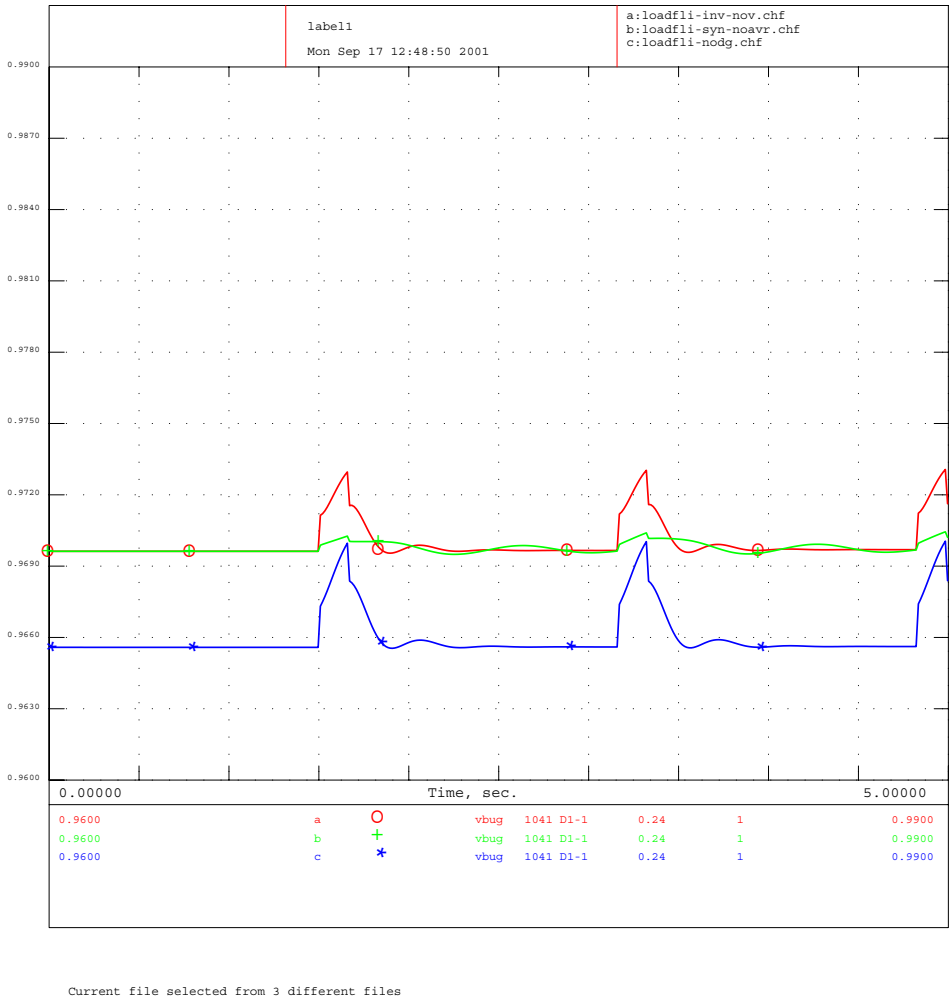


Figure 9. Example of load-induced flicker with and without DGs.

- Inverter based DGs have the potential to provide substantial benefit on flicker if equipped with controls that provide voltage regulation or some other functional equivalent.

DG-induced flicker

Above mechanisms which could cause the power output of DGs to fluctuate are discussed. Figure 11 shows the potential impact of such a fluctuation on the distribution system. There are two cases, one with rotating type DGs (the green traces with crosses) and one with inverter-type DGs (the red traces with circles). In these cases, one DG in P2 system (the large one at bus G2-1) is subjected to a 25% power fluctuation at 0.6 Hz. In the case of the rotating DGs, this fluctuation is modeled as a perturbation in shaft power. In the case of the inverter

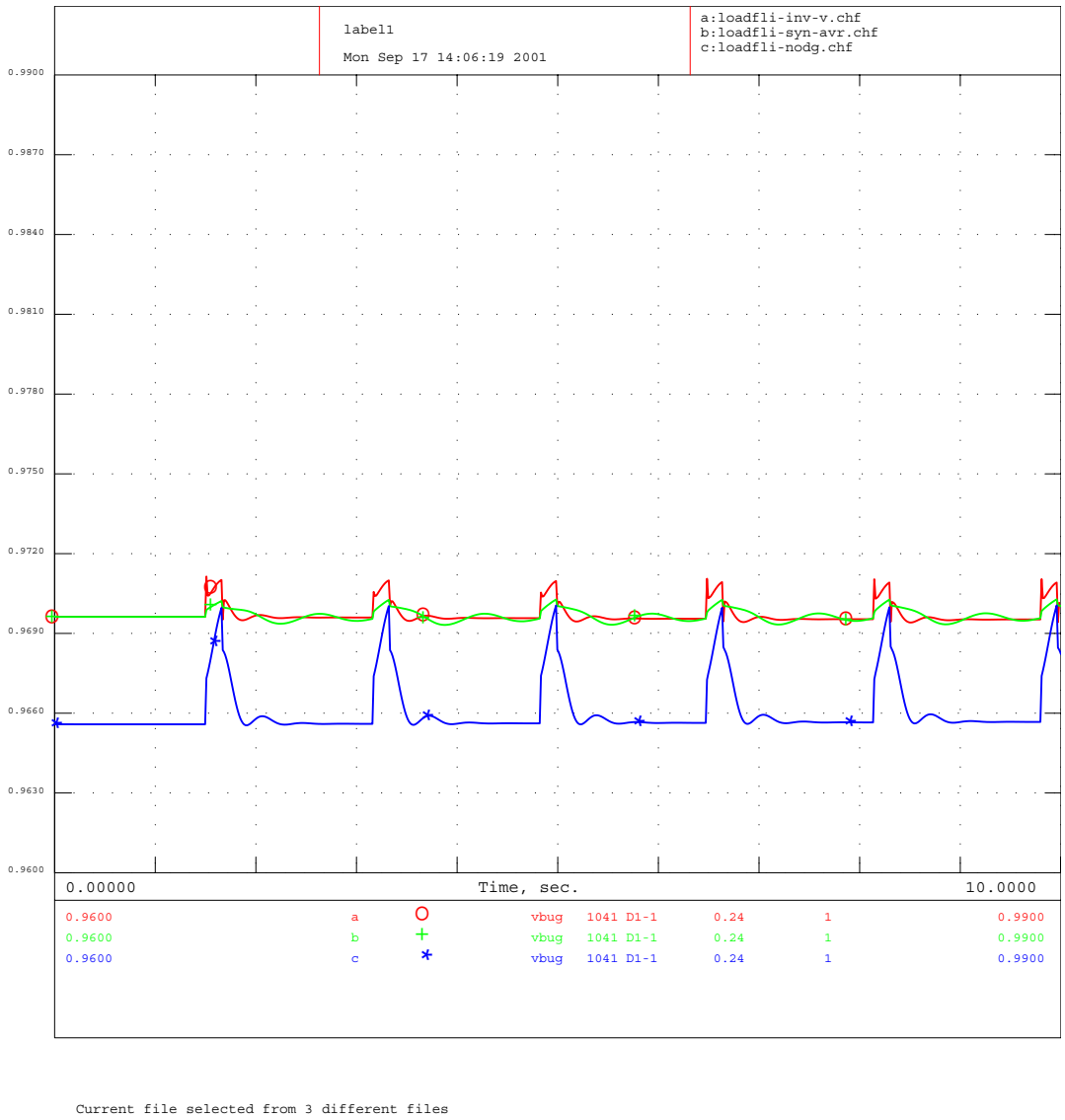


Figure 10. Example of load-induced flicker with and without DGs.

based DG, the fluctuation is modeled as a perturbation in active power output. Both systems have a flicker response to the power perturbations. The voltage fluctuations in this case are 0.22%, which would be just below the threshold of perception in the vicinity of one Hz. The case with the rotating equipment also exhibits some damped oscillatory behavior since the power fluctuations cause the machines to swing. Both cases illustrate the potential for DGs to cause flicker, and the need to avoid or minimize such power fluctuations from the DGs.

3.2.3 DC current injection

When DG power converters are directly connected (without isolation transformers) to the utility grid, there is the potential to inject DC current. This can impact transformers and other magnetic elements causing saturation and can cause torque ripple in adjacent machine loads. There can also be continuous DC voltage being applied under internal DG

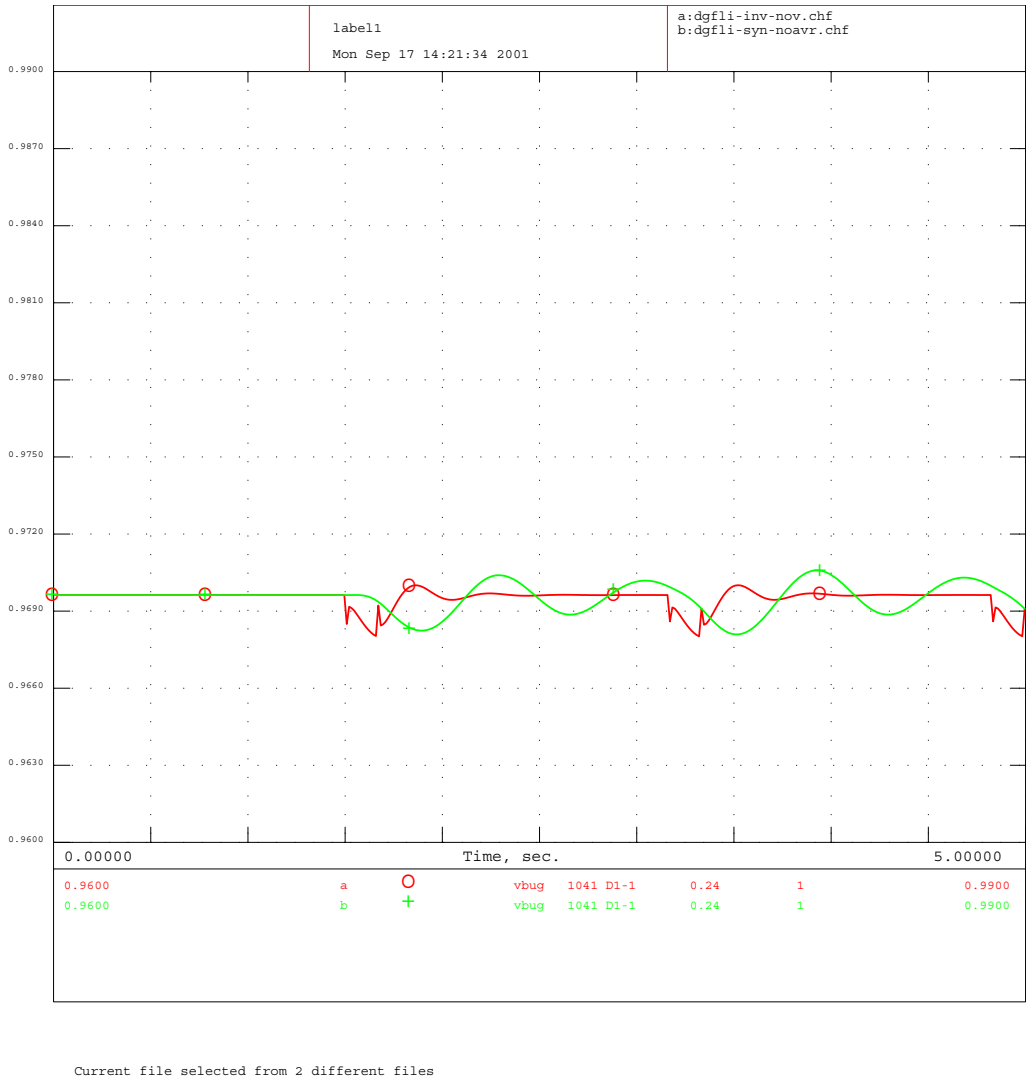


Figure 11. Example of DG-induced flicker.

power converter faults. The protection of the system has to be designed to clear such conditions. In grid-parallel mode, DC current injection limits are typically met by DG control functions. In stand-alone operating mode, the output DC voltage and its integral should be limited. This is to ensure that loads with low DC impedance such as machines and transformers do not saturate.

3.2.4 DG grounding issue

A grid-connected DG, whether directly or through a transformer, should provide an effective ground to prevent unfaulted phases from overvoltage during a single-phase to ground fault. The effective ground is defined as "*grounded through a sufficiently low impedance such that for all system conditions the ratio of zero-sequence reactance to positive-sequence reactance (X_0/X_1) is positive and less than 3, and the ratio of zero-sequence resistance to positive-sequence reactance (R_0/X_1) is positive and less than 1.*"[12]

DG with a transformer

Figure 12 shows a DG with a delta-wye isolation transformer. The grid distribution transformer is grounded wye-wye, which is the most common connection used for three-phase distribution transformers in North America.

During a single-phase fault, an equivalent sequence circuit can be derived (refer to Appendix E) and is shown in Figure 13.

Where, $Z_{120,INV}$ is the inverter sequence impedance, $Z_{120,TR}$ is the DG output transformer sequence impedance, $Z_{120,DT}$ is the distribution transformer sequence impedance, and $Z_{120,Grid}$ is the grid sequence impedance. I_{INV} is a controlled positive-sequence current by the inverter. $I_{120,A}$ is the fault phase sequence current and $V_{120,A}$ is the fault phase sequence voltage.

Based on Figure 13, the following scenarios can be observed:

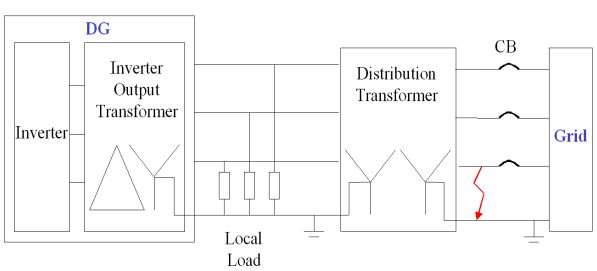


Figure 12. DG with a transformer interconnected to the grid through a distribution transformer during a single-phase fault at the distribution primary side.

- When grid is connected, i.e. the circuit breakers stay closed, the grid will provide a grounding source (sufficiently low zero-sequence impedance). Therefore, the system is still effectively grounded.
- When grid is disconnected, i.e. the circuit breakers opened, the grid sequence impedances are no longer part of the circuit. The distribution transformer provides a series path for zero sequence, but does not provide a grounding source.
- The zero-sequence impedance of the load can vary largely. Therefore, a parallel low-impedance grounding source should be provided.
- The inverter isolation transformer provides a shunt zero-sequence path to the load zero-sequence impedance. The transformer shunt zero-sequence impedance is normally low enough to provide effective grounding. However, the low zero-sequence impedance transformer will be subject to overload due to system disturbance. Normally, the transformer zero-sequence impedance is designed such that the effective ground can be provided (low enough), while it can also withstand system disturbance (high enough). This is a tradeoff in the DG transformer design.

DG without a transformer

For a DG without a transformer, for example, a four-leg inverter (or other topologies providing three-phase four-wire output without an output transformer), the grounding performance has to be examined. Figure 14 shows a four-leg inverter-based DG without a transformer.

During a single-phase fault, an equivalent sequence circuit can be obtained as in Figure 15.

Similarly, based on Figure 15, the following scenarios can be observed:

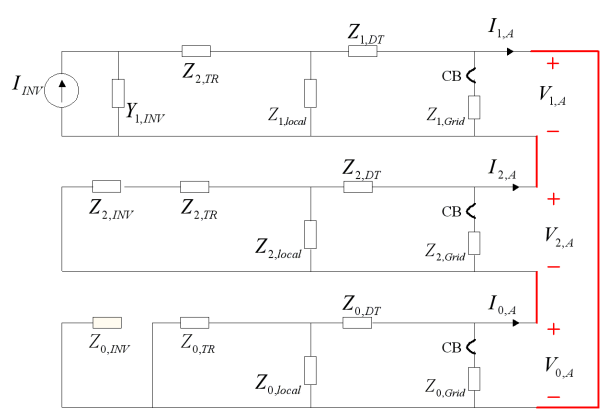


Figure 13. Equivalent sequence circuit during a single-phase to ground fault.

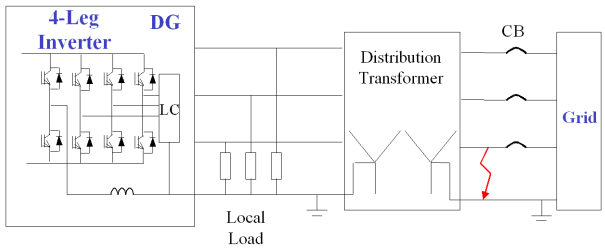


Figure 14. Four-leg inverter-based DG interconnected to the grid through a distribution transformer during a single-phase fault at the distribution primary side.

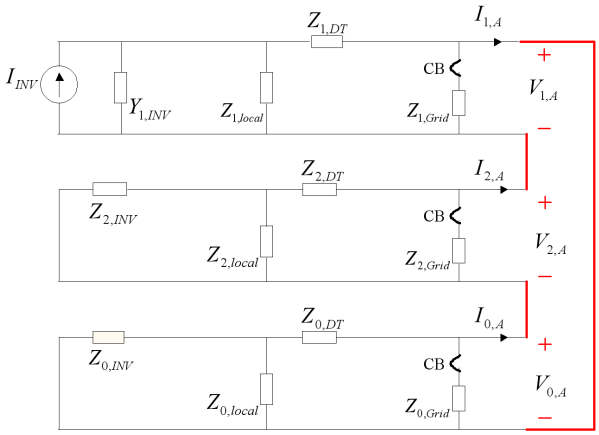


Figure 15. Equivalent sequence circuit of the four-leg DG system during single-phase to ground fault.

- When grid is connected, the grid will provide a grounding source. Therefore, the system is still effectively grounded.
- When grid is disconnected, i.e. the circuit breakers opened, the four-leg inverter should be designed such that a low zero-sequence impedance $Z_{0,INV}$ is obtained for the DG to provide an effective ground.

3.2.5 Unbalanced grid

Several factors can cause grid voltage to be unbalanced:

- Load imbalance is the most significant cause. A large portion of the connected load on typical distribution feeder is single-phase load, and the individual phase loadings have considerable statistical variation. As a result, the current flow is normally unbalanced, leading to unequal series voltage drops in the phases.
- Line impedance asymmetry is a secondary, less significant, cause for distribution voltage unbalance[13]

The most significant impacts of grid voltage unbalance on an inverter DG are:

- Additional non-characteristic harmonic currents will be injected into the system, degrading power quality.
- Second harmonic ripple will be present on the dc bus of the inverter. This can stress inverter equipment, increase losses, and interact with the dc source. For example, ripple can be detrimental to a battery used for energy storage, and can cause torque pulsations in rotating machines.
- Inverter phase current unbalance, due to the voltage unbalance, will slightly increase inverter losses.

This section will discuss the impact of unbalanced grid voltage on a PWM inverter-based DG, since the unbalanced grid impacts on rotating machines are well known.

Figure 16 shows the system one-line representation diagram under study. The DG comprises of an AC prime mover, diode rectifier, DC bus with bulk capacitor, and a three-phase inverter. The control design for the inverter is based on a rotating d-q referenced frame. The phase-lock loop (PLL) control is also based on d-q referenced frame, not zero-crossing detection commonly used for a single-phase system

The parameter variations are:

- Negative sequence grid voltage: 0%, 2.5%, 5% (defined as the ratio of negative-sequence voltage over positive-sequence voltage)

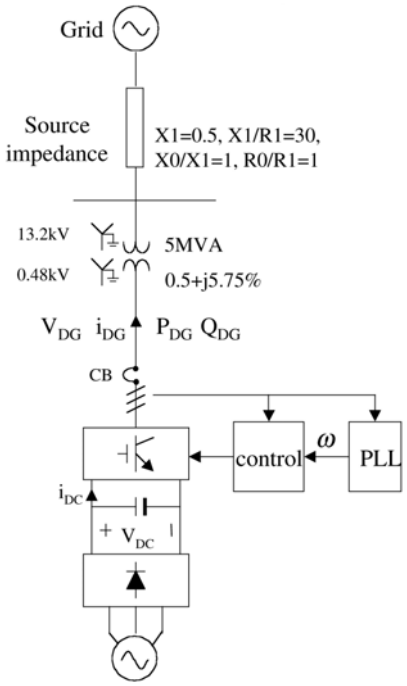


Figure 16. System diagram for unbalanced grid case study.

- PLL bandwidth (BW): 10 Hz, 30 Hz.

This section is focused on unbalanced grid impacts on DG and the implications to DG design

Since the DG is controlled as a balanced (positive-sequence) current source, the product of positive-sequence current and the negative-sequence voltage will cause two times fundamental frequency power ripple. This 120 Hz ripple will appear at the inverter input DC bus, mainly in form of ripple current i_{dc}. The DC bus voltage v_{dc} is much less affected due to bulk DC bus capacitor in a normal design. In the case that a PLL is realized in a dq reference frame, the output of the PLL, ω, will also pick up some 120 Hz ripple. Due to the limited current control bandwidth, the DG will have some negative-sequence current, i_{dg2}, response to the negative-sequence voltage. Figure 17 shows the ripple components (normalized) of the DC bus current i_{dc}, PLL output ω, and the DG output current unbalance (the ratio of negative-sequence current over positive-sequence current).

The unbalanced grid will also cause harmonics in the inverter output current. The higher the PLL bandwidth, the better the tracking performance in synchronizing voltage frequency. However, due to the presence of unbalance grid voltage, the higher PLL BW causes more DG output current distortion, as shown in Figure 18. The DG with 30 Hz PLL bandwidth has more output current THD.

Therefore, to reject the 120 Hz disturbance caused by voltage unbalance, the bandwidth of the PLL should be sufficiently lower than 120 Hz, if a conventional dq PLL is used. Typically, three methods are used to obtain accurate PLL output when there is voltage unbalance.

- Low pass filter. The cutoff frequency is one order lower than 120 Hz. This normally requires the PLL bandwidth to be around 10 Hz.
- Notch filter can be used to filter 120 Hz.[14,15] This way, the bandwidth of PLL can be higher than the method above.
- Algorithm to obtain only positive-sequence voltage information and use it as PLL input.[16] This way, the current reference is only synchronized with positive-sequence voltage.

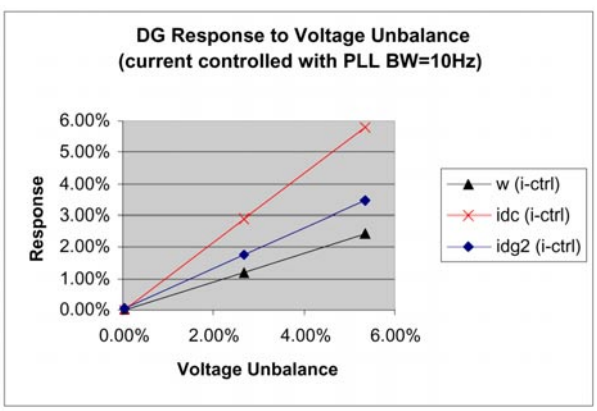


Figure 17. DG response to unbalanced grid . (w: 120Hz ripple of PLL output; idc: 120 Hz ripple of DC bus current; idg2: unbalanced DG output current (negative-sequence over positive-sequence).

3.2.6 Summary

- The harmonic issue with DG is primarily an equipment vendor design issue. Hence, it is a requirement of the DG design that the harmonics are below acceptable limits.
- Flicker and flicker assessment for PCS are discussed in general, including discussions on IEEE and IEC standards.
- The illustrative simulation cases show that DGs can have a generally beneficial impact on distribution system feeder flicker caused by other disrupting loads.
- Rotating type DGs have an advantage in their inherent ability to mitigate flicker caused by rapidly changing loads. This is due to their short circuit strength.
- Inverter type DGs can be operated to have characteristics similar to a rotating machine. Most DG inverter designs, however, are based on a constant-current control mode which does not inherently provide significant flicker mitigation.
- Inverter type DGs will have significant beneficial impact on flicker only if they have a voltage regulation function or if they have a control scheme where they are operated as controlled voltage sources (i.e., as virtual synchronous generators).

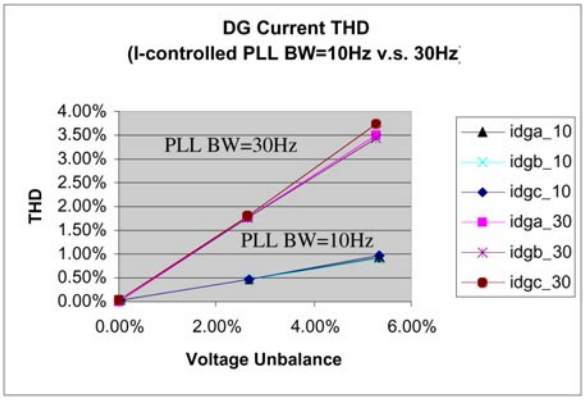


Figure 18. DG output current distortions with different PLL control bandwidth.

- The IEC standards only address 50 Hz 230 V systems. The equations used in the recommended approach are taken from IEC standard for European system. They need to be updated to be appropriate for the U.S. 120 V 60 Hz system.
- It has to be ensured that the DG does not inject DC current into the grid.
- Usually, the load zero-sequence impedance varies largely and cannot guarantee low impedance to meet grounding requirements. Therefore, a DG, whether connected through a transformer or directly connected to the grid, should provide a sufficiently low zero-sequence impedance in order to have an effective ground.
- For a DG with a transformer, the transformer can normally provide the effective ground. There is a trade-off between grounding requirement and system disturbance rejection requirement in the design of the transformer zero-sequence impedance.
- For a DG without a transformer, special attention should be paid to the zero-sequence impedance design so that effective ground can be provided. Unlike the DG with a transformer providing the effective ground passively, the DG without a transformer must shape the zero-sequence impedance characteristic using an active control approach.
- Grid voltage unbalance will require predominantly 120 Hz ripple power from the DG. Due to the ripple power, the DG DC bus capacitor should be sized appropriately in order to limit voltage ripple and consequent impact on other DG equipment such as batteries and generators.
- The ripple current i_{dc} is proportional to the degree of unbalance (negative-sequence voltage over positive-sequence voltage).
- With a conventional dq-frame PLL, higher bandwidth will cause higher 120 Hz ripple component in the PLL output ω, and higher output current THD.

4. Protection and Reliability Case Studies

The power system will impose a complex set of conditions upon DGs. The response of DGs to those conditions, especially system faults, will dictate how DGs are integrated. In this section, a range of normal power system stimulus are applied to DGs and their behavior is observed. The possible impact on the performance and reliability of the EPS is explored and potential problems, benefits, and improvements are noted.

4.1 TRANSIENT RESPONSE AND FAULT BEHAVIORS

4.1.1 Capacitor switching

Capacitor switching is a normal operation for a utility system. The transients associated with these operations are generally not a problem for utility equipment.[17] These low frequency transients, however, can be magnified in a customer facility or result in a nuisance tripping of power electronics based devices, such as adjustable-speed drives (ASDs).[18]

Transient overvoltage and over current related to capacitor switching can be characterized by peak magnitude, frequency and duration. These parameters are useful indices for evaluating potential impacts of these transients on power system equipment.

Case studies have been performed to investigate the impact of capacitor switching on the DG-enhanced distribution system. Figure 19 shows the system diagram with one-line representation. To observe worst-case scenarios, no load is connected to the feeder.

The following cases were studied:

- Switching in the capacitor when V_{feeder} (phase A) is at its peak
- Switching in the capacitor when V_{feeder} (phase A) is at its zero-crossing
- Switching in the capacitor when V_{feeder} (all phases) is at its zero-crossing
- Switching in the capacitor *without DG* when V_{feeder} (phase A) is at its peak

Switching in the cap when V_{feeder} (one phase) is at its peak

All three phase capacitors switched in at t = 237.55 ms, when phase A voltage is at its peak.

Figure 20 shows the three-phase feeder voltages. Initially, all three-phase voltages jump to zero because capacitor voltage cannot change instantaneously. Then the phase A voltage overshoots to nearly 2 p.u. Theoretically, it can reach 2 p.u. But due to damping from system losses, the overshoot is normally less than 2 p.u. This particular case shows relatively light damping of the transient because the

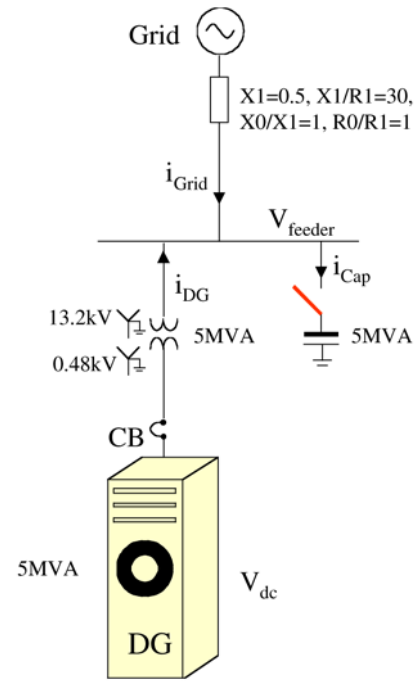


Figure 19. System diagram for capacitor switching case study.

model reflects a situation where the switched capacitor is near to a substation, and the system impedance is dominated by the low-loss impedance of the primary substation transformer and there are no loads modeled. In a more typical situation, the overshoot will be less than shown in this case. The whole dynamic takes about less than two cycles to settle down. The oscillation frequency is around 400 Hz.

The transient overvoltage may cause DG input DC bus overvoltage. The DC bus voltage has been reported in adjustable-speed drives (ASDs) application.[18] This phenomenon, however, is not observed in the DG case, as shown in Figure 21. The voltage overshoot is less than 0.5%, which is far below the design margin. The ratings of DC bus capacitor and switches are at least 10% higher than rated DC bus voltage.

The reasons for the different responses between adjustable-speed drives (ASDs) and DG are described below.

- For ASDs, the line AC voltages are the input to ASDs rectifier, typically a diode or thyristor rectifier. The transient overvoltage at the AC side can be directly reflected by the DC side. Therefore, the DC bus overvoltage can be as high as nearly 2 p.u. Due to the fact that the DC bus capacitance will be smaller on an ASD, com-

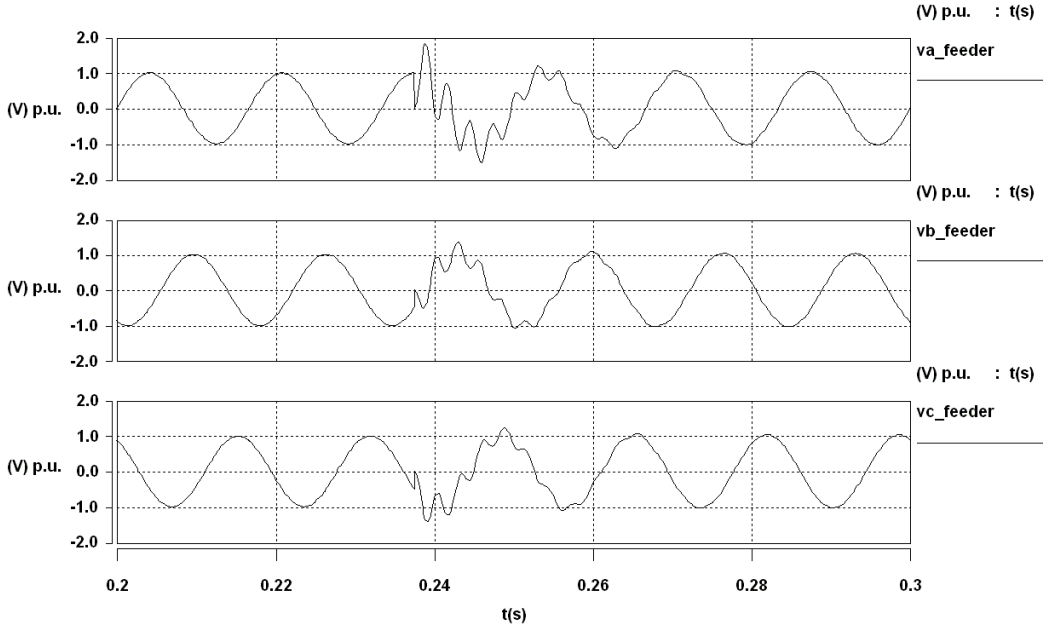


Figure 20. feeder voltage after switching in the capacitor when phase A is at its peak.

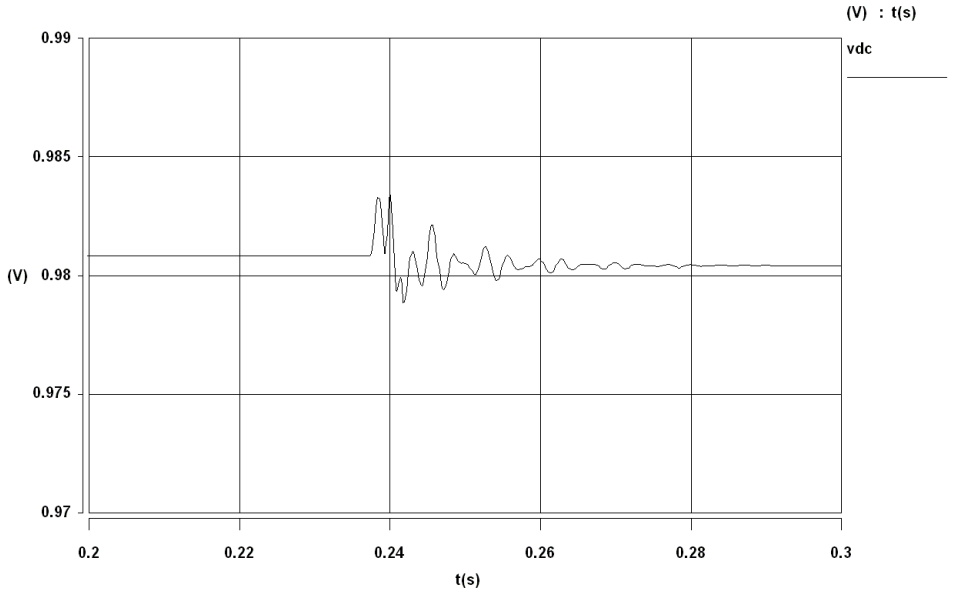


Figure 21. DG DC bus voltage (p.u.).

pared to a PWM DG inverter, the ASD will be more vulnerable to dc-link overvoltage trip.

- For DG, the line AC side is DG's inverter output. The DG is controlled as a current source to the grid. The grid voltage is the only input for PLL synchronization. Usually, PLL has a low pass filter and its bandwidth is much lower than line frequency. Therefore, the transient overvoltage and high-frequency (in this case, 400 Hz) oscillation will not affect the DG significantly. The PWM inverter simulated in this case uses controls (include current control and PLL) in dq frame. If the controls are based on zero-crossing in abc frame, then the DG may be more vulnerable to the transient distortion.

Switching in the cap when Vfeeder (one phase) is at its zero-crossing

When the capacitors switch in at phase A voltage zero-crossing, there will be a less severe transient phase A voltage and current. However, the transients in the other two phases are more pronounced, and can also reach nearly 1.8 p.u. overvoltage. There is no significant difference between this case and the previous case.

Switching in the cap when Vfeeder (all phases) is at its zero-crossing

To minimize the transient, a synchronous capacitor switch might be used.[19] Synchronous switching is used more frequently in transmission systems, and is not very common on distribution systems.

The waveforms in Figure 22 and Figure 23 show significant improvement in the transient behavior.

Switching in the cap without DG when Vfeeder (phase A) is at its peak

The event of switching capacitor without DG is also simulated to compare the transients with the case having a DG. Figure 24 shows the feeder voltages for both cases. It can be seen that the DG adds additional damping to the transient. Typically, the DG has nearly infinite impedance at 60 Hz due to its current regulation. However, the transient frequency (400 Hz in this case) is not within DG's current regulation bandwidth. Therefore, the DG has a finite impedance at the transient frequency which provides some beneficial damping effect. This damping is likely to be much less significant than the damping provided by loads.

Conclusions

- Energizing a shunt capacitor bank from a predominantly inductive source can result in an oscillatory transient that can ideally approach twice the normal system voltage. The problem can be minimized by synchronous control of the capacitors. Synchronous closing, however is only occasionally applied on high-voltage transmission systems, and not a common practice in distribution systems.
- Because capacitor voltage cannot change instantaneously, energization of a capacitor bank results in an immediate drop in system voltage toward zero, followed by an oscillating transient voltage superimposed on the 60 Hz fundamental waveform. The peak voltage magnitude depends on the instantaneous system voltage at the instant of energization, and can reach two times of the normal system voltage under worst-case conditions. The transient frequencies generally fall in the range of 300–1000 Hz, depending on the inductance of the system and capacitor bank ratings.
- Transient overvoltage due to capacitor switching is generally just below the level at which utility distribution system surge protection, such as arresters, begin to operate. However, these transients will often be coupled through step-down transformers to customer equipment. While the impact of the transient on some load, such as ASDs, is significant, its impact on DG can be minimal due to the nature of the DG control and operation.
- While the switching capacitor has little impact on DGs dynamics, one noticeable benefit of DG during capacitor switching is that DG adds additional damping to the transient. The dynamics of the event with DG is noticeably improved comparing with those without DG.

4.1.2 Fault analysis

The impact of DG units on fault currents can be significant. This can affect the reliability and safety of the distribution system. The fault behavior of rotating generators is well known and well documented.[20] Newer DG technologies will predominantly be of the power electronic variety. Hence, this study focuses the behavior of power electronic DGs during fault in the utility system. The DG considered for this study is a 3-phase 4-wire with a delta-wye transformer at the DG output. The DG inverter is current controlled to inject the required real and reactive power into the grid. It is normally controlled as unity power factor, thus the reactive power reference is zero.

The fault contribution from a single small DG unit is not large, however, the aggregate contributions of many small units, or a few large units, can alter the short circuit levels enough to cause overcurrent protection (fuse-breaker) miscoordination,

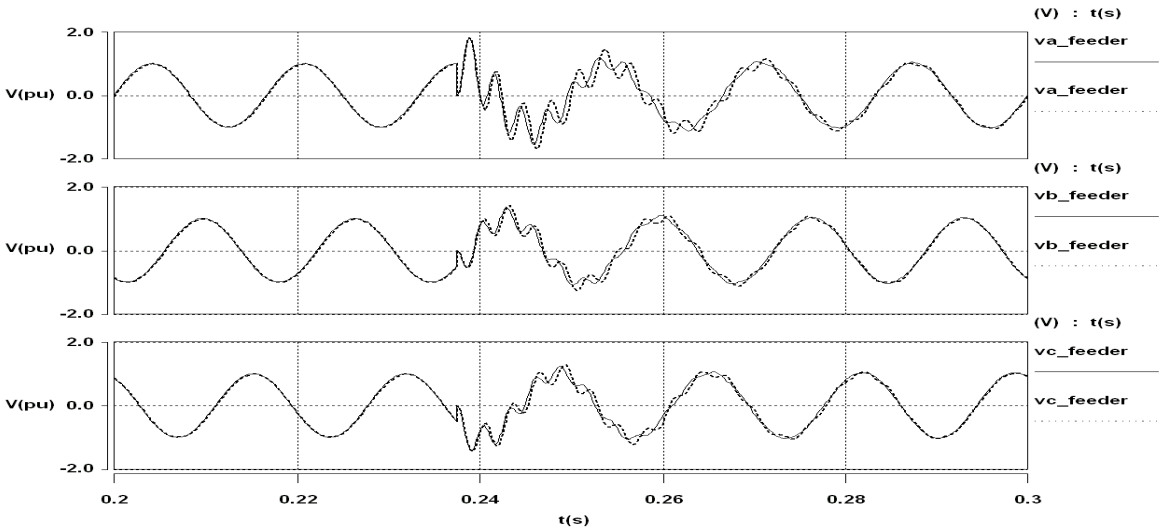


Figure 24. Transient dynamics with (solid line) and without DG (dotted line).

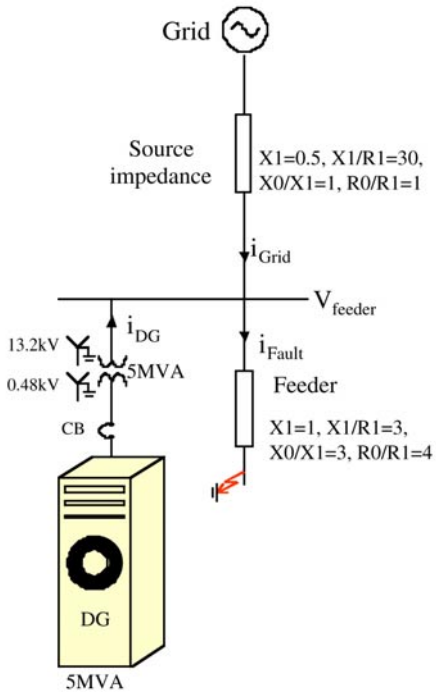


Figure 25. One-line diagram of the system under study.

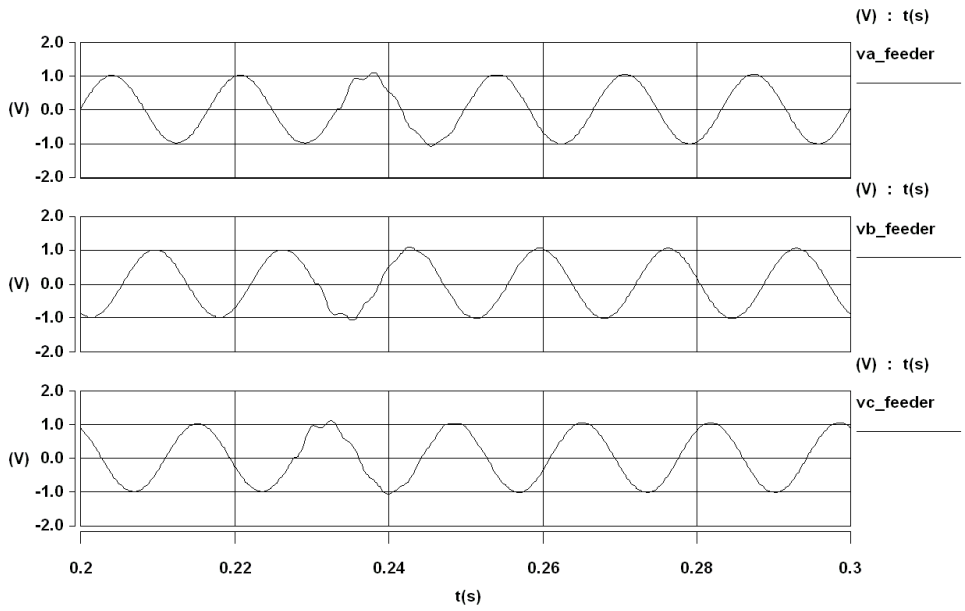


Figure 22. Feeder voltage when capacitor switch in at all phases voltage zero-crossing.

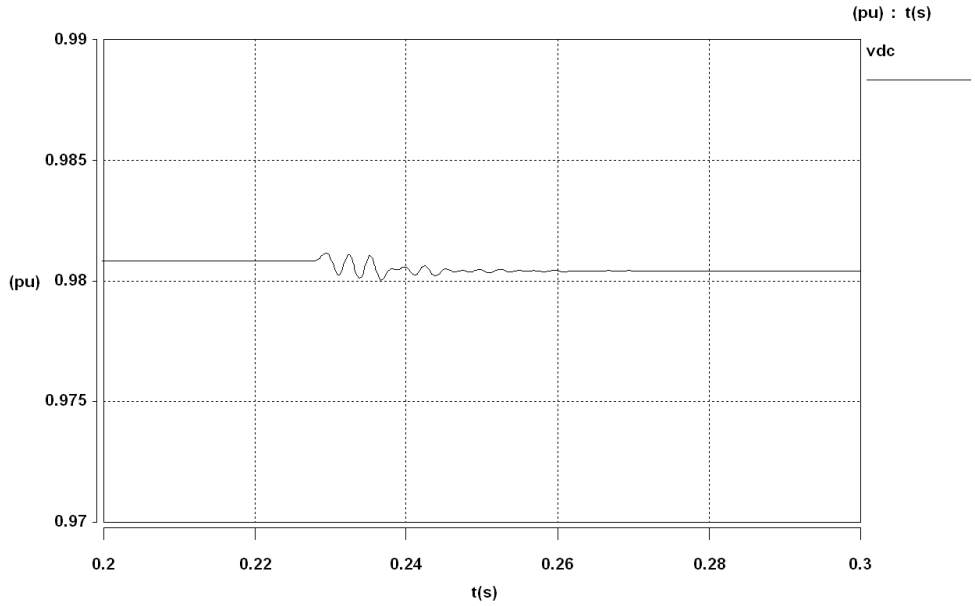


Figure 23. DG DC bus voltage when capacitors switch in at all phases voltage zero-crossing.

excessive fault currents, nuisance fuse operation, and hamper fault detection. For example, normally it will take five to six cycles for the upstream breaker using an instantaneous trip setting to clear a fault, hence a fuse needs to be sized so that its minimum melt time is longer than the total breaker fault clearing time (must be at least six cycles plus some margin time). If the fault current increases due to DG contribution to the fault current, its minimal melt time may be significantly shorter than six cycles and it will no longer coordinate with the circuit breaker. The coordination of the fuse and the time overcurrent relay at different fault current level is critical to power system protection. It is possible for the DG to maintain voltage on a distribution feeder and reduce the fault current level at the substation. This can further delay the operation of the time overcurrent relay. Some utilities have a policy where they would prefer a down stream fuse to open and thus prevent disruption on the rest of the distribution feeder. This study is focused on the fuse saving strategy previously discussed. However, fault current contributions of the inverter-DG under different conditions are studied and compared to those of an induction motor load.

Figure 25 shows the system under study with one-line diagram. The following cases were studied:

- Three-phase ground fault with DG
- Single-phase ground fault with DG
- Three-phase ground fault with DG and feeder fault (X1=0)
- Three-phase ground fault with induction machine

The system with both high source impedance and low source impedance is studied.

Three-phase to ground fault with DG

The fault occurs at the remote end of the feeder. The fault lasts for 0.2 s and is then cleared. Figure 26 shows the fault, grid and DG currents. Since the DG is current controlled, it will supply constant current with a short transient when the fault occurs and clears. It can be seen that the grid supplies the majority of the fault current.

During the fault, the feeder voltage will drop. The voltage drop is dependent on the fault impedance and the line impedance to the point of fault occurrence, which is proportional to the distance of the fault. In this case, the voltage drop is not large or long enough to trip the DG. The DG under/overvoltage trip settings are based on P1547 requirements. Figure 27 shows per-cycle I^2t of the fault, grid and DG currents. The per-cycle I^2t is calculated every period of the fundamental output current. The per-cycle I^2t value provides information on the coordination of the fuse and time-overcurrent relay in the system.

In this case, the DG fault current contribution is only a very small fraction of the total fault current. Therefore, it is not likely to affect fuse-breaker coordination. It has also been studied that the DG fault current contribution has a larger percentage with higher DG penetration and under weaker line conditions.

Single-phase to ground fault with DG

Figure 28 shows the fault, grid and DG currents during a single-phase fault. It is found that the DG current contribution to the fault is slightly larger than that due to the three-phase fault. This is due to the DG delta-wye transformer, which provides a path for zero-sequence current. The zero-sequence currents of DG, grid, and fault are shown in Figure 29. The magnitude of the zero-sequence currents depends on the X0 to X1 ratio.

Similarly, during the single-phase fault, the I^2t contribution of the grid and the fault are almost identical. The I^2t of the DG is miniscule by comparison.

As a conclusion, under both three-phase and single-phase fault, the inverter-based current controlled DG has little impact on fault contribution and fuse-saving strategy.

Three-phase to ground fault at the feeder. (X1=0)

When the fault is right at the feeder (X1=0 for the feeder in Figure 1) where the DG is connected, the DG will trip due to undervoltage. The tripping time for voltage under 50% is user defined but the maximum is 0.16 s as required in P1547. This maximum limit is to ensure that the DGs are offline before any recloser action. Disconnecting the DGs too fast can reduce the benefits to the power system provided by the DG during faults, as described in the "Power systems dynamics and stability" case study section. Figure 30 shows the per-cycle I^2t contribution at the fault, grid and DG. Again, the fault current contribution is predominantly from the grid. The DG's current contribution, which is already small, is further reduced when the DG trips off-line.

Three-phase to ground fault with induction machine

Utilities have experience evaluating the impact of motor loads on the distribution feeder fault current. Hence, a study was carried out to compare the DG with an induction machine load at the same power level. The machine considered in the case study is an aggregate of many small machines. The parameters of the individual machine are listed in Table 3.

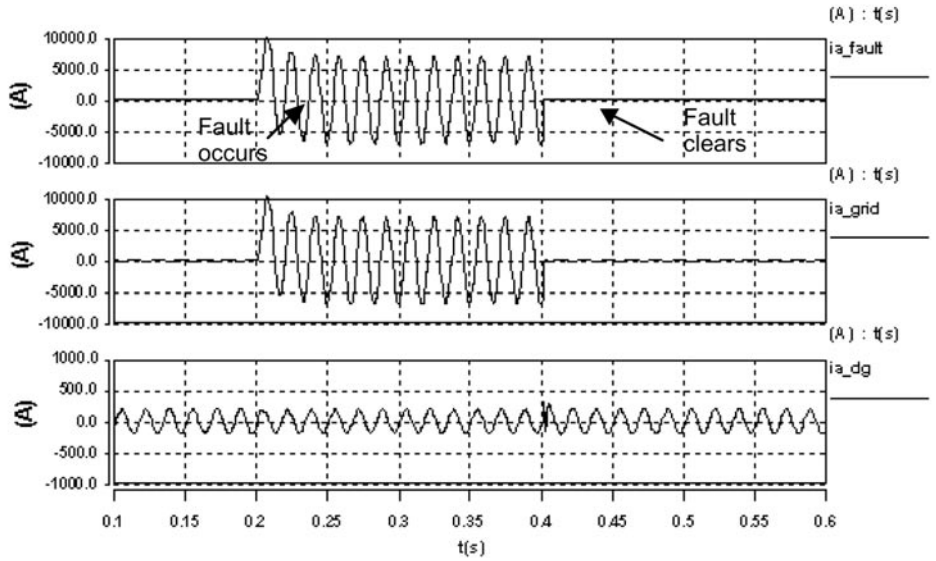


Figure 26. Feeder, grid and DG high side phase A current during fault.

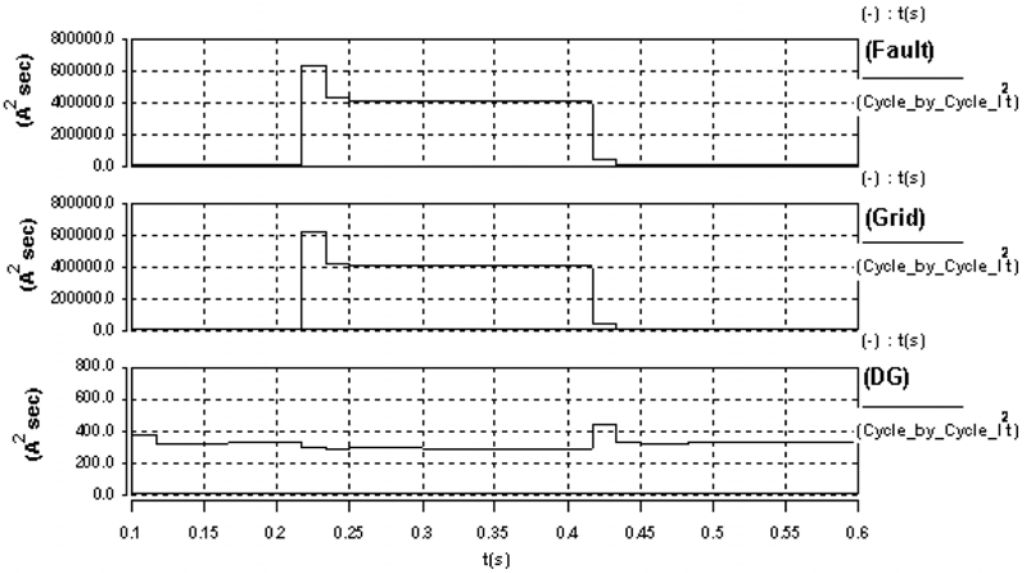


Figure 27. Cycle-by-cycle I^2t contribution from feeder2, grid and the DG.

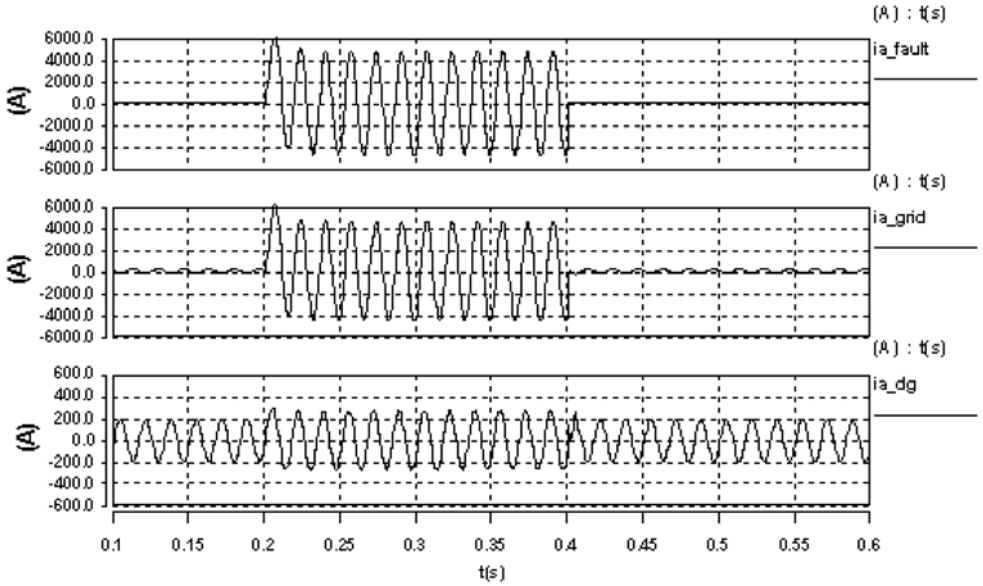


Figure 28. Feeder, grid and the DG high side current on the faulted phase.

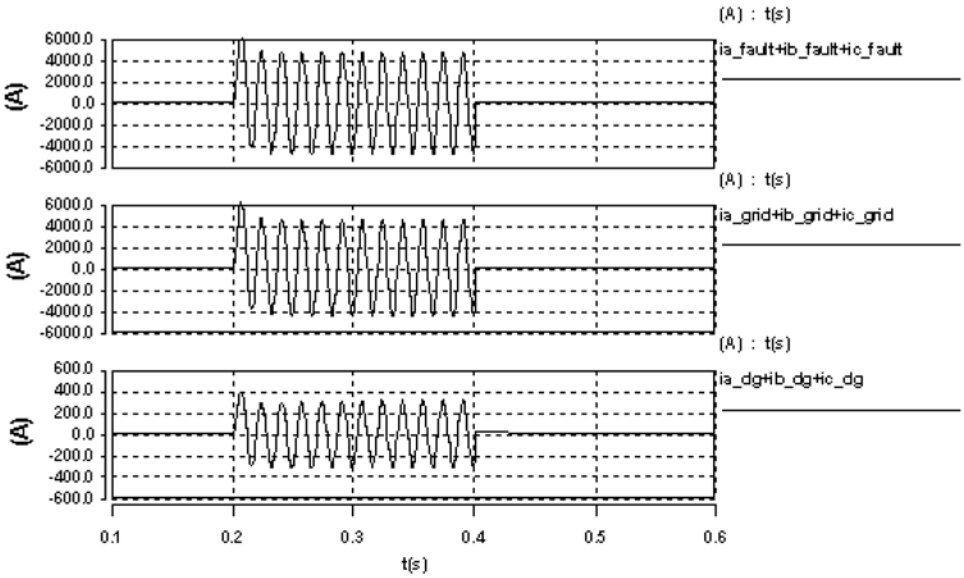


Figure 29. Zero sequence currents of fault location, grid and DG.

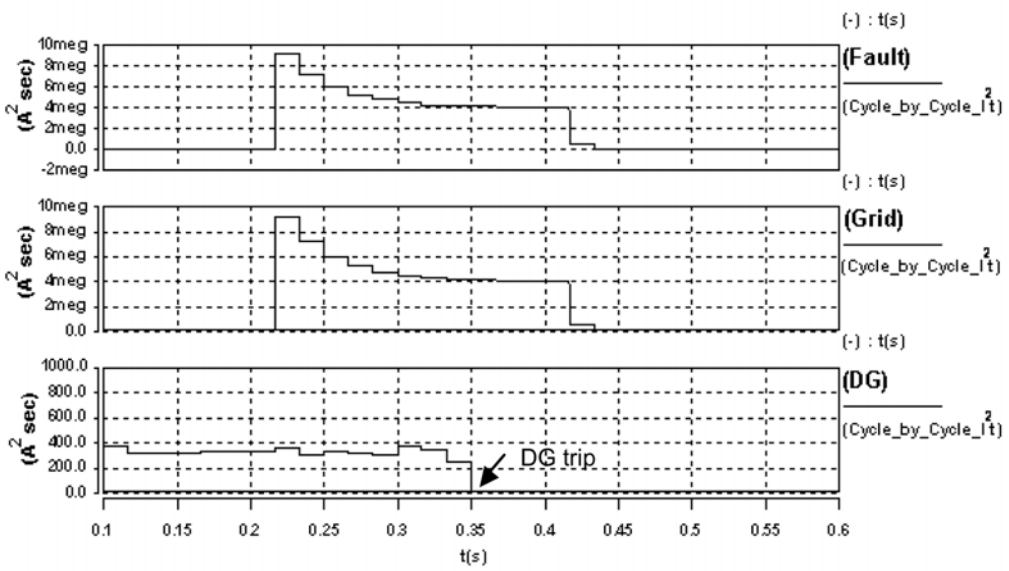


Figure 30. Cycle-by-Cycle I^2t contribution during fault at the feeder, grid and the DG.

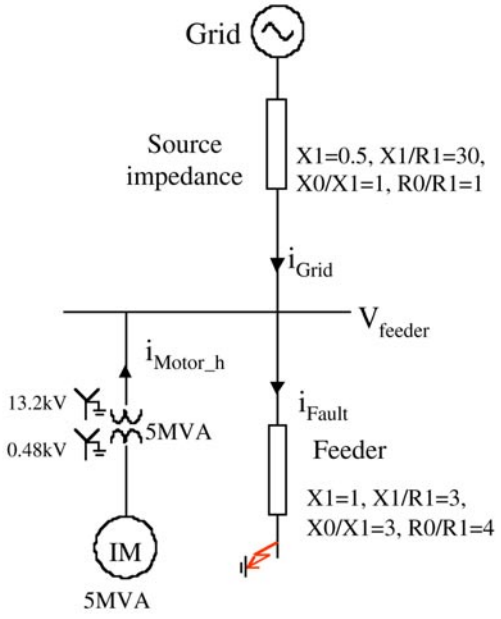


Figure 31. One-line diagram of the system for fault studies with induction machine load.

Table 3 Parameters of the induction machine

Vll_rated	480 V
Power	15 hp
Rs	0.0301 pu
Rr	0.0064 pu
Xm	2.3120 pu
Xls	0.0665 pu
Xlr	0.0116 pu
Jpu	2.6672 s
Dpu	0.0197 pu

The machines are connected in a three-phase three-wire configuration. The machine models include both stator and rotor flux dynamics. Magnetic saturation is not captured in the simulation. The modeled mechanical load has a quadratic speed-torque relationship. Figure 31 shows the one-line diagram of the system under study.

Figure 32 shows the fault, grid and motor (transformer high side) currents. It can be observed that the motor phase current has a phase jump at the beginning of the fault, signifying that the motor momentarily feeds power into the grid. There is an initial drop in the current magnitude because of the drop in the voltage magnitude. However, it can be observed in Figure 33 that the per-cycle I^2t increases as the fault proceeds because of the increased motor slip, caused by the sag in the motor terminal voltage. Once the fault is cleared, the terminal voltage increases leading to an inrush into the induction machine. Figure 34 shows the motor torque and speed response to the fault. It is clearly seen that the fault current contribution from motor is larger than inverter-DG.

4.1.3 Summary

The I^2t contributions of the DG and the grid into the fault are summarized in Table 4 for the various cases studied. These values represent the contribution during the fault condition in the system.

Table 4 Comparison of the I^2t contribution [1] during the different fault cases

	Fault	Grid	DG/IM
With DG & low source impedance	5.13 Meg	4.99 Meg	3348
Without DG & low source impedance	5.1 Meg	5.1 Meg	0
With Induction Machine	5.04 Meg	5.3 Meg	15873
With DG & high source impedance	**407**	**277.5**	**35.85**
Without DG & high source impedance	**377**	**377**	**—**
Single phase to ground fault	2.35 Meg	2.14 Meg	7246

1. I^2t has been calculated over a 200ms fault duration

As can be noted from the above table, for the case with the low source impedance, the contribution of the DG is negligible. However, for the case, where the grid connection is through a weak line (highlighted rows), there is a significant reduction in the I^2t contribution by the grid with the DG present in the system. This might affect the fuse coordination in the EPS, especially for the case of large DG penetration.

4.1.4 Conclusions

- Current output from the inverter-DG remains at the load current setpoint, except for a minor and brief transient.
- For inverters, the fault contributions will depend on its operating current level and the DG under voltage protection trip settings.
- The single-phase fault will cause zero-sequence current in a four-wire system. Because of the zero-sequence current, the faulted phase DG current is larger than the one with balanced three-phase fault.
- For induction motors, the significant current lasts only a few cycles and is determined by dividing the pre-fault voltage by the transient reactance of the machine. The fault current contribution is usually much larger than that of current controlled inverter-DG. It is common practice to ignore the fault current contribution of induction motor loads, particularly small, distributed motor loads, in distribution overcurrent conditions. The results show the DG is much smaller than that of the motor loads. Thus, there is ample precedent for considering current-controlled inverter-based DG as an insignificant short circuit current condition. However, the fault impact of DGs needs to be reevaluated in case the DG controls are

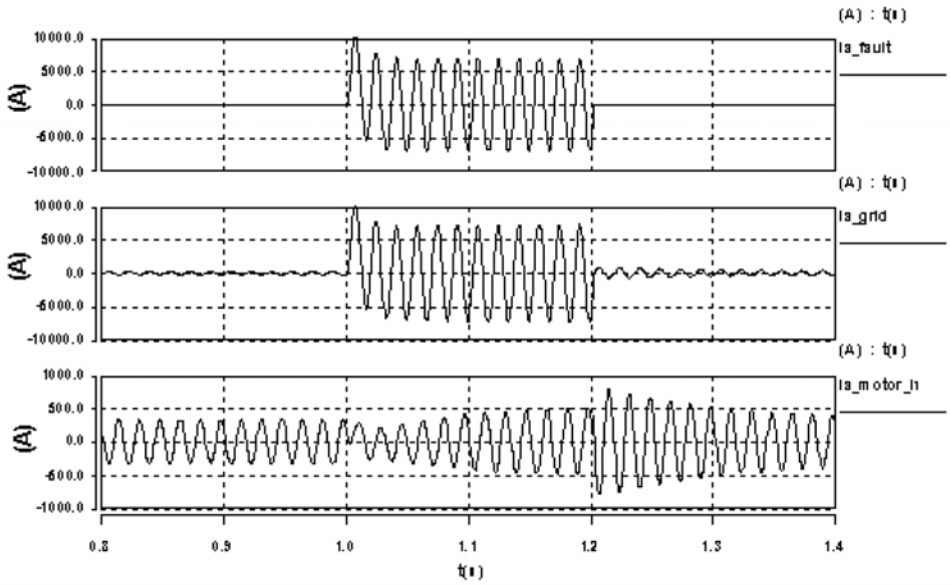


Figure 32. Currents in feeder, grid and motor transformer high side during the fault event.

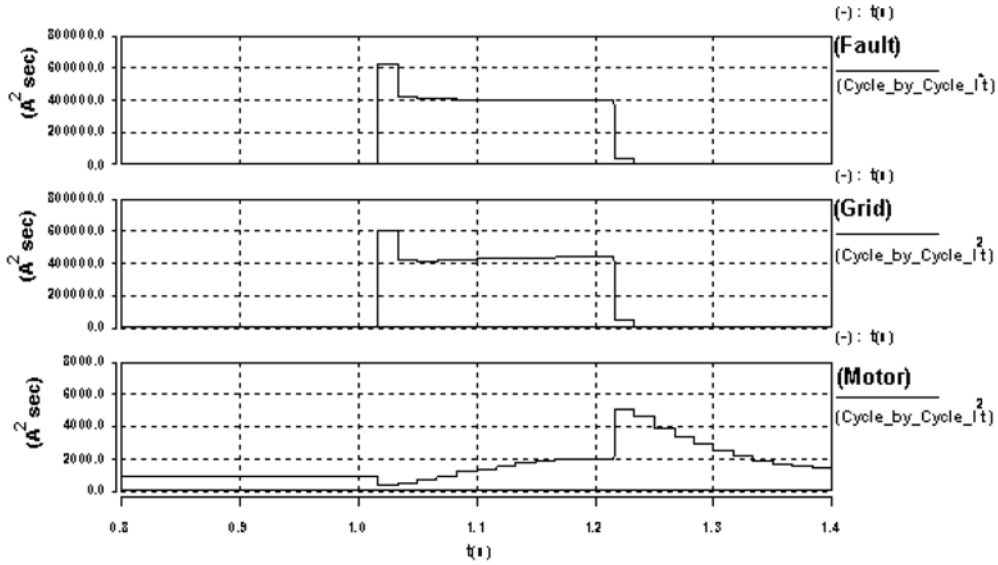


Figure 33. Cycle-by-Cycle I^2t contribution in the feeder, grid and induction motor high side during the fault.

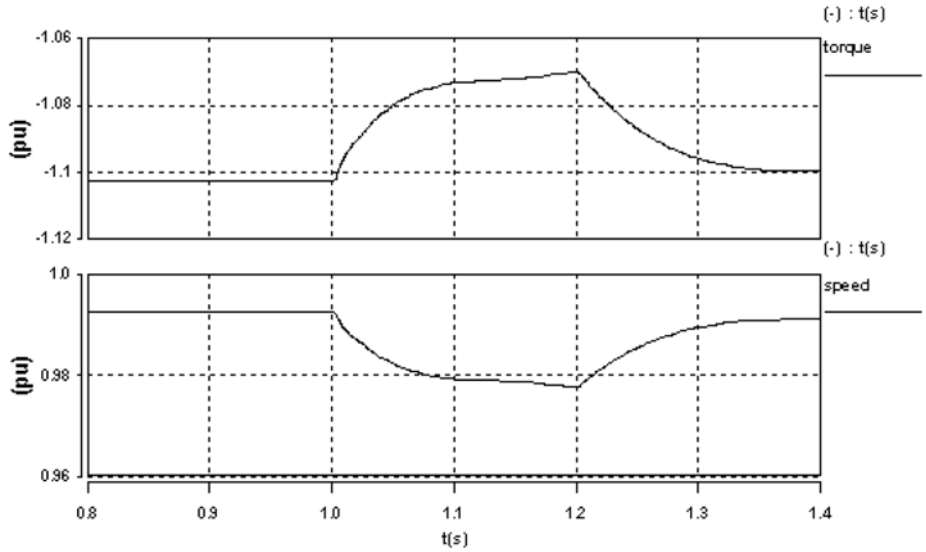


Figure 34. Machine torque and speed during the fault.

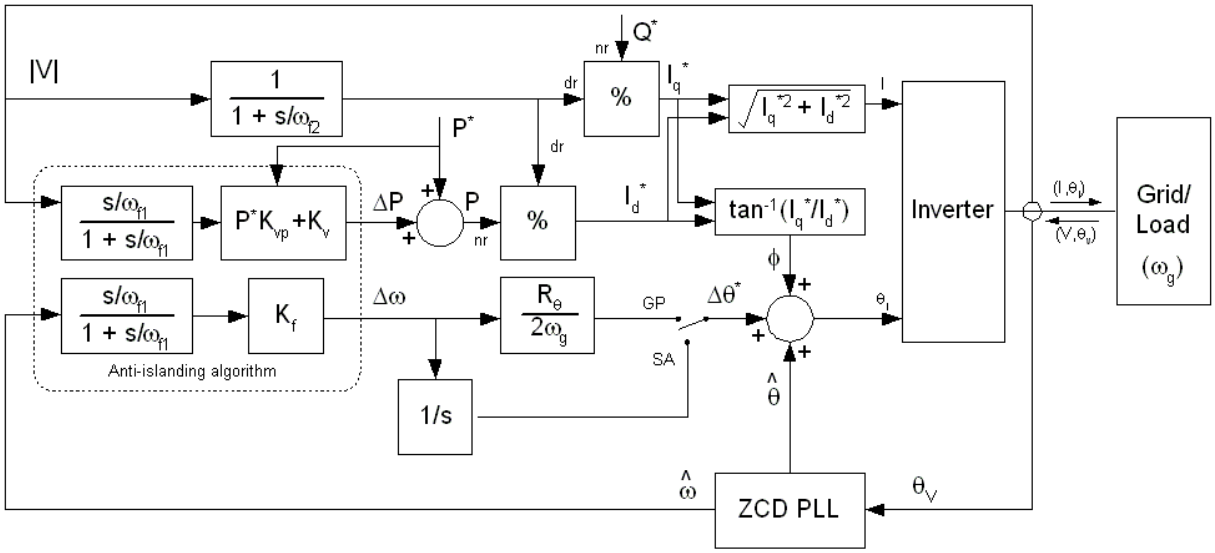


Figure 35. GE's interpretation of the block diagram representation of the Sandia anti-islanding algorithm.

changed to accomplish other functions such as voltage support.

- I^2t contributions for weak system might be concern with increased DG penetration.
- Modern inverter-based DGs do not contribute to system fault current beyond the pre-fault operating current level. However, the current contribution of the DG system to a single phase fault may be greater than the three phase case which conflicts with IEEE P1547 requirement that ground fault current contribution of a DG shall not be greater than 100% of the fault current contribution of the DG to a three phase fault. This is because the DG is a nearly ideal current source for the positive sequence, but is generally a constant impedance or voltage source for the zero sequence. Both are desirable characteristics, and the result reveals that the wording of P1547's single-phase to three phase fault current ratio requirement is more appropriate for conventional rotating generators. The wording of this requirement needs additional consideration with respect to its consistency with inverter-based applications.

4.2 ANTI-ISLANDING PROTECTION OF DG

Islanding of a grid connected DG occurs when a section of the utility system containing such generators is disconnected from the main utility, but the independent DGs continue to energize the utility lines in the isolated section (termed as an island). Unintended islanding is a concern primarily because it poses a hazard to utility and customer equipment, maintenance personnel and the general public. Poor power quality can damage loads in the island. Another concern is the out of phase switching of the recloser leading to damage to the DG, neighboring loads and utility equipment. Any feature available to reduce the run-on time of an islanded system can be termed as "anti-islanding."

Many techniques have been proposed to prevent islanding caused by DGs.[24,25] An algorithm proposed by the Sandia National Laboratories is analyzed in this study because it is considered to be effective. Sandia's active islanding algorithms had been developed for single-phase inverter units. The algorithm consists of the Sandia frequency shift (SFS) and the Sandia voltage shift (SVS) schemes. The principle behind both the methods is an accelerated frequency and voltage drift respectively created with positive feedback. In the presence of the utility, the frequency and voltage shifts are not effective in drifting the two parameters. However, once the grid is disconnected, these methods force the frequency and/or voltage to shift outside the operating windows, causing the inverter to disconnect due to o/u voltage and frequency protection.

Since these were originally developed for a single phase inverter, the technique adopted to measure frequency is based on the zero crossing of the voltage waveform, and the voltage magnitude is obtained from RMS calculations. This method has been extended to three phase DGs by GE and has been studied under the NREL contract.

4.2.1 Analysis of Sandia anti-islanding algorithm

A block diagram representation of the Sandia's algorithm is shown in Figure 35. The first step is to determine the gain settings for the Sandia voltage scheme (SVS) and the Sandia frequency scheme (SFS) algorithms. The critical gains of the Sandia anti-islanding algorithm are:

- K_f for the SFS
- K_{vp} and K_v for SVS
- ω_{f1} for the wash out functions
- ω_{f2} for the power regulation loop

The critical gains for SFS and SVS have to be determined for RLC loads (set according to IEEE P1547) so as to mitigate islanding situations. The gain settings of the algorithm, shown in Figure 35, have been obtained by performing a small signal analysis of the DG system with the tuned RLC load (according to IEEE 929 [2] and IEEE P1547 anti-islanding test specifications).

The algorithm gains are determined by investigating the open loop behavior as a function of frequency. The voltage magnitude and the phase signal flow paths were opened so as to obtain the SVS and SFS gains, respectively. The Sandia voltage and frequency schemes are explained in detail below.

Sandia's frequency shift (SFS) algorithm

The block diagram of the SFS algorithm is shown in Figure 36. The frequency estimate from the phase lock loop is passed through a washout function to determine changes in the ambient frequency. This information multiplied by the SFS gain, is added to the frequency reference of the current injected by the DG inverter. As the DG commanded frequency on average cannot be different from the grid frequency, the phase angle has to be periodically reset for meaningful power transfer from the DG to the rest of the grid system to occur. In the single phase case, this reset of the phase angle in the DG current reference waveform occurs at the voltage zero crossings.

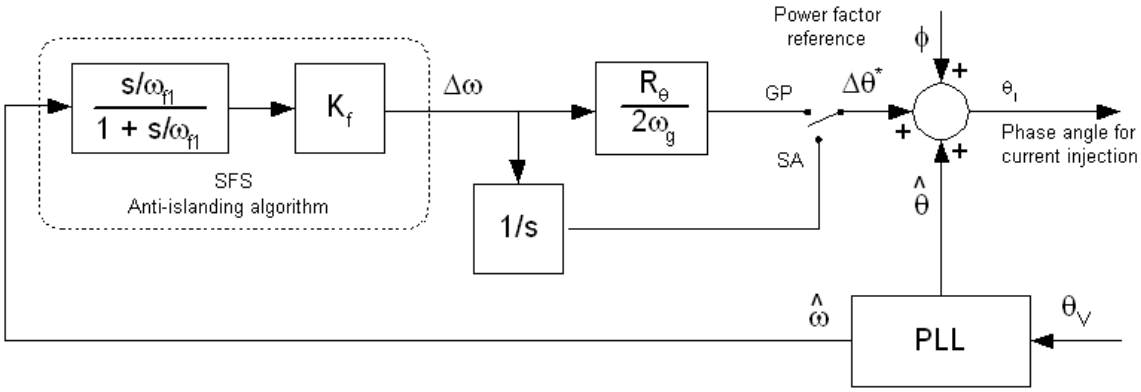


Figure 36. Block diagram highlighting the SFS component of the Sandia anti-islanding algorithm.

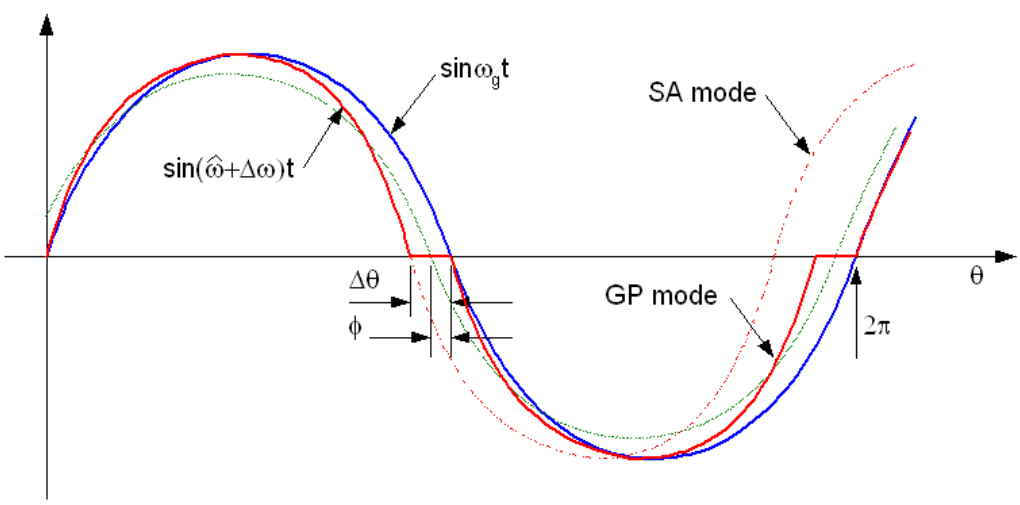


Figure 37. Nature of waveforms caused by the SFS algorithm.

In the SFS modification for a three-phase DG, the frequency of the system is determined using a continuous tracking Phase Locked Loop (PLL) in a synchronous reference frame. This frequency estimate is then passed through a washout, to determine the trend in system frequency. The change in estimated system frequency is multiplied by the SFS gain constant (K_f) to obtain the increment or decrement in the output frequency of the DG inverter's current injection into the grid.

The $R_\theta/2\omega_g$ block in Figure 36 is an equivalent representation of the actual DG system behavior that captures the change in the phase corresponding to the error in frequency. The derivation of this block in the grid parallel mode (GP) is based on the equivalent phase angle change (ϕ) calculated in response to a change in frequency ($\Delta\omega$) as a function of the system frequency (ω_g). This can be explained by considering the single phase implementation where the frequency command from the SFS is higher than the nominal frequency and reset period of 180°, as shown in Figure 37.

$$\Delta\theta = \frac{\Delta\omega T}{2\pi/R_\theta}$$

where, T is the period and R_θ is the reset angle. Simplifying for the period in terms of ω we get

$$\Delta\theta = \frac{\Delta\omega R_\theta}{\omega_g}$$

The effective phase shift $\phi = \Delta\theta/2$. For the situation of a 180° value for R_θ, the phase shift is given by

$$\phi = \frac{\Delta\omega\pi}{2\omega_g}$$

at 60 Hz the relationship is ϕ = 4.1666e-3 $\Delta\omega$.

In the stand-alone mode (SA), the phase angle error is the by integral of the frequency error. This is then added to the reference phase angle, and the power factor angle reference, to provide the reference command for the phase angle of the current injected by the DG. The magnitude of the DG current is determined by the SVS loop, as explained below. Note that the SA mode considered in this analysis is during the transition of from grid parallel mode. In this condition the grid has been disconnected but the DG has not yet made any decision for mode transition and continues to injects current out of its terminals.

Sandia's voltage shift (SVS) algorithm:

The block diagram of the SVS algorithm is shown in Figure 38. The input to this block is the magnitude of the system voltage. The error in the system voltage determines the shift in the reference power, to drive the DG voltage further away from the operating voltage range. The voltage magnitude, after a low pass filter, is also used to determine the magnitude of the reference current settings for the DG. This is to ensure that the desired level of real and reactive power is being delivered by the DG. As compared to the SFS, the gain in the feedback loop is not a constant, but is a function of the real power reference setting. This is to reduce the dependence of the SVS algorithm on the reference power setting.

The anti-islanding algorithm works by forcing the island with the DG to become unstable whenever the grid is disconnected. Hence, for the active anti-islanding to be effective, the open loop gain has to be greater than one. Once the SFS and SVS gains are obtained, the time domain simulations for RLC and motor loads are considered in order to verify the behavior of the algorithm using detailed three phase load and DG models. The next section interprets the characteristics of the SFS and SVS active anti-islanding algorithms based on frequency domain analysis.

4.2.2 Implications of the gains settings of the Sandia anti-islanding algorithm

One of the goals of the analysis of block diagram representation of the anti-islanding algorithm is to evaluate the dependence of the gain settings of the SFS and SVS on the type of load. Passive and active loads are considered. The gains should be designed for the worst case load for the schemes to be effective under all circumstances. R and RLC loads are evaluated for passive loading. High and low inertia three phase induction machines loads are evaluated for active loads. Driving induction machine loads with current source DG, without explicit speed control loops, are not feasible on a sustained basis.[26] This makes the task of evaluating the anti-islanding algorithm with induction motor loads, at different DG and load parameters, a challenging task using time domain small signal techniques. Hence this task is deferred to the section on time domain analysis. Therefore all the discussion below is for RLC loads with the L and C set so that the load has a quality factor of 2.5 as defined in IEEE 929 and IEEE P1547 testing requirements. For the purpose of analysis, the SFS and SVS loops are considered decoupled except at the load. The voltage magnitude fed back into SVS is held at the nominal value

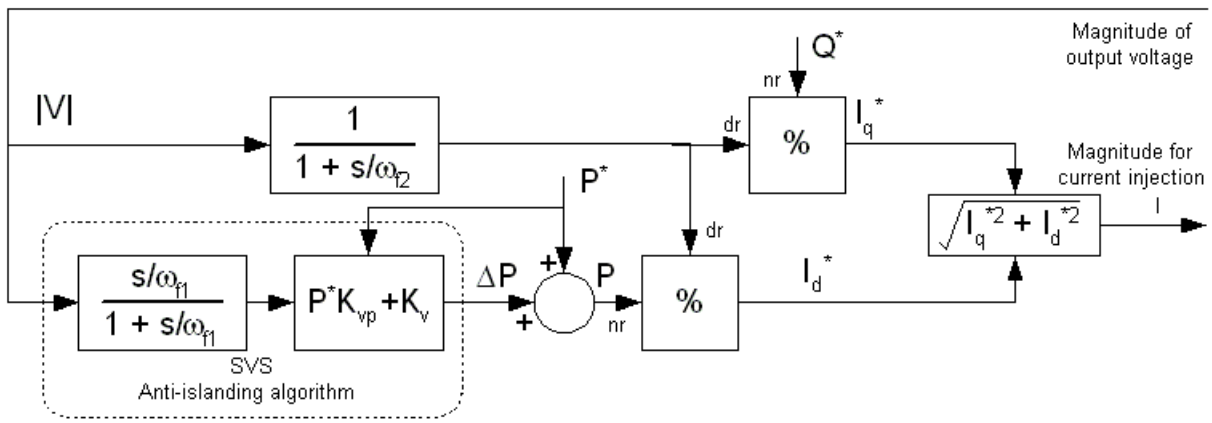


Figure 38. Block diagram highlighting the SVS component of the Sandia anti-islanding algorithm.

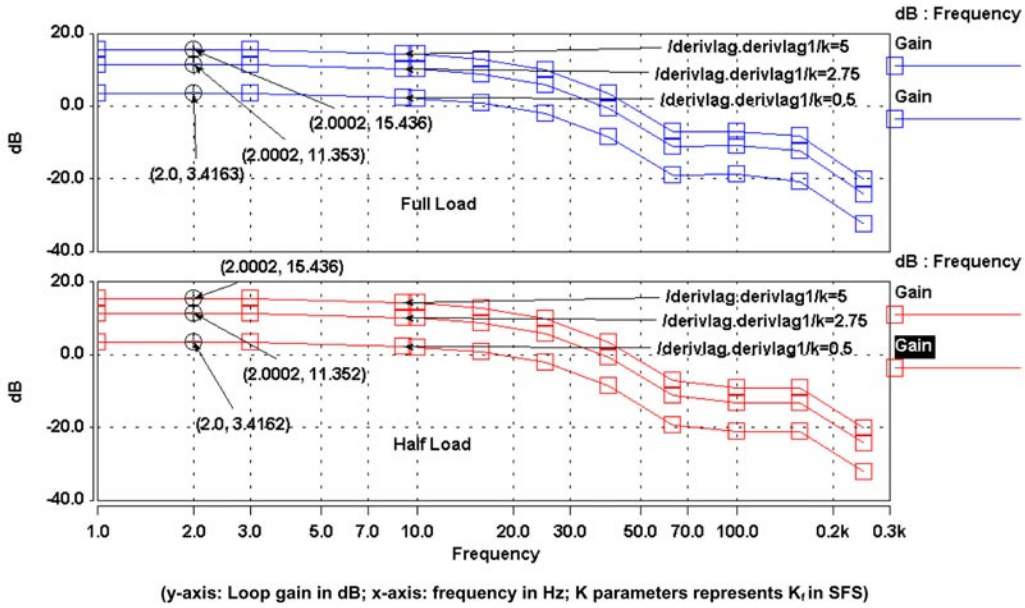


Figure 39. Loop gain of the SFS algorithm with RLC load at 50% and 100% power level.

during the study of SFS algorithms. The frequency measurement into SFS is held at the nominal value (60 Hz) during the analysis of the SVS algorithm.

Figure 39 shows the open loop gain frequency response of the SFS algorithm with the RLC load at 50% and 100% power level. The gains are the open loop gains obtained by breaking the θ_v signal flow path in Figure 35. All gains referred to in the analysis are calculated in per unit on the DG base. It can be seen the response is nearly flat for low frequencies (10 Hz and below) and droops down at higher frequencies. Gains greater than 0 dB are inherently unstable because it results in positive feedback under closed loop conditions with phase angle approximately zero (not shown in the plot). It can be observed that the load power levels did not affect the loop gain of the SFS algorithm. This implies that the power level of DG operation does not affect the SFS.

Similarly, Figure 40 shows the open loop gain frequency response of SVS algorithm. In this case the loop gains are obtained by opening the |V| signal flow path shown in GE's interpretation of the block diagram representation of the Sandia anti-islanding algorithm. The loop gain characteristics of the SVS algorithm is flat at low frequencies (below 5 Hz). The magnitude of the gain is higher than 0dB indicating that the SVS algorithm will be effective (i.e. unstable) for the gains shown in Figure 40.

Figure 41 indicates additional characteristics of the SVS loop gain, as a function of the gain constants K_v and K_{vp}. It can be observed that the SVS loop gain characteristics have a tendency to reduce as load is increased. At light loads, it can be observed that there is lower sensitivity of the SVS loop gain to variations in k_{vp} (keeping $k_v = 1$). It can be observed from Figure 41 that at overloads the SVS loop has lower sensitivity to k_v (keeping $K_{vp} = 1$). In general it was observed for all loads, there is a cross over of the dominant gain from K_{vp} to K_v at the value of 1. At full load, the loop gain follows the same path for variations in either K_v or K_{vp}. This can be explained by the fact that at rated load, the equivalent gain offered by the algorithm is just the sum of K_v and the product of K_{vp} and Power. At 100% power the gain in each of these paths equals unity.

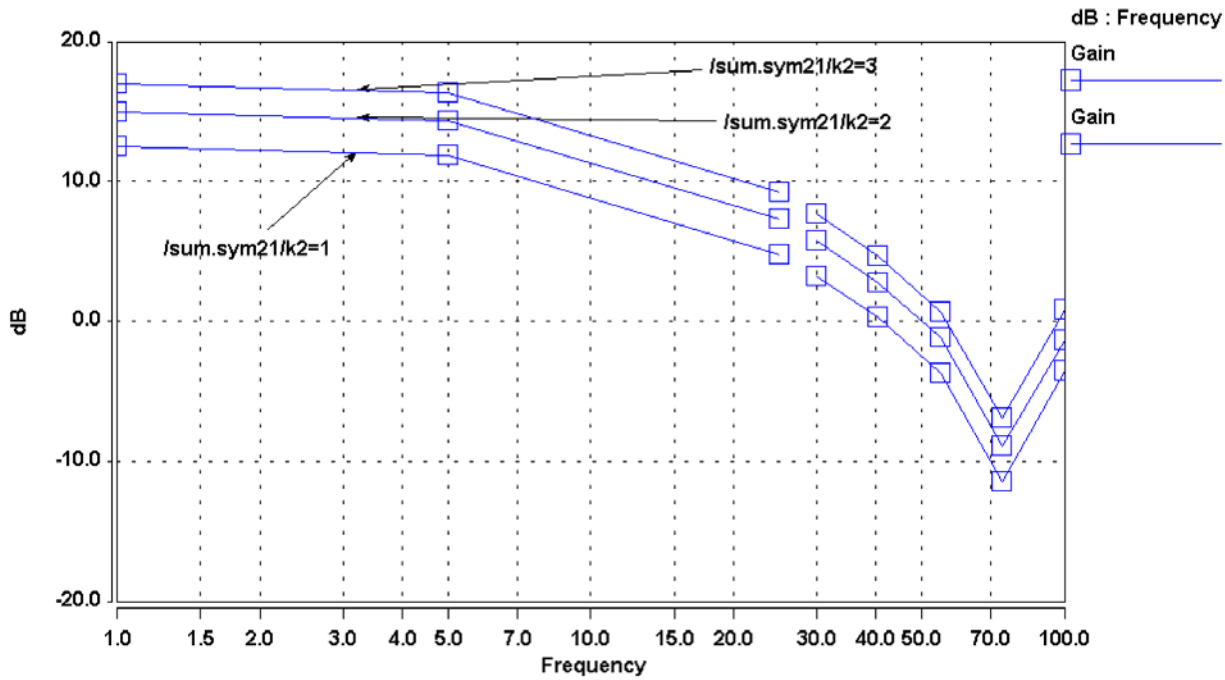
The plots on Figure 42 are obtained by keeping one gain (either K_p or K_{vp}) constant at 1pu and varying the other gain at different output power levels. Figure 42 (a) and (b) indicate that as the loading on the DG increases, the loop gain has a decreasing trend. This means that the SVS algorithm tends to be less effective for higher loadings. This can be explained because of the larger capacitor in the RLC circuit at higher loads, which makes it difficult to drift the voltage away from the nominal value. Ideally, the gains should have remained constant even for any change in power output.

Figure 42(c) shows the effect of increasing K_{vp} at different load levels. The curves at different power levels tend to converge as the gain is increased. Figure 42(d) shows the effect of increasing Kv at different load levels. The curves at different power levels tend to diverge as the gain is increased. Hence, an optimum tradeoff between K_v and K_{vp} has to be obtained that minimizes the sensitivity of SVS to load power level. The term K_{vp}, which multiplied by Power, tries to make it more insensitive to load power level when compared to using a single gain constant in the feedback path of the SVS as described in the explanation for Figure 41.

Figure 42 (c) and (d) indicate that higher the gain the higher the instability causing faster detection of an islanding situation. However, setting the gains too high leads to greater harmonic distortion in the DG load current.[27] Hence, a minimum acceptable gain has to be selected.

Washout and power regulation time constants

The schemes use a number of parameters (ω_{f1}, ω_{f2}, K_{vp}, K_v, K_f) that have to be set appropriately for the algorithm to operate properly. The corner frequency ω_{f1} is set to differentiate between a change in measured frequency or voltage due to variation in DG's operating point and other slow dynamics of the power system. Hence, ω_{f1} is set to 0.1 Hz. Hence, voltage or frequency changes that occur in a time of less that 10s can excite the anti-islanding algorithm. If the voltage or frequency change sustains for longer than 10 s then it is considered a change in the nominal operating condition. The corner frequency ω_{f2} is set to 0.01 Hz. This is used to filter the measured voltage amplitude, which is then used to obtain the current command from the power command. In case the DG terminal voltage rises, the anti-islanding algorithm tries to increase the power command, while the power regulation loop through ω_{f2} lowers the reference current magnitude to maintain constant real and reactive power level. The corner frequency of ω_{f2} has been set to be decade lower than wf1 in the anti-islanding algorithm, so that the change in current magnitude due to voltage regulation and anti-islanding do not counteract each other. The setting of 0.01 Hz corner frequency will also allow the DG prime mover to respond and change its power level in a time frame



(y-axis: loop gain in dB; x-axis: in Hz; K parameters represents Kvp in SVS)

Figure 40. Loop gain of the SVS algorithm for varying K_{vp}, with K_v = 1, for RLC loads.

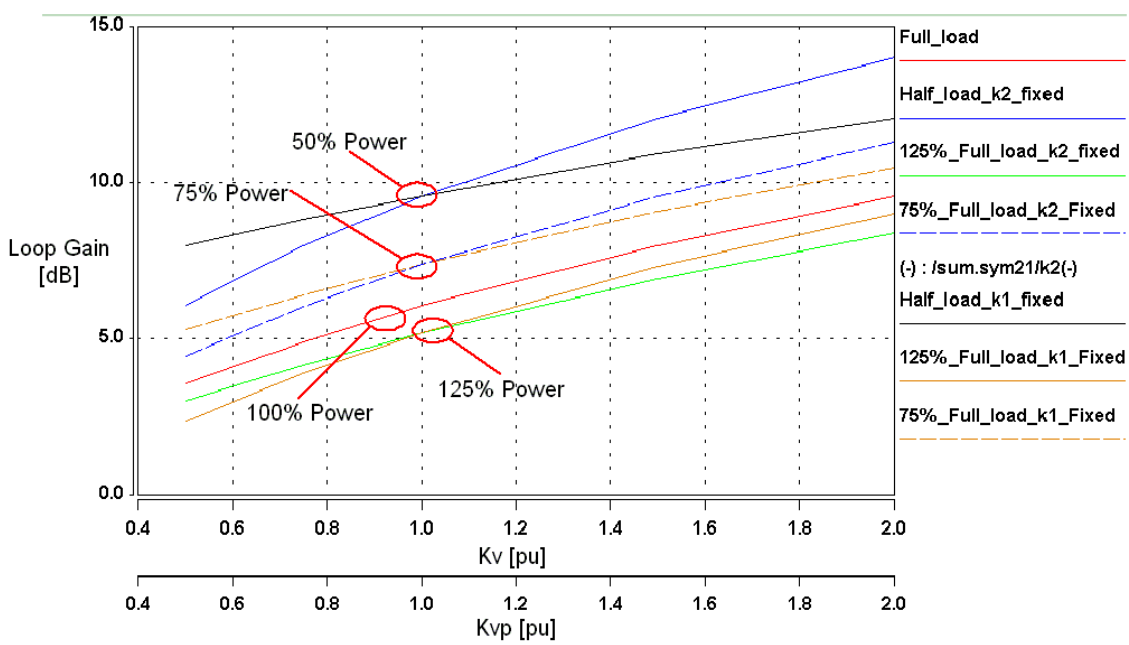


Figure 41. Variations of loop gain in dB at 2 Hz at varying load power level and gain constants for SVS.

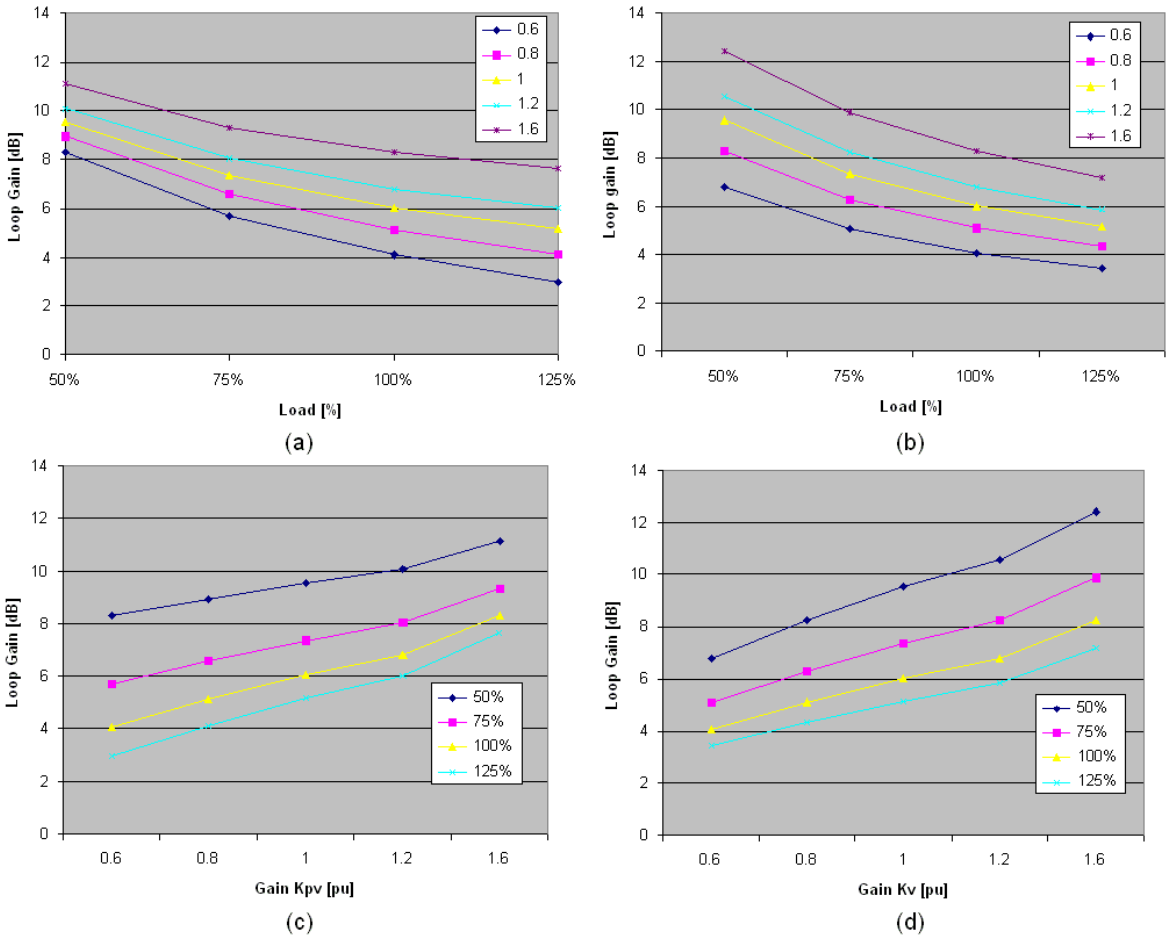


Figure 42. Influence of load and gain constants on the SVS loop gain. \(a) Effect of load [%] on loop gain [dB] at various Kvp [p.u.]. (b) Effect of load [%] on loop gain [dB] at various Kv [p.u.]. (c) Effect of Kvp gain [p.u.] on loop gain [dB] at various loads [%]. (d) Effect of Kv gain [p.u.] on loop gain [dB] at various loads [%].

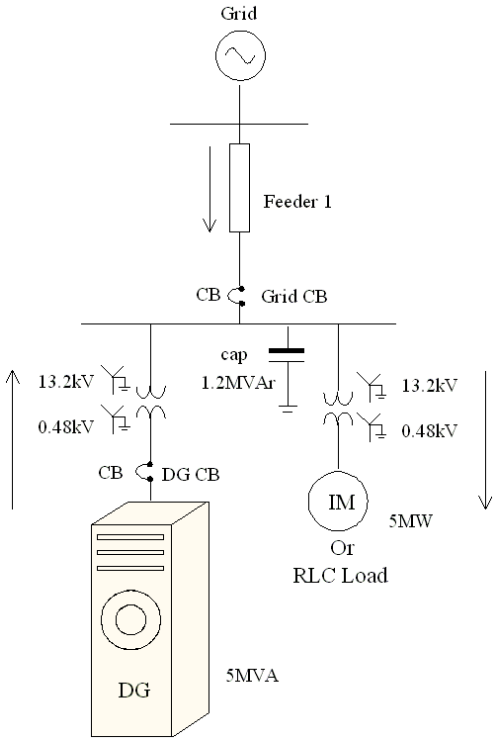


Figure 43. Single line diagram for testing the anti-islanding scenario.

(of the order of 10 s) to a change in the measured output voltage.

The range of values for the SFS and SVS gain determined from the above analysis provides design space for time domain simulations of the DG system. The time domain simulations are application dependent and need to be considered on an individual basis. The time domain simulations will provide acceptance trade off curves between the time to detect island and harmonic distortion.

4.2.3 Time-domain simulations

Detailed time domain simulations of the system have been carried out with passive and active loads using the SVS and SFS algorithm described in the previous sections. The circuit considered for the time domain simulation is shown in Figure 43. The following cases are described below:

- RLC load without anti-Islanding algorithm
- RLC load with anti-Islanding algorithm
- Motor load having high inertia
- Motor load with low inertia.

The gains of the SFS and SVS algorithms were selected to be within the range obtained from the analysis in the previous sections. However, a detailed trade-off study has not been performed to pick optimum gains. The gains for all the above cases studied are the same—

- Gain setting for SFS is 10
- Gain setting for SVS is $K_v = 2$ and $K_{vp} = 2$—i.e., a sum of four for the case with DG supplying rated load at unity power factor.
- The DG power level is 5 MW and it injects current into the grid at unity power factor.

RLC load without anti-islanding algorithm:

The RLC resonant load was first tested without any anti-islanding protection. The waveforms for this case are shown in Figure 44. It can be observed from the voltage and current waveforms, that the DG continues to feed the RLC load and forms an island. The frequency and voltage drift by a small amount due to a minor difference in RLC values and due to the small numerical mismatch between the real and reactive power in the load and generator. However, the drifts in frequency and voltage magnitude are not sufficient to detect an islanding situation in an acceptable time frame (based on the passive anti-islanding limits on voltage and frequency set according to IEEE P1547).

RLC load with anti-islanding algorithm:

Figure 45 depicts the voltage and current at the DG terminals for the RLC load, for the case where the active anti-islanding algorithm is enabled. The system was islanded at time 0.70037 s by disconnecting the grid. The DG detected the island and tripped due to a drift in the frequency because of the active anti-islanding algorithm.

Motor load with high inertia and anti-islanding algorithm:

The next load considered is a three phase induction motor load with a high inertia ($J_{(pu)} = 2.6$s). The motor operates such that the entire 5MW generated by the DG is consumed by it. The reactive power consumed by the machine is fully compensated by capacitor banks at the 13.2 kV bus (Figure 43). The settings for the algorithm are the same as for the other cases. Figure 46 shows that the DG has a tendency to drift on. The trip is finally detected at around 1.92 s.

Motor load with low inertia

For the case shown in Figure 47, the motor inertia is 0.4 s (p.u.) with all other parameters remaining the same. The DG, which acts as a current source, accelerates the motor after being disconnected from the grid. As a result, the anti-islanding algorithm detects the frequency drift beyond the limit points and trips. The trip time in this case is reduced to 0.328 s.

4.2.4 Summary

- The DG without active anti-islanding has a tendency to island for a resonant RLC load, thus creating a number of possible hazardous conditions for the system.
- The single phase Sandia anti-islanding algorithm can be effectively adapted for three phase DG applications. In frequency domain it has been observed that the loop gains did not vary with the load type. The algorithm when tuned for rated DG power level will be effective under all realistic operating conditions.
- The algorithm is not as effective for some induction motor loads. In particular, large inertia loads with significant reactive compensation. More research is needed to fully quantify these loads and to investigate anti-islanding alternatives.

4.3 RECLOSING

Reclosing of breakers after a temporary fault is a common practice to prevent interruption of supply to end customers. The fault clearing breakers are delayed from closing after a fault to allow the fault path to deionize.[28] The time delay provided for reclosing is generally determined by the nature of the load, which the recloser is protecting.

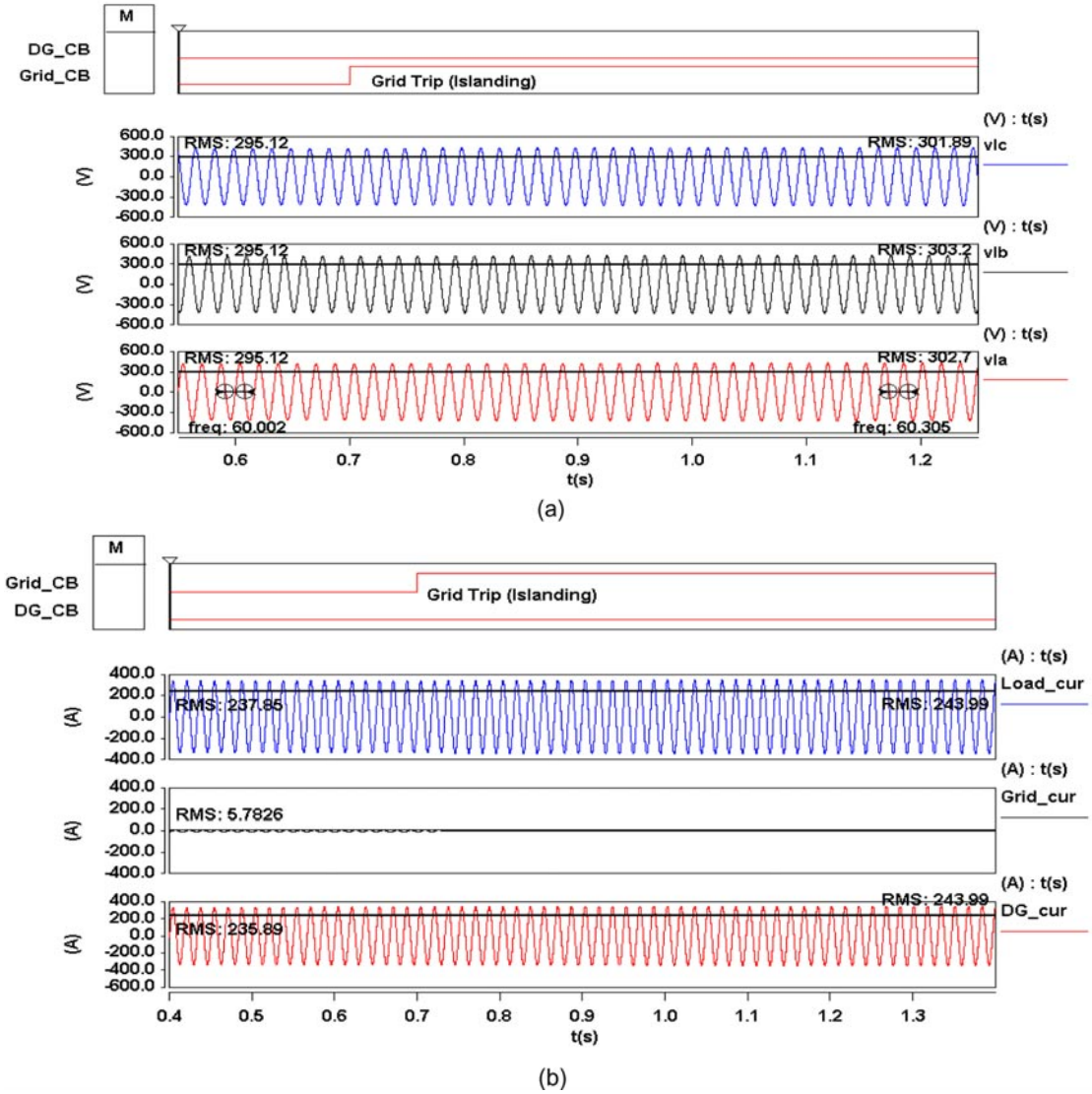


Figure 44. Waveforms for the RLC load without anti-islanding protection (a) Load phase voltage, (b) Current.

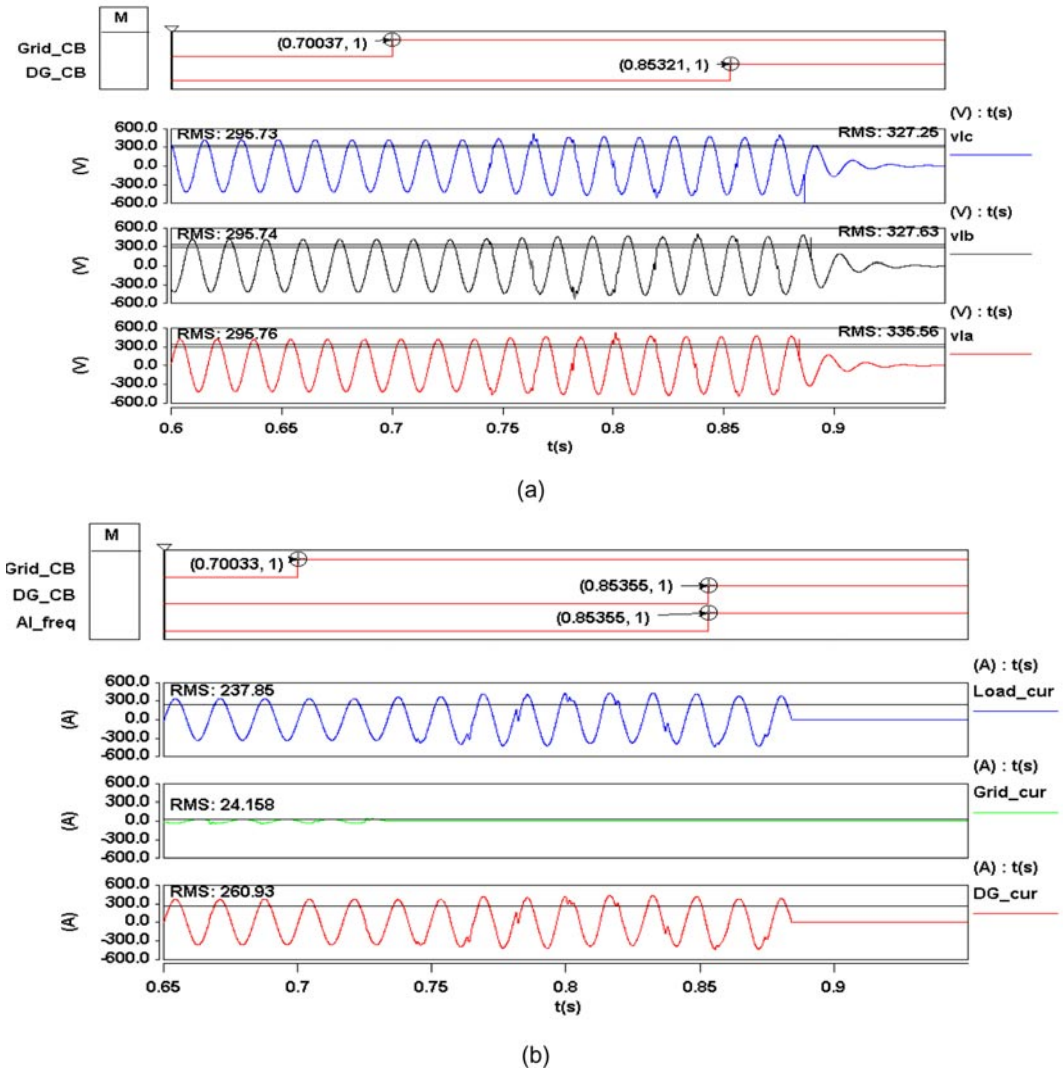


Figure 45. Waveforms for RLC load with K_f = 10 and K_v and K_{vp} = 2 (a) Load phase voltage and (b) current waveforms.

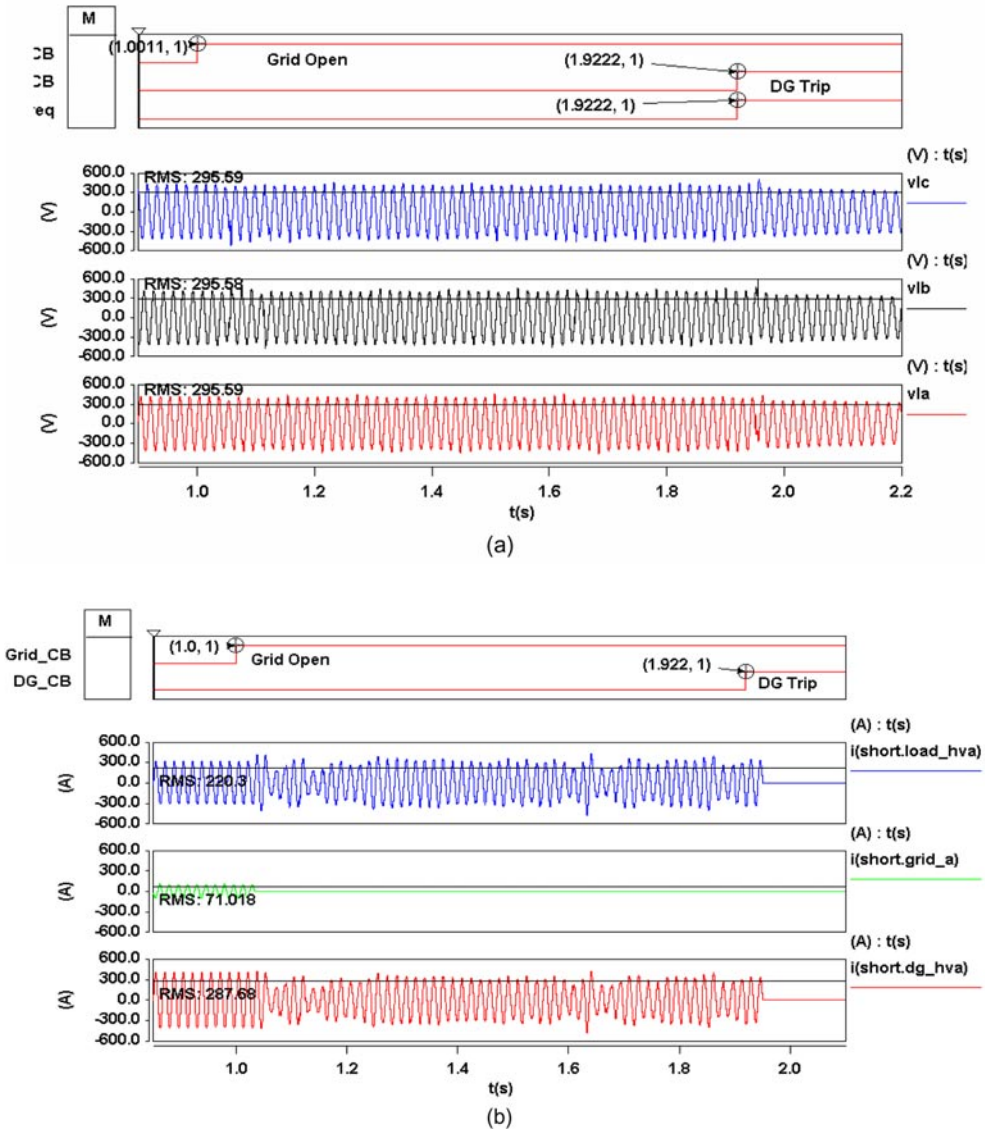


Figure 46. Waveforms for islanding situation with a high inertia motor. (a) Load phase voltage, (b) current waveforms.

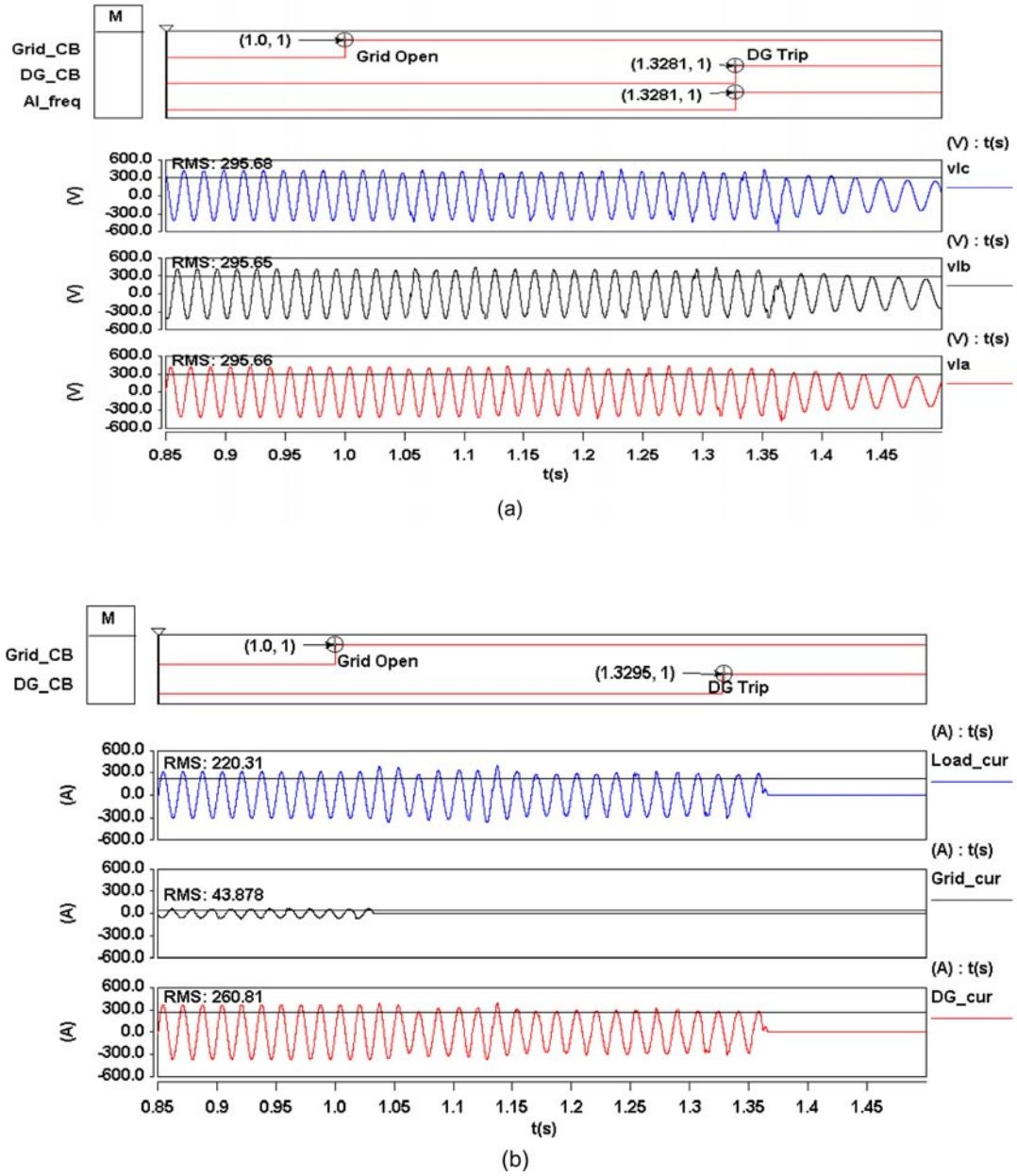


Figure 47. Waveforms when the island load is a low inertia motor. (a) Load terminal voltage, (b) currents.

4.3.1 Out of phase reclosing

The introduction of DG adds to the complexity of the issue. Normally, with anti-islanding protection, the DG will trip off-line when grid is disconnected. However, the possibility of DG run-on always exists. If the DG continues to feed an island with motor loads and capacitive components, a situation may arise wherein, the recloser closes onto an island when the grid and DG voltage are not in phase, or out of phase in worst case. The out-of-phase reclosing will cause overvoltage and large inrush current, which may damage equipment in the system. Appropriate relays required to prevent such an occurrence are rarely installed along with distribution reclosers. This section will illustrate the effects of out of phase reclosing on the distribution network.

The circuit considered for this case study is shown in Figure 48. For a typical distribution network, induction motors comprise a large percentage of the total load. Capacitors are also commonly present in the system for voltage regulation or power factor correction. Cables and lines will also contribute stray capacitance to the system.

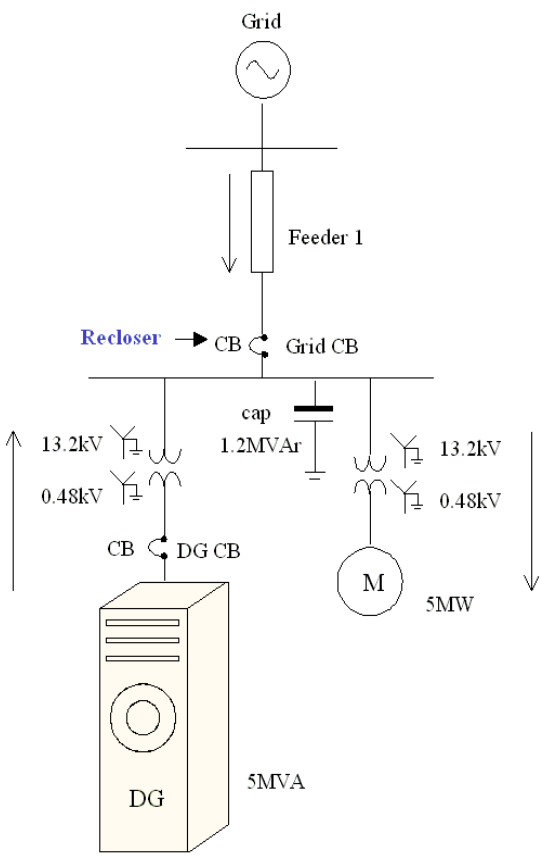


Figure 48. One line diagram of the circuit used to study impact of reclosing.

The DG is controlled to supply rated power at unity power factor. The capacitors on the 13.2 kV bus provide voltage support by compensating the reactive power needed by the motor. The capacitor provides about 1.3 MVar ensures that there is no reactive power miss-match when the recloser opens.

If the DG runs on when the grid is disconnected, a small frequency difference can lead to a large phase angle difference between the DG and the grid. Given a typical recloser delay time setting and islanded DG frequency, the phase shift of the grid and DG may not be very large by the time of reclosing. However, to evaluate the worst-case conditions, this study will look at reclosing with nearly 180° out-of-phase conditions.

To illustrate the impact on the presence of DG on reclosing, the following scenarios are studied:

- Three phase reclose with motor load of high inertia with DG.
- Three phase reclose with motor load of high inertia without DG.
- Three phase reclose with motor load of low inertia with DG.
- Three phase reclose with motor load of low inertia without DG.

Three-Phase reclosing with high-inertia Motor Load and with DG

The recloser disconnects the DG from the grid and the DG continues to supply the island with the motor load and the capacitor. The voltage of the island drifts out of phase from that of the grid due to a slight unbalance in the loads and also due to the active anti-islanding algorithm can lead to frequency shifts. The recloser is closed when the grid and DG are 180° out of phase in phase A, at around 0.763 s, as shown in the Figure 49. This results in the characteristic ringing in the voltage, with overvoltages more than 2 p.u. This voltage magnitude may be sufficient to damage utility and customer equipment, including surge arrestors.

Due to the reclose, nearly twice the rated volt-second is applied to the motor terminals resulting in a heavy inrush current in the motor. Magnetic saturation characteristic, which is not represented in the simulation, can lead to even larger inrush current. This current is supplied by the grid, since the DG is controlled as a current source with current limit. The currents supplied by the DG, grid, and that drawn by the load are shown in Figure 50.

Three-Phase reclosing with large inertia motor load and without DG

As a comparison, the reclosing was simulated for a system with the grid supplying the motor and capac-

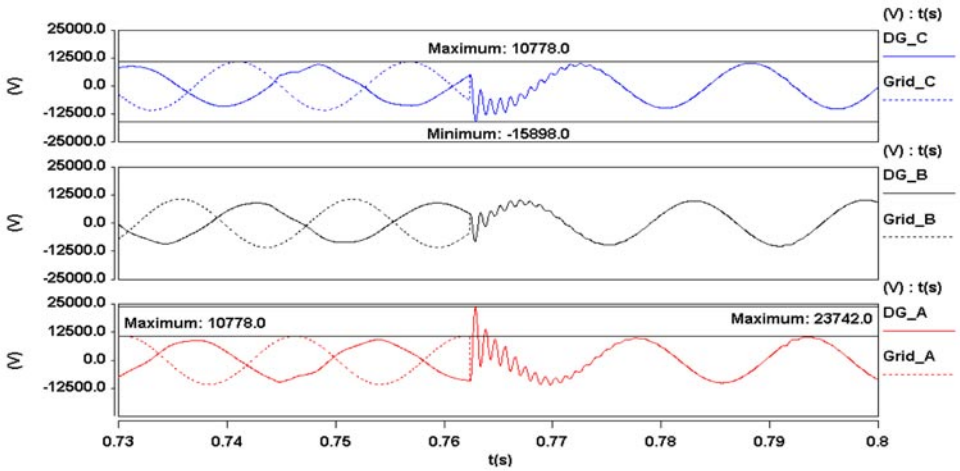


Figure 49. Phase voltage waveforms of the DG and grid showing the effect of out-of-phase reclosing.

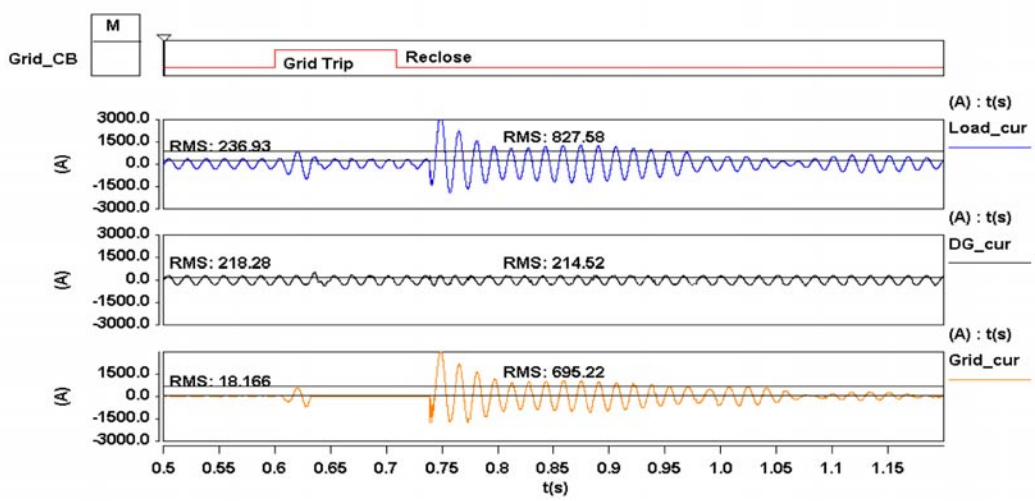


Figure 50. Inrush currents observed for the motor load after the three phase reclosing.

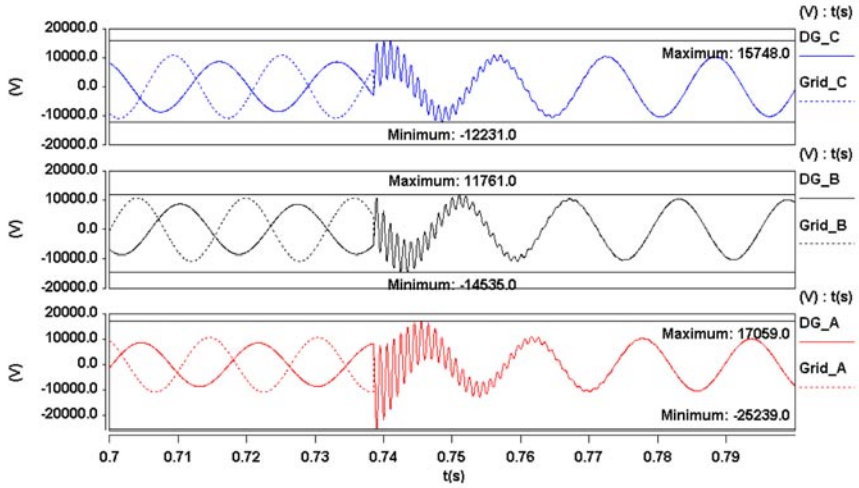


Figure 51. Voltage waveforms for the reclosure action when the DG is absent.

itor load only without DG. A 180° phase shift is set before reclosing for consistent comparison. In this case, it is assumed that the large inertia and flux in the machine along with the capacitive compensation sustains the voltage of the load system. The waveforms obtained are shown in Figure 51.

The results indicate that any element in the power system that can store sufficient energy and if it can sustain an island can lead to out of phase reclosing. The oscillations observed in the case without the DG have a larger magnitude and last for a longer time as compared to the case with the DG. This indicated that the DG, in this example, provides some damping to high frequency oscillations.

Three-phase reclosing with low-inertia motor load and with DG

It is common for the machine loads in a distribution feeder to have lower inertia. Hence, the impact of the reclosing on an island with a low-inertia (0.4 s) motor is studied both with and without DG.

Typical waveforms observed are shown in Figure 52. The reclosing is carried out 0.3 s after the trip. If the reclosing time is further increased, the DG will trip because of undervoltage. The capacitive compensation and the power injected by the DG is such that the real and reactive power drawn from the grid is close to zero. In this case, the voltage dips to a low value at the time of the reclosing. Hence, the voltage overshoot observed is of reduced magnitude compared with reclosing on high-inertia case. Figure 53 shows the currents of DG, grid and the motor load. The current inrush into the machine is lower because of the reduced back emf. The motor acceleration time is smaller than normal start up. However, the peak inrush current is larger than that for motor startup, as shown in Figure 54.

Three-phase reclosing with low-inertia Motor load and without DG

For comparison, the case with low-inertia motor and without DG is simulated. The waveforms observed for this case are as shown in Figure 55. In this case, due to the residual voltage is nearly zero, the worst case overvoltage should be smaller than the case with a DG. The inrush current after reclosing, as shown in Figure 56, is practically the same as during motor startup.

A comparison of the motor speeds, rotor fluxes and torques for the two cases, low-inertia motor with and without DG, respectively, is shown in Figure 57. It can be seen that the DG tends to hold the motor speed for a longer time as compared to the case without the DG.

4.3.2 Summary

- If the DG real and reactive power is matched and with improper settings of anti-Islanding algorithm can result in the formation of an island. This results in the DG feeding the motor and/or resistive and capacitive load in the absence of grid. Large inertia motors loads with capacitive compensation can also lead to a sustained island even without any DG.
- The difference in the frequency between the islanded DG/load system and the grid can result in out-of-phase reclosing. The possibility of this occurring is relatively rare. However, when it occurs, the impact on the system is very severe. For example:
  - There is the potential for high peak voltages during reclosing that can affect surge arrestors in the utility system.
  - High inrush currents caused by reclosing can damage the motor and trip other breakers in the system.
- An out-of-phase reclosing will have significant adverse effect on the system. To prevent this, effective anti-islanding controls should be incorporated so that the DG will trip off-line before a reclosing event can take place.

4.4 POWER SYSTEM DYNAMICS AND STABILITY

4.4.1 Introductory dynamics discussion

In analysis of bulk power systems, the presence of distributed generation has normally been aggregated, or netted out, with the loads. However, the response of distributed generation to perturbations of voltage and frequency, and more important, to large disturbances such as faults, is potentially very different than that of loads. Thus, when systems begin to have significant penetration of DGs, a wide range of fundamental (power) frequency issues arise, such as:

- Voltage profile
- Short circuit current levels
- Active and reactive power flows
- Thermal (current) loading on circuit elements
- Transient stability (maintenance of synchronism)
- Dynamic stability (damping of electro-mechanical oscillations between generators)
- Voltage stability and collapse
- Reactive power control and management
- Frequency control
- Power interchange control

In this section, power system dynamic simulations are shown that help illustrate the impact of DG on each of these areas of concern. This exami-

Table 5 P2 distributed generation initial conditions and capabilities

DG bus name	Active power output	Reactive power output	Voltage/frequency regulation
B1-3	1700 kW	0.	Yes/Yes
D1-1	200 kW	-100 kVAr	No/No
F1-1	1500 kW	0.	No/No
D2-1	100 kW	0.	Yes/No
G2-1	2900 kW	1200 kVAr	Yes/Yes

nation starts by considering the behavior of a local distribution system, then continues on to consider an entire power grid. Finally, the dynamic aspects of microgrids are examined.

4.4.2 Local distribution system stability issues

One class of dynamic impact of immediate concern is the potential for DG to alter the local dynamics of a specific subsystem or distribution feeder. This becomes a concern when there is a significant penetration of DG relative to the total load power on that feeder. Such localized concentrations are likely to occur, even before DGs become more commonplace. Thus, there is some urgency for the power industry to understand the possible impact of locally high concentrations of DG.

Discussion of P2 system

The P2 system, as shown in Figure 4 serves to illustrate behaviors of interest. The five DGs in system P2 were selected and modeled as a variety of device types in the fault scenarios presented below in Table 5. The table shows the active and reactive power output of the DGs in the base case, and whether the devices were provided with the capability to regulate voltage or frequency. (In subsequent sections, the DGs were modified *en mass* to provide different dynamic characteristics (e.g., with anti-islanding), but these initial power conditions apply to all cases. This illustrates one type of DG diversity that might be encountered on a distribution feeder that evolves in such a way that individual customers add DGs in a largely unplanned and uncoordinated fashion.

Local voltage behavior without high level controls

An example of one potential impact is presented below in Figure 58. This figure shows results of three time simulations of a lateral fault on the 12 kV distribution feeder. One voltage at a location along the feeder is plotted for each of the three cases. The feeder serves about 14 MW of load. Of that load, about 6.4 MW is provided by DGs, which corresponds roughly to a penetration of about 45% DG. The case illustrates the potential impact of DGs tripping due to the fault induced voltage depression. In one case, all of the DGs are presumed to trip by the time the fault clears. This case results in a transient voltage collapse as the motor load served by the feeder stalls. (About 60% of the total load is modeled as induction motors of various types, including some machines that are prone to stalling). The traces which recover represent cases where either none or a modest fraction of the DGs trip.

The mechanism by which the DGs might trip fall into two categories:

- inverter control failures, i.e. inadvertent trip
- anti-islanding trips, i.e. deliberate trips.

The case illustrates that there may be some systemic risks, if DGs are designed (or specified) in such a fashion that they are likely to trip for otherwise survivable disturbances. It should be pointed out that there is no reason why the DGs would necessarily trip under this condition; rather, this is a cautionary illustration.

Impact of various control on local dynamics

The behavior of DGs imbedded in distribution systems will be governed in part by the types of controls provided. The results shown in Figure 58 are for a system with all the DGs having the simplest of controls: constant current. The following is a very brief discussion of possible higher level controls that might be provided with DGs.

Constant power control

This type of control is one level higher than the constant current control inherent to the basic inverter controls. This type of control will likely be the natural default for inverter-based devices for which optimum performance is obtained with steady-state operation of the energy source. For grid- parallel operation there is no requirement that the energy source actively respond to system disturbances. For some devices, cleaner and more efficient operation may result from constant power operation.

Voltage control

Voltage control on DGs has the potential to complicate voltage and reactive power management on

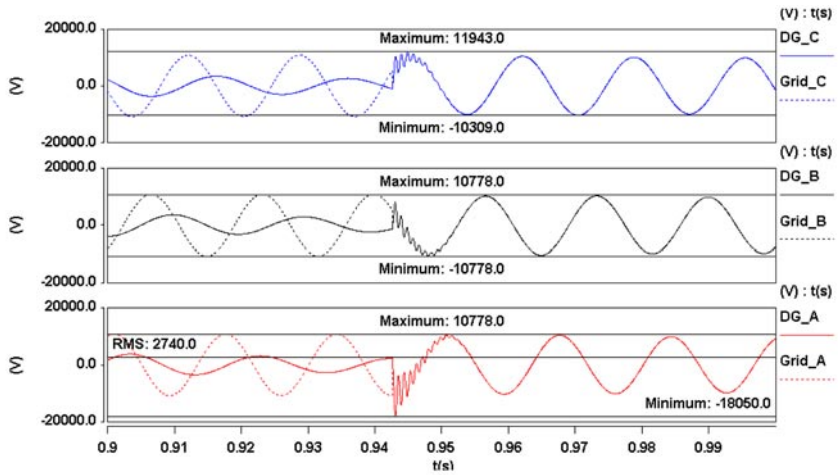


Figure 52. Phase voltage waveform of the DG and grid side terminals of the recloser showing the effect of three phase reclosing for a lower inertia motor.

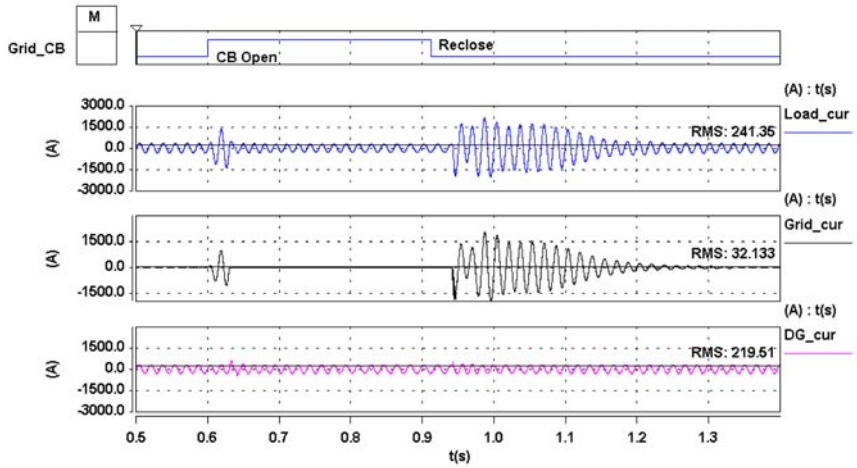


Figure 53. Currents for three phase reclosing of an induction motor with lower inertia.

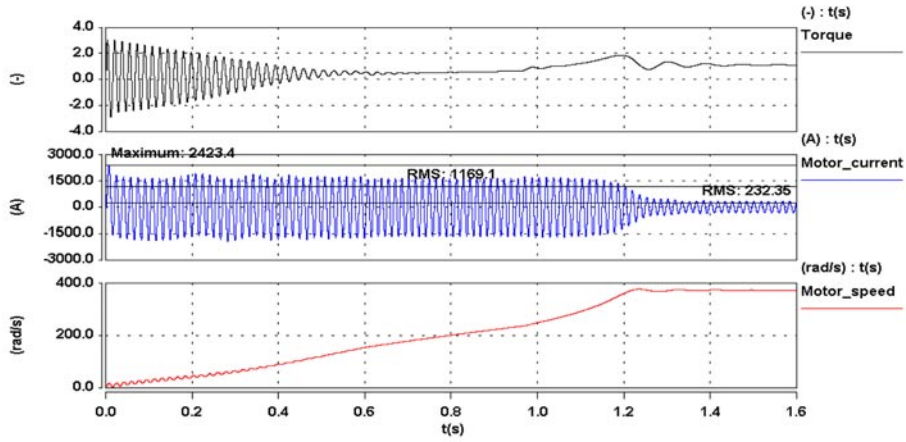


Figure 54. . Inrush current at the starting of the induction motor with low inertia.

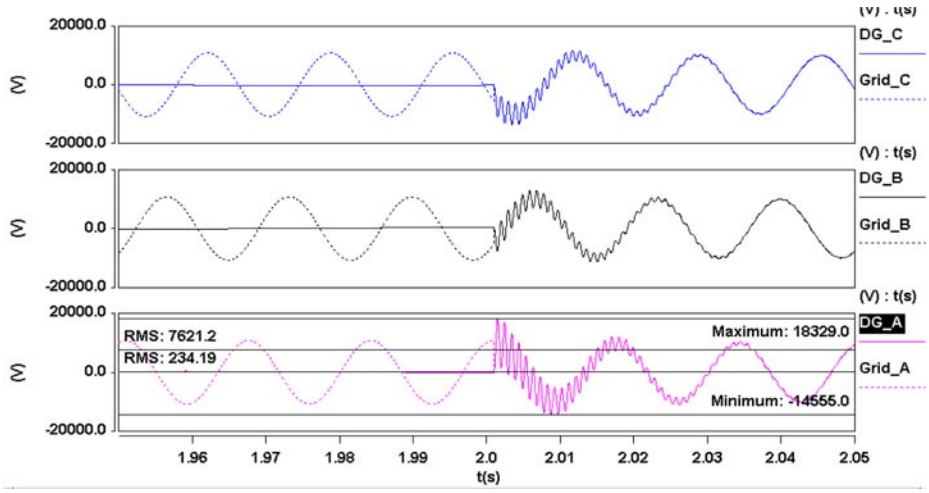


Figure 55. Voltage waveforms at recloser terminals for motor load without DG, but with a lower inertia.

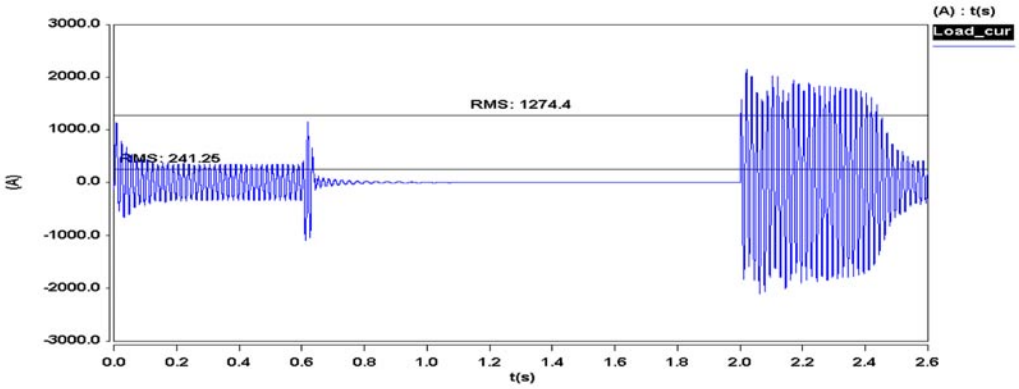


Figure 56. Inrush current for the case with low-inertia motor and without DG.

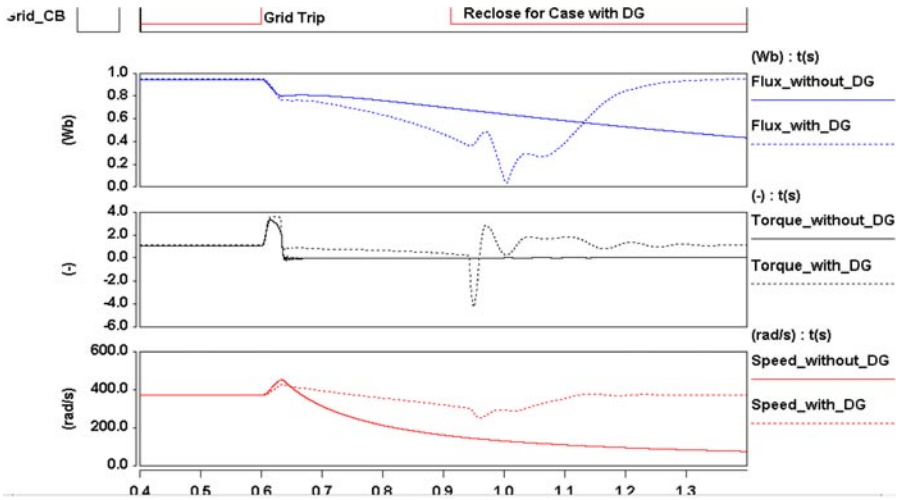


Figure 57. Comparison of rotor flux, motor speed and torque with and without DG for motor load of low inertia.

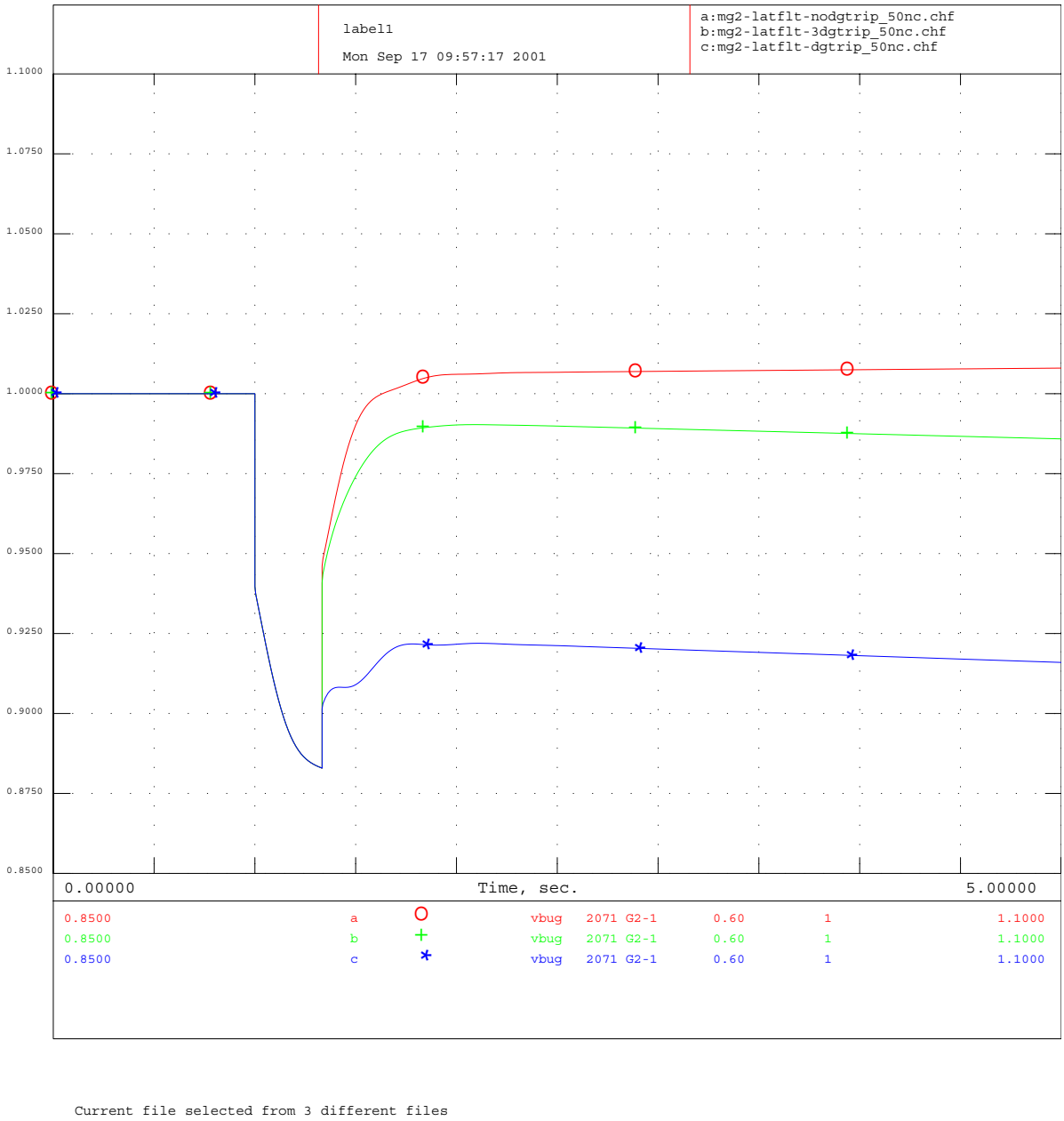


Figure 58. Localized voltage behavior due to DG tripping.

distribution systems, as discussed in section 3.1. On the other hand, the discussion in section 3.2 on flicker illustrated some examples of how voltage regulation has the potential to improve system performance. Voltage regulation is a requirement for isolated operation

Frequency control

This type of control is a yet higher level control than the constant power control. This type of control will be required for islanded operation, but will not normally be applied to grid-connected devices. Frequency control will (generally) direct the DG to increase power output in response to frequency depressions. This function is normally done by the central station generation that provides spinning reserve. Issues related to frequency regulation are examined later in this section.

Appendix F presents the results of a sequence of cases, similar to that shown in Figure 58. In each of the cases in the sequence, the lateral fault is applied and cleared, and a varying number of DGs are trip during the fault. The sequence shows the impact on system response of adding—

- Constant power control
- Voltage control with relatively high gain regulators
- Voltage control with moderate gain voltage regulators
- Combinations of constant power and voltage regulators

The overall response of the distribution system is only moderately impacted by these various control schemes. The voltage profile on the distribution feeder is improved in the cases with voltage regulation. The high gain voltage regulation rapidly returns the voltage to nominal. This performance is unnecessarily aggressive for most applications. The voltage behavior with the more moderate gain voltage regulators is good. The presence of constant power regulation has little impact for these cases.

Impact of various anti-islanding functions on local dynamics

The anti-islanding control discussed in detail in section 4.2 has potential to affect the dynamics of the distribution system. The detailed Saber representation of the anti-islanding schemes (Figure 46) translates approximately into a fundamental positive sequence model, of the structure presented in the *Models and Virtual Test Bed* report.[1] Figure 59 shows this structure, with the anti-islanding schemes highlighted (in red). The anti-islanding schemes work through two paths of the inverter control. The first path, termed SFS scheme according to section 4.2, primarily affects the power output via the current magnitude control, in response to voltage deviations. The second path, termed SVS scheme according to section 4.2, primarily affects the synchronization of the DG, through the angle, in response to frequency deviations. These two schemes can be applied independently or together.

As discussed earlier, the design philosophy of these anti-islanding schemes is to destabilize the island, causing or allowing it to be shut down. The intent of this investigation was to illustrate how an islanded distribution system, with multiple DGs and with dynamic (motor) loads would respond to an islanding event. The case presented in Figure 60 is based on a condition when the distribution system island has good power balance with the host grid. The distribution system is slightly exporting to the host utility. The distribution system is disconnected, without a fault event, from the host utility. This is the condition of primary concern for anti-islanding schemes, since significant import or export will cause rapid instability and shutdown of the islanded system, without any special control action required.

Figure 60 shows four traces for each of frequency and voltage on the islanded distribution system. In each of the four traces, the DGs have no constant power control or voltage regulation functions. The upper set of traces is frequency, and the lower set is of voltage. The first trace (red) shows the behavior of the system with no anti-islanding control. The system becomes unstable over a period of about two seconds. The black trace shows the behavior of the system with only the SFS scheme enabled, and the blue trace shows the behavior with only the SVS scheme enabled. Finally, the green trace shows the destabilization with both schemes enabled. This final condition becomes unstable within about one-half second, roughly four times faster than without anti-islanding.

The interaction of the controls discussed above, and the anti-islanding controls is interesting. A sequence of cases, based on the simulation shown in Figure 60, was executed illustrating the potential interaction between other control functions and the anti-islanding schemes. This sequence shows how the two the anti-islanding schemes interact with the constant power control and with the voltage regulation function discussed above.

Appendix F includes the detailed results of all these combinations. The key results form these cases can be summarized as follows: The constant power control defeats the SFS scheme. The case with the constant power control and only the SFS scheme enabled is stable and allows continued operation of

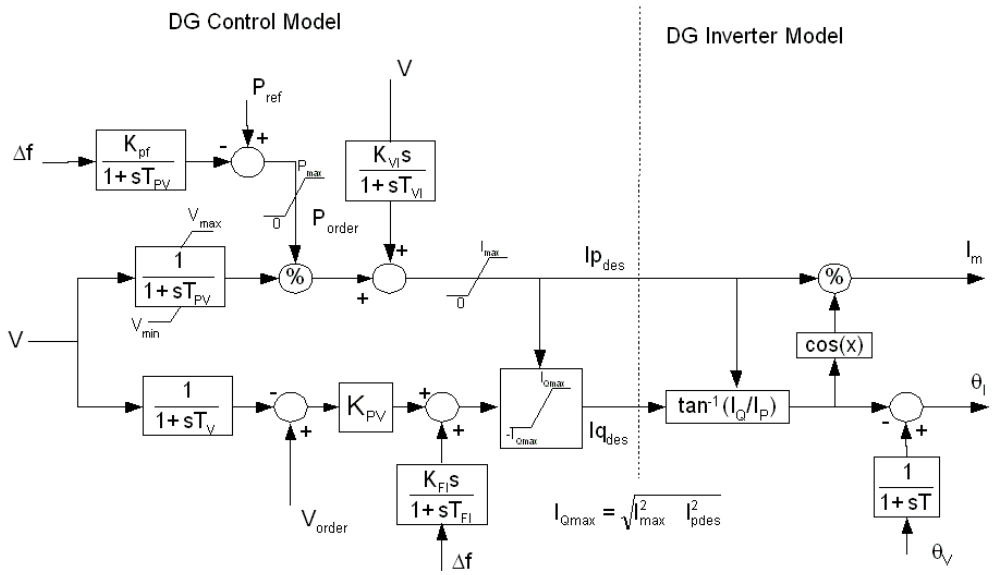


Figure 59. Positive sequence DG inverter-based model with anti-islanding paths.

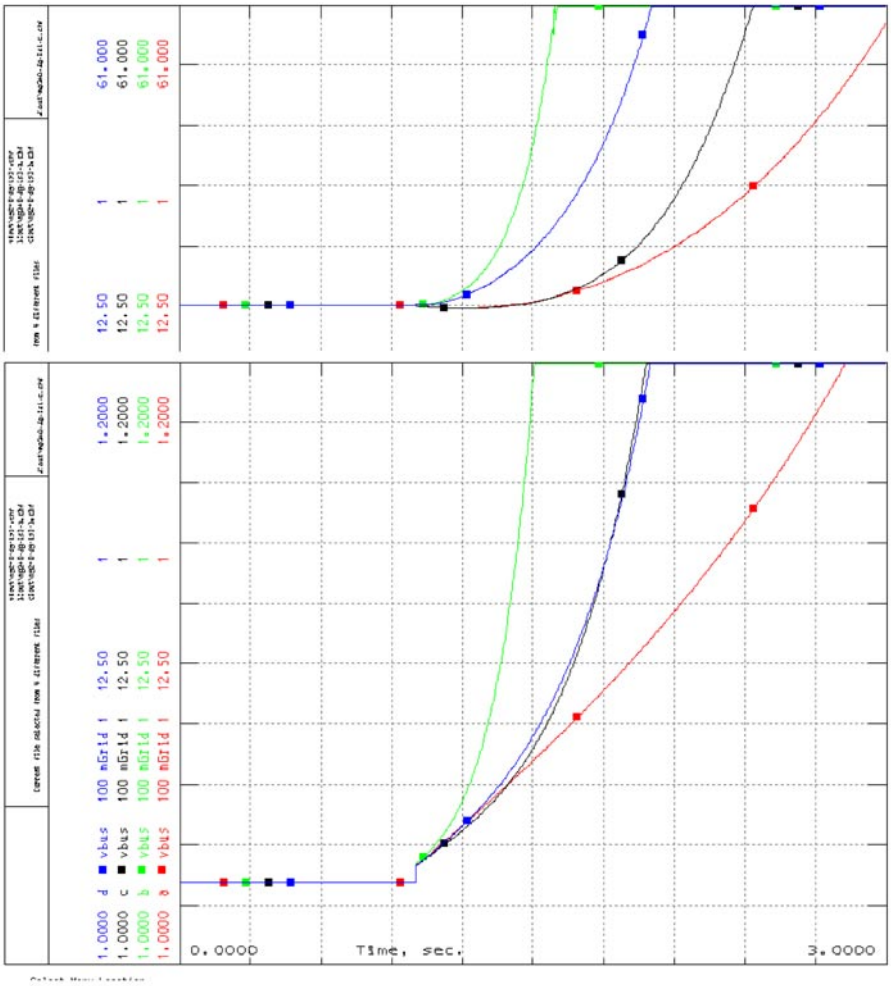


Figure 60. Response of local system with different anti-islanding schemes.

the island (which in this case is not the desired outcome.) The voltage regulation function defeats all the anti-islanding controls, regardless of the combination of schemes and constant power control.

The general trend is not surprising: voltage and power controls, which are primarily aimed at stabilizing the system and the DG (respectively), tend to decrease the effectiveness of the anti-islanding schemes. It should be emphasized that this sequence of cases represents a single set of control gains and structures. Different gains and control designs would undoubtedly result in different performance which could be perfectly acceptable. However, the cases do illustrate one fundamental point: these types of anti-islanding schemes are at odds with the other normal control functions exercised by generation. This is a significant result, in that in the future, successful design of anti-islanding schemes may need to take into account the evolution of DG control requirements for system functions

4.4.3 Bulk system stability issues

In bulk power systems, events on the major transmission corridors or those involving major generating facilities will be felt electrically over the entire system. For example, events of the past few years in the western U.S. have made the general public aware that disturbances in the Pacific Northwest can impact the desert Southwest (and vise-versa).

In the longer term, there are predictions that DG will become a significant factor in meeting total generation requirements for entire power systems. Such widespread deployment of DG is clearly farther in the future than the localized high concentrations discussed above. The widespread deployment of DG raises questions about the impact on dynamic performance of the bulk power system.

In this section, simulations of disturbances on the WSCC system (the western North American grid, comprising all of the continental U.S. and Canada west of the Rockies) are presented to illustrate various potential impacts.

Impact of DG penetration on bulk system dynamics

Figure 61 shows the voltage response of a 500 kV bus (Malin) in WSCC following a single line fault and trip event on the Raver-Paul 500 kV circuit in Washington. One trace represents the base condition, the others represents conditions of increasing DG penetration up to an incremental 20%. In each case with DG, the additional DG is accompanied by a corresponding amount of incremental load. All the DGs are uniformly distributed at equivalent load buses in the data set, and sized in proportion to the load served. Thus, the power flows on the bulk power system are not significantly different in each of the cases. The frequency response of the system, as reflected in one key machine (the Colstrip plant in Montana), is shown in Figure 62

Interestingly, the case with DG and much higher system loads shows better dynamic response than the base case. The maximum voltage and frequency excursions are less, and the oscillations show very slightly better damping. This behavior is with no active voltage control and with constant current output; i.e. with a very simple control structure. The case illustrates that if widespread deployment of DG occurs *at the loads*, as would be expected, the potential impact on system dynamic performance appears to be benign or beneficial.

Impact of anti-islanding schemes on bulk system dynamics

The previous case showed the impact of widespread deployment of inverter-based DGs with basic constant current controls. The following case shows the response of WSCC following an unusually severe event. In this case, a very large power station with multiple units, the Palo Verde NPS, generating over 3000 MW, is assumed to be tripped off-line by some common-mode disturbance. (It should be noted that this disturbance is more severe than standard 'N-1' planning criteria. WSCC criteria dictate that the power system should survive this disturbance, but limited customer interruptions are allowable for events of this severity.)

Figure 63 and Figure 64 show the same two voltage and speeds as presented above. In these figures one trace (red with circles) represents the base condition, the next (green with crosses) represents a condition with twenty percent DG penetration, serving an incremental 20% of the system, and the third (blue with stars) represents a twenty percent DG penetration with all DGs equipped with anti-islanding protection (of the type presented in section 4.2). The case illustrates that the aggregate impact of the anti-islanding schemes (SVS and SFS) is benign to the system performance. The voltage and frequency excursions for all cases are severe. The DG case shows a very slight improvement in voltage recovery and damping of the oscillations, and modest degradation in the recovery of the frequency. The combination of higher system load and DGs causes the slow deep system-wide frequency excursion to be somewhat worse than in the base case. This is essentially unaffected by the anti-islanding schemes. However, the anti-islanding schemes

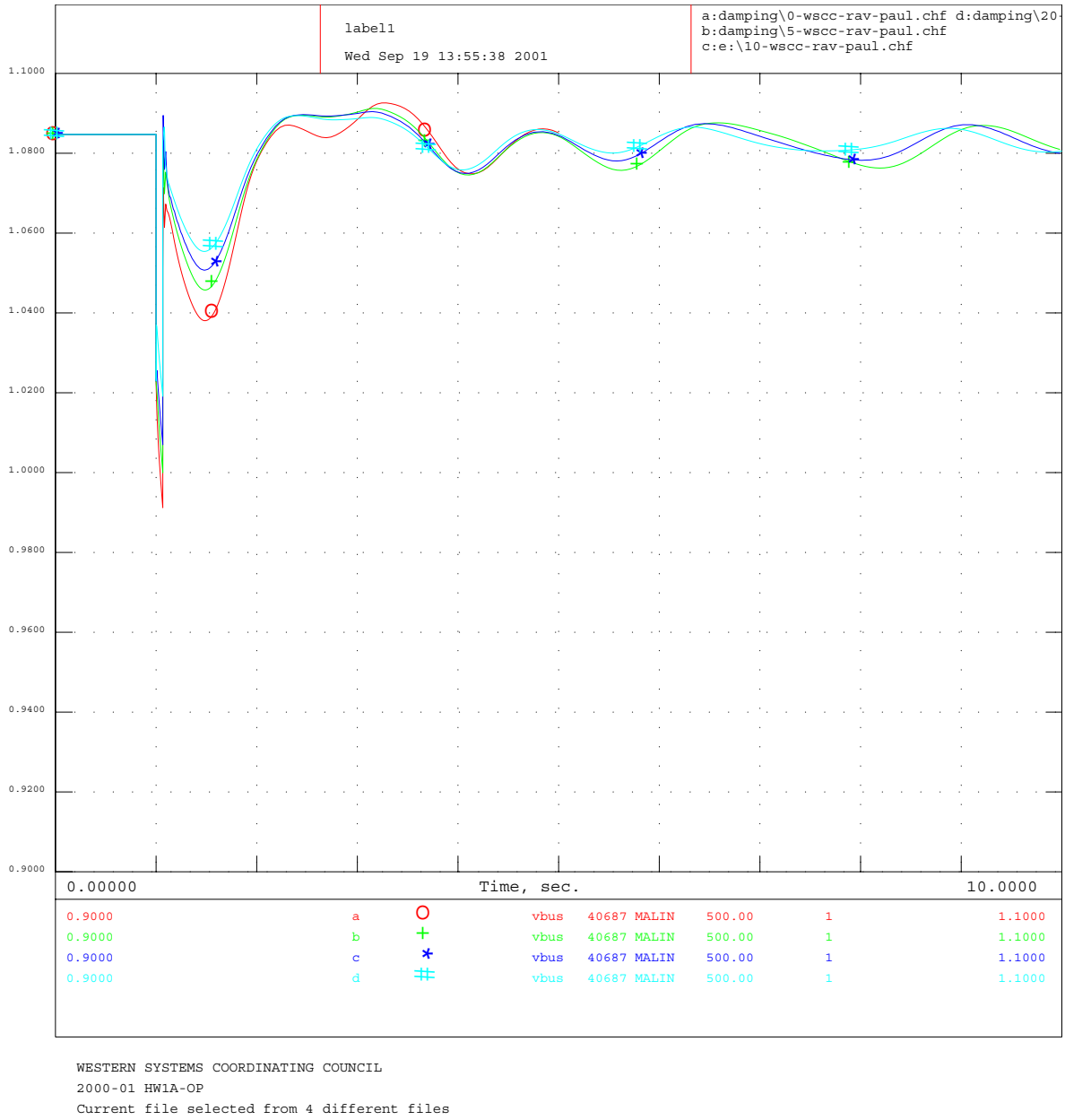


Figure 61. bulk system voltage dynamics with increasing levels of DG penetration.

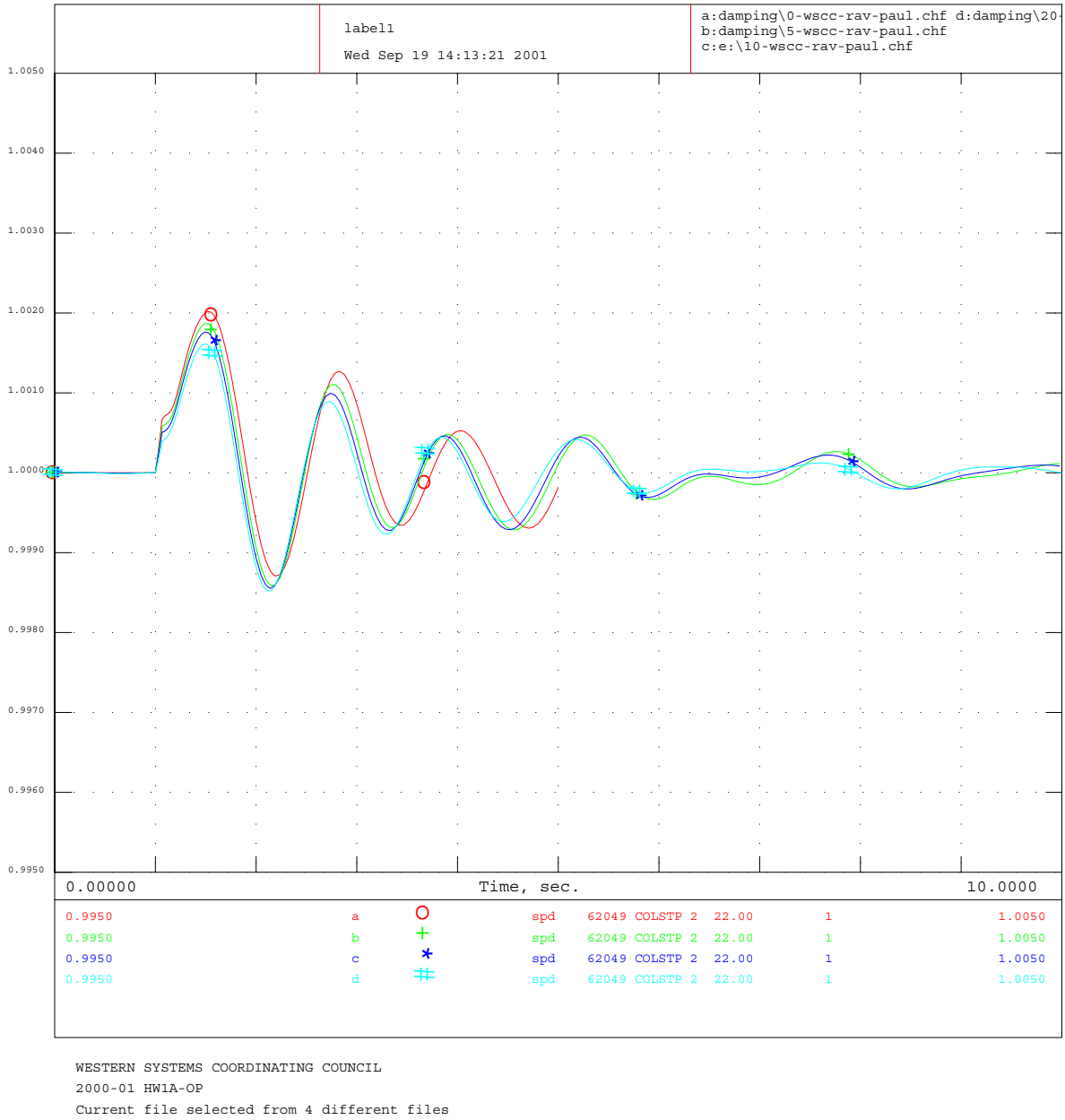


Figure 62. Bulk system frequency dynamics with increasing levels of DG penetration.

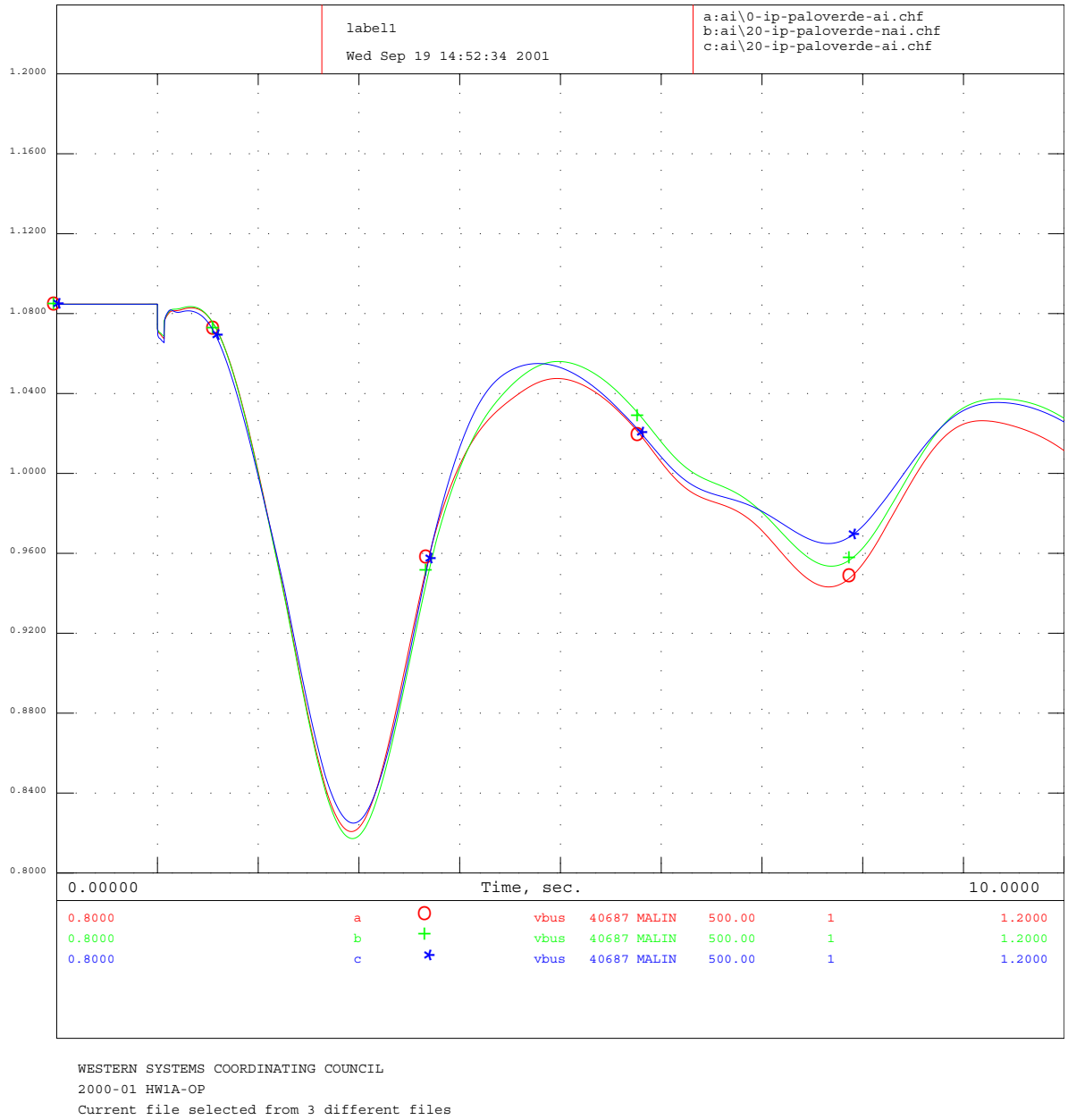


Figure 63. Bulk system voltage dynamics with high DG penetration and impact of anti-islanding.

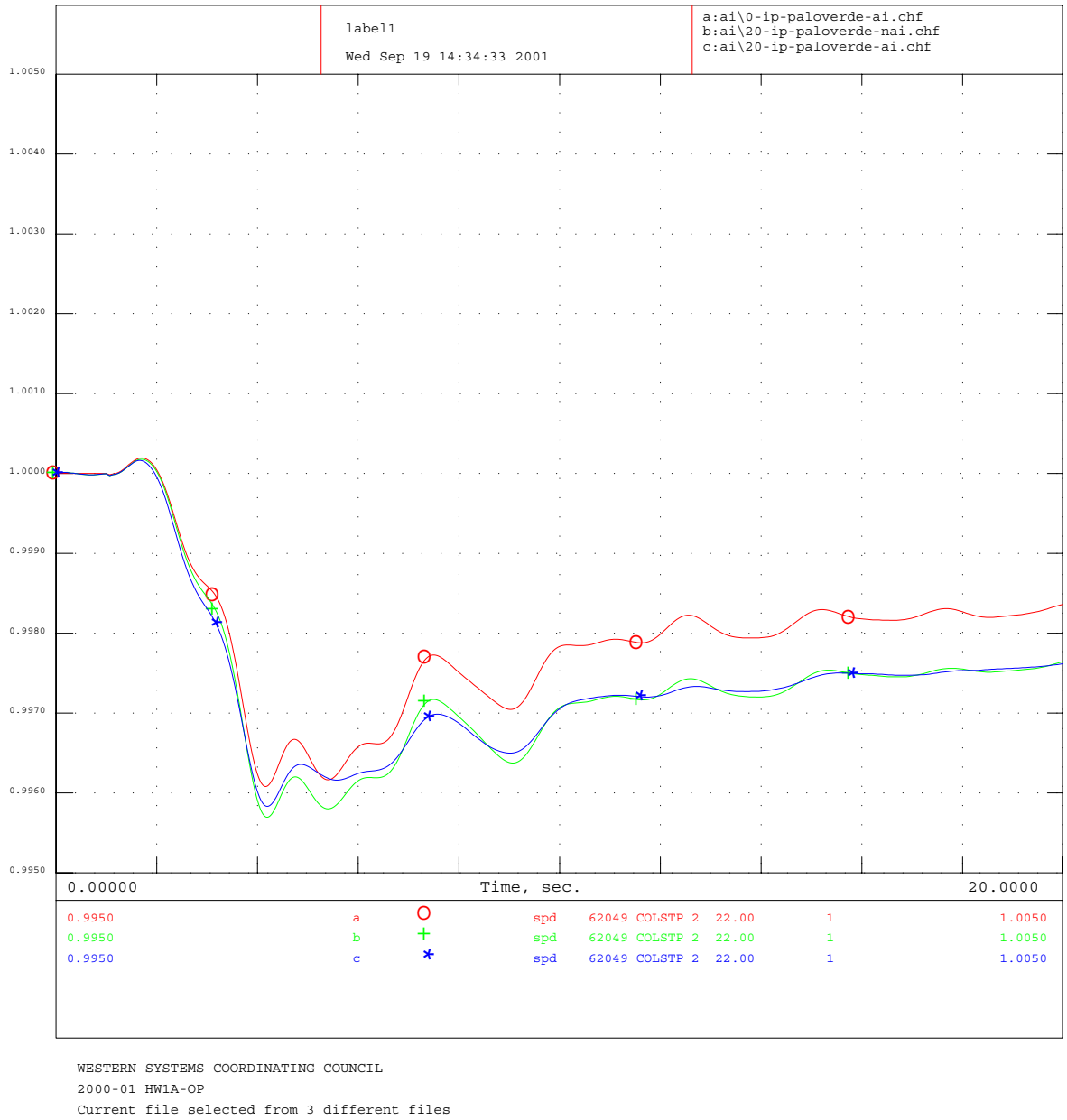


Figure 64. Bulk system frequency dynamics with high DG penetration and impact of anti-islanding.

do contribute positively to damping the faster oscillatory modes of the system. This can be seen by comparing the green and blue traces in Figure 64. These results are specific to this particular control scheme and set of parameters.

Impact of DG tripping on bulk system dynamics

Interconnection standards for DG, including P1547 and several state standards, include ore are trending towards the inclusion of requirements for undervoltage and underfrequency tripping of DG. These requirements are directed at ensuring that DGs rapidly disconnect in response to problems on the distribution system. However, since large-scale disturbances can cause widespread voltage and frequency excursions, this requirement raises some concerns about its potential impact on bulk system dynamics.

Most of the new standards and guidelines dictate that DGs disconnect when voltages drop below 70% for a specified period. This maximum period generally ranges from ten cycles to two seconds. It is important to note that these documents specify the *minimum* voltage and the *maximum* time to trip. Thus, DGs will be in violation if they trip slower or at too low a voltage. However, the DGs may trip faster and at higher voltages than this without violation.

The next five figures present the results of a sequence of cases in which fast undervoltage tripping of the DGs is applied. The disturbance for these cases is the same very severe event as shown in the previous case: tripping of a large multi-unit power plant. In each case there is 20% DG penetration, as described above.

Figure 65 shows the voltages at the 500 kV Malin bus for three conditions: The first trace (red with circles) is the base case, with no undervoltage tripping of the DGs. The second trace (green with crosses) is for DGs that are set to trip when the voltage falls below 70%. The voltage excursion for the 70% case is outside of WSCC criteria for most disturbances. The third trace (blue with stars) is DGs that trip when the voltage falls below 90%. The case with the 90% trip point is very unstable.

Figure 66 shows the speed of the Colstrip machine. The unstable 90% case causes such a severe power deficit in the load areas, that Colstrip loses synchronism with the rest of WSCC. This results in the speed going high (The simulation is stopped at that point, since the entire WSCC system is cascading into widespread blackout). The 70% case shows a deeper frequency excursion, with a slower recovery. The results are somewhat alarming. The widespread voltage depression due to the fault, causes many DGs throughout the system to trip, which in turn leads to a cascading failure of the entire network.

Figure 67 shows the power flow on Path 15, in central California. In this plot, the first trace (red with circles) is for the 70% voltage trip case, and the second plot (green with crosses) is for the 90% case. Before the disturbance, Path 15 is carrying approximately 300 MW (north to south). Following the disturbance and the widespread trip of DGs, the flow jumps to over 2000 MW. Figure 68 shows a similar behavior on the California-Oregon interface (COI). On that interface, the flow jumps from about 3300 MW to well over 5000 MW.

Figure 69 shows the cumulative behavior of the DGs that drives the response shown in the pervious figures. This plot shows the amount of DG that is tripped due to undervoltage. Again, the first trace (red with circles) is for the 70% voltage trip case, and the second plot (green with crosses) is for the 90% case. The voltage depression during the fault causes about 1000 MW of DG to trip before the fault is cleared. Once the fault is cleared, the system voltages recovery is sufficient such that no additional DGs trip. In the case of the more sensitive 90% trip point, approximately 5000 MW of DG (about one-quarter of the total) trip during the fault. The subsequent widespread power shortage, due to the DGs tripping, causes a cascading failure. Over the course of the next few seconds, several thousand more MW of DG trip. The exact details are relatively unimportant, since the system is beyond the point of no return within a fraction of a second following the fault clearing.

To better understand the risk of DGs tripping in response to fault induced voltage dips, it is useful to look at the geographic distribution of voltage. Figure 70 shows the voltages of several 500 kV locations in WSCC, in response to the trip of entire Palo Verde station. The sequence of voltages ranges from the California-Oregon border (the deepest voltage dip) to southern California (the shallowest dip). This plot makes it easy to see that the more sensitive the DGs (i.e., the high the trip threshold) the broader the geographic (and electric) area that will be subject to DGs tripping. It is also interesting to note that deepest voltage dip for this particular event is geographically the farthest away of the four locations plotted.

4.4.4 Microgrid dynamics

One business and technical structure that shows promise as a means to take full advantage of distributed generation is the microgrid. Microgrid is a

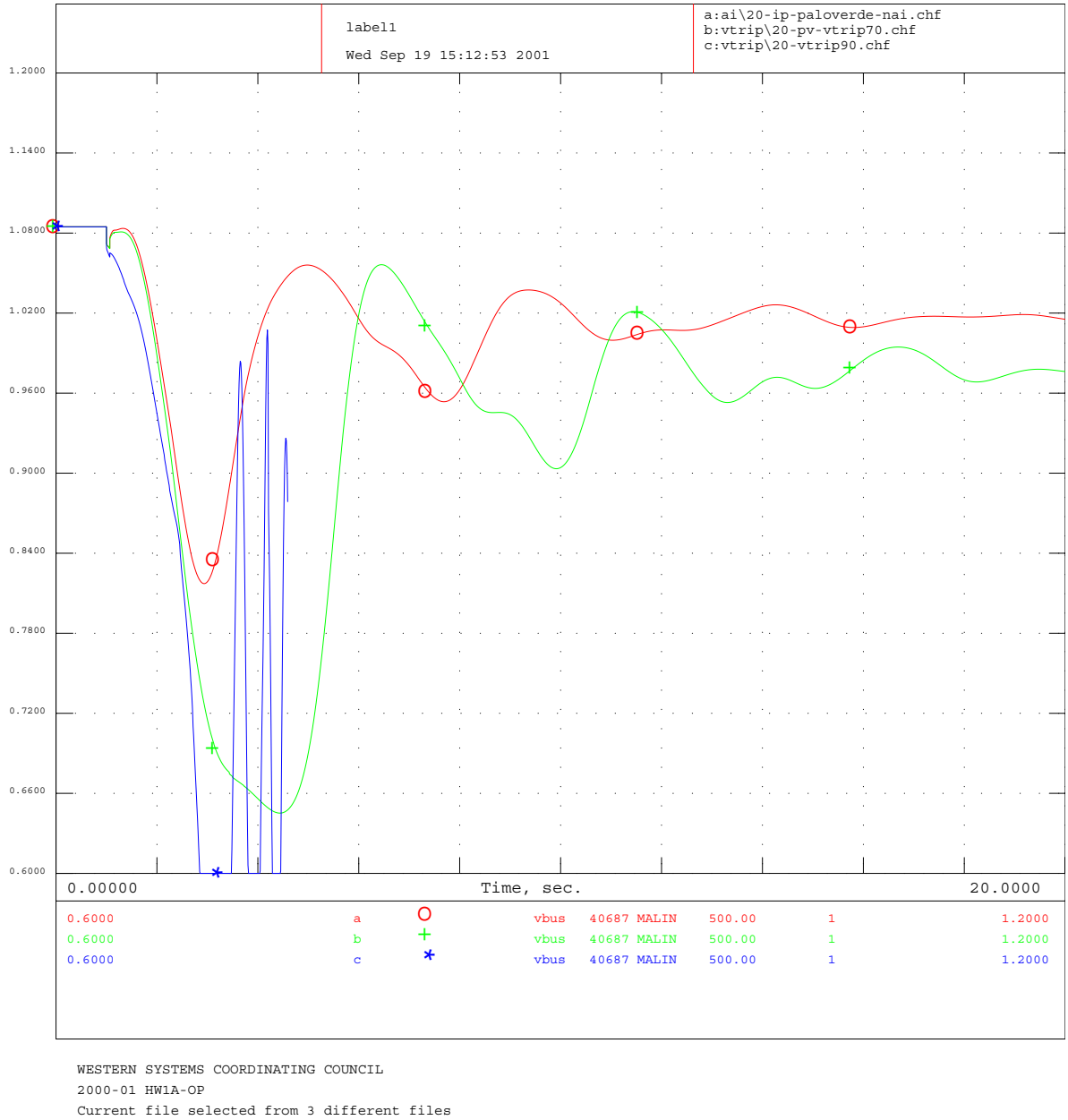


Figure 65. Bulk system voltage dynamics with low voltage DG tripping.

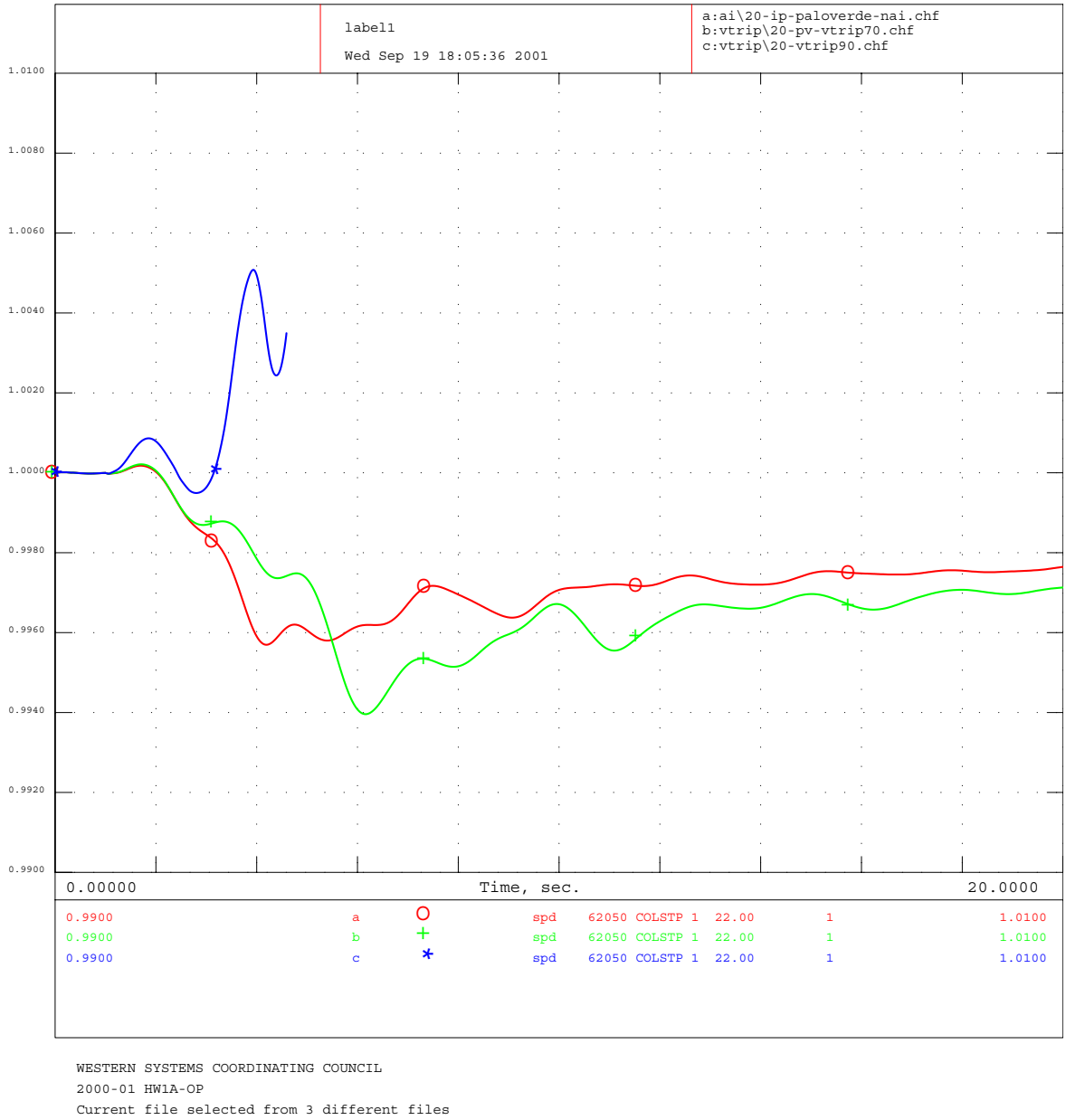


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Figure 66. Bulk system speed dynamics with low voltage DG tripping.

Figure 67. WSCC Path 15 power flow dynamics with low voltage DG tripping.

Figure 68. WSCC California-Oregon interface power flow dynamics with low voltage DG tripping.

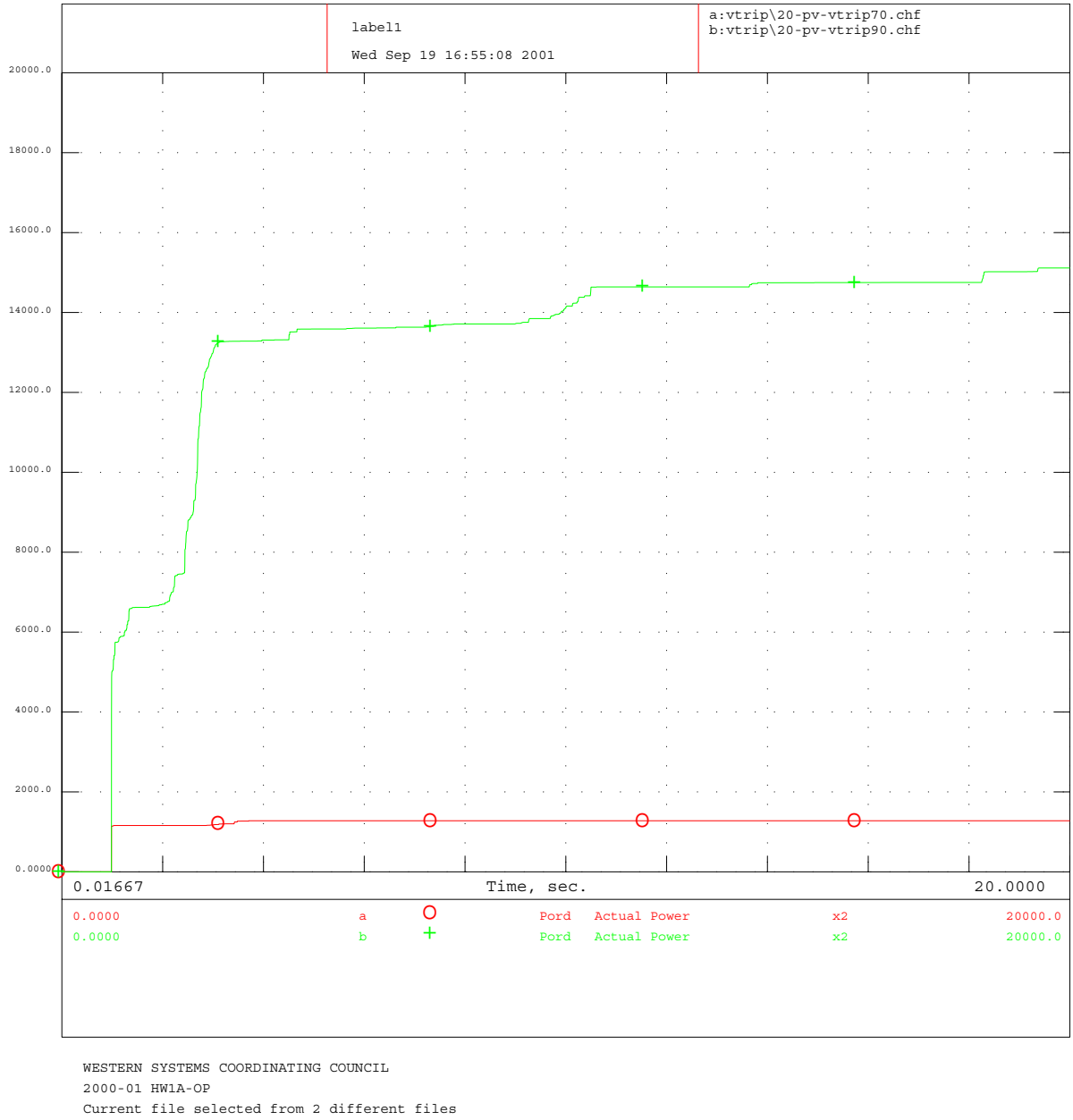

Figure 69. Cumulative DG tripping in bulk system due to low voltage.

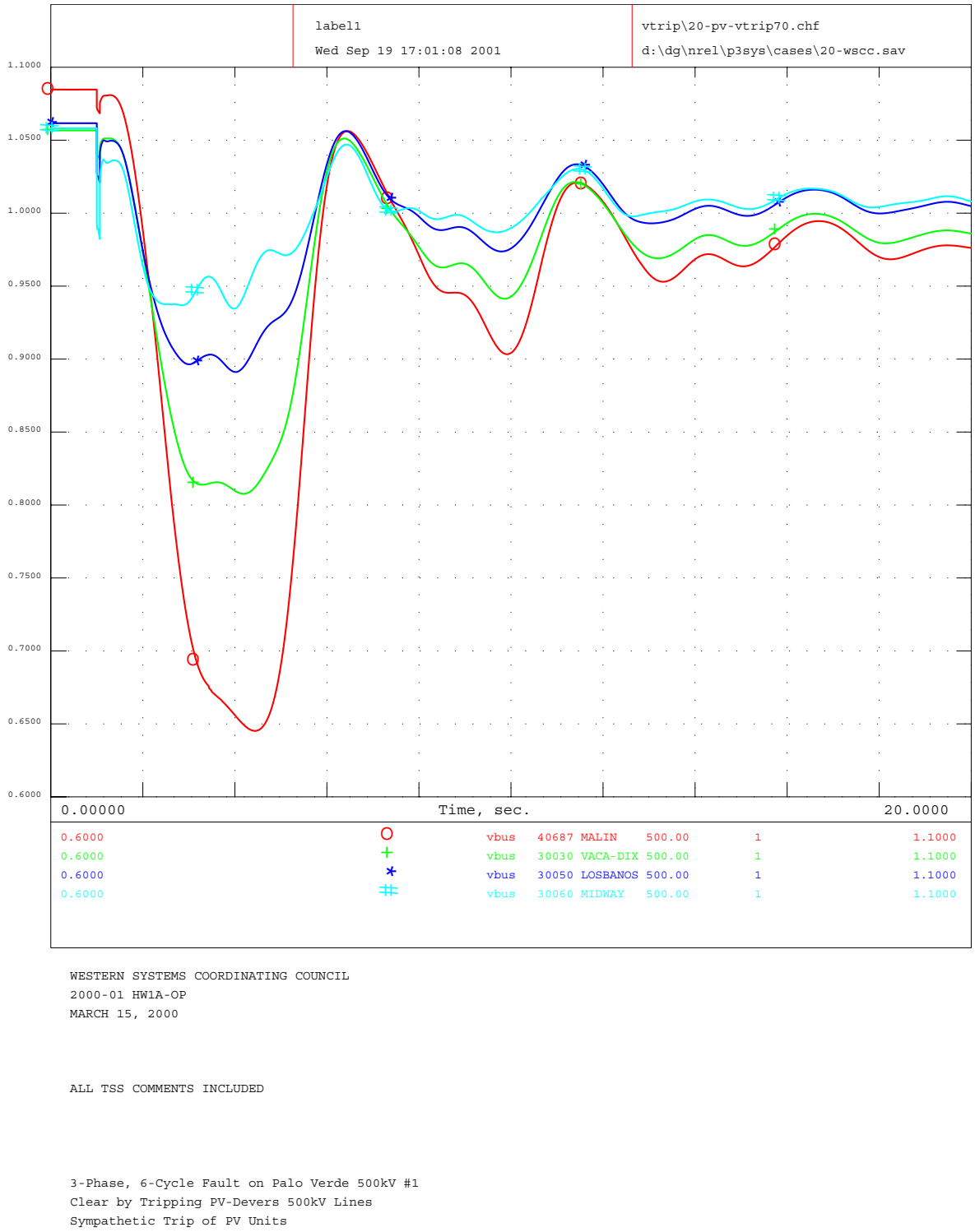

Figure 70. Bulk system geographic distribution of voltage depression due to raver-paul fault with DG tripping in bulk system on low voltage at 70% level.

loosely defined term that describes a small power system, generally with multiple generators and loads. Concepts for microgrids fall into two general categories:

- Systems that are intended to always be operated isolated from a large utility grid
- Systems that are normally connected to a larger grid.

Conceptually, the isolated microgrid is like a scaled down version of a largescale utility grid. Many of the technical requirements are the same. In order to supply reliable, quality power, the microgrid must have mechanisms to regulate voltage and frequency in response to changes in customer loads and in response to disturbances.

For the grid-connected microgrid, the distinction is more subtle. The basic concept is that the microgrid be designed and operated such that it presents the appearance of a single, predictable and orderly load or generator to the grid at the point of interconnection. This arrangement provides several potential advantages for all of the stakeholders:

- DG owners may be able to rate and operate their generation more economically, by being able to export (and import) power to the microgrid.
- The microgrid takes advantage of load diversity to reduce the total installed DG capacity required.
- The load customers may be able to have continued service (possibly at a reduced level) when connection to the host utility is lost.
- The host utility may be able to depend on the microgrid to serve load customers in such a fashion that substation and bulk power infrastructure need not be rated (or expanded) to meet the entire load, as if the DG were not present. (This last point is a major, legitimate obstacle to DG.)
- The microgrid could be controlled in such a fashion as to be active asset to bulk system reliability (for example by providing spinning reserve or black start services, to name two.)

In order to realize these potential benefits the DGs in the microgrid must have, at the least, additional controls. Further, most of these potential benefits require some level of coordination and communication. These controls, which are basically aimed at making viable islands, are largely incompatible with present industry trends and the requirements of current interconnection standards.

In this section, the P2 distribution system is operated as a microgrid. This system includes many of the basic constituents of a microgrid, making it suitable for exploring many of the dynamic performance issues surrounding microgrids. The system includes multiple DGs, a range of loads with varying dynamic characteristics, and a simple grid structure (the tie between the ends of two feeders is closed for the cases presented here.)

Microgrid dynamics with autonomous controls

The ability of a grid-connected microgrid to survive loss of connection to the host utility depends on a number of factors. The microgrid must have sufficient dynamic regulating capability to be able to tolerate the change in both active and reactive power flow that will result from loss of the utility tie. This means that at least some of the DGs must have both voltage and frequency regulation functions.

The following four figures show the results of a sequence of simulations on the P2 system. For these simulations, all five of the DGs on the microgrid are inverter-based devices with voltage and frequency regulation capability, limited according to their individual rating. The controls are the proportional controls presented earlier, and are autonomous, i.e. there is no coordination or communication assumed between them in the time frame of the simulation. In each case, the microgrid is disconnected from the host utility by opening the substation breaker.

Figure 71 shows the voltage traces at one bus (the D2 bus) for four different initial conditions: The first trace (red with circles) is for an initial condition of importing 2 MW, or about 20% of the microgrid load, from the host utility. The system response is unstable for this case. The second trace (green with crosses) is for an initial condition of about 1 MW import. The third race (blue with stars) is for a nearly balanced initial condition, and the fourth trace (teal with pound symbols) is for an initial export of about 1 MW. Figure 72 shows the corresponding frequency traces. Figure 73 shows the active power output of one of the DGs, and Figure 74 shows the reactive power output of that same DG.

There are several observations that can be made. The most obvious is that the microgrid can operate stably following disconnection from the grid with autonomous proportional controls, as long as the power export (or import) preceding the disturbance is not too large. For this case, 'too large' was somewhere between 1– 2 MW (or roughly 10 and 20% of the microgrid load). In general, to be viable the DGs on the microgrid must have sufficient range to pickup the change, and they must respond

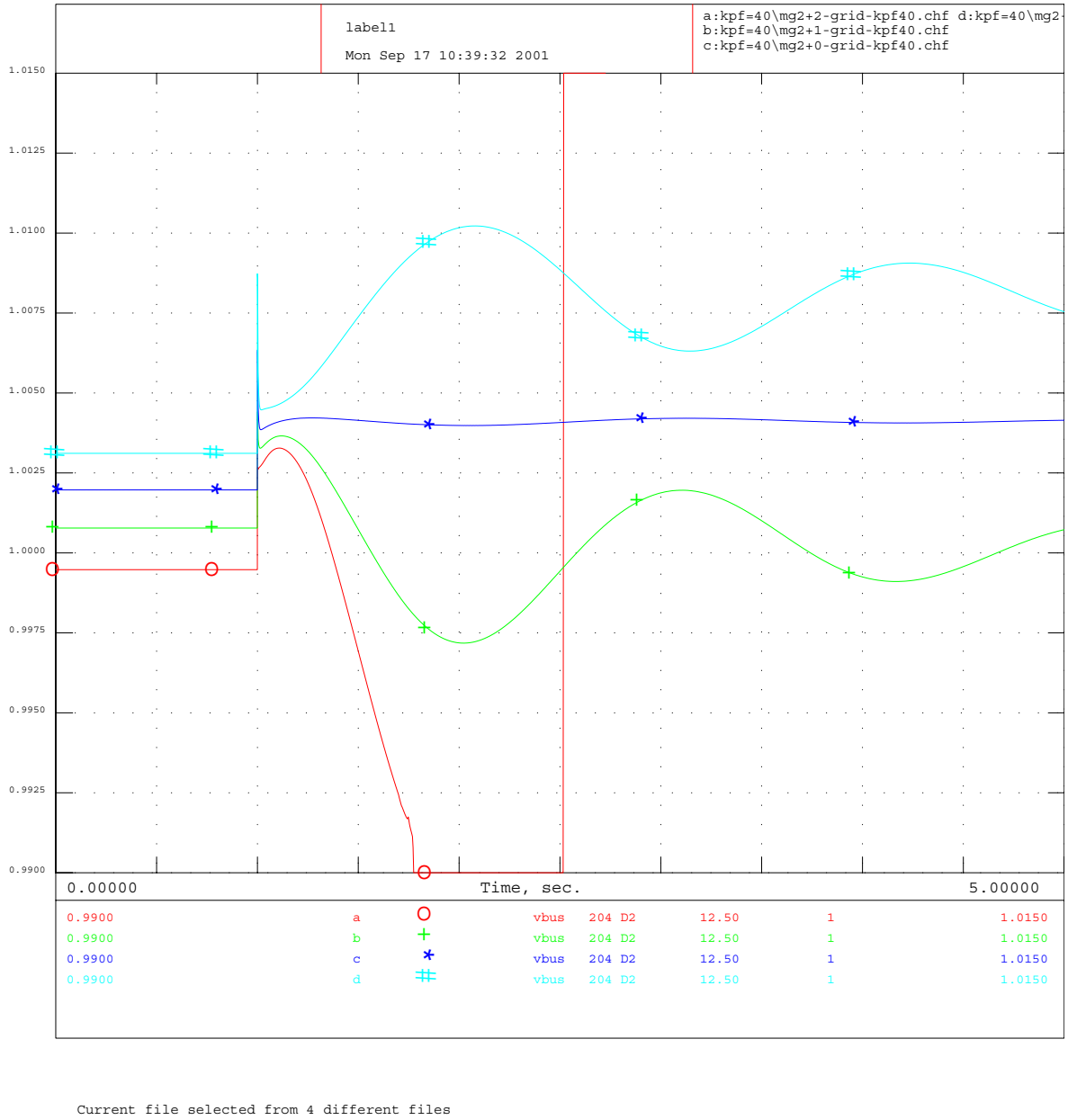

Figure 71. Microgrid voltage at bus D2 following islanding from bulk system.

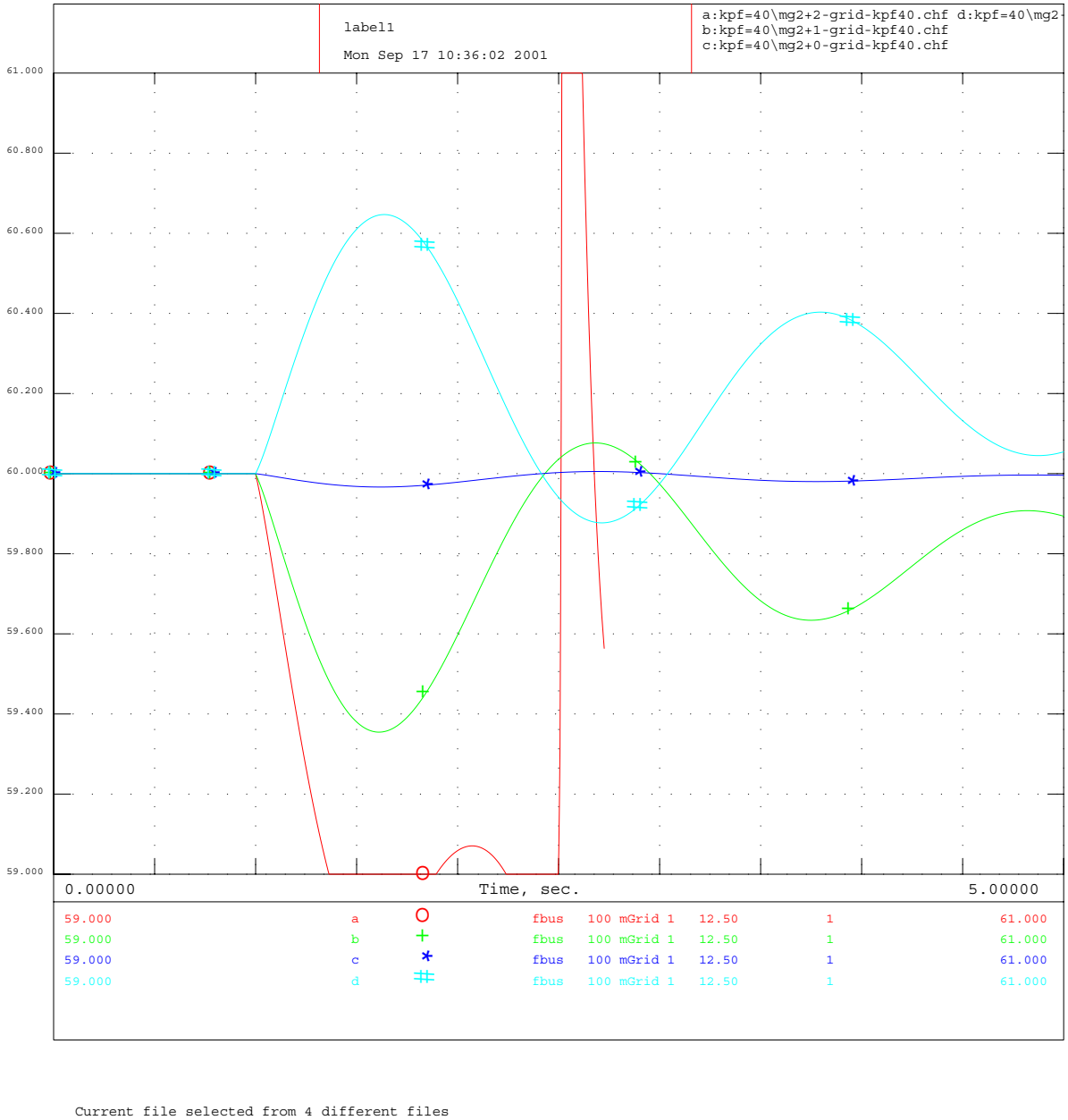

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Figure 72. Microgrid frequency following islanding from bulk system.

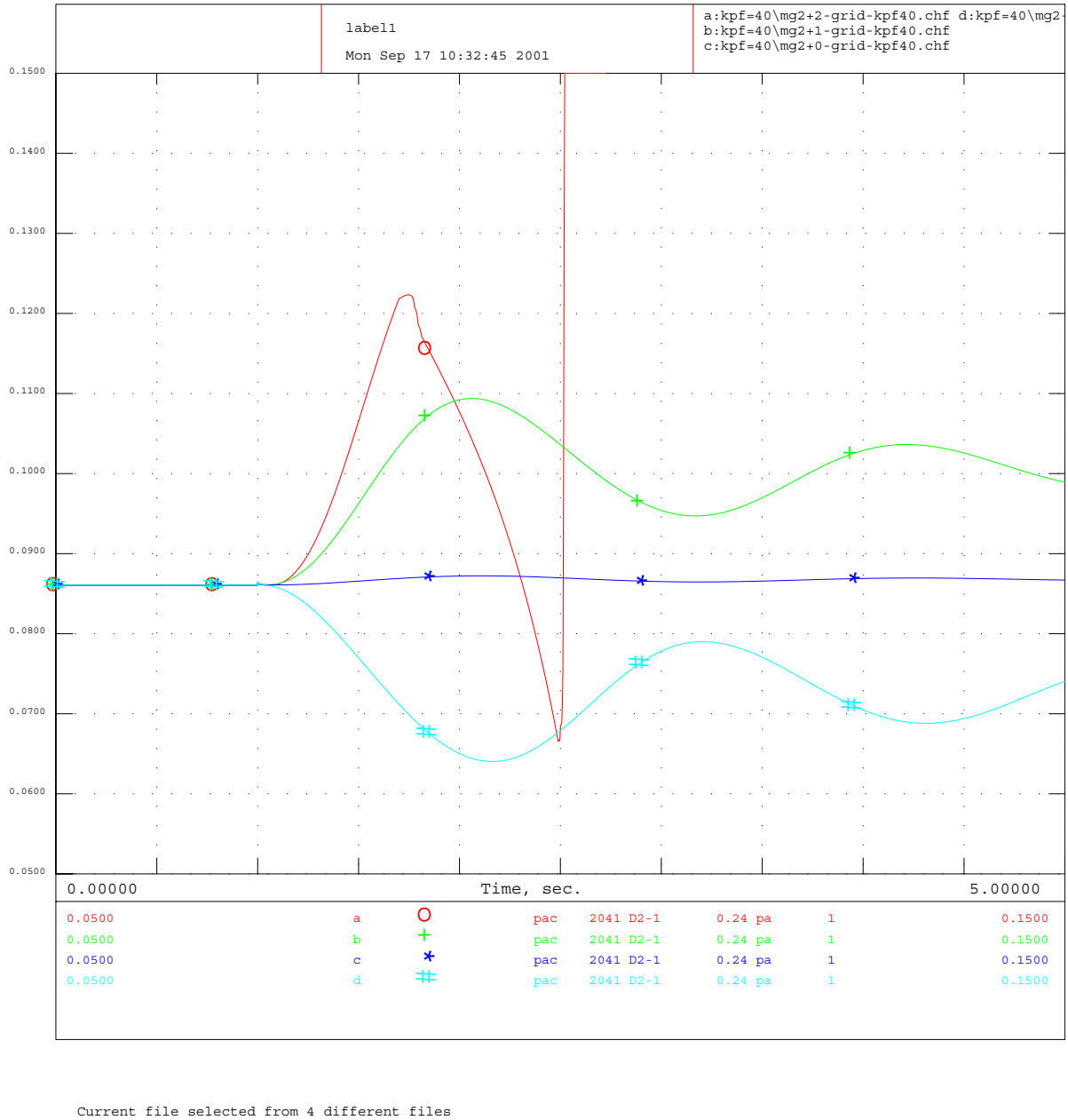


Figure 73. Active power output of DG at bus D2 following microgrid islanding from bulk system.

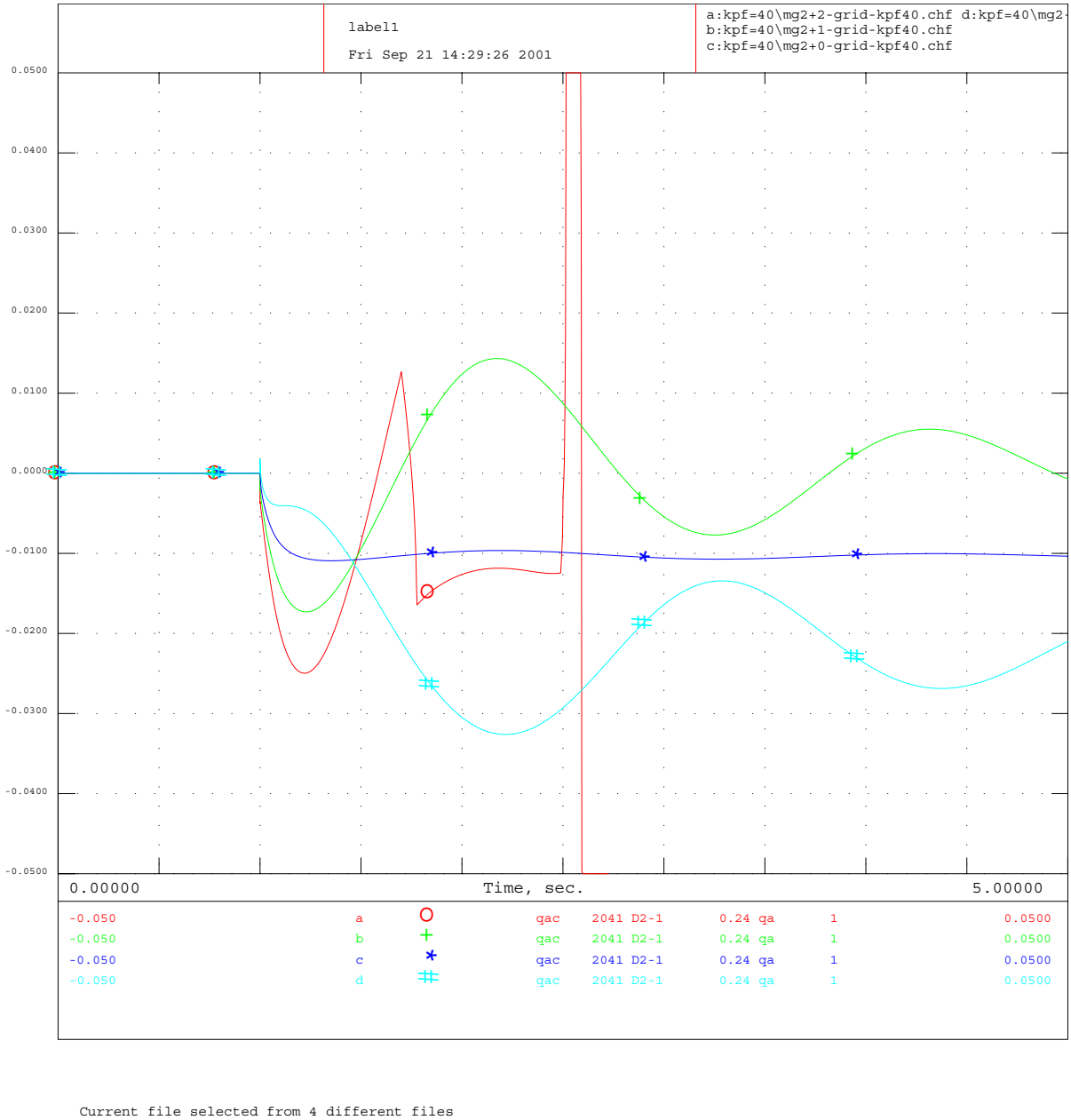


Figure 74. Reactive power output of DG at bus D2 following microgrid islanding from bulk system.

quickly (and stably). In other words, the microgrid must act like a regular utility grid—at least in this time frame.

The behavior of an isolated microgrid presents similar requirements. Again, as with a large conventional utility grid, the isolated microgrid must retain sufficient regulating reserves to allow it to respond to system disturbances. One disturbance that the microgrid must tolerate is loss of one of the DGs.

Figure 75 shows the response of the P2 system to trip of one DG. Unlike the previous sequence of cases, the initial condition for this disturbance was already islanded. The figure shows four traces. The disturbance is trip of one DG, which is initially producing about 1.5 MW. The first trace (red with circles) is the active power output of one of the four remaining DGs. The second trace (green with crosses) is the reactive power output of the same DG. The third trace (blue with stars) is the frequency. The fourth trace (teal with pound symbols) is the terminal voltage of the same DG.

The response shown in Figure 75 is relatively complex. To understand the response, it helps to remember that the inverter-based DGs are limited in the current that they can deliver. In this disturbance, loss of the DG initially causes the frequency on the microgrid to drop rapidly. This can be seen clearly in the first half second following the DG trip (blue trace is dropping). The frequency regulation function (governor function) responds by increasing the active power output of the DG (red trace rises in the same time period.) In the same time period, the voltage (teal) steps up but then begins to decline as well. The voltage regulation function responds initially by dropping the reactive power output, but then boosting it as the voltage declines (green). Just before two seconds, a dramatic change occurs. This is because the DG inverter has run into its current limit. At this point, this particular control is designed to give active power priority over reactive power. Therefore the reactive power drops to zero (green) trace, and the active power *current* is pegged at the maximum until about three seconds. The active power (red) droops a bit in the middle of this time period, because the voltage (teal) drops abruptly in combined response to the system swing and the reduction in reactive power output. (The active power output is the product of the active power current, which is pegged, and the voltage which droops.) The system survives the swing, and inverter comes out of current limits at about three seconds, restoring the voltage regulation function as well.

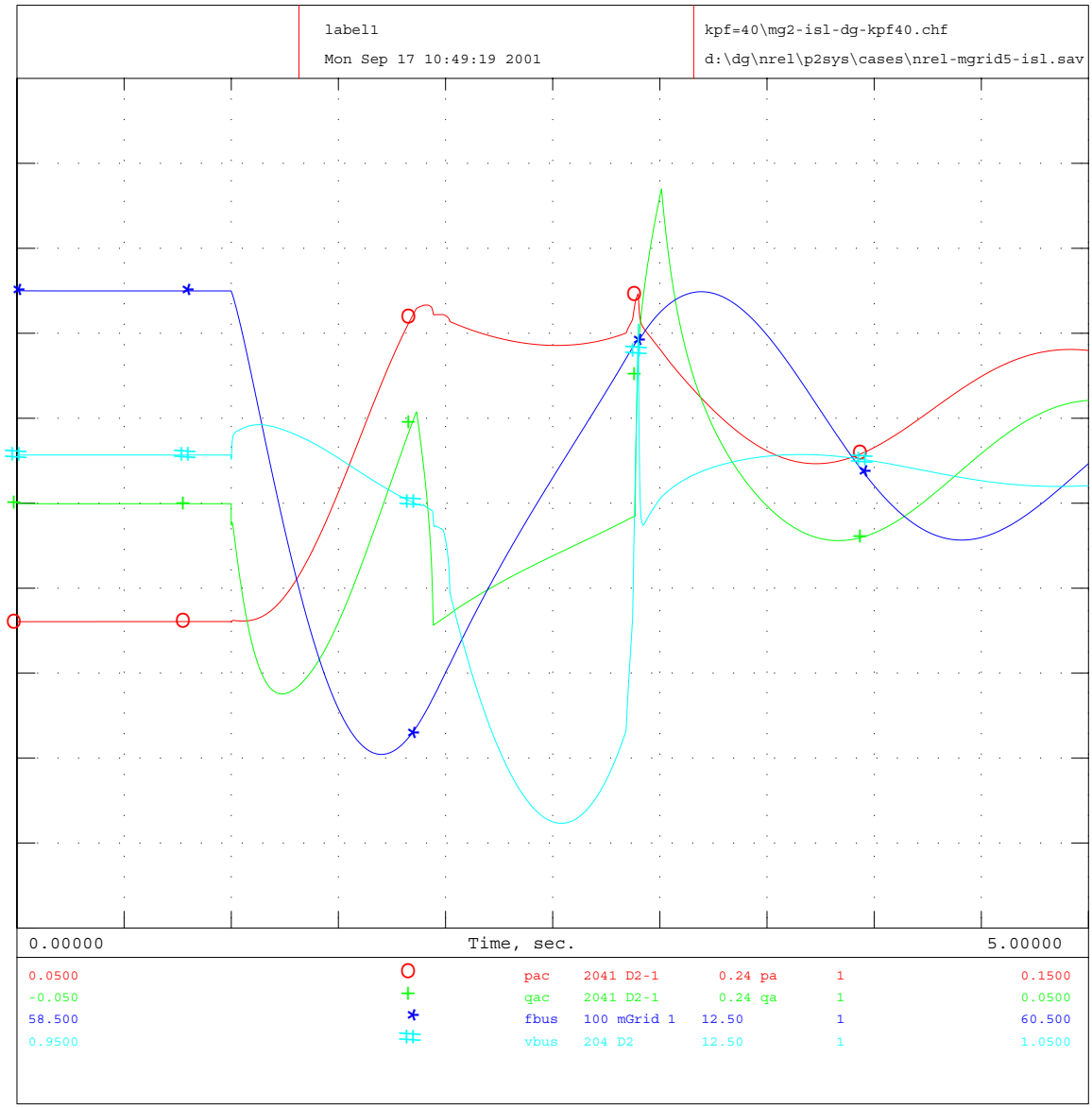
This case helps illustrate several points of interest. First, it is possible for microgrid with autonomous DG controls to tolerate upsets and operate stably. Second, it shows that the behavior of the DGs when pushed against limits can be an important factor in whether a system survives an upset. The case illustrated shows only one possible control response to hitting limits. Others could be devised and have been proposed. It is not clear from this one example, which control strategy is most robust and likely to give the best performance over the widest range of possible conditions.

Microgrid dynamics with supervisory control

The cases above show that autonomous controls of DG hold promise for providing acceptable dynamic performance in the time immediately following system upsets. Coordinated or supervised control may widen the window of events that can be successfully tolerated by the microgrid. Another aspect of microgrids mentioned in the introduction to this section, is the potential to provide a controlled and limited burden on the host utility. In order for the entire microgrid to present such a limited burden requires some type of supervisory control. In this section, one such supervisory control is tested.

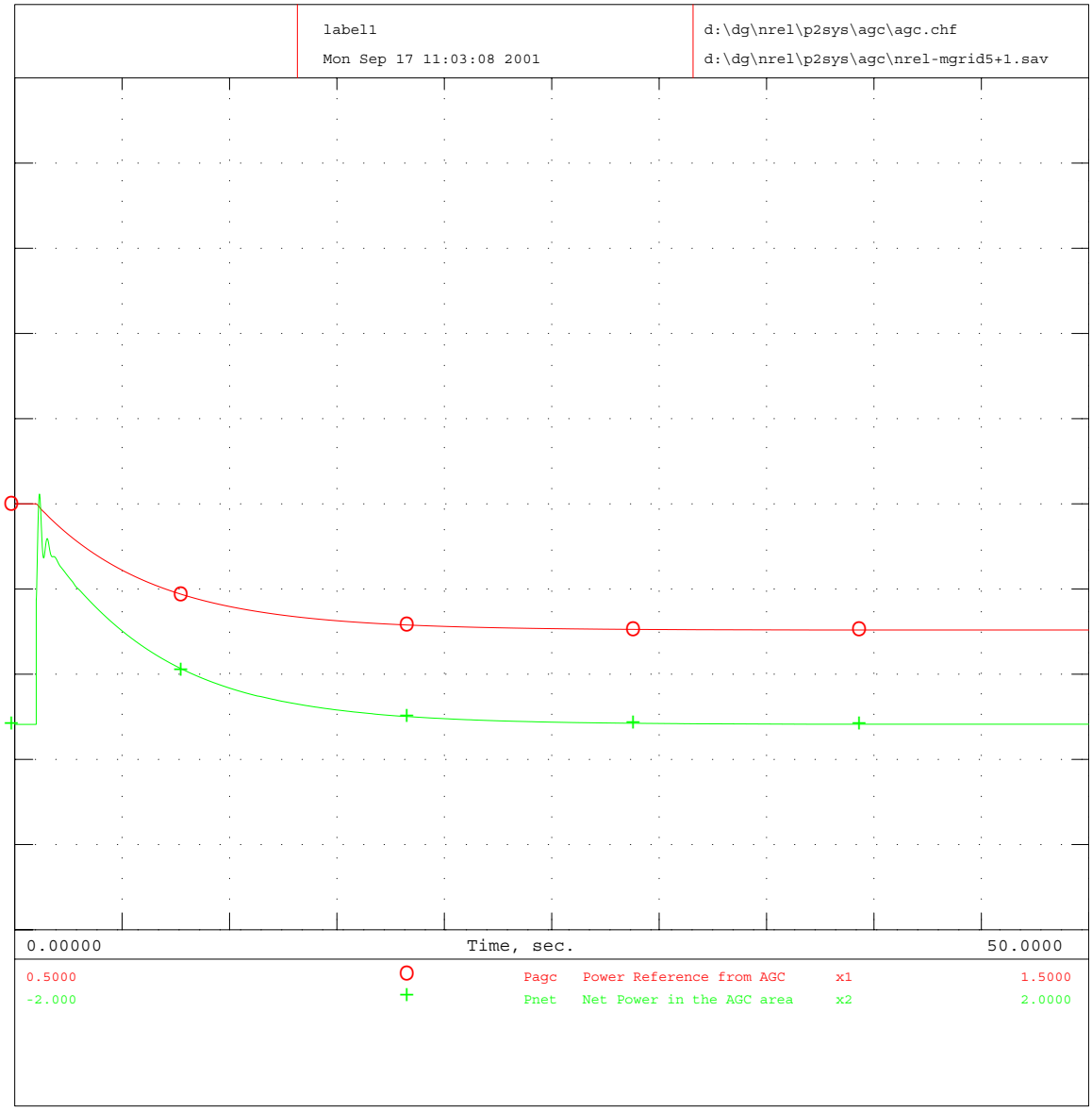
The case shown here is the microgrid response to a load trip. For this case, the micro grid initially exports power to the host grid. The supervisory controller is based on a typical automatic generation control (AGC) that would be used to control power exchange between two bulk power systems. In this case, the objective of the supervisory control is to quickly return the power exchange between the microgrid and the host grid to a specified level. The traces in Figure 76 show (1) the power exchange with the grid, measured at the substation (the green trace with crosses) and the (2) power command signal sent to the DGs within the microgrid that are under supervision. For this control, deviation of the power exchange with the grid from the initial condition provides the input signal (error) to the controller. The output signal commands the DGs on the microgrid to adjust their output—downwards in this case. For this event, the power is returned to the scheduled level within a minute. This response could be made faster or slower, depending upon the physical and contractual requirements of the systems. Appendix G includes figures with show voltage, frequency and active and reactive power traces for this case.

This case illustrates that a microgrid could be controlled in a similar way to that of a large utility grid, so as to minimize the microgrid's impact on the host utility.



Load Trip
System 2
Trip DG at buses 1061

Figure 75. Response of to trip of one DG on microgrid initially operating islanded.



Load Trip
System 2
Trip loads at buses 201 and 2071

Figure 76. Power exchange and control response to load trip within the microgrid with power balancing supervisory control.

4.4.5 Power system dynamics summary

The presence of distributed resources on the power system has the potential to affect system dynamics. Several cases were presented in this section, which help illustrate these effects. The cases cannot be considered comprehensive enough to allow definitive conclusions to be drawn, however, several observations about the behaviors presented can be made:

Observations on local dynamics

- Local distribution system dynamics are most affected by DGs trips.
- DG controls do not have a major impact on local dynamics when the connection to the host utility is maintained.
- Anti-islanding schemes (of the type tested here) appear to be effective at destabilizing islands containing multiple DGs and loads with relatively complex dynamics.
- Voltage and power regulation tend to act contrary to the anti-islanding schemes.

Observations on bulk system dynamics

- Widespread penetration of DGs *at the load* appears to be benign with respect to system response to bulk system disturbances.
- Anti-islanding schemes (of the type tested here) appear to have little impact on system response to bulk system disturbances.
- Aggressive tripping of DGs in response to undervoltages appears to present a substantial hazard to the bulk system, and was shown to bring down the entire U.S. western system in one extreme case.

Observations on microgrid dynamics

- Microgrids appear to be viable, within limits, when DGs are provided with fast autonomous voltage and frequency controls.
- Microgrid supervisory control was shown to provide satisfactory performance in terms of managing power exchange with the host utility (for one illustrative case.)

5. Summary

Future electric power systems should be versatile and flexible so electric energy can be freely generated, transmitted, distributed, and consumed. This program will develop requirements that support the definition, design, and demonstration of a DG-EPS interconnection interface box that allows DG sources to be interconnected to the EPS in a manner that provides value to the end user without compromising reliability or performance. The first major task of this program is to study the DG-EPS interconnection issues using a GE-designed virtual test bed (VTB). The VTB is a simulation platform suite that includes EPS, DG, and load models.

As part of this program's effort to develop a DG-EPS interconnection interface box that allows DG sources to be interconnected to the EPS, various DG-EPS interconnect cases were studied by conducting simulations utilizing the GE-designed VTB as described in Models and Virtual Test Bed Report (reference). The results from these case studies will enable us to make recommendations for improvement to the IEEE P1547 standard as well as provide inputs to the design of the interconnection interface box.

The set of simulations run on the VTB were based on a case list compiled by the team from various brainstorming sessions, IEEE P1547 Draft Standard, Edison Electric Institute Distributed Resources Task Force Interconnection Study, and literature searches. The cases studied are grouped into two categories: power quality case studies and protection and reliability case studies.

The power quality case studies include:

- Voltage regulation
- DG design considerations to meet power quality requirements:
  - Harmonics
  - Flicker
  - DC current injection
  - Grounding
  - Unbalanced grid

The protection and reliability case studies include:

- Transient response and fault behaviors:
  - Capacitor switching
  - Fault Behaviors
- Reclosing
- Anti-islanding studies
- Power systems dynamics and stability

Some key findings from these initial studies of the impact of DG-EPS interconnect include the following:

- Widespread penetration of DGs at the load appears to be benign with respect to system response to bulk system disturbances.
- With significant levels of DG penetration, it will be difficult to avoid detraction from EPS voltage regulation performance., While IEEE P1547 presently requires that a DG not cause the EPS voltage to all outside of the prescribed regulation range, achieving this goal may become increasingly difficult using conventional approaches. EPS voltage regulation performance problems due to DG can be mitigated if there is integrated control of system voltage and reactive power management. IEEE P1547 may need to incorporate provisions where the reactive power output of the DG is controlled by the EPS operator.
- Simultaneous tripping of DGs in a system dependent on the DG output can result in widespread and severe voltage problems. Presently, P1547 is biased in favor of fast tripping in order to rapidly detect and eliminate inadvertent islands. There may need to be further consideration of the fine balance between island avoidance and making the system vulnerable to voltage collapse.
- Anti-islanding schemes (of the type studied in this project) appear to be effective at destabilizing islands containing multiple DGs and loads with relatively complex dynamics while having little impact on system response to bulk system disturbances. This is a highly complex subject, and further investigation is highly desirable.
- Inverter-type DGs will have significant beneficial impact on flicker caused by system loads, only if they have a voltage regulation function or if they have a control scheme where they are operated as controlled voltage sources (i.e., as virtual synchronous generators).
- Modern inverter-based DGs do not contribute to system fault current beyond the pre-fault operating current level. However, the current contribution of the DG system to a single phase fault may be greater than the three phase case which conflicts with IEEE P1547 requirement that ground fault current contribution of a DG shall not be greater than 100% of the fault current contribution of the DG to a three phase fault. This is because the DG is a nearly ideal current source for the positive sequence, but is generally a constant impedance or voltage

source for the zero sequence. Both are desirable characteristics, and the result reveals that the wording of P1547's single-phase to three phase fault current ratio requirement is more appropriate for conventional rotating generators. The wording of this requirement needs additional consideration with respect to its consistency with inverter-based applications.

- Take-aways for future DG designs:
  - Single phase Sandia Anti-islanding scheme can be effectively extended to 3 phase DG systems;
  - Inverter based DGs will have significant beneficial impact on flicker only if they include a voltage regulation function;
  - DG voltage regulation functionality may be beneficial in reducing the impact of DG penetration on EPS voltage regulation performance. However, local control may not be sufficient and a system level voltage control approach may be necessary in many applications.
  - DG voltage regulation may reduce the effectiveness of active anti-islanding schemes.
  - Transformer-less DGs should pay special attention to zero-sequence impedance design so an effective ground can be provided.

The GE-designed interconnect interface box will address some of the issues identified above, such as integrated control of system voltage; reactive power management; and communication to a supervisory level to manage microgrid power exchange.

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Appendices

Appendix A.
Global Voltage Range Plots for Generic Feeder Voltage Regulation Analysis Cases

This appendix provides plots of the global maximum and minimum voltage results for each voltage regulation case performed using the generic radial feeder models, as a function of DG penetration. The global maximum and minimum voltages are the maximum and minimum primary voltages anywhere on the feeder, for either peak or minimum system loading. The global maximum and minimum for each case are usually not for the same location nor the same load level. These plots summarize the overall voltage regulation performance, and clearly indicate the DG penetration level where voltage regulation issues become significant.

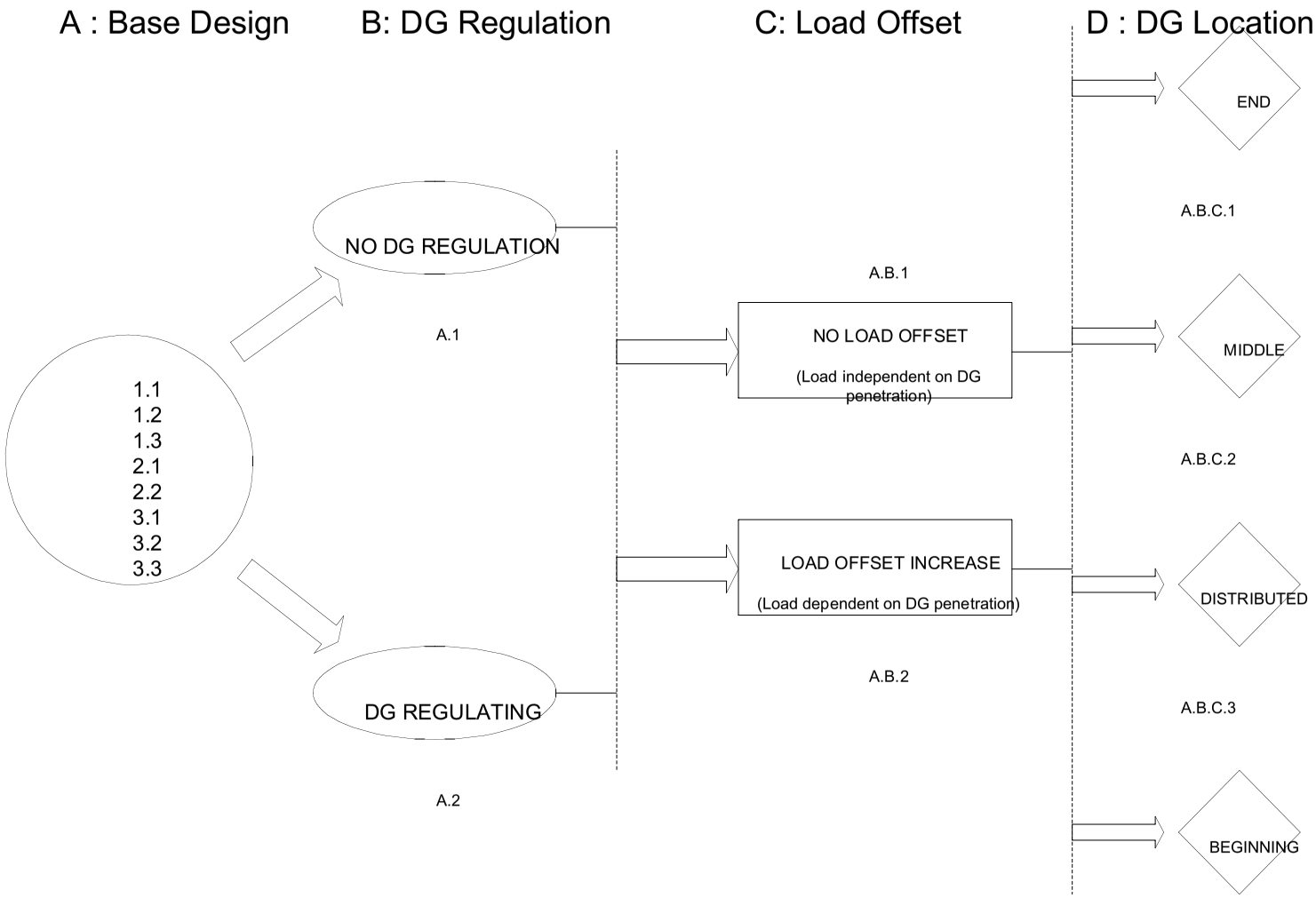
The solid lines in the global voltage range plots indicate the range for the DG operating at 100% of capacity. Because the DG might operate at any power level between 0% and 100%, the full voltage range must also include voltages where the DGs are not generating. This is equivalent to the voltage range at 0% DG penetration. Where the voltage range for 0% DG output is outside of the range for 100% output, then the extended range is shown by broken lines in the plots, labeled reference max and reference min .

Case Key

A total of 128 sub-cases were performed, as indicated by the case tree structure illustrated on the following page. Within each sub-case, loadflow analyses were performed for two load levels and six DG penetration levels in order to generate the global voltage range plots shown in this appendix. Thus, a total of 1,536 individual loadflow cases were performed.

The case tree structure shown on the next page indicates the sub-case numbering scheme used to identify voltage range plots in this appendix. Also, each plot has a label which can be interpreted as follows:

1. **DG Location** (DG at End, DG at Middle, DG at Beginning, DG Distributed, self-explanatory)
2. **Load Change Scenario** (No Offset feeder load independent of DG penetration, Offset Increase — feeder peak load increased an amount equivalent to DG capacity)
3. **DG Voltage Regulator Implementation** (No DG Regulation, DG Regulating refer to whether the DG reactive power output is controlled to regulate the local bus voltage



Example:
8-mile feeder with LTC Tap =1.01, R LDC=0.75, X LDC=1.5, w/o SVR,900 kVA capacitor banks (Base Design 2.1)
No DG Regulation, Load Offset Increase, DG located at the beginning of the feeder..
Label in Appendix is 2.1.1.2.4

BASE DESIGN 1.1

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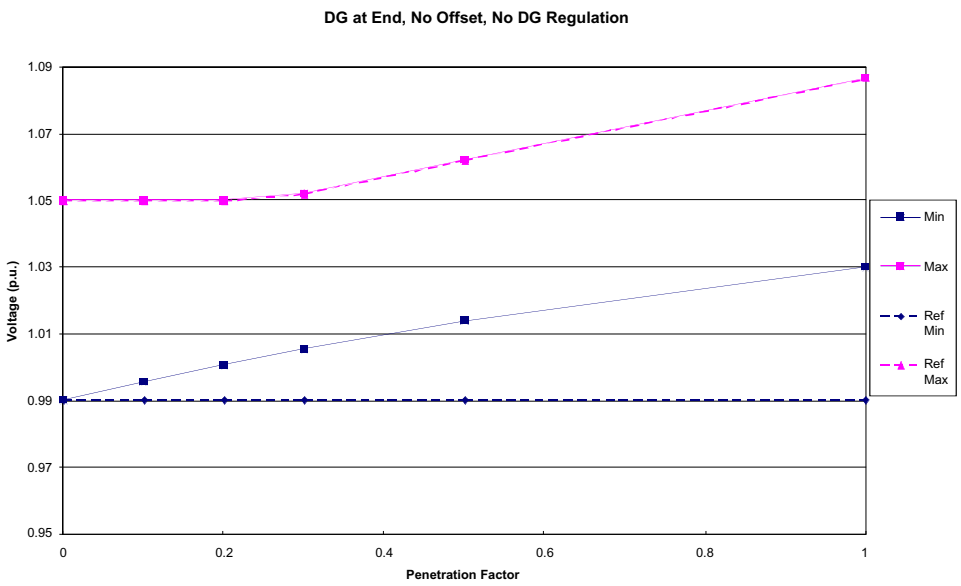

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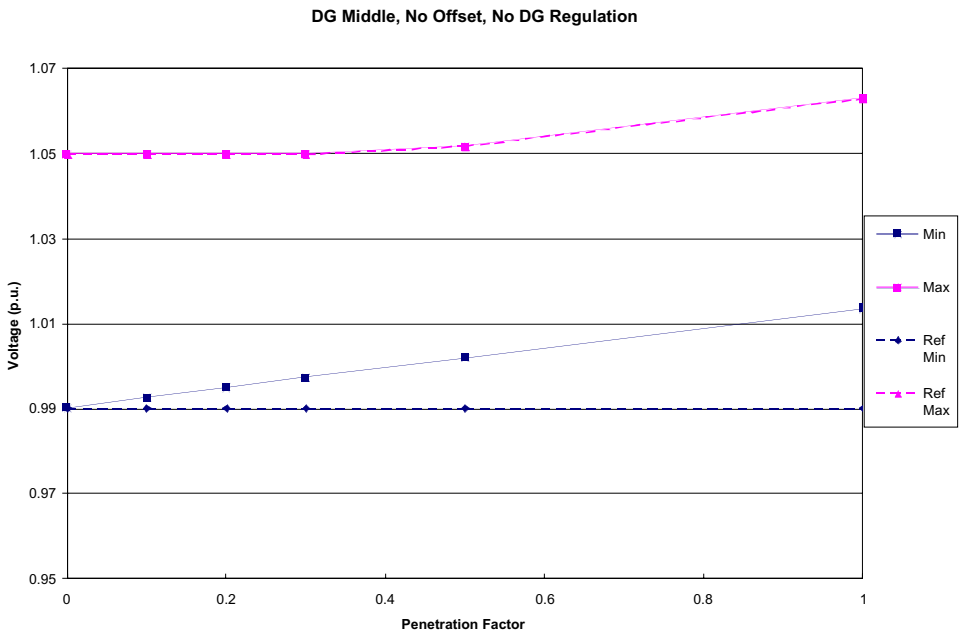

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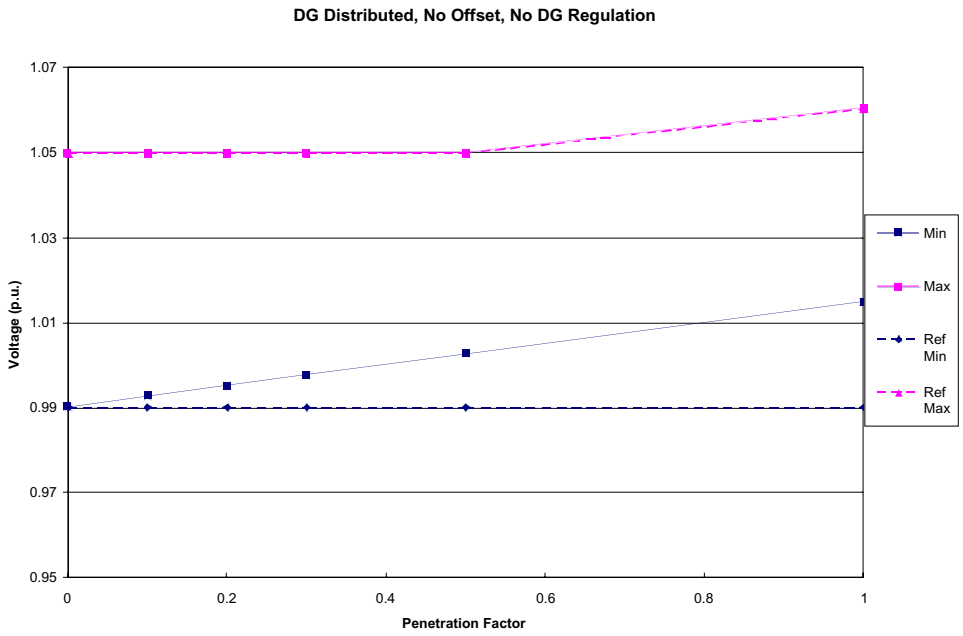
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1.05
1.03
1.01
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0.95
Voltage (p.u.)
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Penetration Factor
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Max
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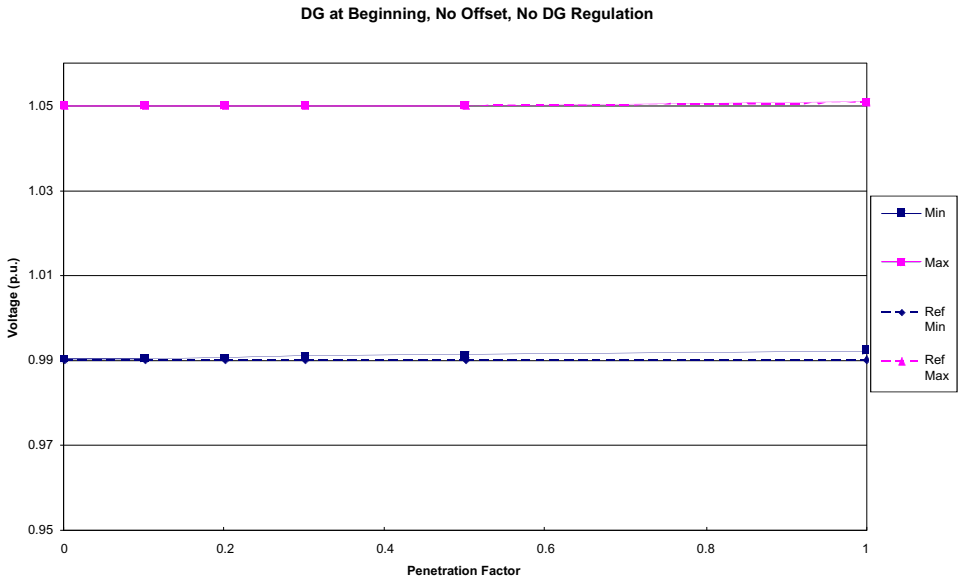
Ref Max

1.1.1.1.4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Voltage (p.u.)
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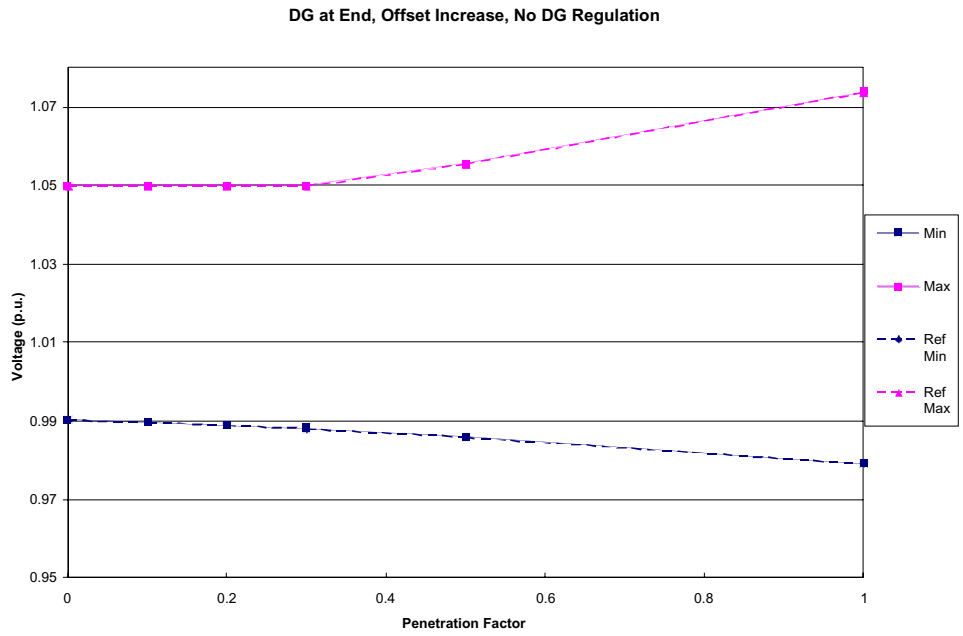
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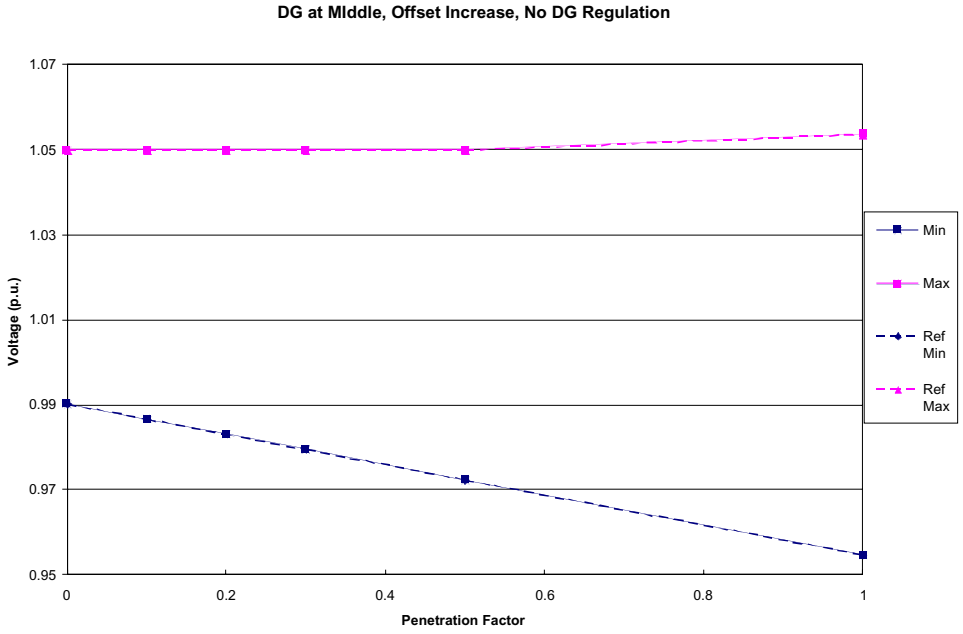
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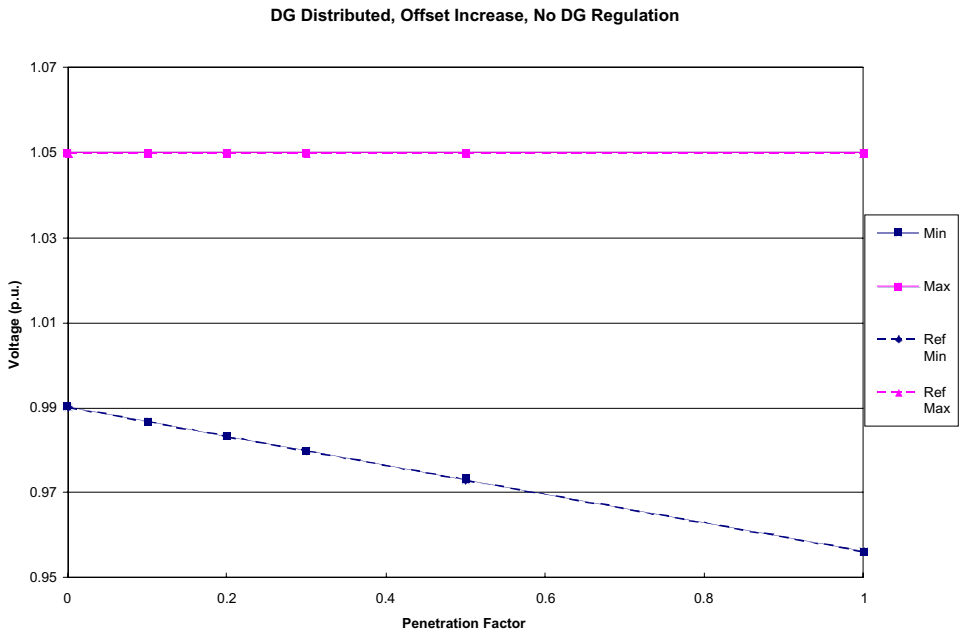
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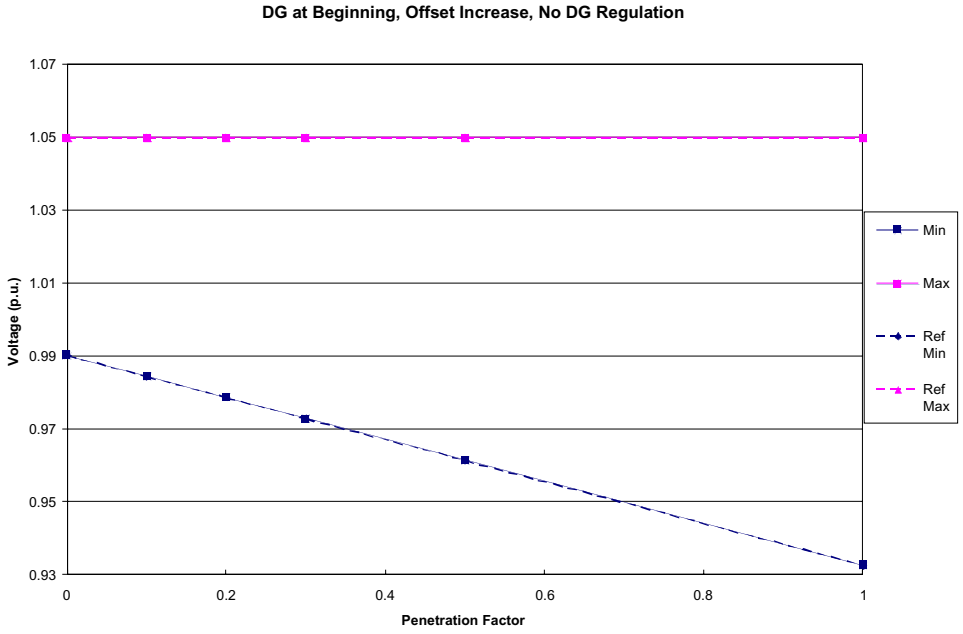
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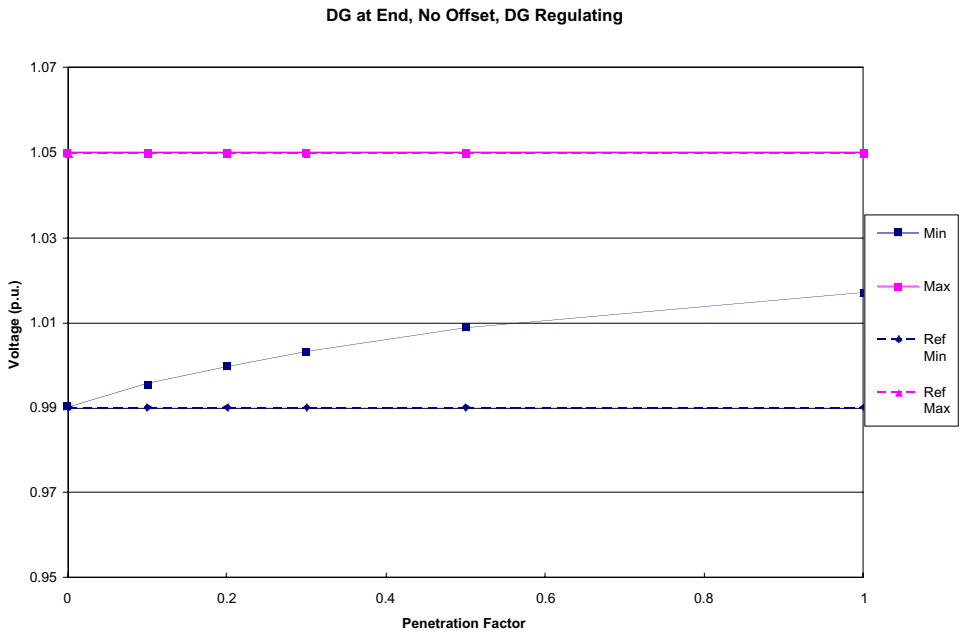
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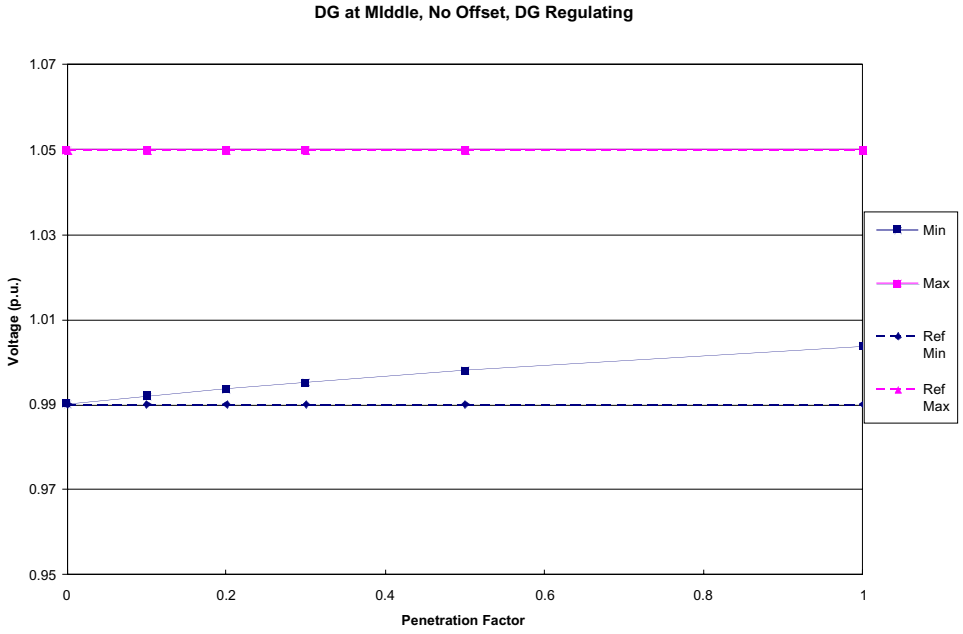
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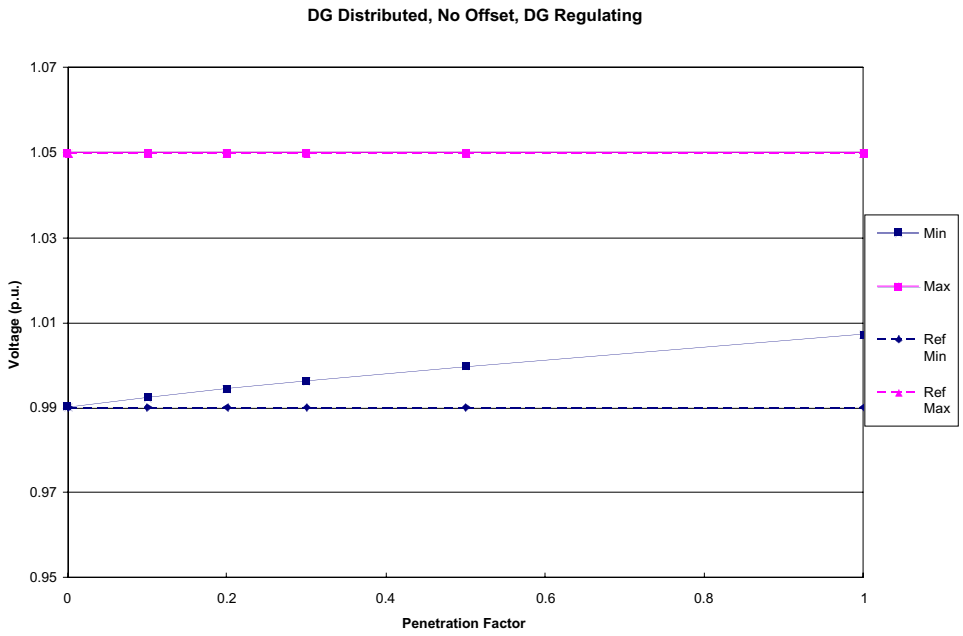
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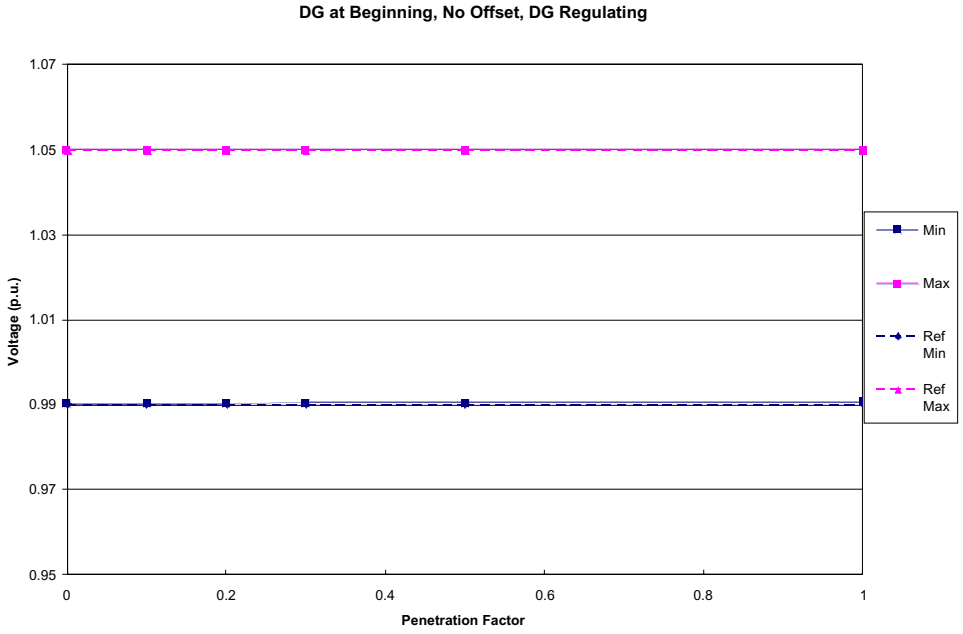
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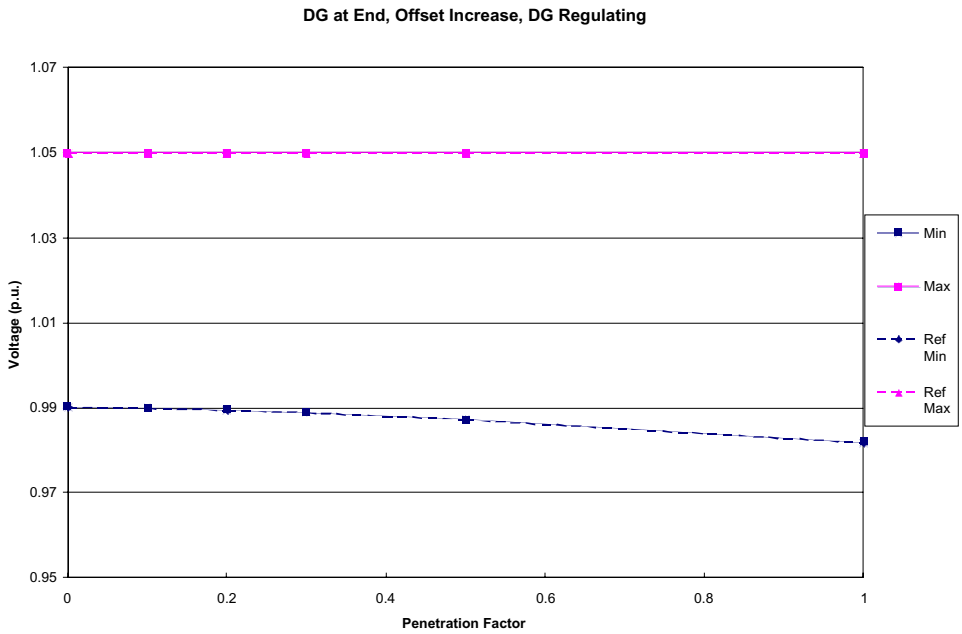
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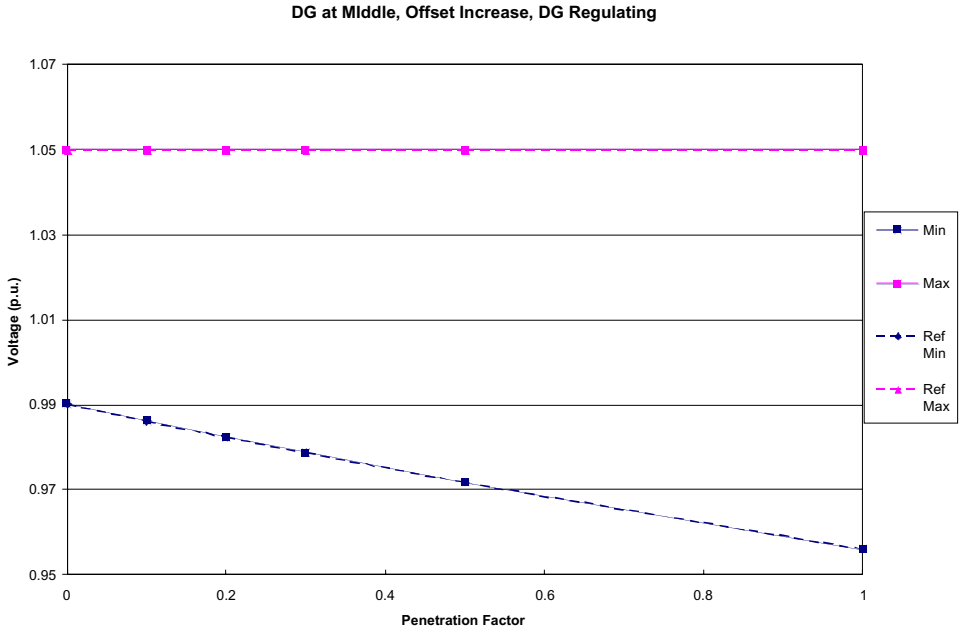
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Penetration Factor
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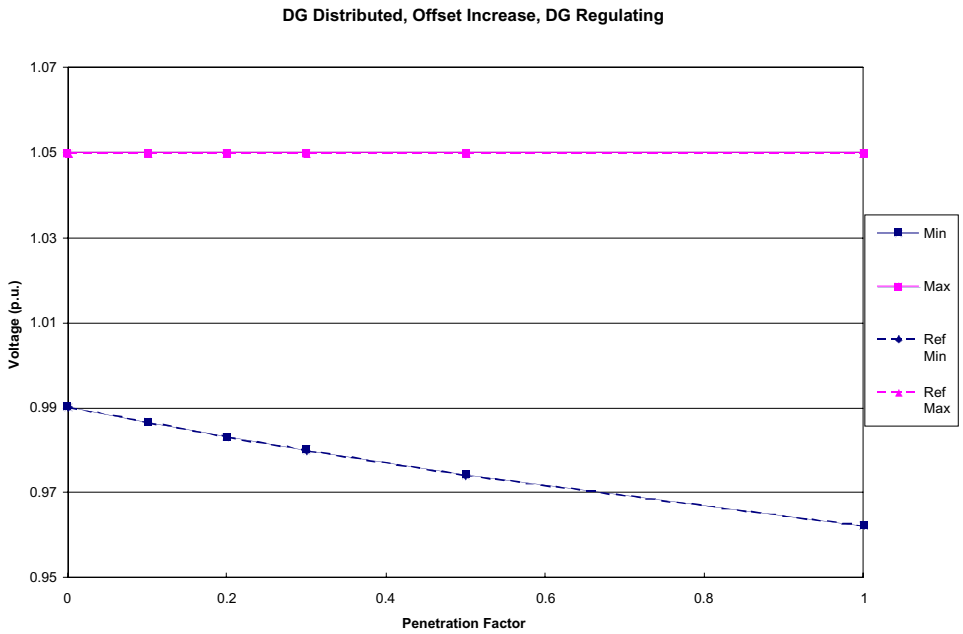
1.1.2.2.3


DG Distributed, Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
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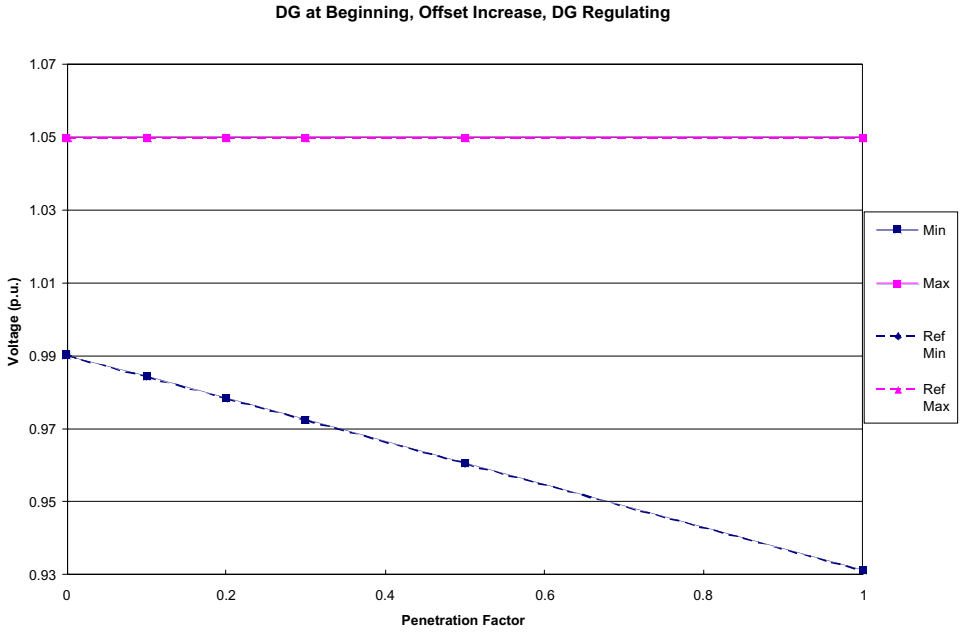
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.1.2.2.4


DG at Beginning, Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
Voltage (p.u.)
0
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0.4
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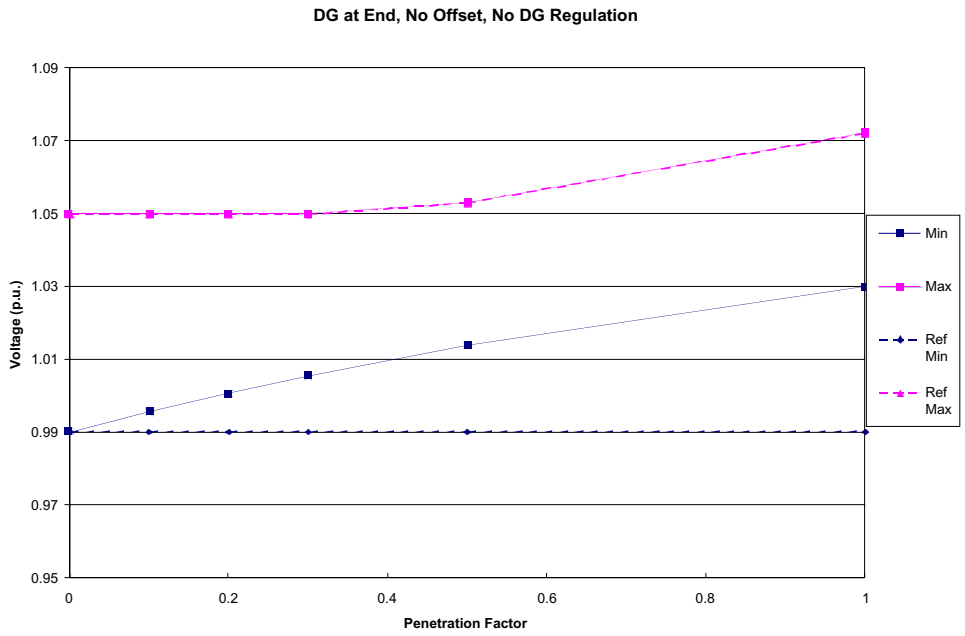
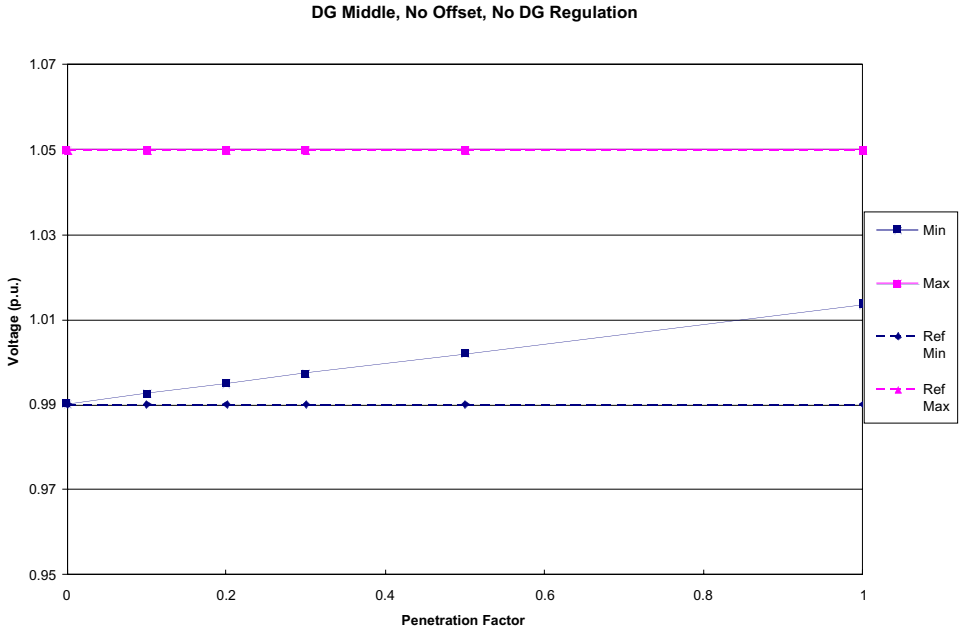
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

BASE DESIGN 1.2

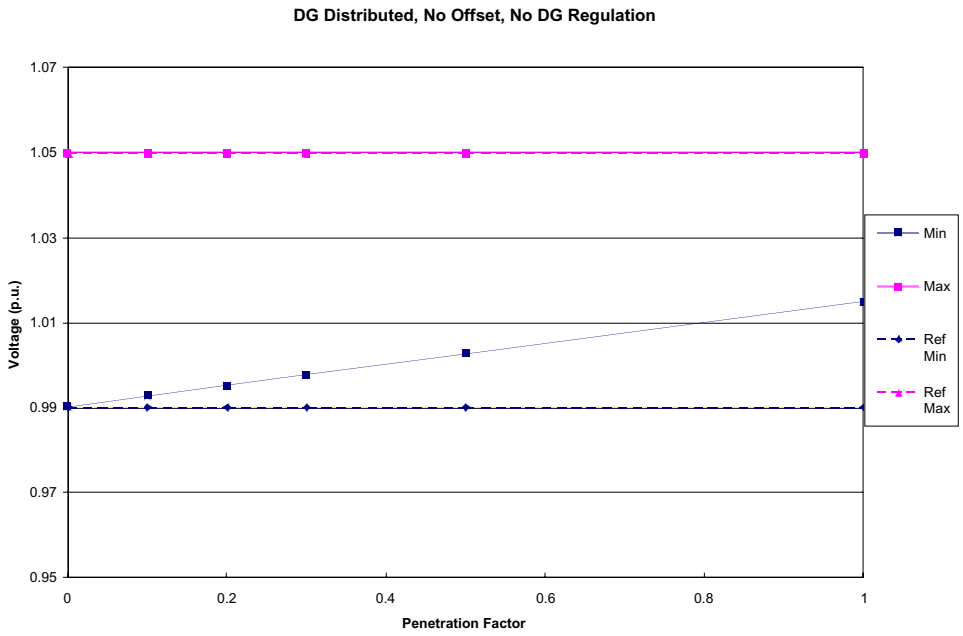
1.2.1.1.1



1.2.1.1.2



1.2.1.1.3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1.03
1.01
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0.97
0.95
Voltage (p.u.)
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0.4
0.6
0.8
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Penetration Factor
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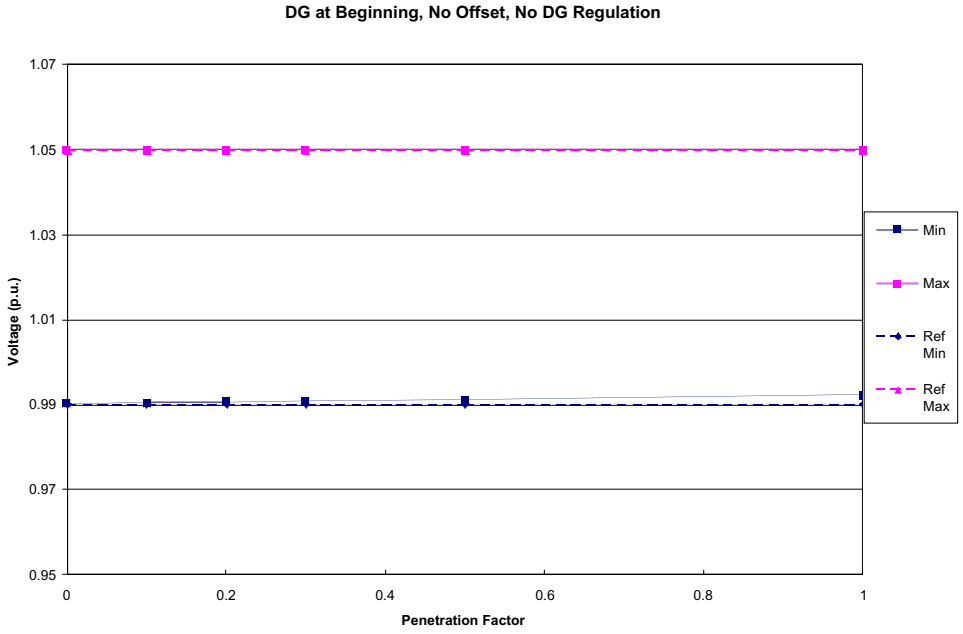
Max
Ref Min
Ref Max

1.2.1.1.4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1.01
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0.97
0.95
Voltage (p.u.)
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0.4
0.6
0.8
1
Penetration Factor
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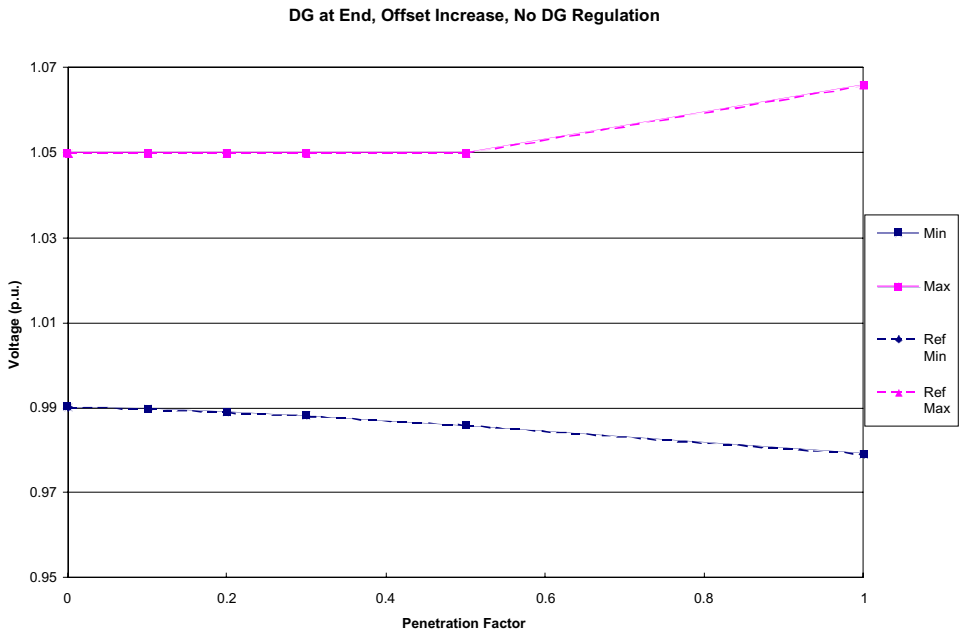
Max
Ref Min
Ref Max

1.2.1.2.1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0.95
Voltage (p.u.)
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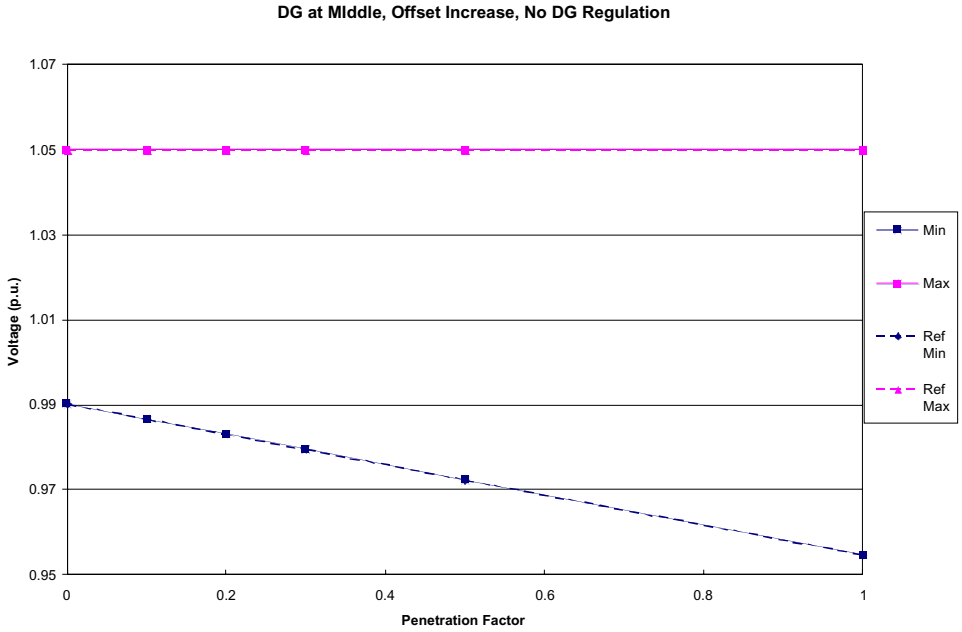
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.2.1.2.2


DG at MIddle, Offset Increase, No DG Regulation
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1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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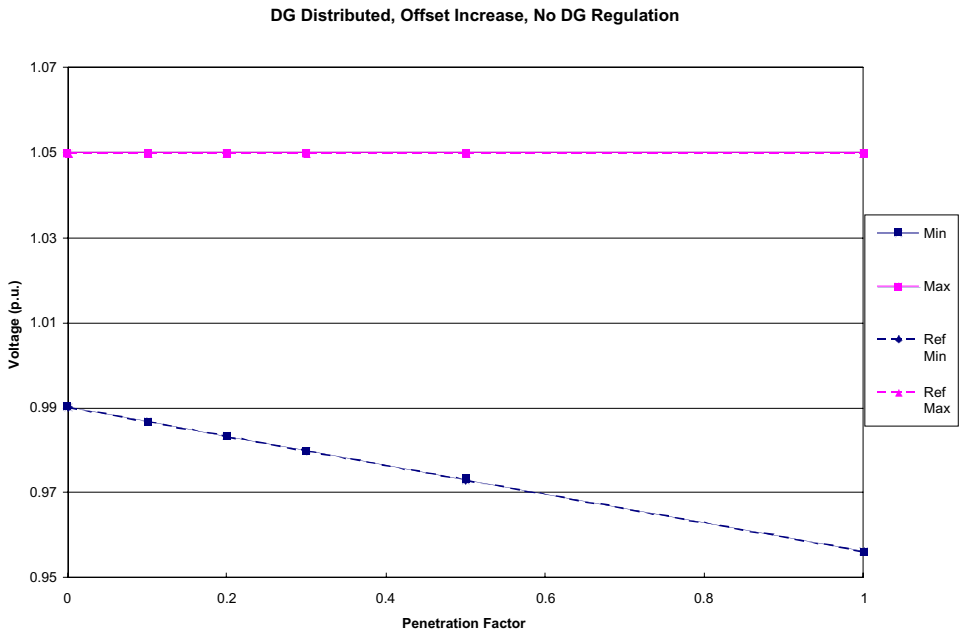
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.2.1.2.3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1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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0.4
0.6
0.8
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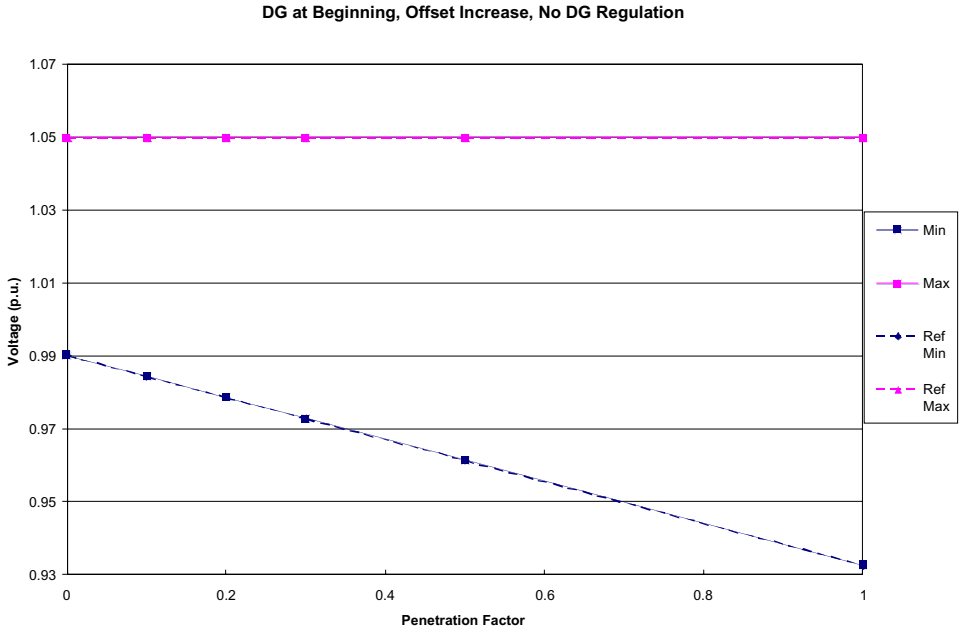
Penetration Factor
Min
Max
Ref Min
Ref Max

1.2.1.2.4


DG at Beginning, Offset Increase, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
Voltage (p.u.)
0
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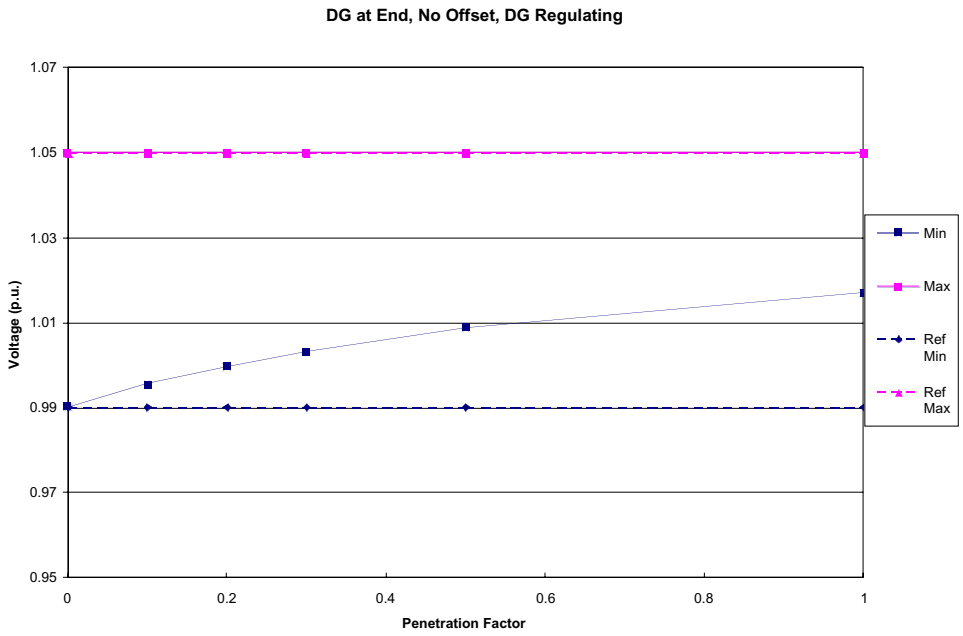
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.2.2.1.1


DG at End, No Offset, DG Regulating
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1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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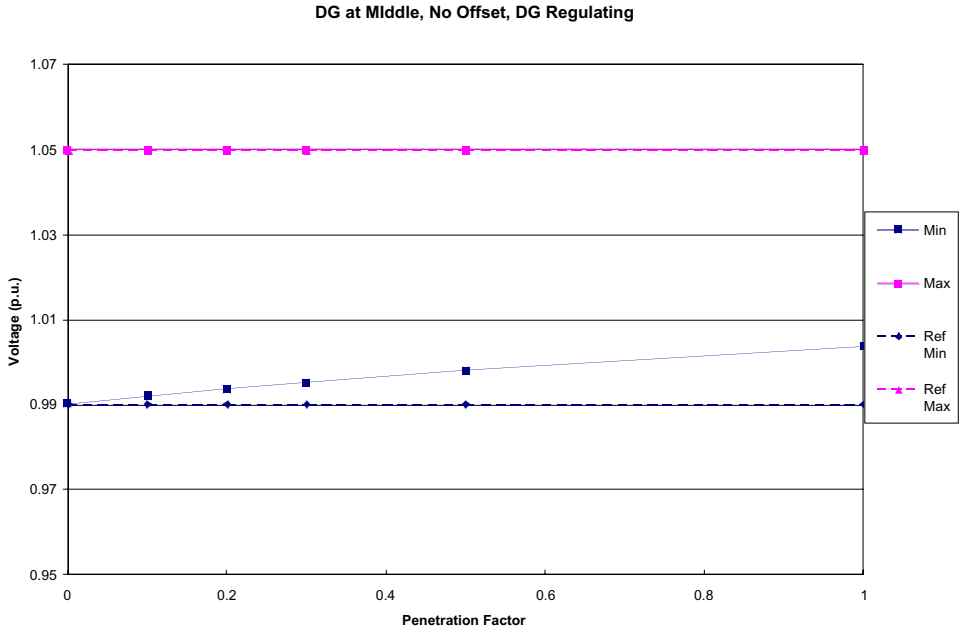
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.2.2.1.2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1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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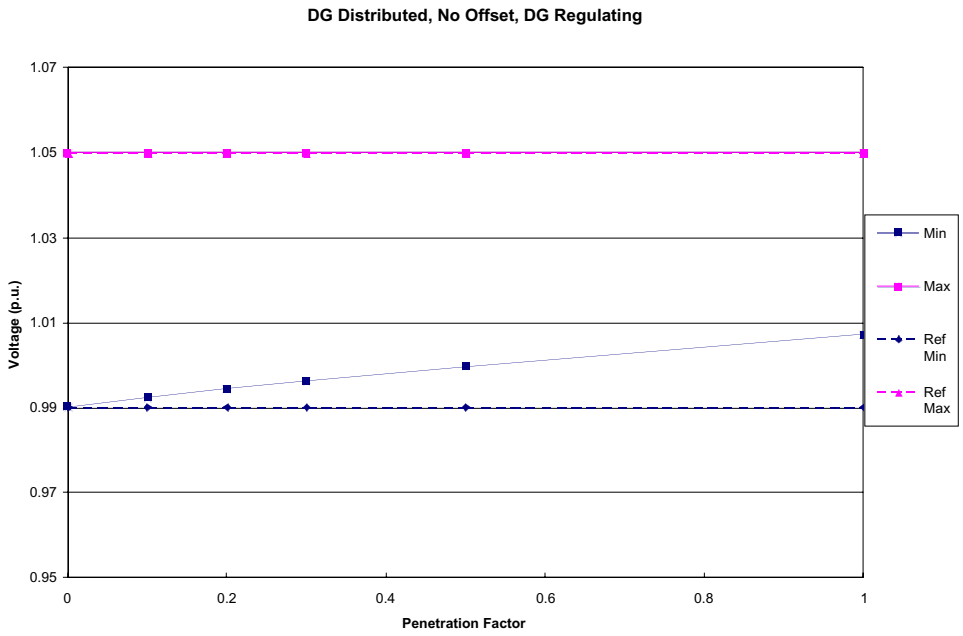
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.2.2.1.3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1.01
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0.97
0.95
Voltage (p.u.)
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0.6
0.8
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Penetration Factor
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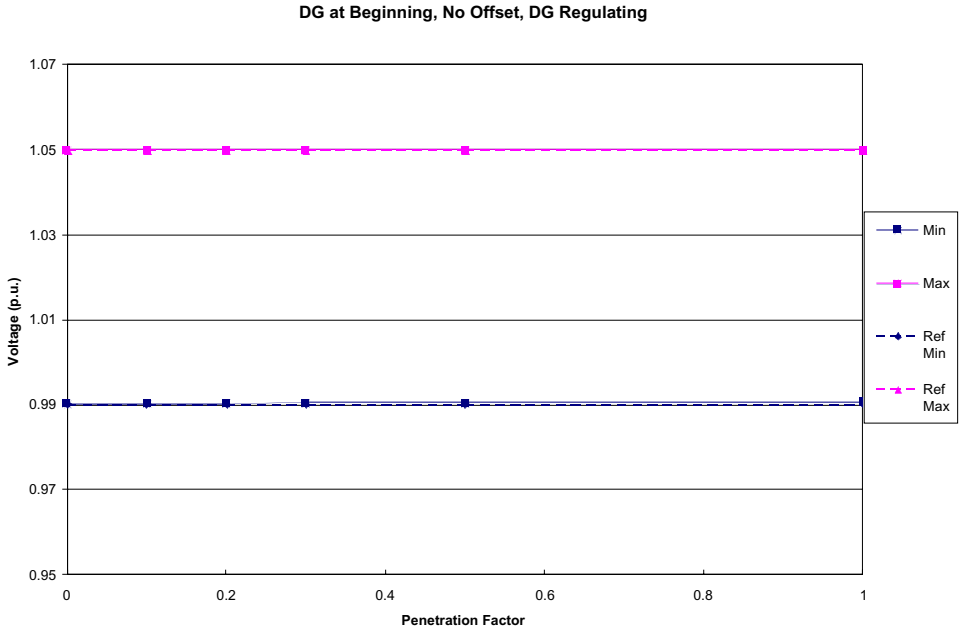
Max
Ref Min
Ref Max

1.2.2.1.4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1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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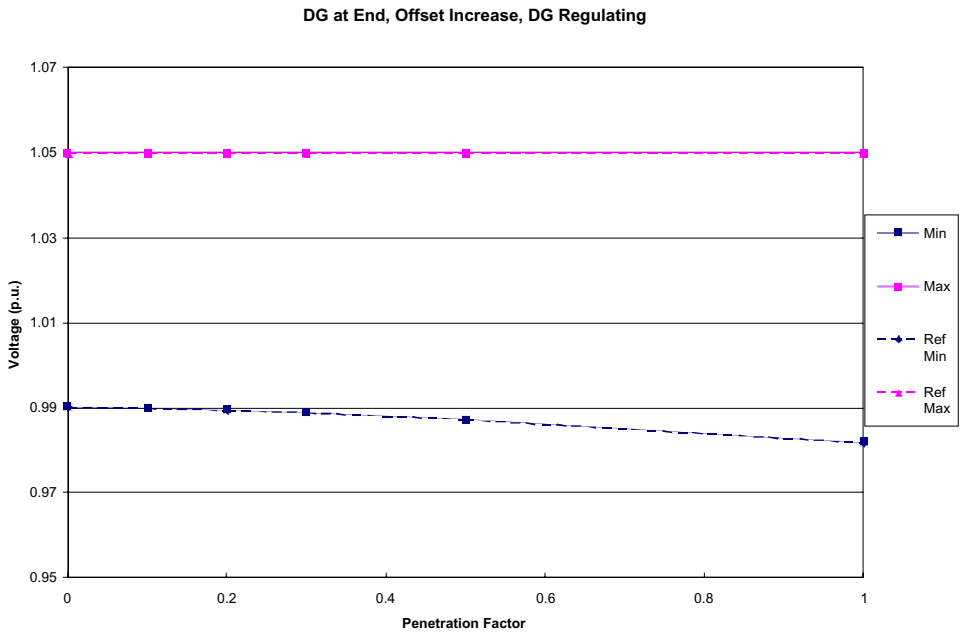
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.2.2.2.1


DG at End, Offset Increase, DG Regulating
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1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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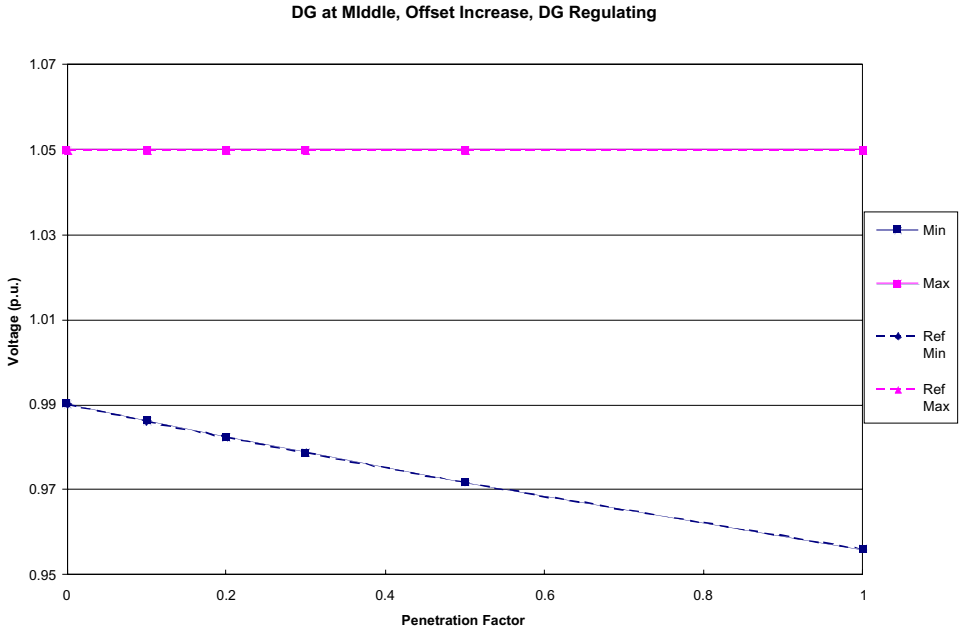
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.2.2.2.2


DG at MIddle, Offset Increase, DG Regulating
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1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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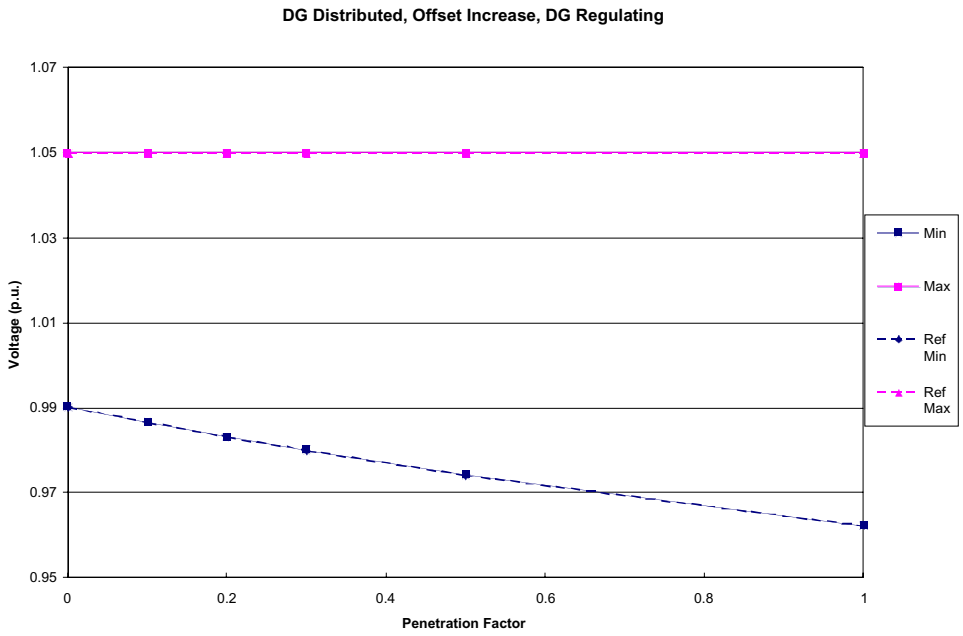
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.2.2.2.3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1.01
0.99
0.97
0.95
Voltage (p.u.)
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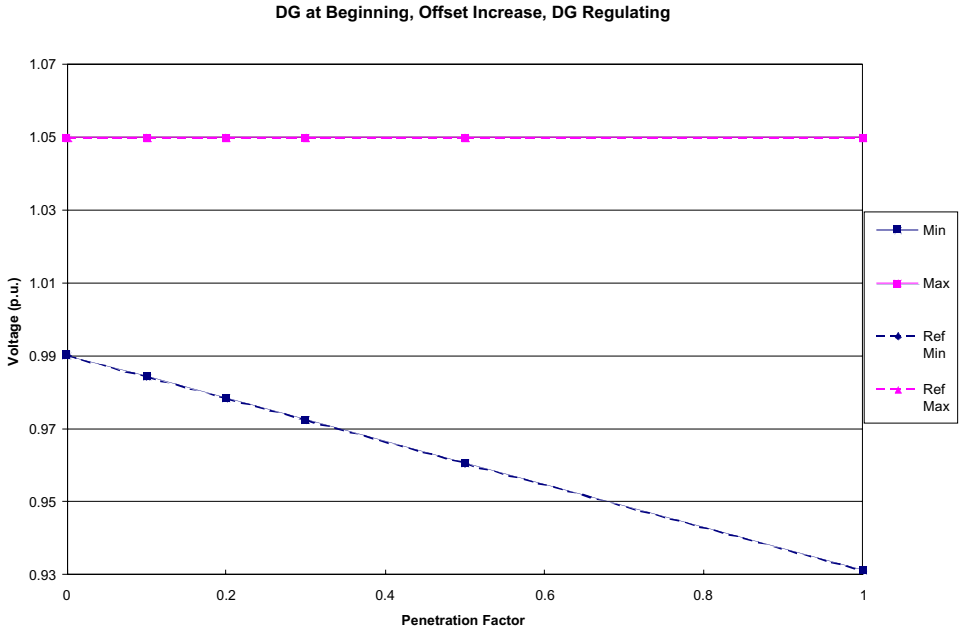
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.2.2.2.4


DG at Beginning, Offset Increase, DG Regulating
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1.01
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0.95
0.93
Voltage (p.u.)
0
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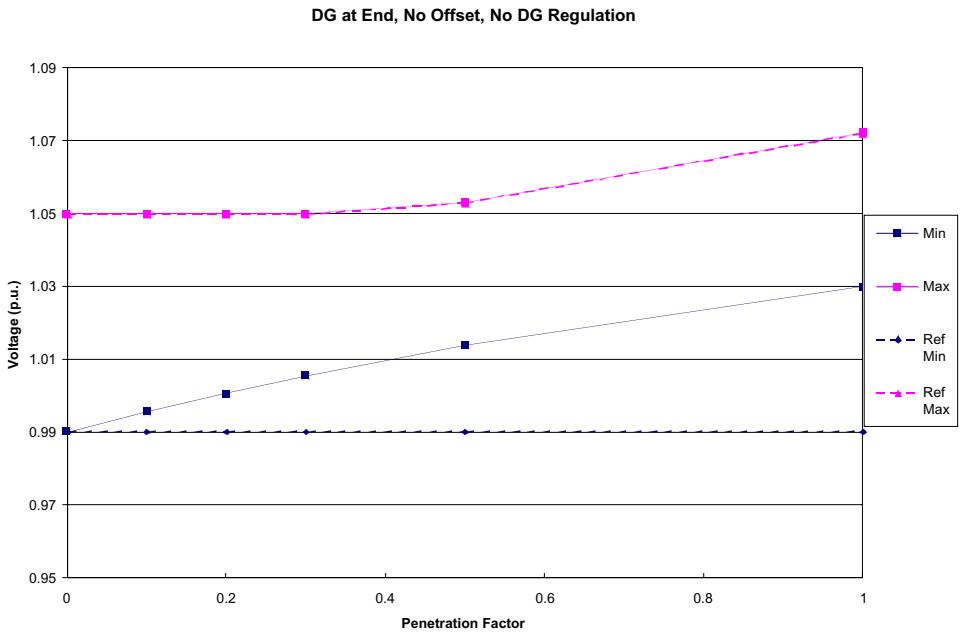
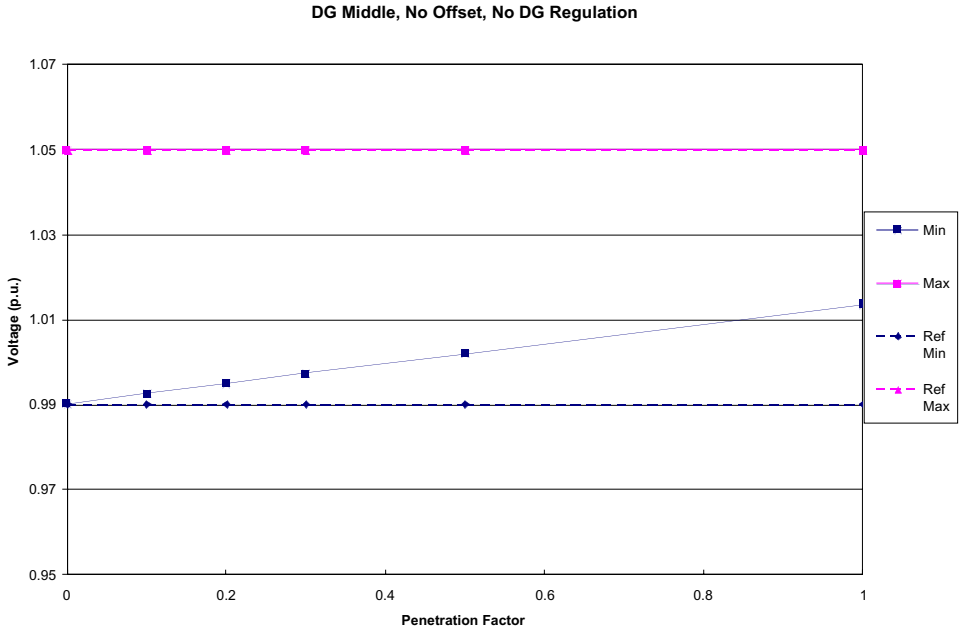
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

BASE DESIGN 1.3

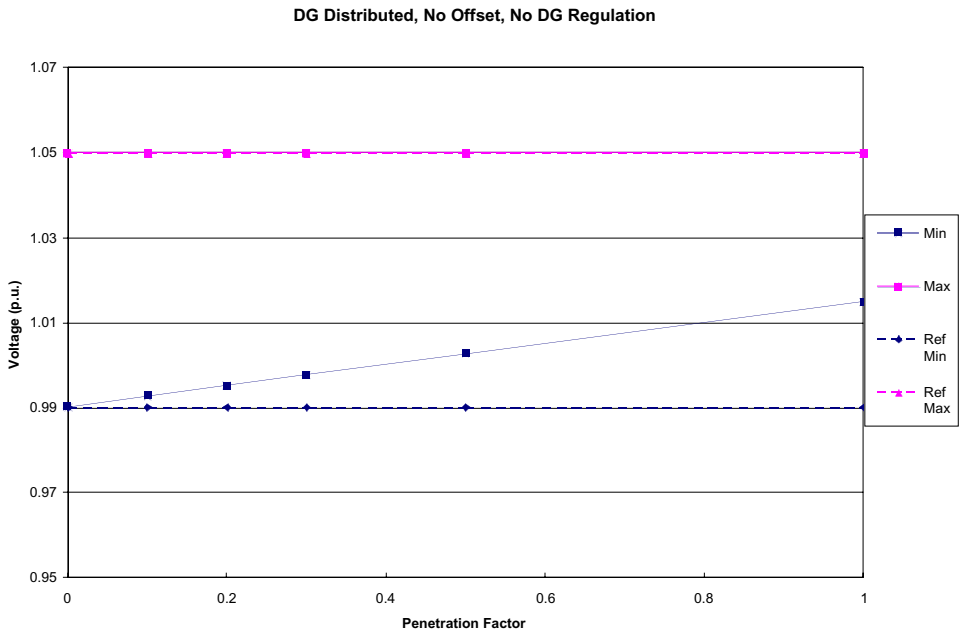
1.3.1.1.1



1.3.1.1.2



1.3.1.1.3


DG Distributed, No Offset, No DG Regulation
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1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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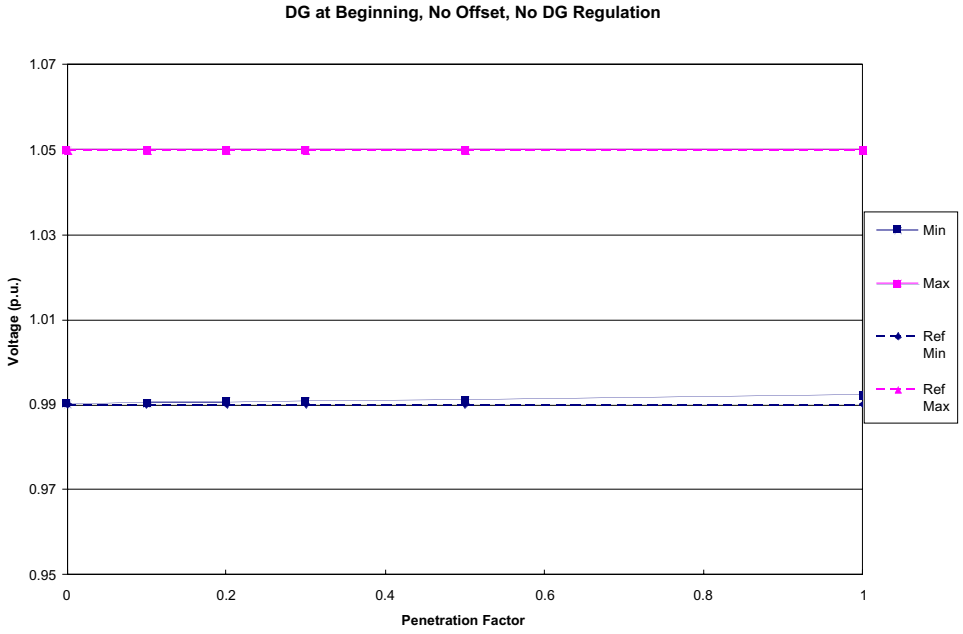
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.1.1.4


DG at Beginning, No Offset, No DG Regulation
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1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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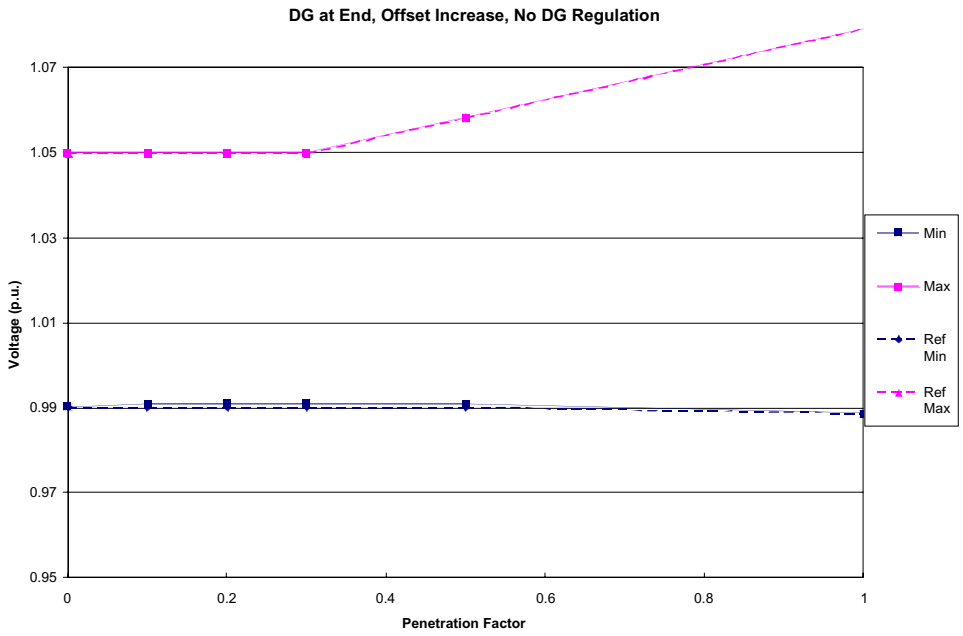
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.1.2.1


DG at End, Offset Increase, No DG Regulation
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1.01
0.99
0.97
0.95
Voltage (p.u.)
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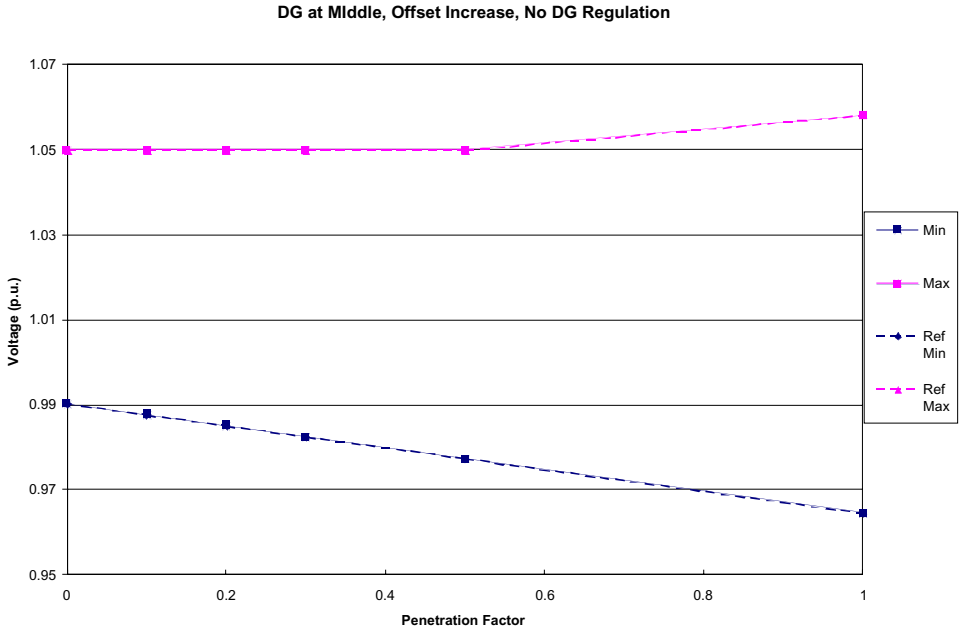
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.1.2.2


DG at MIddle, Offset Increase, No DG Regulation
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1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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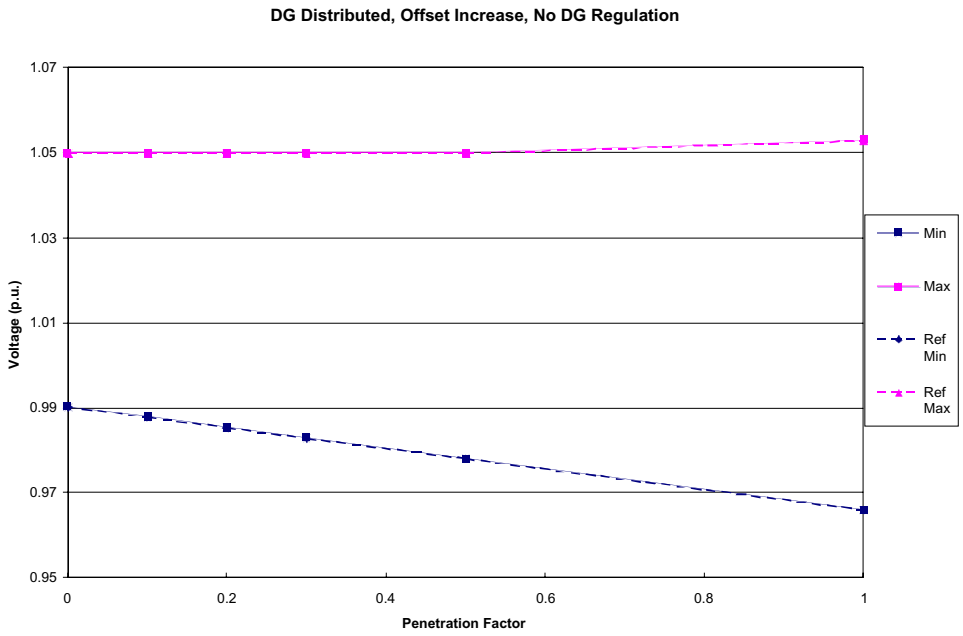
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.1.2.3


DG Distributed, Offset Increase, No DG Regulation
1.07
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1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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0.4
0.6
0.8
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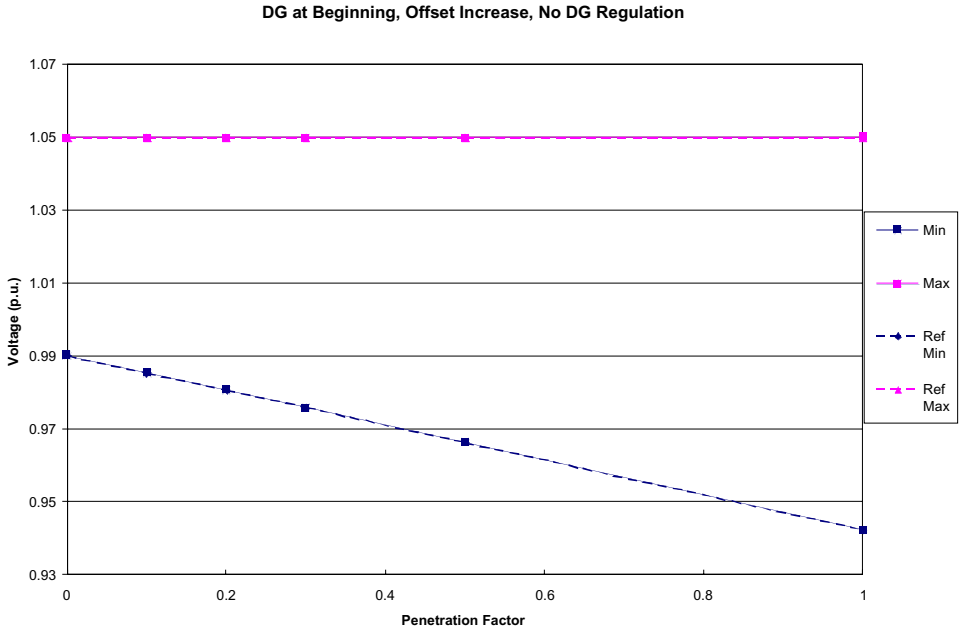
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.1.2.4


DG at Beginning, Offset Increase, No DG Regulation
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1.05
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1.01
0.99
0.97
0.95
0.93
Voltage (p.u.)
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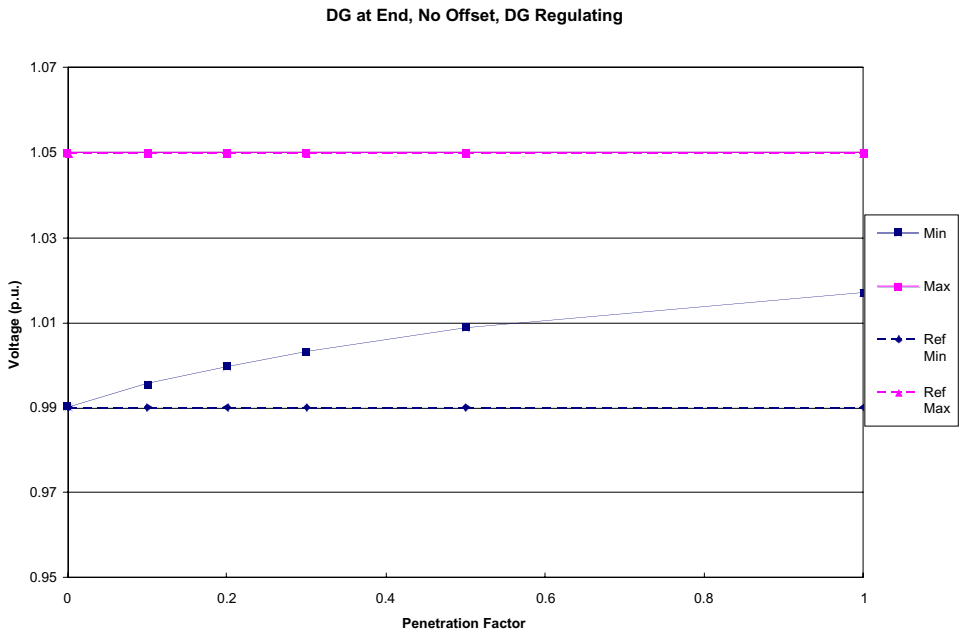
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.2.1.1


DG at End, No Offset, DG Regulating
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1.01
0.99
0.97
0.95
Voltage (p.u.)
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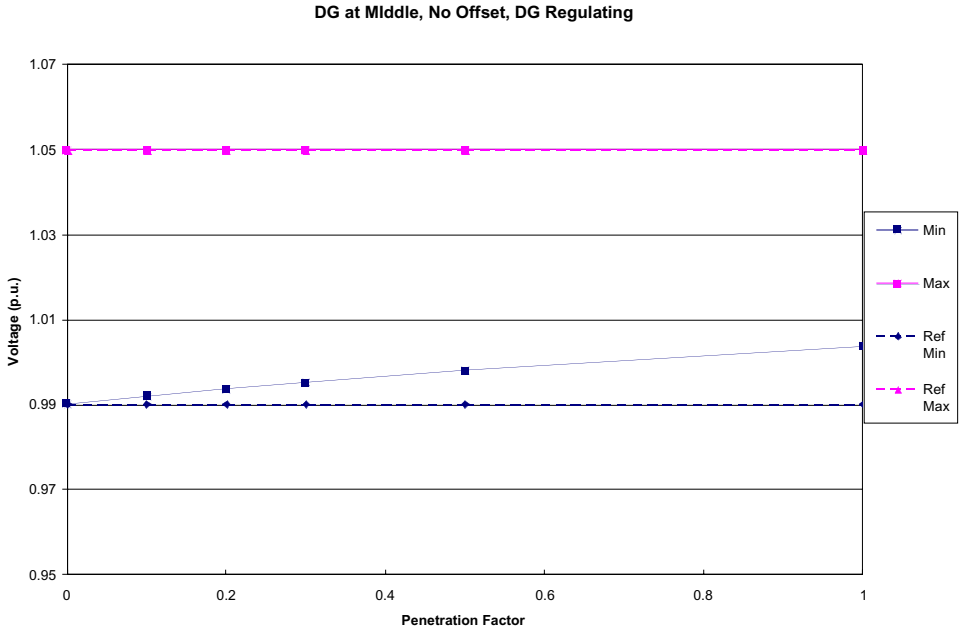
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.2.1.2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0.95
Voltage (p.u.)
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0.4
0.6
0.8
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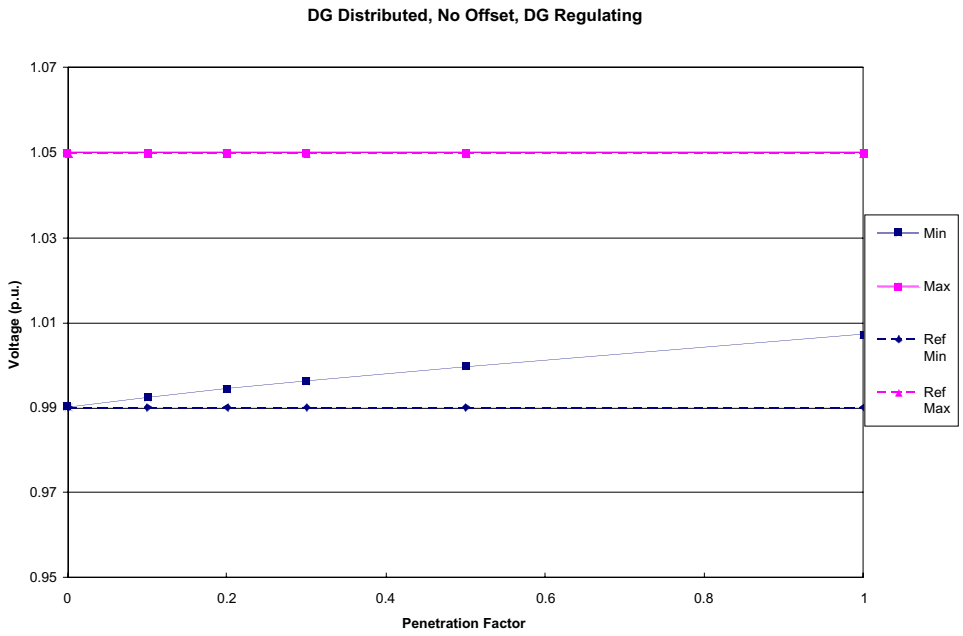
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.2.1.3


DG Distributed, No Offset, DG Regulating
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Voltage (p.u.)
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0.4
0.6
0.8
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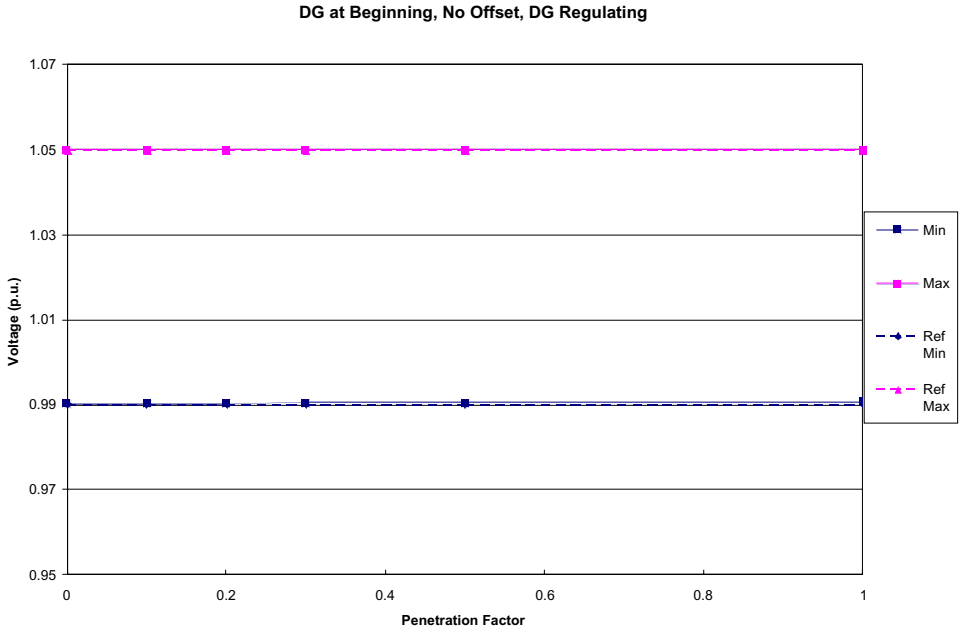
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.2.1.4


DG at Beginning, No Offset, DG Regulating
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0.95
Voltage (p.u.)
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0.8
1
Penetration Factor
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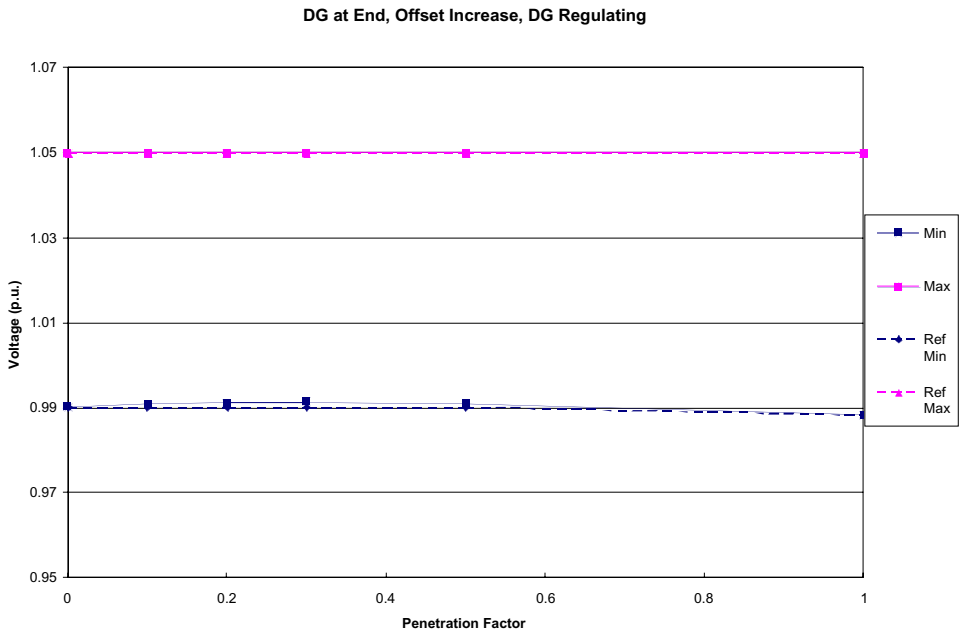
Max
Ref Min
Ref Max

1.3.2.2.1


DG at End, Offset Increase, DG Regulating
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1.01
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0.97
0.95
Voltage (p.u.)
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0.4
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0.8
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Penetration Factor
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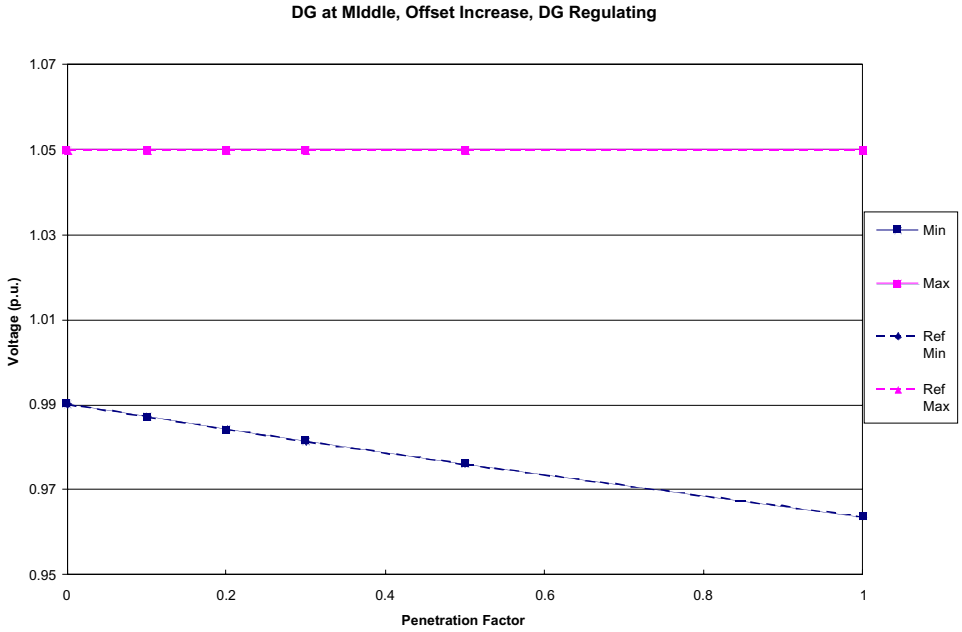
Max
Ref Min
Ref Max

1.3.2.2.2


DG at MIddle, Offset Increase, DG Regulating
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1.01
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0.97
0.95
Voltage (p.u.)
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0.4
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0.8
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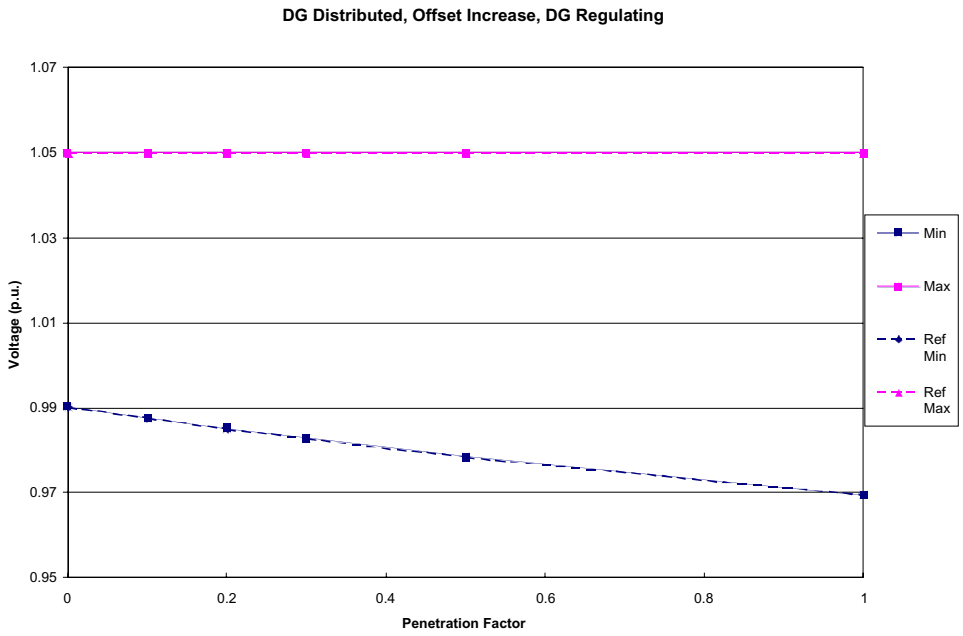
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.2.2.3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1.01
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0.97
0.95
Voltage (p.u.)
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0.8
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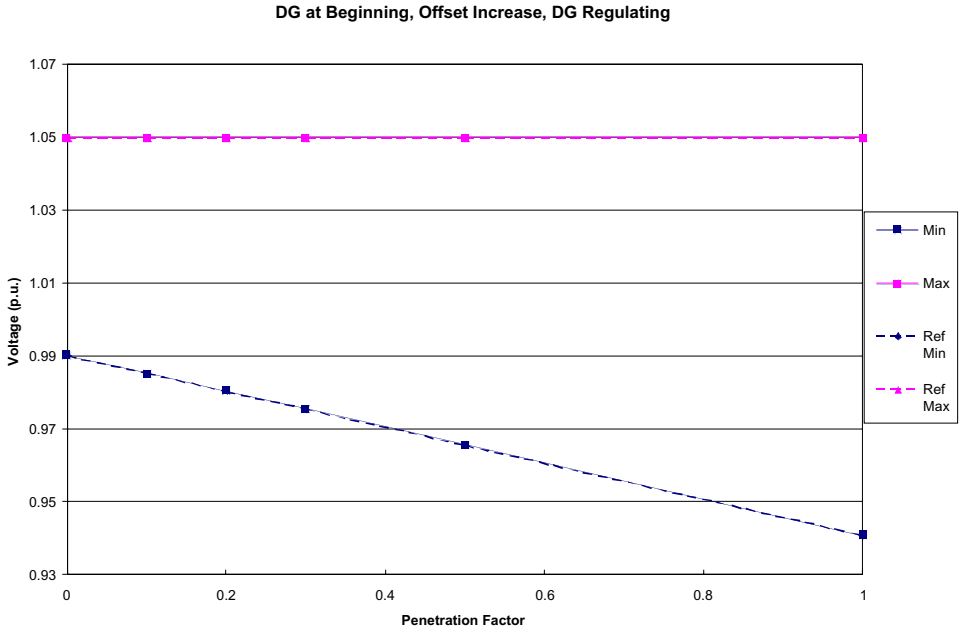
Penetration Factor
Min
Max
Ref Min
Ref Max

1.3.2.2.4


DG at Beginning, Offset Increase, DG Regulating
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0.93
Voltage (p.u.)
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Penetration Factor
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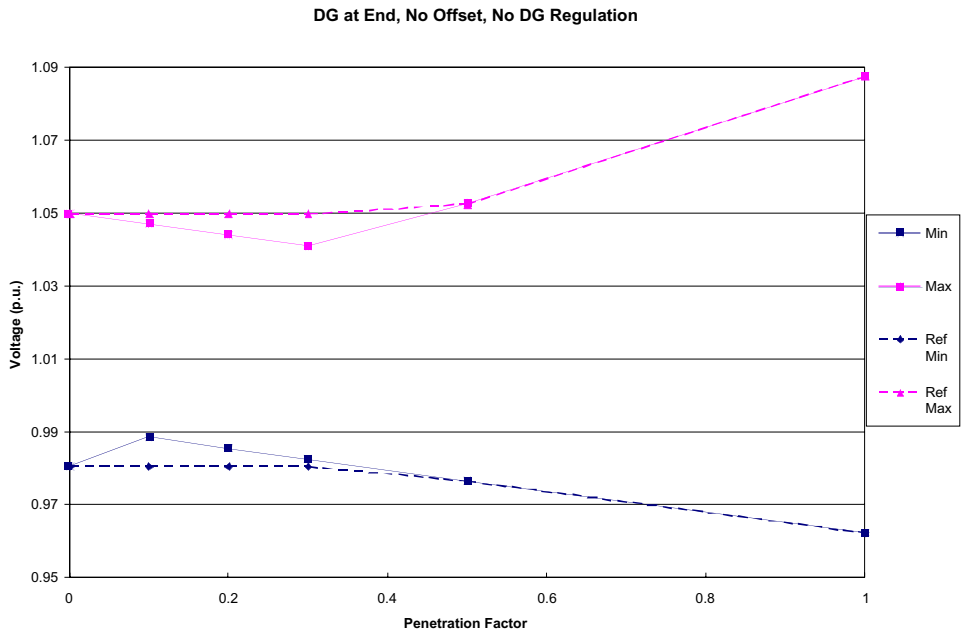
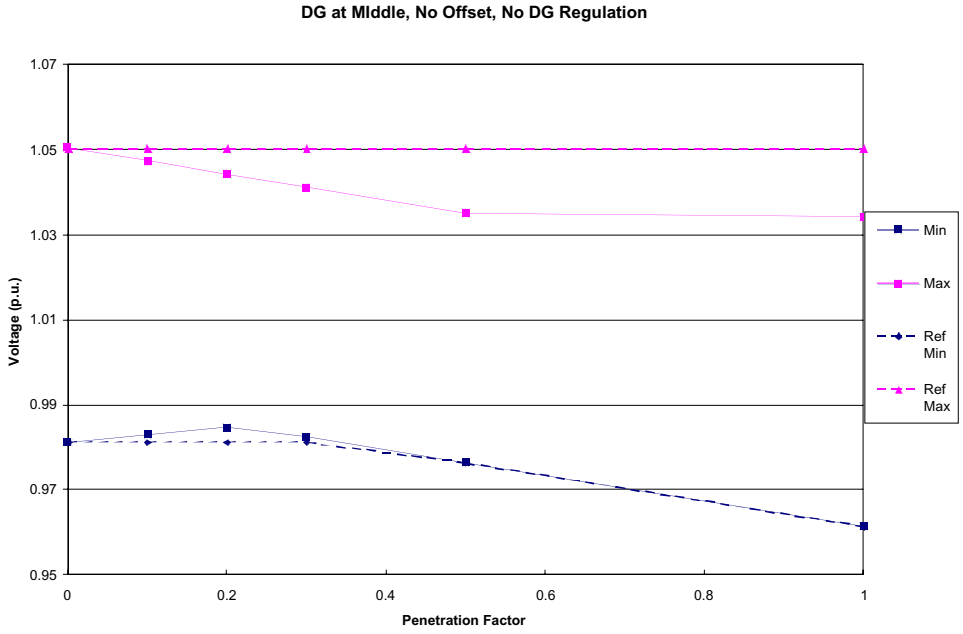
Max
Ref Min
Ref Max

BASE DESIGN 2.1

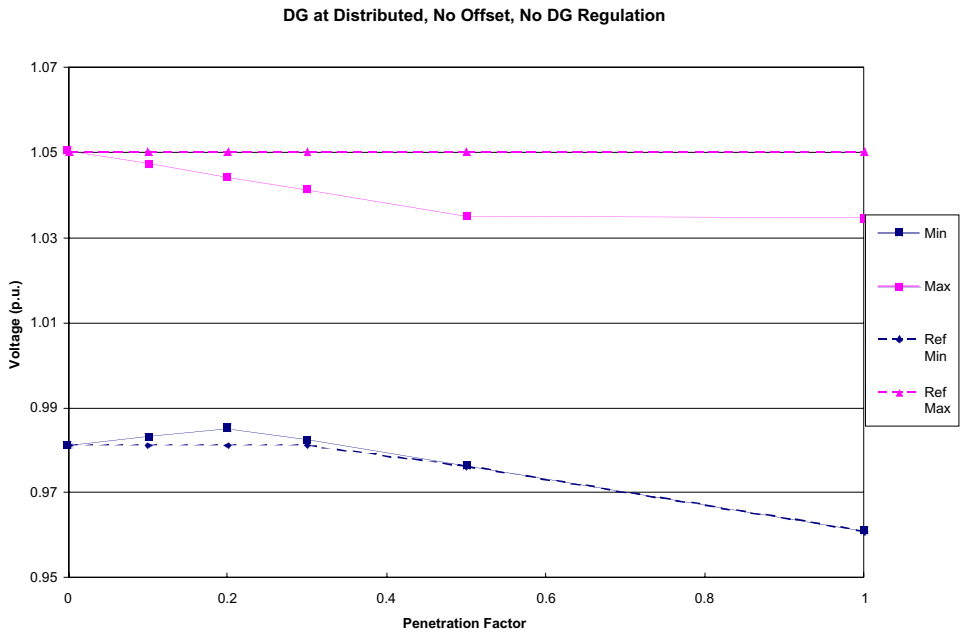
2.1.1.1.1



2.1.1.1.2



2.1.1.1.3


DG at Distributed, No Offset, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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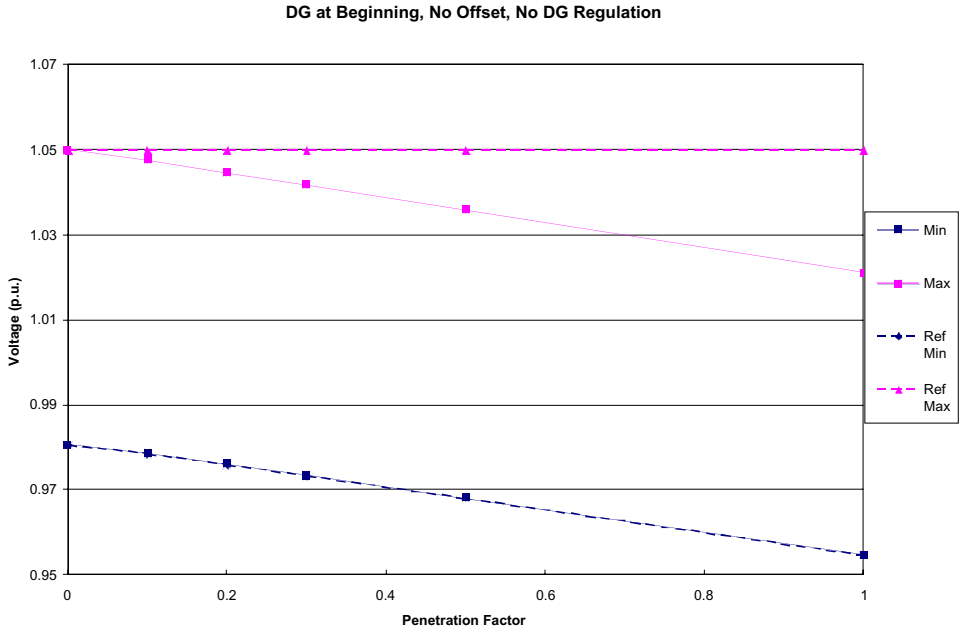
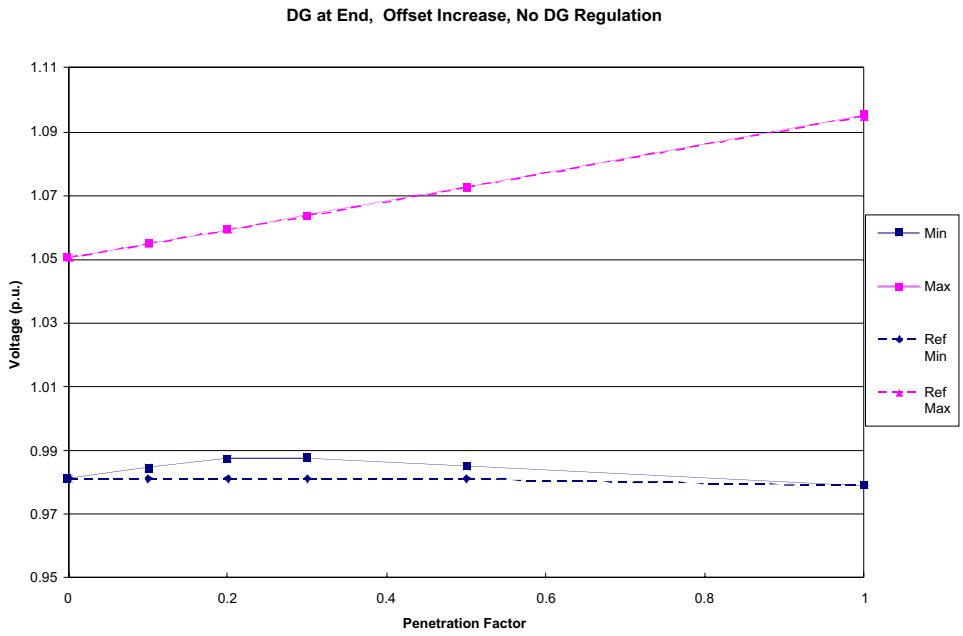
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.1.1.4


DG at Beginning, No Offset, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.1.2.1


DG at End, Offset Increase, No DG Regulation
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1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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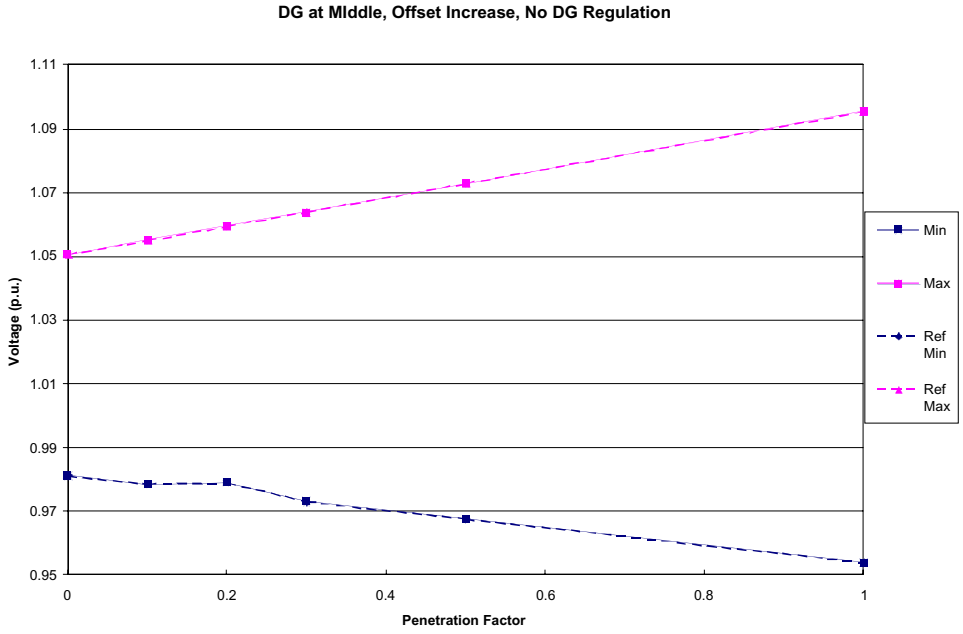
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.1.2.2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1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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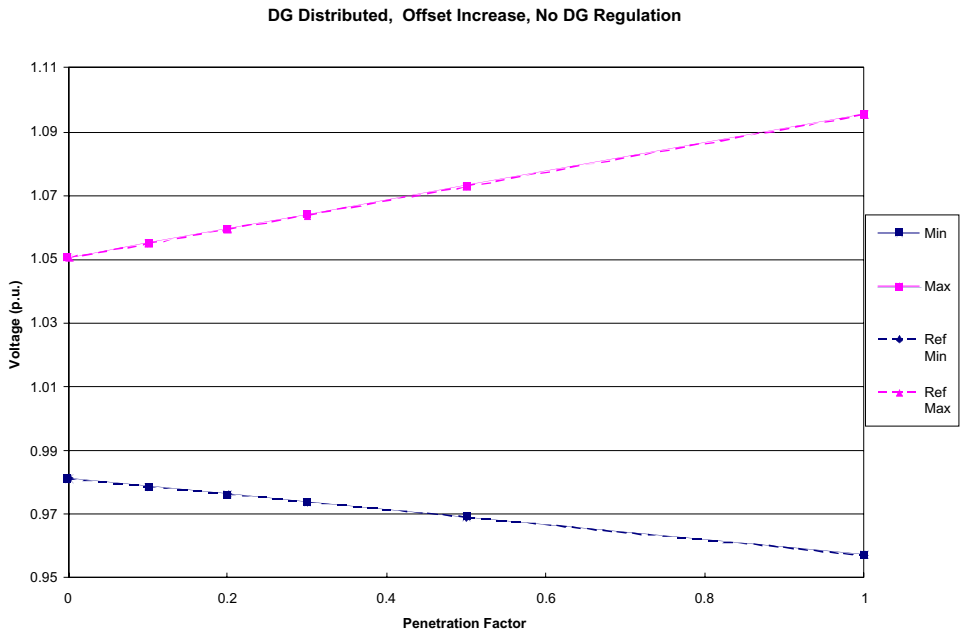
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.1.2.3


DG Distributed, Offset Increase, No DG Regulation
Voltage (p.u.)
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1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0
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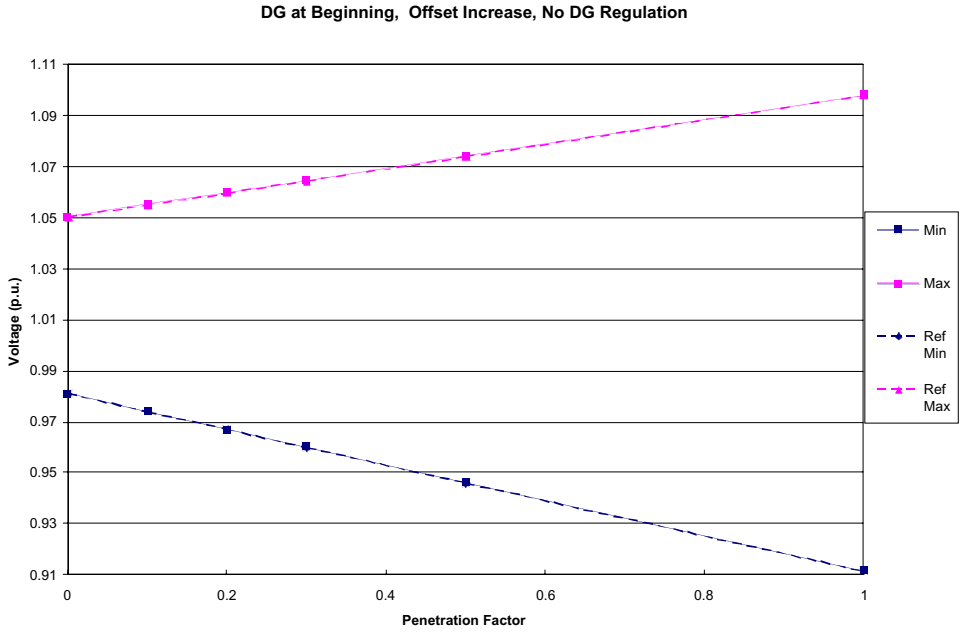
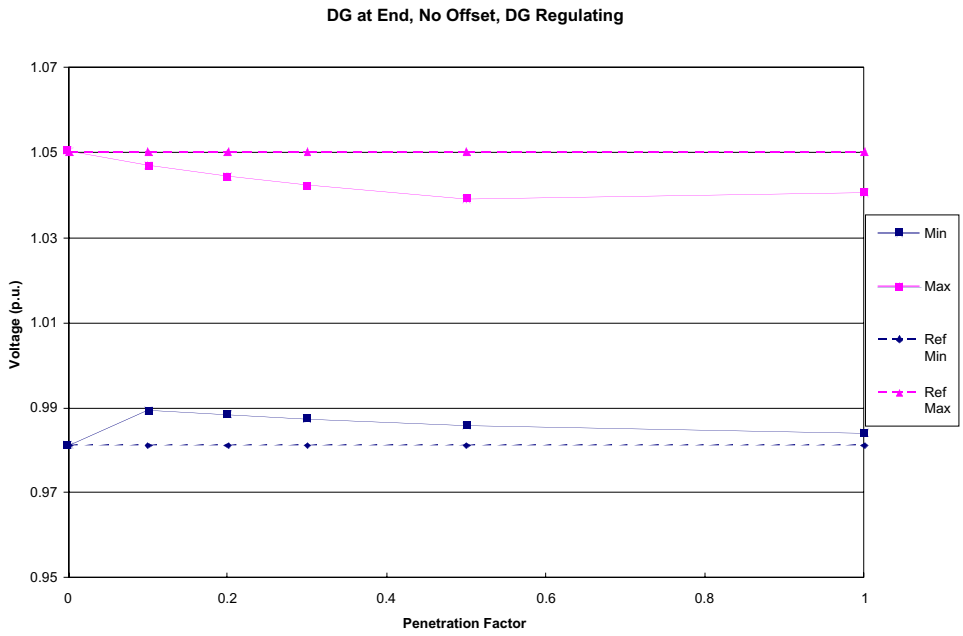
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.1.2.4


DG at Beginning, Offset Increase, No DG Regulation
Voltage (p.u.)
1.11
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
0.91
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.2.1.1


DG at End, No Offset, DG Regulating
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1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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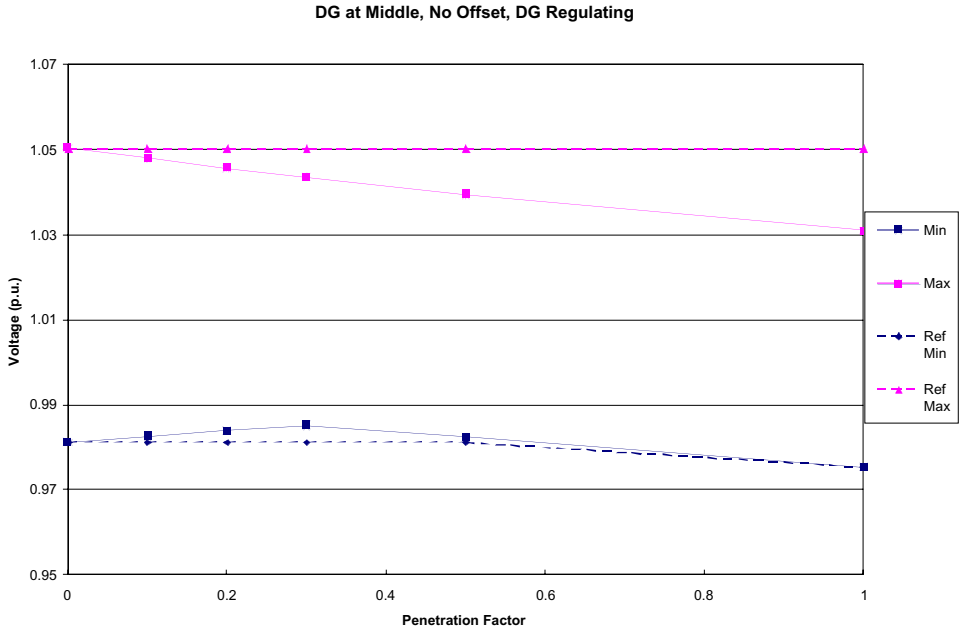
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.2.1.2


DG at Middle, No Offset, DG Regulating
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1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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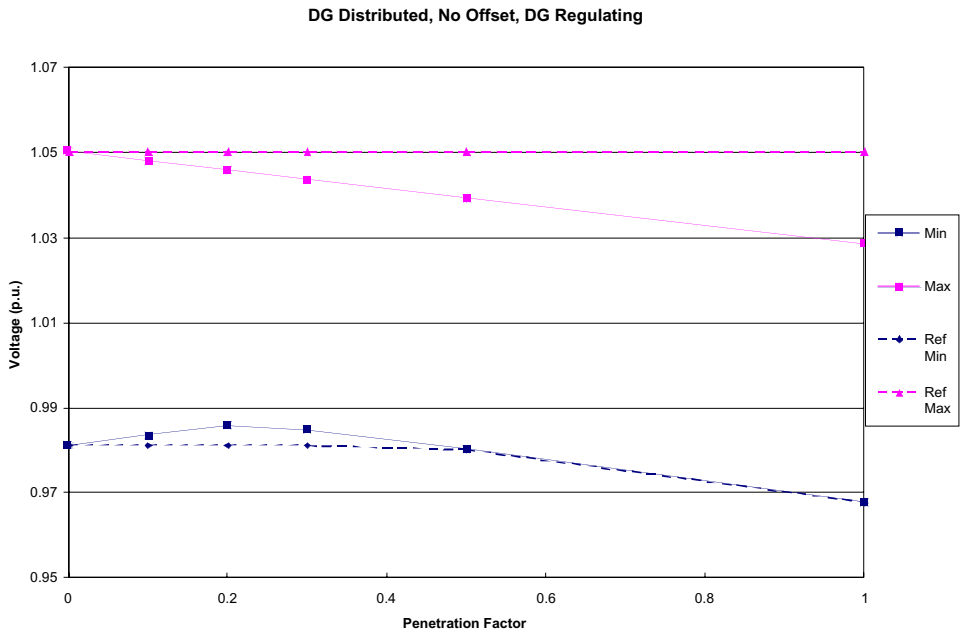
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.2.1.3


DG Distributed, No Offset, DG Regulating
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1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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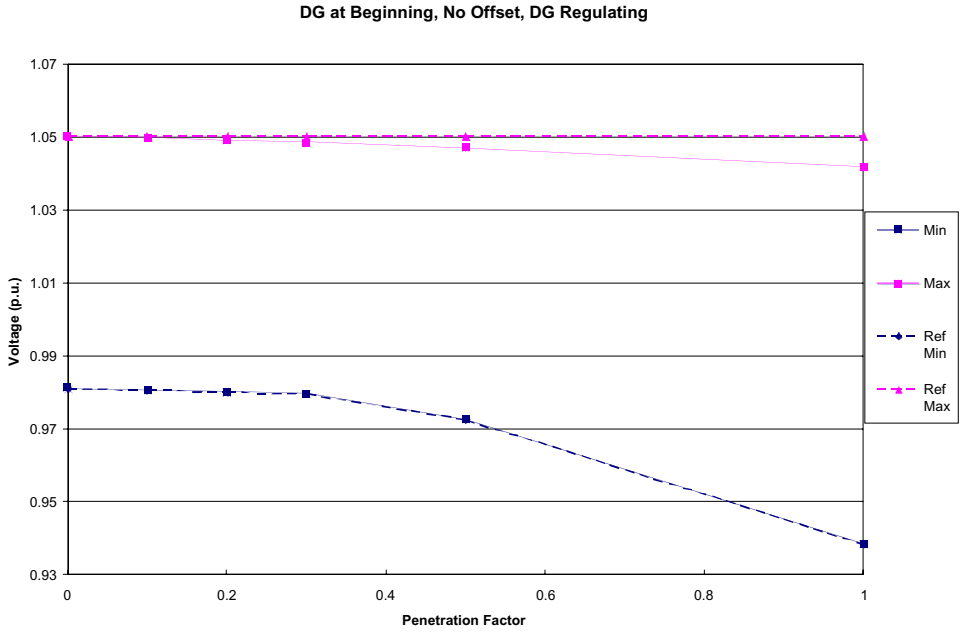
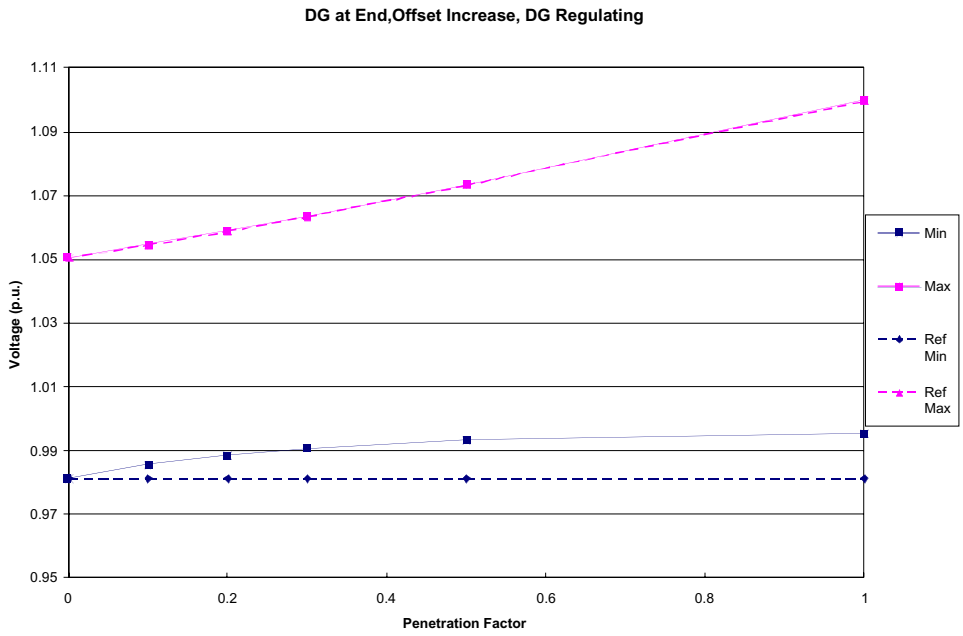
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

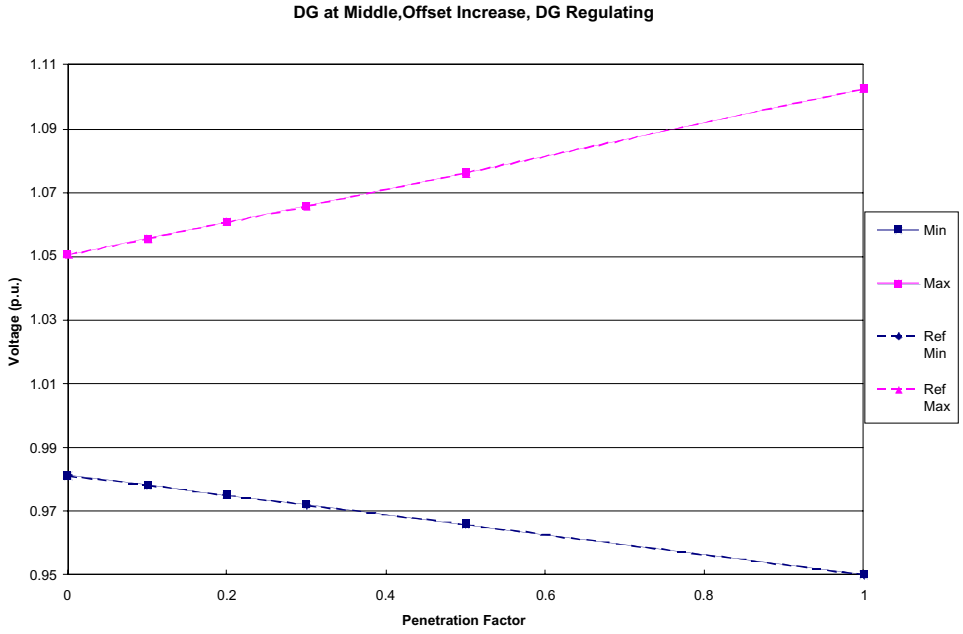
2.1.2.1.4


DG at Beginning, No Offset, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

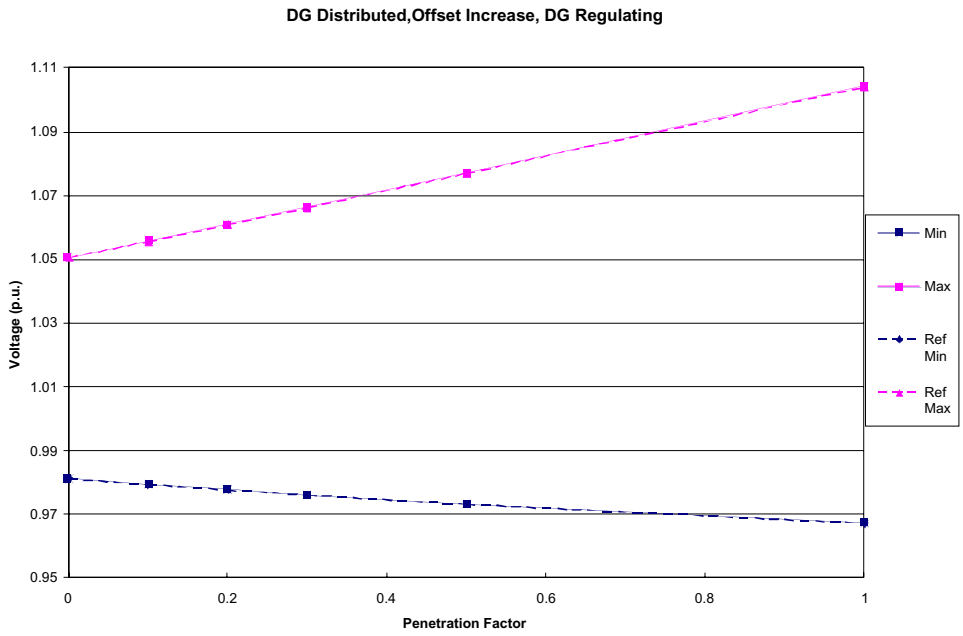
2.1.2.2.1


DG at End,Offset Increase, DG Regulating
Voltage (p.u.)
1.11
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.2.2.2


DG at Middle,Offset Increase, DG Regulating
Voltage (p.u.)
1.11
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.2.2.3


DG Distributed,Offset Increase, DG Regulating
1.11
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
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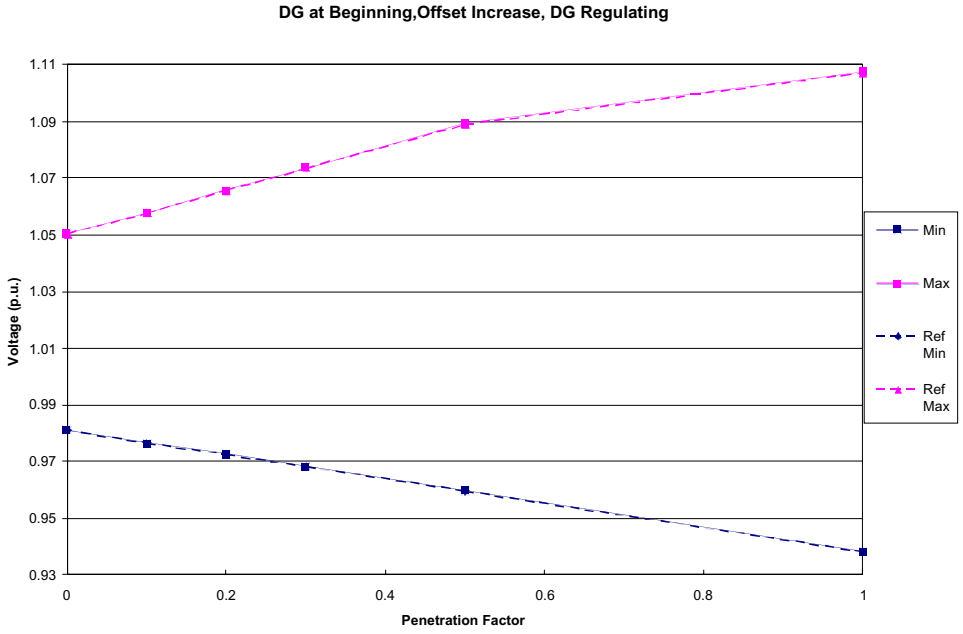
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.1.2.2.4


DG at Beginning,Offset Increase, DG Regulating
1.11
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
Voltage (p.u.)
0
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0.4
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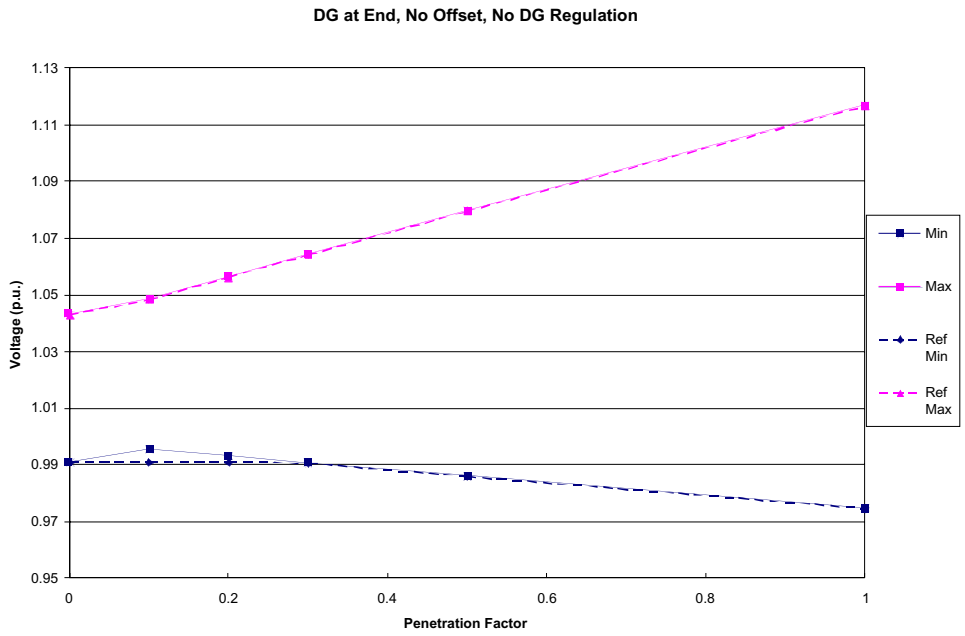
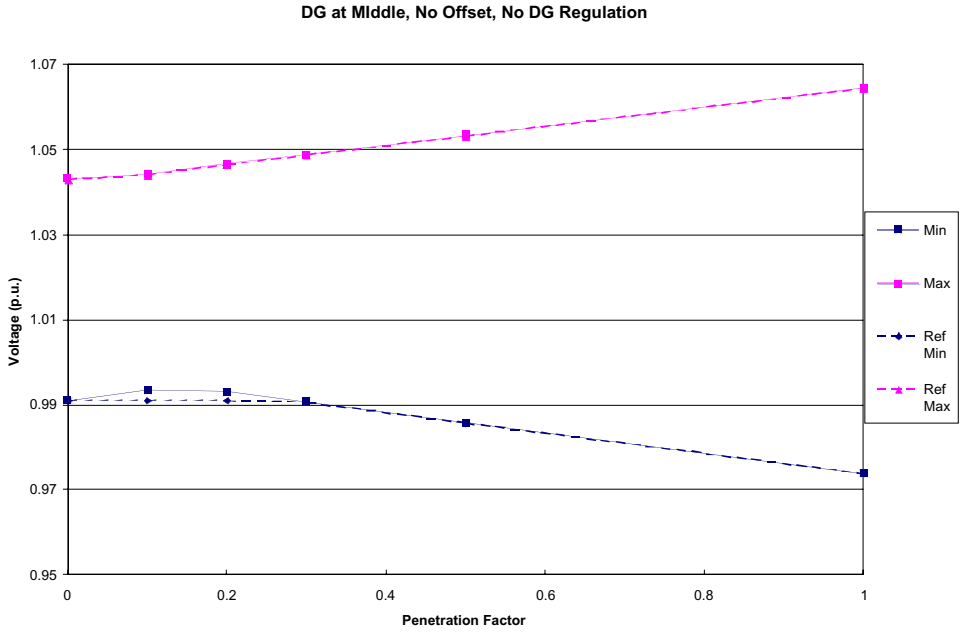
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

BASE DESIGN 2.2

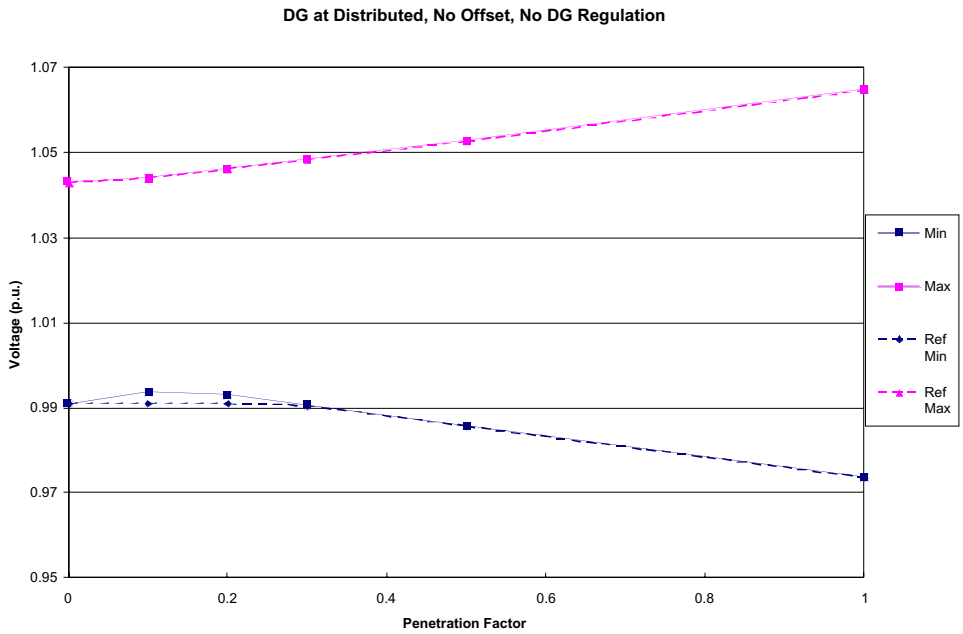
2.2.1.1.1



2.2.1.1.2



2.2.1.1.3


DG at Distributed, No Offset, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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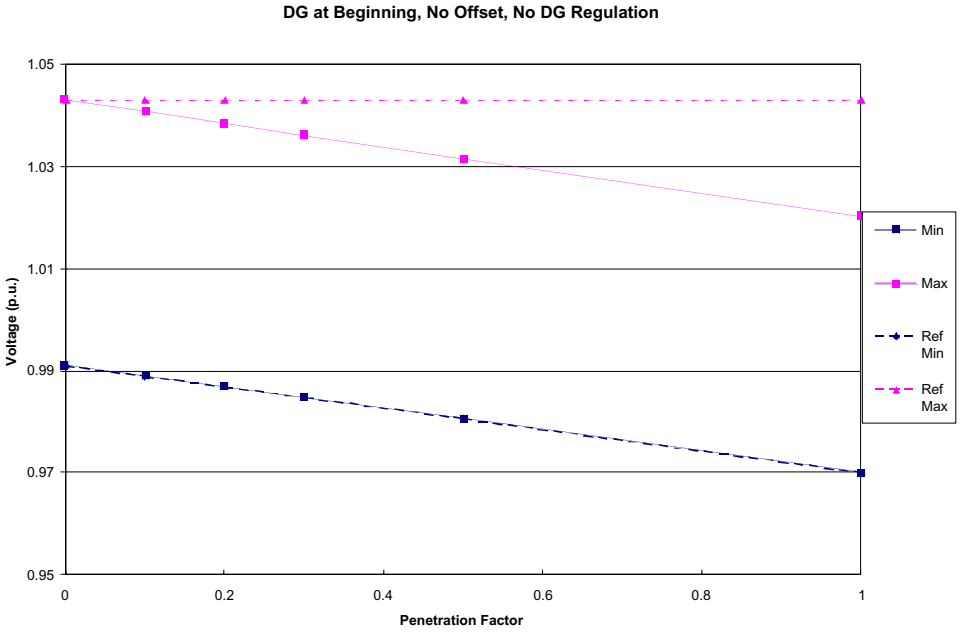
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.1.1.4


DG at Beginning, No Offset, No DG Regulation
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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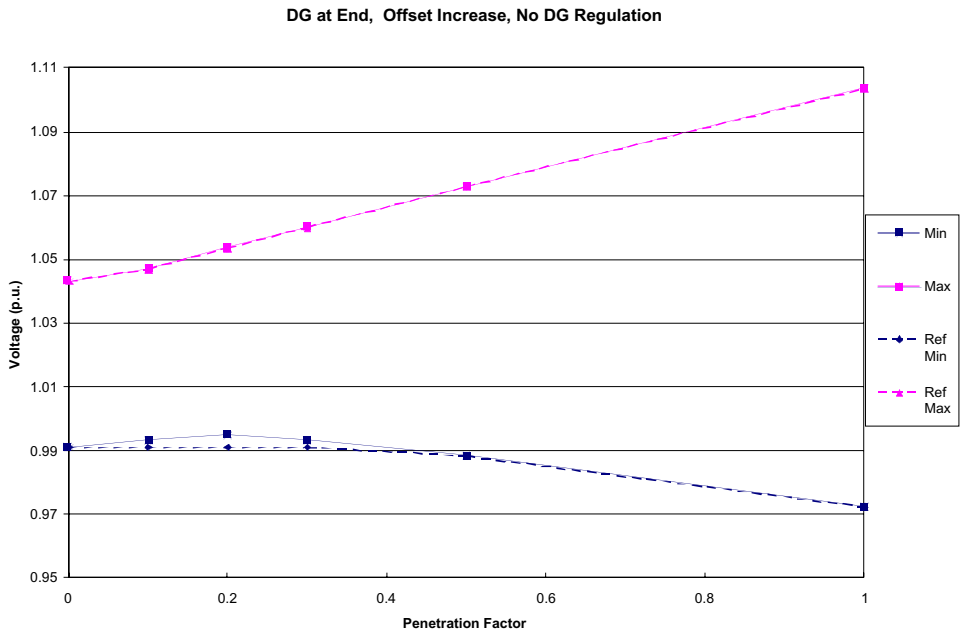
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.1.2.1


DG at End, Offset Increase, No DG Regulation
1.11
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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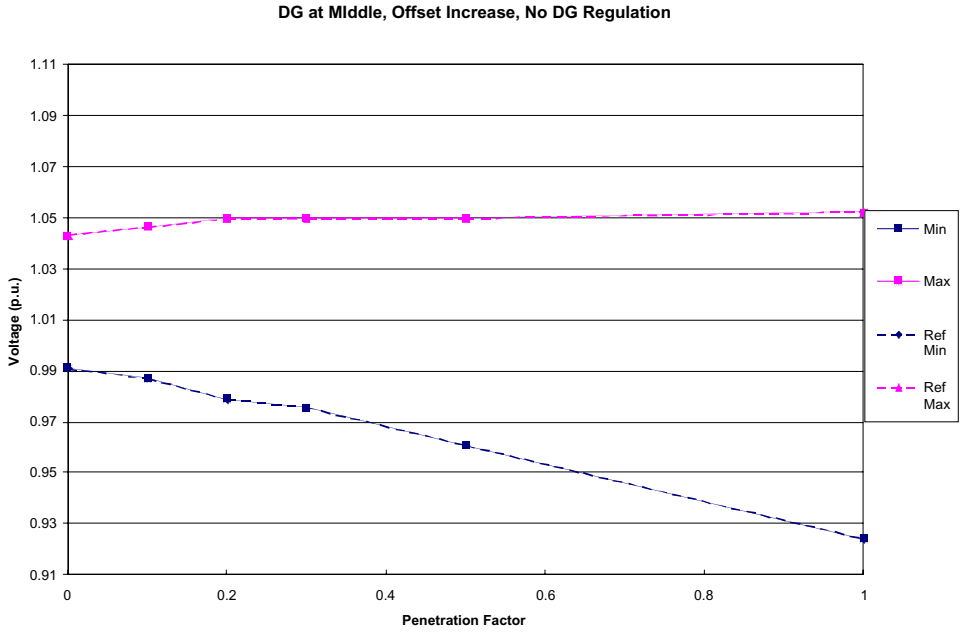
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.1.2.2


DG at MIddle, Offset Increase, No DG Regulation
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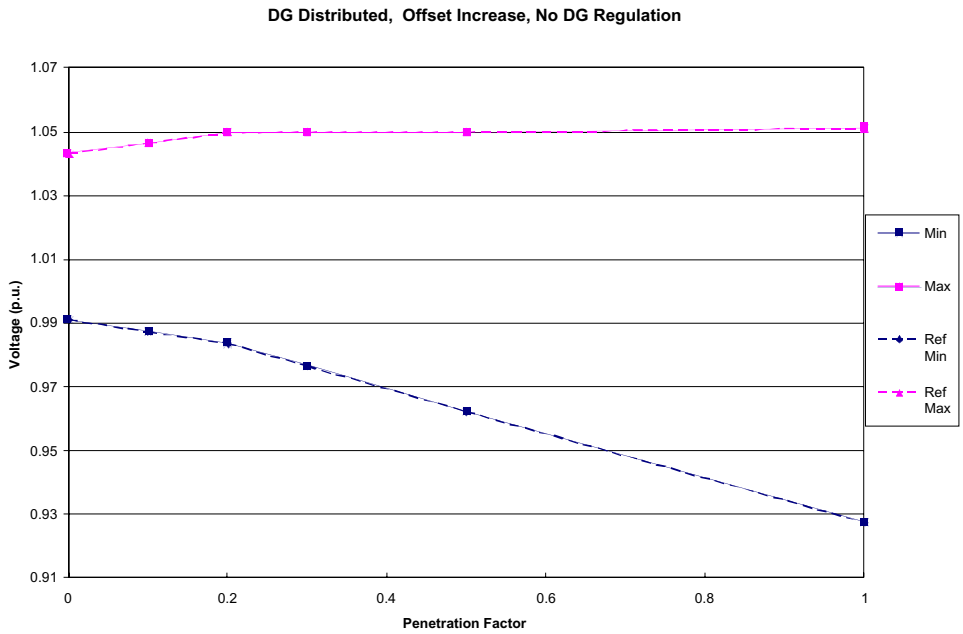
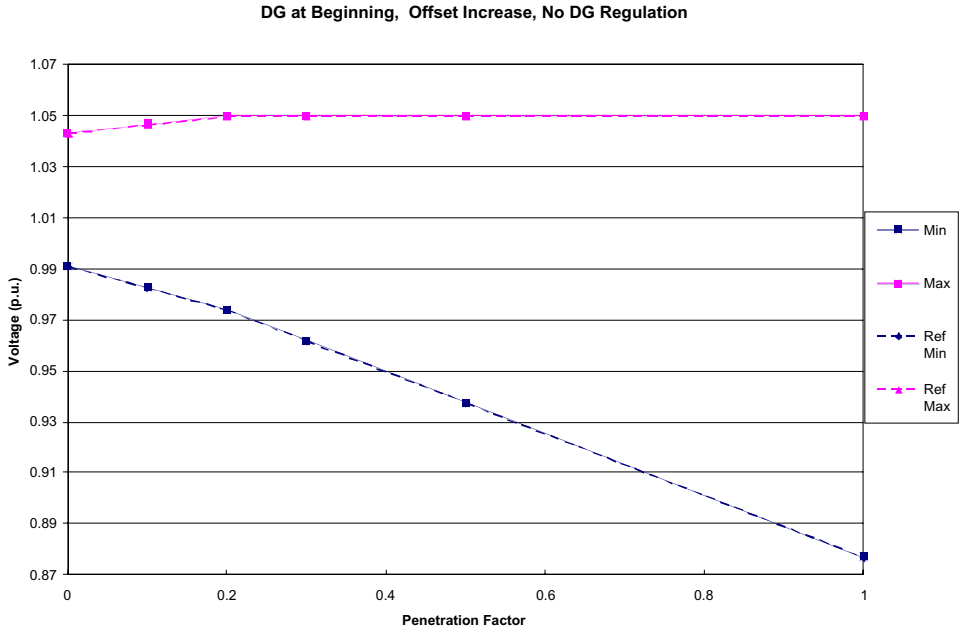
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
0.91
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.1.2.3


DG Distributed, Offset Increase, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
0.91
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.1.2.4


DG at Beginning, Offset Increase, No DG Regulation
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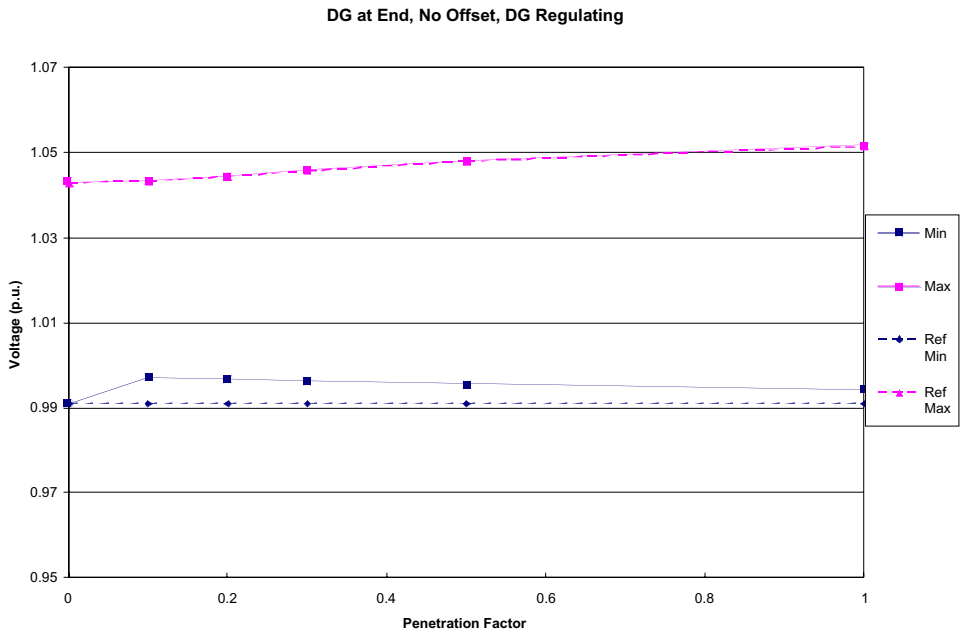
0.97
0.95
0.93
0.91
0.89
0.87
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.2.1.1


DG at End, No Offset, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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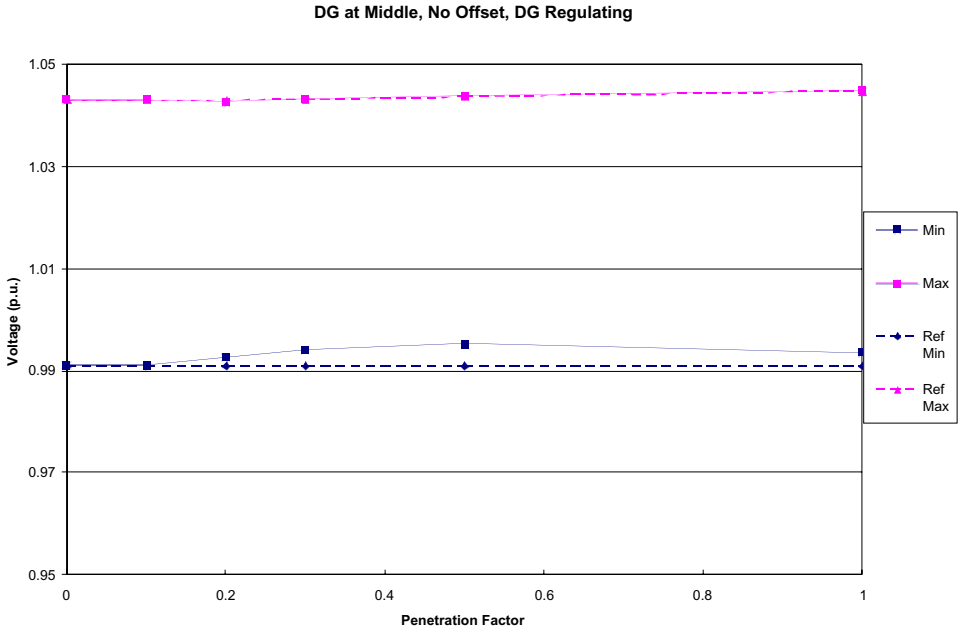
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.2.1.2


DG at Middle, No Offset, DG Regulating
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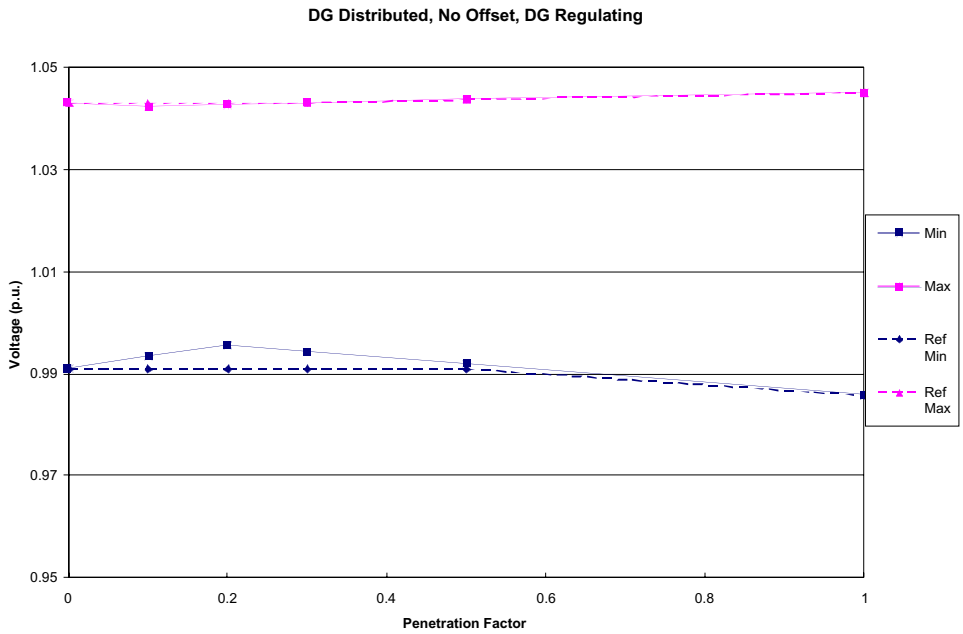
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.2.1.3


DG Distributed, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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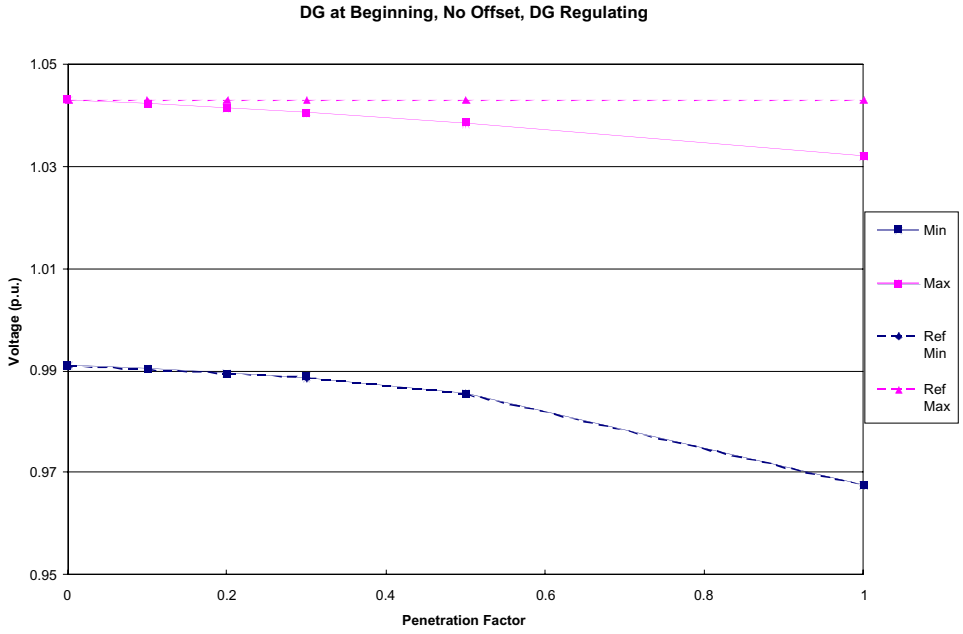
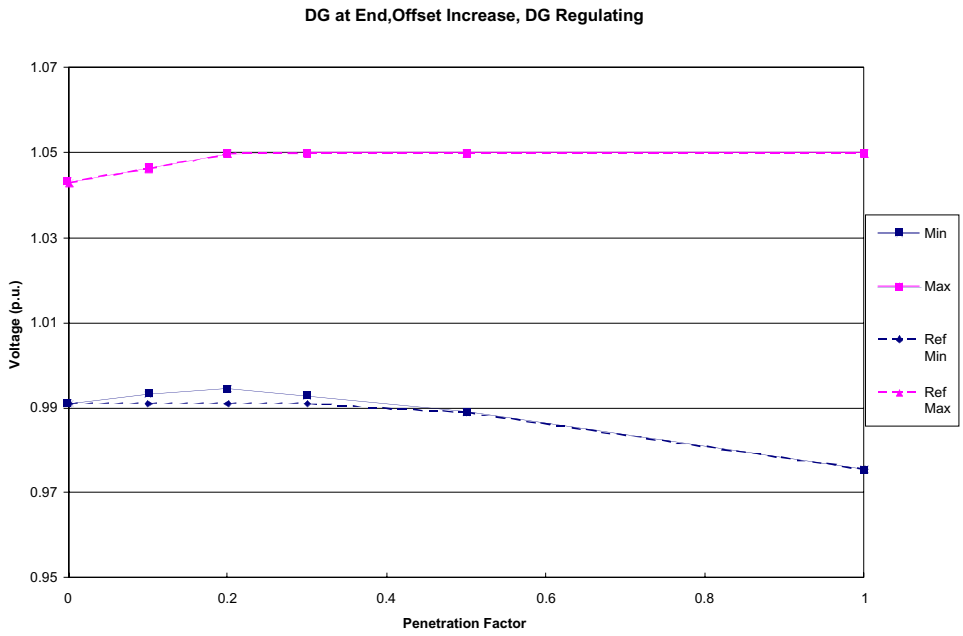
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.2.1.4


DG at Beginning, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.2.2.1


DG at End,Offset Increase, DG Regulating
1.07
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1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
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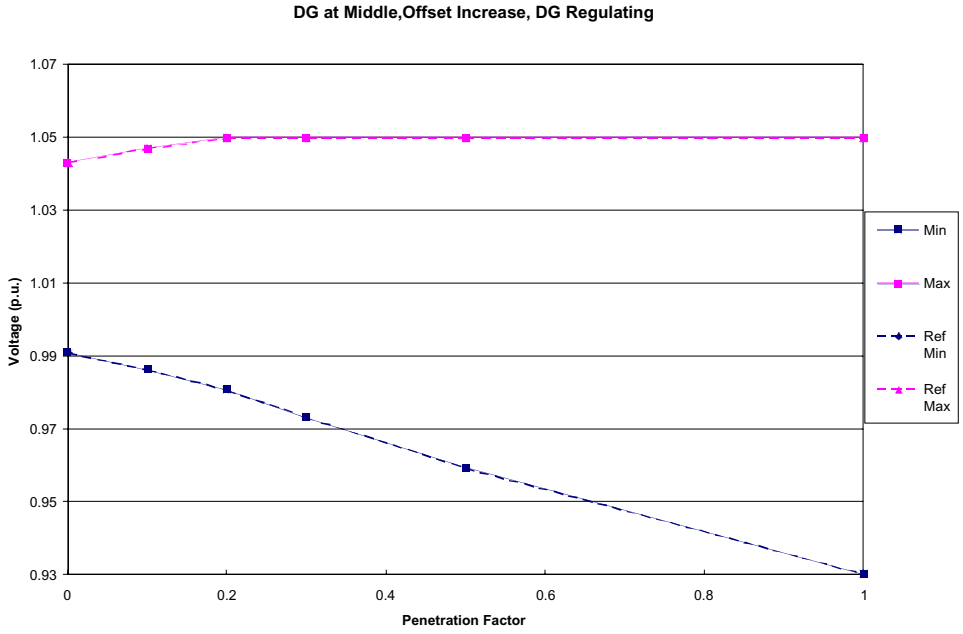
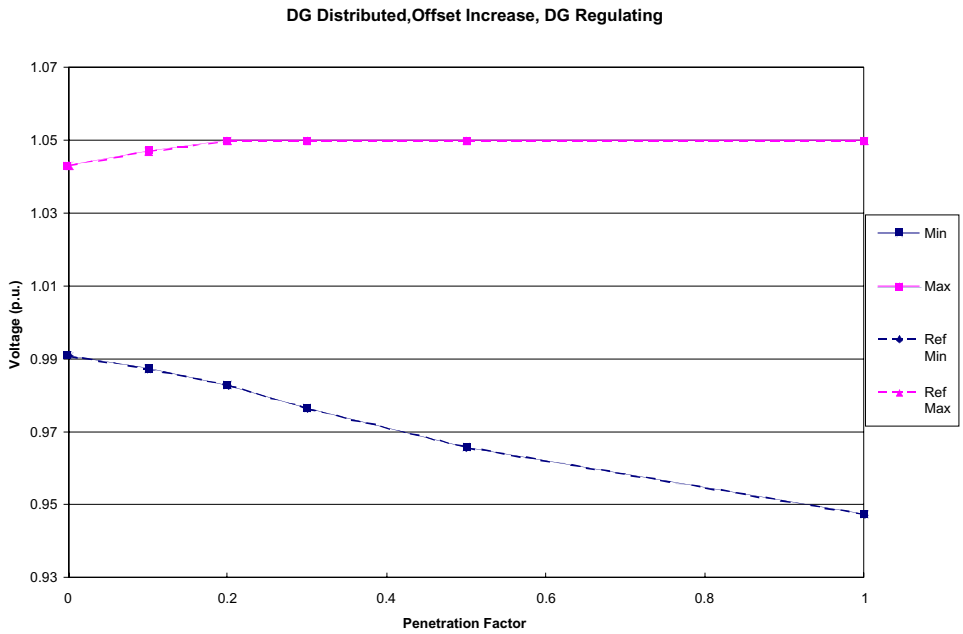
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.2.2.2


DG at Middle,Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.2.2.3


DG Distributed,Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
Voltage (p.u.)
0
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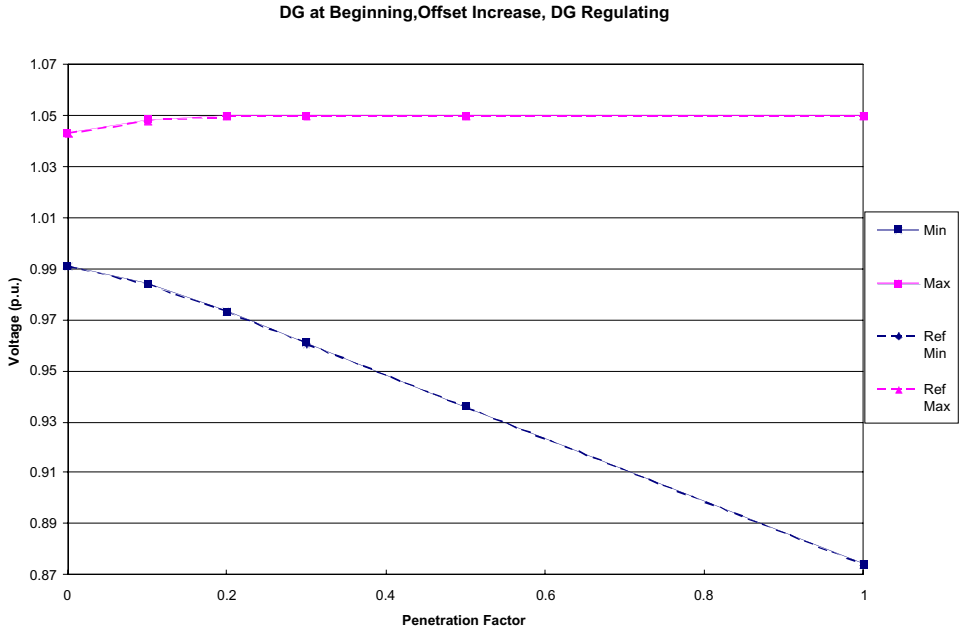
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

2.2.2.2.4


DG at Beginning,Offset Increase, DG Regulating
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1.05
1.03
1.01
0.99
0.97
0.95
0.93
0.91
0.89
0.87
Voltage (p.u.)
0
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0.8
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Penetration Factor
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Max
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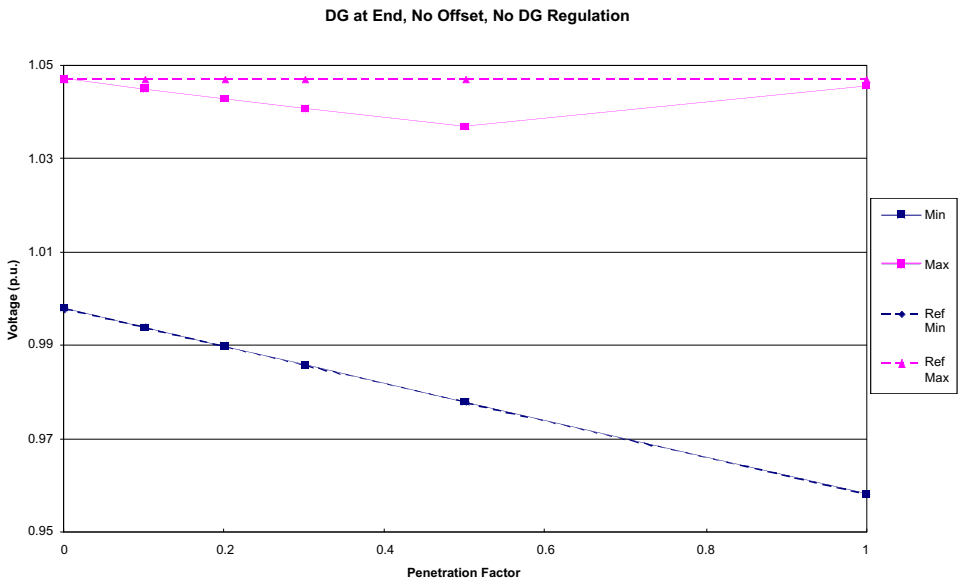
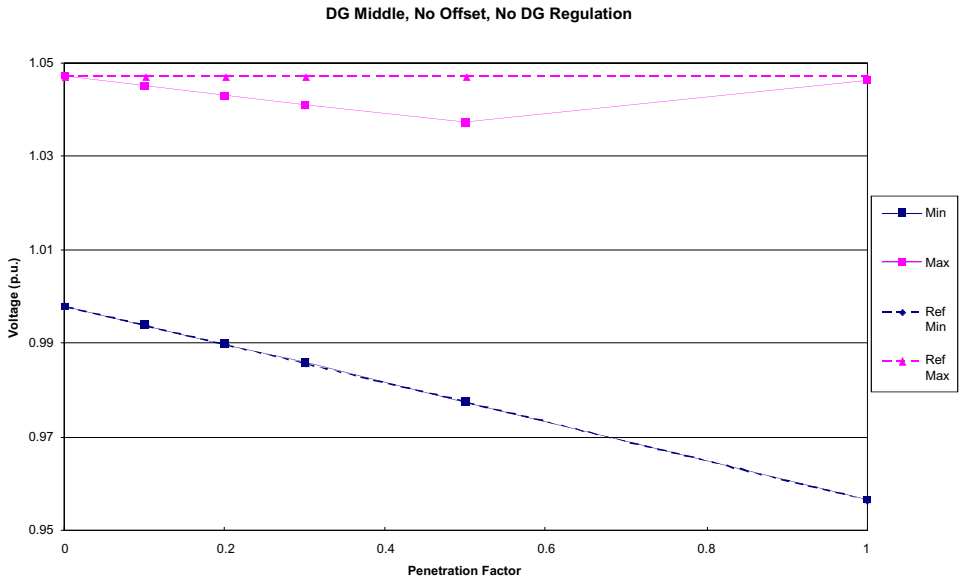
Ref Max

BASE DESIGN 3.1

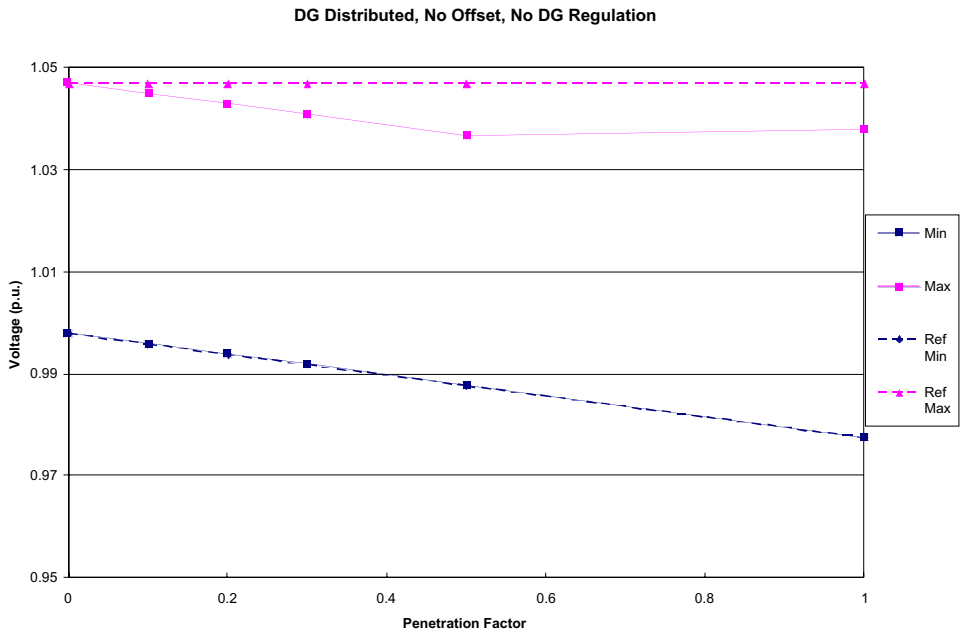
3.1.1.1.1



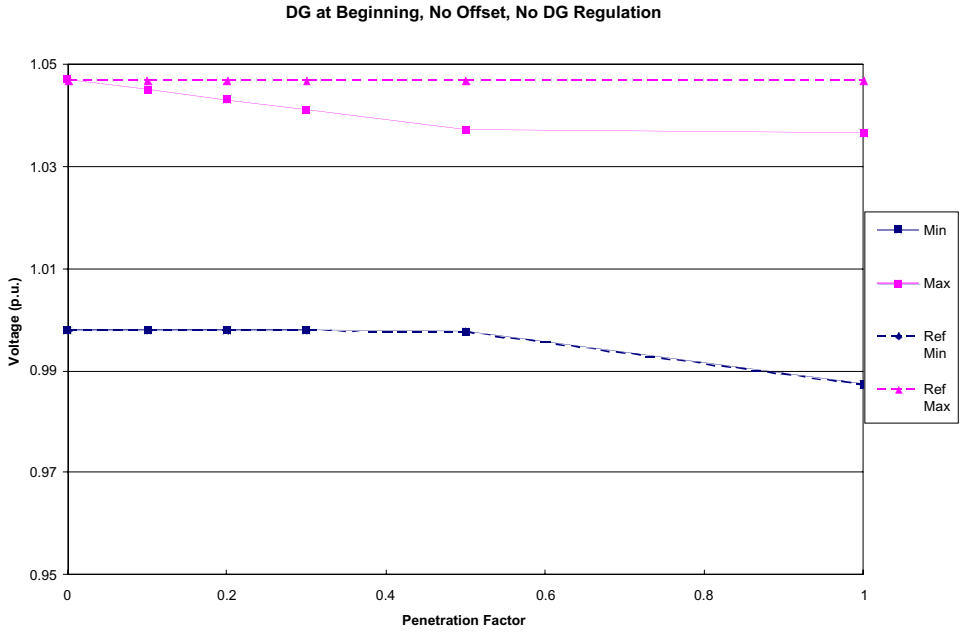
3.1.1.1.2



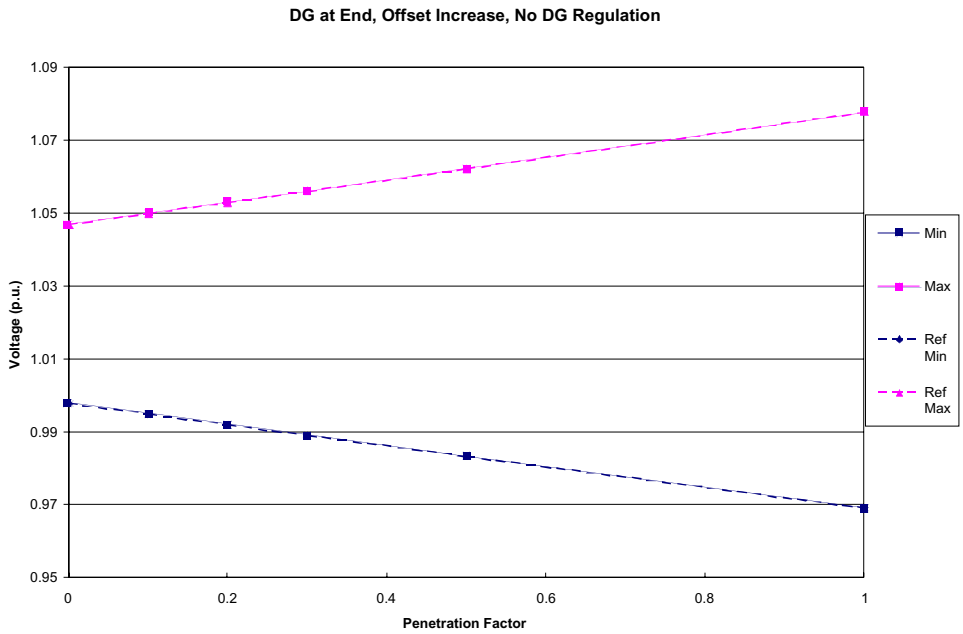
3.1.1.1.3


DG Distributed, No Offset, No DG Regulation
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

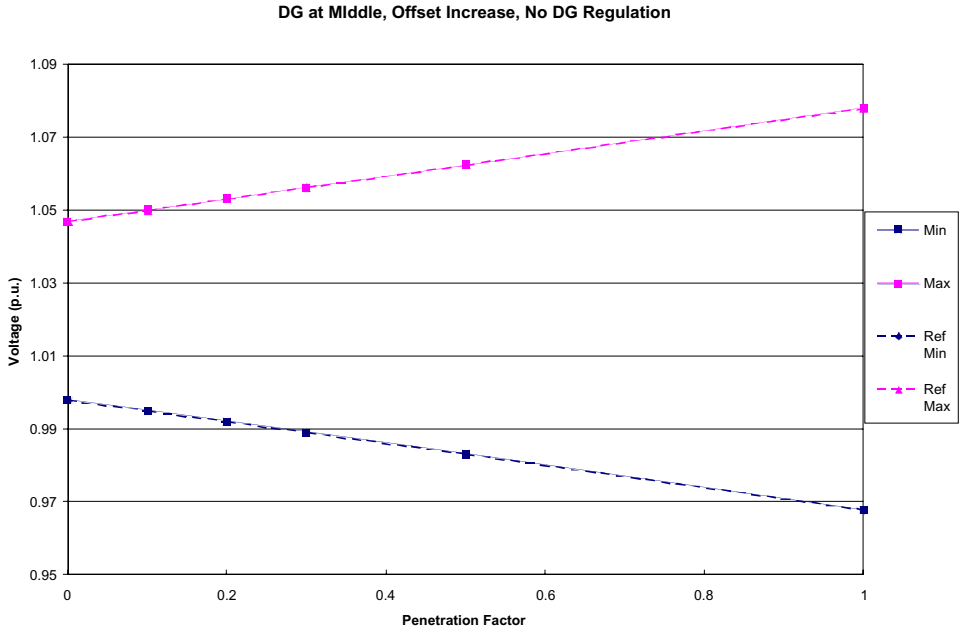
3.1.1.1.4


DG at Beginning, No Offset, No DG Regulation
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

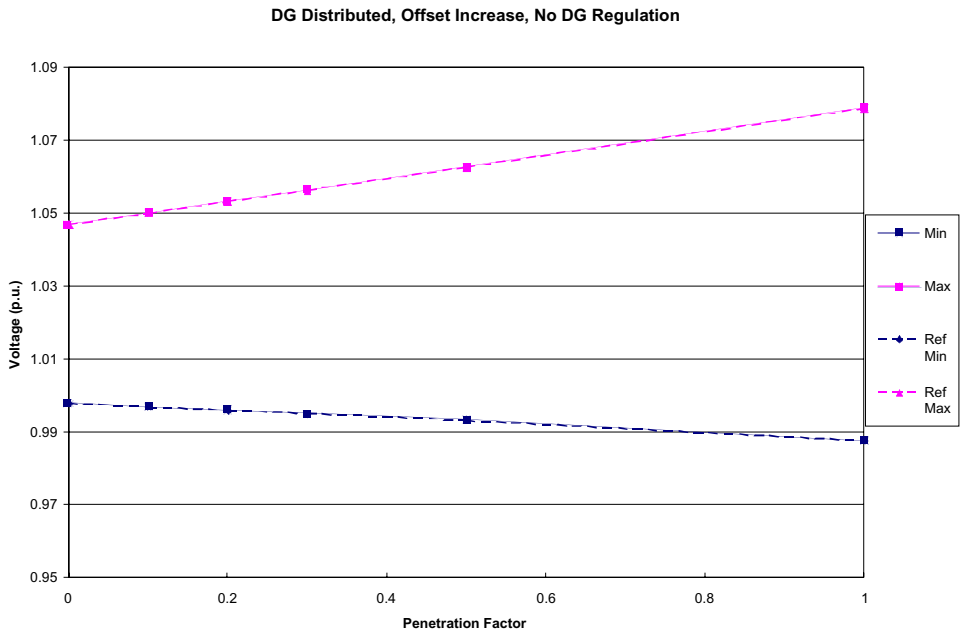
3.1.1.2.1


DG at End, Offset Increase, No DG Regulation
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

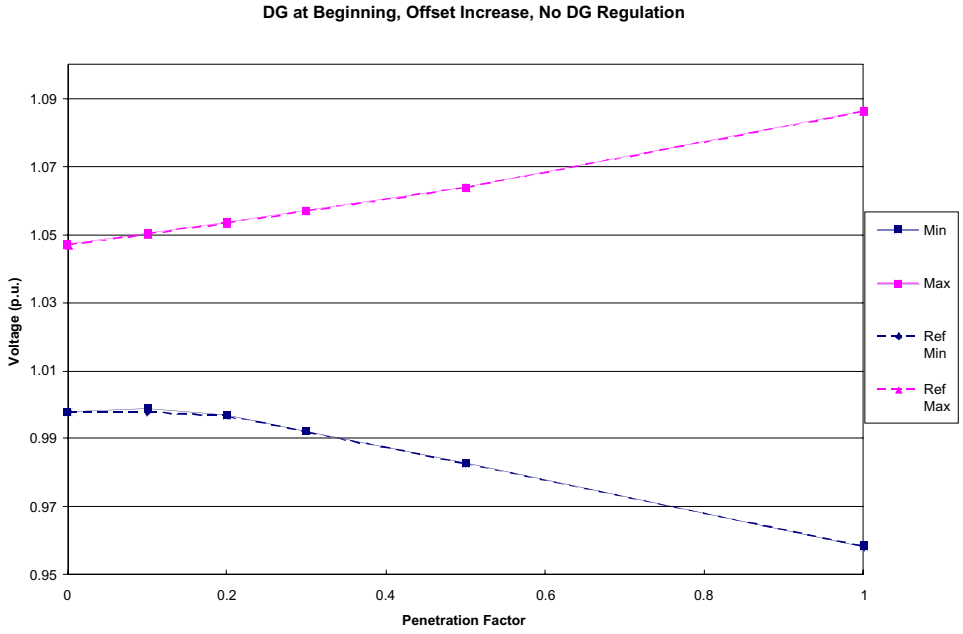
3.1.1.2.2


DG at MIddle, Offset Increase, No DG Regulation
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

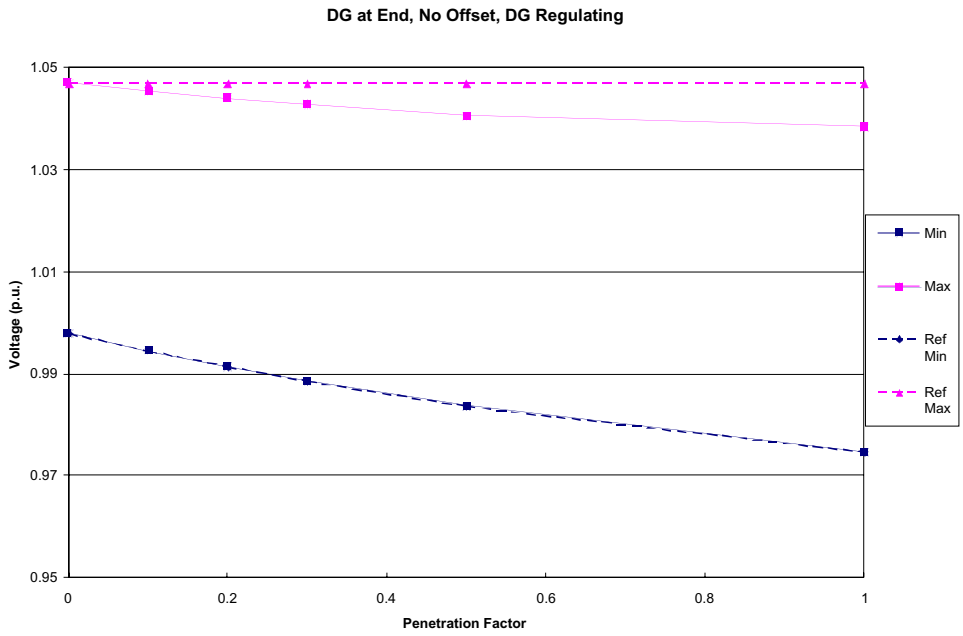
3.1.1.2.3


DG Distributed, Offset Increase, No DG Regulation
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

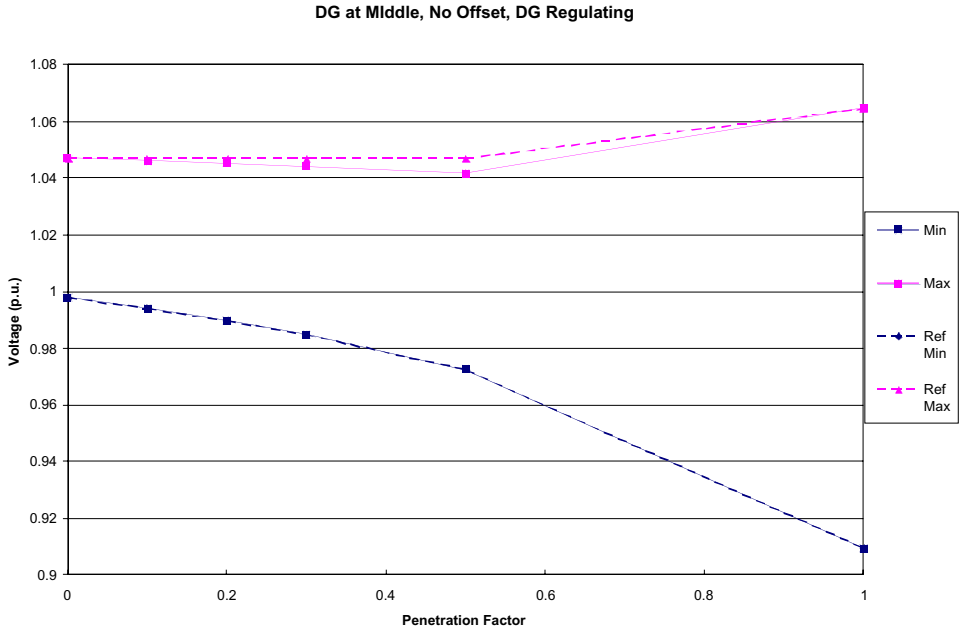
3.1.1.2.4


DG at Beginning, Offset Increase, No DG Regulation
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

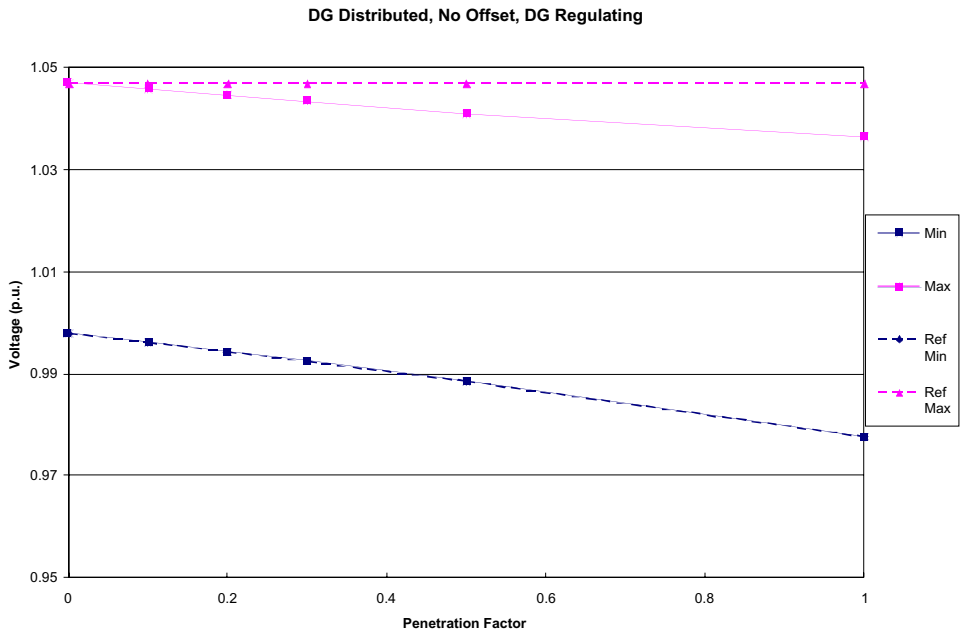
3.1.2.1.1


DG at End, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

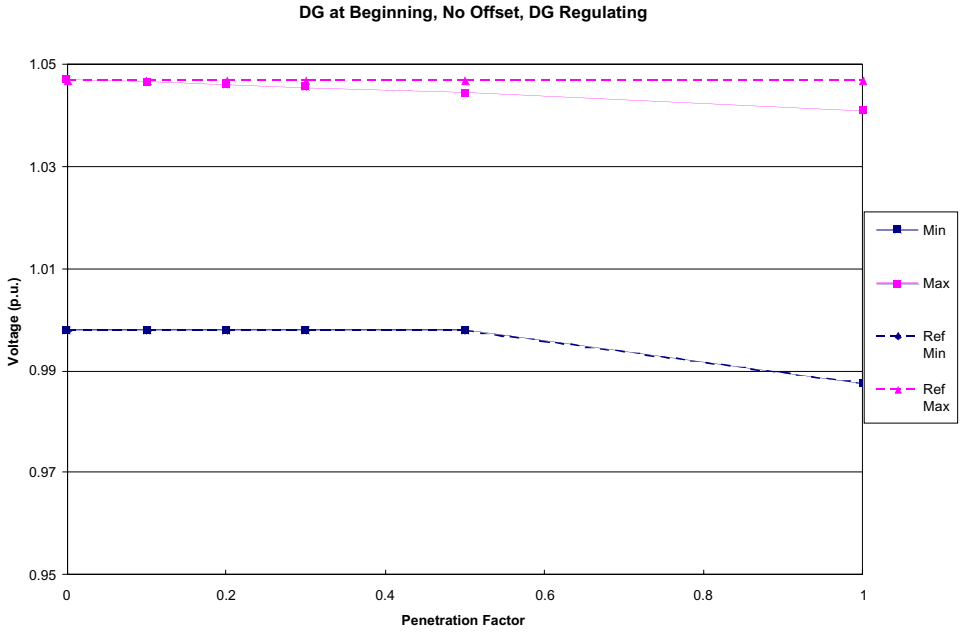
3.1.2.1.2


DG at MIddle, No Offset, DG Regulating
1.08
1.06
1.04
1.02
1
0.98
0.96
0.94
0.92
0.9
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

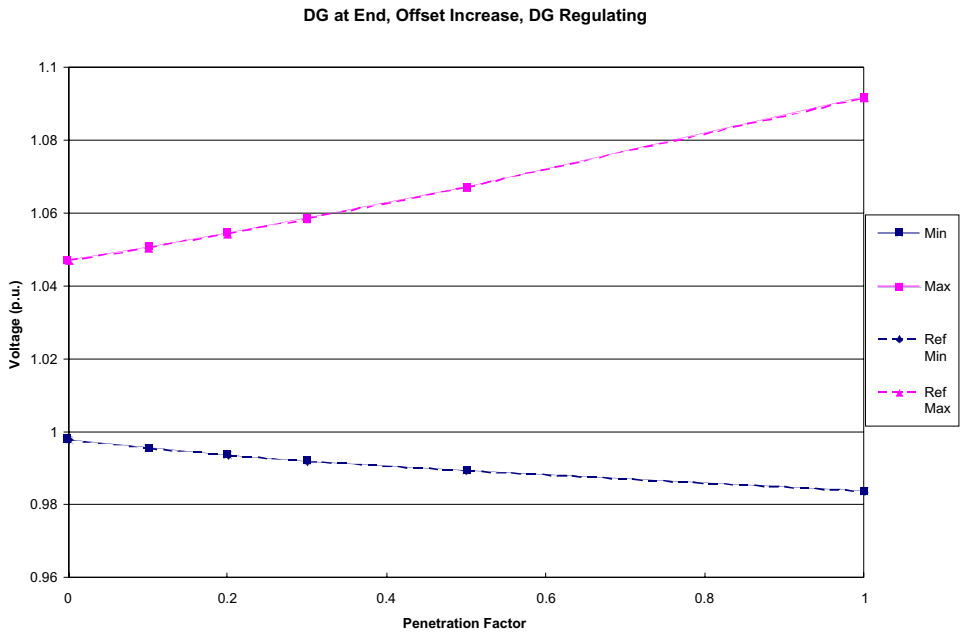
3.1.2.1.3


DG Distributed, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

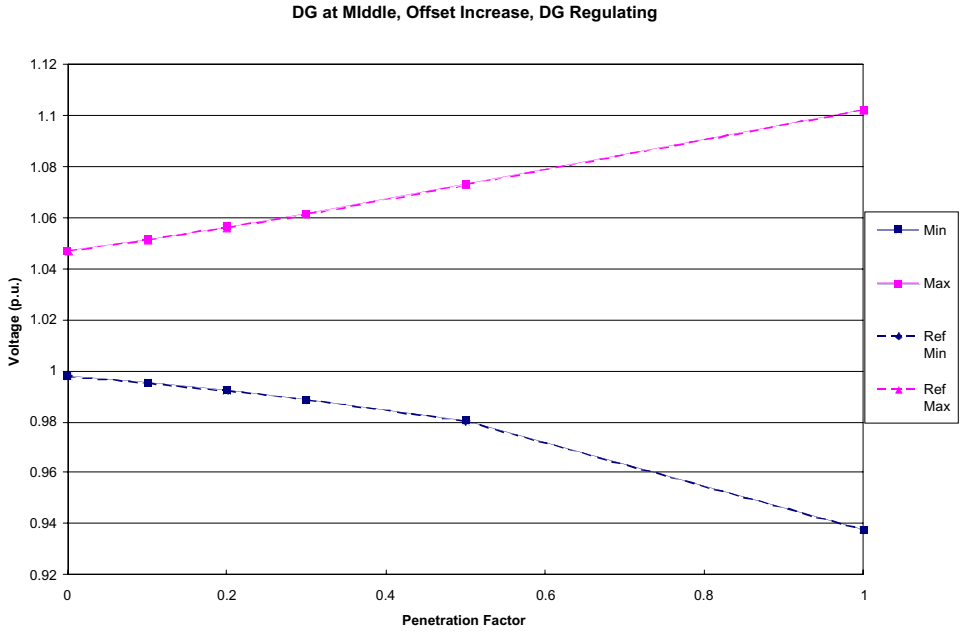
3.1.2.1.4


DG at Beginning, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

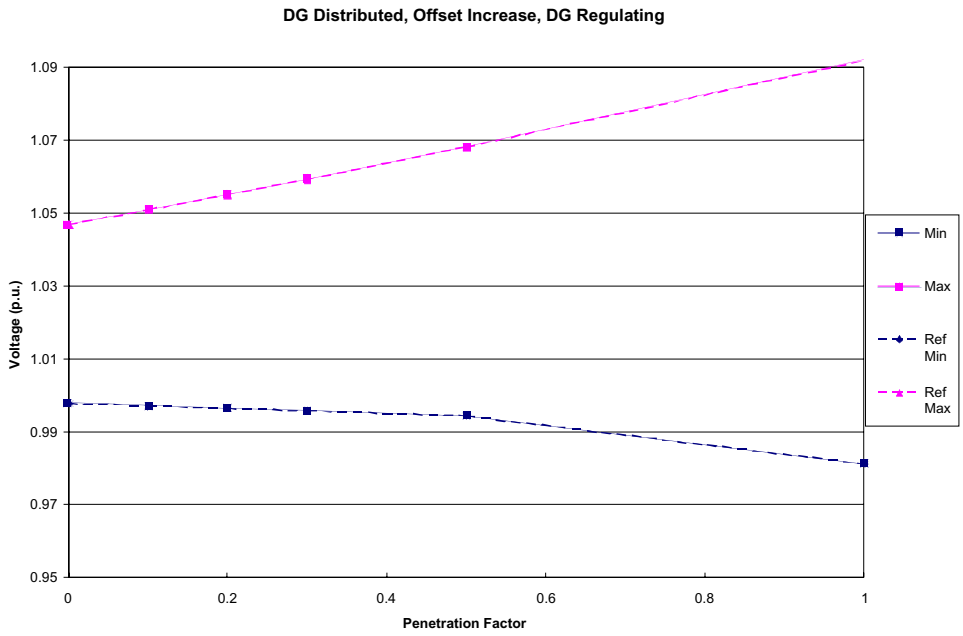
3.1.2.2.1


DG at End, Offset Increase, DG Regulating
Voltage (p.u.)
1.1
1.08
1.06
1.04
1.02
1
0.98
0.96
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

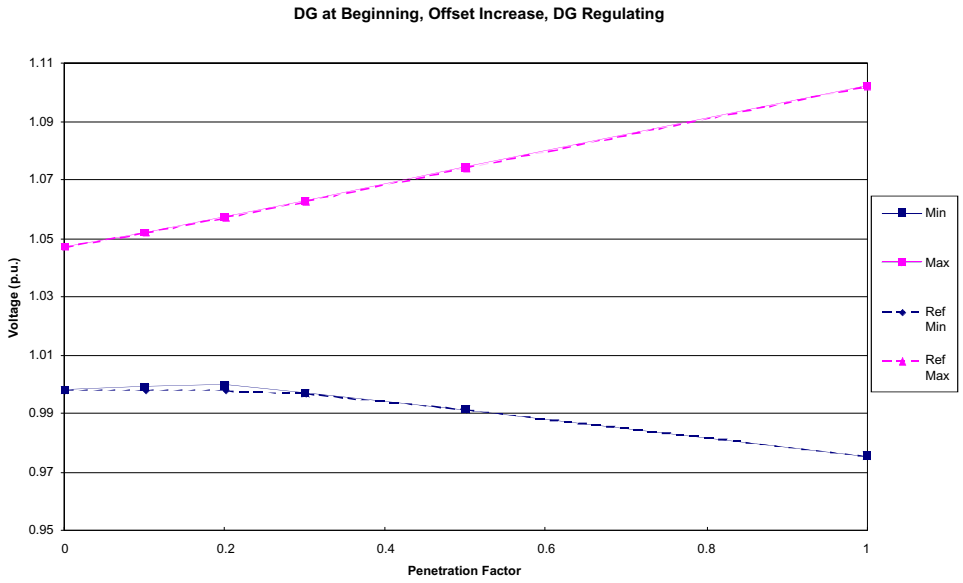
3.1.2.2.2


DG at MIddle, Offset Increase, DG Regulating
Voltage (p.u.)
1.12
1.1
1.08
1.06
1.04
1.02
1
0.98
0.96
0.94
0.92
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

3.1.2.2.3

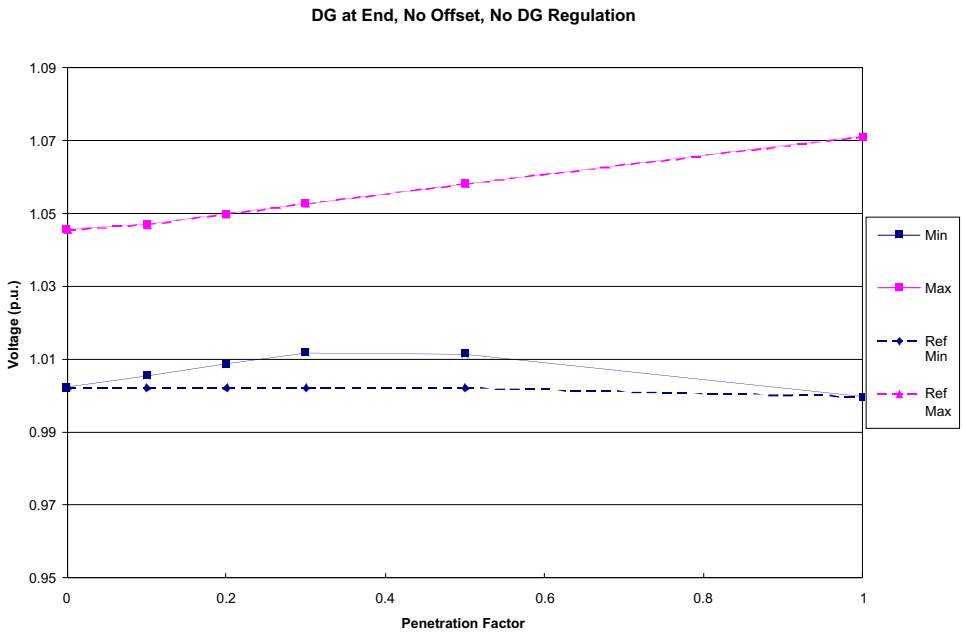

DG Distributed, Offset Increase, DG Regulating
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

3.1.2.2.4

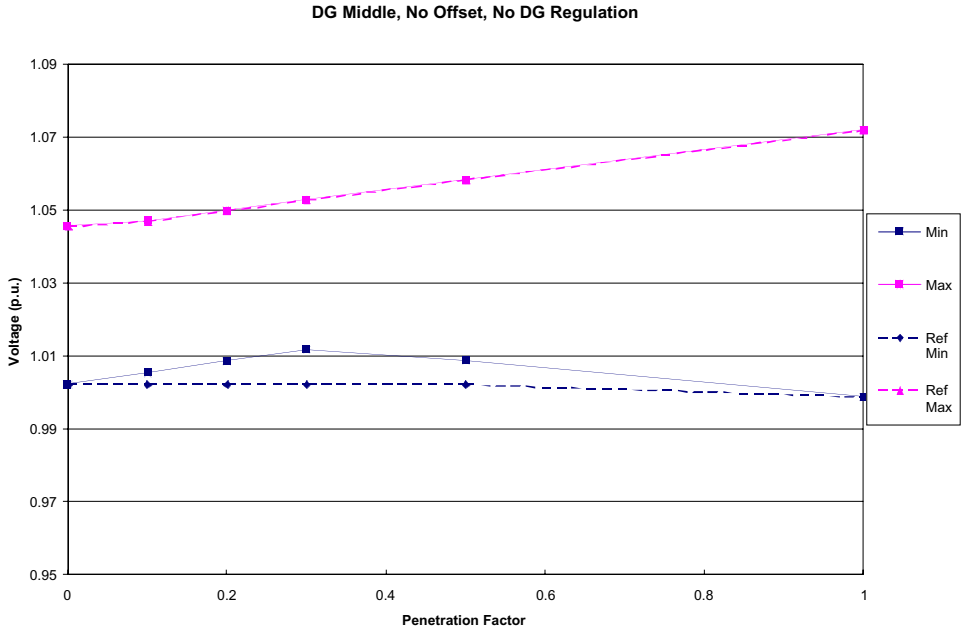

DG at Beginning, Offset Increase, DG Regulating
1.11
1.09
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

BASE DESIGN 3.2

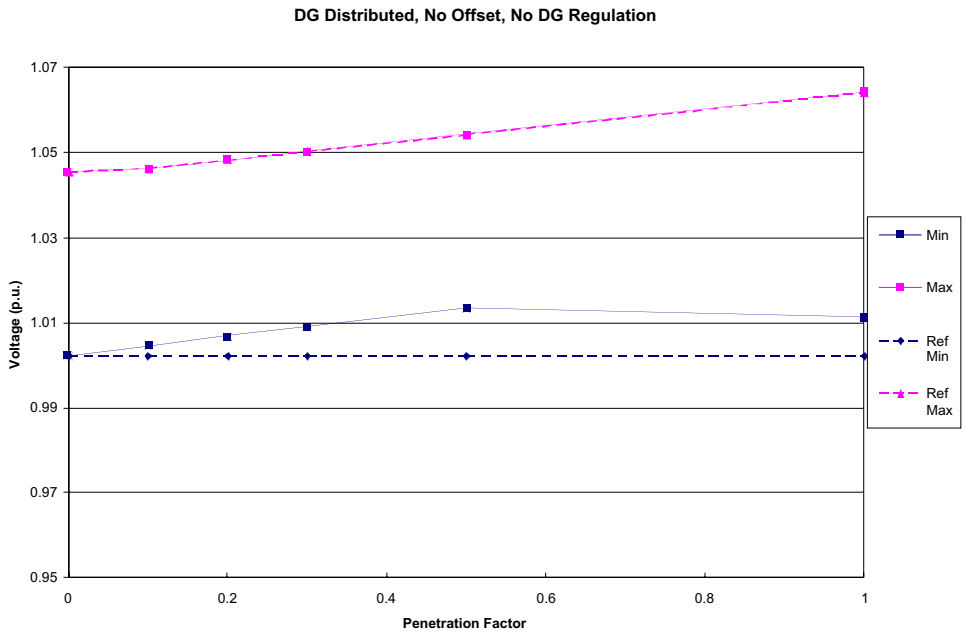
3.2.1.1.1



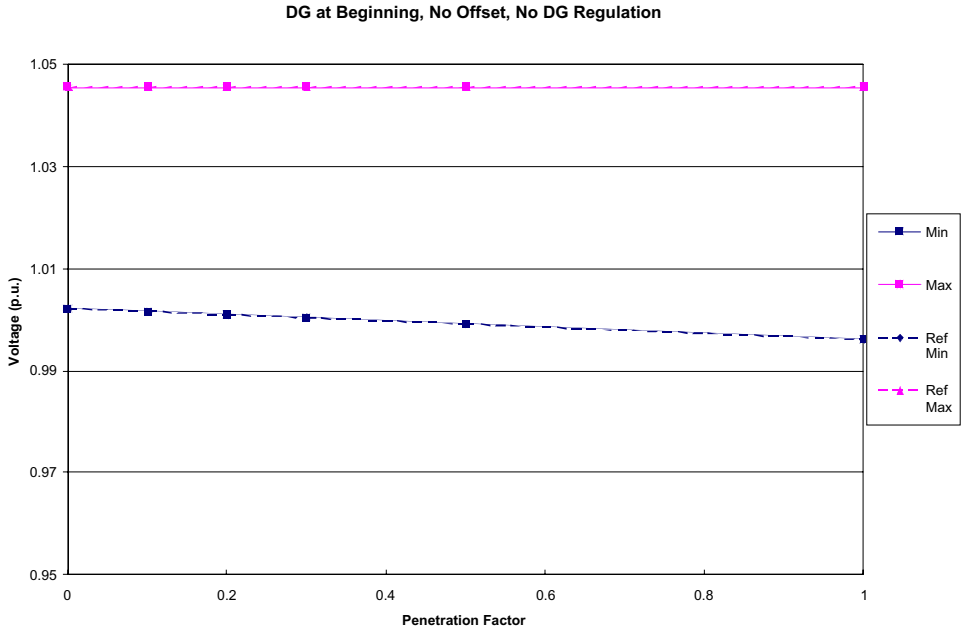
3.2.1.1.2



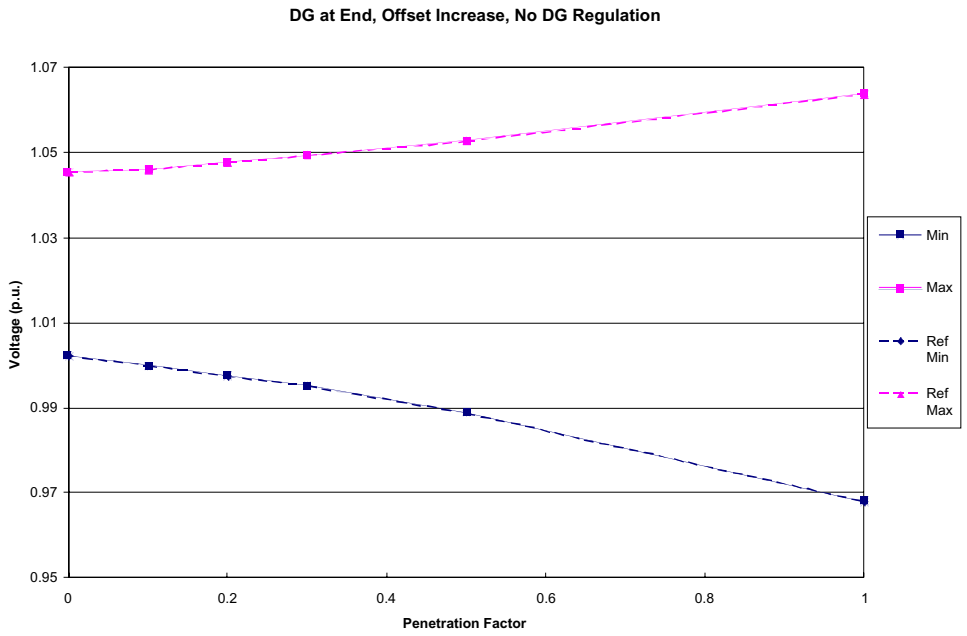
3.2.1.1.3


DG Distributed, No Offset, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

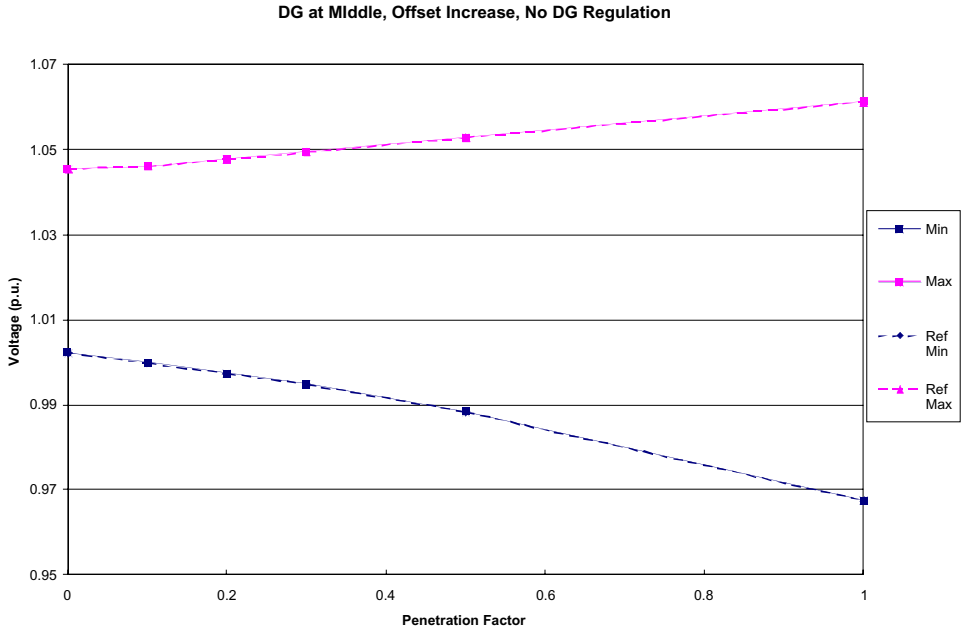
3.2.1.1.4


DG at Beginning, No Offset, No DG Regulation
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

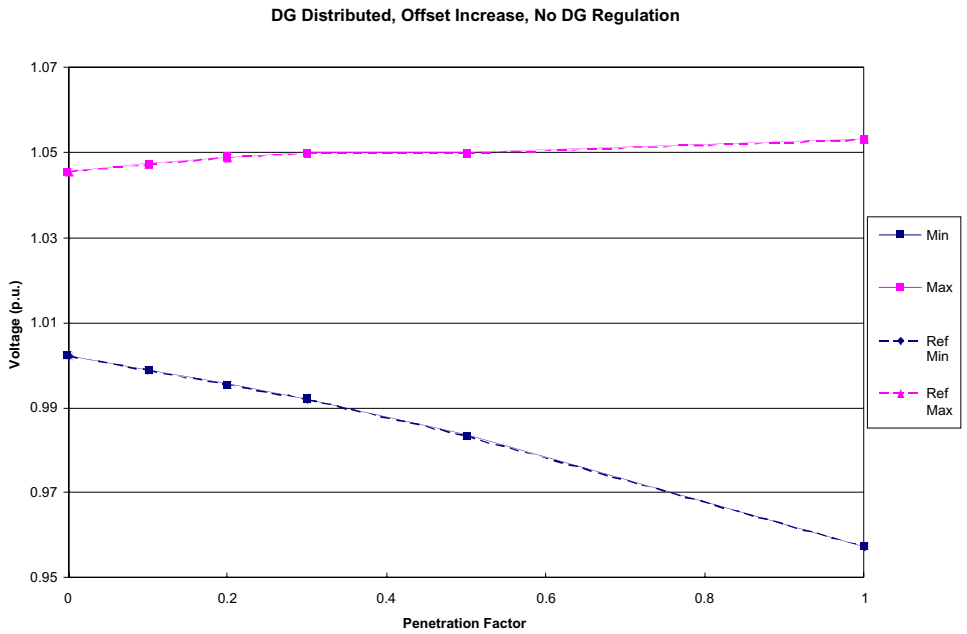
3.2.1.2.1


DG at End, Offset Increase, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

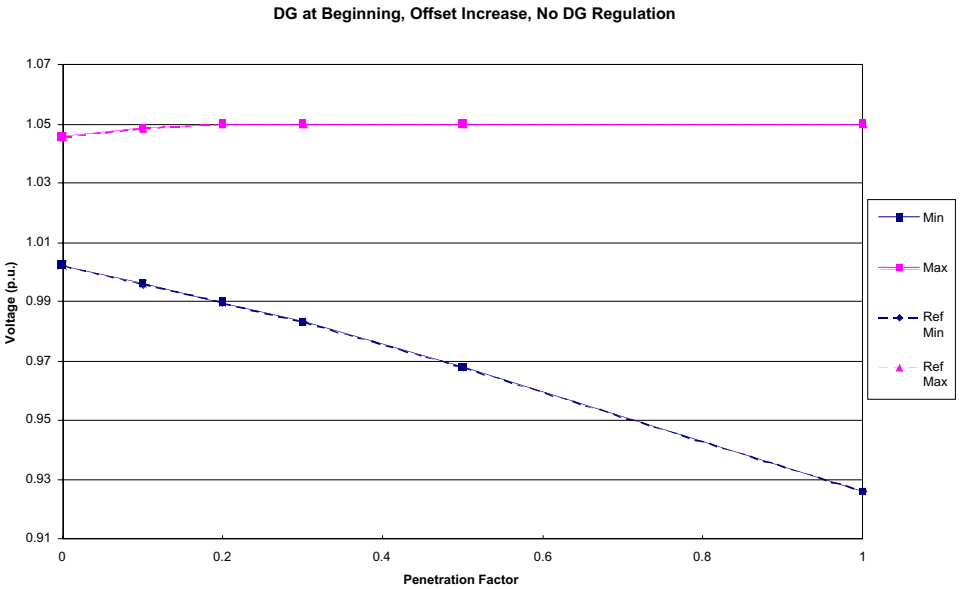
3.2.1.2.2


DG at MIddle, Offset Increase, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

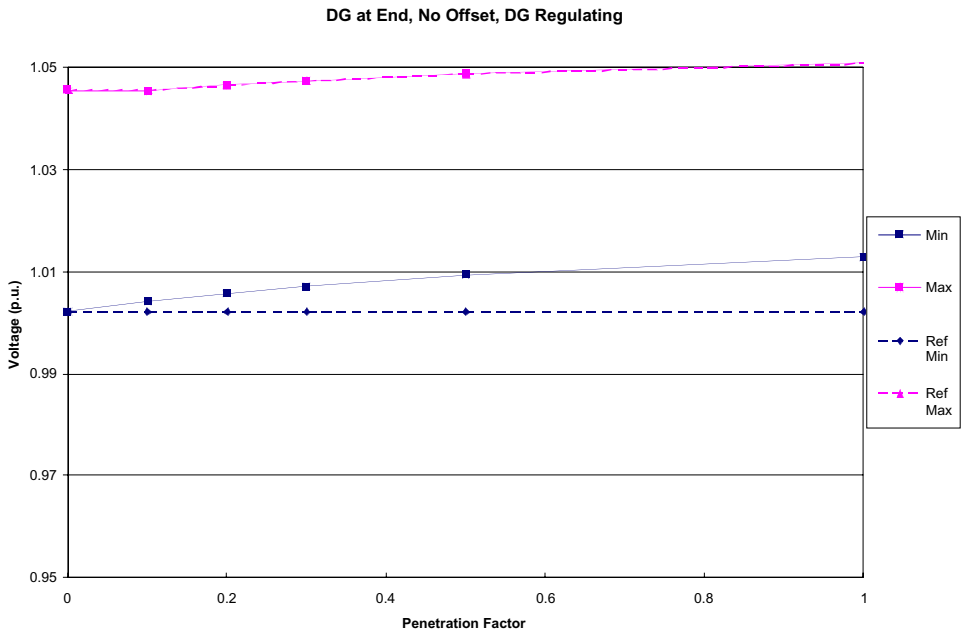
3.2.1.2.3


DG Distributed, Offset Increase, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

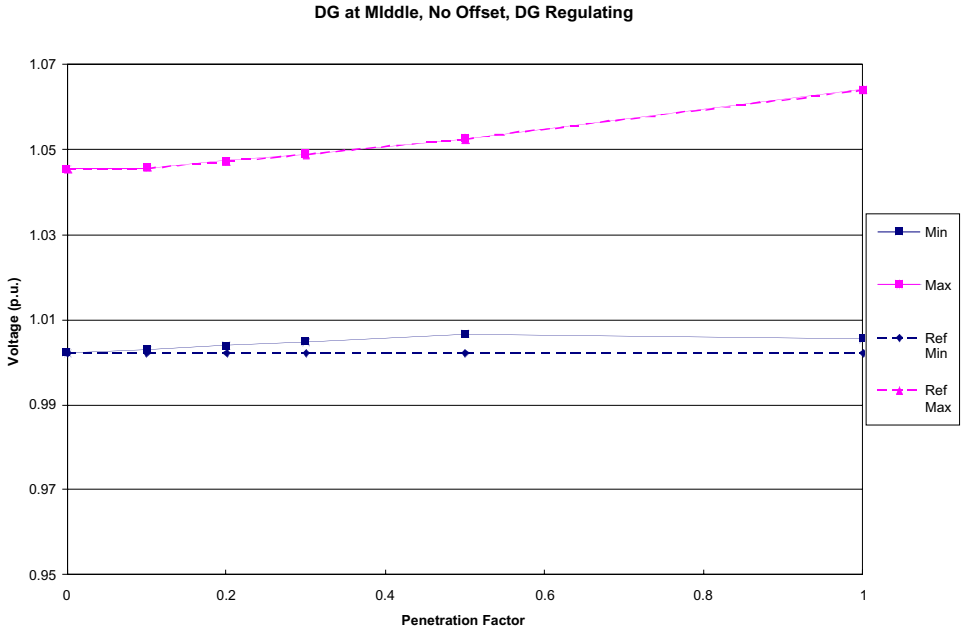
3.2.1.2.4


DG at Beginning, Offset Increase, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
0.91
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

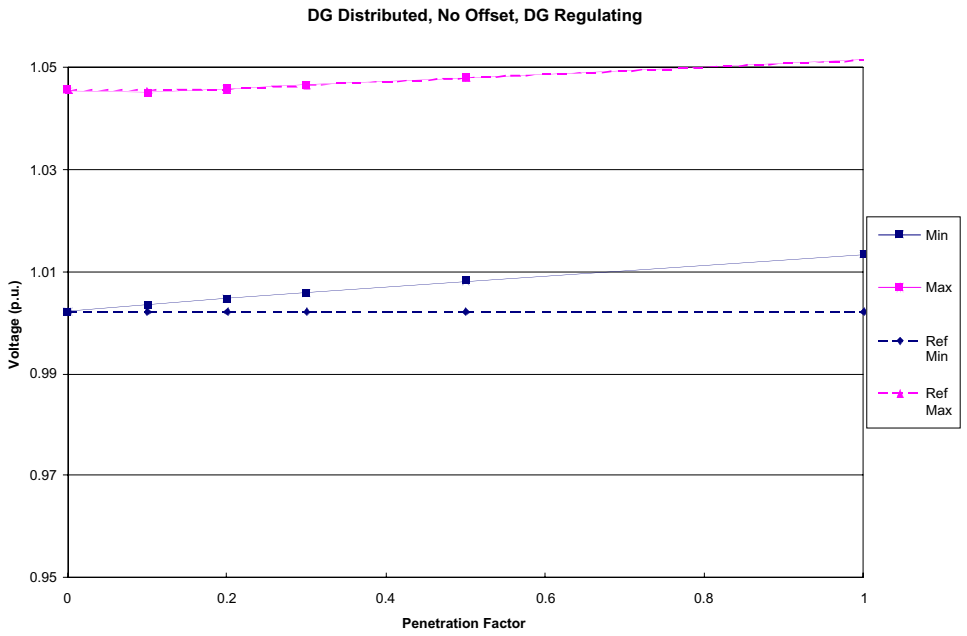
3.2.2.1.1


DG at End, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

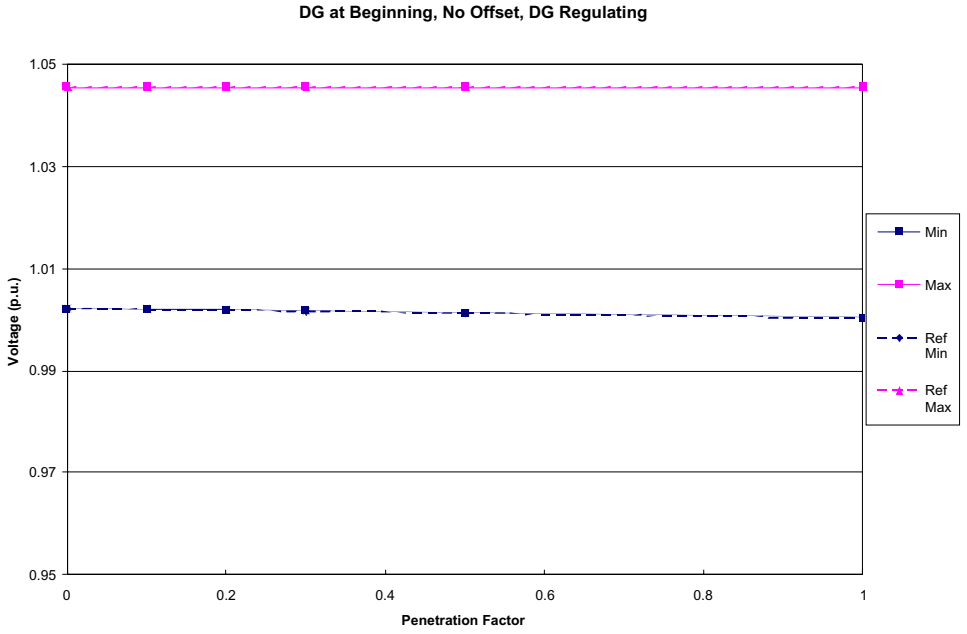
3.2.2.1.2


DG at MIddle, No Offset, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

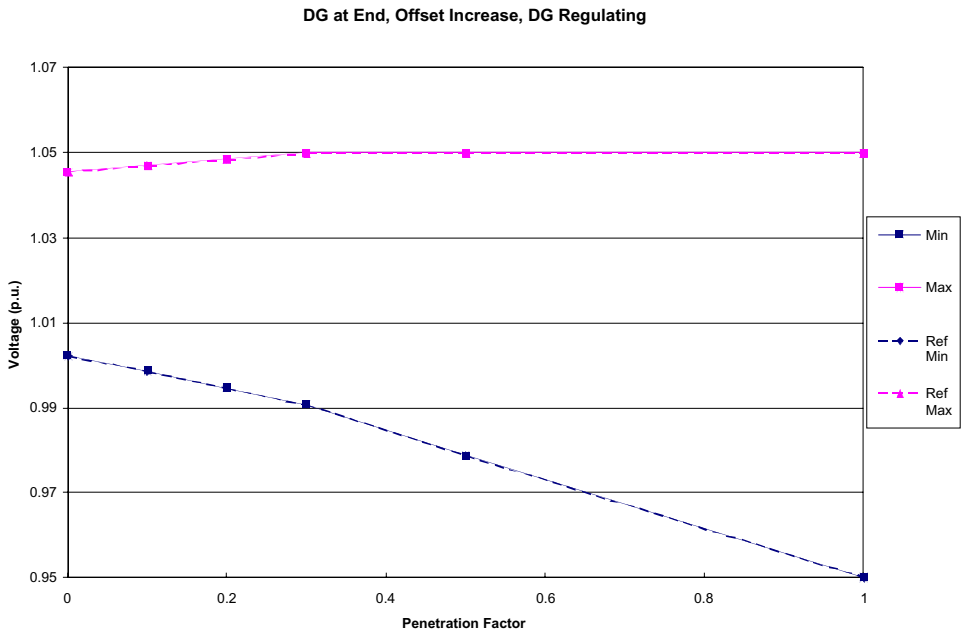
3.2.2.1.3


DG Distributed, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

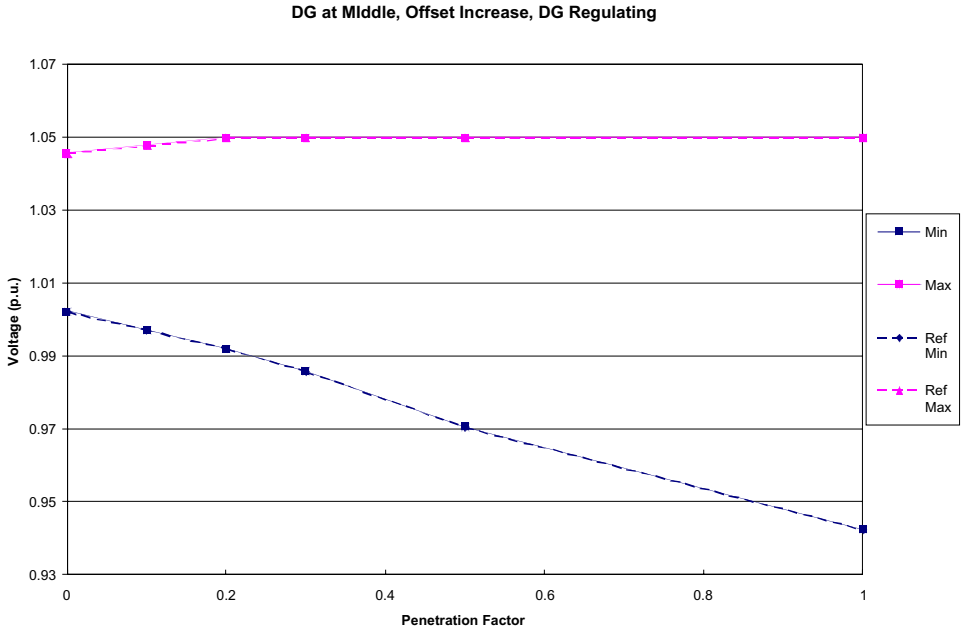
3.2.2.1.4


DG at Beginning, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

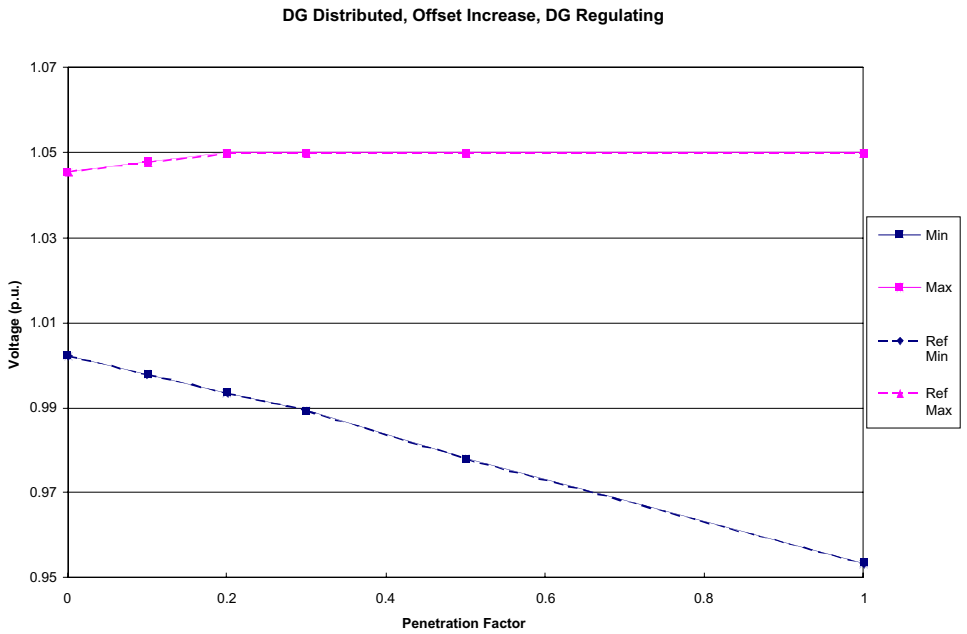
3.2.2.2.1


DG at End, Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

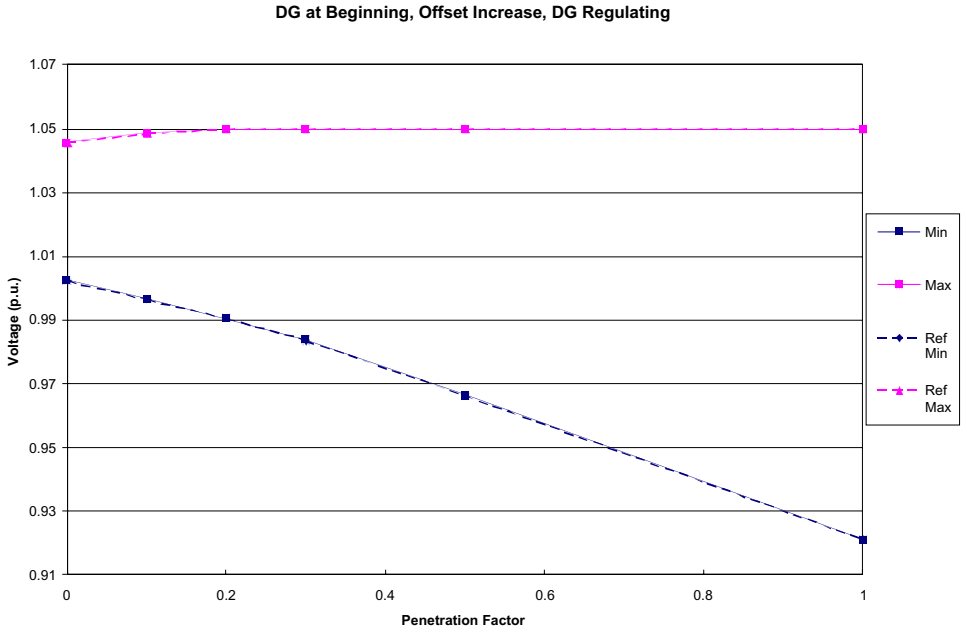
3.2.2.2.2


DG at MIddle, Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

3.2.2.2.3

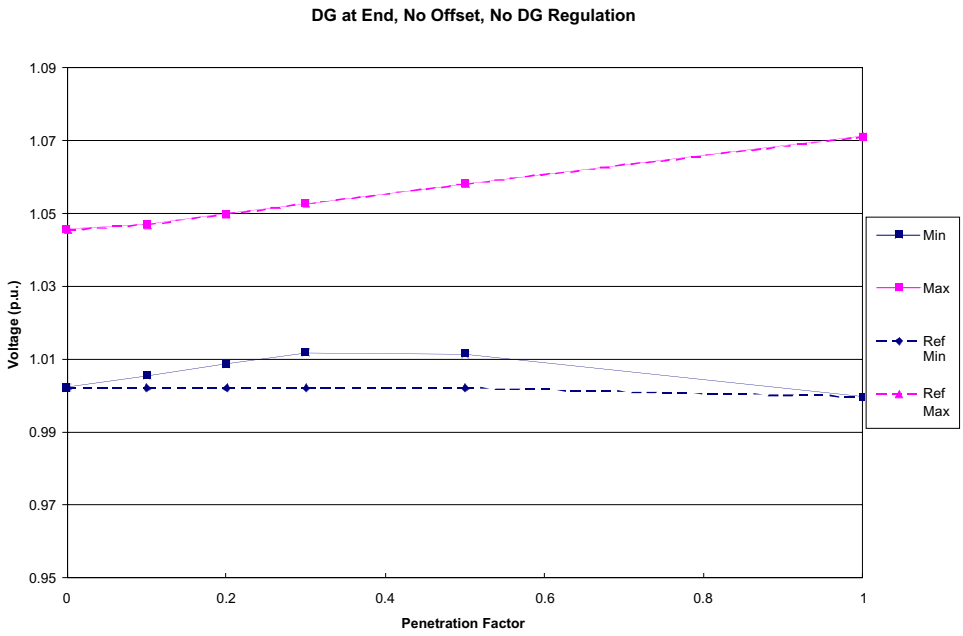

DG Distributed, Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

3.2.2.2.4

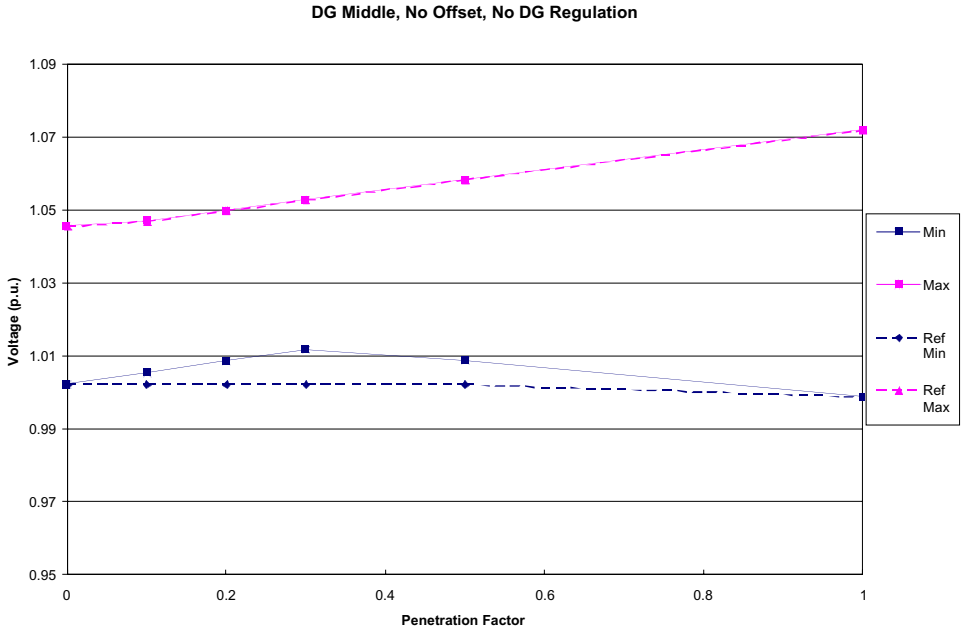

DG at Beginning, Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
0.91
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

BASE DESIGN 3.3

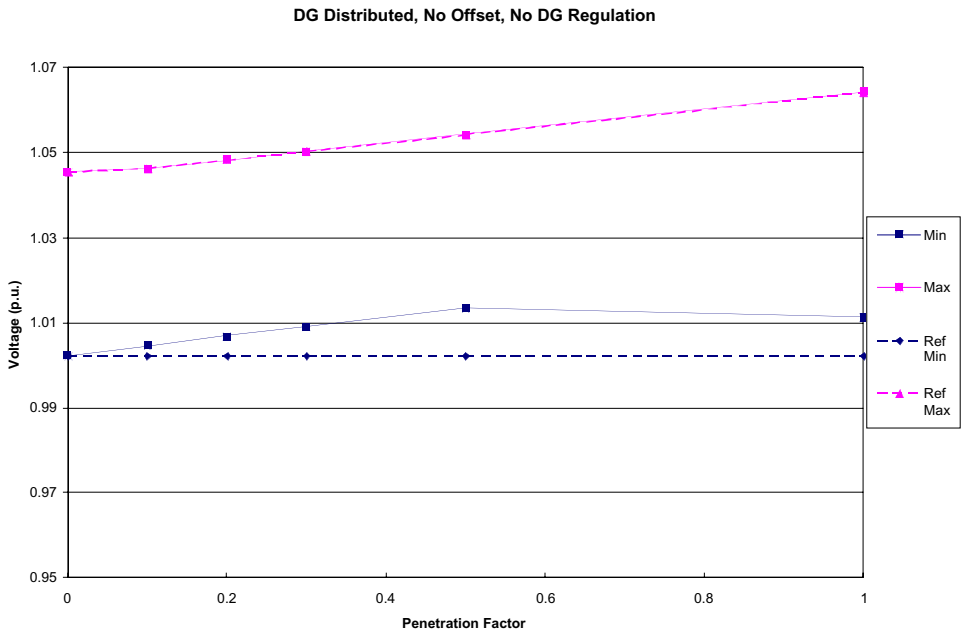
3.3.1.1.1



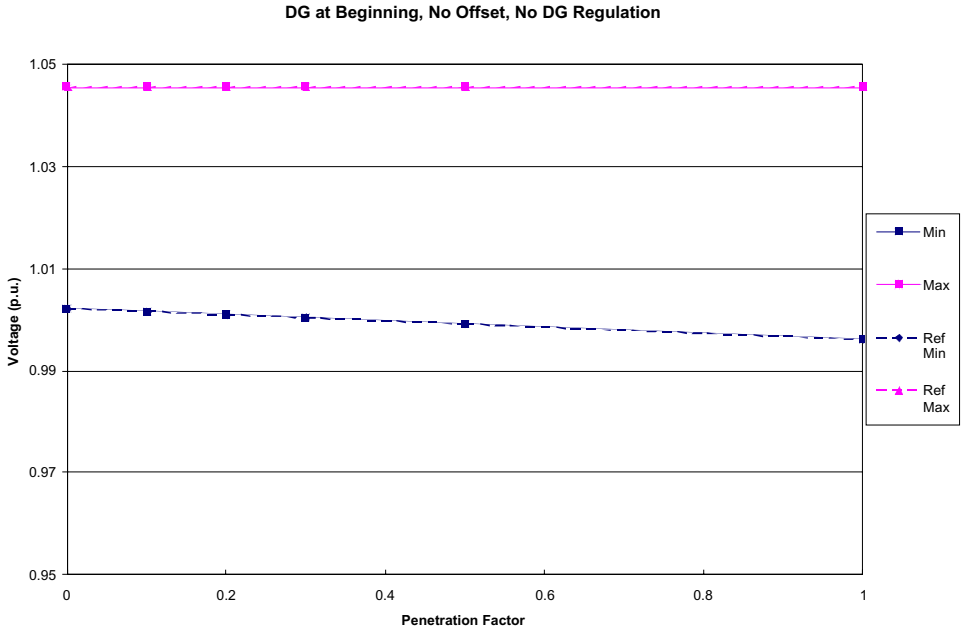
3.3.1.1.2



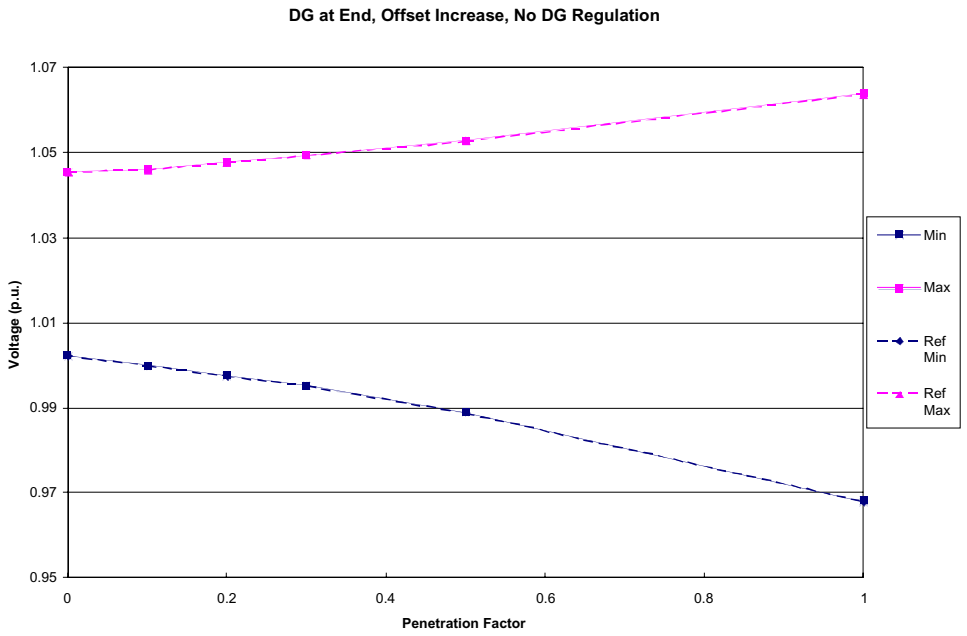
3.3.1.1.3


DG Distributed, No Offset, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

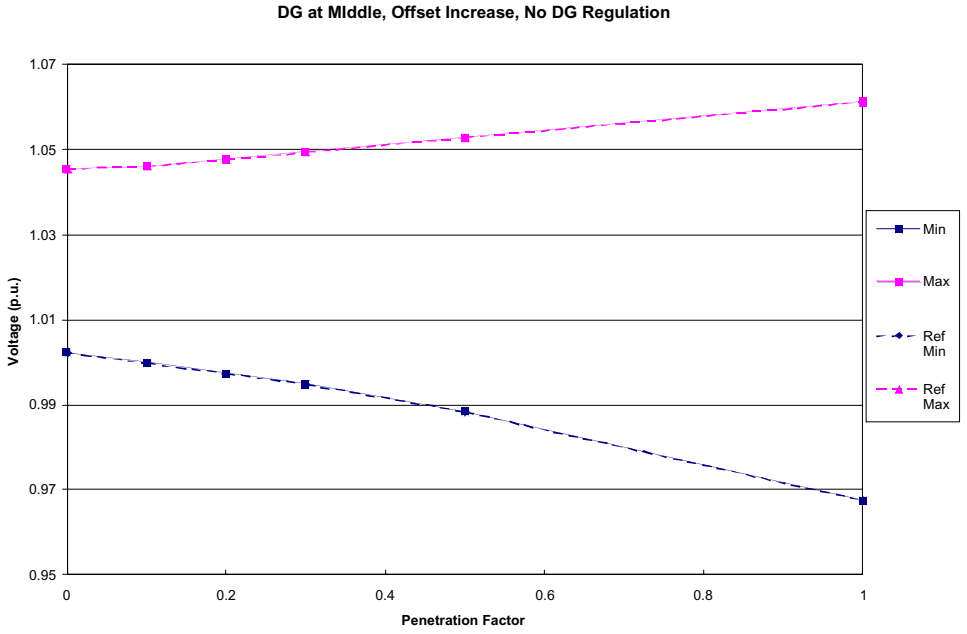
3.3.1.1.4


DG at Beginning, No Offset, No DG Regulation
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

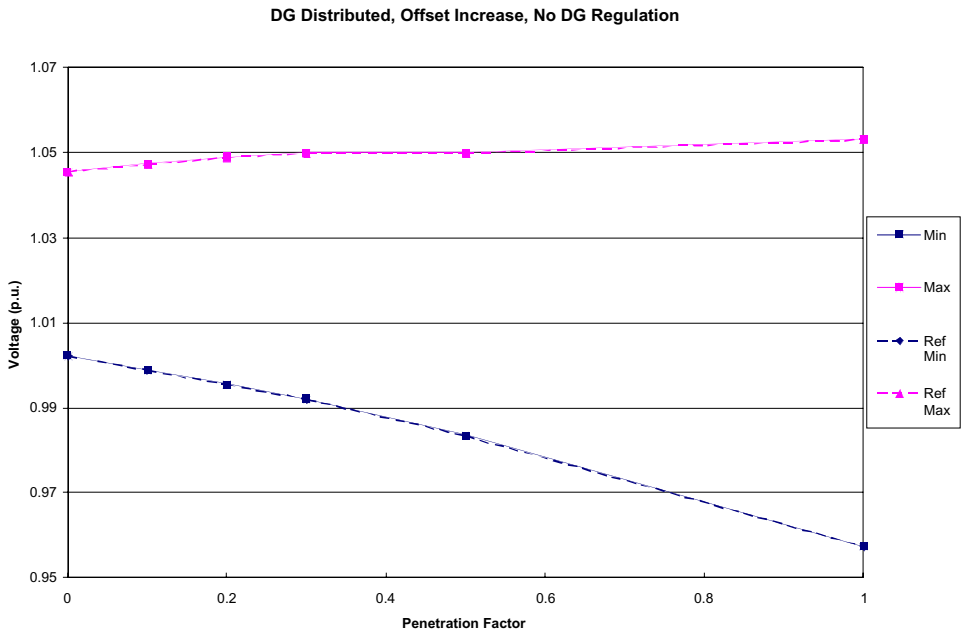
3.3.1.2.1


DG at End, Offset Increase, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

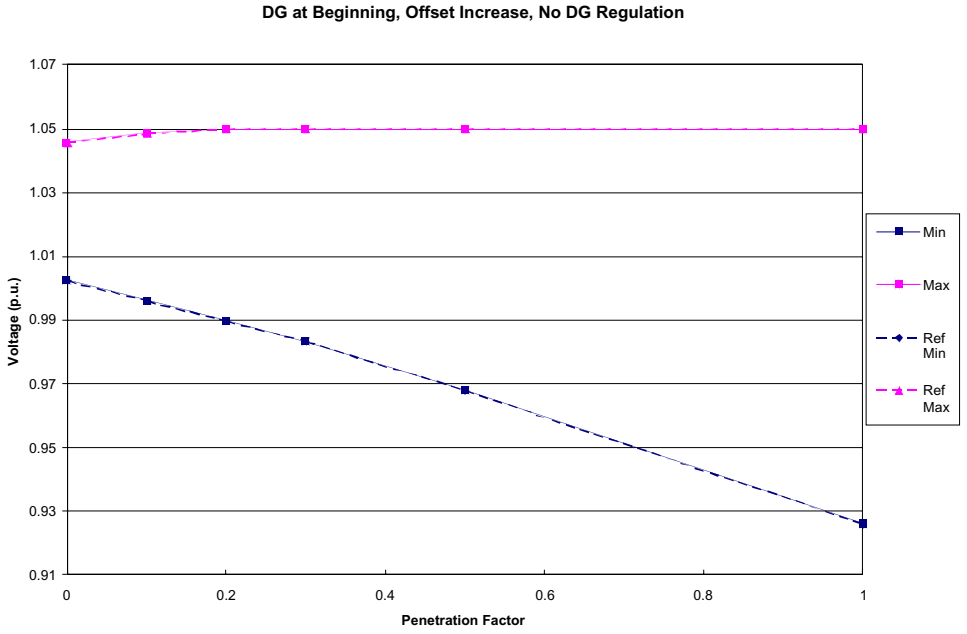
3.3.1.2.2


DG at MIddle, Offset Increase, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

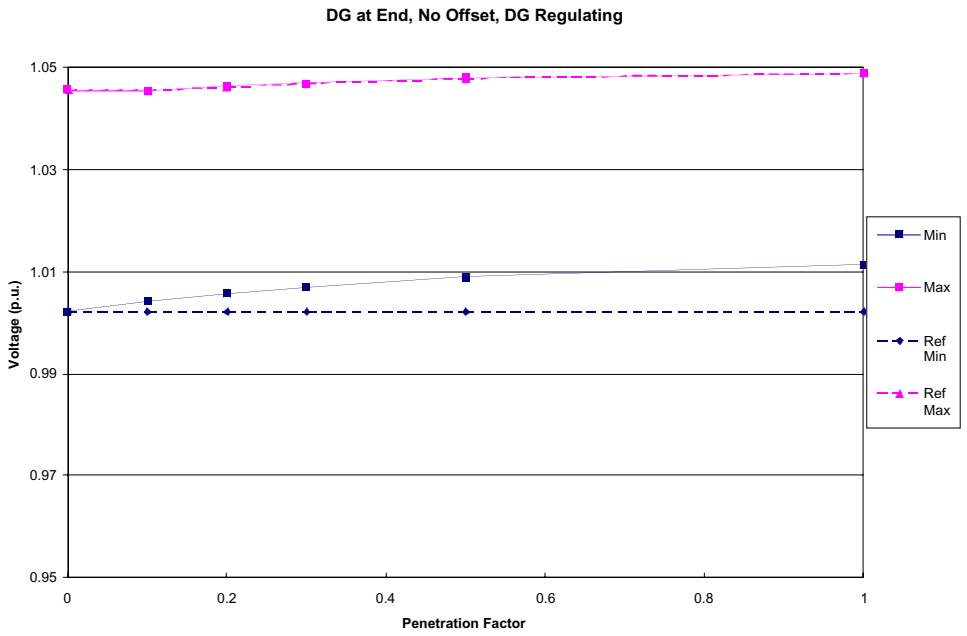
3.3.1.2.3


DG Distributed, Offset Increase, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

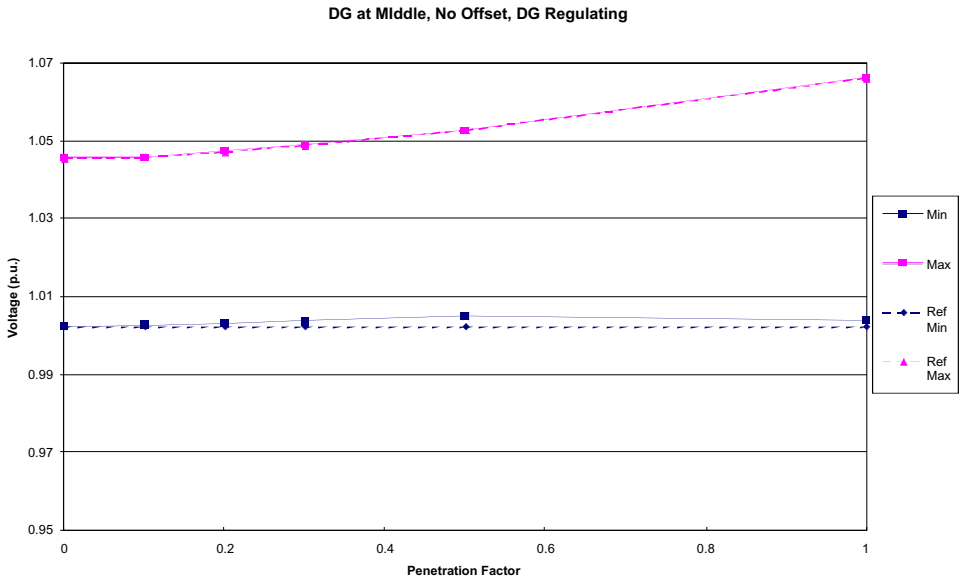
3.3.1.2.4


DG at Beginning, Offset Increase, No DG Regulation
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
0.91
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

3.3.2.1.1


DG at End, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

3.3.2.1.2


DG at MIddle, No Offset, DG Regulating
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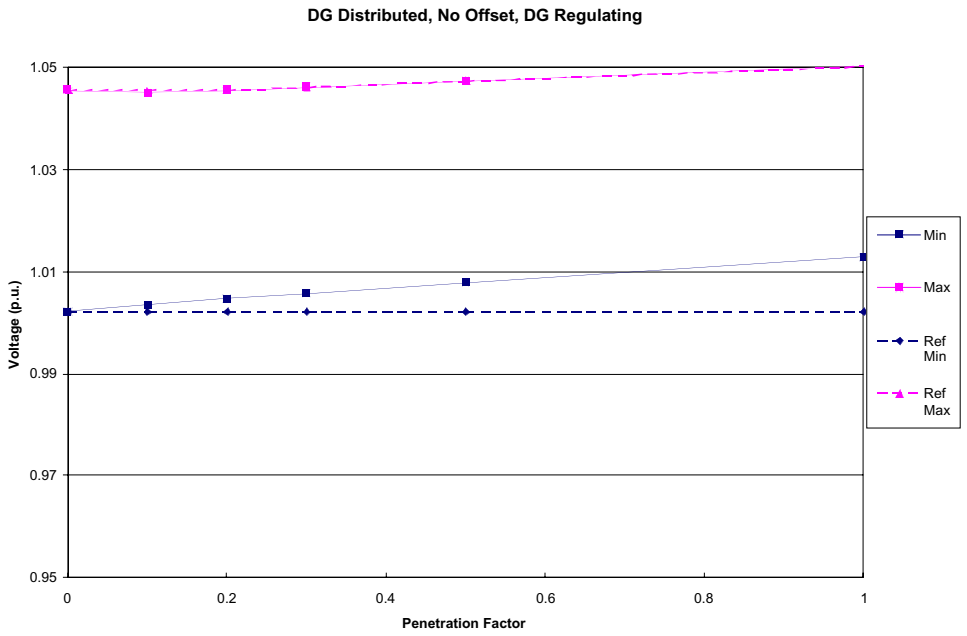
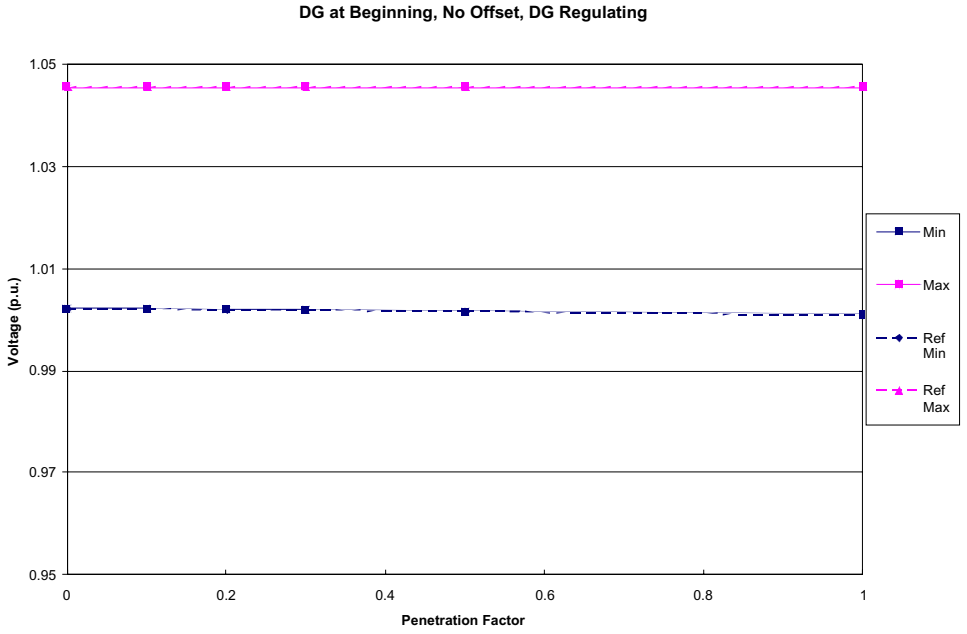
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

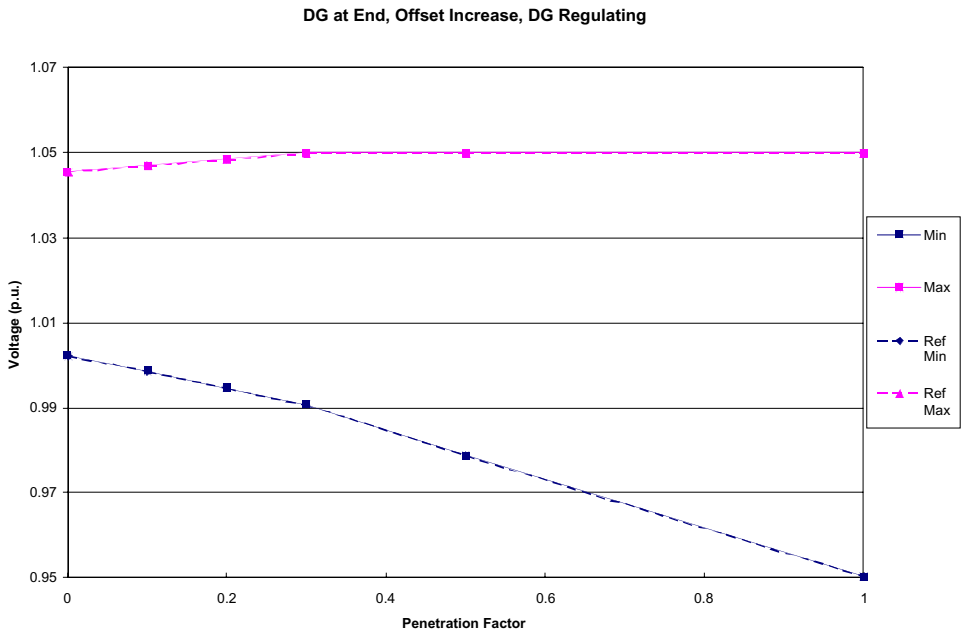
3.3.2.1.3


DG Distributed, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

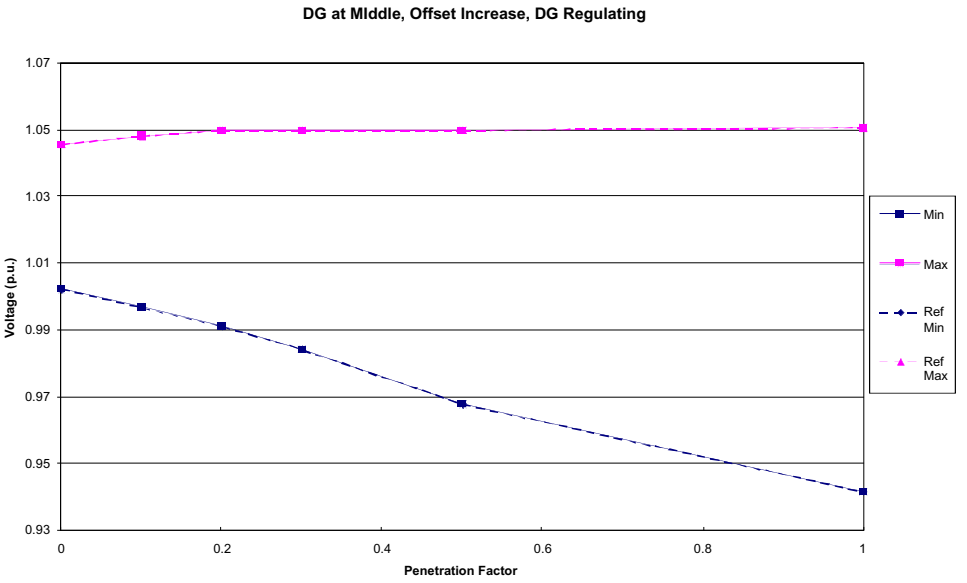
3.3.2.1.4


DG at Beginning, No Offset, DG Regulating
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

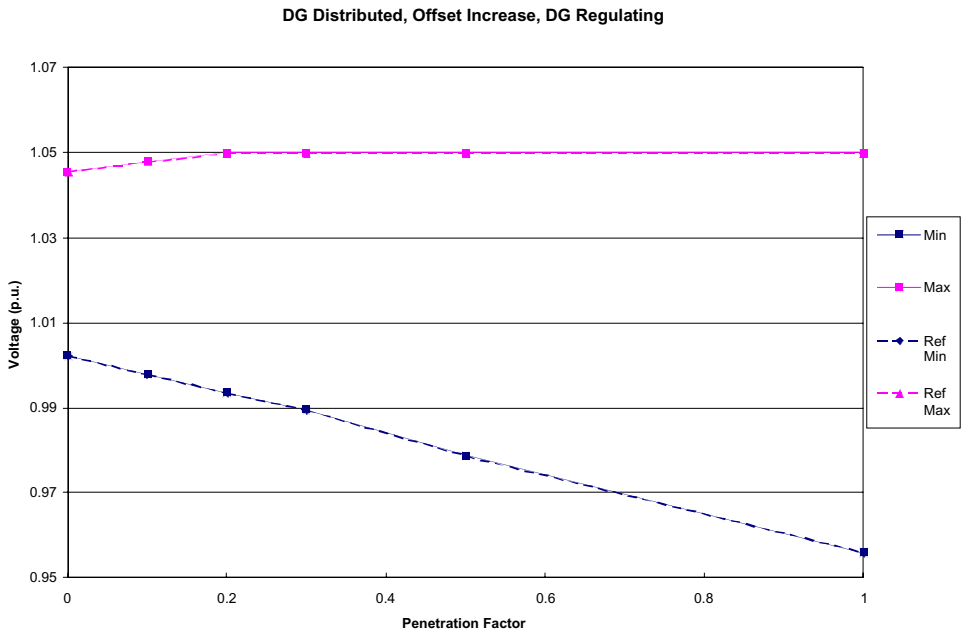
3.3.2.2.1


DG at End, Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

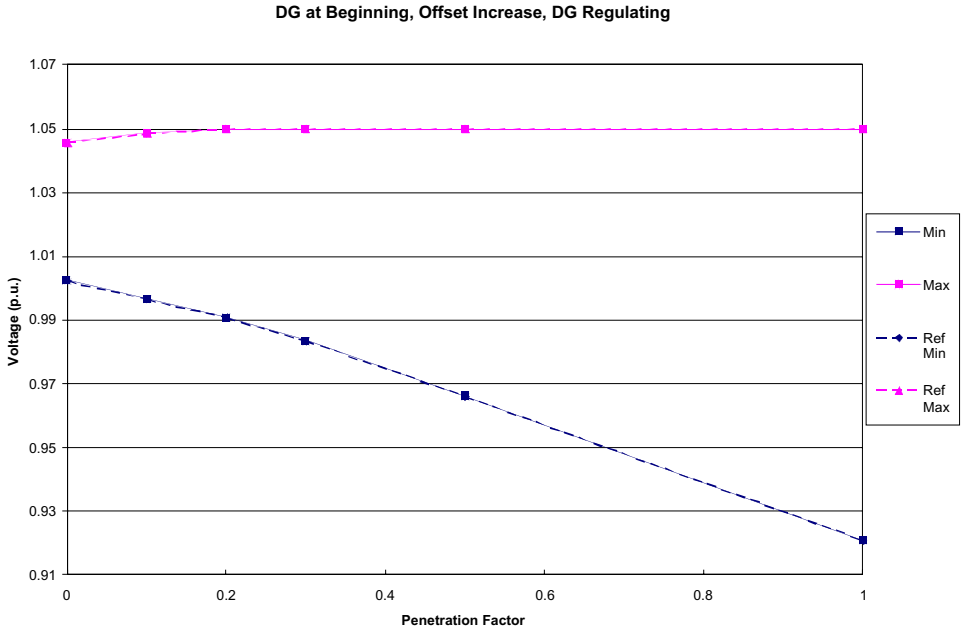
3.3.2.2.2


DG at MIddle, Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

3.3.2.2.3


DG Distributed, Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

3.3.2.2.4


DG at Beginning, Offset Increase, DG Regulating
1.07
1.05
1.03
1.01
0.99
0.97
0.95
0.93
0.91
Voltage (p.u.)
0
0.2
0.4
0.6
0.8
1
Penetration Factor
Min
Max
Ref Min
Ref Max

Appendix B. Narrative Discussion of Generic Feeder Voltage Regulation Cases

CASE 1.1

Description of the Feeder

Feeder Length: 4 miles
LTC: Tap setting = 1.05, Resistive LDC =0.0, Reactive LDC = 0.0
SVR: None
Capacitor Banks: None
Regulation Reference Point (when regulation is enabled): DG voltage (secondary)

Scenario 1- Feeder load independent of DG penetration

(This scenario labeled No offset on the plots.)

For this scenario, the voltage regulation problems occur for the light load situation. An overvoltage problem occurs when the DG is lumped at the end (starting at a penetration factor of 20%) and the middle (30%) of the feeder. When the DG is lumped at the beginning and distributed throughout the feeder, no problem exists. When the DG is permitted to regulate its local voltage, the over voltage problem is eliminated for both DG at the end and middle.
There are no voltage regulations problems caused by DG penetration for the heavy load condition.

Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity (Offset increase)

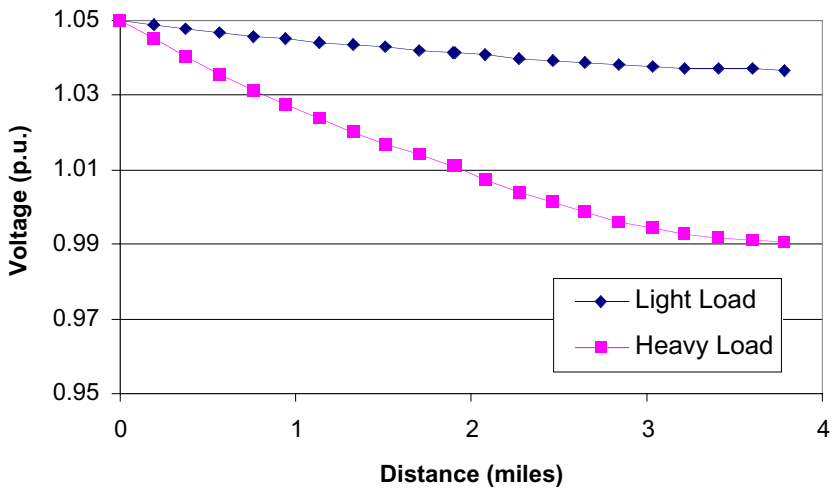
(This scenario labeled Offset increase on the plots.)

For the light load condition, there is only a minor overvoltage problem when the DG is lumped at the end of the feeder, but this problem occurs only for a very large penetration factor (100%). Therefore, it is not a major concern. Also, when voltage regulation is applied to the DG, this overvoltage is eliminated.

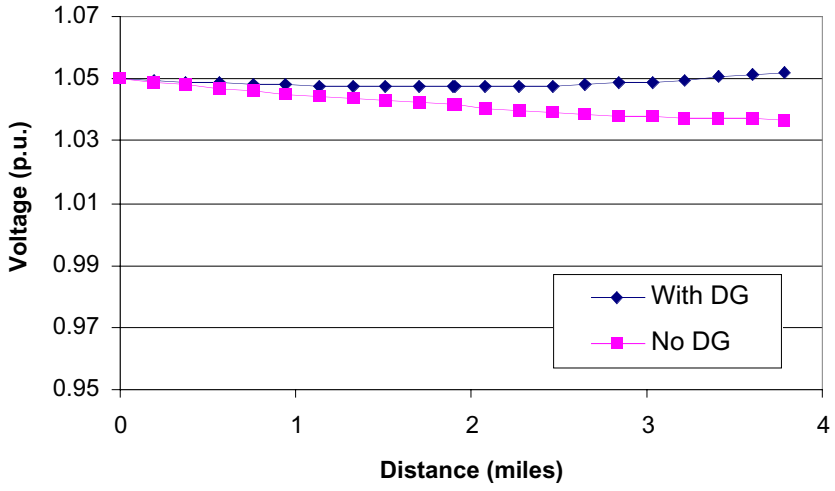
For the case of heavy load situation, a huge under-voltage occurs; particularly when the DG is lumped at the beginning (threshold at 20% penetration factor), but is least severe when the DG is lumped at the end (threshold between 50% and 100% penetration). This can be explained because the additional incremental load forces the system to supply the additional reactive power, increasing the voltage drop across the feeder. When the DG is situated at the beginning of the feeder, the power contribution from the DG and the grid add together to create a large voltage drop. Providing voltage regulation capability to the DG, within the typical DG reactive capacity constraints, does not mitigate this problem.

CASE 1.1

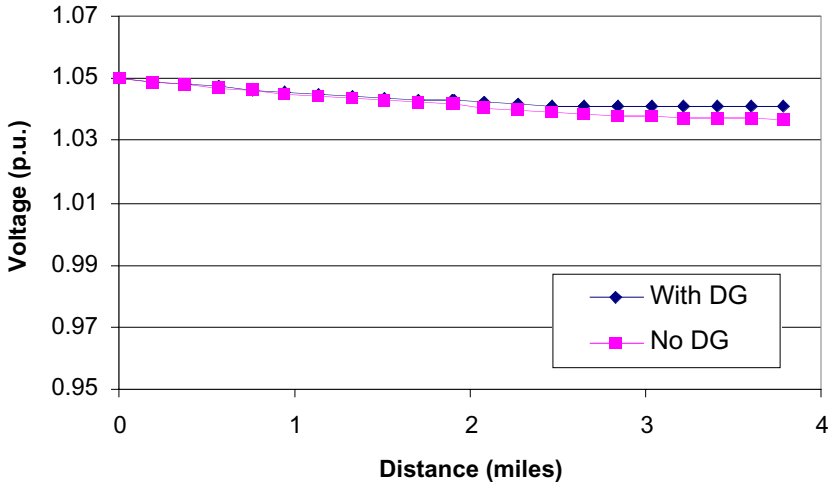
Base Case (No DG)



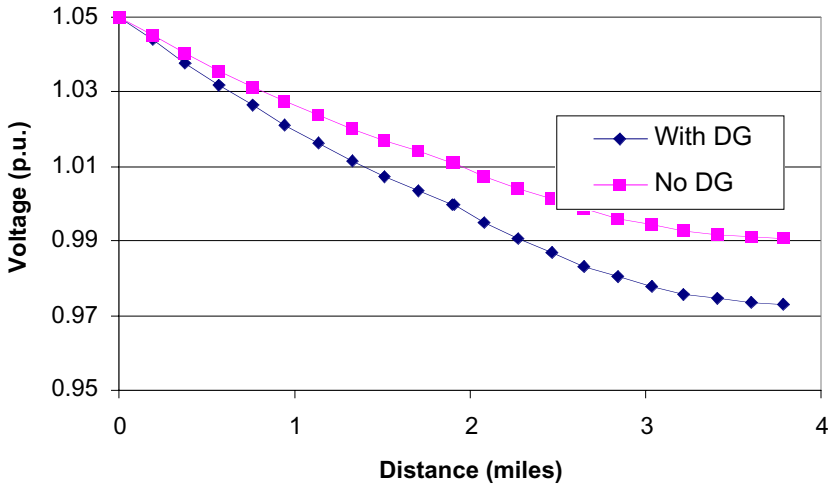
Light Load, No offset, DG at the End, (30% Penetration)



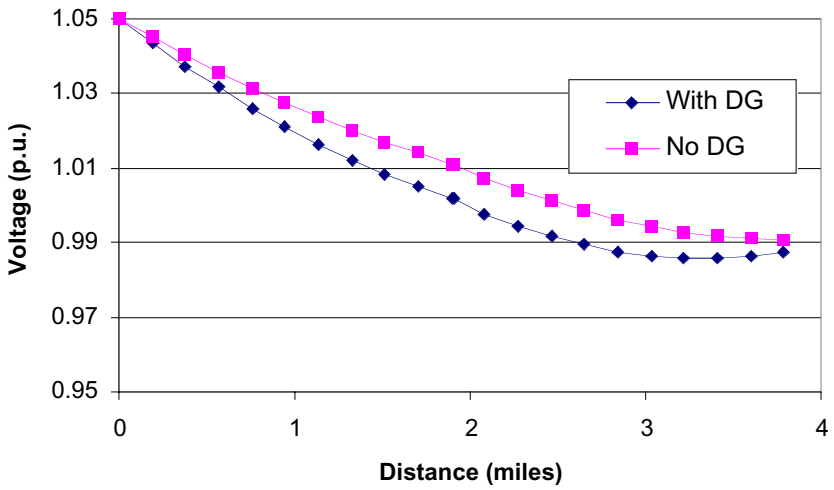
Light Load, No offset, Regulation, DG at the End, (30% Penetration)



Heavy Load, Offset increase, DG at the Beginning (30% Penetration)



Heavy Load, Offset increase, DG at the End, (50% Penetration)



CASE 1.2

Description of the Feeder

Feeder Length: 4 miles
LTC: Tap setting = 1.04, Resistive LDC =0.3, Reactive LDC = 0.6, Max=1.05
SVR: None
Capacitor Banks: None
Regulation Reference Point (when regulation is enabled): DG voltage (secondary)

Scenario 1- Feeder load independent of DG penetration

This scenario is similar to the situation in case 1.1 for light load, but the load drop compensation (LDC) in the LTC control helps improve the situation. With LDC, there is no overvoltage problem when the DG is lumped in the middle of the feeder. For the DG located at the end, the threshold of concern has been raised from 20% penetration in case 1.1 to between 30% and 50% penetration. The reason for this is that the DG is providing more power than the load demand for the light load case, and the substation source is absorbing power, the LTC load drop compensation works in a reversed way and reduces the voltage at the substation end. The decrease in substation voltage is sufficient to allow for the voltage rise along the feeder such that the voltage at the feeder end is in the acceptable range. Voltage regulation by the DG is effective in eliminating the overvoltage that do occur.

Like in case 1.1, there is no voltage regulation problem for the heavy load situation.

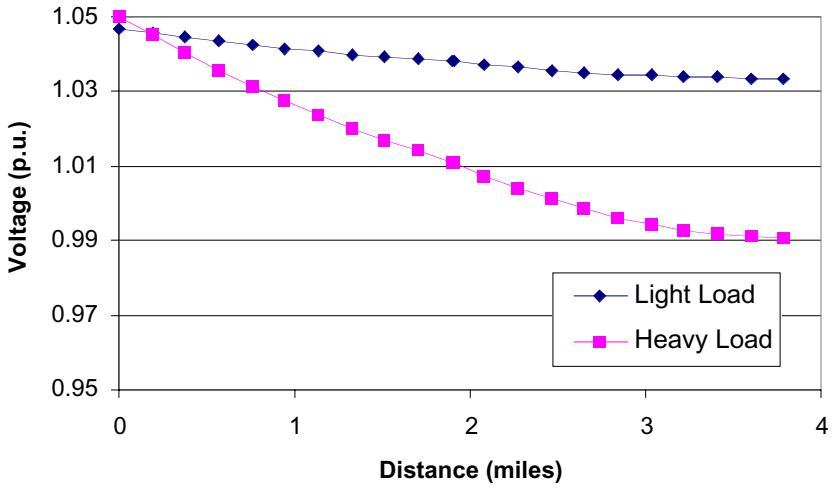
Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

The situation for the light load condition is very similar to case 1.1; overvoltage exists at the end of the feeder for very large (close to 100%) penetration. Also, when regulation by DG is applied, this small problem is eliminated.

For heavy load the situation does not change from case 1.1. Although load drop compensation was added, the LTC was locked to a maximum of 1.05 p.u. in order to not reach unacceptable overvoltage levels at loads close to the substation. Basically, the regulation by the LTC is the same as in case 1.1, and voltage regulation is not an adequate mitigant.

CASE 1.2

Base Case (No DG)



Light Load, No offset, Regulation, DG at the End (30% Penetration)

CASE 1.3

Description of the Feeder

Feeder Length: 4 miles
LTC: Tap setting = 1.05, Resistive LDC =0.0, Reactive LDC = 0.0
SVR: None
Capacitor Banks: 4 banks located at 20%, 40%, 60% and 80% of the feeder length. Each bank supplies _ of the additional reactive power due to the incremental load, which depends on penetration factor and the power factor of the load. The compensation is fixed for each penetration level, and based on rated peak load. Thus, the compensation is present for the light load as well as heavy load situation, representing a compensation design using fixed capacitor banks.
Regulation Reference Point (when regulation is enabled): DG voltage (secondary)

Scenario 1- Feeder load independent of DG penetration

In this case, capacitors were added only in proportion to the incremental load added with increased DG penetration. In this scenario, feeder loads are fixed. Thus, for this scenario, results are the same as in Case 1.1.

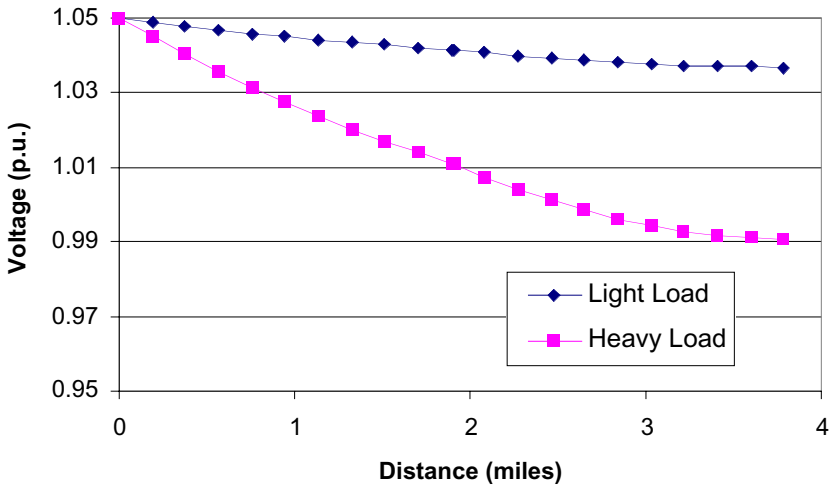
Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

For the light load case, the capacitor aggravate the overvoltage problem. Instead of only overvoltage problems being limited to the situation where the DG is located at the end of the feeder, overvoltages also occur when the DG is located in the middle of the feeder, or when the DG is uniformly distributed. However, when DG voltage regulation is enabled, this overvoltage problem is eliminated.

For the heavy load situation, providing incremental rective compensation helps, but this measure is not sufficient to avoid serious undervoltage problems.

CASE 1.3

Base Case (No DG)



CASE 2.1

Description of the Feeder

Feeder Length: 8 miles
LTC: Tap setting = 1.01, Resistive LDC =0.75, Reactive LDC = 1.5
SVR: None
Capacitor Banks: 900 kVA banks located at 20%, 40%, 60% and 80% of the feeder length.
Regulation Reference Point (when regulation is enabled): DG voltage (secondary)

Scenario 1- Feeder load independent of DG penetration

For light load, the load drop compensation reduces the voltage at the substation end. Because of the high LDC settings, undervoltage problems occur for all the tested DG locations, starting at a 50% DG penetration factor. Also, above a 50% penetration, there is an overvoltage problem when the DG is at the remote end of the feeder. Allowing regulation by the DG increases the threshold of voltage regulation problems to between 50% and 100% penetration for all DG locations other than DG at the beginning of the feeder. With the DG at the beginning, the undervoltage problem becomes more severe when DG voltage regulation is included.

When the feeder is heavily loaded, the load drop compensation is effective in minimizing undervoltage problems. Undervoltage occurs only when the DG is at the beginning with very large penetration factors. Voltage regulation by the DG solves this problem.

Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

For the light load situation, there are no voltage regulation problems.
The incremental load results in severe voltage regulation problems when the system is heavily loaded. First, due to the load drop compensation on the LTC, there are overvoltage problems for any penetration factor greater than zero, and for all DG locations. Additionally, this excessive boost at the LTC is still not enough to compensate for the voltage drop across the feeder. This results in undervoltage problems, particularly when the DG is located at the beginning. Only when the DG is at the end is this under-voltage problem not present. Regulation by the DG is not effective in mitigating these problems.

CASE 2.2

Description of the Feeder

Feeder Length: 4 miles
LTC: Tap setting = 1.02, Resistive LDC =0.6, Reactive LDC = 1.1 Max=1.05
SVR: None
Capacitor Banks: 1200 kVA banks located at 20%, 40%, 60% and 80% of the feeder length.

Regulation Reference Point (when regulation is enabled): DG voltage (secondary)

Scenario 1- Feeder load independent of DG penetration

Light load: By reducing the load drop compensation and increasing the capacitive compensation, the undervoltage problem of case 2.1 at the substation is almost eliminated (little under-voltage at 100% penetration for all locations). However, there now exists an even larger overvoltage at the remote end of the feeder with lower penetration thresholds (end: 20%, middle: 30-50%, distributed: 30-50%). Applying DG voltage regulation eliminates the overvoltage problem.

Heavy Load: Similar to case 2.1.

Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

Light Load: Large overvoltages appear at 20% penetration when the DG is located at the end. DG regulation eliminates this problem.

Heavy Load: By setting a maximum to the LTC voltage, the overvoltage problem of Case 2.1 is eliminated. However, this increases the undervoltage problem that occurs at every location of the DG (50% penetration for DG at the feeder end, 20% middle, 20% distributed, 10% beginning). When the DG is located at the beginning, the undervoltage is very severe. At the remote end of the feeder, the voltage drops as low as 0.87 p.u. Voltage regulation does not eliminate the problem.

CASE 3.1

Description of the Feeder

Feeder Length: 8 miles
LTC: Tap setting = 1.02, Resistive LDC =0.5, Reactive LDC = 1
SVR: Tap setting = 1.01, Resistive LDC =1.0, Reactive LDC = 2.0
Capacitor Banks: 900 kVA banks located at 20%, 40%, 60% and 80% of the feeder length.

Regulation Reference Point (when regulation is enabled): DG voltage (secondary)

Scenario 1- Feeder load independent of DG penetration

For the light load situation, there is no overvoltage problem due to the corrective action of the load drop compensation. Instead, undervoltages occur at the feeder location immediately after the SVR when the DG is located at the middle and at the end for large penetration factors (threshold of concern is 50% penetration). This can be attributed to the excessive load drop compensation of the SVR and to the direction of the real power at that location. When the DG is located at the end and the middle (both locations are after the SVR) the flow of real power is high in the direction of the substation, so the real component of the drop compensation at the SVR reduces the voltage significantly. Additionally, there is also flow of reactive power (supplied by the cap banks) in that direction at the SVR location, which makes the reactive component of the drop compensation to further reduce the voltage at that point. When the DG is distributed, or at the beginning, there is no undervoltage since the real flow is now reversed. Regulation by the DG does not eliminate the problem. For the DG located at the middle of the feeder, regulation of the DG secondary voltage toward a 1.0 p.u. setpoint aggravates the problem.

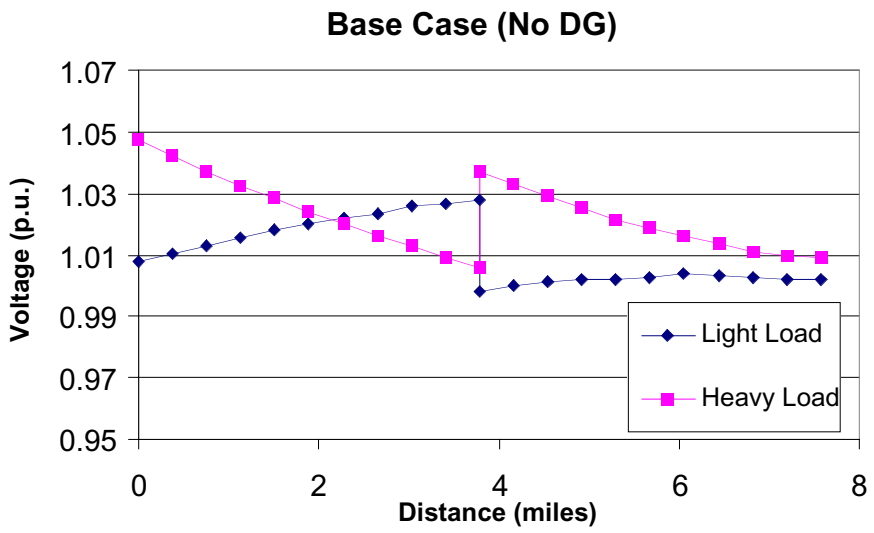
For the heavy load situation, there is no voltage regulation issue.

Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

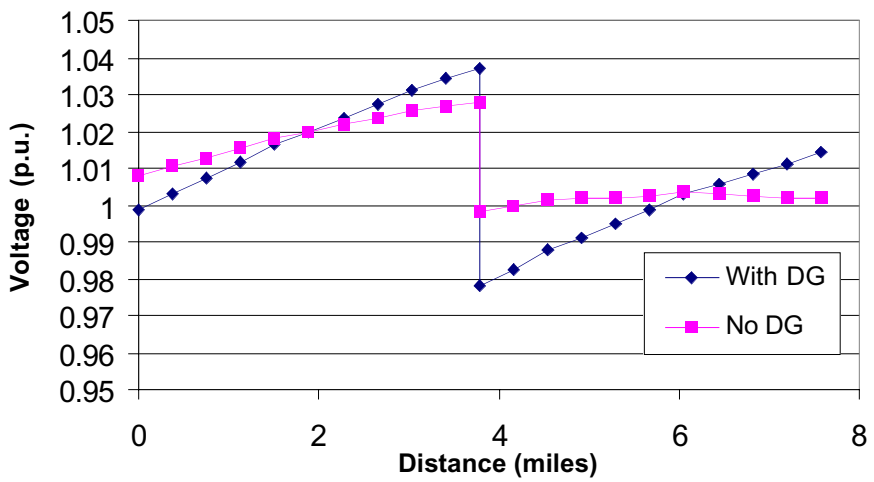
For the light load situation, there is also an undervoltage problem when DG is at middle or at the end, but the undervoltage problem is less severe than in Scenario 1 for this case (threshold penetration is almost 100%). DG regulation eliminates the undervoltage when the DG is at the end, but makes the situation worse when DG is at the middle.

For the heavy load situation, there is an overvoltage problem for any DG location and for any significant penetration factor. This occurs due to an excessive boost at the substation end by the LTC load drop compensation, and the fact that the LTC was limited to a maximum value in this case. Implementing DG voltage regulation aggravates this overvoltage problem.

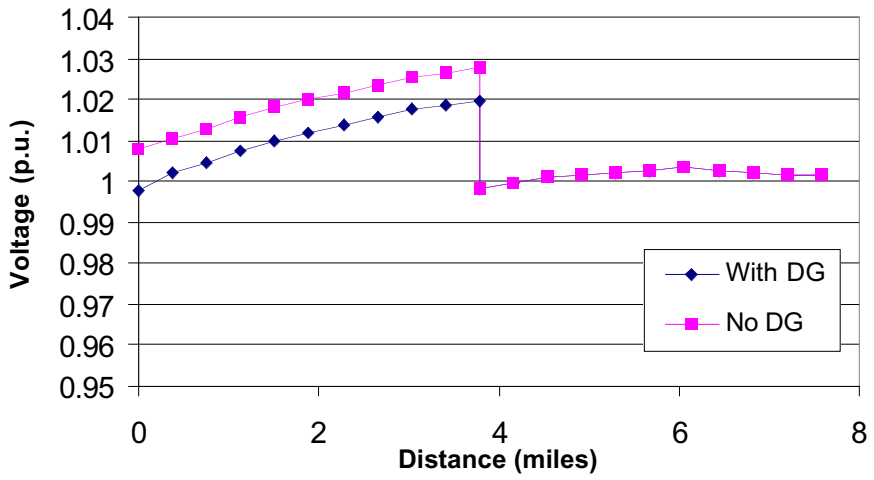
CASE 3.1



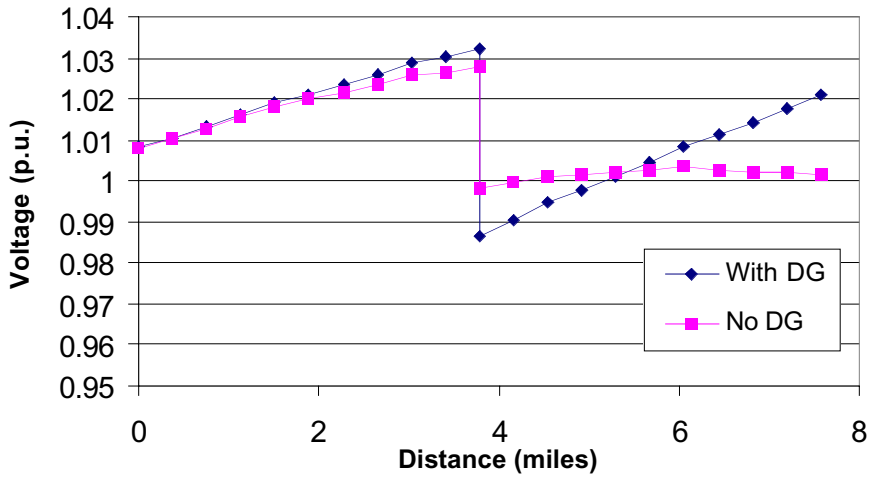
Light Load, No Offset, DG at the End (50% Penetration)



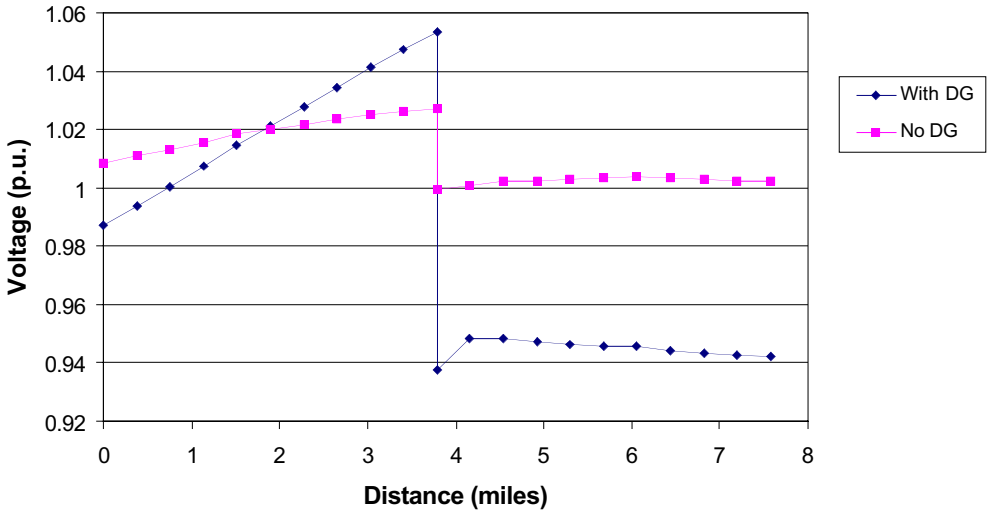
Light Load, No Offset, DG at the Beginning (50% Penetration)



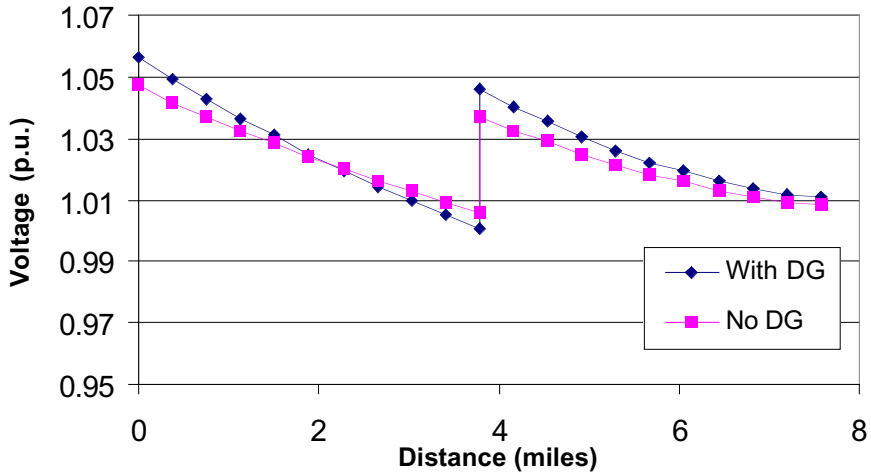
Light Load, Offset Increase, Regulation, DG at the End (100% Penetration)



Light Load, Offset Increase, Regulation, DG at the Beginning, 100%



Heavy Load, Offset Increase, DG Distributed (30% Penetration)



CASE 3.2

Description of the Feeder

Feeder Length: 8 miles
LTC: Tap setting = 1.03, Resistive LDC =0.25, Reactive LDC = 0.5 (Max =1.05)
SVR: Tap setting = 1.03, Resistive LDC =0.6, Reactive LDC = 1.1 (Max= 1.05)
Capacitor Banks: 900 kVA banks located at 20%, 40%, 60% and 80% of the feeder length.

Regulation Reference Point (when regulation is enabled): DG voltage (secondary)

Scenario 1- Feeder load independent of DG penetration

At light load there is an over-voltage problem for almost all locations of the DG and at low penetration factors. Thresholds of concern are: 20% for DG at the feeder end and middle, and 30% for DG distributed uniformly. Only for DG located at the beginning of the feeder is there no overvoltage situation. The overvoltages occur right before the SVR. For DG at the end, there is also a substantial overvoltage at the feeder end. Regulation by the DG eliminates the problem when the DG is located at the end and is distributed, but regulation does not eliminate overvoltage for DG located at the middle. This is because, for DG at the middle, the DG location is right after the SVR where the overvoltage has already been corrected. Thus, the DG voltage regulator does not observe the overvoltage condition experienced elsewhere.

For heavy load, there is no significant problem, other than a slight overvoltage at high penetration (100%) when the DG is at the end of the feeder.

Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

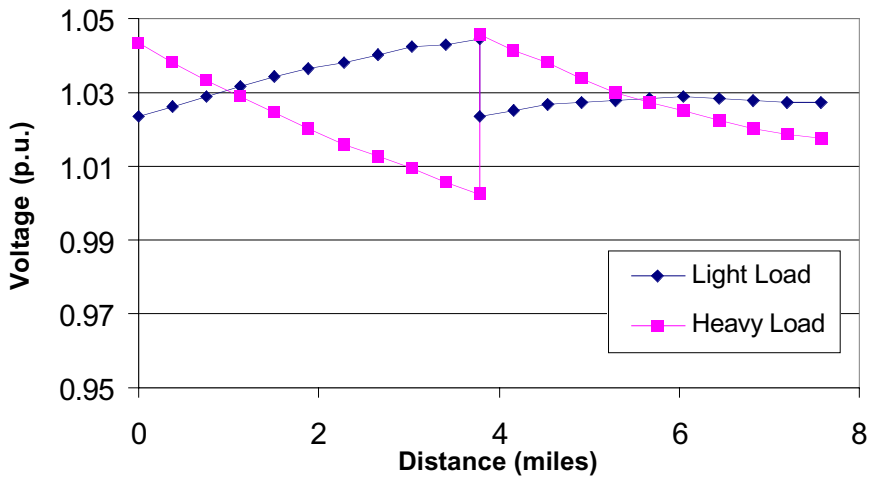
For the light load case, overvoltages also occur in this scenario, but their severity is somewhat reduced by the additional load present. The threshold penetrations where voltage regulation problems begin are somewhat higher (30% for end and middle and 50% for distributed, no problem for DG at the beginning). For this case, DG voltage regulation eliminates the overvoltage for all situations. The reason that the regulation is effective in this scenario is because the voltage at the DG location is more than 1.0 p.u. (which is the DG voltage regulaor setpoint assumed in this study), which will cause the DG to absorb reactive power. In contrast, the voltage at the DG location in Scenario 1 is less than 1.0 p.u., the DG s reactive output acts to oppose the system goal of reducing the voltage.

At heavy load, there is undervoltage problem for every location of the DG. When the DG is located at the end, middle or it is distributed, undervoltage occurs only for very high penetration factors (threshold of concern are between 50% and 100%). Only for DG

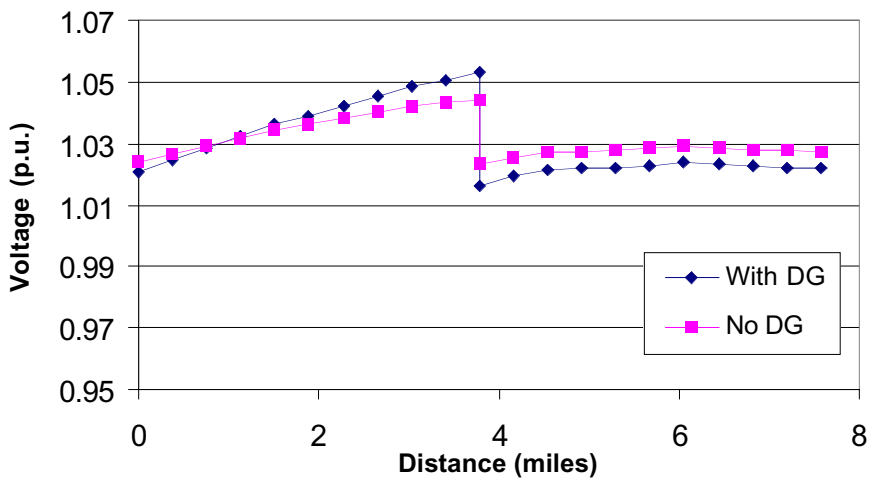
located at the beginning of the feeder is the penetration threshold lower (30%). The undervoltage occurs due to the excessive drops across the feeder starting from the substation, due to the incremental load needed to be supplied. As expected, the worst situation is when the DG is at the beginning since the current in the feeder is the largest, increasing the drops. Regulation by the DG increases the undervoltage problem.

CASE 3.2

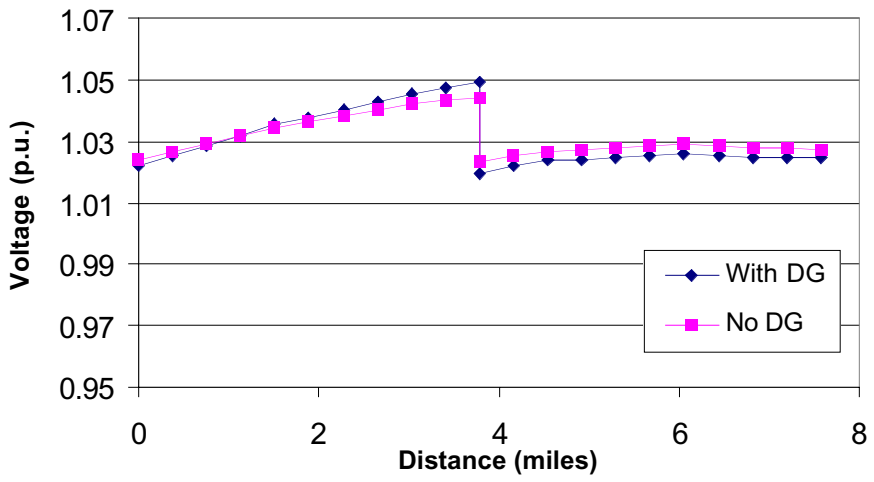
Base Case (No DG)



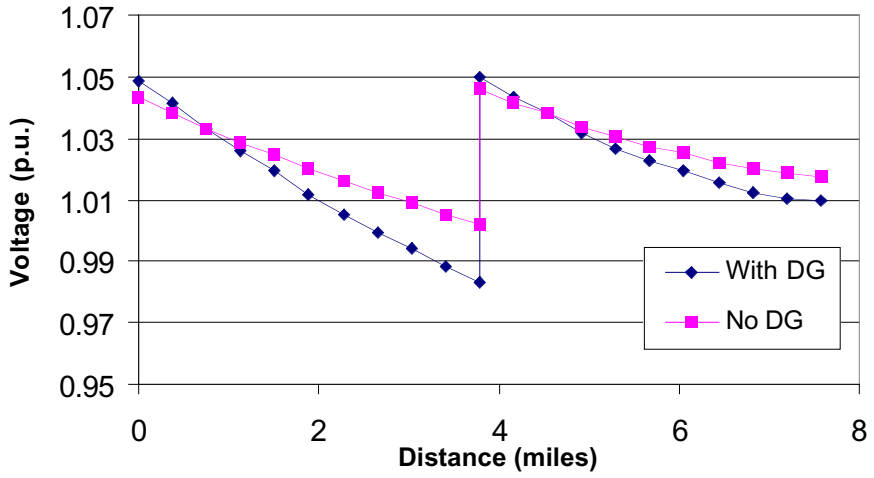
Light Load, No Offset, DG at the Middle (30% Penetration)



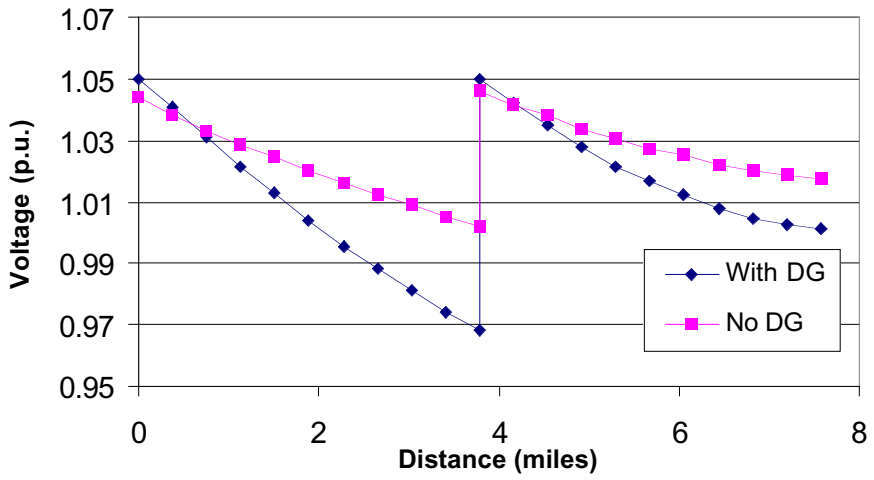
Light Load, No Offset, Regulation, DG at the Middle (30% Penetration)



Heavy Load, Offset Increase, No regulation, DG at the Beginning (30% Penetration)



Heavy Load, Offset Increase, No regulation, DG at the Beginning (50% Penetration)



CASE 3.3

Description of the Feeder

Feeder Length: 8 miles
LTC: Tap setting = 1.03, Resistive LDC =0.25, Reactive LDC = 0.5 (Max =1.05)
SVR: Tap setting = 1.03, Resistive LDC =0.6, Reactive LDC = 1.1 (Max= 1.05)
Capacitor Banks: 900 kVA banks located at 20%, 40%, 60% and 80% of the feeder length.

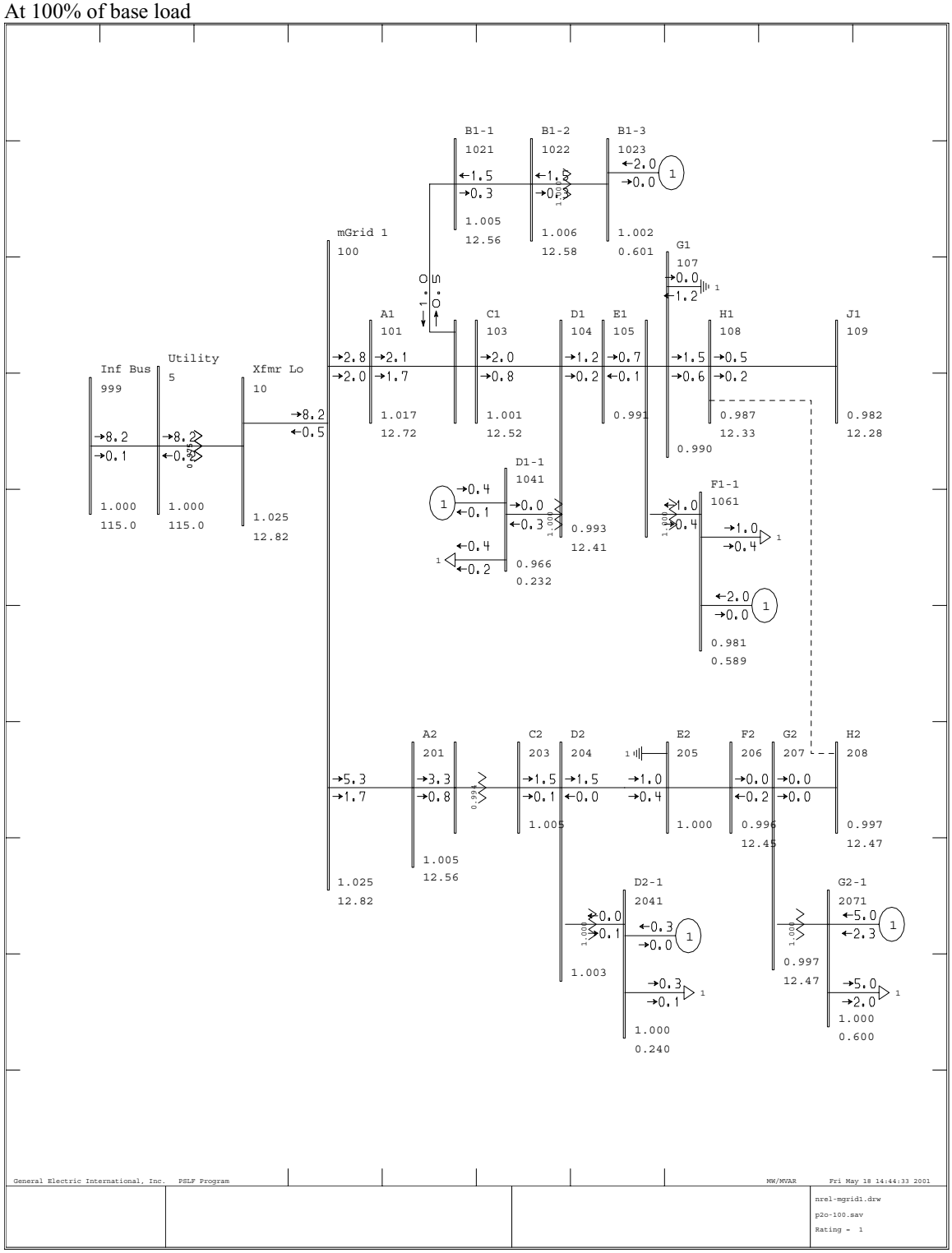
Regulation Reference Point (when regulation is enabled): Bus Voltage (primary)

Scenario 1- Feeder load independent of DG penetration
This case differs from Case 3.2 in that the DG voltage regulation seeks to regulate the primary voltage at the DG location instead of the secondary voltage. The results for this scenario are very similar for those of Case 3.2.

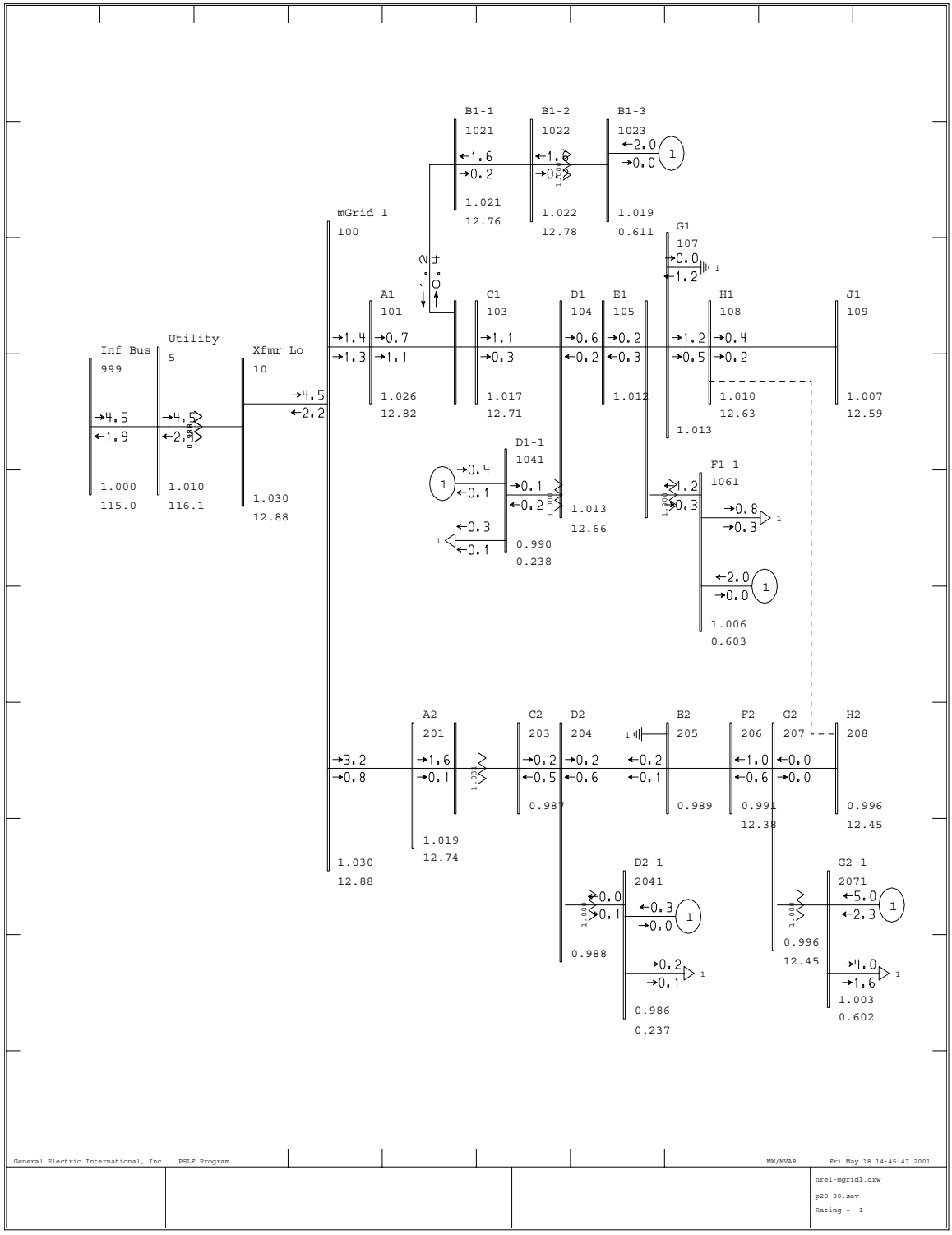
Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity
The voltage at the primary side of the distribution transformer is usually larger than the per-unit voltage at the secondary (DG) side for this situation. The voltage difference, however, is small - usually half a percent, so the regulation performance is very similar. For the light load case, similar to Case 3.2 where the secondary (DG) voltage was regulated, the overvoltage is eliminated. Regulation of the primary side for the heavy load case does not remedy the undervoltage problem and can actually aggravate the problem.

Appendix C.
P2 Case Study Voltage Profiles

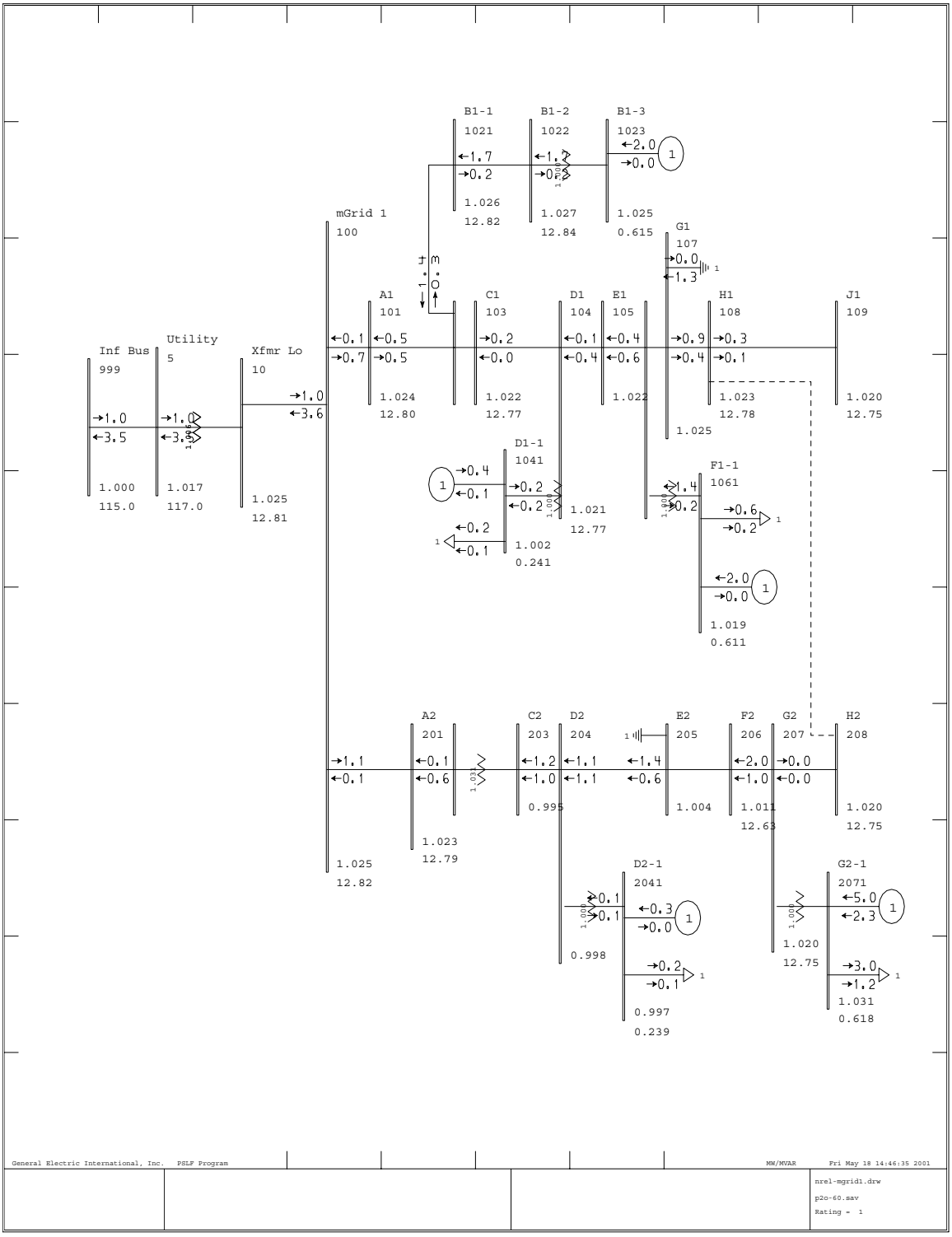
One-line Diagram Showing Voltages, Active and Reactive Flows
At 100% of base load



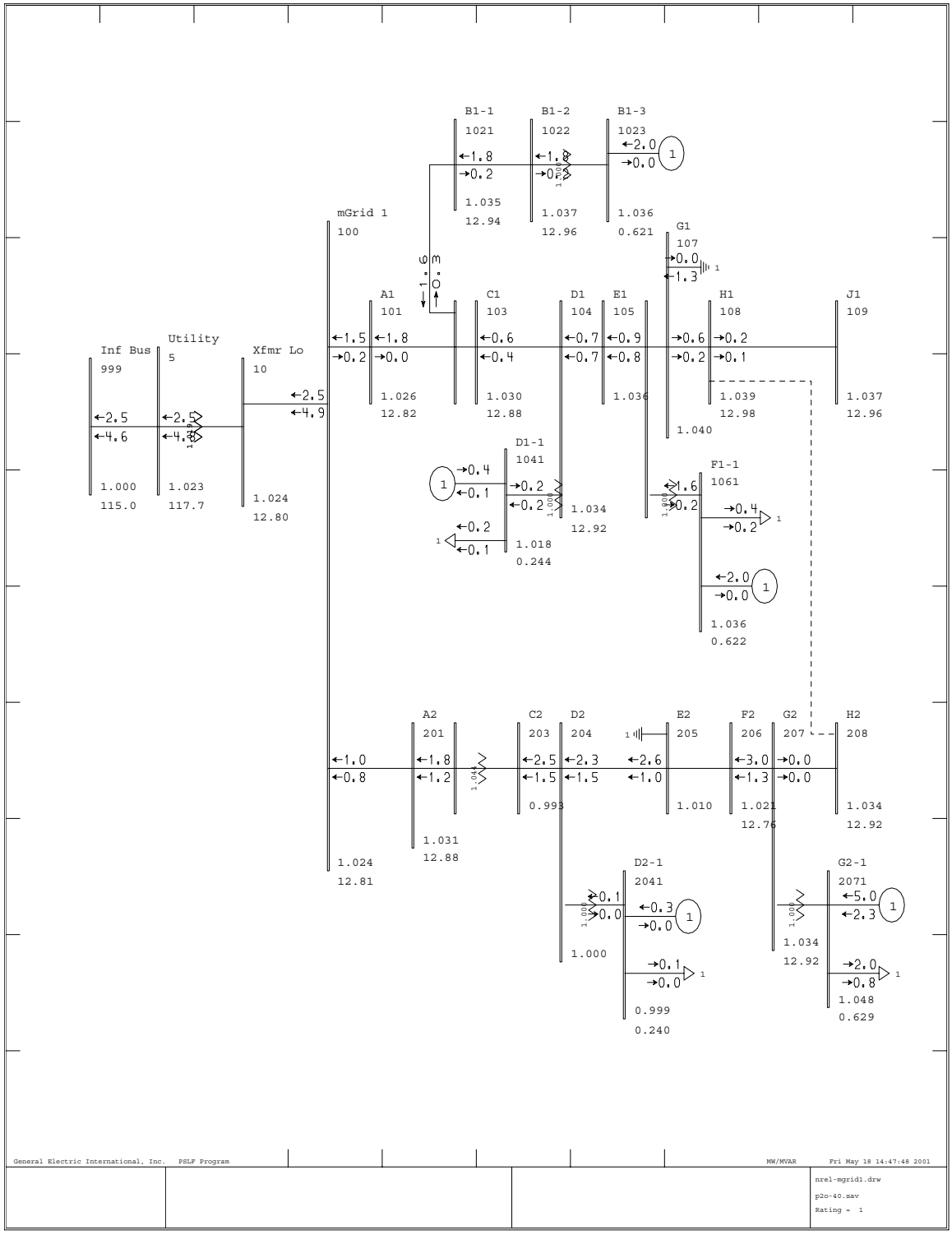
One-line Diagram Showing Voltages, Active and Reactive Flows
At 80% of base load



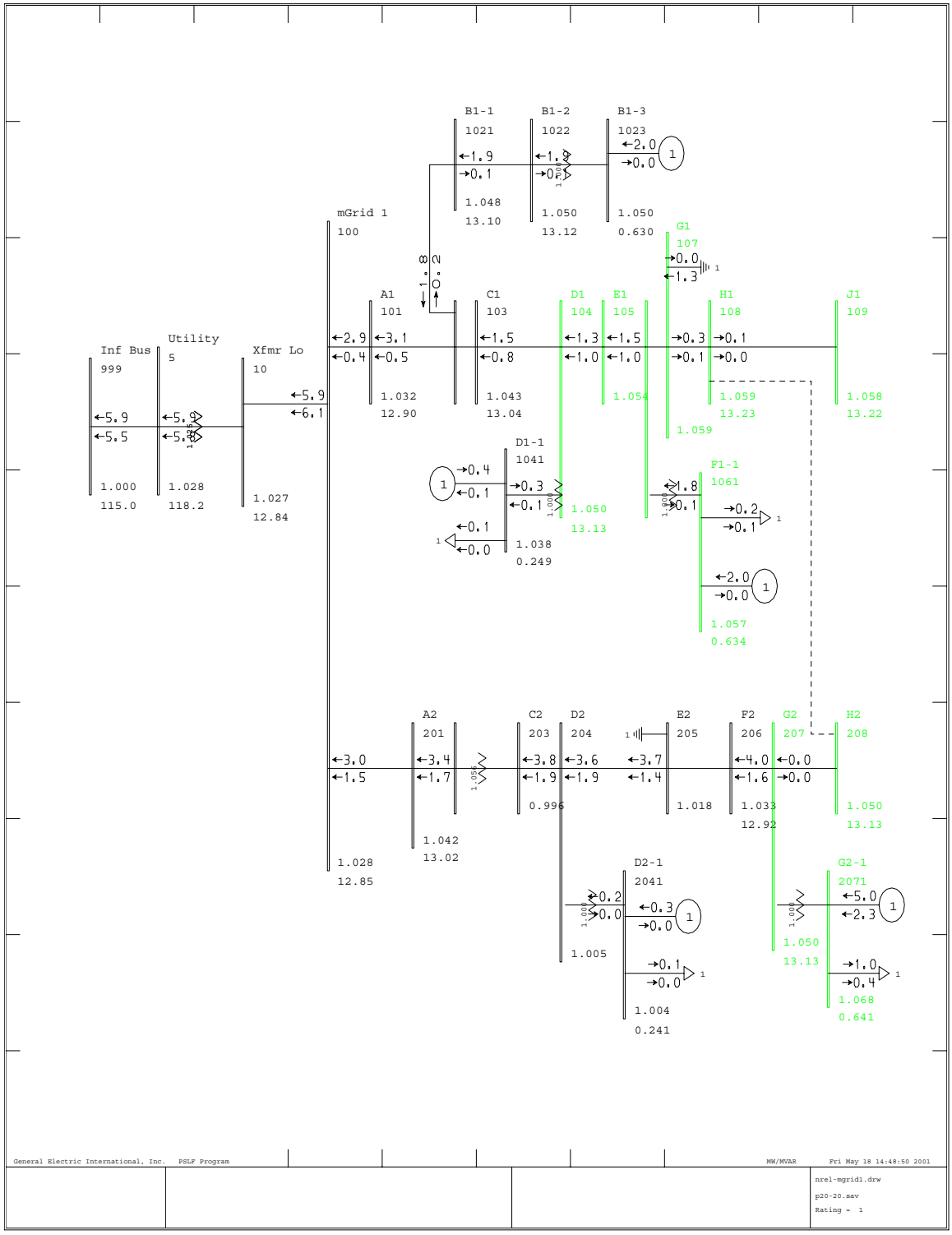
One-line Diagram Showing Voltages, Active and Reactive Flows
At 60% of base load



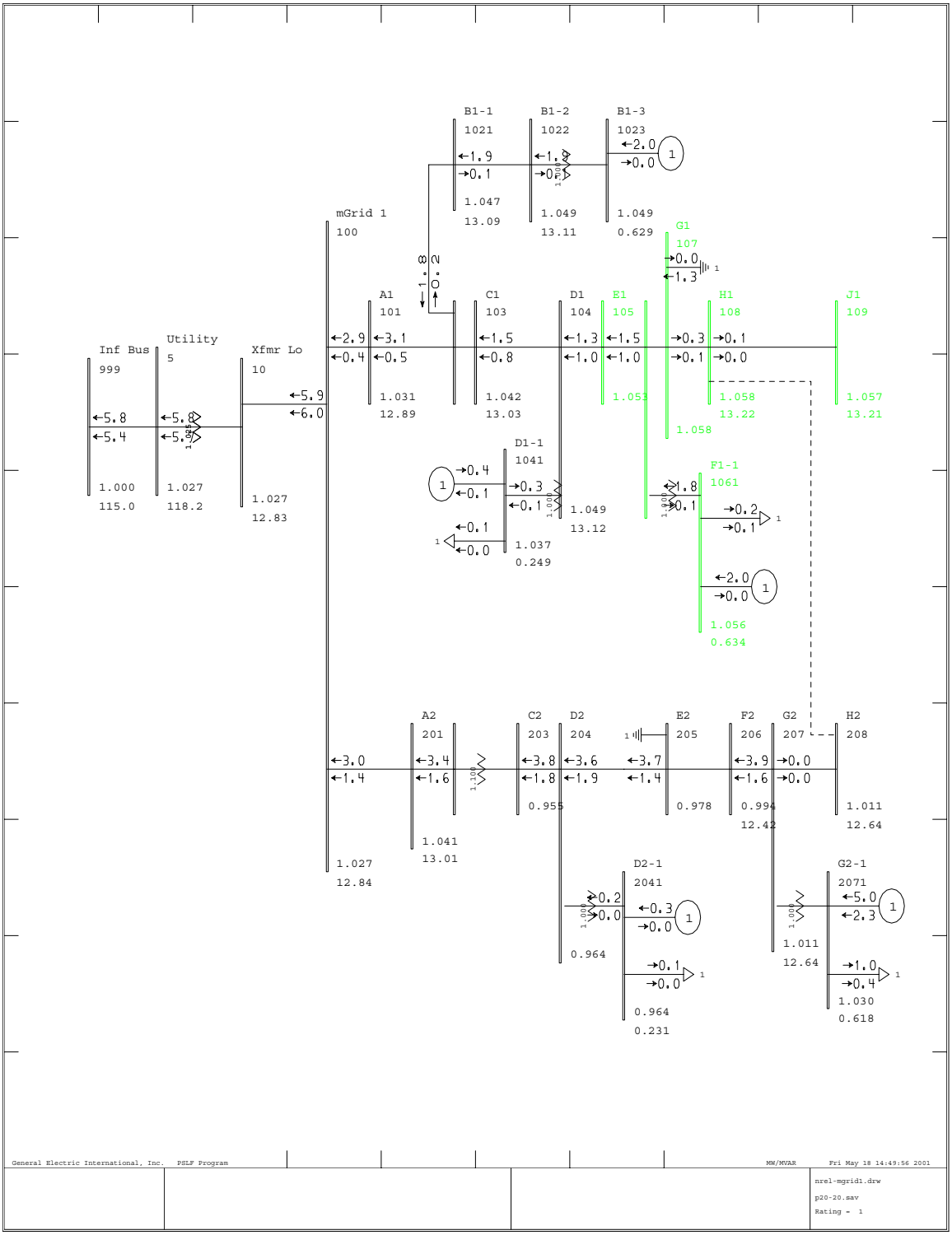
One-line Diagram Showing Voltages, Active and Reactive Flows
At 40% of base load



One-line Diagram Showing Voltages, Active and Reactive Flows
At 20% of base load



One-line Diagram Showing Voltages, Active and Reactive Flows
At 20% of base load
With SVR control reversal due feeder active flow reversal



Appendix D. Flicker

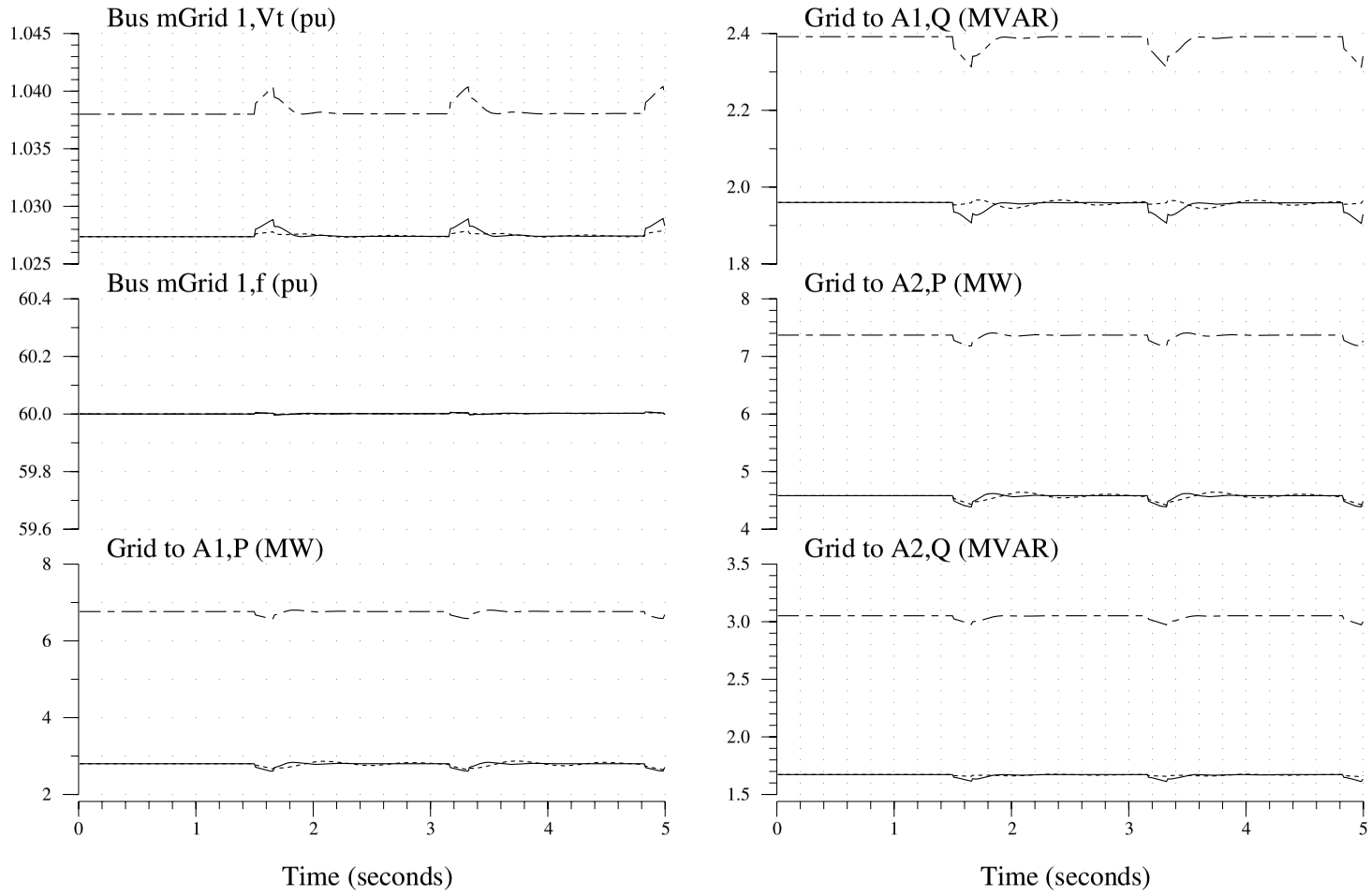
SEPARATOR 1: P2 SYSTEM LOAD-INDUCED FLICKER CASE.

3 Traces: No DGs; with Inverter type DGs; with Rotating type DGs
Without Voltage Control

Flicker: Load fluctuations.Without Voltage control

System Quantities

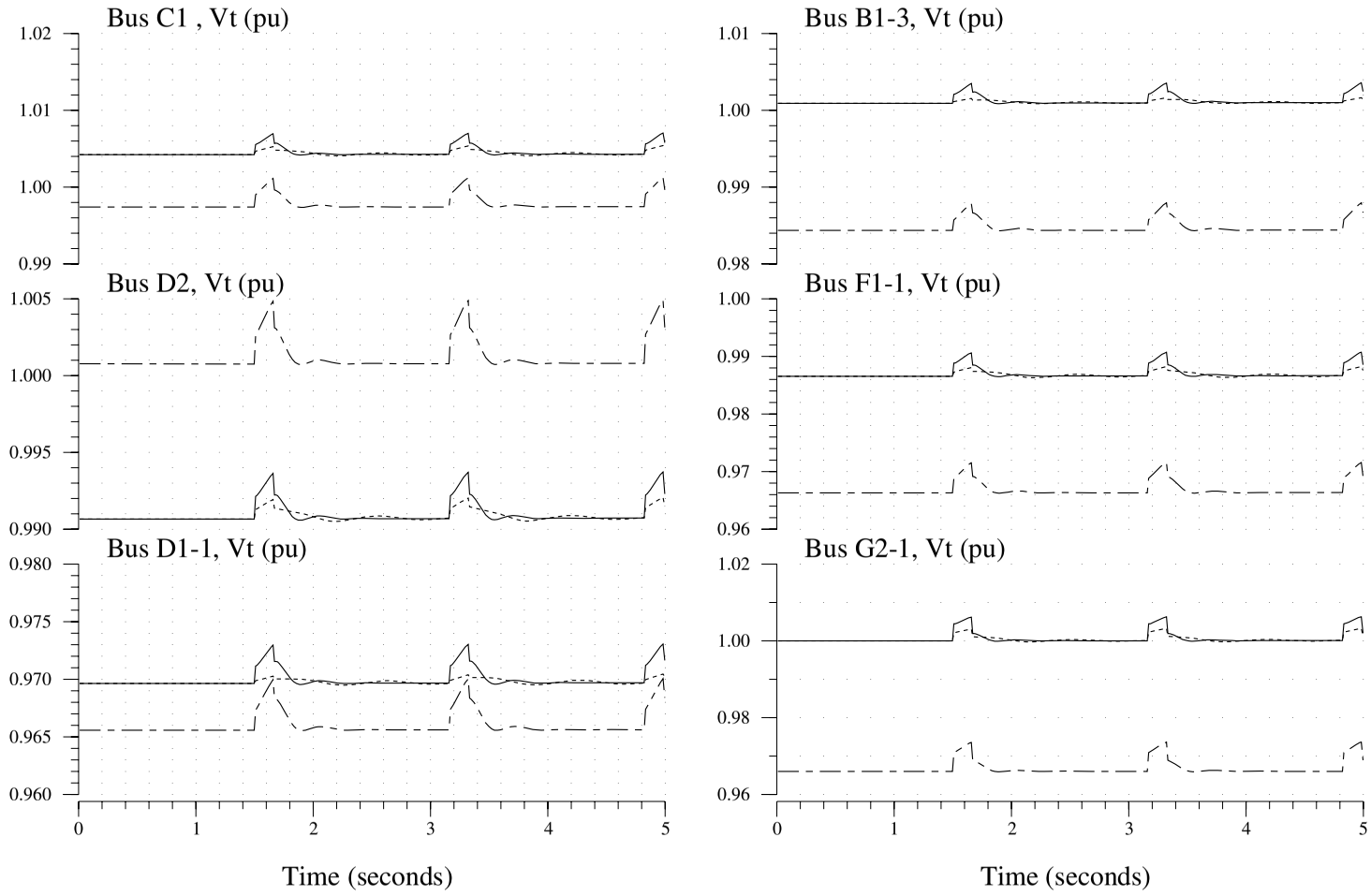
inverter type DG (____), rotating DG (_ _ _), no DG (__ _ __)



Flicker: Load fluctuations.Without Voltage control

DG Voltages

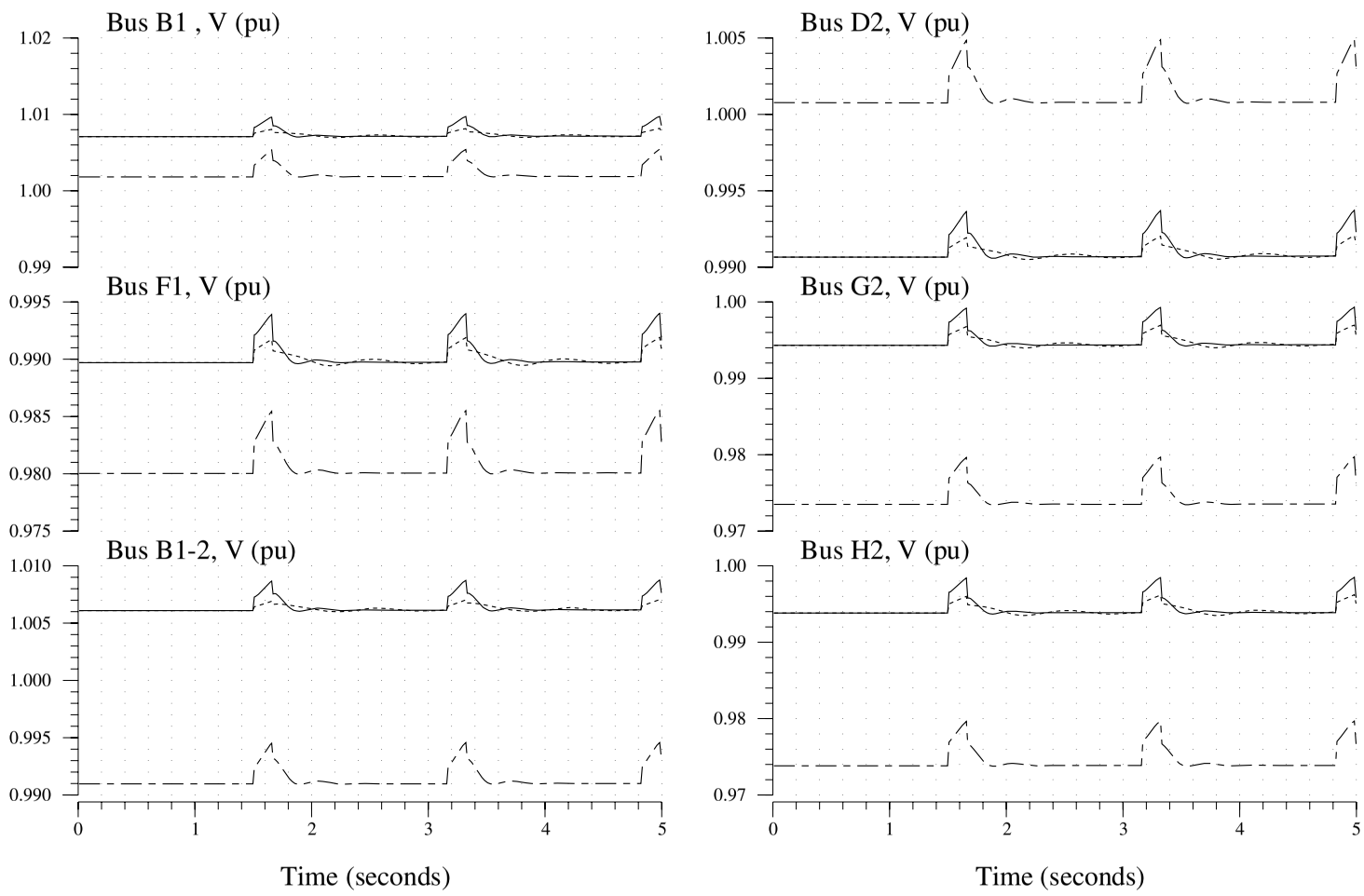
inverter type DG (____), rotating DG (_ _ _), no DG (__ _ __)



Flicker: Load fluctuations.Without Voltage control

Voltages

inverter type DG (____), rotating DG (_ _ _), no DG (__ _ __)



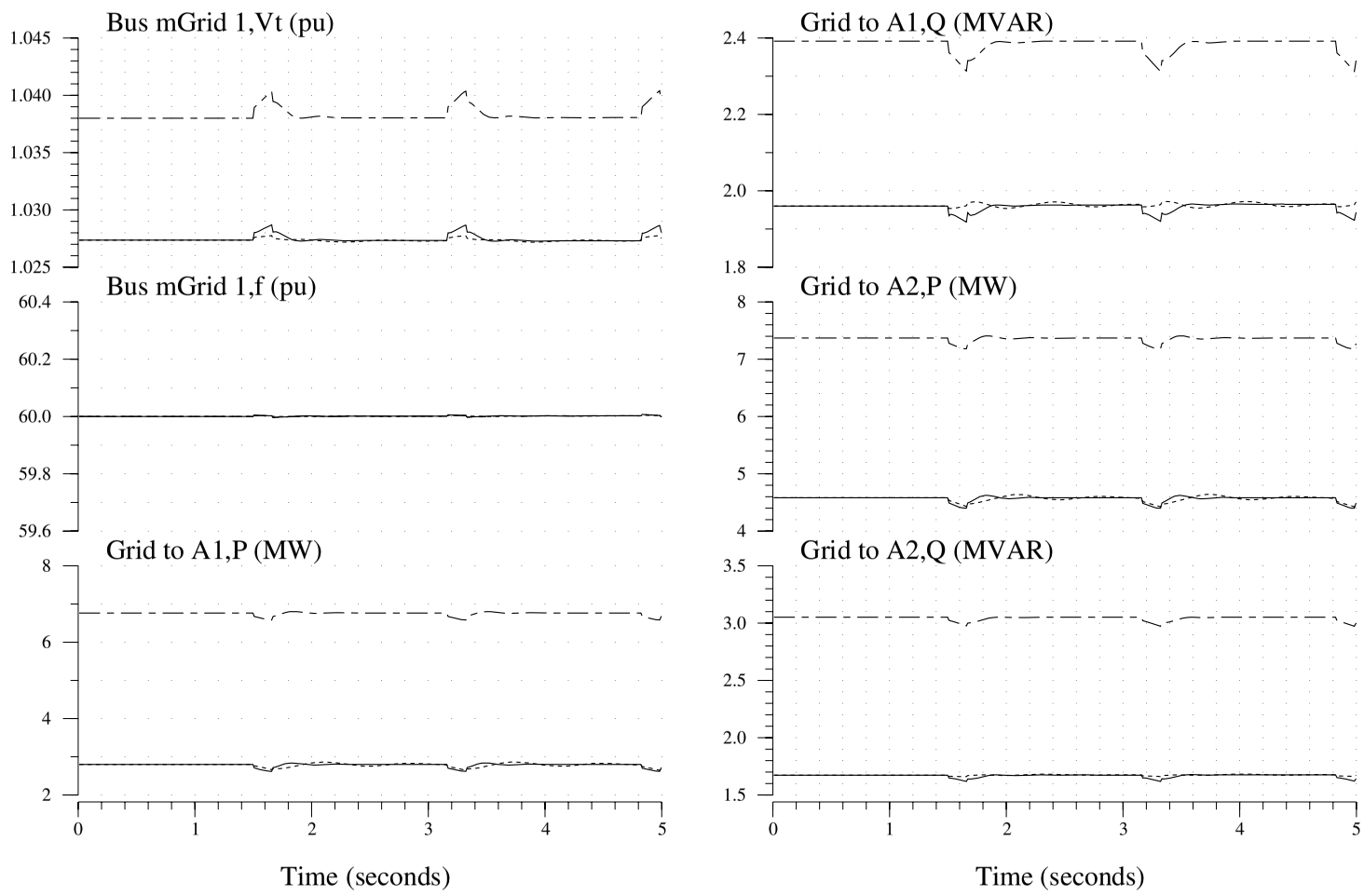
SEPARATOR 2: P2 SYSTEM LOAD-INDUCED FLICKER CASE.

3 Traces: No DGs; with Inverter type DGs; with Rotating type DGs
With Voltage Control

Flicker: Load fluctuations.Voltage control

System Quantities

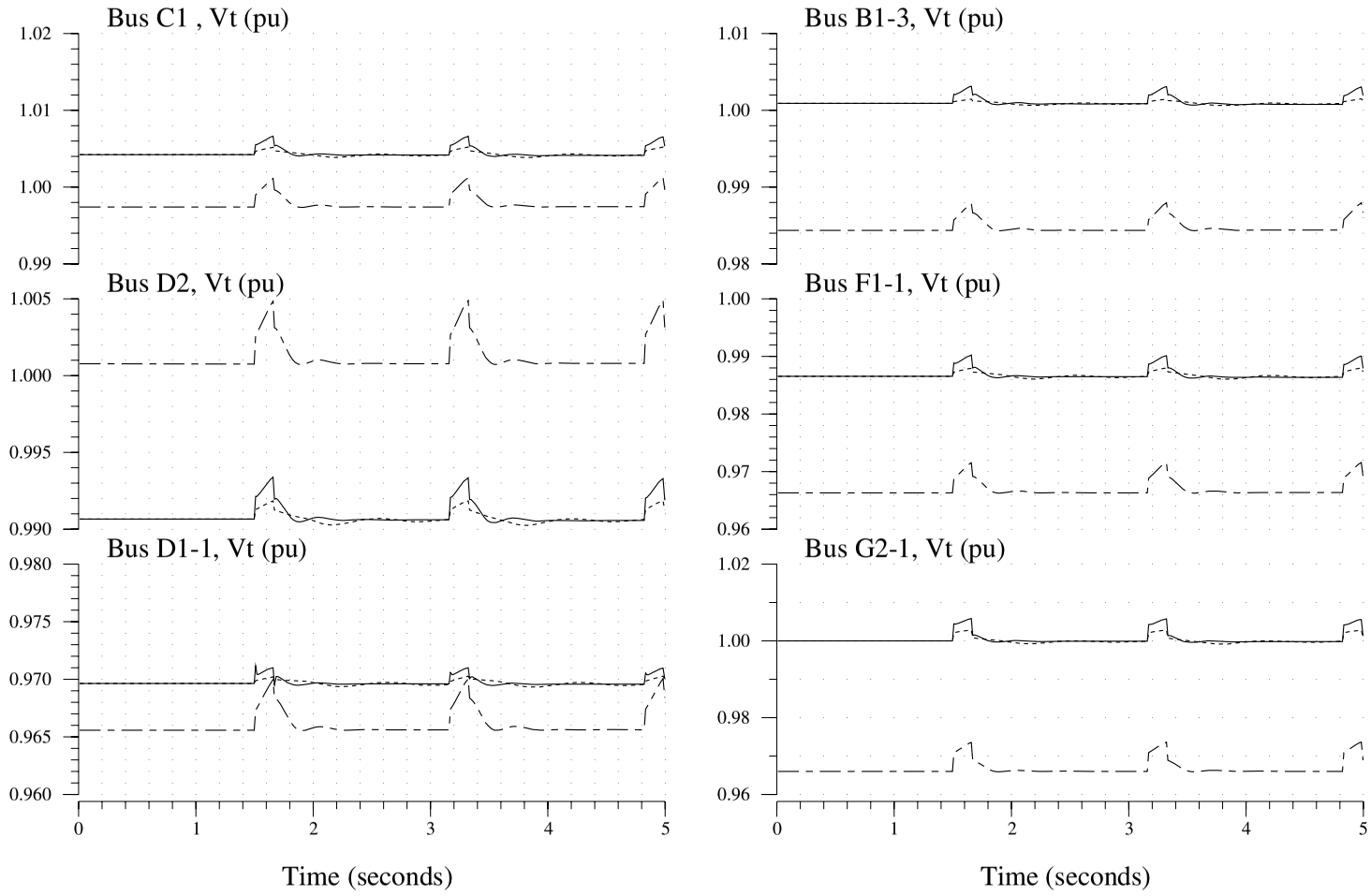
inverter type DG (____), rotating DG (_ _ _), no DG (__ _ __)



Flicker: Load fluctuations.Voltage control

DG Voltages

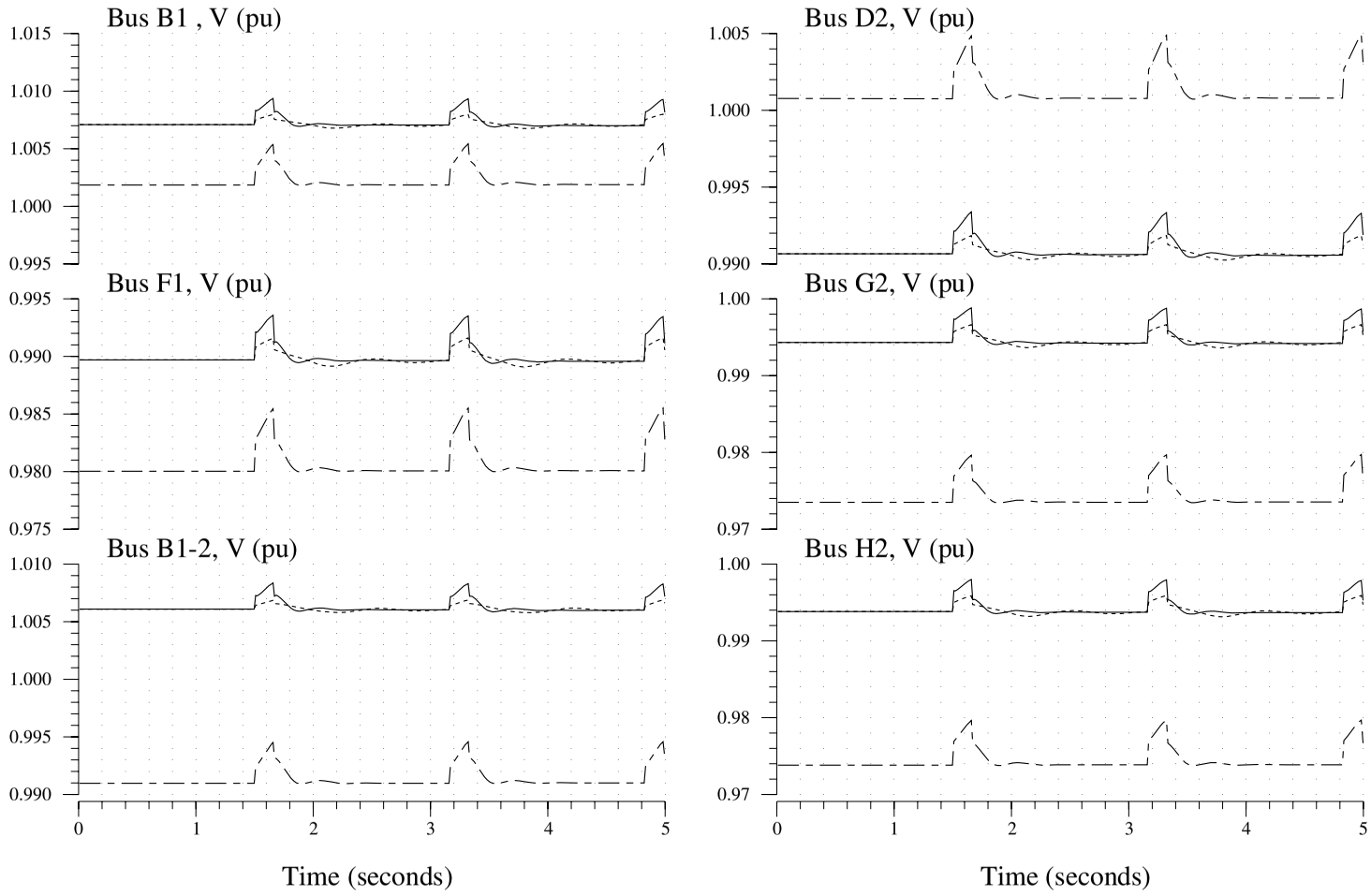
inverter type DG (____), rotating DG (_ _ _), no DG (__ _ __)



Flicker: Load fluctuations.Voltage control

Voltages

inverter type DG (____), rotating DG (_ _ _), no DG (__ _ __)



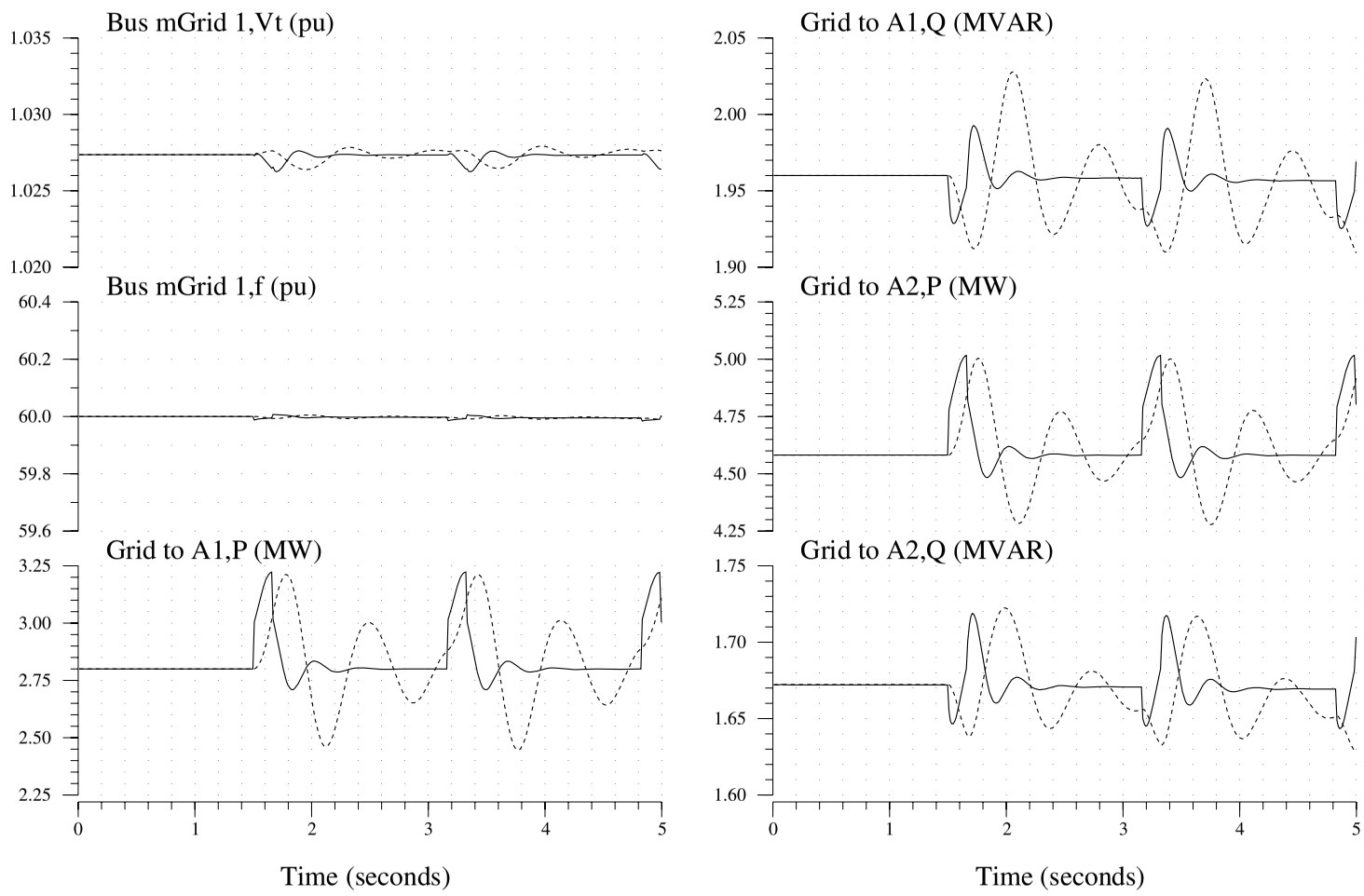
SEPARATOR 3: P2 SYSTEM DG-INDUCED FLICKER CASE.

2 Traces: with Inverter type DGs; with Rotating type DGs
Without Voltage Control

Flicker: Prime mover fluctuations.Without Voltage control

System Quantities

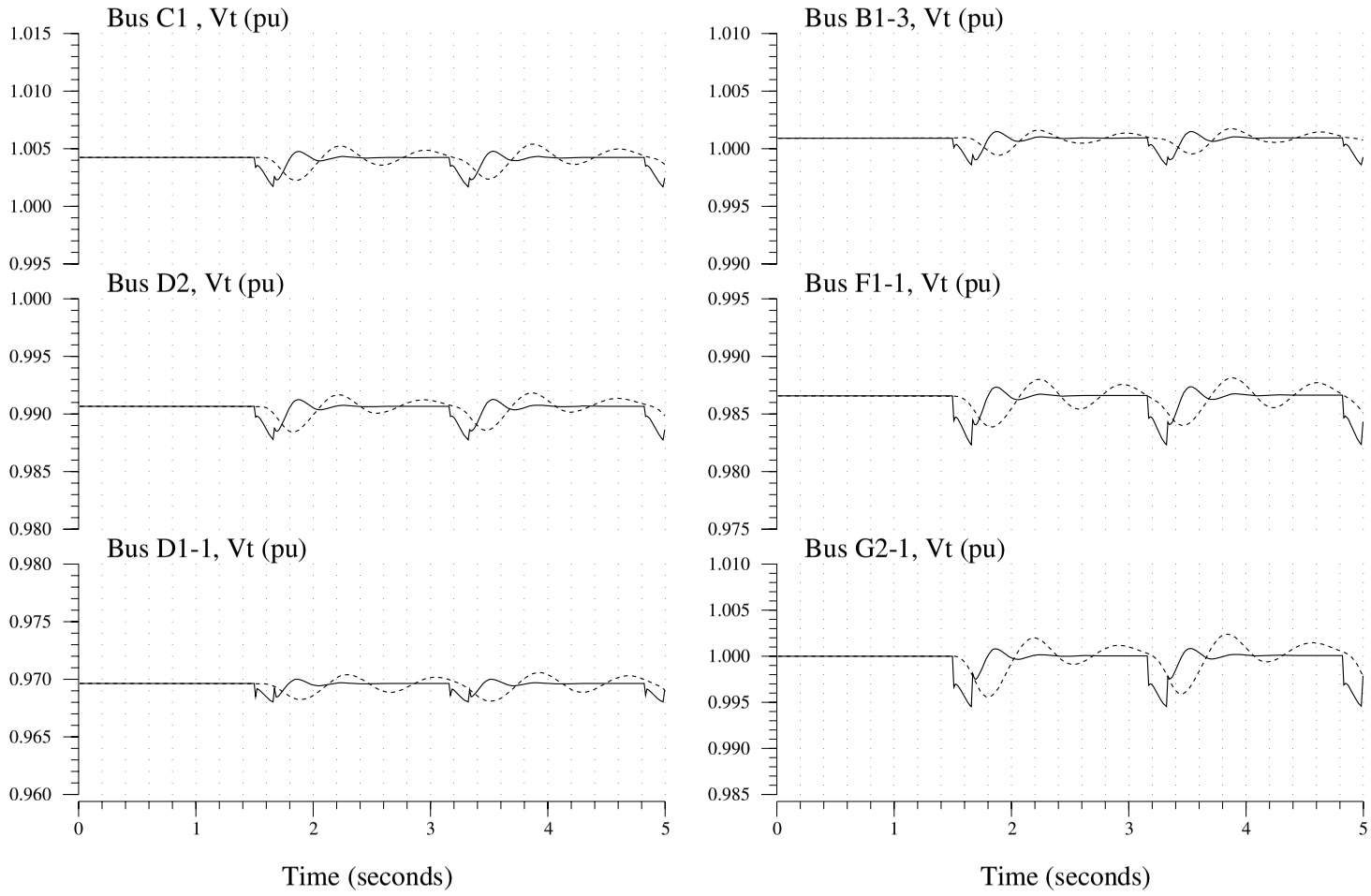
inverter type DG (____), rotating DG (_ _ _)



Flicker: Prime mover fluctuations.Without Voltage control

DG Voltages

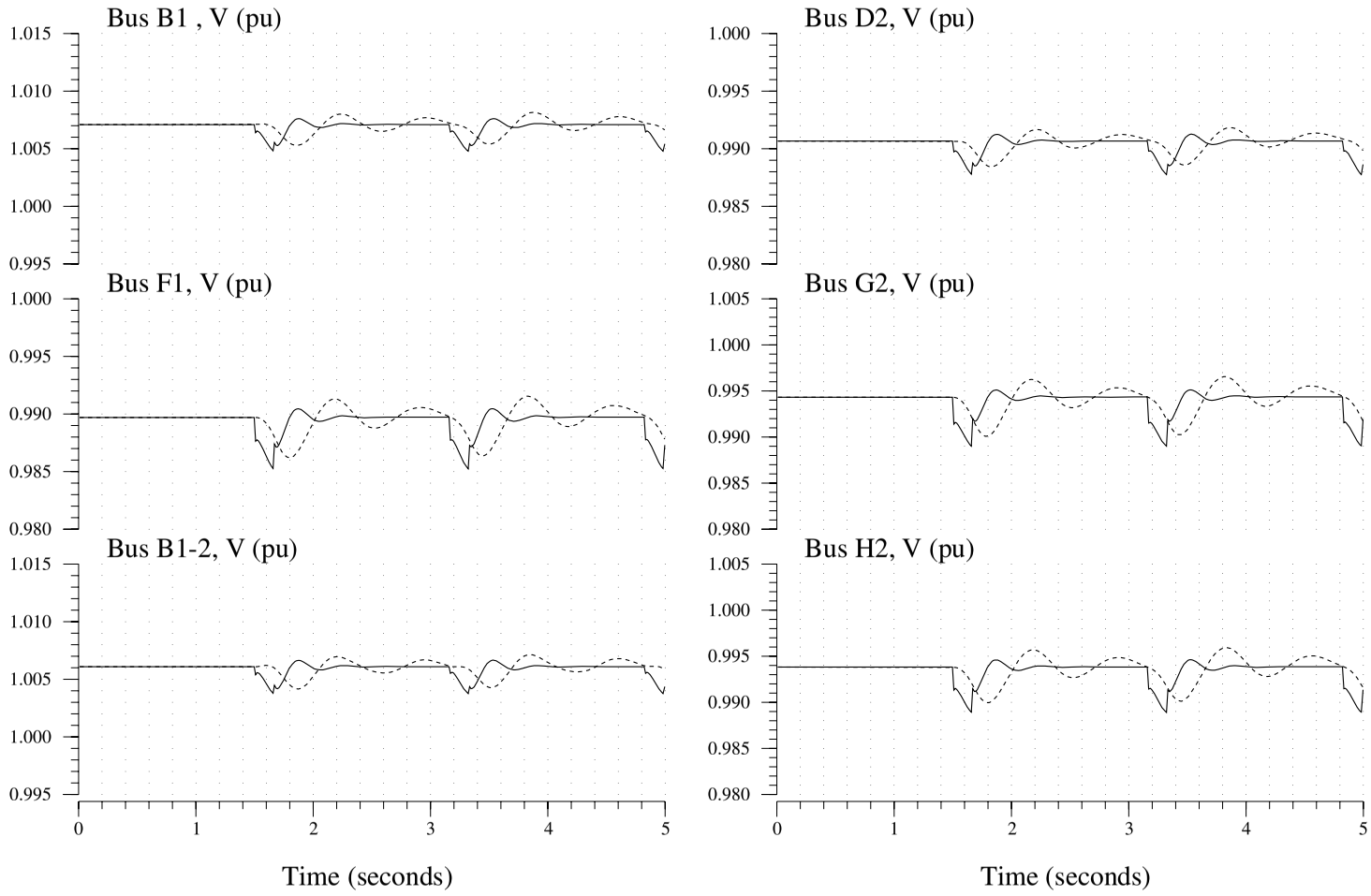
inverter type DG (____), rotating DG (_ _ _)



Flicker: Prime mover fluctuations.Without Voltage control

Voltages

inverter type DG (____), rotating DG (_ _ _)



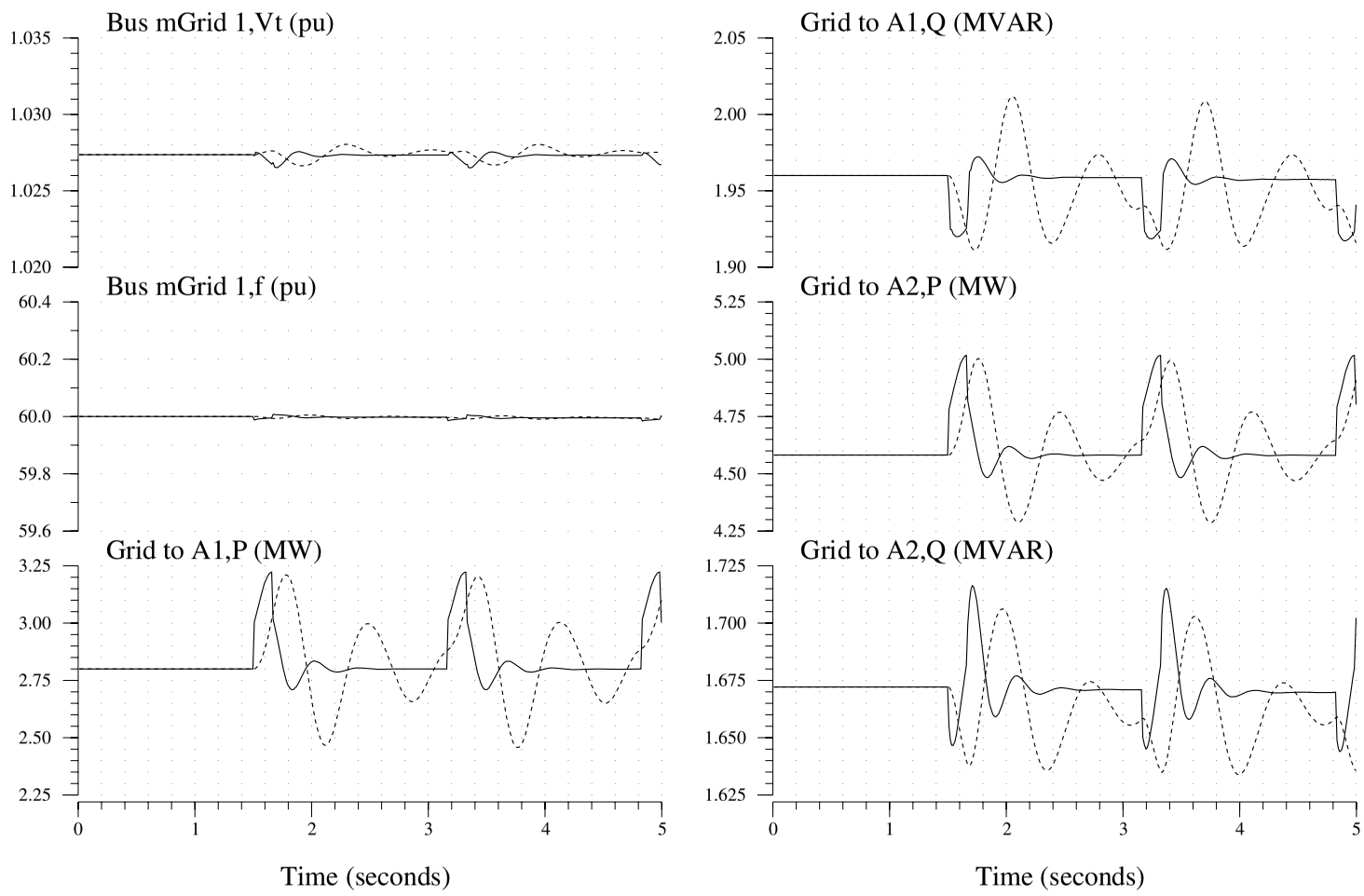
SEPARATOR 4: P2 SYSTEM DG-INDUCED FLICKER CASE.

2 Traces: with Inverter type DGs; with Rotating type DGs
With Voltage Control

Flicker: Prime mover fluctuations. Voltage control

System Quantities

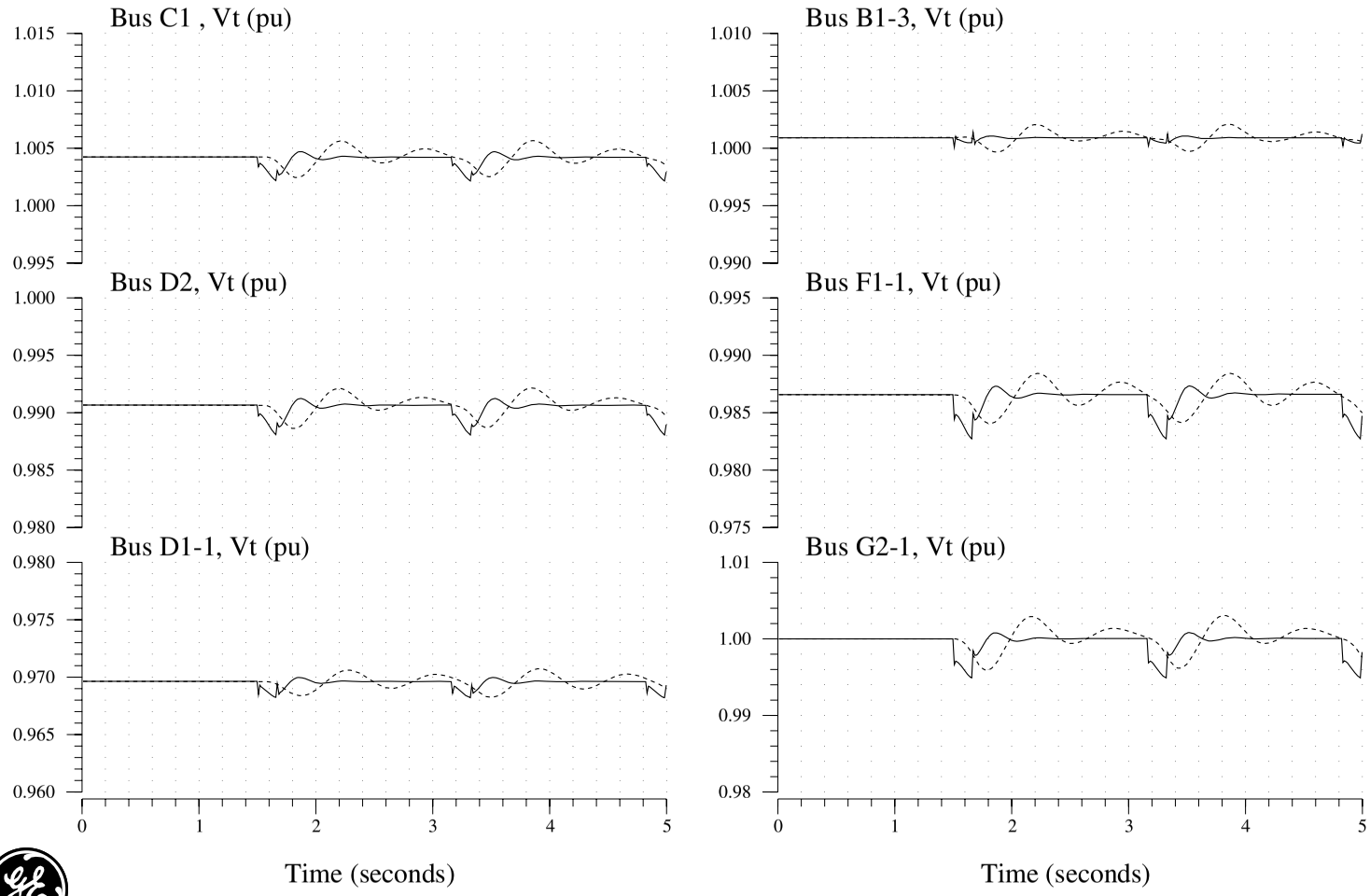
inverter type DG (____), rotating DG (_ _ _)



Flicker: Prime mover fluctuations. Voltage control

DG Voltages

inverter type DG (____), rotating DG (_ _ _)

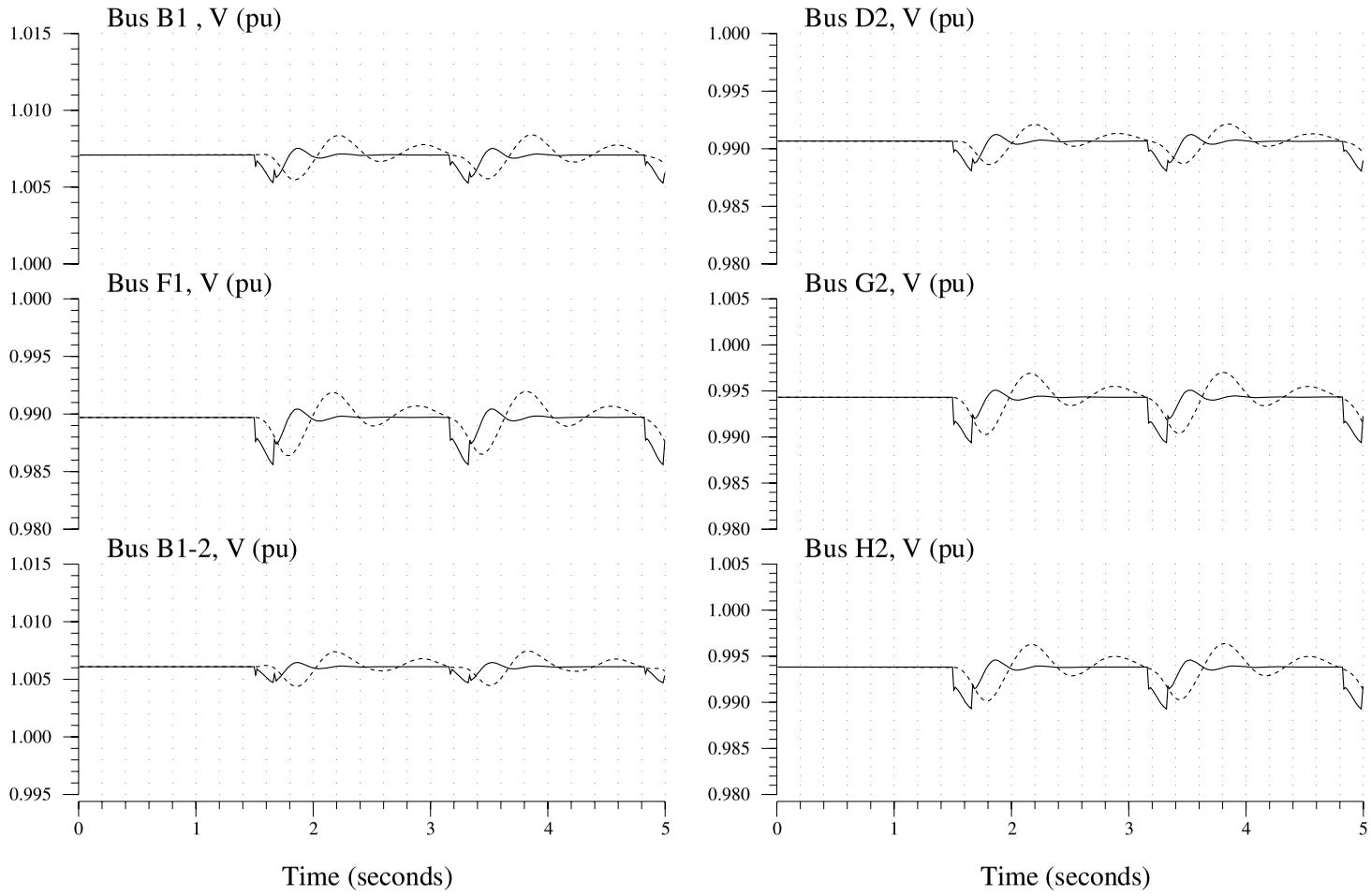


22-JUN-2001 16:54:38 out\psfiles\dgfli-inv-v.chan

Flicker: Prime mover fluctuations. Voltage control

Voltages

inverter type DG (____), rotating DG (_ _ _)



Appendix E.
Sequence Circuit During a Single-Phase Fault

During a single-phase fault, for example, phase A to ground fault, the fault voltage and currents are:

$$V_{A,fault} = 0 \tag{1}$$

$$I_{B,fault} = I_{C,fault} = 0 \tag{2}$$

Convert the equations using symmetrical components, one can obtain:

$$V_{1,A} + V_{2,A} + V_{0,A} = 0 \tag{3}$$

$$a^2 \cdot I_{1,A} + a \cdot I_{1,A} + I_{1,A} = a \cdot I_{1,A} + a^2 \cdot I_{1,A} + I_{1,A} = 0 \tag{4}$$

note that:

$$\begin{bmatrix} F_A \\ F_B \\ F_C \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \cdot \begin{bmatrix} F_1 \\ F_2 \\ F_0 \end{bmatrix}, \tag{5}$$

where: $F_{A,B,C}$ is phase voltage or current, $F_{1,2,0}$ is sequence voltage or current.
From (4), the sequence current relationship can be derived

$$I_{1,A} = I_{2,A} = I_{0,A} \tag{6}$$

Based on (3) and (6), Figure 1 shows the positive-, negative- and zero-sequence equivalent circuit after phase A single-phase fault.

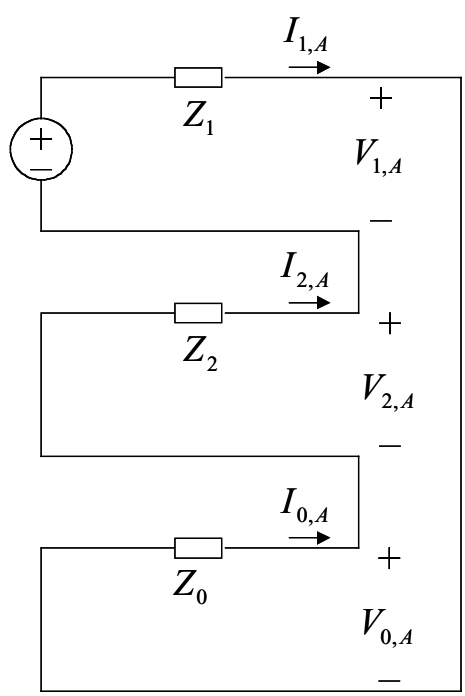


Figure 1 Sequence circuit during a single-phase fault.

Where: Z_1, Z_2, and Z_0 are the overall system positive-, negative- and zero-sequence impedances during the fault.

The sequence voltages $V_{1,A}$, $V_{2,A}$, and $V_{0,A}$ can be calculated based on the circuit in Figure 1.

Then, the unfaulted phase voltages are:

$$V_B = a^2 \cdot V_{1,A} + a \cdot V_{2,A} + V_{0,A}$$

$$V_C = a \cdot V_{1,A} + a^2 \cdot V_{2,A} + V_{0,A}$$

Appendix F.
Local Dynamics

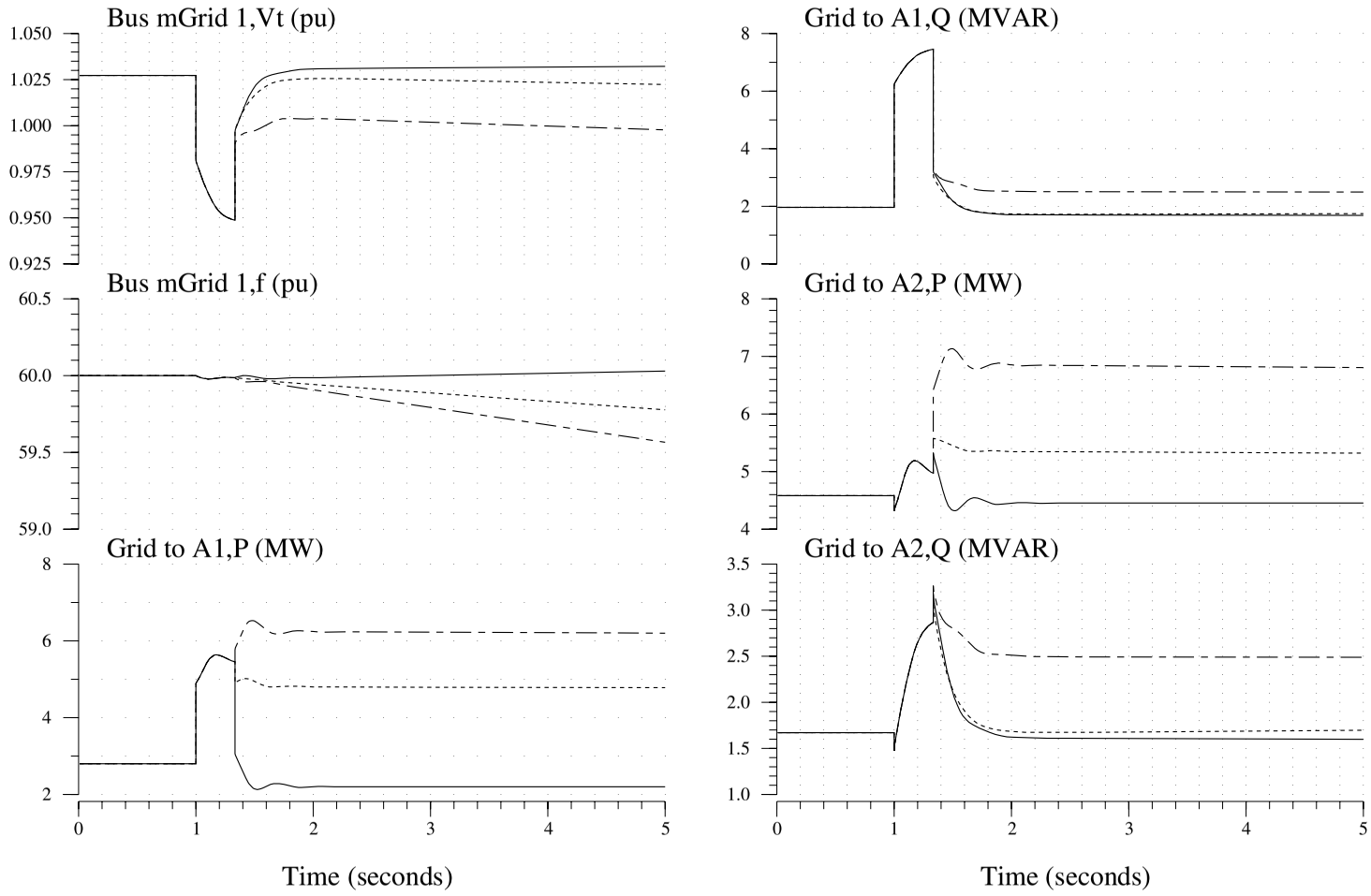
SEPARATOR 1: P2 SYSTEM RESPONSE TO A LATERAL FAULT

All inverter-based DGs with no special controls (constant current control)

System 2: Without Controls

System Quantities

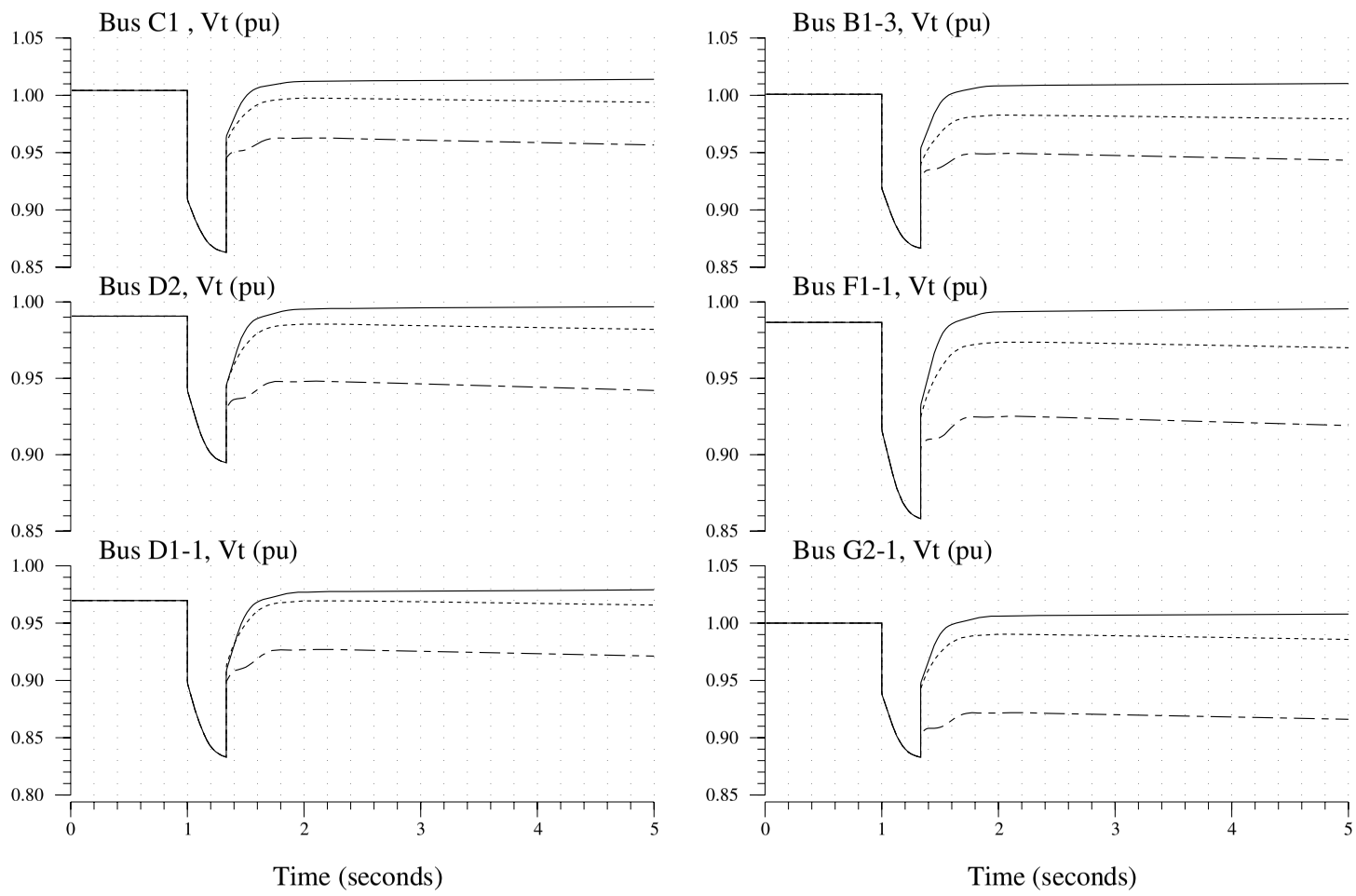
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



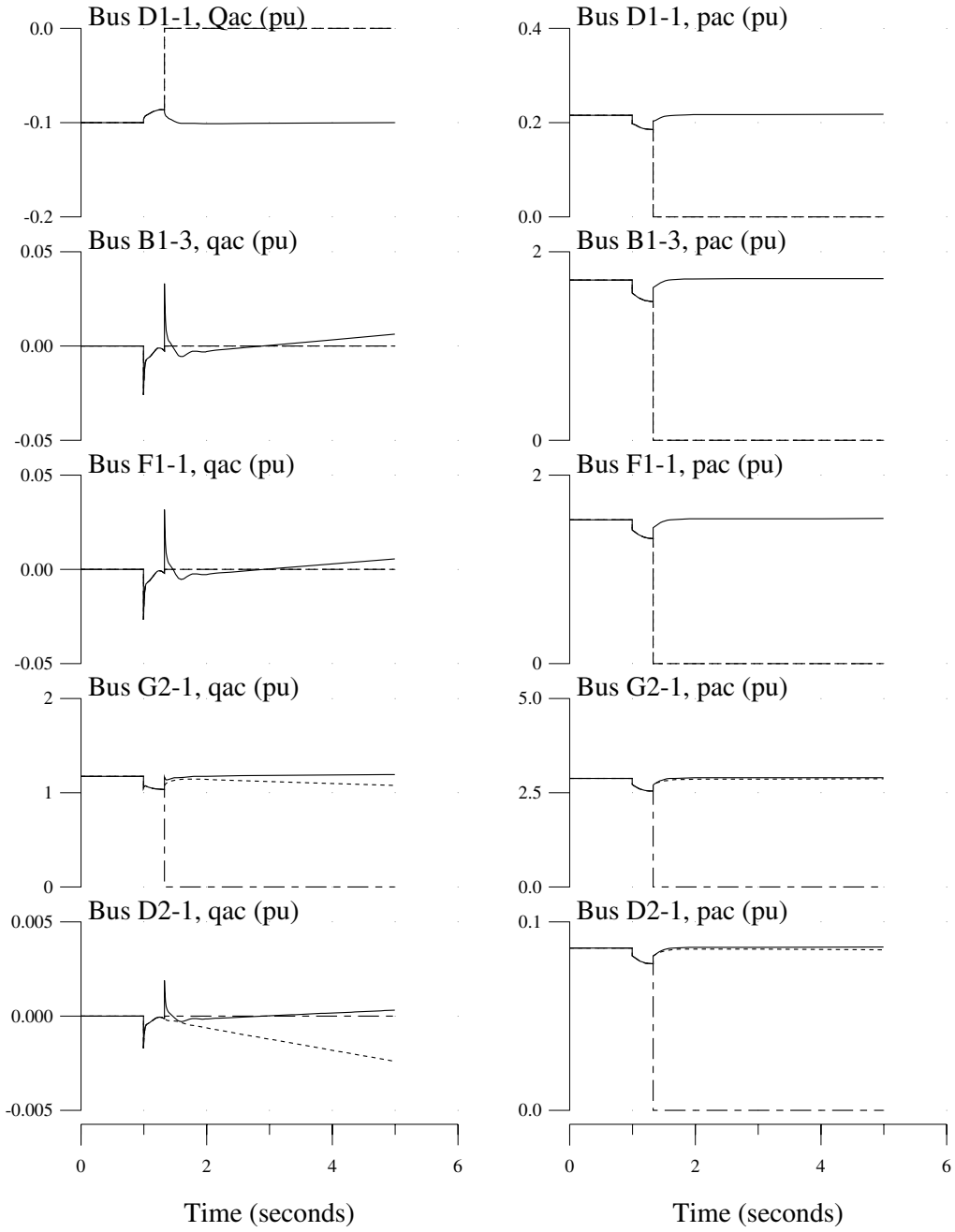
System 2: Without Controls

Voltages

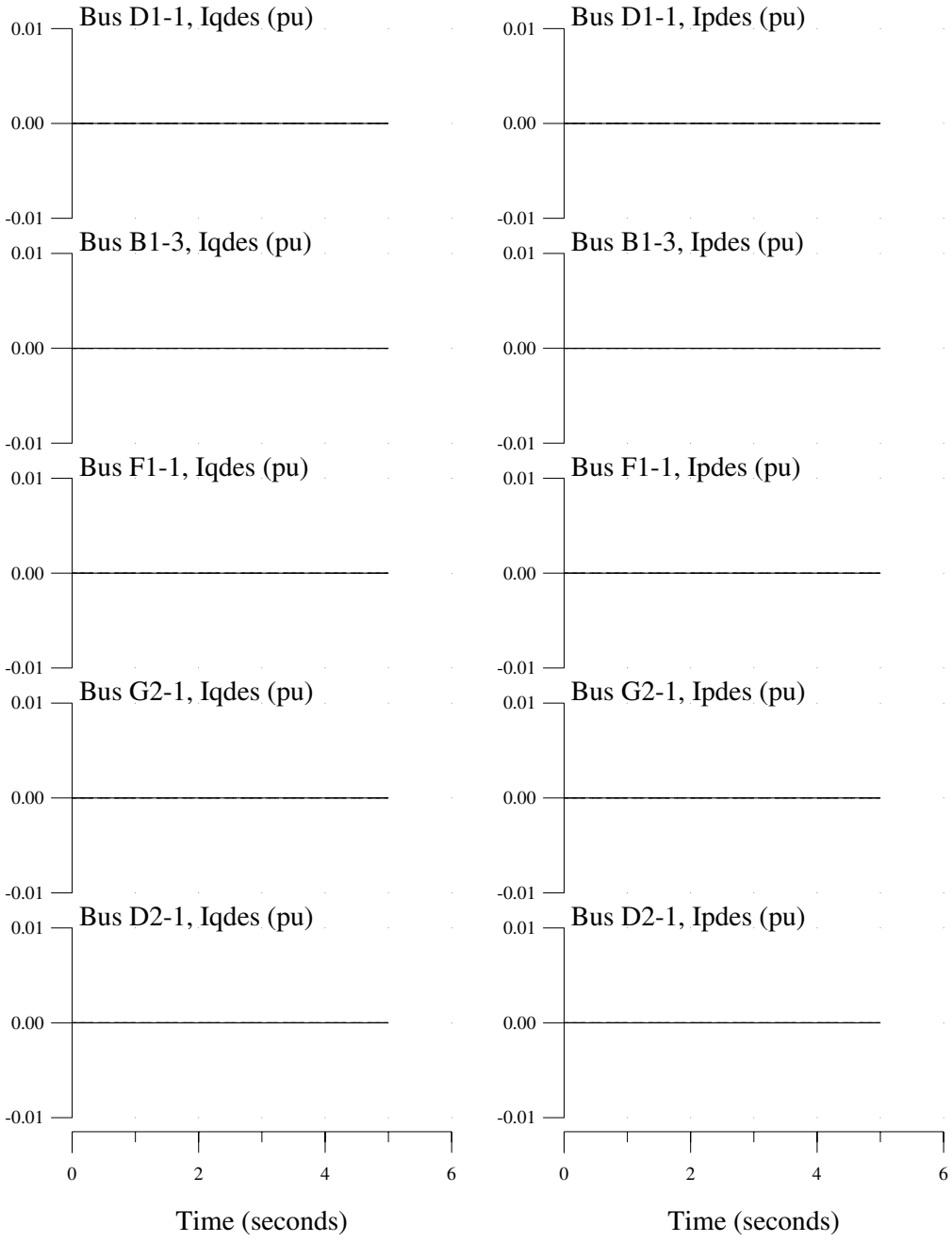
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Without Controls
DG Active and Reactive Power
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Without Controls
DG Control Signals
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



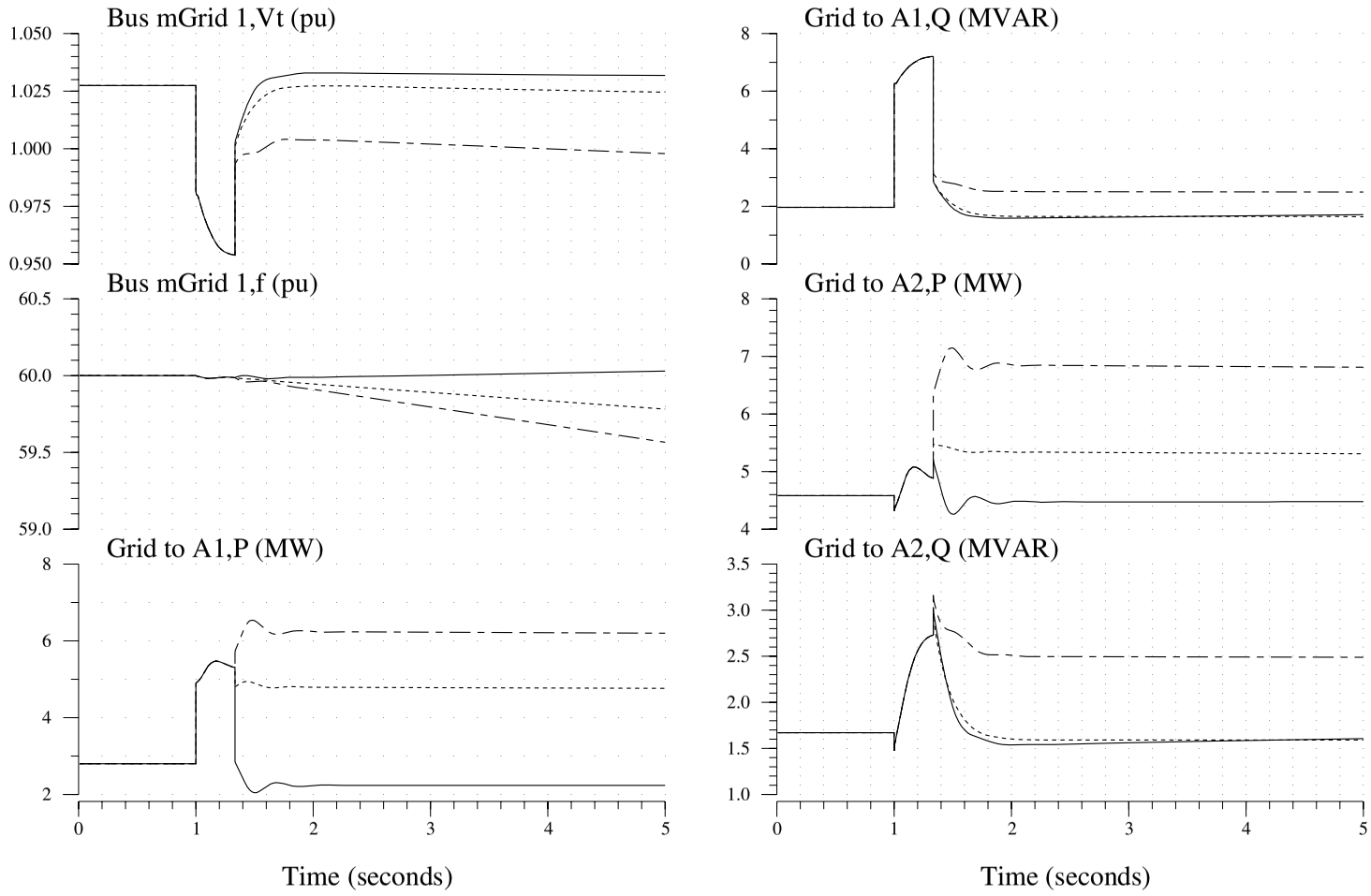
SEPARATOR 2: P2 SYSTEM RESPONSE TO A LATERAL FAULT

All inverter-based DGs with constant power control

System 2: Power Control

System Quantities

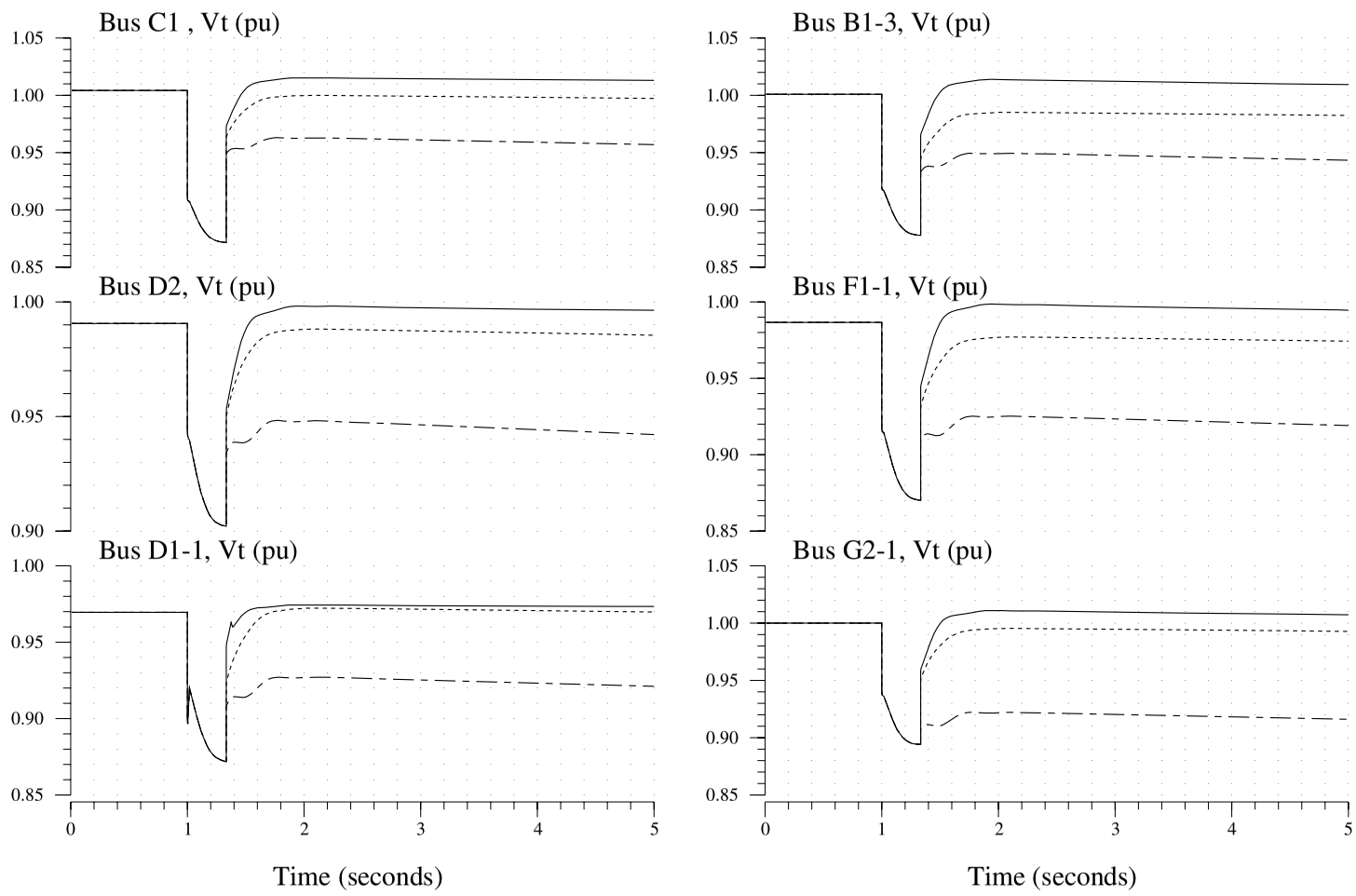
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



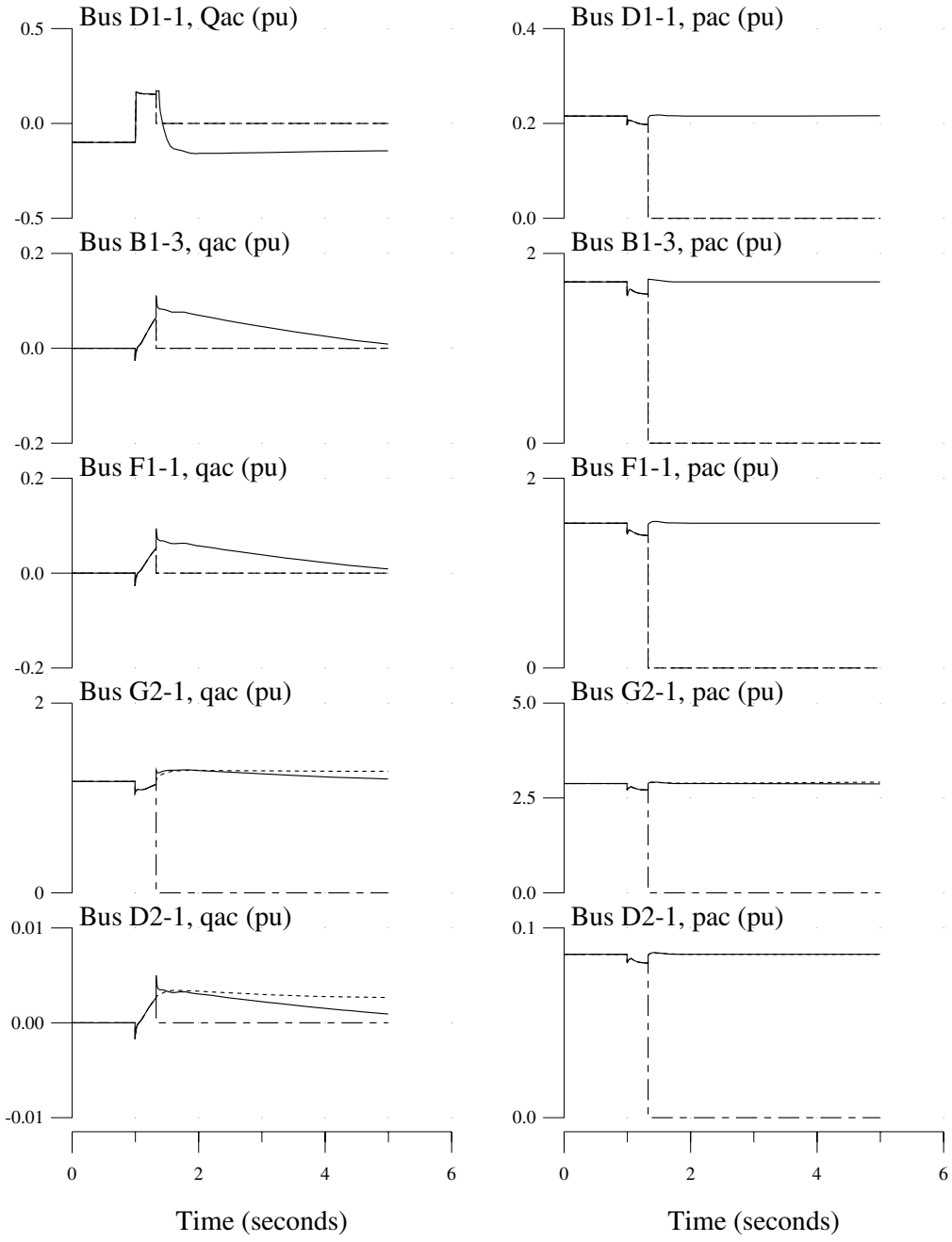
System 2: Power Control

Voltages

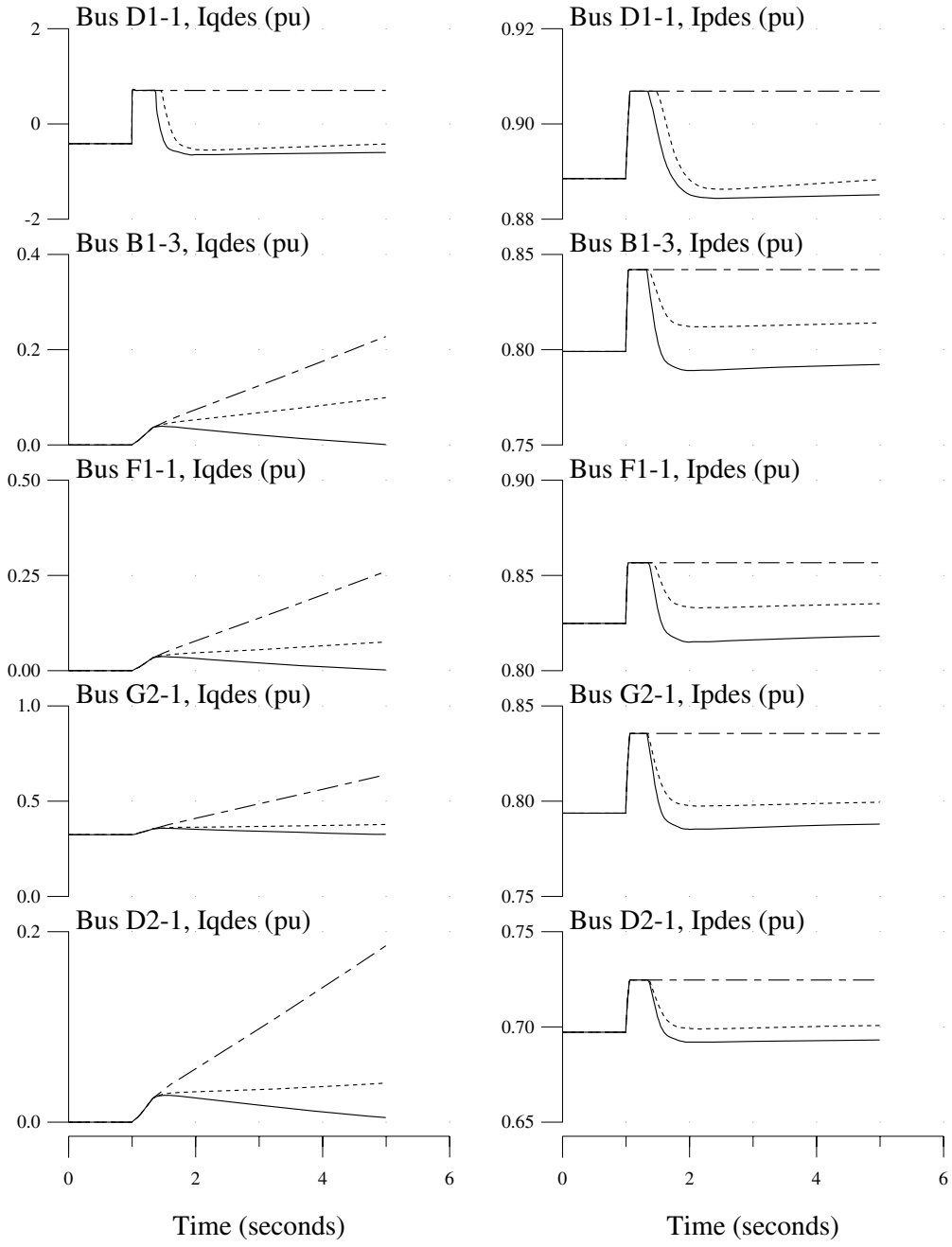
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Power Control
DG Active and Reactive Power
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



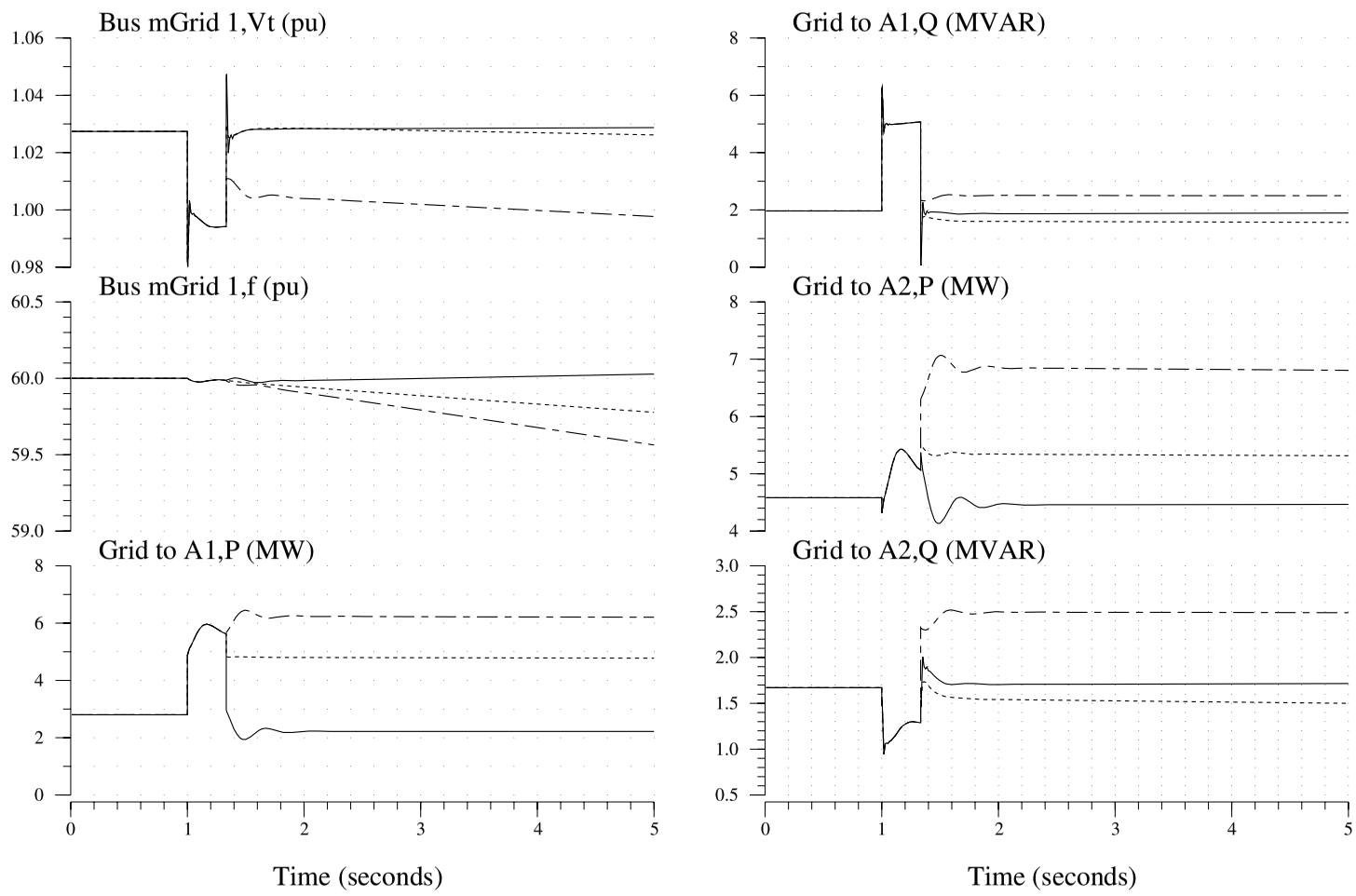
System 2: Power Control
DG Control Signals
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



SEPARATOR 3: P2 SYSTEM RESPONSE TO A LATERAL FAULT

All inverter-based DGs with high gain voltage control

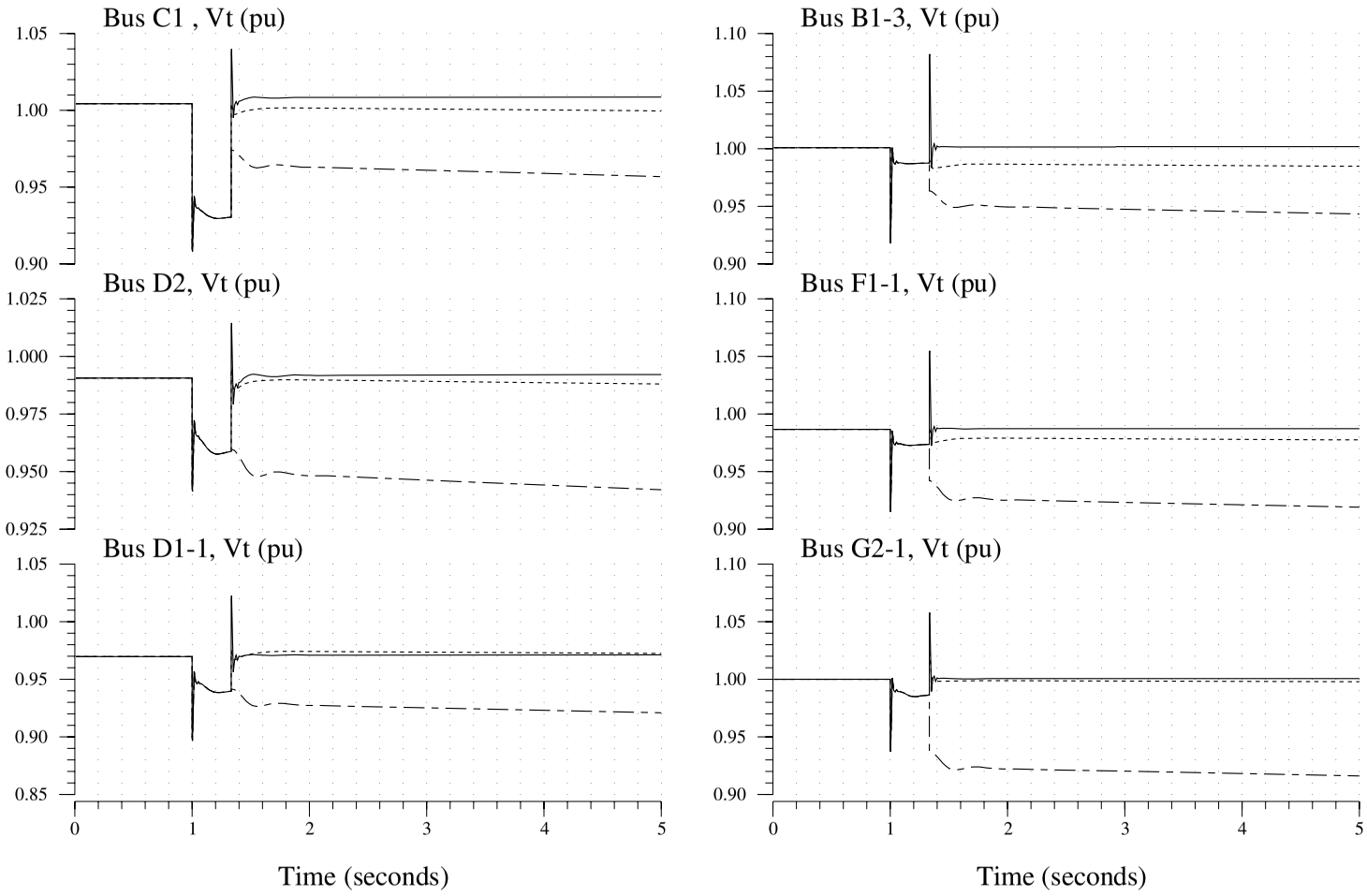
System 2: Voltage Control
System Quantities
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



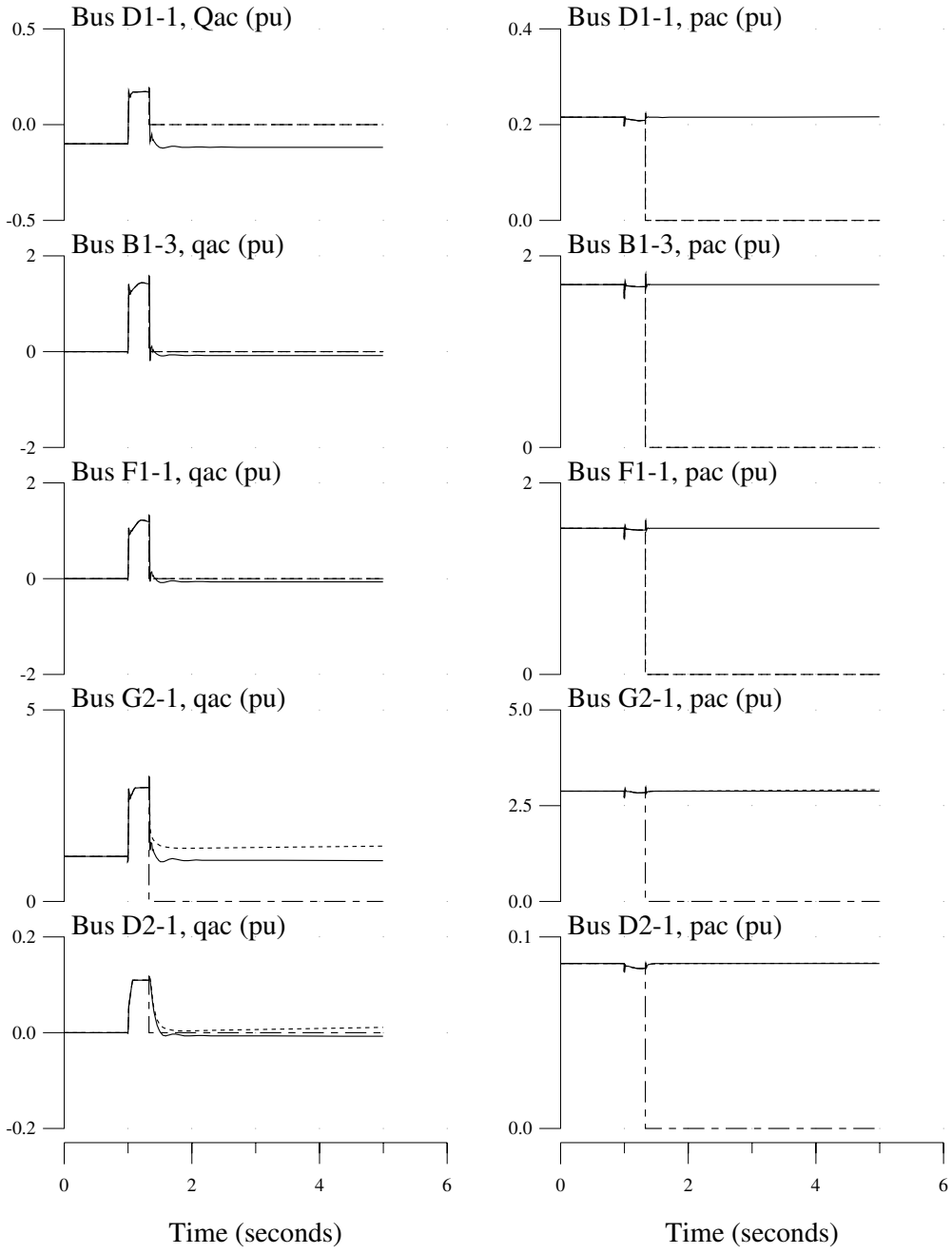
System 2: Voltage Control

Voltages

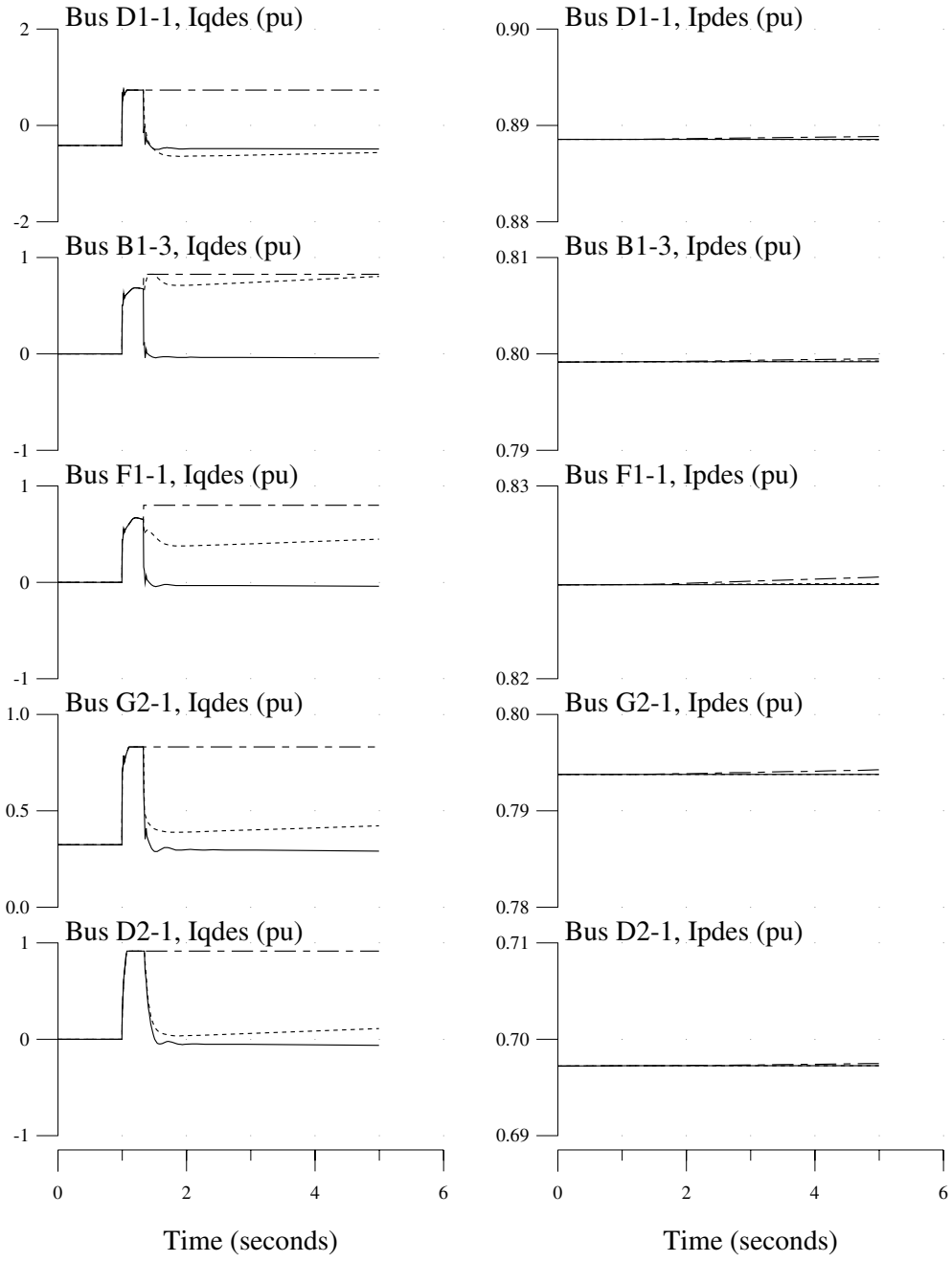
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Voltage Control
DG Active and Reactive Power
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Voltage Control
DG Control Signals
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



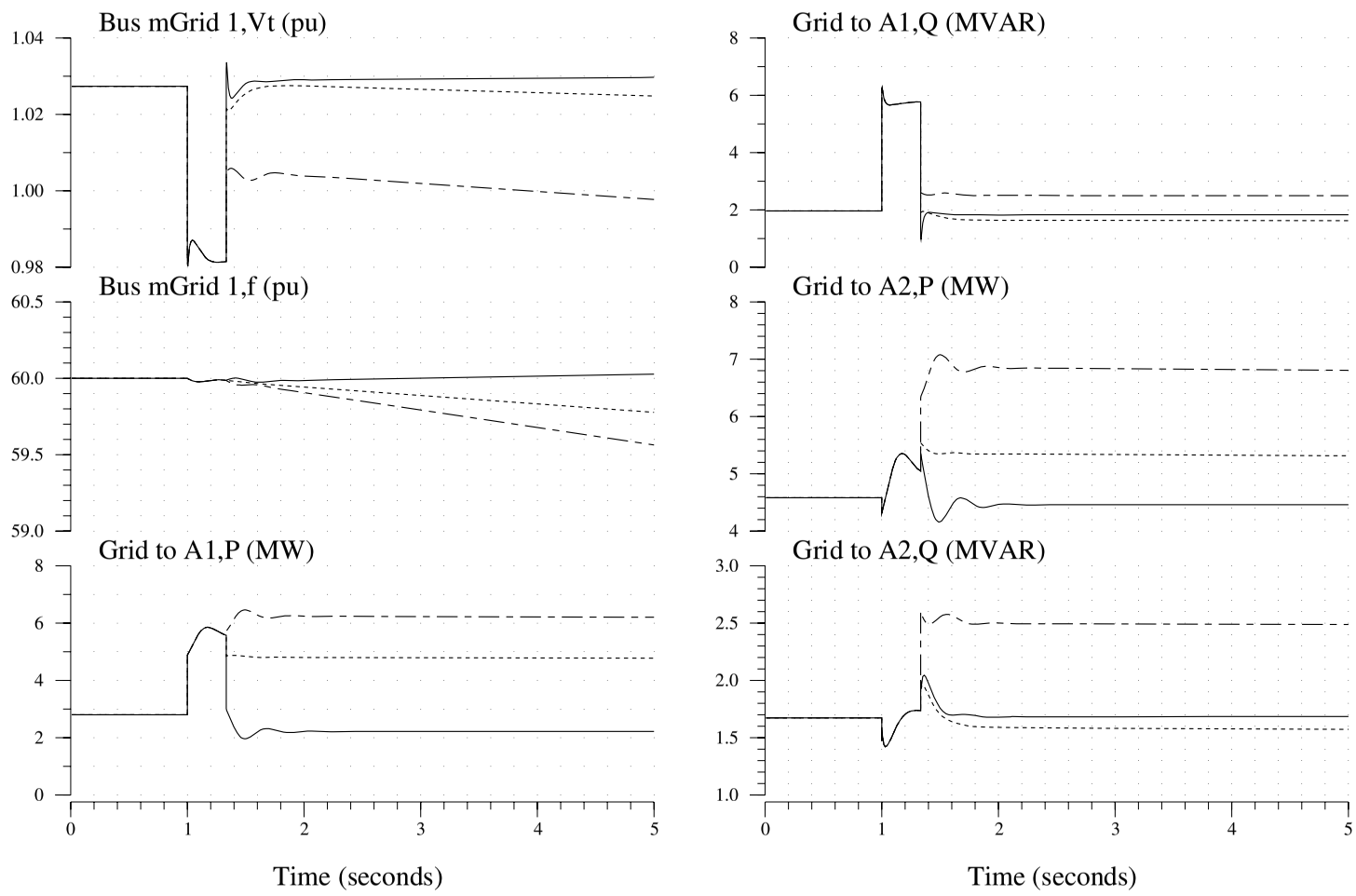
SEPARATOR 4: P2 SYSTEM RESPONSE TO A LATERAL FAULT

All inverter-based DGs with moderate gain voltage control

System 2: Voltage Control

System Quantities

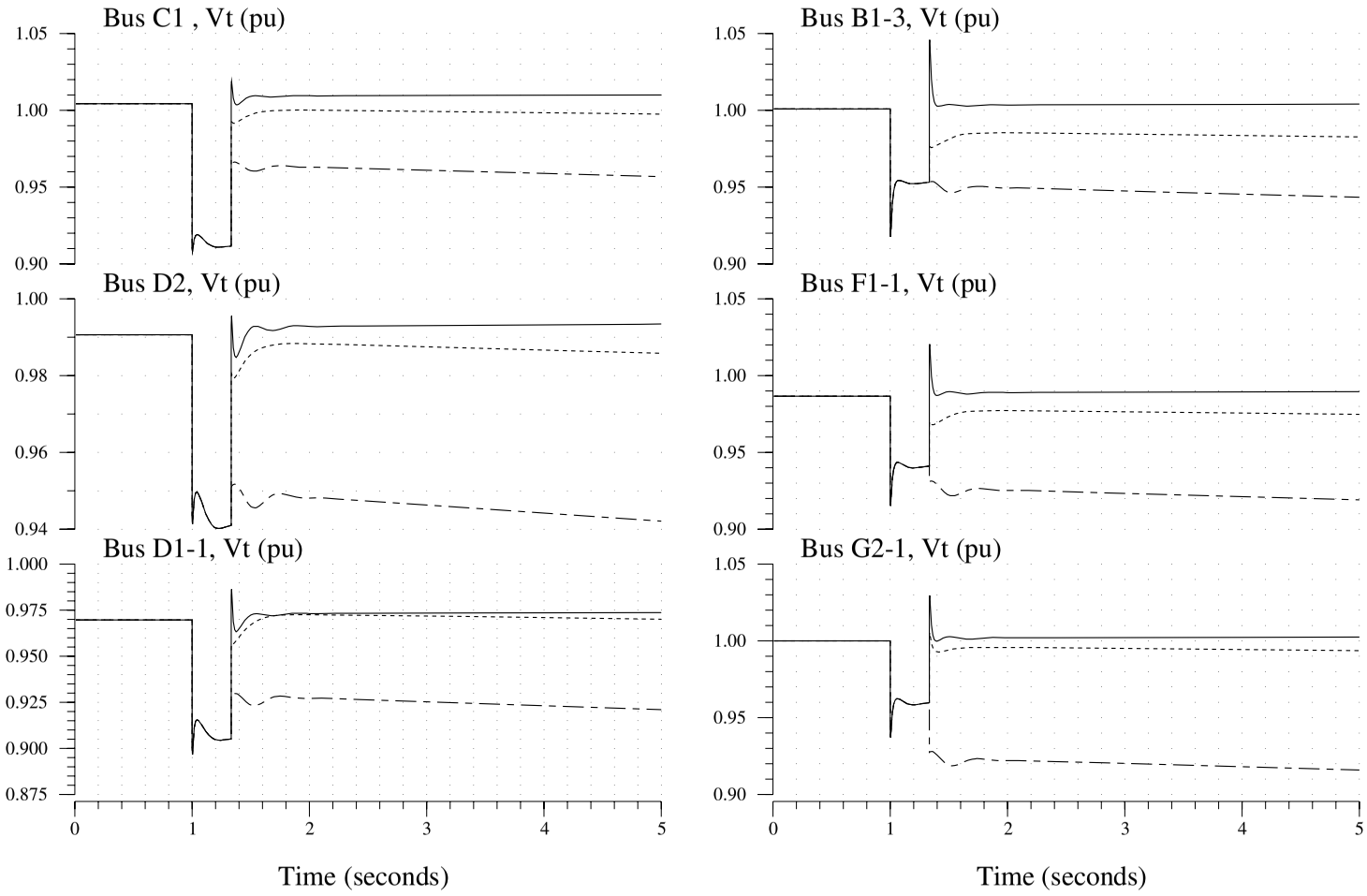
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



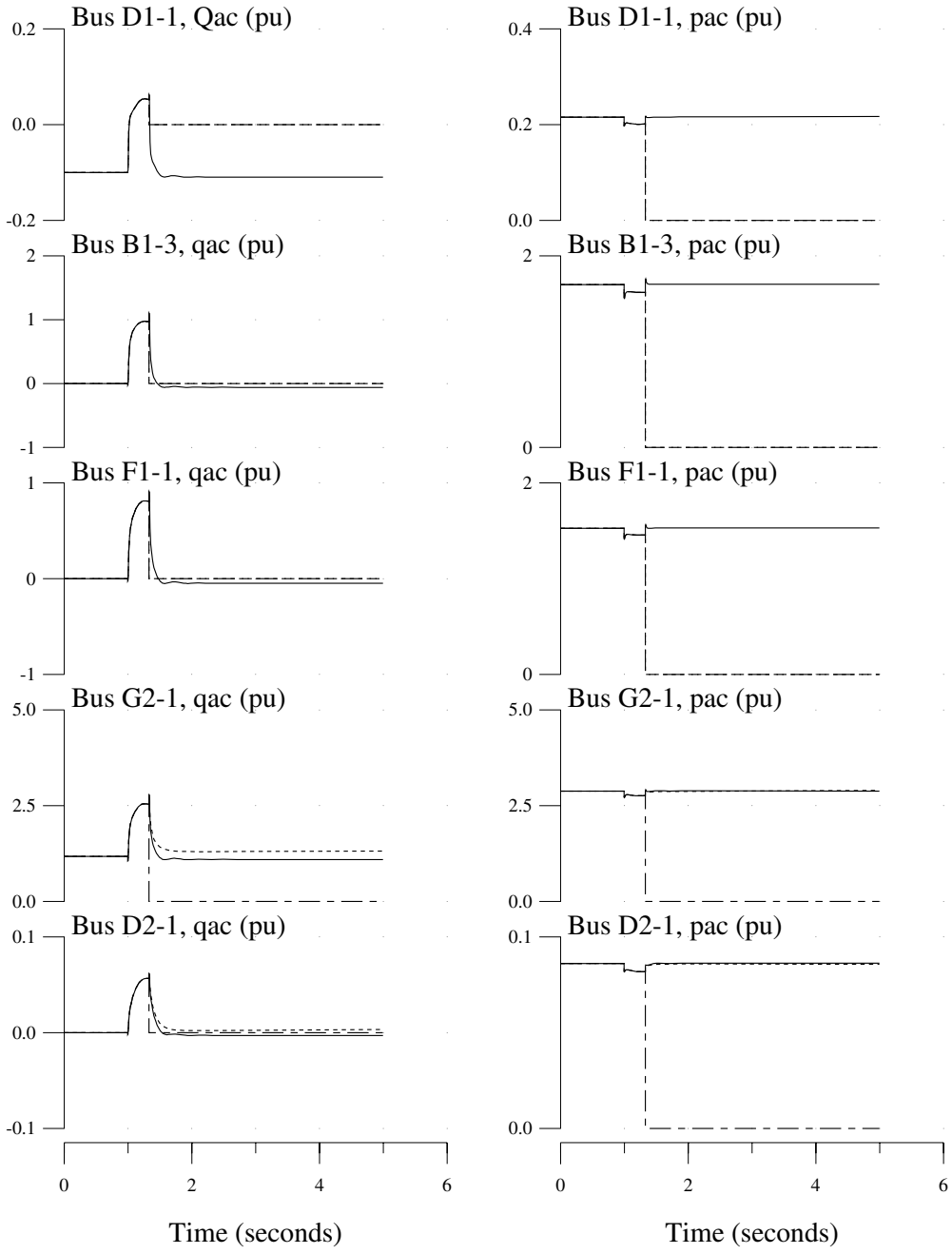
System 2: Voltage Control

Voltages

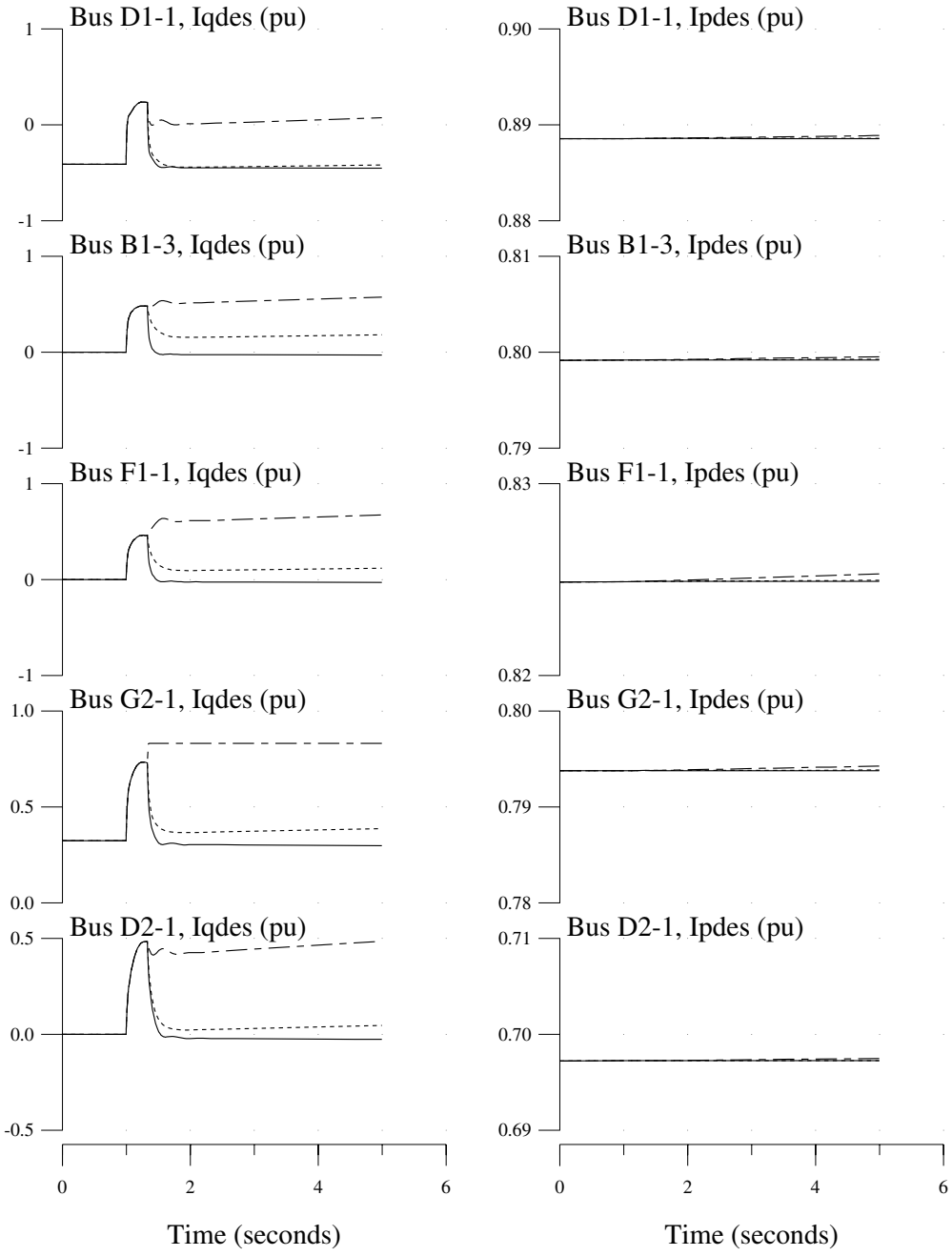
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Voltage Control
DG Active and Reactive Power
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Voltage Control
DG Control Signals
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



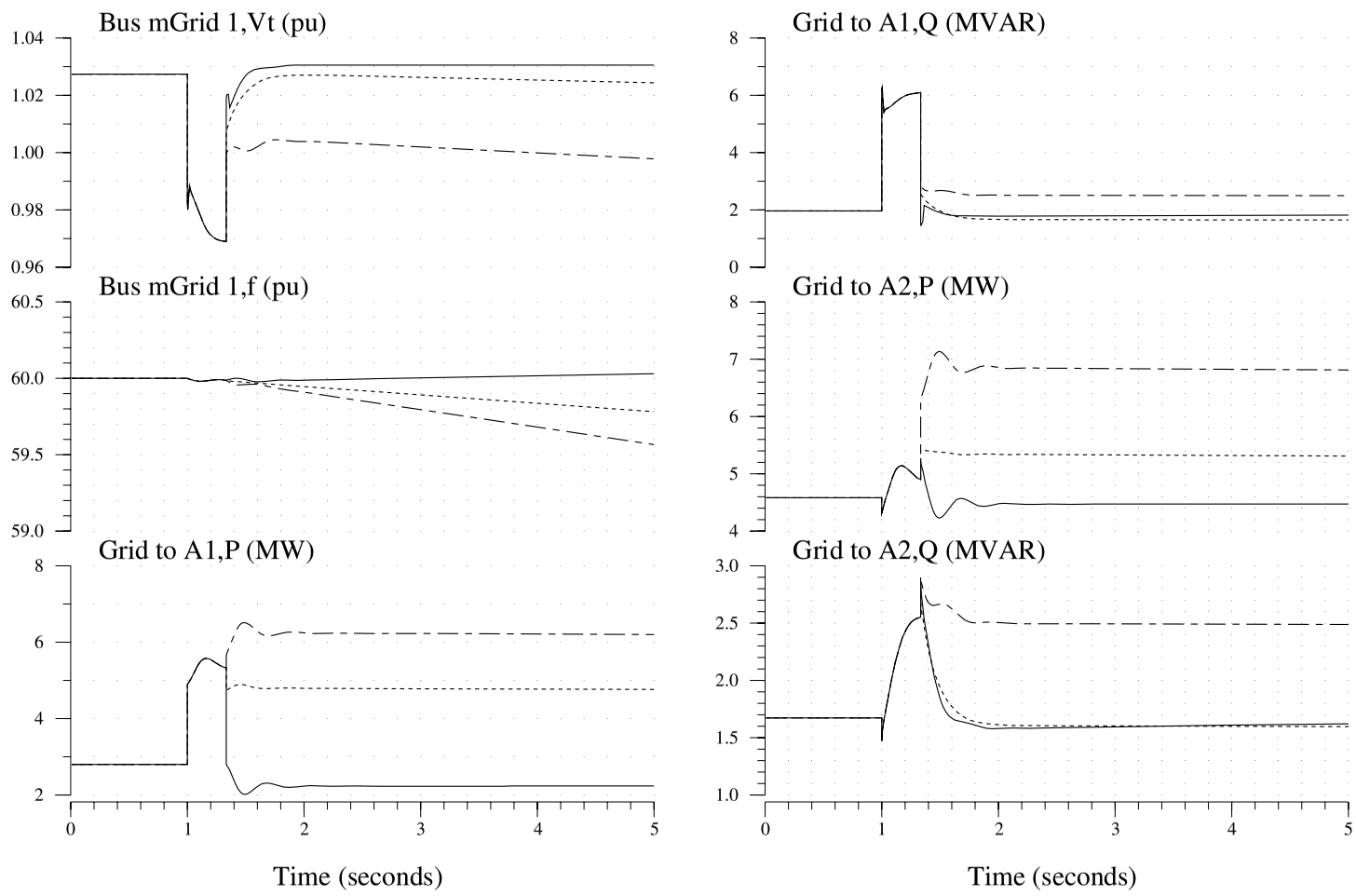
SEPARATOR 5: P2 SYSTEM RESPONSE TO A LATERAL FAULT

All inverter-based DGs with high gain voltage control and constant power control

System 2: Power and Voltage Control

System Quantities

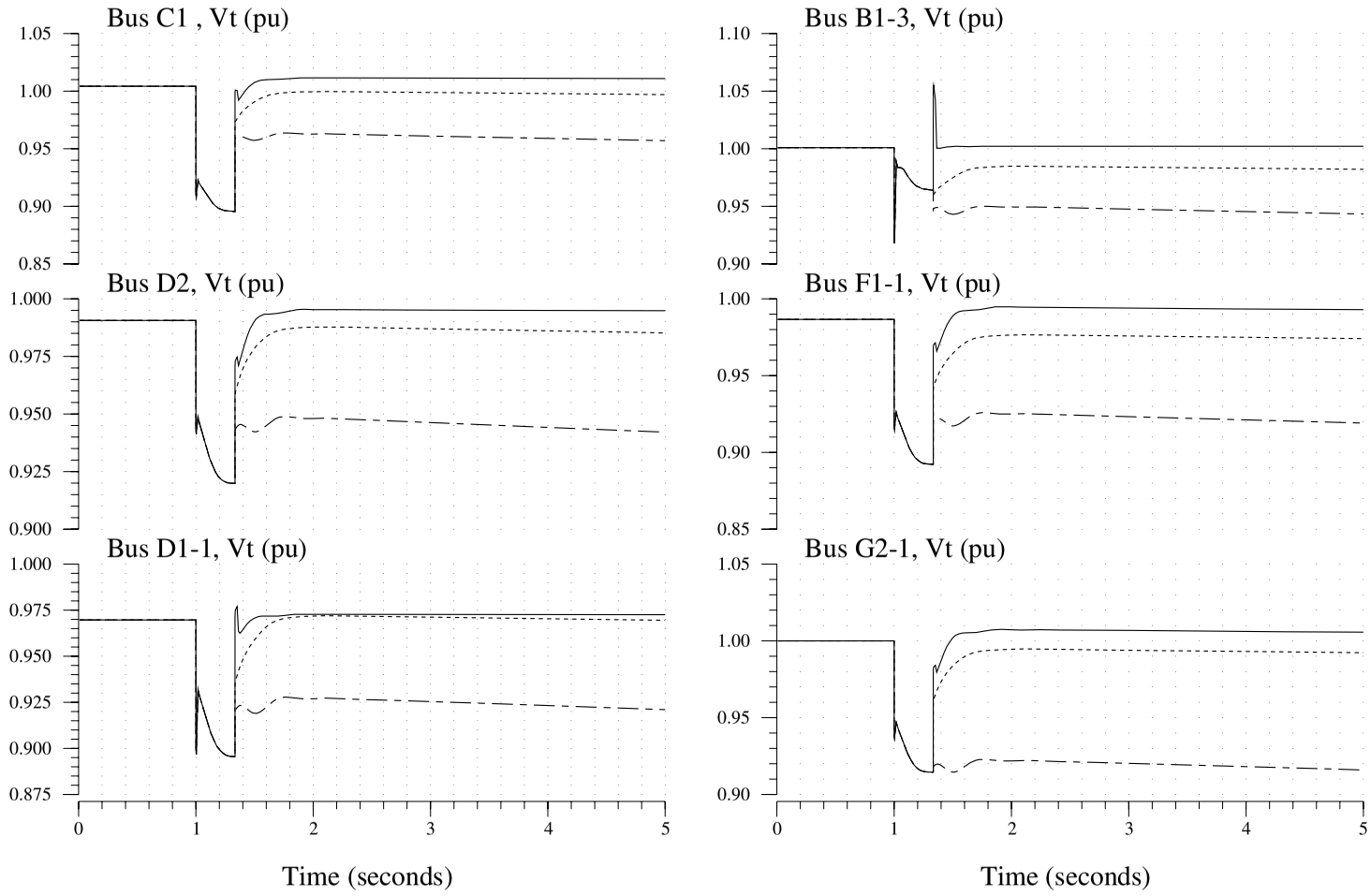
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



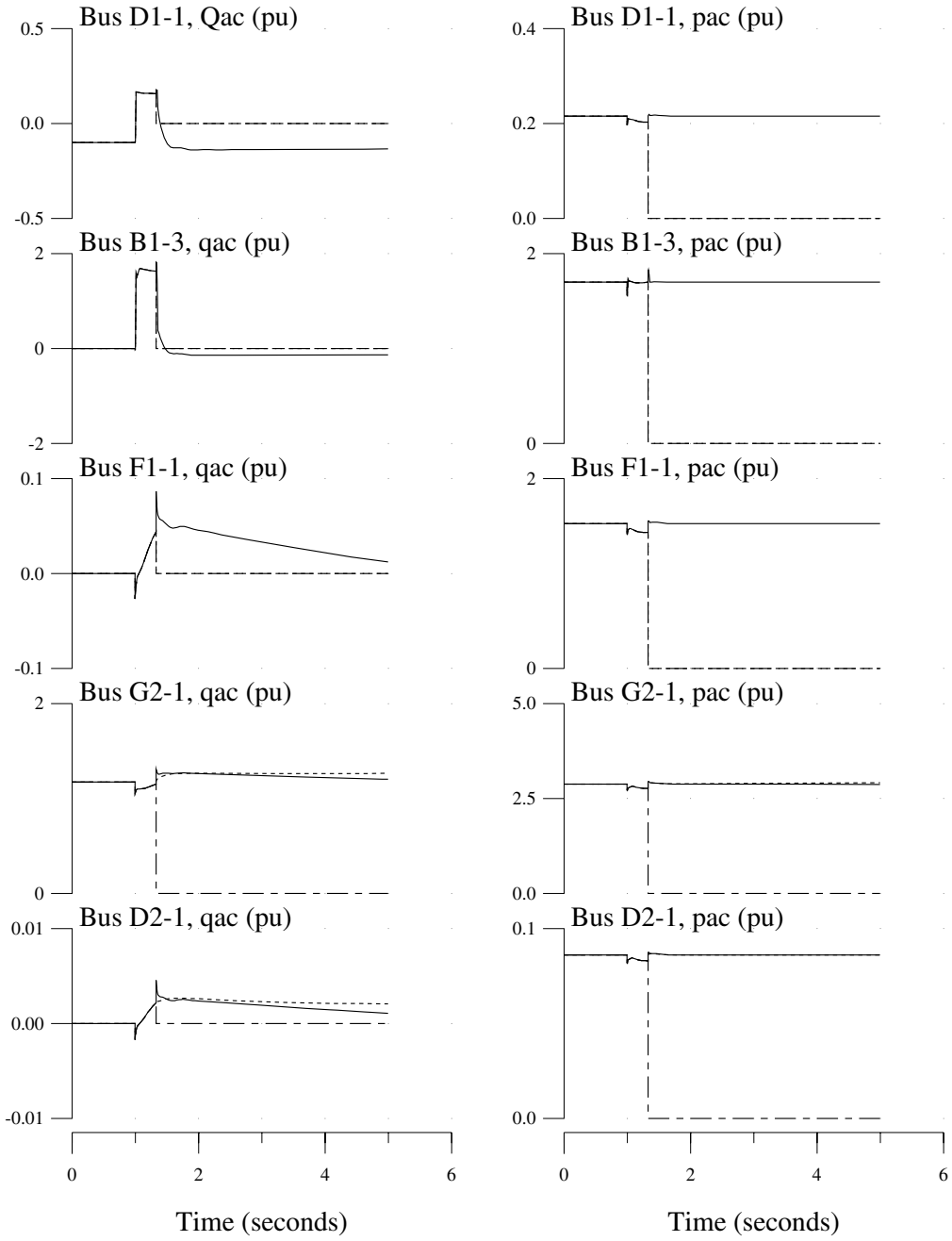
System 2: Power and Voltage Control

Voltages

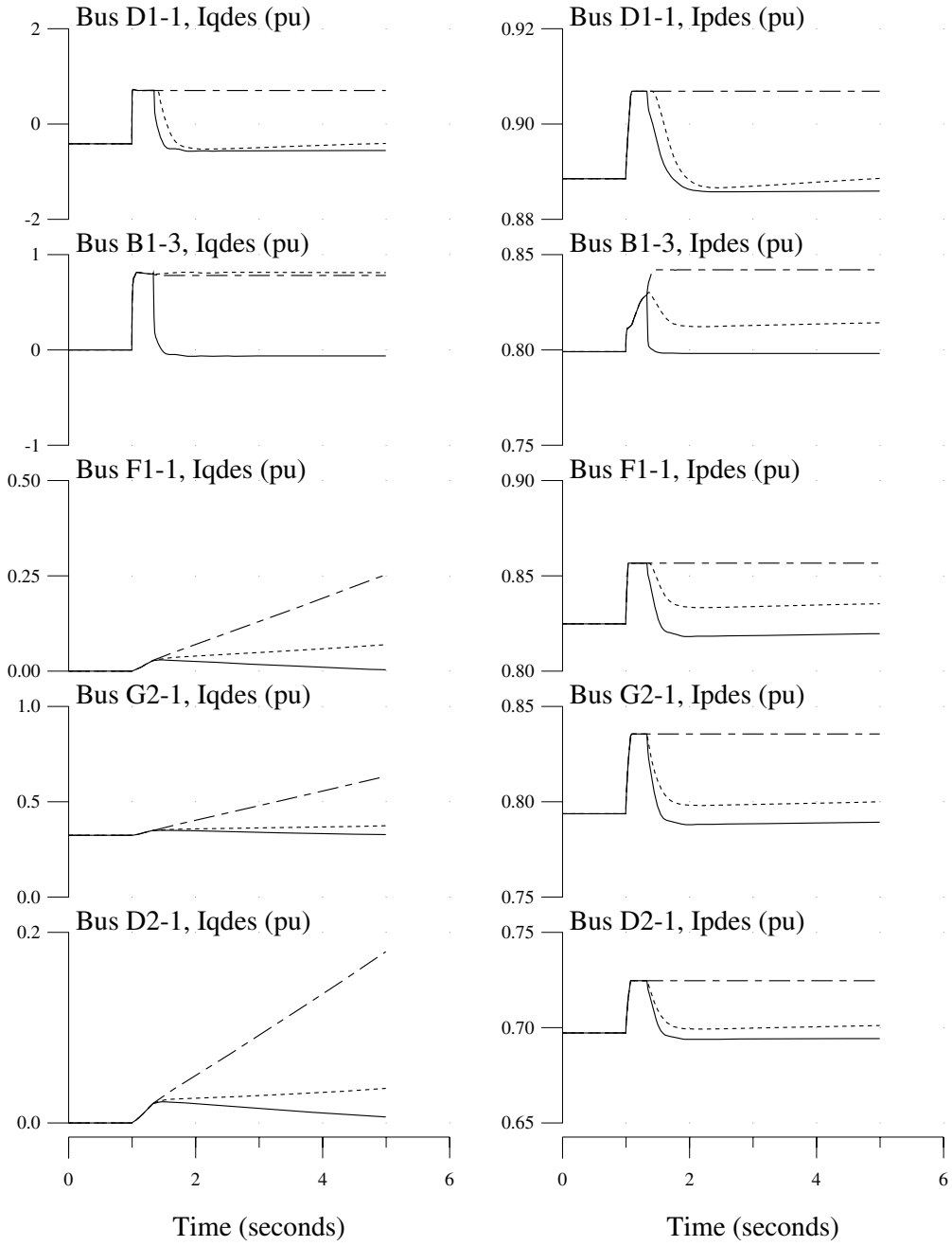
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Power and Voltage Control
DG Active and Reactive Power
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Power and Voltage Control
DG Control Signals
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



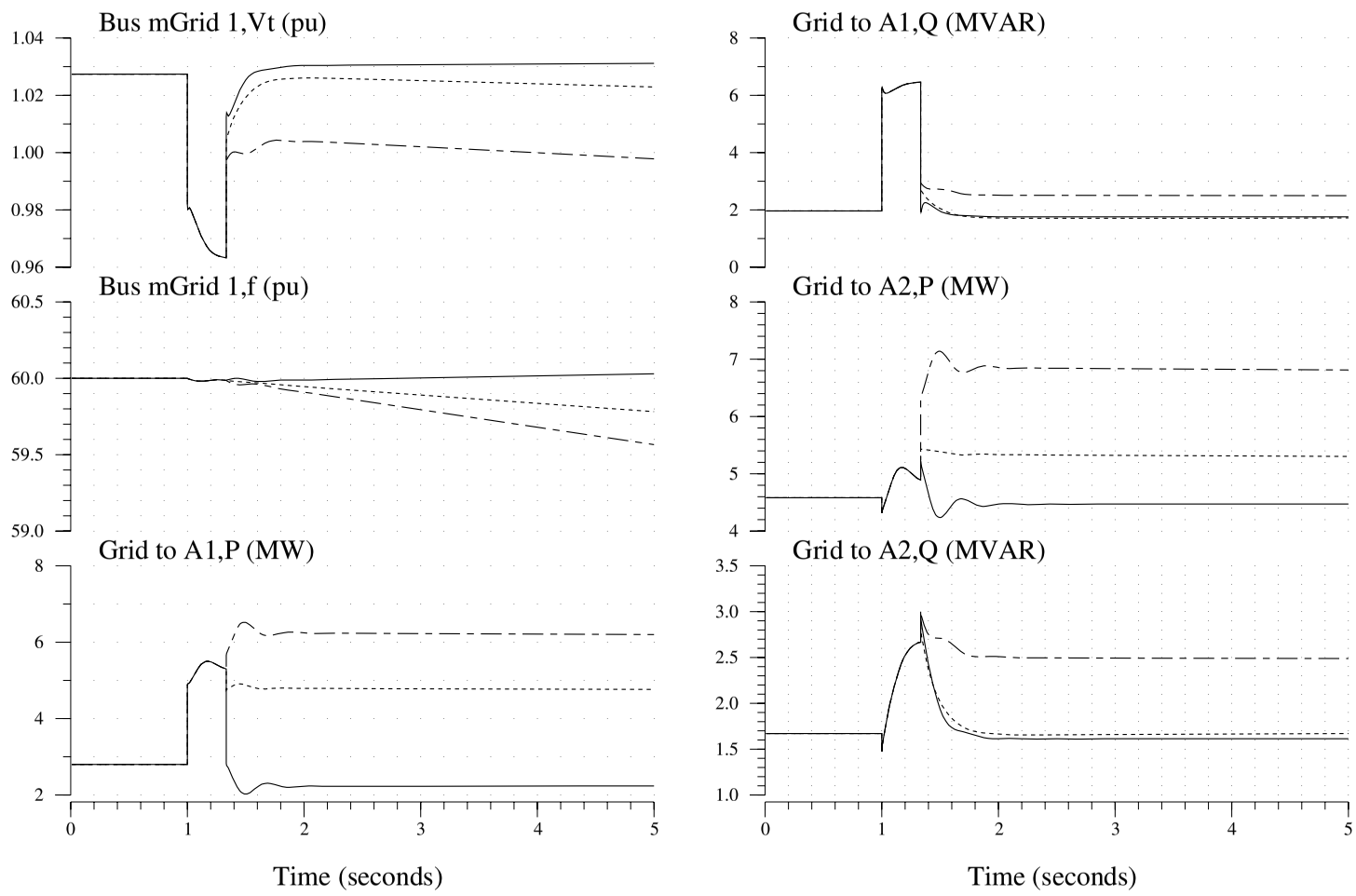
SEPARATOR 6: P2 SYSTEM RESPONSE TO A LATERAL FAULT

All inverter-based DGs with moderate gain voltage control and constant power control

System 2: Power and Voltage Control

System Quantities

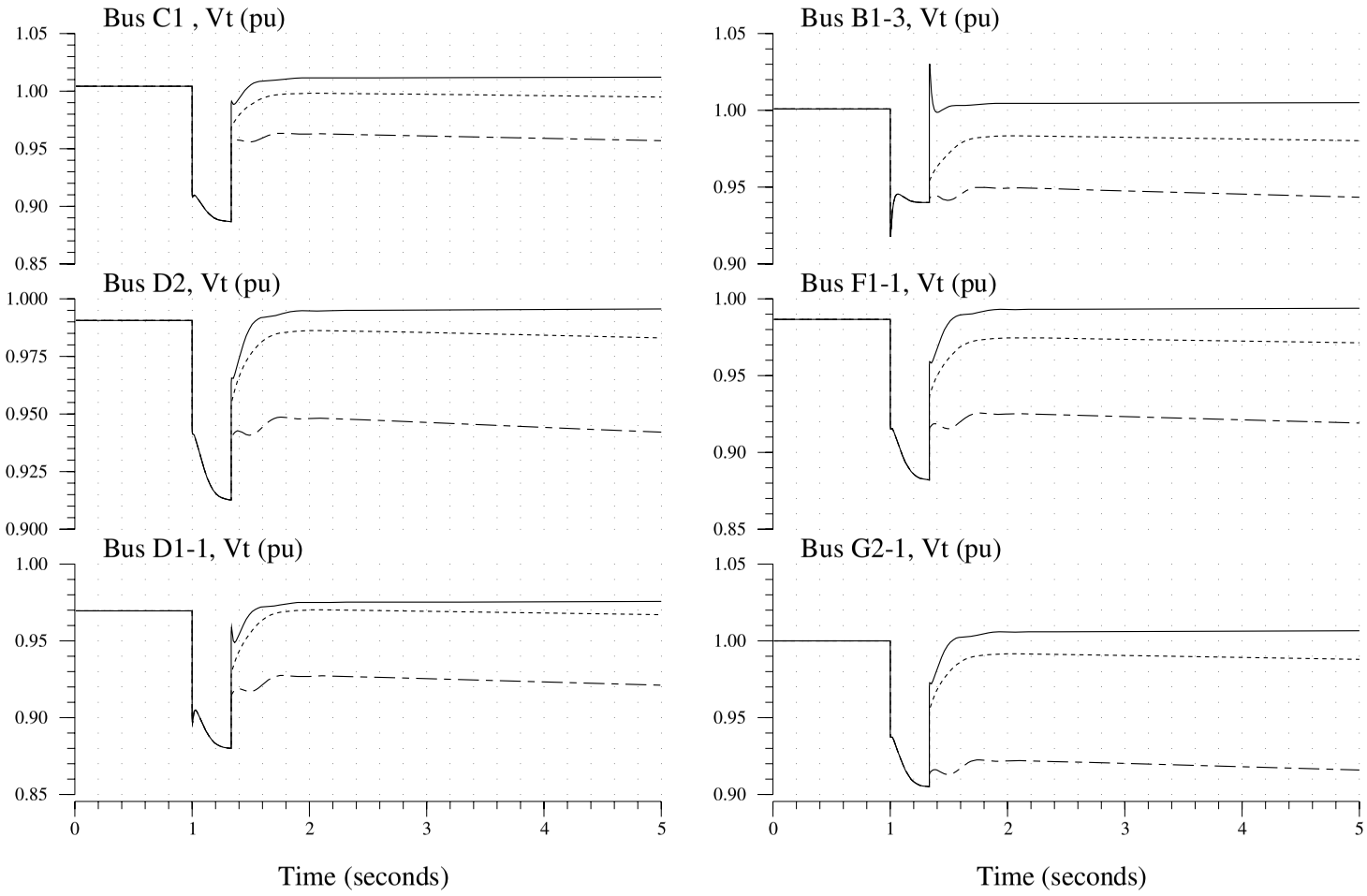
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



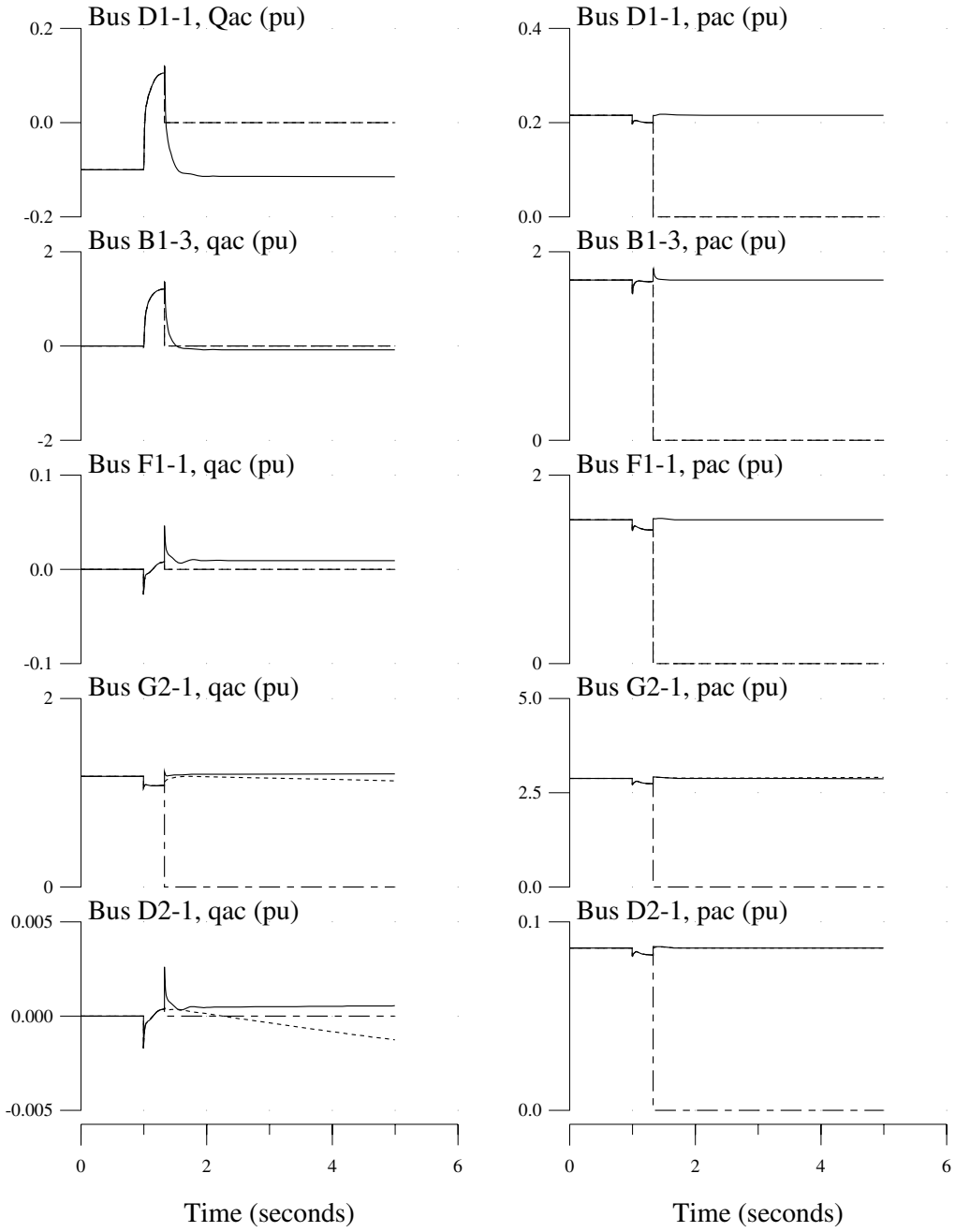
System 2: Power and Voltage Control

Voltages

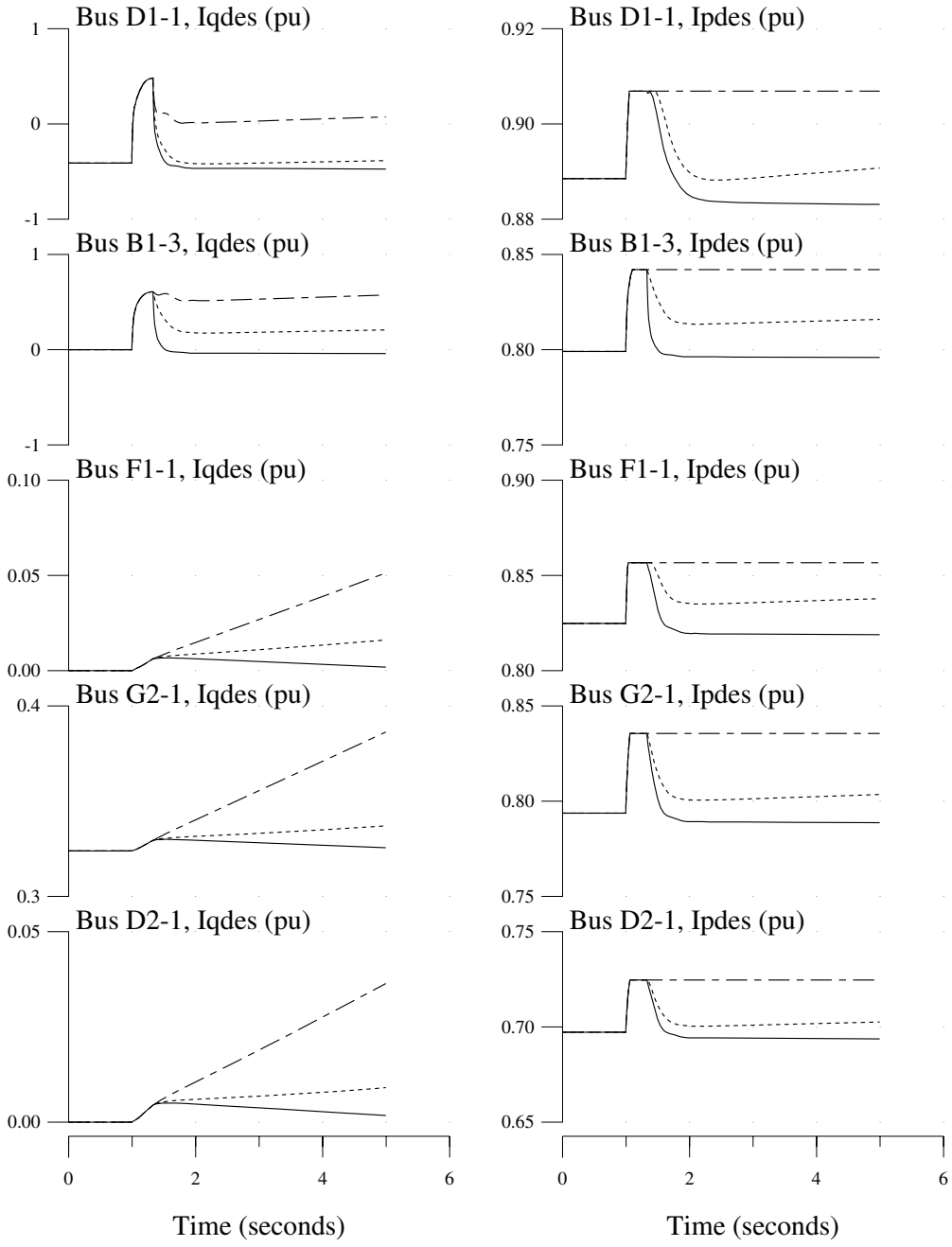
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Power and Voltage Control
DG Active and Reactive Power
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



System 2: Power and Voltage Control
DG Control Signals
no DG trip (____), 3DG trip (_ _ _), all DG trip (__ _ __)



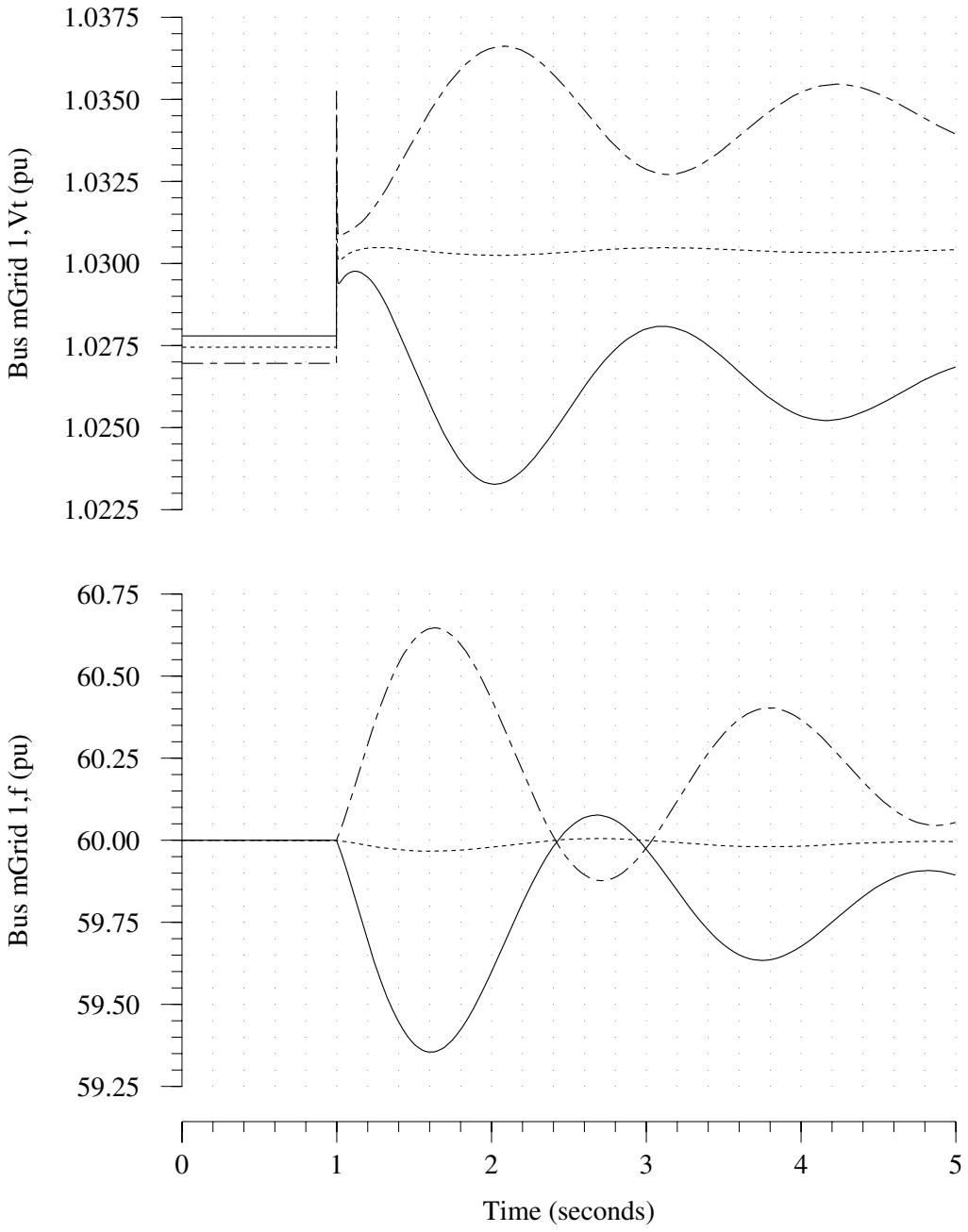
Appendix G. Microgrid

SEPARATOR 1: P2 SYSTEM CONFIGURED AS A MICRO GRID

All Inverter Based DGs with Voltage and Frequency Regulation
Response to Trip of Microgrid from the Utility Grid

3 Cases on Each Set of Axes reflect different initial power exchanges with the utility grid:
Solid Trace: Microgrid Initially Importing approximately 1 MW.
Dotted Trace: Microgrid Initially nearly balanced (very small import)
Dot-Dash Trace: Microgrid Initially Exporting approximately 1 MW

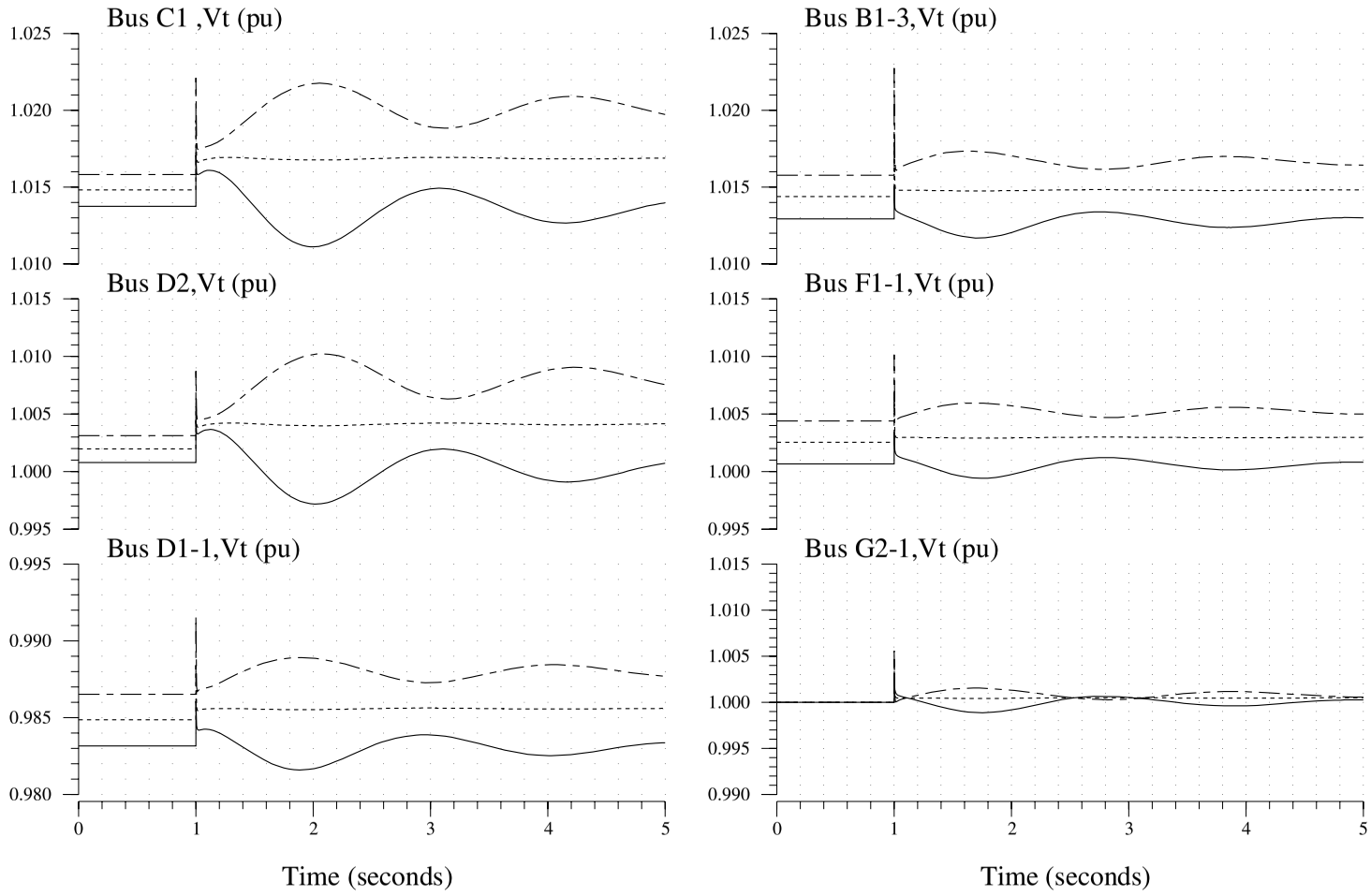
System 2: Frequency Regulation
System Quantities
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)



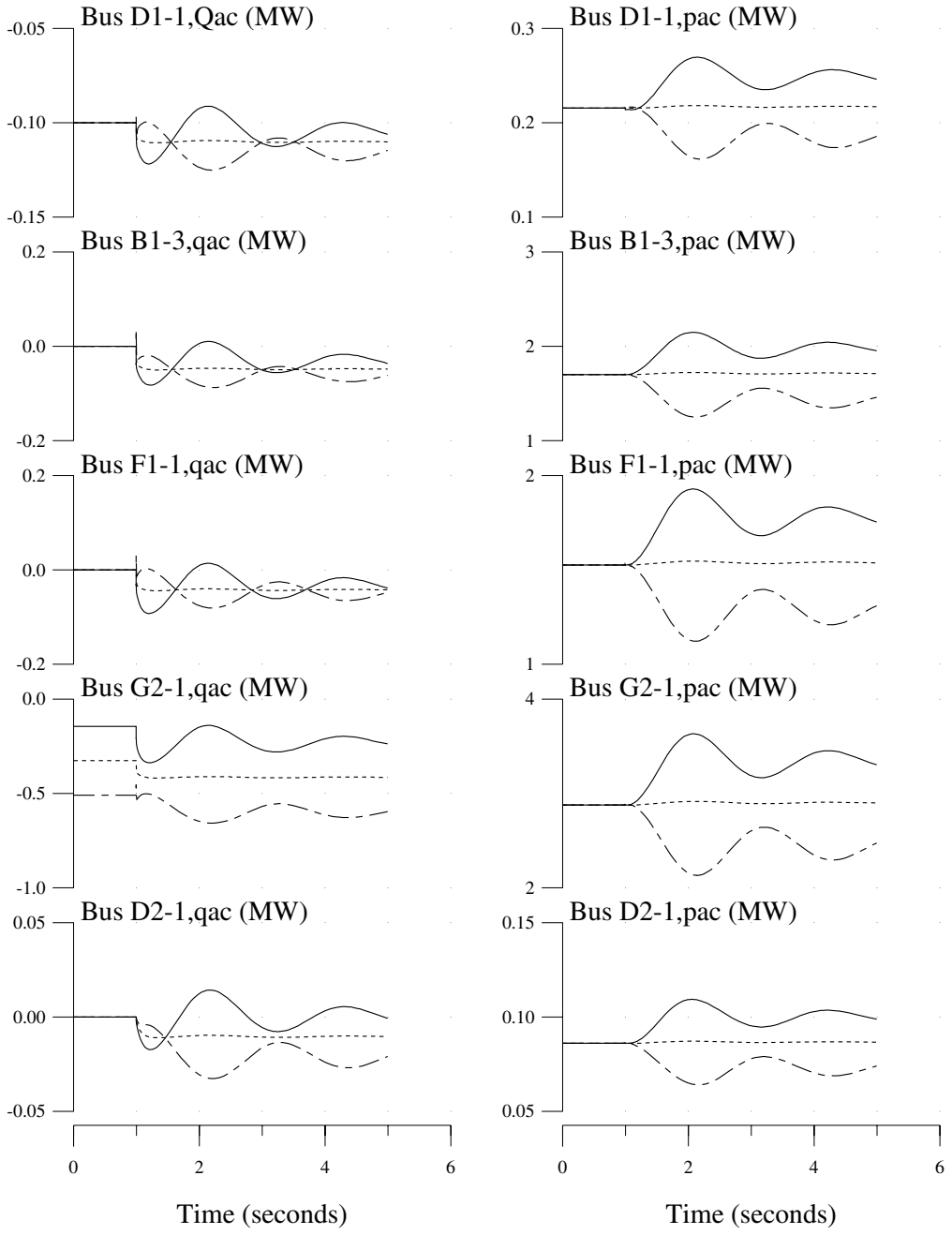
System 2: Frequency Regulation

Voltages

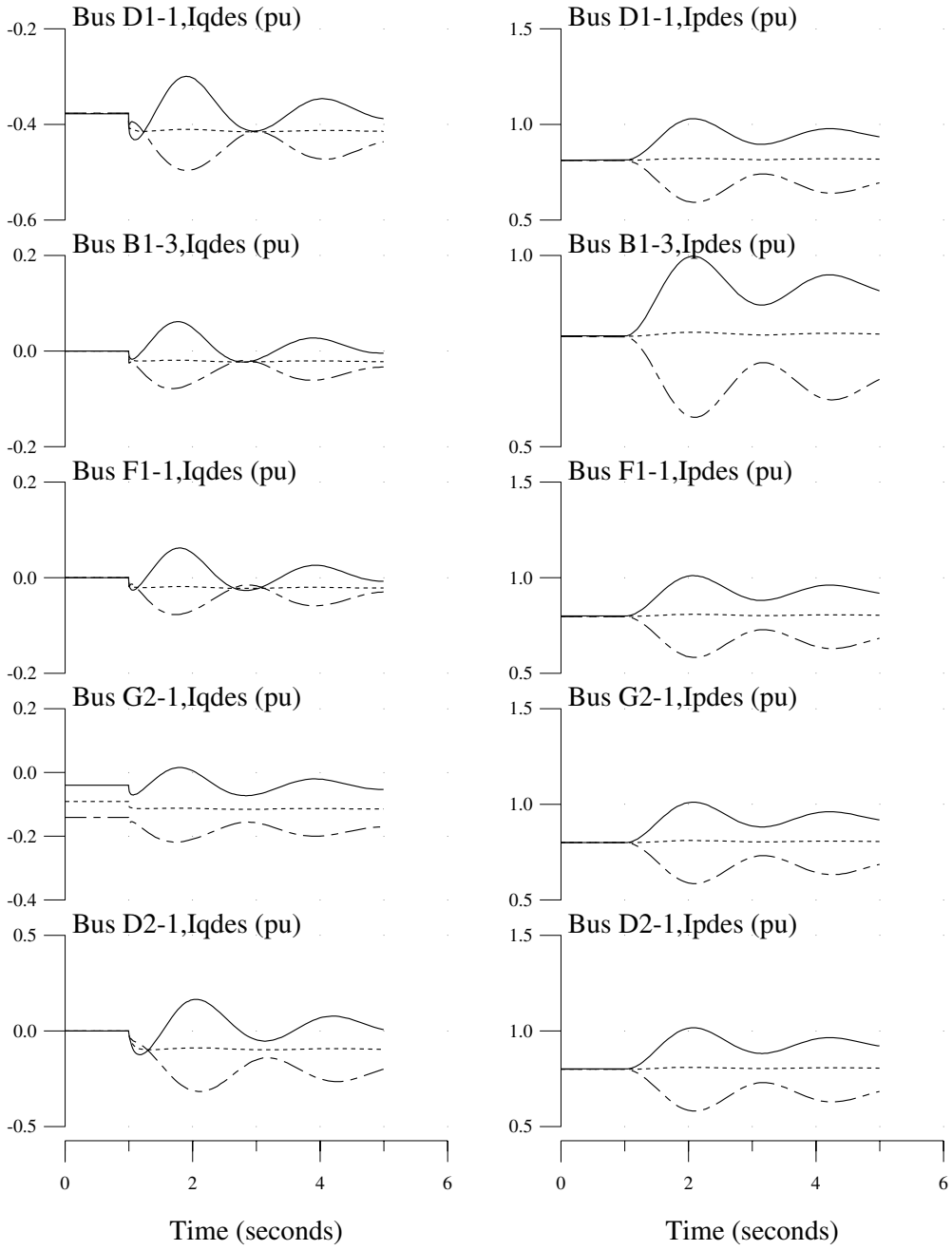
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(- - -)



System 2: Frequency Regulation
DG Active and Reactive Power
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)



System 2: Frequency Regulation
DG Control signals
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)



SEPARATOR 2: P2 SYSTEM CONFIGURED AS A MICRO GRID

All Inverter Based DGs with Voltage and Frequency Regulation

Response to Trip of Microgrid from the Utility Grid

This is the same case as shown in the previous group of traces, except that the ***unstable*** *case with initial import of 2 MW is included. Note the change in scales, and trace patterns.*

4 Cases on Each Set of Axes reflect different initial power exchanges with the utility grid:

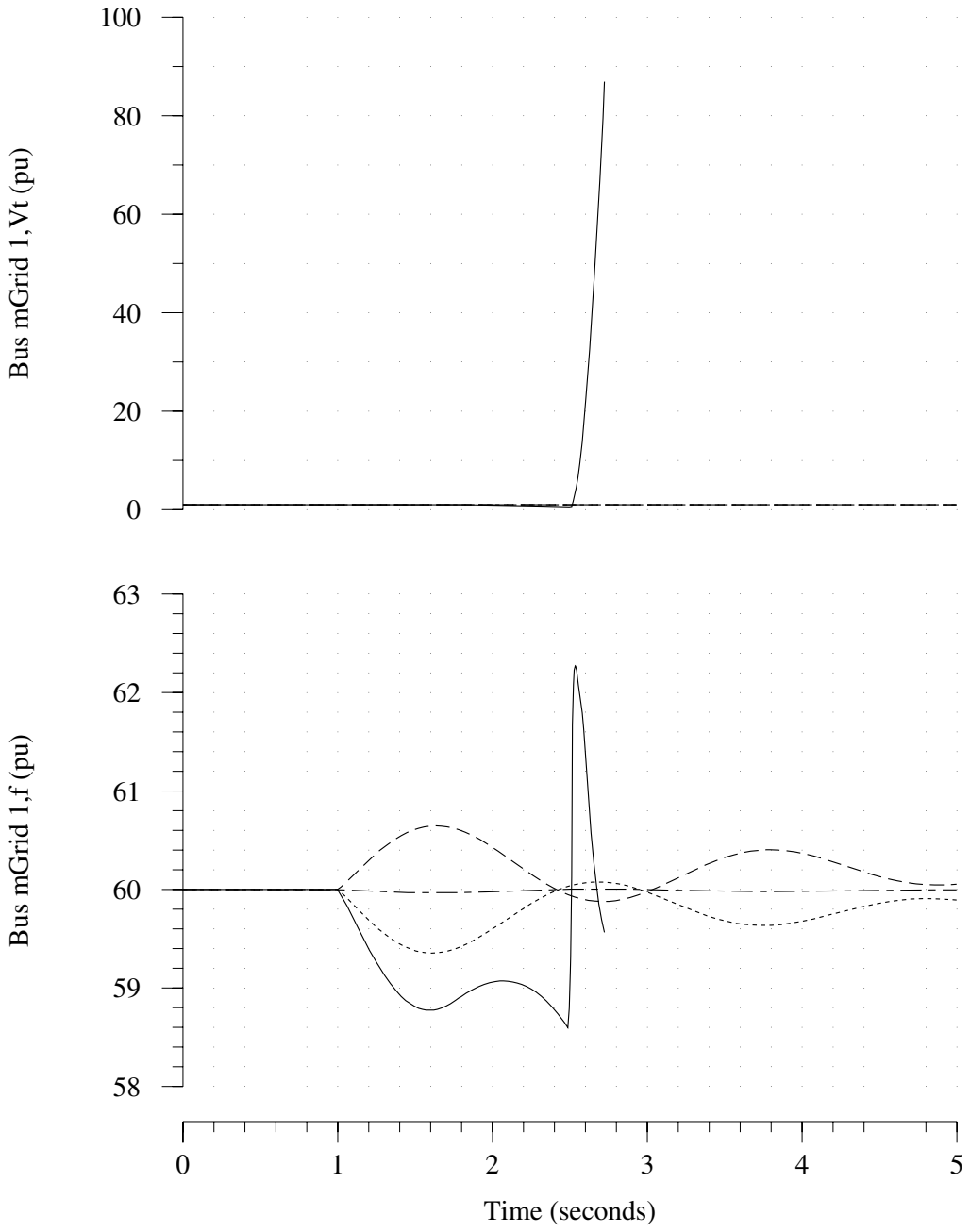
Solid Trace: Microgrid Initially Importing approximately 2 MW.

Dotted Trace: : Microgrid Initially Importing approximately 1 MW.

Dot-Dash Trace: Microgrid Initally nearly balanced (very small import)

Dash Trace: Microgrid Initially Exporting approximately 1 MW

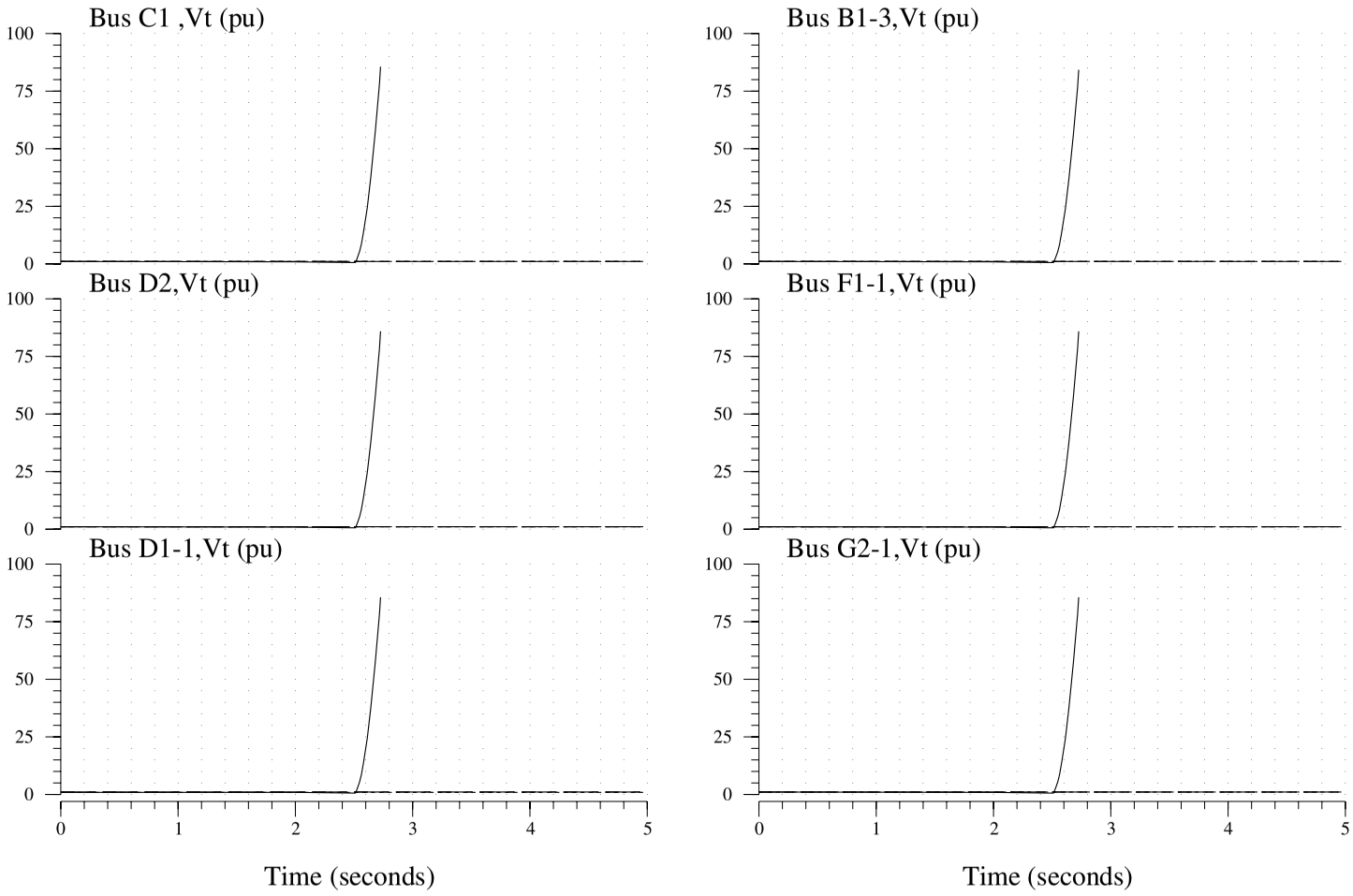
System 2: Frequency Regulation
System Quantities
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)



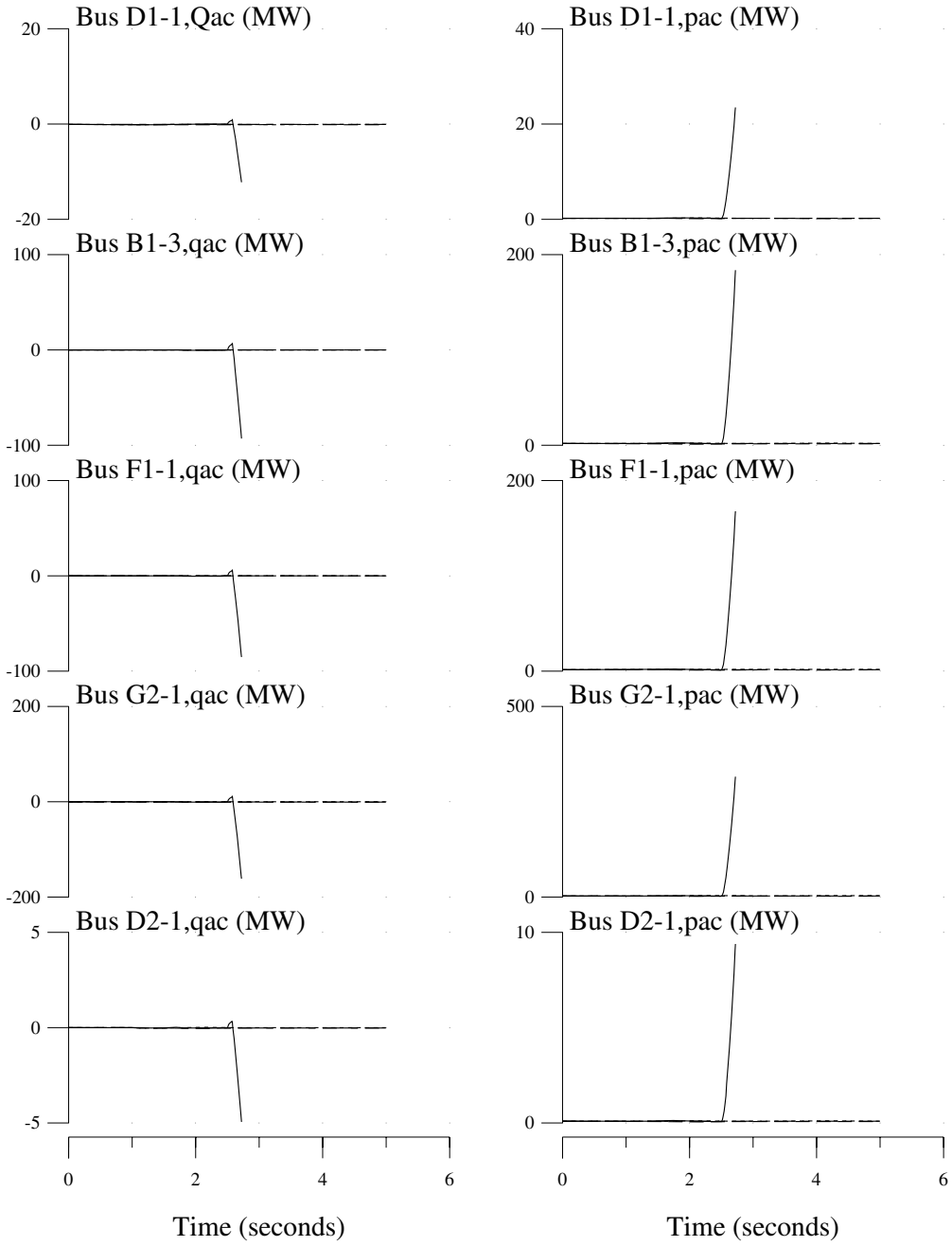
System 2: Frequency Regulation

Voltages

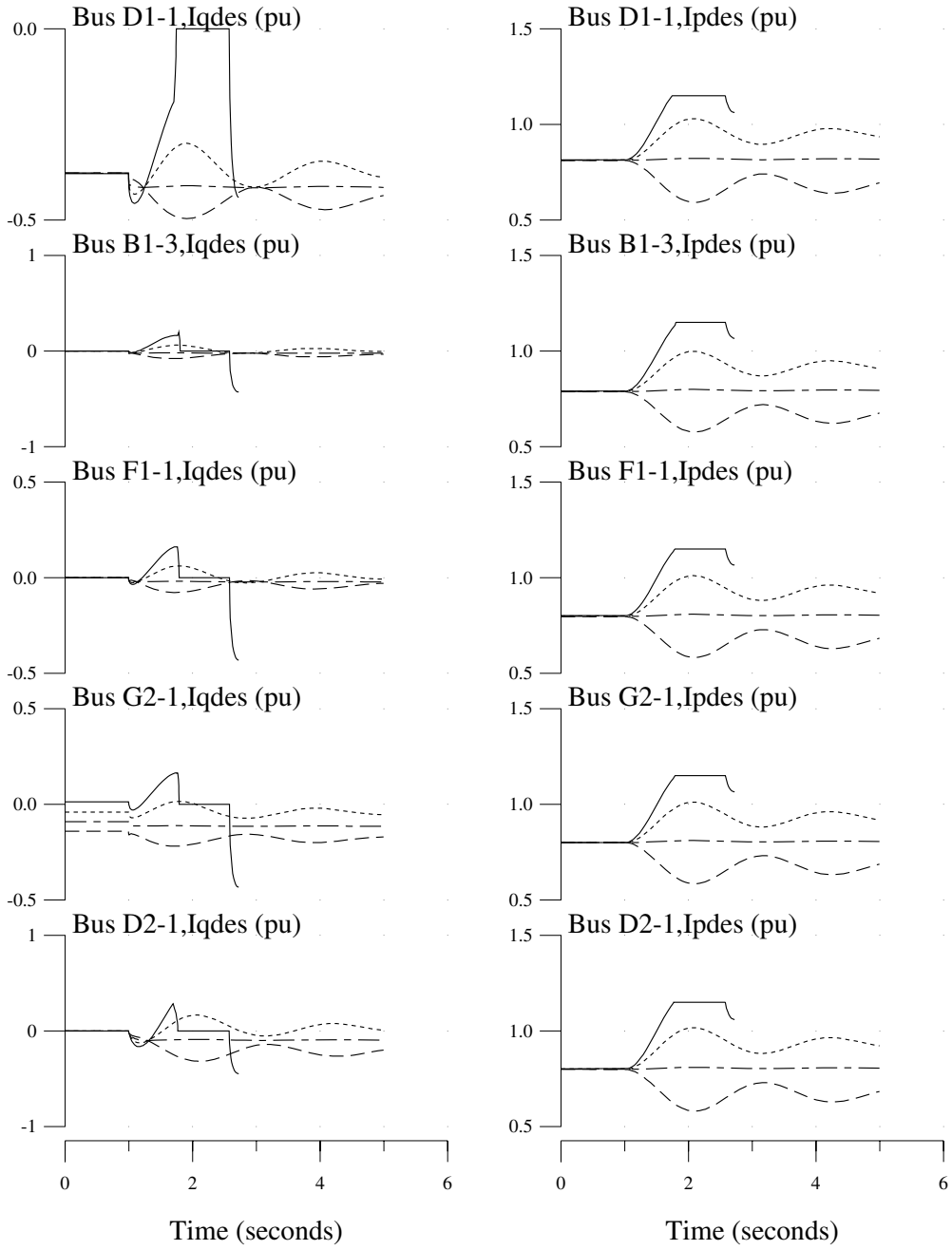
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(- - -)



System 2: Frequency Regulation
DG Active and Reactive Power
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)



System 2: Frequency Regulation
DG Control signals
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)

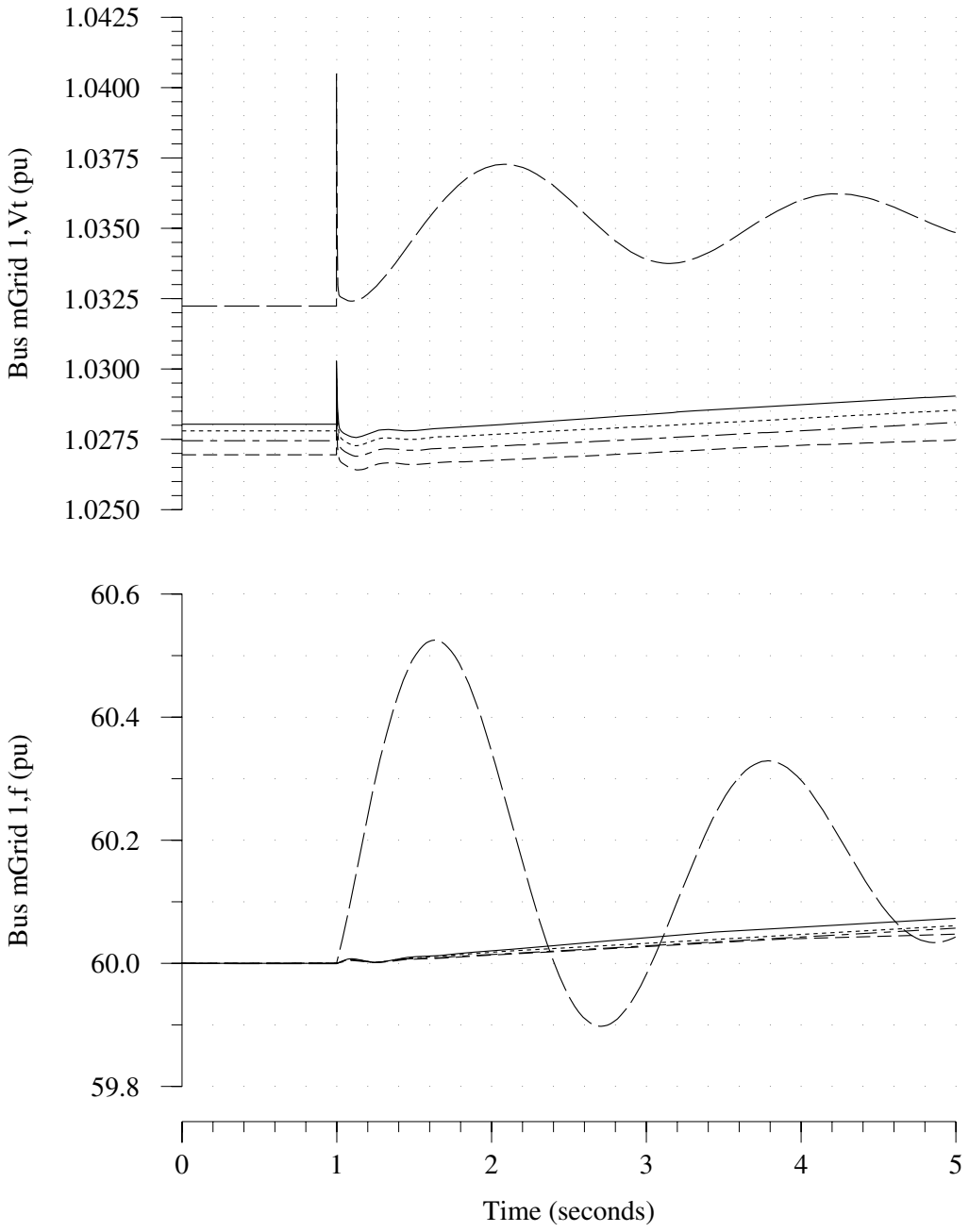


SEPARATOR 3: P2 SYSTEM CONFIGURED AS A MICRO GRID

All Inverter Based DGs with Voltage and Frequency Regulation
Response to Trip of a Load on the Microgrid

5 Cases on Each Set of Axes reflect different initial power exchanges with the utility grid:
Solid Trace: Microgrid Initially Importing approximately 2 MW.
Dotted Trace: : Microgrid Initially Importing approximately 1 MW.
Dot-Dash Trace: Microgrid Initally nearly balanced (very small import)
Dash Trace: Microgrid Initially Exporting approximately 1 MW
Long Dash: Microgrid Initially Operating Islanded from the Grid

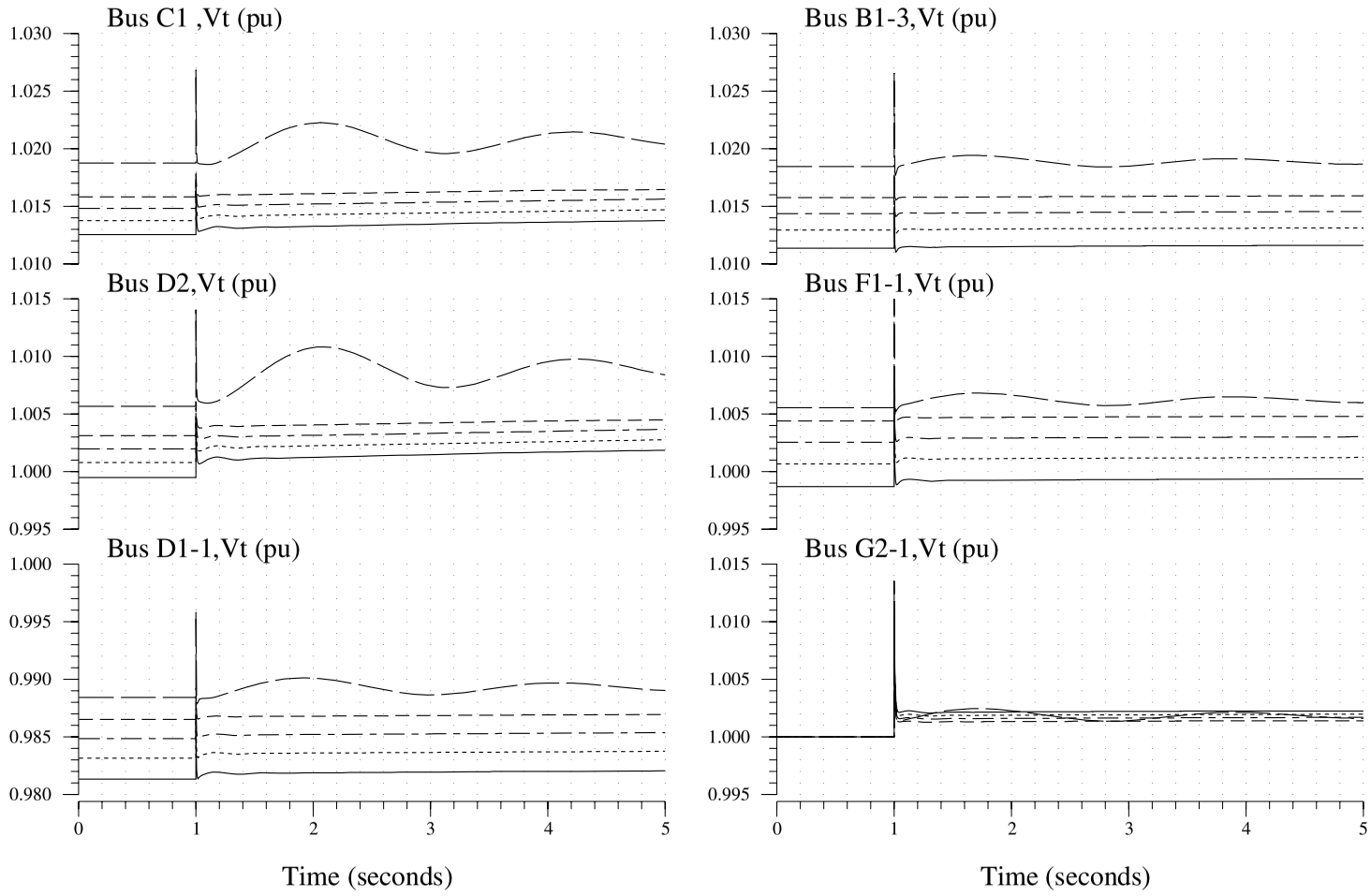
System 2: Frequency Regulation
System Quantities
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)



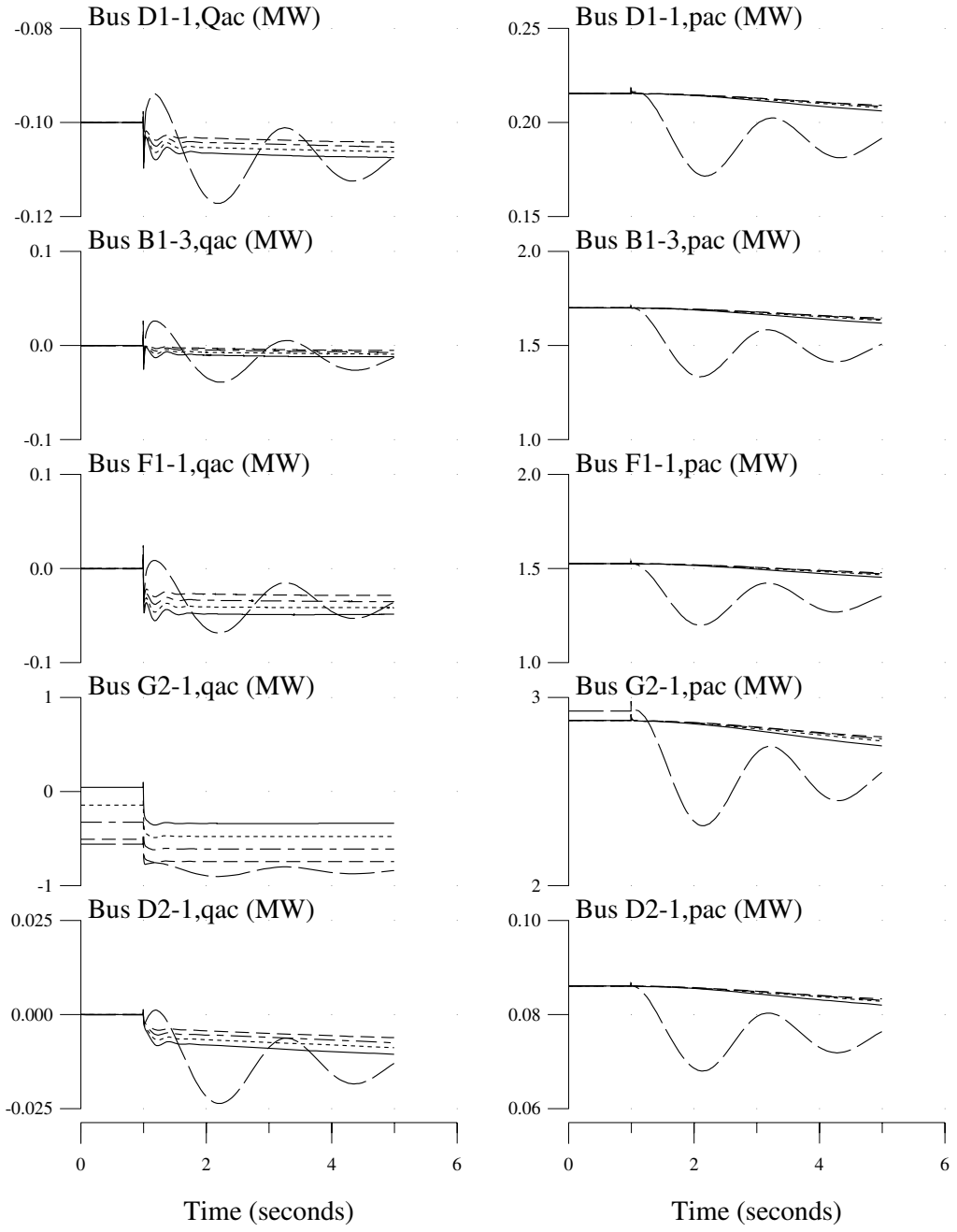
System 2: Frequency Regulation

Voltages

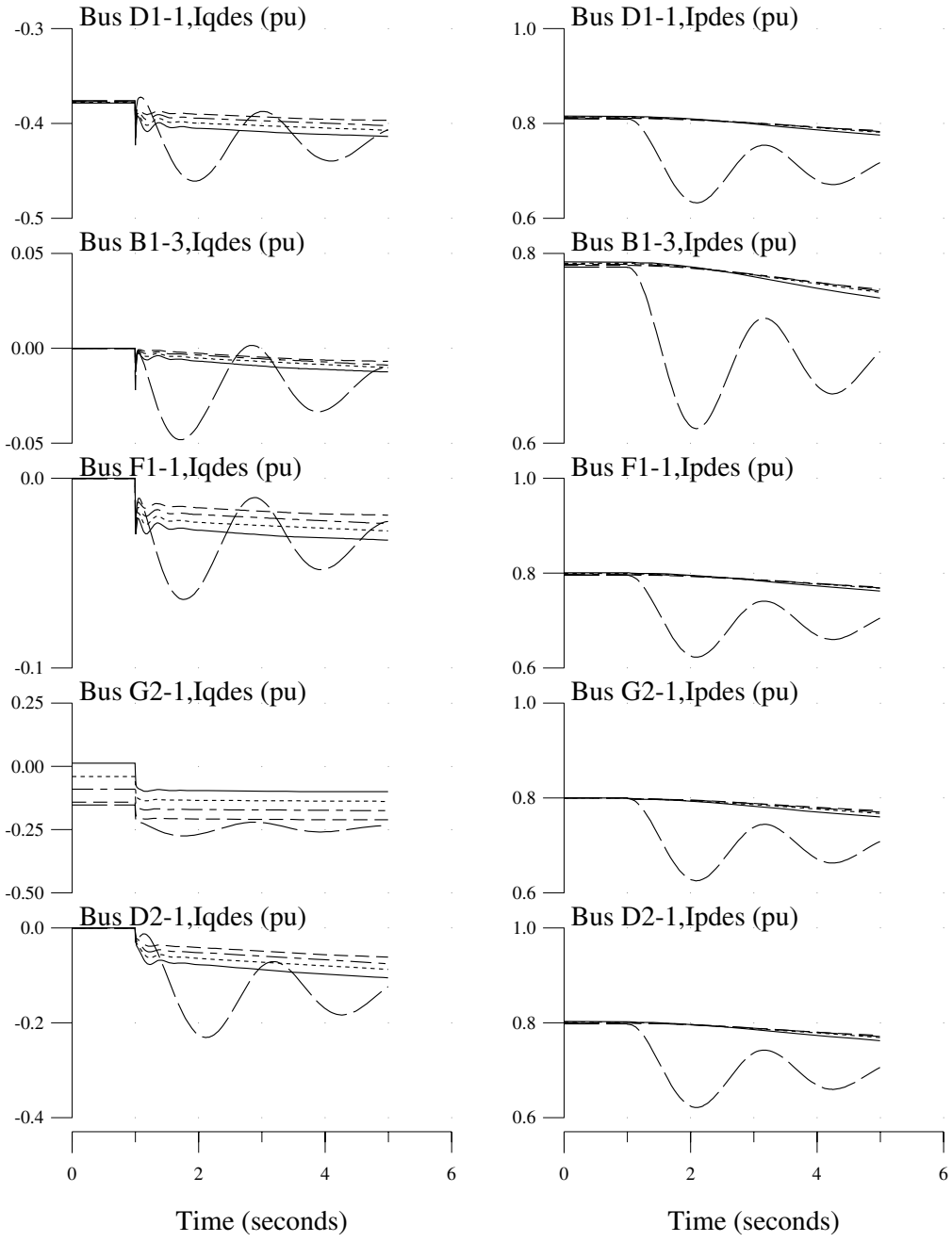
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(- - -)



System 2: Frequency Regulation
DG Active and Reactive Power
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)



System 2: Frequency Regulation
DG Control signals
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)

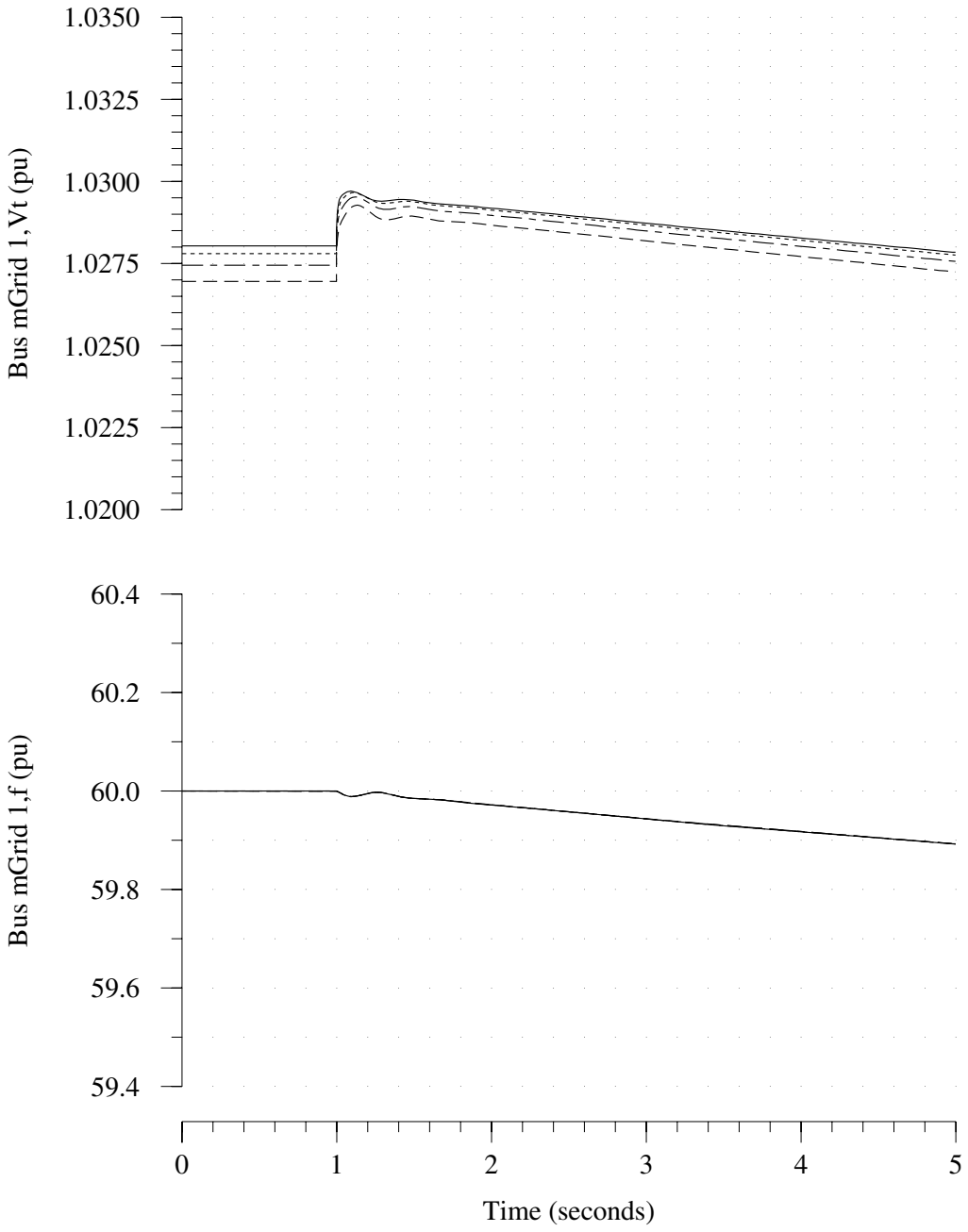


SEPARATOR 4: P2 SYSTEM CONFIGURED AS A MICRO GRID

All Inverter Based DGs with Voltage and Frequency Regulation
Response to Trip of a DG on the Microgrid

4 Cases on Each Set of Axes reflect different initial power exchanges with the utility grid:
Solid Trace: Microgrid Initially Importing approximately 2 MW.
Dotted Trace: : Microgrid Initially Importing approximately 1 MW.
Dot-Dash Trace: Microgrid Initally nearly balanced (very small import)
Dash Trace: Microgrid Initially Exporting approximately 1 MW

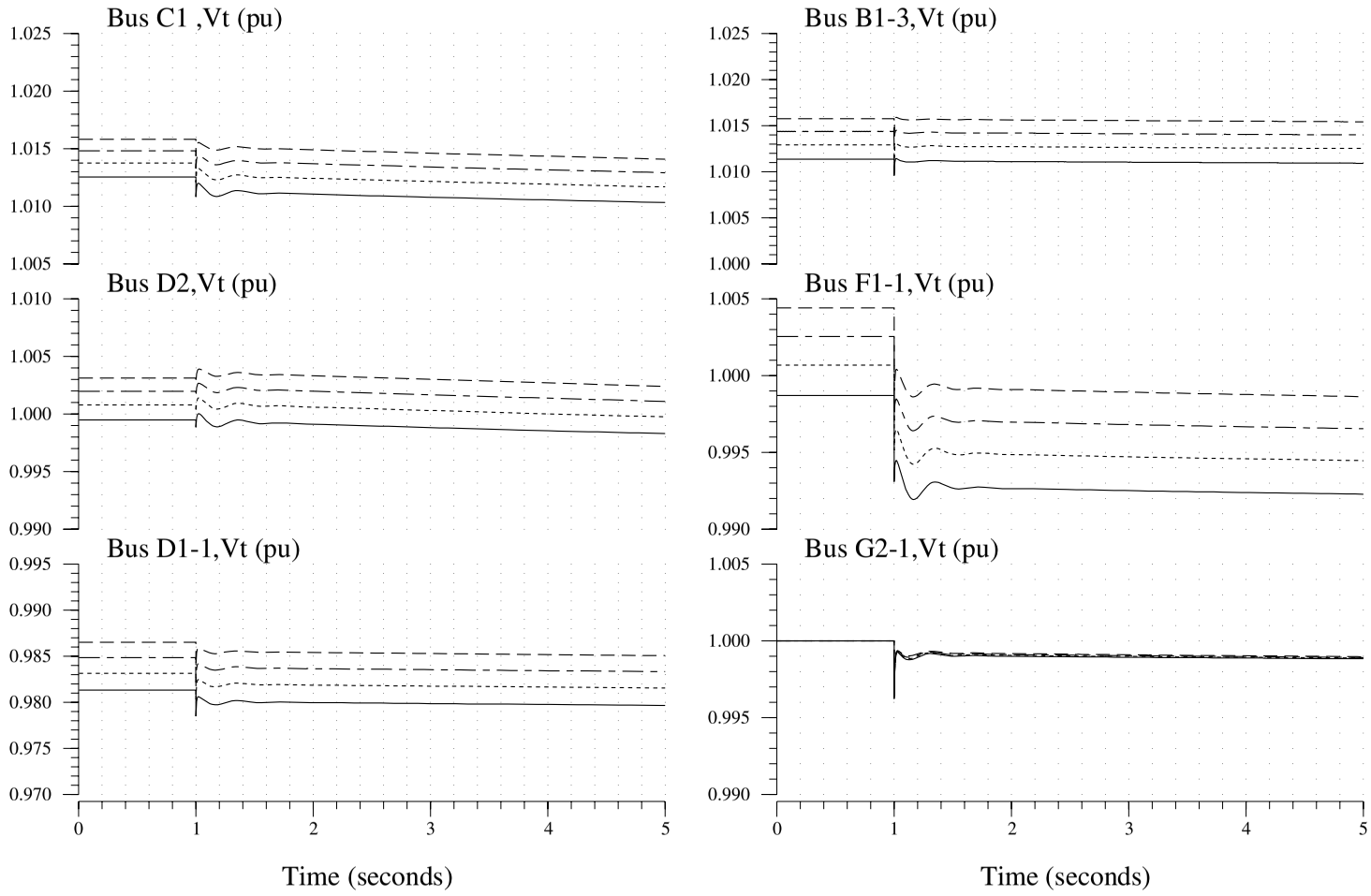
System 2: Frequency Regulation
System Quantities
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)



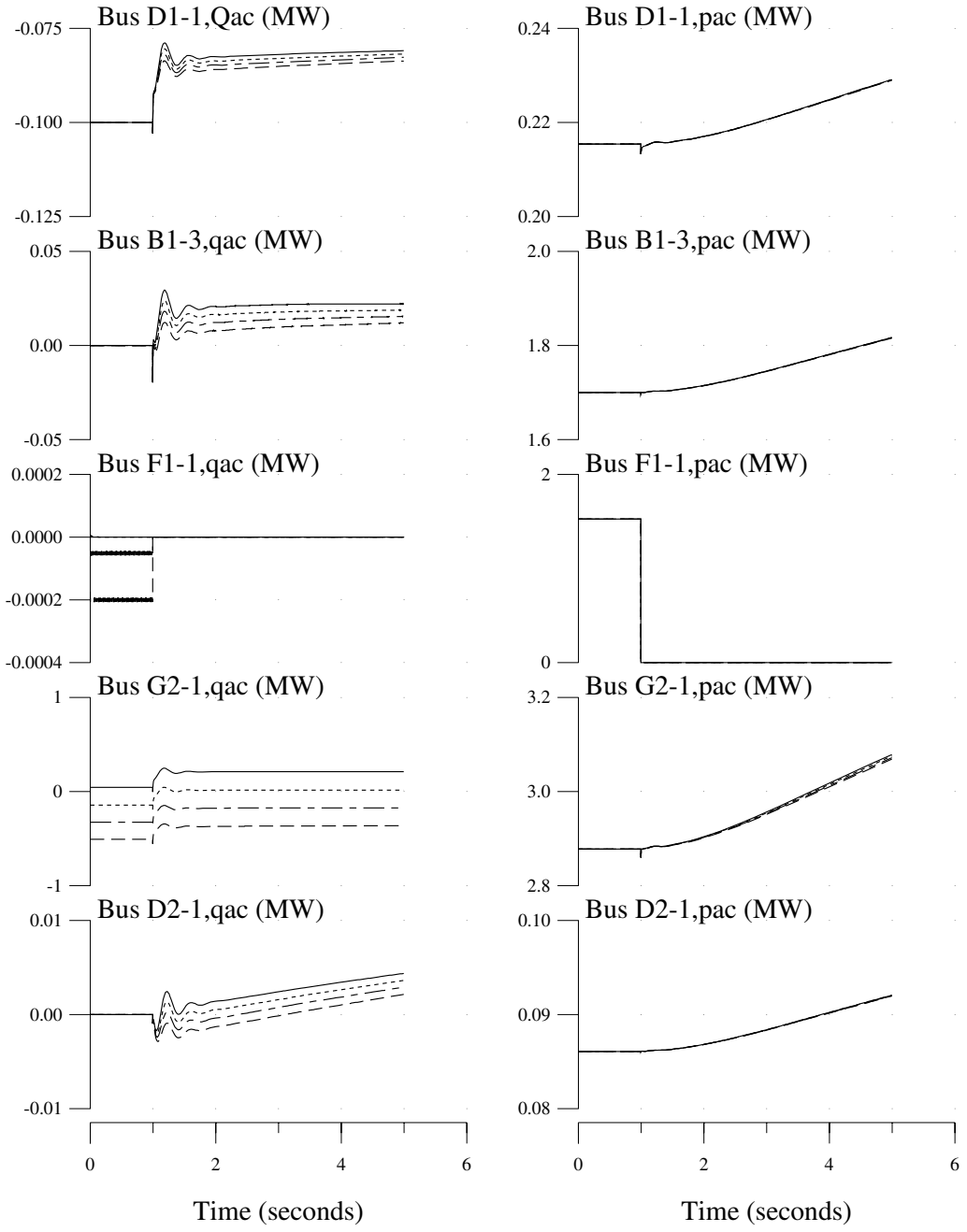
System 2: Frequency Regulation

Voltages

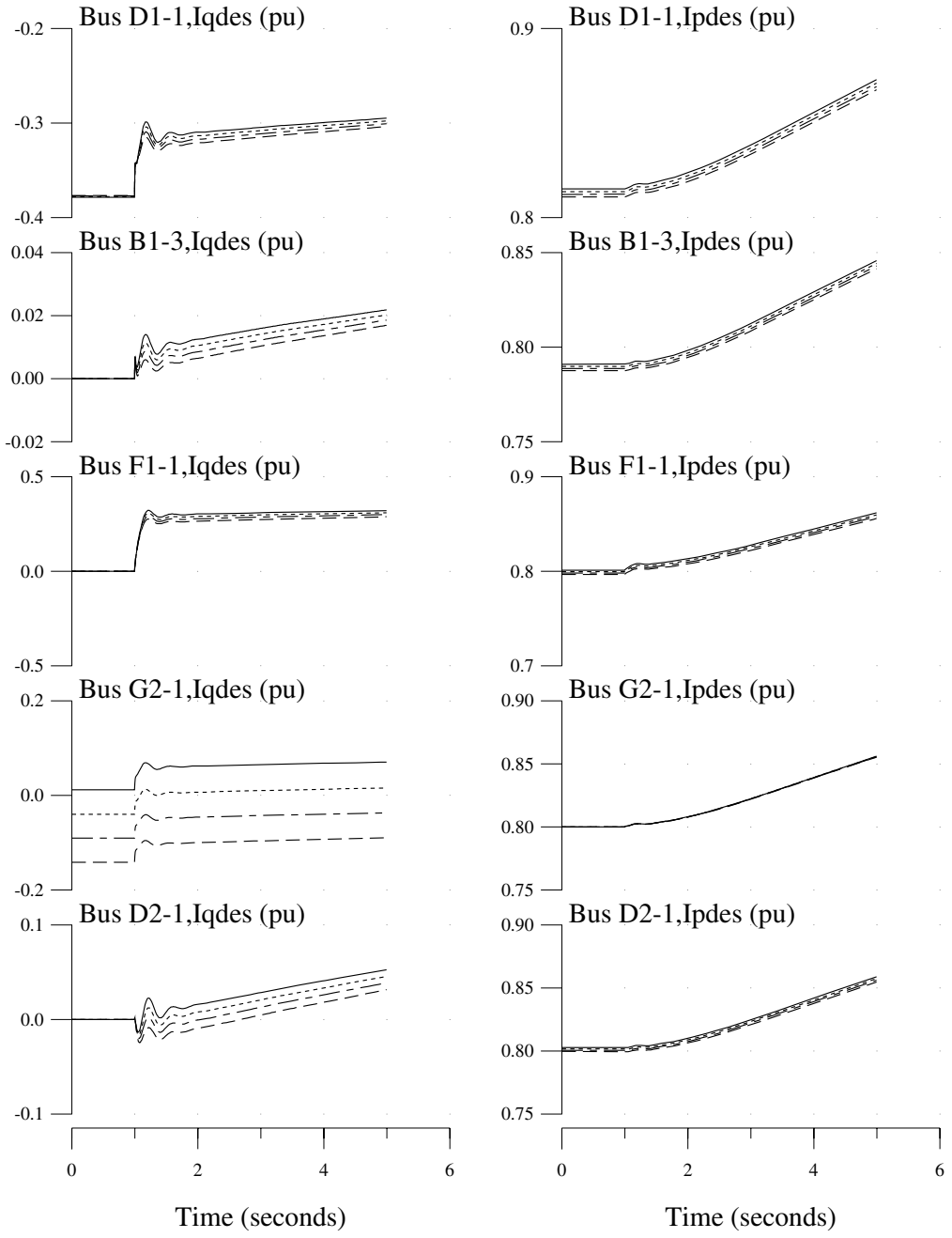
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(- - -)



System 2: Frequency Regulation
DG Active and Reactive Power
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)



System 2: Frequency Regulation
DG Control signals
Initial power from the external grid +2MW(____),+1MW(- -),+0MW(__ _ __),-1MW(__ __),isl(___ ___)

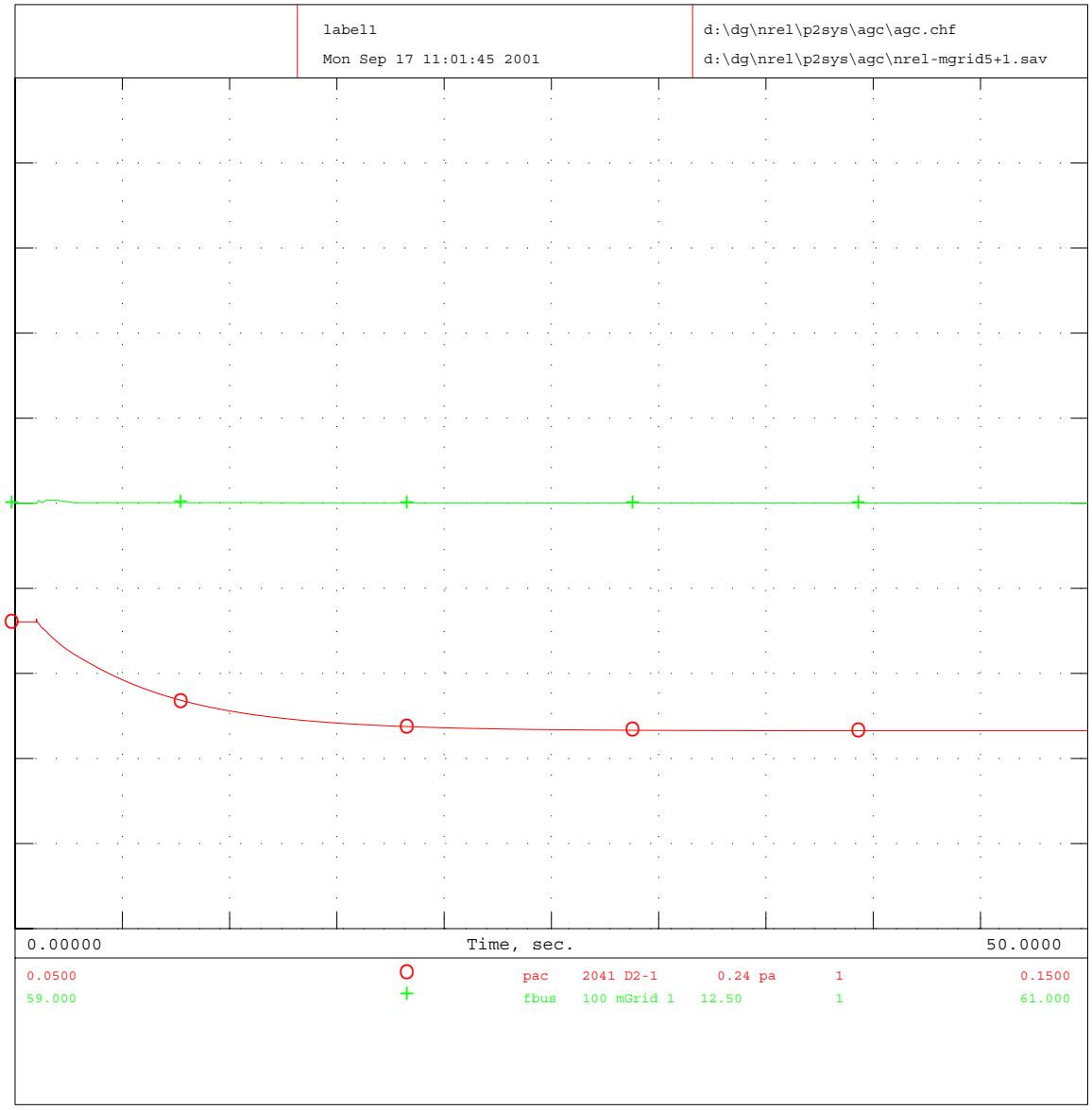


SEPARATOR 5: P2 SYSTEM CONFIGURED AS A MICRO GRID WITH SUPERVISORY CONTROL

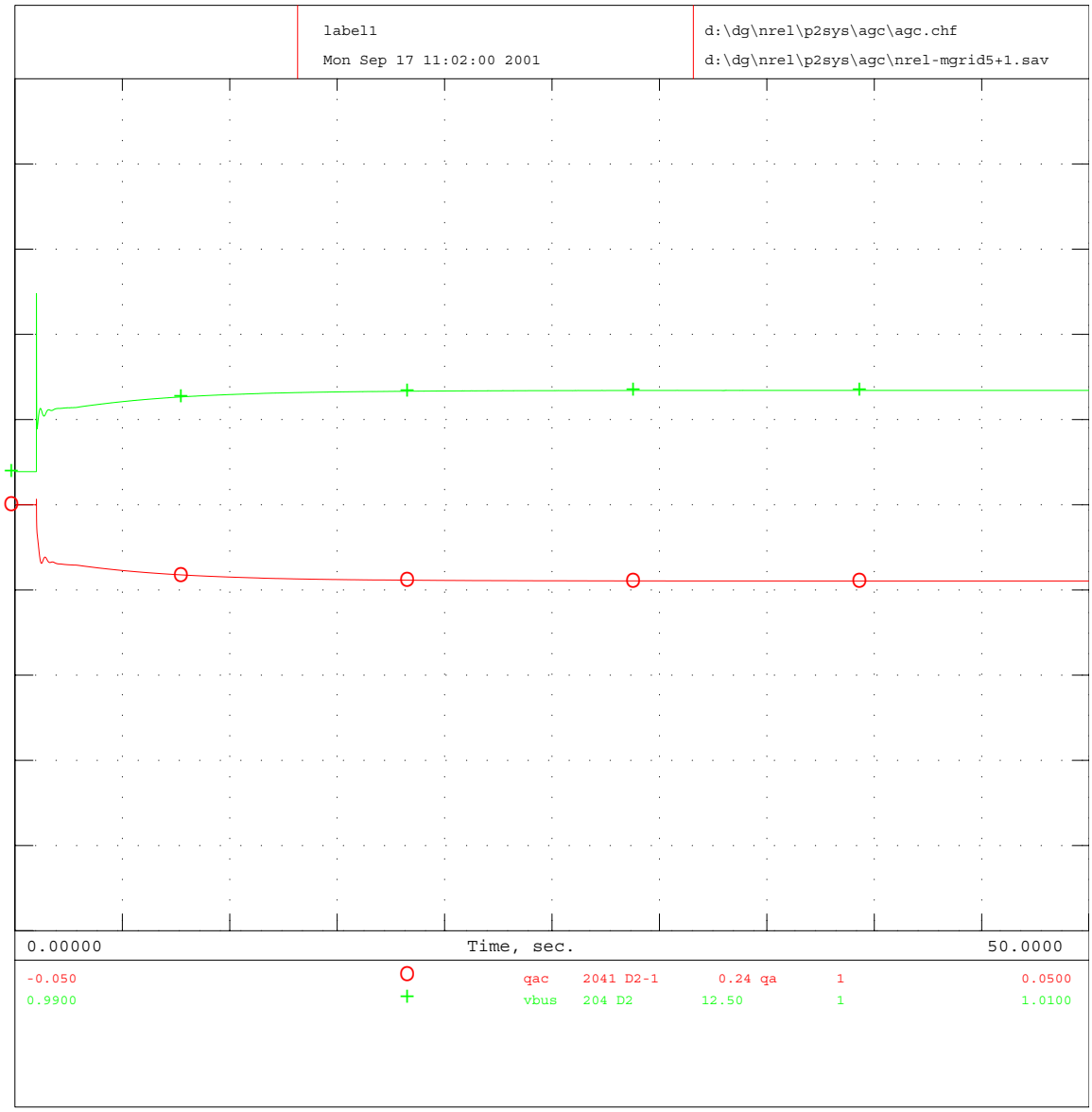
All Inverter Based DGs with Voltage and Frequency Regulation
Response to Trip of a Load on the Microgrid

First Page - 2 Traces:
Green Trace: System Frequency
Red Trace: Active Power of DG on bus D2

Second Page – 2 Traces:
Green Trace: Bus Voltage
Red Trace: Reactive Power of DG on bus D2



Load Trip
System 2
Trip loads at buses 201 and 2071



Load Trip
System 2
Trip loads at buses 201 and 2071

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

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1. REPORT DATE *(DD-MM-YYYY)*
08-2003

2. REPORT TYPE
Subcontract

3. DATES COVERED *(From - To)*

4. TITLE AND SUBTITLE
DG Power Quality, Protection and Reliability Case Studies Report

5a. CONTRACT NUMBER
NAD-1-30605-01

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
GE Corporate Research and Development

5d. PROJECT NUMBER
SR-560-34635

5e. TASK NUMBER
DP03.1001

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
GE Corporate Research and Development
One Research Circle
Niskayuna, NY 12309

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
NREL/SR-560-34635

12. DISTRIBUTION/AVAILABILITY STATEMENT

13. SUPPLEMENTARY NOTES

14. ABSTRACT
This report summarizes various distributed generation-electric power system interconnection cases studied by conducting simulations using a virtual test bed.

15. SUBJECT TERMS
distributed generation; case studies; virtual test bed; interconnection; interconnection interface; DG; distributed power; distributed energy resources; DER; Distribution and Interconnection R&D; National Renewable Energy Laboratory; NREL; GE

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
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