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Investigation of Electrical Activity of Dislocation and Grain Boundary in Polycrystalline Float Zone Silicon

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Investigation of Electrical Activity of Dislocation and Grain Boundary in Polycrystalline Float Zone Silicon

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ABSTRACT

In this paper, the charge carrier recombination behavior of grain boundaries(GBs) and intra-grain dislocations in high purity polycrystalline float-zone(FZ) silicon were studied by electron beam induced current (EBIC), laser microwave photoconductance decay (PCD) and preferential etching/Normaski optical microscopy. It was found that the lifetime on a single wafer increased from ~10µs to 100µs as the average grain size varied from 100µm to several millimeters, while both dislocations near the surface and grain boundaries produce a strong EBIC contrast at room temperature. Since the near surface dislocation EBIC contrast disappears with increasing space charge probe depth, i.e., diode bias, the electrical activity is not likely to be intrinsic to the grown crystal, but due to contamination introduced during chem-mechanical polishing. However, the "clean" grain boundaries continue to act as strong recombination centers.

1. Introduction

Dislocations and grain boundaries are intrinsic extended defects in polycrystalline silicon. It is known that they generally act as recombination centers and decrease the minority lifetime of PV material. Since the recombination intensities of dislocations and grain boundaries are strongly influenced by process-induced or deliberate decoration with transition metals [1-4], it is important to know how "clean" dislocations or grain boundaries behave. In this paper, a high purity FZ crystal grown at NREL was examined electrically by EBIC and microwave-PCD measurements, with the results being correlated with preferential etching/Normaski microscopic observations. Examining these defects in pure materials provides a baseline for learning more about their interactions with impurities and comparing with the more highly contaminated sheet or thin film silicon.

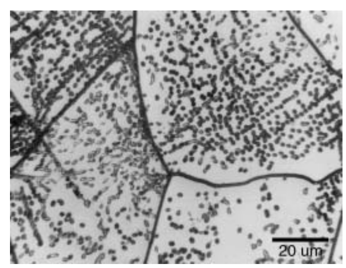
2. Experiment:

A FZ crystal was grown at NREL under conditions that deliberately induced the formation of polycrystalline grains. The samples were Ga doped with a concentration of 2.8×10^{15} cm^{-3}, as determined from C-V measurements. The grain size within a given wafer ranged from ~100 microns to several millimeters. Aluminum Schottky diodes were prepared on the chem-mechanical polished surface. EBIC measurements were performed at room temperature with an accelerating voltage of 20 KV and a probe current of about 0.2 nA. Following EBIC measurements, the Al contacts were striped off and the samples were Secco etched and examined with a Normaski optical microscope.

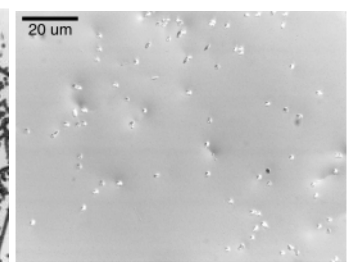
Microwave PCD lifetime mapping was performed on the double side polished wafers. Before measurement, samples were boiled in a Piranha solution. During PCD mapping, the wafer was immersed in a 5% HF solution to passivate the surface. The step size used for generating the lifetime map was 0.8 mm. A 904 nm GaAs laser with a Si penetration depth of ~30 µm was used as a carrier injection source. After PCD measurements, the sample was Secco etched for 1 min. A photo was taken with a digital camera to record the grain size distribution for correlation with the lifetime distribution map.

3. Results and Discussion:

The etching/optical microscopy revealed that the dislocation density and the grain structure in the polycrystalline FZ samples were usually very inhomogeneous, see Figs. 1(a)-(c), which show the variety of dislocation densities (from zero to over 10^6 cm^{-2}), and grain sizes (from 0.1 to several mm in diam), that can occur on the same wafer.



(a)



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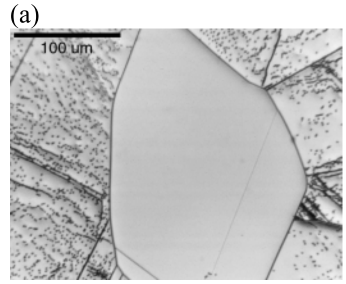
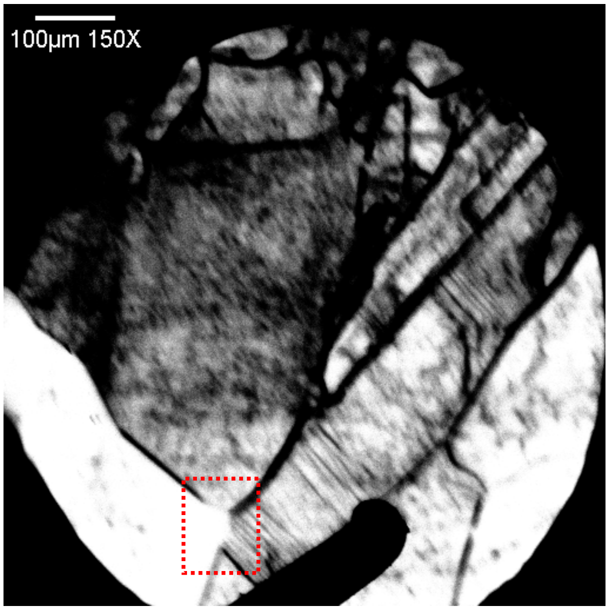


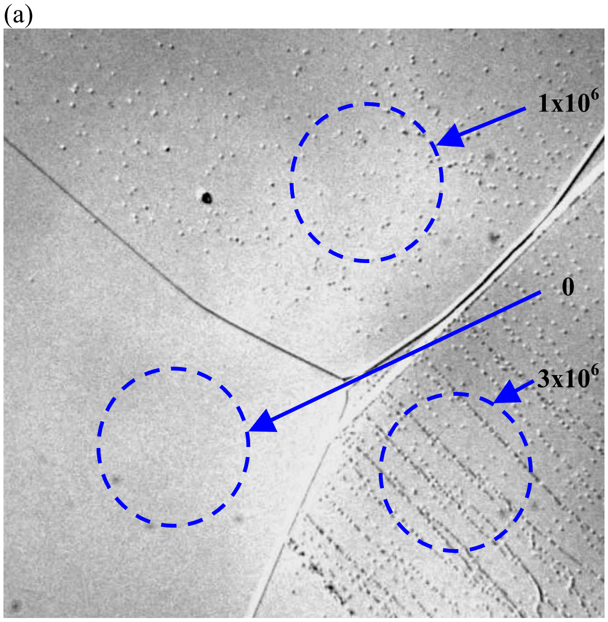
(c)

Fig. 1. Nomarski images (a) in a small grain region, (b) within a large grain, and (c) a dislocation-free grain. The sample was Secco etched for 1 min.

The recombination behavior of the different grains was studied by fabricating Al Schottky diodes on grains with different dislocation densities. Figure 2 compares the EBIC and corresponding optical microscope images of a diode. Note that a density of $\sim1\times10^6$ cm^{-2} dislocations yields a gray contrast, implying a decrease in the lifetime relative to the white contrast of the adjacent dislocation-free grain. Since it has been shown that clean dislocations in epitaxial silicon layers are electrically inactive at room temperature [1-2], the high contrast observed is likely due to metal contamination of the near surface region. This has previously been demonstrated at NCSU [5] to be due to the impurities introduced during chem-mechanical polishing of the wafer, since bias dependent imaging to investigate deeper volumes of the sample shows that the dislocation contrast disappears.



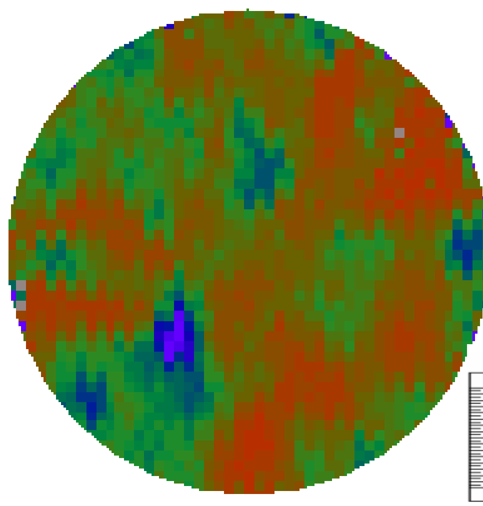
(a)



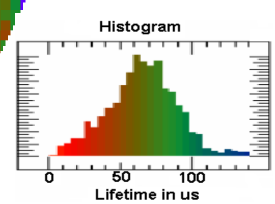
(b)

Fig. 2. EBIC (a) and corresponding Normaski (b) images of the boxed region. Dislocation densities (in cm^{-2}) for different regions were indicated in figure (b).

Additional evidence was obtained from the generally high values of minority carrier lifetime obtained by mapping the PCD across an entire wafer, as shown in Fig. 3, which correlates the grain boundary recombination with the corresponding macro-photo taken after polishing and etching. A convenient bright contrast occurs in the photo of Fig. 3(c) due to the scattering from the grain boundaries. Thus, dark regions correspond to a large grain region with less recombination, and vice verse. It was found that the lifetime increased form ~10µs to 100µs as the grain size varied from 100µm to several millimeters. The lifetime of the small grain region, i.e., less than 20µs, was mainly limited by the grain boundary recombination. Since the penetration depth of the GaAs laser is about 30µm, the lifetime measured here may be considered as the bulk lifetime, with possible contamination of the near surface region accounting for only a small part of the lifetime variation. It is apparent that the grain boundaries and their associate lattice distortions act as strong recombination centers. This is consistent with the results of Ciszek [4], they found that lifetime decreases with decreasing grain area, from 200 µs at $2x10^{-2}$ cm^2 grain area to 4 µs at $5x10^{-4}$ cm^2 grain area in high-purity silicon. However, since the dislocation density is usually high in the small grain region, see Fig. 1(a)-(b), the lifetime variation might also relate to the dislocation distribution.



(a)



(b)

(c)

Fig. 3. PCD lifetime map (a) and corresponding picture (c) of a poly FZ wafer. The histogram of the lifetime mapping is shown in (b). The wafer diameter is 22mm.

4. Conclusion:

The recombination behavior of clean dislocations and grain boundaries in high purity polycrystalline float-zone silicon were studied by EBIC, PCD and Normaski optical microscopy. It was found that both dislocations and GBs gave rise to strong EBIC contrasts at room temperature. PCD measurements showed that the lifetime increased form ~10μs to 100μs with the grain size varying from 100μm to several millimeters. While the dislocation EBIC contrast is likely due to contaminations introduced during chem-mechanical polishing, it was straightforward to conclude that clean grain boundaries acted as strong recombination centers, considering the relative large laser injection depth used in PCD measurements.

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