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APIVT-GROWN SILICON THIN LAYERS AND PV DEVICES

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ABSTRACT

Large-grained (5-20 μm) polycrystalline silicon layers have been grown at intermediate temperatures of 750°-950°C directly on foreign substrates without a seeding layer by iodine vapor transport at atmospheric pressure with rates as high as 3 μm/min. A model is constructed to explain the atypical temperature dependence of growth rate. We have also used this technique to grow high-quality epitaxial layers on heavily doped CZ-Si and on upgraded MG-Si substrates. Possible solar cell structures of thin-layer polycrystalline silicon on foreign substrates with light trapping have been examined, compared, and optimized by two-dimensional device simulations. The effects of grain boundary recombination on device performance are presented for two grain sizes of 2 and 20 μm. We found that 10^4 cm/s recombination velocity is adequate for 20-μm grain-sized thin silicon, whereas a very low recombination velocity of 10^3 cm/s must be accomplished in order to achieve reasonable performance for a 2-μm grain-sized polycrystalline silicon device.

INTRODUCTION

One of the most attractive ways to achieve efficient and practical thin-silicon solar cells is to directly deposit large-grained poly-Si thin layers (10-20 μm) on foreign substrates at a high rate without the need for a seeding layer. Atmospheric pressure iodine vapor transport (APIVT) of silicon is based on a disproportionation reaction between SiI_2 and SiI_4. It is a non-vacuum, open-chamber deposition technique with potential for continuous processing, with low capital cost and no need for expensive effluent treatment [1].

Recent efforts on microcrystalline silicon solar cells with amorphous silicon technology have resulted in respectable efficiencies to be used as the bottom cell in a tandem structure, owing to a number of possible beneficial factors including a-Si passivating c-Si crystallites, hydrogen passivation, preferred orientation, and an intrinsic absorber. However, such cells may be difficult to make with high enough efficiencies for low-cost single junction products. In developing practical and efficient thin-silicon solar cells using the APIVT-deposited silicon layers, continued improvement in material properties and optimized device structures must be investigated. In this paper, we present our recent progress in material growth, defect passivation, and diagnostic device results. Using a 2D silicon device simulator MicroTec®, we studied the quantitative effects of grain boundary recombination on device performance in addition to possible thin-silicon solar cell structures with light trapping and optimized device designs.

POLY-SILICON GROWTH AND DEVICES

With APIVT, grains as large as 5 μm are obtained even at a temperature of 750°C [1]. As the deposition temperature is raised to 900°C, grain size increases to about 20 μm. This is about ten times the grain size achievable by a typical chlorosilane-CVD process. A 20-μm-grained poly-Si film approaches PV device quality if intragrain defects are not the limiting recombination mechanism. Passivation of intragrain defects (mostly stacking faults and twins) and grain boundaries by hydrogenation increased Hall mobility from 51 cm²/V·s to 76 cm²/V·s. After passivation, we also observed improvement in the minority carrier diffusion length from internal quantum efficiency measurement in a finished device.

Typical growth is very fast (about 3 μm/min) in a configuration with close source-substrate spacing, so that loss of silicon to the sidewall of the reactor is limited. In order to study the growth mechanism, a larger separation of source-substrate was used. Because of increased loss of silicon to the reactor wall, the growth rate was reduced to about 1 μm/min, but we gained the ability to control the substrate temperature independently of the source temperature. Data in Fig.1 show atypically insensitive growth rates to substrate temperature at a constant source temperature of 1300°C. Using a growth model that incorporates arrival of SiI_2, surface migration of SiI_2, and departure of SiI_4, we can derive the relationship between growth rate and temperature.

From Wajda and Glang's [2] calculation of partial pressures of SiI_2 and SiI_4, we use the following approximation for the partial pressures:

$$P(SiI_2) \propto T; \qquad P(SiI_4) \propto A - T^2,$$

where A is a constant and T is the substrate temperature. So pressure differences between the substrate and source locations would be:

$$\Delta P(SiI_2) \propto (T - T_{source}); \qquad \Delta P(SiI_4) \propto (T_{source}^2 - T^2).$$

If there were no correlation between SiI_2 and SiI_4, we would have,

the rate of arrival for $SiI_2 \propto -\Delta P(SiI_2)$,

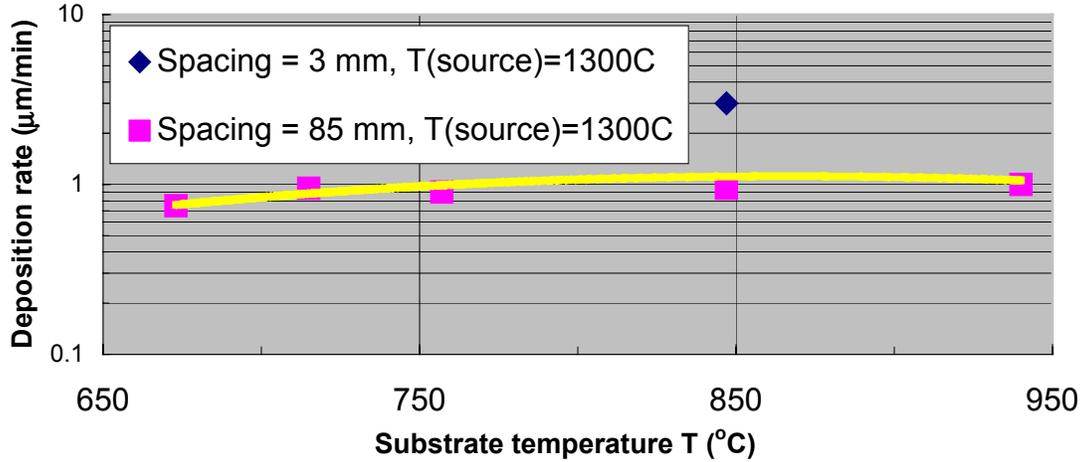and the rate of departure for $SiI_4 \propto \Delta P(SiI_4)$.

Fig. 1. Growth rate vs. temperature. The solid line is the fit by using Q=0.27 eV.

The actual SiI_2 arrival rate should also be proportional to SiI_4 departure rate. In consideration of surface migration of SiI_2 as the necessary step to find a suitable site for a silicon atom, we have the rate of deposition by the APIVT technique as:

$$R \propto (T - T_{source})(T_{source}^2 - T^2)\exp(-\frac{Q}{kT})$$

where Q is the activation energy for surface migration of SiI_2. This correlation is used in Fig.1 to fit the experimental data, resulting in a Q value of 0.27 eV. From the relationship, a simple explanation of this weak temperature dependence of growth rate is that as the substrate temperature is raised, surface migration is easier and thus the growth rate is higher. This is the normal temperature dependence as observed in a CVD process. However, as the substrate temperature is increased, the temperature difference between the source and substrate is decreased, resulting in a smaller free energy driving force and thus slower transport of silicon from source to substrate.

We fabricated a heterojunction solar cell with an a-Si emitter on a polycrystalline Si layer grown by APIVT. A relatively low V_{oc} of 0.47 V is observed [1], indicating that junction-shunting and minority-carrier recombination are still limiting the device performance. Such behavior has been widely observed on all as-grown polycrystalline silicon. Rather than bypassing this problem by doing complex single-crystal layer transfer procedures followed by a subsequent epitaxy process [3], we choose to improve the polycrystalline silicon material itself, taking advantage of the larger as-grown grain sizes compared to other available techniques. Two-dimensional device simulation on grain boundary effects will later show that grain boundary passivation can be relaxed from a recombination velocity of 10^3 cm/s to a more attainable 10^4 cm/s when the grain size is increased from 2 μm to 20 μm, in order to obtain an open-circuit voltage of 0.55 V.

Effective photon absorption for thin layer silicon solar cells is another issue of equal importance frequently addressed by many authors. However, this may not be as serious a problem as people usually think. Calculation of light absorption by silicon of the usable AM1.5 spectrum in Fig. 2 indicates that if the layer thickness is less than 30 μm, a 15% current loss compared to an optically thick cell is to be expected, at which point one should employ effective light trapping. Fortunately, internal reflection at the back interface between a silicon layer and some foreign substrates usually is effective for this light-trapping purpose. For example, in Fig. 3, a bare 30μm-thick APIVT-grown silicon layer on Corning LGA-139® glass-ceramics (with excellent coefficient of thermal expansion match with Si) reveals that only 0%-10% of incident light is transmitted through (lost by) the layer after taking into account front surface reflection and substrate absorption, as compared to a calculated loss of 15%-98% for the given thickness of silicon in a wavelength range of 850 nm-1100 nm. This translates to a current loss less than 5%. Even in this case, a reflective metal coating on the backside of the substrate would eliminate this small loss nevertheless.
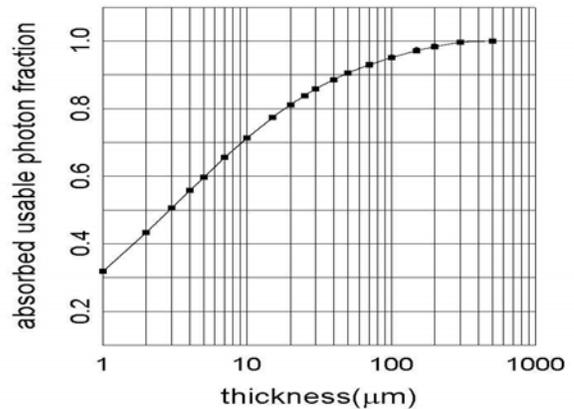

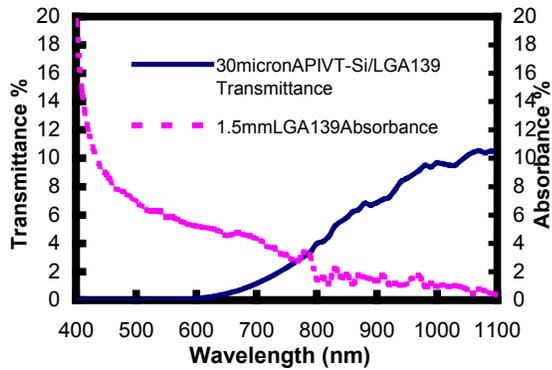Fig.2. Calculated absorption of usable AM1.5 by silicon

Fig. 3. Transmittance of a thin Si layer on LGA-139®.

EPITAXIAL SILICON GROWTH AND DEVICES

We obtain high-quality epitaxial growth on silicon substrates when a clean interface is maintained. This allows us to attain high-quality active layers on low-cost metallurgical-grade silicon substrates for solar cells or different doping layers on single crystal substrates for micro-electronic applications. Epitaxial layers also give us a measure of the solar cell performance limitations of this material independent of any grain-size effect.

A hetero-junction solar cell with an a-Si emitter was fabricated on a 20-μm thick epitaxial Si layer grown on a heavily doped single-crystal Si wafer (0.0095 Ω-cm) (Fig. 4 top). In comparison to the similarly structured device on a CZ-Si control wafer, the APIVT-grown epitaxial Si layer demonstrates a thickness-limited 23 mA/cm^2 and the same V_{oc} = 0.53 V of the CZ-Si control cell. A diffused junction device on a thinner epitaxial layer on heavily doped CZ-Si shows an even slightly higher V_{oc} of 0.56 V (Fig.4 middle). This result proves that the growth technique is capable of producing high-quality material as long as grain boundaries are not involved. Successful epitaxial growth on upgraded metallurgical-grade silicon provided by Crystal Systems, Inc., was also obtained [4]. A test device with a diffused p/n junction resulted in a less efficient cell, mostly due to poor V_{oc} (Fig.4 bottom). This might have something to do with impurity out-diffusion from the substrate because we used a relatively high temperature (~1100°C) procedure during growth. Using lower temperature below 900°C is possible for high-quality epitaxial growth, which will significantly reduce the impurity problem from an MG-Si substrate. TEM studies of the epitaxial layers on CZ-Si indicate a very low density of crystallographic
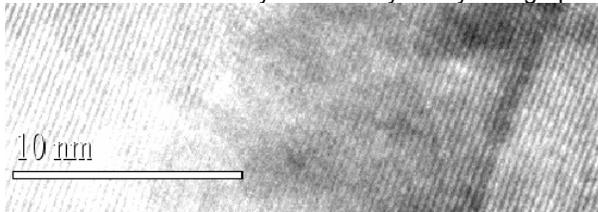

Fig. 5. High-resolution TEM image of an epitaxial silicon layer (left 4/5) on a CZ-Si substrate (right 1/5)

defects (such as stacking faults, twins, and dislocations) compared to the substrate, as shown in Fig. 5.
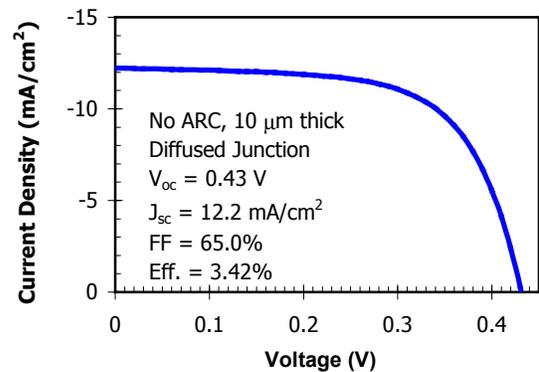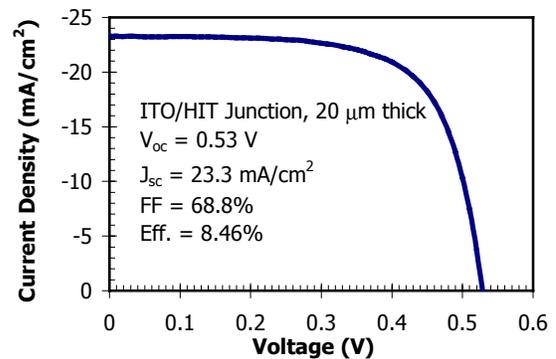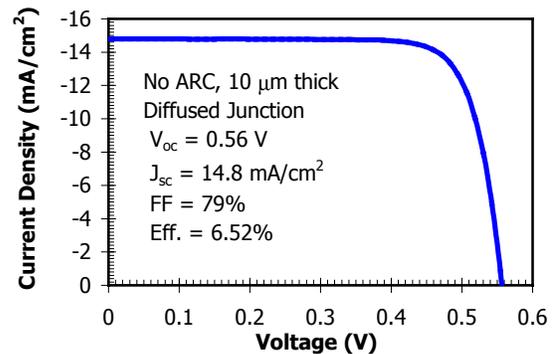

No ARC, 10 μm thick
Diffused Junction
V_{oc} = 0.56 V
J_{sc} = 14.8 mA/cm^2
FF = 79%
Eff. = 6.52%

ITO/HIT Junction, 20 μm thick
V_{oc} = 0.53 V
J_{sc} = 23.3 mA/cm^2
FF = 68.8%
Eff. = 8.46%

No ARC, 10 μm thick
Diffused Junction
V_{oc} = 0.43 V
J_{sc} = 12.2 mA/cm^2
FF = 65.0%
Eff. = 3.42%

Fig. 4. I-V curves of devices made on various epitaxial silicon layers grown by APIVT. Top: HIT cell of a 20-μm-thick layer on heavily doped CZ-Si; Middle: diffused junction of a 10-μm-thick layer on CZ-Si; Bottom: diffused junction of a 10-μm-thick layer on MG-Si.

2D DEVICE SIMULATIONS

MicroTec® is an affordable and robust 2D semiconductor process and device simulator [5] with many built-in, necessary physical models pertinent to silicon solar cells. Possible solar cell structures of thin-layer polycrystalline silicon on foreign substrates with light trap-

ping have been examined, compared, and optimized by this two-dimensional device simulation. It is used here to quantitatively examine the effects of grain boundary recombination on device performances. Fig. 6 shows a sketch of a simple $N^+/P/P^+$ thin silicon model device with a total thickness of 20 μm and an average grain size of 20 μm. The simulation domain consists of half of a grain (the shaded area). The grain boundary runs vertically across the junction on the right edge of the simulation domain. The calculated IV curves are given in Fig. 7 with recombination velocities at the grain boundary varying from 10^2 to 10^6 cm/sec. It is very clear that for a grain size of 20 μm, a recombination velocity lower than 10^4 cm/s is necessary to avoid significant loss of performance ($V_{oc} \geq 0.55$ V). This velocity, however, has to be lowered to 10^3 cm/s for a grain size of 2 μm, as shown in Fig. 8.
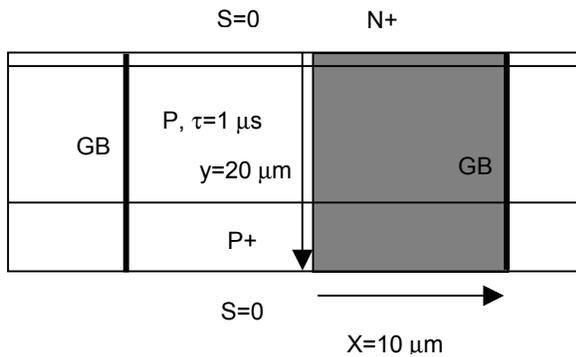

Fig. 6. Sketch of a polycrystalline silicon solar cell model having a thickness of 20 μm and an average grain size of 20 μm. The shaded area is the simulation domain.
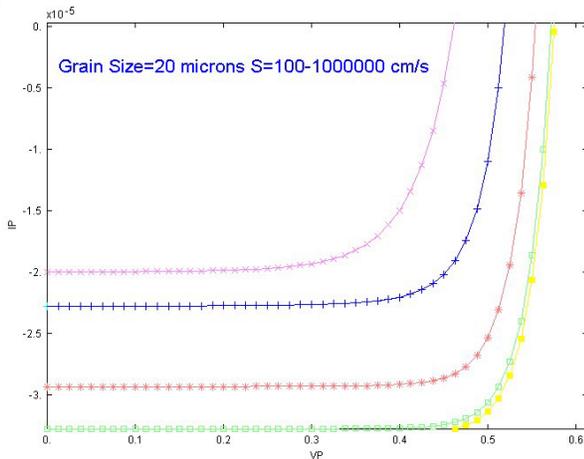

Fig. 7. Simulated IV curves for various recombination velocities at the grain boundary for a thin silicon solar cell with a grain size of 20 μm. From top to bottom: 10^6, 10^5, 10^4, 10^3, and 10^2 cm/s.

CONCLUSIONS

Large-grained polycrystalline silicon is readily deposited with a high rate by the APIVT technique. The weak temperature dependence of growth rate is explained by a growth model derived from a three-step

mechanism: arrival of SiI_2, surface migration of SiI_2, and departure of SiI_4. This technique has also been used to grow high-quality epitaxial layers on heavily doped CZ-Si and on upgraded MG-Si substrates.

The effects of grain boundary recombination on device performances were examined by two-dimensional device simulation for two cases with grain sizes of 2 and 20 μm respectively, and it is found that 10^4 cm/s recombination velocity is adequate for 20-μm grain-sized thin silicon, whereas a much lower value of 10^3 cm/s must be accomplished for a 2-μm grain-sized silicon. Passivating the grain boundaries to a recombination velocity below 10^4 cm/s seems to be a priority to achieve reasonable performances for the APIVT-grown silicon.
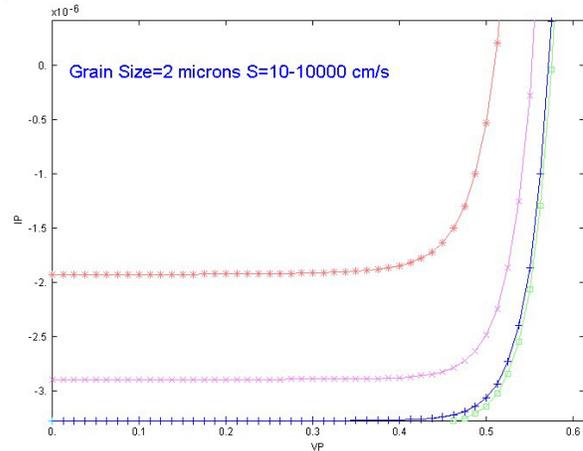

Fig. 8. Simulated IV curves for a 2-μm-grained thin silicon solar cell. From top to bottom, for recombination velocities of 10^4, 10^3, 10^2, and 10 cm/s, respectively.

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