

11th Workshop on Crystalline Silicon Solar Cell Materials and Processes

Extended Abstracts and Papers

Workshop Chairman/Editor: B. L. Sopori

Program Committee:

J. Gee, J. Kalejs, T. Saitoh, R. Sinton, M. Stavola,
D. Swanson, T. Tan, E. Weber, J. Werner, and
B.L. Sopori

*Holiday Inn
Estes Park, Colorado
August 19-22, 2001*



National Renewable Energy Laboratory

1617 Cole Boulevard
Golden, Colorado 80401-3393

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11th Workshop on Crystalline Silicon Solar Cell Materials and Processes

TABLE OF CONTENTS

Title/Author(s):	Page
Workshop Theme: <i>Emerging Technologies for Crystalline Si Solar Cells</i> Bhushan Sopori	1
<i>Intrinsic Point Defects in Silicon and Their Control in Crystal Growth and Wafer Processing</i> R. Falster and V. V. Voronkov	2
<i>The Role of Transition Metals in Solar Cell Efficiency</i> A. A. Istratov and E. R. Weber	11
<i>Optimization of Silicon Crystal Growth and Wafer Processing for High Efficiency and High Mechanical Yield</i> G. A. Rozgonyi, A. Karoui, L. Kordas, and T. Ciszek	18
<i>Lifetime Spectroscopy of FeB Pairs in Silicon</i> Daniel Macdonald and Andres Cuevas	24
<i>Electrical Behavior of Crystal Defects in Silicon Influence of a Contamination</i> M. Kittler, W. Seifert, and V. Kveder	32
<i>Restructuring of Photovoltaic R&D Programs in Japan</i> Tadashi Saitoh	40
<i>Beyond Wafers and Silicon Thin-Films: Third Generation Photovoltaics</i> Martin A. Green	48
<i>Electronic Transport in Amorphous/Crystalline Silicon Heterojunction Solar Cells</i> U. Rau, N. Jensen, and J. H. Werner	49

<i>The Impact of TC0s on Next-Generation Solar Cells</i>	57
Timothy J. Coutts	
<i>Resonance Ultrasonic Diagnostics of Elastic Stress in Silicon Wafers</i>	58
A. Belyaev, S. Ostapenko, and I. Tarasov	
<i>Handling of Crystalline Silicon Solar Cells in High Throughput Production Tools</i>	59
Julio Bragagnolo, Junichi Akita, Hisashi Sato, Yoshiro Chikaki, Tohru Hashimoto, Masafumi Ito, and Ichiro Sugiyama	
<i>Hydrogen in Crystalline Silicon for Solar Cells</i>	65
S. Martinuzzi	
<i>Investigation of Gettering Mechanisms in Crystalline Silicon</i>	73
T. Y. Tan	
<i>Lifetime Enhancement and Low-Cost Technology Development for High Efficiency Manufacturable Silicon Solar Cells</i>	80
A. Rohatgi, V. Yelundur, and J. Jeong	
<i>Silicon Ribbons – State of the Art and Results from UKN Research</i>	85
Giso Hahn, Patric Geiger, and Alexander Hauser	
<i>Protocrystalline-Microcrystalline Phase Transitions in Si:H Materials and Their Effect on Solar Cell Characteristics</i>	93
C. R. Wronski, R. J. Koval, J. M. Pearce, A. S. Ferlauto, J. Koh, and R. W. Collins	
<i>Le Châtelier’s “Principle of Moderation” and the Self-Passivation of Extended Defects in CIS Materials</i>	95
Billy J. Stanbery	
<i>Methods in Microelectronics for Rapid Thermal Annealing of Implanted Dopants</i>	102
A. T. Fiory	
<i>Rapid Thermal Processing for High Throughput Silicon Solar Cell Production</i>	114
Ralf Lüdemann, Daniel Biro, Stefan Peters, Dominik M. Huljic, and Ralf Preu	
<i>Monitoring Physical Parameters of Si Solar Cells in PV Manufacturing</i>	122
Bhushan Sopori, Yi Zhang, Roderick Faison, Jamal Madjdpour, Christian Fredrick, Peter Hacke, Dan Meier, and Juris Kalejs	
<i>Cu Metallization in Microelectronics</i>	128
Paul S. Ho	
<i>Self-Doping Silver Contacts for Silicon Solar Cells</i>	129
D. L. Meier, H. P. Davis, R. A. Garcia, J. A. Jessup, P. Hacke, S. Yamanaka, and J. Salami	

<i>Thick Film Conductor Technology for Solar Cells</i>	137
Alan F. Carroll and Richard J. S. Young	
<i>Thick Film Solutions for High Efficiency, Low Cost Solar Cell Processing</i>	145
Kristina McVicker, Tung Pham, Aziz Shaikh, and Todd Williams	
 Poster Papers	
<i>Crystal Growth and PV Devices Using a New Si Feedstock Source</i>	146
T. F. Ciszek, M. R. Page, T. H. Wang, and J. A. Casey	
<i>Novel Methods for Purifying Metallurgical-Grade Silicon</i>	150
T. F. Ciszek, T. H. Wang, M. R. Page, P. Menna, R. E. Bauer, E. A. Good, and J. A. Casey	
<i>Thin Layer Si Growth by Atmospheric Pressure Iodine Vapor Transport</i>	155
T. H. Wang, T. F. Ciszek, M. R. Page, R. E. Bauer, and M. D. Landry	
<i>Wire Surface Kinetics in Hot-Wire Chemical Vapor Deposition</i>	159
Jason K. Holt, Maribeth Swiatek, David G. Goodwin, and Harry A. Atwater	
<i>Guidelines for More Accurate Determination and Interpretation of Effective Lifetime from Measured Quasi-Steady-State Photoconductance</i>	163
J. Brody, A. Rohatgi, and A. Ristow	
<i>Impact of Copper on Minority Carrier Diffusion Length in p-Type and n-Type Silicon</i>	168
R. Sachdeva, A. A. Istratov, and E. R. Weber	
<i>Application of X-Ray Fluorescence Microprobe Technique for the Analysis of Fully Processed Solar Cells</i>	172
O. F. Vyvenko, A. A. Istratov, T. Buonassisi, E. R. Weber, and R. Schindler	
<i>Scale-Up of the CSI B-Removal Process for the Production of Solar Grade Silicon</i>	177
David B. Joyce, Chandra P. Khattak, and Frederick Schmid	
<i>Application of the Diagram Method in the Theory of Recombination Processes</i>	183
E. V. Kanaki and S.Zh. Karazhanov	
<i>Development of a Technology of Silicon Production by Recycling Phosphorus Industry's Wastes</i>	189
M. F. Tamendarov and B. N. Mukashev	
<i>Rapid ARC Formation Using a Simple and Versatile Etching Process</i>	194
C. C. Striemer, F. Shi, and P. M. Fauchet	

<i>Crystalline Silicon Technologies in CIS Countries</i>	199
D. S. Strebkov, V. Zadde, A. Pinov, K. Touryan, and L. Murphy	
<i>Quantitative Modelling of Nucleation Kinetics in Experiments for Poly-Si Growth on SiO₂ by Hot-Wire Chemical Vapor Deposition</i>	208
Maribeth Swiatek, Jason K. Holt, and Harry A. Atwater	
<i>Influence of Copper on the Carrier Lifetime of n-Type and p-Type Silicon</i>	212
K. Stewart, A. Cuevas, D. Macdonald, and J. Williams	
<i>A Compact, Contactless Lifetime Tester Using the Resonant-Coupled Photoconductive Decay Technique</i>	216
R. K. Ahrenkiel and S. W. Johnson	
<i>Calibration and Error Analysis of High Accuracy Residual Stress Polariscopes</i>	220
S. He and S. Danyluk	
<i>Gettering of Gold in H⁺ or He⁺⁺ Ion Implanted Cz Silicon Wafers</i>	221
Isabelle Périchaud	
<i>Counterdoping of p-Type Silicon by Hydrogen Ion Implantation</i>	225
D. Barakel and S. Martinuzzi	
<i>Light Induced Degradation in Manufacturable Multi-Crystalline Silicon Solar Cells</i>	229
Ben Damiani, Mohamed Hilali, and Ajeet Rohatgi	
<i>Lifetime Enhancement During Processing of Porous Silicon Cells</i>	235
M. Hilali, B. Damiani, and A. Rohatgi	
<i>Temperature-Dependent Cross-Sectional EBIC Study of Hydrogen Passivation of Defects in mc-Silicon</i>	240
O. F. Vyvenko, O. Krüger, and M. Kittler	
<i>Metallizations by Direct-Write Ink Jet Printing</i>	246
Tanya Rivkin, Alex Miedaner, Calvin Curtis, Jeff Alleman, John Perkins, Lee Smith, and David Ginley	
<i>Shunt Detection in Solar Cells with the Corescanner and Lock-In Thermography: A Comparison</i>	253
O. Breitenstein, J. P. Rakotoniaina, and A. S. H. van der Heide	
<i>Etch Pit and EBIC Correlations of High Purity Dislocated FZ Silicon</i>	257
M. C. Wagener, I. Sen, G. A. Rozgonyi, and T. F. Ciszek	
<i>In-Line Testing of Minority-Carrier Lifetime</i>	260

Ronald A. Sinton

<i>Room-Temperature Mapping of Defects in mc-Si Wafers and Solar Cells</i>	264
I. Tarasov, S. Lulu, S. Ostapenko, W. Seifert, M. Kittler, and J. P. Kaleis	
<i>Effect of Aluminum-Induced Gettering and Backside Surface Field on the Efficiency of Silicon Solar Cells</i>	265
P. S. Plekhanov, M. D. Negoita, and T. Y. Tan	
<i>Boron and Phosphorus Dopant Diffusion in Crystalline Si by Rapid Thermal Activation</i>	271
A. T. Fiory, S. G. Chawda, S. Madishetty, N. M. Ravindra, A. Agarwal, K. K. Bourdelle, J. M. McKinley, H.-J.L. Gossmann, and S. P. McCoy	
<i>Modelling Low-Temperature Diffusion of H in Si: Influence of Impurities and Defects</i>	279
Yi Zhang, Bhushan Sopori, Robert Reedy, Kim Jones, and N. M. Ravindra	
<i>Pilot Manufacturing of Dendritic Web Photovoltaic Products</i>	285
J. R. Easoz and D. L. Meier	
<i>Processing and Handling of Low Thickness Silicon Solar Cells</i>	289
J. C. Jimeno, R. Gutiérrez, V. Rodríguez, F. Hernando, F. Recart, and G. Bueno	
<i>Contact Resistance Scanning for Process Optimization: The Corescanner Method</i>	293
A. S. H. van der Heide, J. H. Bultman, J. Hoornstra, and A. Schönecker	
<i>Thin Film Silicon Solar Cells on Low Cost Glass and Glass-Ceramic Substrates: Recent Progress</i>	297
S. Krasulya and D. G. Ast	

Emerging Technologies for Crystalline Si Solar Cells

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In the last few years photovoltaic (PV) energy production has become a profitable business, and silicon continues to be the dominant technology. Silicon photovoltaic (Si-PV) manufacturers are expanding their production lines to meet the increasing market demands. As a part of the expansion, the PV industry is also developing and introducing newer technologies that are more suitable for lower-cost, large-area devices. Although PV-Si manufacturers continue to buy feedstock and Si wafers that are rejects from the microelectronics industry, there is a concerted effort to include newer cell-processing methods—methods that deviate from the traditional microelectronic device processing and are designed for PV manufacturing.

The PV industry is in the process of identifying solar-grade silicon using newer techniques to upgrade metallurgical grade Si. In the area of crystal growth, more efficient crystal-pullers and furnaces, with faster growth speeds and improved impurity control, are being installed. Wire sawing has already been a very effective cost reduction step that has allowed thinner wafers with lower kerf losses and a reduction in the damage removal. Newer approaches for wafer handling and transporting for chemical etching and texturing are being developed where the wafers essentially “float” in the chemical tanks to provide surface contact between the wafer and the etchant.

In the area of solar cell processing, the expansion of the Si-PV industry is not taking place by installing used diffusion furnaces, but by new designs of optically heated belt furnaces. Likewise, newer approaches for solar cell metallization, use of PECVD nitride for simultaneous deposition of AR coating and hydrogen passivation, and RTP-like processing methods are finding their way in the expanding PV industry. In the near future, the PV industry is likely to standardize wafers, processes, and equipment based on the new technologies that are starting to take hold.

As the Si-PV industry gears up for changing the technologies for the manufacture of solar cells, there are issues of automation and process control that are lurking over the heads of manufacturers. Wafer breakage and low mechanical yield are nagging issues in the manufacturing of solar cells. Understanding the mechanisms of breakage and automatic gentler-handling of wafers are needed to ameliorate this problem.

As a theme of this 11th workshop, we will have an opportunity to discuss these emerging technologies—related to the fundamental aspects of physics as well as challenges in engineering designs. In addition to conventional sessions related to impurities, defects, and cell processing, this workshop includes special sessions on *Si mechanical properties and wafer handling, thin film cells, and metallization*. Hopefully, these are the condiments for lively discussions on emerging technologies in solar cell manufacturing. This workshop is a Si-PV community-wide effort—by the Program Committee, speakers who devote considerable effort in preparing reviews, chairpersons/discussion leaders who guide the discussions, the poster presenters who bring in the latest research results, and the active participation of the entire audience.

Intrinsic point defects in silicon and their control in crystal growth and wafer processing

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Taking into account a wide variety of recent results from studies of silicon crystal growth and high temperature wafer heat treatments, a consistent picture of intrinsic point defect behavior is produced. The relevant point defect parameters: diffusivities, equilibrium concentrations and the details of the interaction of vacancies with oxygen are deduced. The experimental observations reviewed here include the properties of grown-in microdefects and vacancy-controlled oxygen precipitation effects in rapidly cooled wafers. These results are combined to produce a set of simple unified schematic diagrams which illustrate the key features of intrinsic point defect reaction during both crystal growth and wafer processing. This has led to a series of important engineering advances in crystal growth and wafer technologies. “PerfectSilicon” (or microdefect-free) crystal growth and “Magic Denuded Zone[®]” technology for the control of oxygen precipitation in silicon wafers are two examples of this.

1. Introduction

The study of intrinsic point defect-related agglomerates (micro-defects) and related effects in crystal growth has yielded a rich array of information on the properties of the intrinsic point defects at high temperature. The incorporation of intrinsic point defects into a growing crystal and their subsequent agglomeration into larger defects is controlled by the details of how the crystal was solidified and subsequently cooled. Interstitial and vacancy type microdefects occur in two clearly defined modes of growth. A threshold (or critical) growth rate for the change-over from interstitial-type A/B swirl-defects to vacancy-type D-defects was found to be proportional to the near-interface axial temperature gradient G [1,2]. In other words, the type of grown-in microdefects is controlled simply by the ratio v/G . Swirl-defects are formed if v/G is below some universal critical ratio ξ_t and D-defects are formed otherwise. This simple ‘ v/G rule’ holds both for float-zoned and Czochralski-grown crystals [3], in spite of a great difference in the oxygen content. The physical meaning of this rule is very simple [1]: the type of intrinsic point defects incorporated into growing crystal is controlled by the parameter v/G , according to the defect transport equations for diffusion, convection and annihilation of point defects in the vicinity of the interface.

2. Point defect reactions during crystal growth

Vacancy mode. Growing a crystal at $v/G > \xi_t$ results in incorporation of vacancies while the interstitial concentration is undersaturated and decays fast due to recombination with vacancies. The vacancies agglomerate into voids (D-defects) on further cooling – if

the vacancy concentration is not too low [3]. The identification of D-defects with octahedral voids was recently demonstrated [4,5]. The voids, though of low density (ca. 10^6cm^{-3}) and small size (c.a. 150nm), can cause large yield problems in the manufacture of some high density integrated circuits, in particular DRAMs. The main problem is a gate oxide failure which can result from the intersection of such a void with the polished silicon surface. Other void-related problems are found in device isolation [6].

At low vacancy concentration void formation is suppressed, and oxide particles are produced instead of voids from supersaturated vacancy solution [3]. At still lower vacancy concentration even the vacancy consumption is suppressed, with the consequence of appreciable residual vacancy concentration which can greatly enhance oxygen precipitation [7,8]. For these reasons the main vacancy region (that containing voids) is surrounded first by a marginal particle band (P-band) and further by a band of enhanced oxygen precipitation (L-band). Particularly the P-band is often manifested as a so called OSF-(oxidation-induced stacking fault) ring in oxidized wafers.

Fig. 1 is a kind of vacancy “map” which illustrates the problem of the incorporation of vacancies into a growing crystal. Starting at the equilibrium concentration at the melt temperature ($C_v^*(T_m)$), the vacancy concentration is reduced as the crystal cools through a transient phase in which vacancy and self-interstitial fluxes complete with each other via mutual annihilation. Eventually this stops when the concentration of self-interstitials becomes exhausted. At this point an essentially constant concentration of the surviving species (vacancy) is obtained. It is the survived vacancy concentration, set at high temperature by the v/G rule, which is then launched into the

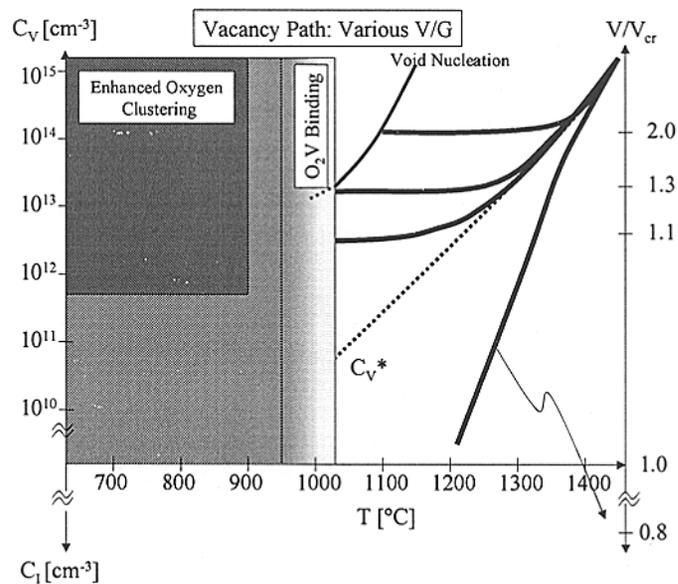


Fig. 1. An illustration of the incorporation of vacancies into a growing crystal at various values of v/G relative to the critical value.

possible reactions at lower temperatures. The reference value of the ratio of the actual to critical v/G value is given on the right hand scale for several examples. The value for each example corresponds to the value at the vacancy concentration saturation value.

Interstitial growth mode. Growing a crystal at $v/G < \xi_t$ results in incorporation of self-interstitials while the vacancy concentration is undersaturated and decays rapidly. The resulting supersaturated self-interstitials agglomerate into A/B-swirl-defects. The A-defects were found to be extrinsic dislocation loops [9]; these are considered to be even more dangerous microdefects than voids. The B-defects seem to be small globular clusters of interstitials [10] (most likely, including carbon interstitials). Particularly, at low interstitial concentration only B-defects are formed. At still lower concentrations, no detectable defects are formed. Accordingly, the main interstitial region of a crystal (that containing A-defects) is surrounded with a band of B-defects.

Void reaction control. One approach to an engineering improvement of the microdefect problem is to grow crystals in the vacancy mode but to engineer the reactions which produce voids. It is found that the resultant density of voids is proportional to the factor $q^{3/2} C_V^{-1/2}$ [3], where q is the cooling rate at the temperature at which the reaction occurs and C_V the local concentration of vacancies (a function of v/G parameter). The void reaction occurs over a very narrow temperature range (about 5K) at some 'nucleation temperature' which depends on C_V [3]. The range of typical nucleation temperatures lies between about 1000 and 1100 °C [7, 11, 12]. Fig. 2 shows an example of the path taken by vacancies through void formation and subsequent vacancy consumption for a specific v/G condition.

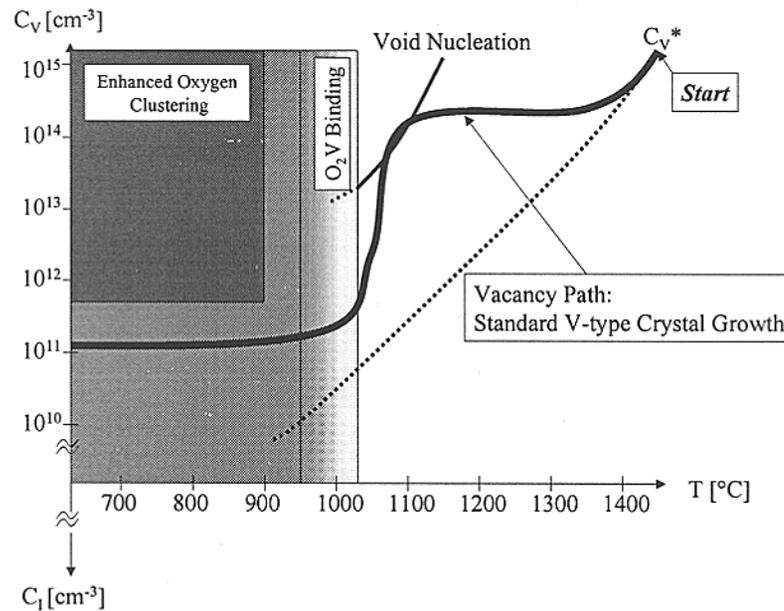


Fig. 2. An illustration of the production of voids in a growing crystal in the most usual case.

The problem of reducing void defect density is thus a coupled engineering problem. One must engineer simultaneously the coupled problems of the incorporation of vacancies near the growth interface (v and G at about the melt temperature) and the cooling rate at the reaction temperature (v and G at a temperature which depends on C_V).

Coupled to the coupled problem described above is the precipitation of oxygen which is also strongly dependent on vacancy concentration. In fact, vacancies come to completely dominate the initial clustering of oxygen which ultimately leads to

precipitation when their concentration exceeds about 10^{12} cm^{-3} . This is illustrated in the diagrams by the region marked “enhanced oxygen precipitation”. This fact is used to great effect in the MDZ[®] process described below. But it can also have a huge impact in defect distributions resulting from crystal growth. During crystal growth, if the consumption of vacancies to voids is not efficient (for example in the case of rapid cooling) then the residual concentration of vacancies can be large enough to enter this region. Such an effect had been called “anomalous oxygen precipitation”. It is illustrated in Fig. 3. Such precipitation enhancement is also the main cause of much of the observed banding phenomena in silicon near the critical value of v/G .

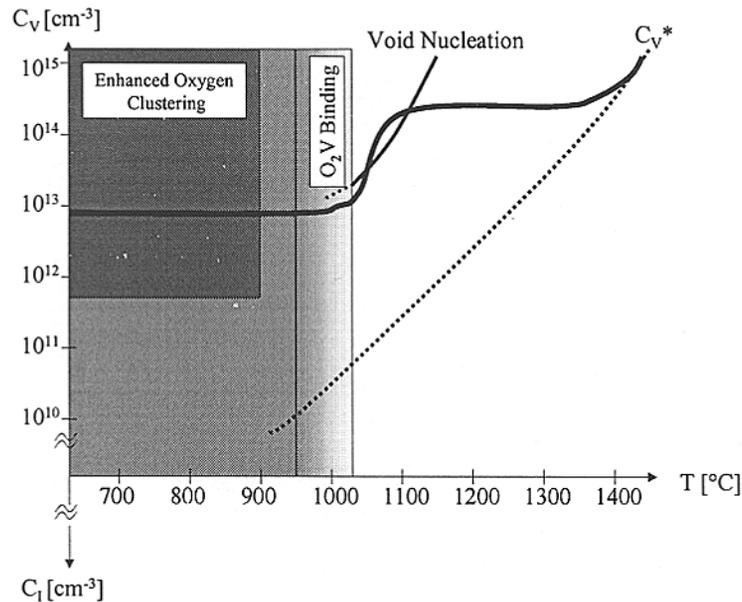


Fig.3 An illustration of the effect of more rapid cooling through the void growth regime resulting in “anomalously” high values of oxygen precipitation. Here the cooling rate is sufficiently fast such that vacancy consumption by voids is insufficiently fast to suppress the concentration below the critical value for “enhanced clustering”.

Perfect Silicon. A more robust solution to the micro-defect problem and one which circumvents the question and resultant complications of whether or not the material is sufficiently improved to meet the needs of an arbitrary IC process is not to control the micro-defect reaction, but to suppress it. As described above, there exist two marginal bands straddling the transition from vacancy to interstitial type silicon in which the reactions which produce micro-defects do not occur. In these regions, the concentrations of either vacancies or self-interstitials are too low to drive the reactions during the cooling of the crystal. They differ in character due to the differing effects of unreacted vacancies or interstitials on the subsequent nucleation of oxygen clusters at lower temperatures. Excess vacancies enhance the clustering, while excess interstitials suppress it. In terms of process control, the width in v/G space around the critical value which produces sufficiently low concentrations of both vacancies or interstitials is on the order of 10%. Growth processes which can control v/G to within 10% around the critical value both axially and radially are capable of producing microdefect-free silicon. This is

not an easy task. Methods exist which result in the partial relaxation of this requirement such that the production of such "Perfect Silicon" is practically possible along nearly the entire crystal length.

3. The control of oxygen precipitation through the engineering of vacancy concentration in silicon wafers: the Magic Denuded Zone[®] wafer

The control of the behavior of oxygen in silicon is undeniably one of the most important challenges in semiconductor materials engineering. In the 20 or so years since the discovery of the internal gettering effect in silicon wafers, many scientists and engineers have struggled with the problem of precisely and reliably controlling the precipitation of oxygen in silicon which occurs during the processing of wafers into integrated circuits. This has been met with only partial success in the sense that the "defect engineering" of conventional silicon wafers is still, by in large an *empirical* exercise. It consists largely of careful, empirical *tailoring* of wafer type (oxygen concentration, crystal growth method, and details of any additional pre-heat treatments, for example) to match the *specific* process details of the application to which they are submitted in order to achieve a good *and* reliable Internal Gettering (IG) performance. Reliable and efficient IG requires the robust formation of oxygen precipitate free surface regions (denuded zones) and a bulk defective layer consisting of a minimum density (at least about 10^8 cm^{-3} [13]) oxygen precipitates during the processing of the silicon wafer. Uncontrolled precipitation of oxygen in the near surface region of the wafer represents a risk to device yield. The basis of the conventional method for dealing with the creation of such a layered structure has been to insure sufficient out-diffusion of oxygen from the near surface region in order to suppress nucleation and growth. In recent years due to radical reductions in the total thermal budgets of processes which make submicron devices, this is no longer possible, except at large added cost.

But there is another way [14]. In the discussion above dealing with vacancy incorporation in crystal growth, it was noted that there exists a region of vacancy concentration accessible through crystal growth in which no microdefects are formed but in which the clustering of oxygen is significantly enhanced. It is also possible to achieve such levels of vacancy concentration in *thin wafers* through the proper control of their heating and cooling. In fact, it is possible, through the judicious control of point defect generation, injection, diffusion and recombination to install vacancy concentration profiles into silicon wafers which result in the ideal precipitation performance for Internal Gettering (IG) purposes. Such ideal vacancy profile means a high vacancy concentration in the wafer bulk and a proper vacancy depletion in the near-surface region. The installation of controlled concentration profiles of vacancies is now a manufacturing process.

While high concentration of vacancies enhance oxygen clustering, it is found that there is a lower bound on vacancy concentration for which clustering is "normal". This is quite a sharp transition and lies around about $5 \times 10^{11} \text{ cm}^{-3}$. Thus a profiled vacancy concentration allows for the programming of "layered" structures, just what is required for the effective engineering of IG structures. This is the basis underlying the "Magic Denuded Zone[®]" (or MDZ[®]) wafer [14]. A schematic of this new materials processing technique is shown in Fig 4. The use of such a *vacancy-based* approach greatly simplifies the use of silicon by decoupling the formation of the IG structure from the

details of the crystal growth process, the oxygen content of the wafer and the details of the thermal process used to fabricate the device in question.

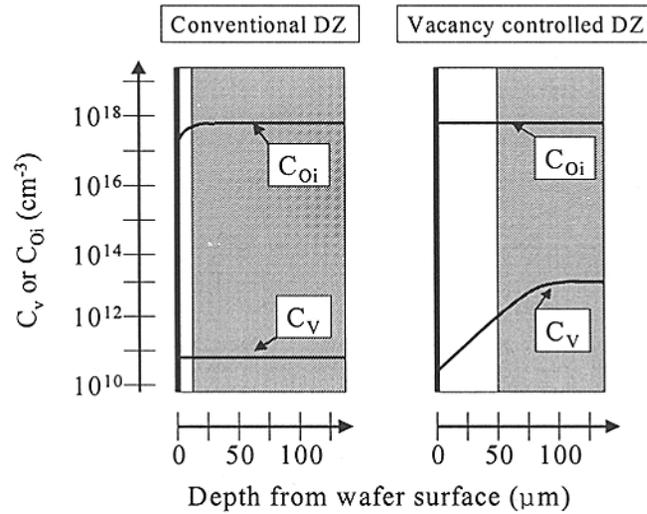


Fig 4. Schematic comparison of conventional and the vacancy controlled denuded zone. The shaded regions are those of subsequent high levels of oxygen precipitation.

The installation of vacancy concentration profiles in thin silicon wafers. The installation of appropriate vacancy concentration profiles in a thin silicon wafers is a three step process, all of which occur in a single Rapid Thermal Processing (RTP) step [14]. 1) When silicon is raised to high temperatures, vacancies and interstitials are spontaneously produced in equal amounts through Frenkel pair generation, a very fast reaction. At distances far removed from crystal surfaces we thus have $C_I = C_V = \{C_I^*(T)C_V^*(T)\}^{1/2}$, where T is the process temperature. Were the sample to be cooled at this point the vacancies and interstitials would merely mutually annihilate each other in the reverse process of their generation. 2) In thin wafers however the surfaces are not far away and this situation changes very rapidly. Assuming equilibrium boundary conditions (not oxidizing or nitriding) leads to coupled fluxes of interstitials to the surface and vacancies from the surface ($C_I^*(T) < C_V^*(T)$ (the equilibrium concentrations) for the temperature ranges of interest (see below)) and the rapid establishment of equilibrium conditions throughout the thickness of the wafer. Experiments suggest that this occurs very rapidly – in a matter of seconds or even less. This equilibration is primarily controlled by the diffusivity of the fastest component, the self-interstitials, since the concentrations are roughly equal. 3) Upon cooling, two processes are important: direct recombination of vacancies and interstitials, and diffusion toward the surfaces. In the wafer bulk the slower vacancies are now the dominant species of the coupled diffusion and hence the equilibration processes toward the equilibrium state at the surface is not as fast as the interstitial dominated initial equilibration. It is thus possible to freeze in excess bulk vacancies at not unreasonable cooling rates (ca.50-100°C/s). The residual bulk concentration of vacancies following recombination with interstitials, C_V , is the initial difference $C_V^* - C_I^*$ (at the process temperature, T). Closer to the surfaces C_V is lower due to out-diffusion (again now primarily controlled by the dominate vacancies) toward the decreasing equilibrium values at the wafer surface. The level of bulk precipitation is controlled by the process temperature, through $C_V^* - C_I^*$, while the depth of the denuded

zone is controlled by the cooling rate, through the diffusion of vacancies during cooling. Such information, coupled with numerical simulation of the diffusion process, can be very important points of reference in analysing the parameters of the native point defects in silicon. For example, the difference in the equilibrium concentrations, $C_V^* - C_I^*$ is $5-8 \times 10^{11} \text{ cm}^{-3}$ at about $1175 \text{ }^\circ\text{C}$ while at about $1250 \text{ }^\circ\text{C}$ much higher value is found, about $2-5 \times 10^{12} \text{ cm}^{-3}$. Further experiments with various cooling rates and subsequent relaxation rates of an installed profile during a second RTP process at a different temperature give insight into the diffusivity of vacancies at various temperatures. Such information gained from such experiments can be coupled with information gleaned from crystal growth experiments to compile a unified picture of the point defect parameters at high temperatures [15, 17]. Figure 4 illustrates both the installation of vacancy concentration profiles and the local oxygen precipitation achieved by it. Data of platinum diffusion experiments ($C_{Pt} \lambda C_V$ for the 730°C diffusion [16]), oxygen precipitate depth profile and a vacancy concentration profile simulation for the heat treatment using the parameters (a unified set from the combination both crystal growth and wafer heat treatment data) shown in Table 1 [17].

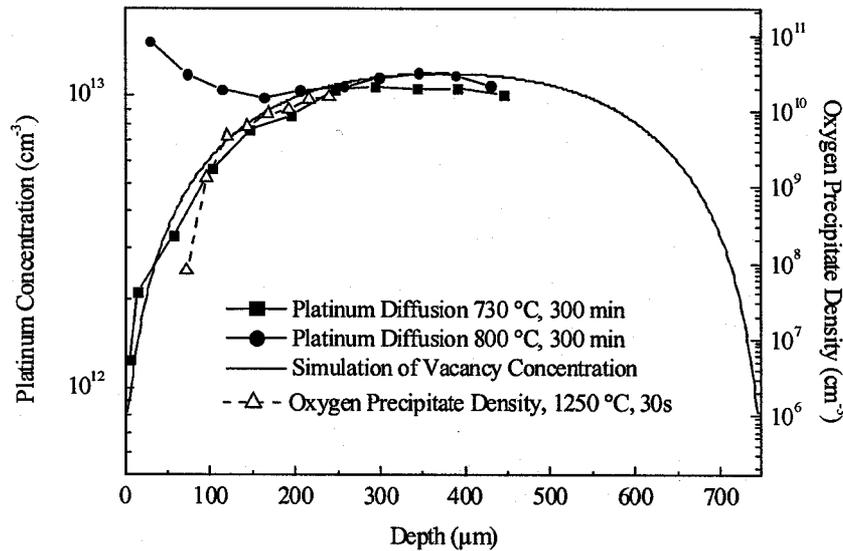


Fig. 4. Depth profiles of platinum diffusion profiles measured at 730 and 800°C , calculated vacancy concentrations, and measured oxygen precipitate densities in an RTP treated sample processed at 1250°C . The oxygen precipitate density axis is scaled to correspond to the vacancy-precipitate density calibration.

Parameter	Melting point value	Activation energy (eV)
C_V^*	$1. \cdot 10^{15} \text{ cm}^{-3}$	4.5
C_I^*	$7.7 \cdot 10^{14} \text{ cm}^{-3}$	4.7
D_V	$7. \cdot 10^{-5} \text{ cm}^2 \text{ s}^{-1}$	0.35
D_I	$3. \cdot 10^{-4} \text{ cm}^2 \text{ s}^{-1}$	0.25
K_{IV}	$10^{-11} \text{ cm}^3 \text{ s}^{-1}$	1.0

Void parameters: $C_{Void} = 3 \cdot 10^6 \text{ cm}^{-3}$; $R_{Void} = 55 \text{ nm}$

Oxygen binding: $T_{Bind} = 1070 \text{ }^\circ\text{C}$; $E_{Bind} = 5 \text{ eV}$

Table I: Point defect parameters used for the vacancy profile calculations

The rules governing vacancy-interstitial reaction and diffusion are the same for wafer processing as they are for crystal growth. Fig 5 shows a schematic diagram of the installation of vacancy concentration profiles in the RTA processing of thin wafers in the same format as that used to describe crystal reactions.

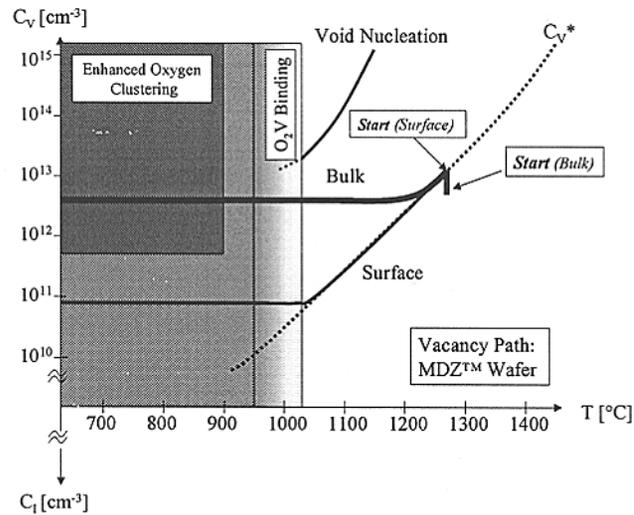


Fig. 5. An illustration of the use of the vacancy template to illustrate the creation of dual zoned precipitation effects in thin silicon wafers (the MDZ[®] wafer) by means of high temperature rapid thermal processing.

4. Conclusions

A unified picture of point defect behavior can be derived from the data on grown-in microdefects and the vacancy profiles created in wafers by RTP. The basic points are

- (1) The equilibrium vacancy concentration is slightly higher than that of self-interstitials, at least at temperatures over 1150°C. This basic inequality allows for (a) vacancy incorporation into growing crystal at v/G over some critical value (b) installation of vacancy profile in RTP-treated wafers to ensure MDZ[®] formation.
- (2) The interstitial diffusivity is essentially higher than that of vacancies. In consequence of this inequality, (a) the self-interstitials are incorporated into growing crystal at low v/G when the diffusion becomes more important than convection, (b) equilibration of point defect profiles is very fast at the RTP temperature but not as fast during subsequent cooling, to ensure desired installed profile of vacancies.
- (3) Recombination rate of vacancies and interstitials is very fast at $T > 1150^\circ\text{C}$. This condition is equally important both in defect incorporation during growth (to account for the v/G rule) and in fast installation of vacancy profile in wafers.

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The role of transition metals in solar cell efficiency

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Abstract: this article is a short summary of results obtained in the framework of the research program, supported by the NREL subcontract XAF-8-17607-04

The production of solar panels grows at a steady rate of 25% per year. The advantages of photovoltaics (PV) are well known: solar generators are environmentally-friendly, do not consume natural resources, and can be installed either at centralized power plants or on the roofs of individual houses. However, the use of photovoltaics is limited by high cost of the systems and consequently high cost of the generated electricity. The only way to decrease the cost per kW of power output is to develop the technology to manufacture cells with high efficiency from low cost wafers. A large effort was invested in the development of cost-efficient technologies for the growth of multicrystalline silicon substrates suitable for photovoltaics. These technologies are primarily based on rapid solidification, when silicon is pulled or casted preferably in the shape of thin substrates (to avoid the costly and material-consuming step of sawing the crystal) at a much higher pulling rates than utilized for normal CZ or FZ growth. Unfortunately, the minority carrier diffusion length of multicrystalline silicon, the primary parameter that determines the efficiency of solar cells, proved to be much lower than in single crystalline silicon. Additionally, it varied significantly from grain to grain. Gettering and passivation treatments were very efficient in further improving the diffusion length in good grains, but were either less efficient or not efficient at all in improving "bad" grains, i.e., grains with initially low diffusion length.

Crystalline (such as CZ or FZ grown) and multicrystalline substrates differ from single crystalline (such as CZ or FZ grown) wafers in a significantly higher metal content in mc-Si silicon and much higher density of lattice defects, including grain boundaries, dislocations, and microscopic structural defects. The concentration of metals is higher in PV mc-Si primarily because PV technology uses faster pulling/solidification rates than single crystalline silicon technology (several cm/min as compared to several mm/min in CZ and FZ growth). Consequently, it cannot benefit from the effect of distribution of impurities between the liquid phase and the growing crystal to the same extent as CZ or FZ technology. Neutron activation analysis (NAA) studies of mc-Si used for fabrication of solar cells revealed that mc-Si contained 10^{12} cm^{-3} to 10^{15} cm^{-3} of metals, including Al, Ca, Fe, Mn, Ti [1, 2]. For comparison, high quality CZ silicon typically contains less than 10^{10} cm^{-3} of metal impurities. Metal impurities can deteriorate the lifetime both when they are dissolved and when they form precipitates at grain boundaries and dislocations. Additionally, there are data that metals form precipitates at intragranular microdefects, which were detected in mc-Si from iron precipitation [3-5] and x-ray fluorescence mapping [6] experiments, reported by our group in 1994-1996, and in TEM studies reported by Werner et al. [7] in 1997. It was shown that the precipitation rate of iron was slow in the "good grains", i.e., grains with initially high minority carrier diffusion length, while in the "bad grains", i.e., grains with initially low minority carrier diffusion length, iron precipitated at a

much faster rate. Furthermore, degradation of the minority carrier diffusion length in “bad grains” was much stronger than in “good grains” [3, 8, 9]. It was suggested that the major difference between the “bad grains” and the “good grains” was that the “bad grains” contained higher concentration of intragranular defects, which serve as efficient precipitation sites for iron [10]. Strong binding energy of metals to these defects was suggested to explain poor improvement of lifetime in “bad grains” after gettering. High density of these precipitation sites, particularly in grains with low minority carrier diffusion length, and strong binding of metals to the precipitates are thought to be the reason of the low effectiveness of standard gettering techniques. The problem of gettering in PV silicon is more challenging than in I.C. silicon since the device-active area is the whole wafer. Therefore, this subcontract was focused on gaining quantitative physical understanding of the processes involved in gettering of precipitated metals, i.e., in (1) dissolution of metal precipitates in the bulk of the wafer; (2) diffusion of metals towards gettering layer, and (3) their capture by gettering sites and competitive trapping of metals by intragranular defects in device-active region.

The work was performed at the University of California, Berkeley, using the experimental facilities at UC Berkeley Campus (including the Microfabrication Laboratory, a fully equipped semiconductor processing lab) and at Lawrence Berkeley National Laboratory (including the Advanced Light Source, a last generation synchrotron used as a high brightness source of radiation for a variety of X-ray microprobe techniques). Other techniques available to the group included Electron Beam Induced Current, Surface Photovoltage, Deep Level Transient Spectroscopy, Transient Ion Drift, and Photoluminescence. Experiments with precipitation and dissolution of metals were performed using horizontal and vertical diffusion furnaces and a unique in-house made rapid thermal annealing system with the quenching capability. The experimental work was done with participation on several graduate students, visiting scientists, and collaborators, including A.A.Istratov, H.Hieslmair, C.Flink, T.Heiser, S.A.McHugo, O.F.Vyvenko, R.Sachdeva, and S.Balasubramanian. Many ideas realized in this project evolved from discussions at the previous NREL workshops.

Two metals were studied in great detail, copper and iron. These two metals were chosen because they are often mentioned as major metal impurities in photovoltaics, and because they are good representatives for the whole group of 3d transition metals, which consist of the fast diffusing metals (which include Cu, Co and Ni) and the more slowly diffusing metals (Ti, V, Cr, Mn, Fe).

The results of our work were presented in detail at the previous NREL workshops and were published in over 30 articles in scientific journals and conference proceedings. The major results and deliverables of the subcontract can be summarized as follows:

1. The theoretical basis of Transient Ion Drift, a novel technique for detection of interstitial copper in silicon, was developed by solving a system of coupled differential equations which describe diffusion and drift of copper in depletion regions of inverse-biased Schottky diodes. The results of these theoretical studies enabled us to quantitatively interpret the nonexponential transients, observed in Transient Ion Drift Measurements [11]. TID was one of the major experimental techniques which were used for studies of Cu in silicon on the following stages of the subcontract.
2. The intrinsic and effective diffusion coefficient of copper in silicon were determined using the temperature-dependent Transient Ion Drift technique [12]. It is shown that the data of Hall and Racette [13], which were used for modeling copper diffusion in silicon for

almost 25 years, underestimate the intrinsic copper diffusivity at room temperature by 3 orders of magnitude. Our data indicated that the intrinsic and effective diffusion coefficients of copper are given by the following equations:

$$D_{\text{int}} = (3.0 \pm 0.3) \times 10^{-4} \times \exp\left(-\frac{0.18 \mp 0.01 \text{ eV}}{k_{\text{B}}T}\right) \text{ (cm}^2/\text{s)} \quad (1)$$

$$D_{\text{eff}} = \frac{3 \times 10^{-4} \times \exp(-2090/T)}{1 + 2.584 \times 10^{-20} \times \exp(4990/T) \times (N_a/T)} \quad (2)$$

where temperature T is measured in Kelvin and the boron doping level, N_a , in cm^{-3} . Note that in the case of heavily doped samples ($N_a > 10^{17} \text{ cm}^{-3}$) or in the case of *Al* or *Ga*-doped wafers one should solve a system of equations given in Ref. [12] rather than use Eq.2.

This result shows that copper can easily diffuse through the thickness of a solar cell within a few hours at room temperature.

3. The unexpectedly high diffusivity of copper at room temperature enabled us to explain the poor stability of point defects of copper [14, 15]. The kinetic barrier for dissociation of complexes of copper with other defects and impurities in silicon consists of two components, equilibrium binding energy of the complex, and the diffusion barrier which interstitial copper has to overcome to dissociate the complex. Since the diffusion barrier of interstitial copper (0.18 eV, [12]) is much lower than the diffusion barrier of the other transition metals (e.g., 0.67 eV for iron, [16]), the total kinetic barrier for dissociation of Cu complexes is also much lower than that of the other metals. Therefore, most copper complexes easily dissociate at room temperature, thus allowing copper to diffuse towards more stable sinks, such as copper precipitates or the wafer surface.
4. In collaboration with the group of Prof. W.Schröter from the University of Göttingen (Germany), the microscopic structure of copper-precipitates in silicon was investigated by Transmission Electron Microscopy and was correlated with the electrical properties of the precipitates [17]. It was found that copper precipitates form defect-like states in the upper half of the silicon band gap, between approximately $E_{\text{C}}-0.15 \text{ eV}$ and $E_{\text{C}}-0.35 \text{ eV}$. The charge state of the precipitates depends on the Fermi level position in the sample. In p-type silicon, where the Fermi level position lies below the electroneutrality level of the precipitates at approximately $E_{\text{C}}-0.2 \text{ eV}$, the precipitates are positively charged and attract electrons (minority carriers in p-Si) [17, 18]. In n-type silicon, where the Fermi level lies at or above the electroneutrality level, the precipitates are either neutral or negatively charged. This finding was instrumental in understanding the kinetics of copper precipitation and recombination properties of copper precipitates (see below).
5. EBIC and SPV measurements of the samples with high density of copper-silicide precipitates revealed their extremely strong recombination activity [19]. We suggested that the defect band, which is located close to the midgap position, provides an efficient recombination channel for minority carriers. Additionally, the positive charge state of copper-silicide precipitates in n-type silicon attracts the minority charge carriers by creating a depletion region around the precipitate and increasing the minority carrier capture cross-section to a value greater than the actual size of the precipitate. Since the DLTS spectra of copper-precipitates are extremely wide, their amplitude does not give a straightforward estimate of the actual concentration of copper precipitates. Our estimates

showed that the DLTS signal of Cu precipitates may drop below the detection limit at a concentration of copper precipitates which is still sufficient to limit the diffusion length at 30-50 μm [17, 20]. Of course, this applies to any type of precipitates, and may explain why DLTS and MCTS measurements performed on mc-Si by a large number of workers never revealed deep traps in concentrations adequate to account for the low values of the minority carrier diffusion length.

6. The electrostatic model of copper precipitation in silicon was suggested and confirmed experimentally [21, 22]. It was shown that precipitation of copper in the bulk of the wafer is unlikely at low copper concentrations because of the large nucleation barrier for the formation of Cu precipitates, which is due to (i) strong compressive strain, caused by large volume expansion [23] during the formation of copper silicide, and (ii) electrostatic repulsion between the positively charged Cu-precipitates and the ionized interstitial Cu_i^+ [21, 22]. The charge state of copper precipitates is determined by the Fermi level position, which depends on the concentration of shallow acceptors (boron) compensated by shallow donors (mainly interstitial copper). If the interstitial copper concentration exceeds the boron concentration, conductivity type inversion occurs. As soon as the Cu_i^+ concentration becomes sufficient for the Fermi level to exceed the electro-neutrality level of the precipitates at approximately $E_C - 0.2 \text{ eV}$ [17, 22], the charge state of copper precipitates changes from positive to neutral or negative, and the electrostatic precipitation barrier disappears or even changes sign to attraction. This facilitates nucleation and growth of multiple Cu precipitates in the bulk of a sample. In n-type silicon, a much lower Cu concentration is required to initiate nucleation of the precipitates since the Fermi level is close to the electro-neutrality level even for very low copper concentrations.

This result implies that copper precipitates are more likely to be observed in the n-type areas of solar cells than in p-type areas. Formation of Cu precipitates may shorten the p-n junctions and decrease the overall efficiency of the cell [24].

7. The electrostatic barrier for copper precipitation was also observed in the studies of the impact of copper contamination on minority carrier diffusion length, where a several orders of magnitude increase in the effective density of recombination sites was observed at copper concentrations necessary to initiate its efficient precipitation in the wafer bulk. In n-type silicon, the dependence of the effective density of precipitation sites on Cu concentration was nearly linear; however, the slope of this dependence was less the unity, indicating that the recombination activity of copper in n-Si is due to complexes consisting of at least several copper atoms. This implies that low levels of copper contamination will not have a pronounced effect on minority carrier diffusion length in p-type silicon and hence will not significantly limit the cell efficiency (aside from the formation of Cu precipitates in the n-type areas of the cells, mentioned above). The availability of heterogeneous precipitation sites for copper (oxide precipitates) had a mild effect on the effective density of copper-related traps.
8. A weak passivating effect of copper was observed in p-type silicon at low copper concentrations. This effect was explained by a defect reaction similar to the reaction involved in hydrogen passivation, i.e., by the formation of complexes of Cu_i with recombination active defects with a lower recombination activity than that of the defects before passivation. Although it is very unlikely that Cu passivation can replace hydrogen

passivation, experiments with copper can be used to better understand the mechanisms of hydrogen passivation in solar cells, and vice versa.

9. X-ray microprobe absorption spectroscopy studies of copper precipitates in multicrystalline silicon did not reveal any phase other than copper silicide [25, 26]. The studies of the thermal stability of copper-silicide precipitates by the same technique showed that these precipitates can be fairly easily dissolved, although their dissolution kinetics was found to be somewhat slower than expected. Thus, we obtained no indications that copper could form gettering-resistant sites in solar cells.
10. An extensive study of the literature data on iron in silicon [16, 27] showed that there are indications that iron may react with the dissolved oxygen by forming iron oxides and iron silicates. Studies of the chemical nature of metal precipitates in multicrystalline silicon, performed in collaboration with S.A. McHugo at the Advanced Light Source [25] confirmed that multicrystalline silicon indeed contains clusters of gettering-resistant iron oxides and silicates. These clusters may be responsible for dissolution-resistant metal-related intragranular defects, found in bad grains of mc-Si in the earlier studies of our group.
11. Study of the thermal stability of iron-silicide precipitates showed that these precipitates cannot be gettering resistant defects since they can be easily dissolved within less than a minute at temperatures above 800°C. Therefore, metal-silicide precipitates, which can be extremely recombination active, are unlikely to form gettering-resistant sites in solar cells.
12. The feasibility of application of the μ -XRF technique for characterization of fully processed solar cells without any chemical cleaning or surface preparation was demonstrated. It was shown that the topography of contact grid, visible in an optical microscope, secondary electron image, and XRF scans, can be used to find the areas of interest in XRF and EBIC tools, as well as in optical techniques and thermography.
13. The X-ray fluorescence technique was applied towards characterization of metal impurities at the location of a shunt in a solar cell [28]. A contamination by titanium, a slowly diffusing heavy metal, was detected at the location of the shunt. This metal can be introduced by the metal belt used on a production line. Since Ti has very low diffusivity in silicon, it is unlikely that it can be easily removed from the location of the shunt by gettering, particularly if this metal contamination was introduced on one of the last steps of solar cell fabrication.
14. A proof of principle for the possibility of in-situ identification of the chemical nature of recombination-active defects by a new technique, X-ray Beam Induced Current (XBIC), was demonstrated [29]. In this technique, an X-ray beam focused to the size on the order of a square micron hits the surface of the solar cell and generates electron-hole pairs, which can be collected by the p-n junction to obtain an EBIC-like map of the recombination activity of defects present in the wafer. On the other hand, any other X-ray microprobe technique, such as X-ray fluorescence, can be used to identify the chemical content of recombination sites observed in the XBIC scans. XBIC was successfully demonstrated in combination with XPS, and implementation of XBIC at the XRF beamline is planned in the near future.
15. An attempt to apply the TID technique for studies of nickel in silicon was made; however, no ion drift transients were observed, which indicates that nickel may be neutral at room temperature.

The summary presented shows that during the three-year span of the subcontract a major progress in understanding the physics of transition metals in silicon and their possible impact on the efficiency of solar cells was achieved. On the other hand, our findings raised a number of new questions which have to be resolved. We hope to address these questions in the next round of the NREL-sponsored research program. These questions include (but not limited to) the following issues:

1. Using a combination of XBIC and XRF, determine what fraction of recombination-active defects in a solar cell contains clusters of transition metals.
2. Determine the recombination activity of gettering-resistant metal clusters, such as metal-oxides and metal-silicates.
3. Determine what other metals, besides Fe, Cu, and Ni, are commonly found in fully processed solar cells.
4. Address in greater detail the nature of shunts in solar cells.
5. Study the kinetics of defect reactions between extended defects (dislocations and grain boundaries), dissolved interstitial oxygen, and metals during solar cell production. Determine the likelihood of the formation of gettering-resistant compounds for different growth techniques and establish a correlation of the density of these defects with crystallization rate, density of lattice defects (such as dislocations and grain boundaries), and concentration of oxygen and carbon.
6. Compare the efficiency of the available passivation techniques, including SiN passivation, for different types of metal clusters in silicon.
7. Address the problem of recombination activity of "clean" lattice defects, such as agglomerates of self-interstitials, vacancies, oxygen, and carbon.

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Optimization of Silicon Crystal Growth and Wafer Processing for High Efficiency and High Mechanical Yield

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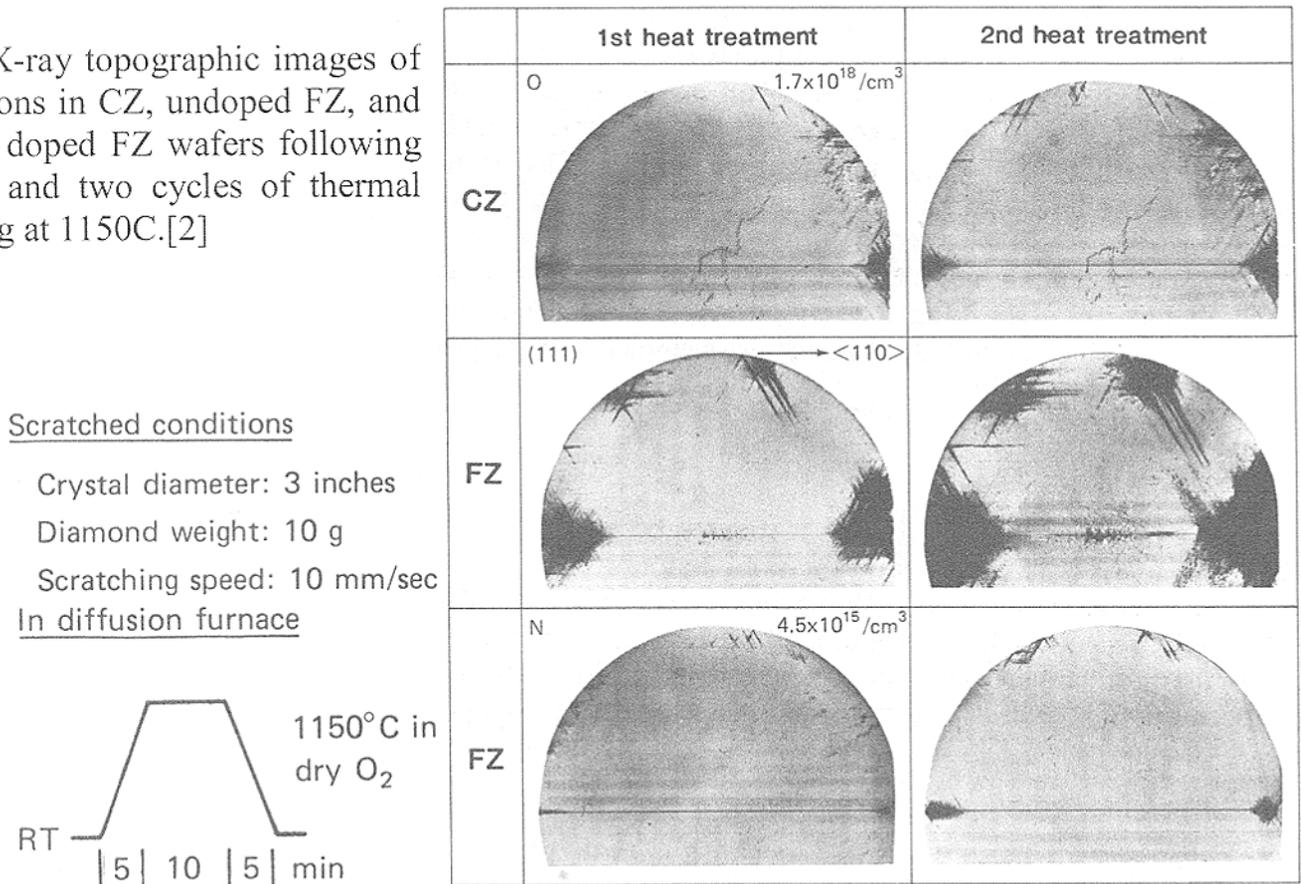
INTRODUCTION Although many aspects of the optimization of silicon crystal growth and wafer processing for producing integrated circuit(IC) devices enable improvements in crystalline photovoltaic(PV) processing, a major defect engineering difference between IC and PV substrates is related to the dominant impurity oxygen. On the one hand, low oxygen wafers from float zone(FZ) grown ingots are the purest materials with the highest minority carrier lifetime [1]. These wafers generally produce the highest efficiency planar and concentrator solar cells. However, FZ material suffers the highest yield losses due to breakage and mechanical failure, as well as performance degradation due to slip dislocations. On the other hand, controlled internal silicon dioxide precipitation gettering of high oxygen Czochralski(CZ) wafers with a tailored near-surface denuded zone, which has become the primary starting material for the IC community, also provides wafers with the best mechanical strength for the unique requirements of PV processing, e.g., texturing. Unfortunately, the CZ wafers suffer from minority carrier lifetime degradation due to bulk recombination at the oxygen precipitates, particularly if they have been decorated by metallic impurities. Thus, since breakage and yield/performance improvements are key issues for the thinner PV CZ wafers, it is important to examine the basic mechanisms and interplay between oxygen hardening, oxygen precipitation lifetime degradation, the impact of nitrogen doping, and the crystal response to the presence of metallic impurities.

The research program at NCSU has been initiated on ultra high purity CZ and FZ silicon wafers supplied by NREL and the member companies of SiWEDS, an NSF sponsored Industry/University consortium of silicon vendors and integrated circuit processing companies. This resource base has been supplemented by representative material from the PV community, and is directed towards an in-depth examination of those mechanical yield and bulk lifetime issues mentioned above. In addition, we are examining the temperature dependent electrical activity of dislocations in high lifetime, ultrapure silicon to determine the underlying energy levels associated with undecorated individual dislocations. The intent is to use these wafers to extend the study to metal impurity contaminated individual and bunched dislocation/grain boundary environments. A final and extremely important consideration is the dynamic state of point defects in those wafer regions which are dislocation free. Although extended defects and impurities in silicon are often specified to have a certain density or concentration, it is often the balance between lattice vacancies and interstitials and their mutual interaction/condensation into dislocations/voids which dictates the quality of a crystal/wafer during growth/processing.

HISTORY Float zone crystals are known to be quite vulnerable to the generation and movement of dislocations, as illustrated in the x-ray topographic(XRT) images presented in the middle pair of scribed wafers in Fig. 1 (from the work of Abe, et al[2]), following a single or double thermal cycle of 1150C. An FZ crystal strengthened by nitrogen doping to $4.5 \times 10^{14} \text{ cm}^{-3}$, see the lower pair of XRT in Fig. 1, is dramatically improved to the point where the N doped FZ

wafer is actually more resistant to dislocation formation than the CZ wafer, see upper pair of XRTs. It has been shown that nitrogen atoms and their related defect complexes are effective in enhancing the nucleation of oxynitride precipitates, which produce a dislocation locking action that is about 100 times more effective than that provided by homogeneous oxygen precipitation[3]. In addition, for low oxygen CZ crystals, which do not produce adequate precipitation for IC internal gettering, nitrogen doping will initiate a gettering action at oxynitride aggregates. This is currently a very active area of study for IC wafer production[4] for two reasons. First, since lower oxygen is achieved by reduced dissolution of quartz crucibles, this also translates into lower levels of metallic impurities. Secondly, nitrogen complexing with vacancies greatly reduces the size and density of octahedral void defects, which are a serious IC yield limiting crystal defect. This point is important in creating defect engineering options for PV applications, which will depend on balancing the vacancy/interstitial and nitrogen/oxygen concentrations such that the wafers are “hard” and charge carriers have a long lifetime.

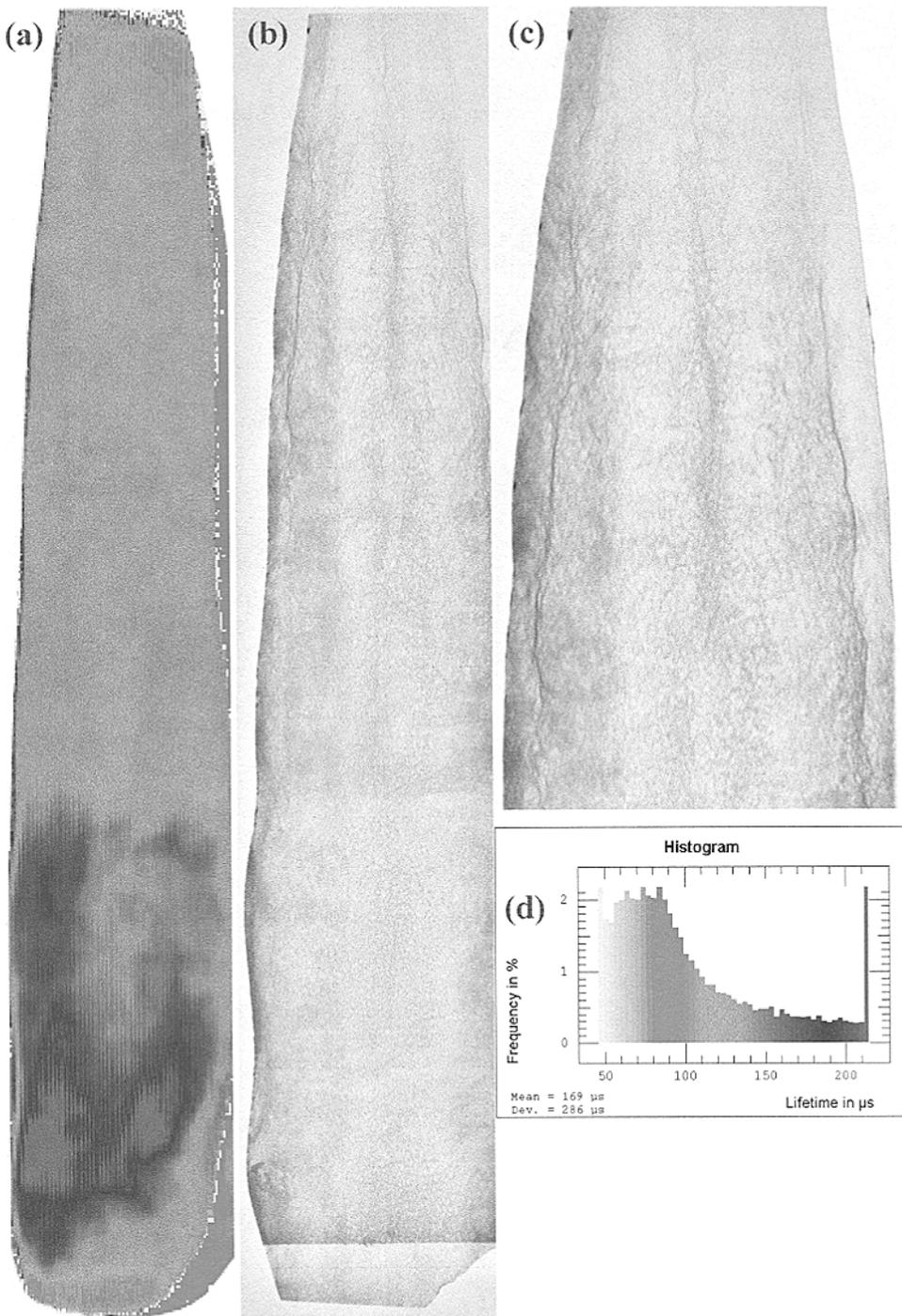
Fig. 1: X-ray topographic images of dislocations in CZ, undoped FZ, and nitrogen doped FZ wafers following scribing and two cycles of thermal annealing at 1150C.[2]



RECENT ACTIVITY Next, we present new results on electrical(recombination lifetime) and structural(dislocation density) correlations in high purity, undoped FZ crystals which serve to illustrate the diagnostic tools available and the approach underway at NCSU. Fig. 2 compares the same axial wafer from an NREL ingot examined at NCSU in a non-destructive fashion by both x-ray topography, see Fig. 2(a), and laser-microwave photoconductance decay, see Fig. 2(b). As expected, the highest lifetimes correspond to the low dislocation density areas; however, it is important to note that the average values of 50 to 100 microseconds in the heavily dislocated areas are still quite high, particularly for PV applications. This is attributed to the fact that the dislocations are “clean” in this high purity FZ crystal and relatively inactive electrically. Work is in progress to track the impact of gettering by adding controlled amounts of metallic impurities, and performing low temperature EBIC imaging and DLTS in addition to the lifetime mapping, to

examine the electrical activity of specific defects and defect free regions. It is important to note that the relatively low impact of a high density of dislocations on minority carrier recombination lifetime shown in Fig. 2, leads us to believe that the proper tailoring of SiO₂ precipitation phenomena will enable long diffusion length PV wafers to be produced which also exhibit enhanced mechanical yield behavior. Thus, the above ongoing electrical/structural approach is being extended to low oxygen content CZ wafers, as well as FZ wafers with deliberately added concentrations of oxygen. The primary thrust will be the influence of nitrogen on the nucleation of oxygen precipitates via the formation of N-V complexes. The interaction of nitrogen with vacancies and interstitials will greatly impact the size and density of precipitates, as well as the

Fig. 2: Correlation between PCD lifetime map(a) and x-ray topographic image(b) for which specific defect regions are evident in both the axial and radial directions. The PCD determined minority carrier recombination lifetime distributions are tabulated in the color-coded histogram in the lower right(d). Note that as the crystal diameter is increased the resulting change in growth conditions produces a dramatic decrease in the dislocation density and increase in the lifetime. In addition, the enlarged XRT image at the upper right(c) indicates strong radial changes in dislocation density occur. The presence of defect “lineage” is also evident just inside the ingot edge and at its center. The corresponding lifetime variations are evident in frame(a).



nucleation and motion of dislocations. The intent is to vary the oxygen content as a means to merge and examine the primary difference between FZ and CZ crystals, and the nitrogen content to increase the hardness of both systems while reducing the recombination at precipitates

PROCESSING "BONUS" DUE TO UNANTICIPATED SURFACE TEXTURE RESULTS
 Next we describe recent results on N-CZ wafers that are likely to have a positive impact on single crystal PV devices by simultaneously providing surface texturing and a near surface gettering sink for bulk impurities. An unusual defect band has been found [5] within the outer micron of the traditional defect free denuded zone in N-CZ wafers, as revealed in Fig. 3(a) by the defect density depth profile obtained by Oxygen Precipitate Profiler (OPP). The SIMS O and N profiles in Fig. 3(b) show a clear correlation of the O and N distributions in that thin surface defect band. Although Fig. 3(a) and (b) were done on materials grown in different conditions and the temperature of the nucleation step (Lo), had a 100 degrees difference, the defects appear to be due to an interaction between N and O atoms while diffusing and clustering in the vicinity of the wafer surface.

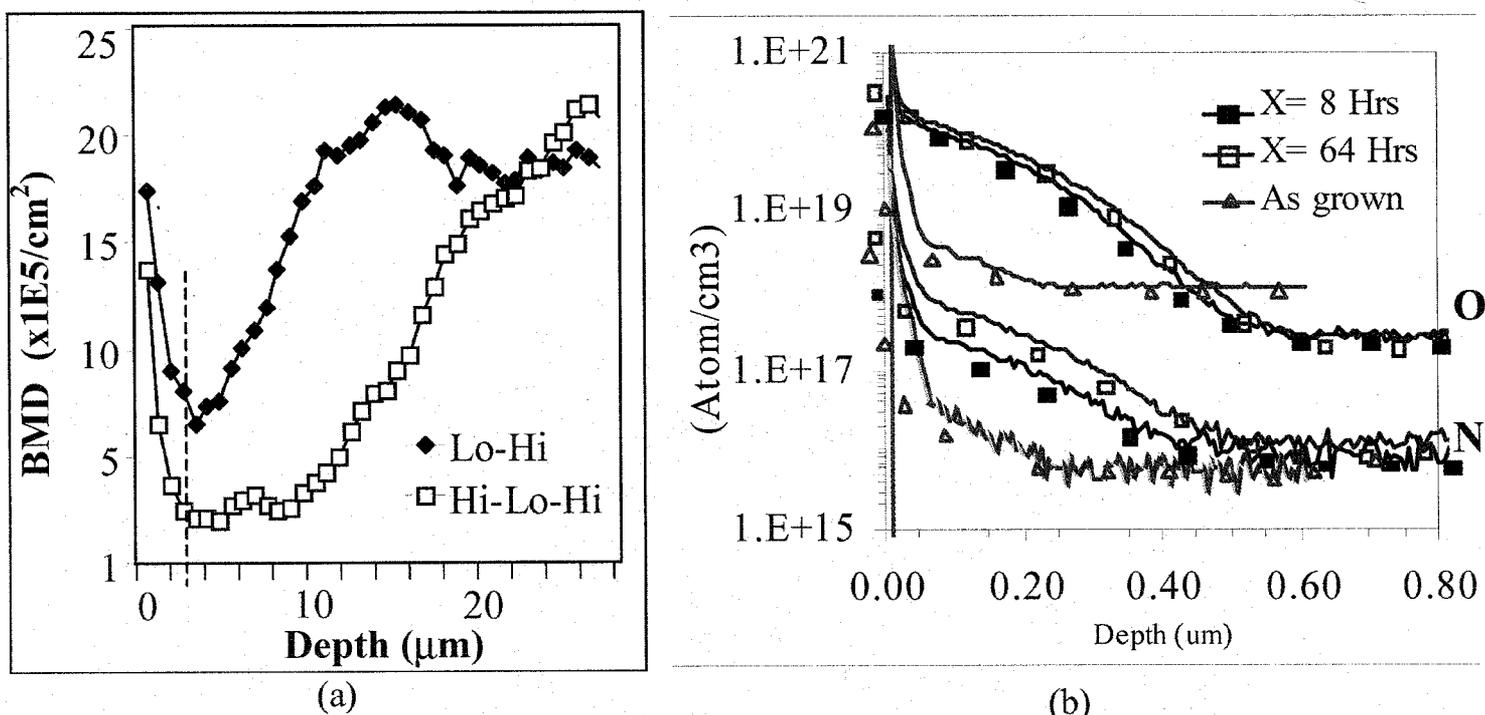


Fig. 3: (a) OPP bulk micro defect distributions of Lo-Hi and Hi-Lo-Hi heat treated N-Cz Si samples (Hi at 1250C for 1 hr, Lo at 650C for 8 hrs, Hi at 1050C for 16 hrs).
 (b) O and N SIMS profiles at the surface of an as grown and heat treated N-Cz Si samples by Lo-Hi process (750C/ X hr + 1050C/16hr).

TEM images in Fig. 4(a) and (b) show precipitates labeled (1) and (3). The unusual heavy and near surface localized oxide precipitation is accompanied by the formation of stacking faults labeled (4) and dislocations.

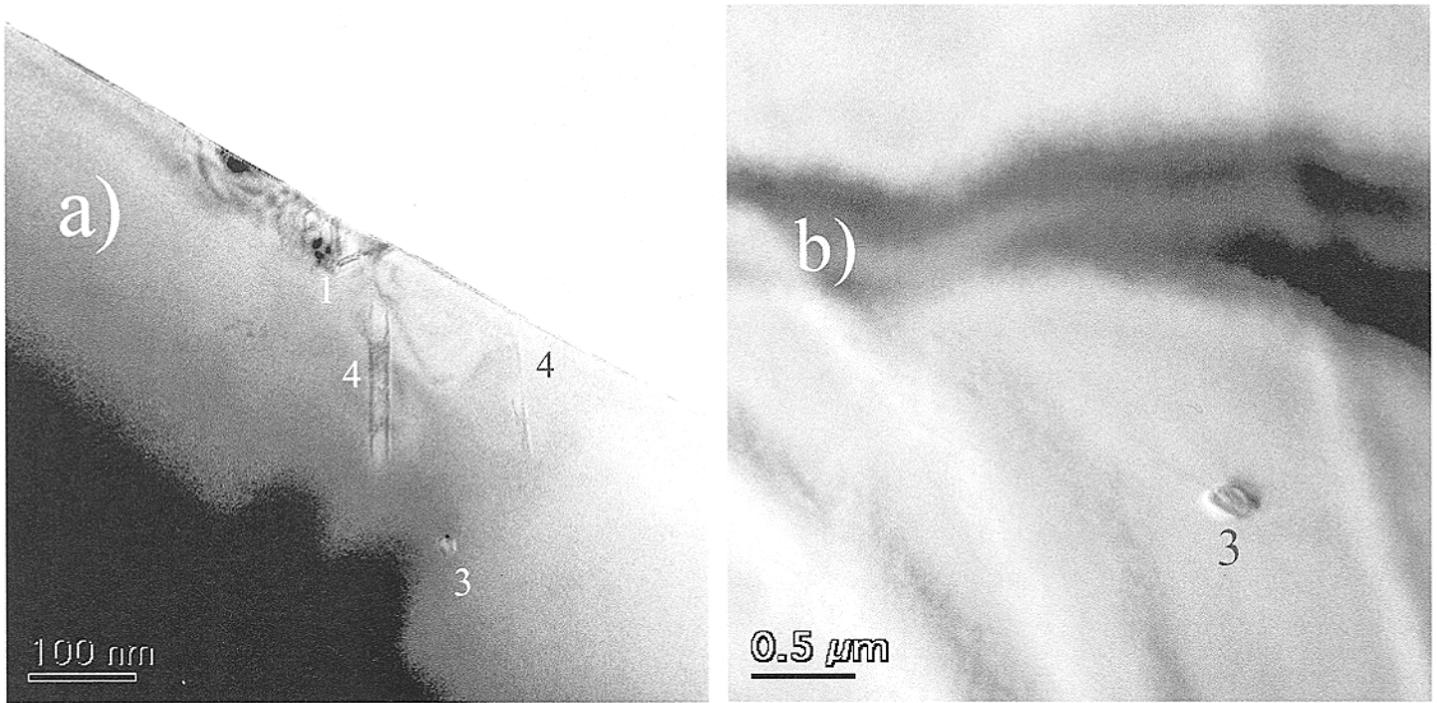
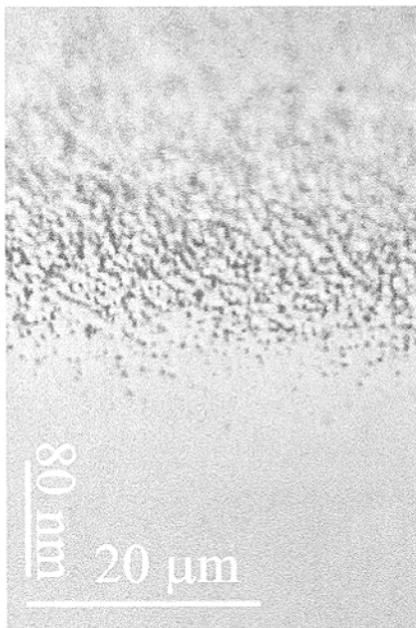
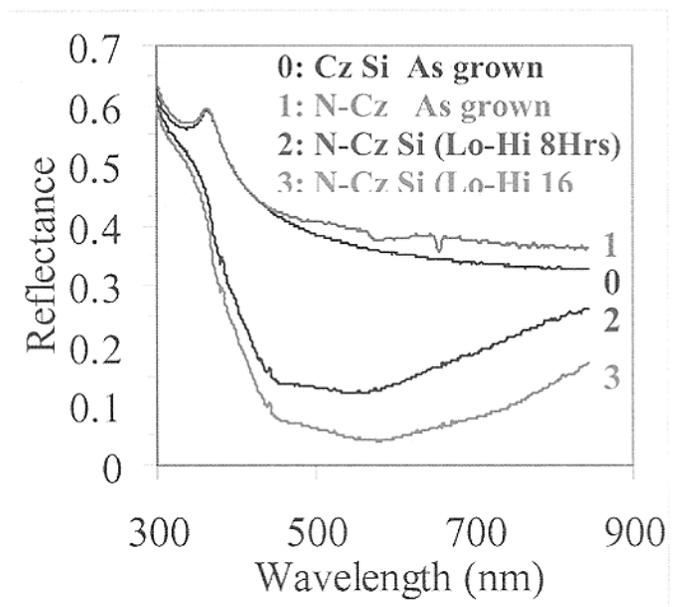


Fig. 4: HR TEM micrographs taken under two beam condition, illustrating the range of defects of an amorphous precipitate at the near surface (defect 1) and at a depth of $3\mu\text{m}$ (defect 3). Note the contrast change at the corner which reveals the stress variation due to the N.

Upon annealing and etching, this near surface gettering band of defects fortuitously forms a very low reflectivity ($<5\%$) textured surface, while the carrier diffusion length is increased due to the gettering. The defects are shown following preferential etching in Fig. 5(a) and Fig. 6, and in cross-section TEM in Fig. 4. The fact that it is nitrogen enhancing the nucleation of near-surface oxygen precipitation is evident from the SIMS depth profiles of N and O presented in Fig. 3(b).



(a)



(b)

Fig. 5: a) Etch pits induced on a bevel polished N-CZ wafer surface by oxygen precipitation following a Lo-Hi anneal and 1 min of Wright etching, b) Normal incidence specular reflectance of as-grown and annealed N-CZ Si, see curves 1-3, compared to conventional Si, curve 0, measured by a Filmetrics Model F20 Reflectometer with a detection solid angle of $\sim 8^\circ$.

In connection to the above described surface defects, a manufacturing compatible process is currently being studied which would generate a surface micro-structure compatible with junction fabrication. This process consists of two simple etching steps (i) dense pit nucleation with the highly stress sensitive defect decoration of Wright etching, see Fig. 6(a), and followed by (ii) pit growth and gettering sink material removal using highly anisotropic etching in an alkali solution, see Fig. 6(b), which also removes any undesirable chemical traces from the Wright etching which might introduce junction contamination.

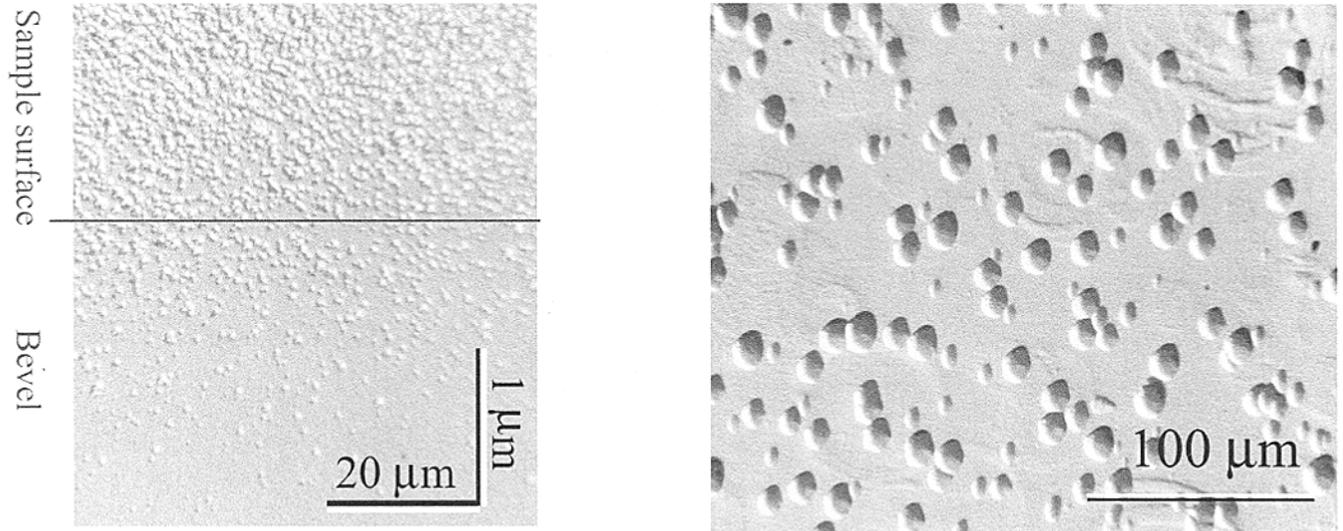


Fig. 6: Nomarski micrographs of N-CZ Si (111) beveled and Wright etched samples for 1 min (a) and a separate sample etched with KOH for 1 min (b).

High density of small etch pits are created by delineating the surface defects and pit growth and connect together with longer KOH etching time.

Conclusions:

This report gives an update on the electrical behavior of dislocations in high purity float zone crystals, and the impact of nitrogen doping on the nucleation of oxygen precipitates. Our experimental results demonstrate that moderately high effective carrier lifetimes of 50 to 200 microseconds can be sustained in heavily dislocated FZ crystals. In N-CZ wafers PV defect engineering options are being explored based on new observations of near-surface defect nucleation and surface texturing. Enhanced light trapping, resulting in a specular reflectance below 5%, can be achieved while etching away surface gettering sinks introduced by the nitrogen doping.

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Lifetime Spectroscopy of FeB Pairs in Silicon

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Abstract – Injection-level dependent lifetime curves of iron-contaminated silicon wafers of various resistivities have been modeled using Shockley-Read-Hall theory. The modeling allows accurate determination of the capture cross-sections of FeB pairs. These cross-sections are then used to extend the validity of a commonly used method for determining iron concentrations to all resistivities. The impact of interstitial iron on solar cell parameters is also modeled and discussed.

1. INTRODUCTION

Iron is an important impurity in silicon devices, whether for photovoltaic or microelectronic applications. As such, it is desirable to characterize the electronic properties of its common forms as accurately as possible. While this has largely been achieved for interstitial iron (Fe_i), it has not fully occurred for the acceptor level of FeB pairs. The energy level of the latter has been determined by deep-level transient spectroscopy (DLTS) with reasonable accuracy, but measurement of the capture cross-sections has to date been uncertain [1].

This paper presents a new technique, known as Injection-level Dependent Lifetime Spectroscopy (IDLS), for accurately determining these properties. The method is based on modeling lifetime measurements on samples with widely varying dopant densities, with Shockley-Read-Hall (SRH) statistics. In terms of determining carrier capture cross-sections, it is more accurate than conventional techniques such as DLTS.

The results have implications for widely used techniques for measuring the iron concentration based on the change in diffusion length after thermal dissociation of FeB pairs [2]. The scaling factors used in these methods are in fact resistivity

dependent, a fact that is not always recognised. The cross-sections of FeB pairs determined in this study by IDLS have allowed these factors to be calculated for any resistivity.

Finally, in operating solar cells, all of the non-precipitated Fe will be present as Fe_i . Using the known energy level and capture cross-sections of this impurity, the impact of varying levels of Fe_i on the I-V curve of a silicon cell can be modeled. One interesting consequence is that the strong asymmetry of the cross-sections results in degradation of the fill factor, even for relatively low Fe_i concentrations.

2. LIFETIME SPECTROSCOPY OF FeB PAIRS IN SILICON

As summarized recently by Istratov *et al.* [1], there exist two charge states of the FeB pair in silicon. One state occurs as a donor level at $E_V+0.1eV$, and the other as an acceptor level at $E_C-0.26(\pm 0.03)eV$. Brotherton *et al.* [3] argued that the acceptor level must be the dominant recombination center of the two, due to the fact that it is deeper. Hayamizu *et al.* [4] showed that the acceptor level does indeed dominate recombination through FeB pairs at room temperature. They performed temperature dependent low-injection lifetime measurements, which could only be adequately described by a relatively deep level around 0.29eV from either band edge.

In another study, Walz *et al.* [5] examined the injection-level dependence of the recombination lifetimes at room temperature of iron-diffused samples for a range of intermediate resistivities, and found that their data could be adequately explained by modeling the combined effect of the acceptor level and the level for interstitial iron. They were able to determine values for the capture cross-sections of the acceptor level by fitting SRH curves. This technique,

referred to here as Injection-level Dependent Lifetime Spectroscopy (IDLS) [6], can allow more accurate measurement of cross-sections than the more commonly used DLTS methods, which require extrapolation of emission rate data to an axis. However, a crucial requirement of the IDLS technique is that samples with widely different dopant densities need to be used. The important feature of these different resistivities is that the injection-level dependence of the lifetime for a given defect is often markedly different, allowing accurate fitting of SRH curves with a consistent and unique pair of capture cross-sections. Walz *et al.*'s study was restricted to a resistivity range of 1 to 20Ωcm due to constraints of their measurement method (ELYMAT). In this work, we study a larger range of resistivities, from 0.3 to 150Ωcm. This corresponds to 25 times the dopant density range used by Walz *et al.*, a feature that turns out to be very important for *uniquely* determining the cross-sections.

In addition to varying the dopant densities, the dissociation behavior of FeB pairs upon illumination may be used to vary the recombination center densities by applying different levels of light-soaking. In our experiments, the total iron concentration is known from the implantation dose, and so the sum of the modeled FeB and Fe_i centers can be forced to equal this value. In this way, a good fit can be achieved for each light-soaking condition and resistivity, resulting in uniquely determined capture cross-sections.

2.1 Experimental Methods

Care needs to be taken during sample preparation to ensure that the deliberately introduced Fe occurs evenly throughout the bulk of the wafers, as this is essential for accurate injection-level dependent lifetime measurements. Also, the impurities to be studied should not be subject to significant gettering at the surfaces or damaged regions, nor undergo excessive out-diffusion or precipitation in the bulk. In this study, avoiding loss of iron through these processes allows us to determine the bulk iron concentration, after annealing, from a knowledge of the implantation dose. This is important in modeling

the lifetime data and allowing the accurate fitting of the SRH parameters.

Boron-doped *p*-type float zone (FZ) silicon samples of four resistivities (0.3, 1, 5 and 150Ωcm) were chosen for this study. The exact details of their preparation is given elsewhere [7]. In summary, they were implanted with 70keV ⁵⁶Fe and annealed at 900°C for 1 hour to distribute the iron uniformly throughout the wafers. Surface passivation was achieved by depositing films of plasma-enhanced chemical vapor deposited (PECVD) silicon nitride [8]. This passivation allows lifetimes of above 1ms to be observed in high resistivity material.

The quasi-steady-state photoconductance (QSSPC) technique[9] was used to measure the injection-level dependence of the effective lifetimes. Control samples were included to ensure that the measured lifetimes reflected the recombination properties of the iron-related states only, and not surface effects or the pre-implanted lifetime of the FZ wafers. This was confirmed by the fact that the effective lifetimes measured on the control samples were almost always an order of magnitude or more greater than the lifetimes of the iron implanted samples.

2.2 Shockley-Read-Hall Statistics

The injection-level dependence of the SRH lifetime τ_{SRH} is a function of the dopant density N_A , recombination center density N_{SRH} , defect energy level E_T and capture cross-sections, and for *p*-Si is given by[10-12]:

$$\frac{1}{\tau_{SRH}} = \frac{N_A + \Delta n}{\tau_{p0}(n_1 + \Delta n) + \tau_{n0}(N_A + p_1 + \Delta n)} \quad (1)$$

Here, $\Delta n = \Delta p$ is the excess carrier density, and τ_{n0} and τ_{p0} are the fundamental electron and hole lifetimes, which are related to the recombination center density, the thermal velocity[13] $v_{th} = 1.1 \times 10^7 \text{ cm s}^{-1}$, and the capture cross-sections via $\tau_{n0} = 1/(v_{th}\sigma_n N_{SRH})$ and $\tau_{p0} = 1/(v_{th}\sigma_p N_{SRH})$. The statistical factors n_1 and p_1 are the electron and hole densities when the Fermi energy coincides with the recombination center energy [12].

Under low- ($\Delta n \ll N_A$) and high-injection ($\Delta n \gg N_A$) conditions, Eq. 1 can be simplified for a given

Recom. Center	Energy (eV)	σ_n, σ_p (cm ²)	Low-inj. τ_{SRH}	High-inj. τ_{SRH}
Fe _i (ref [1])	E _v +0.38	5×10 ⁻¹⁴ 7×10 ⁻¹⁷	τ_{n0}	τ_{p0}
FeB (this work)	E _c -0.23	3×10 ⁻¹⁴ 2×10 ⁻¹⁵	$\tau_{p0}(n_i/N_A)$ + τ_{n0}	τ_{p0}
FeB (Walz)	E _c -0.29	2.5×10 ⁻¹⁵ 3×10 ⁻¹⁴	τ_{n0}	τ_{n0}

TABLE 1. Energy levels, capture cross-sections, and approximations for the SRH lifetimes under low- and high-injection for Fe_i and FeB pairs.

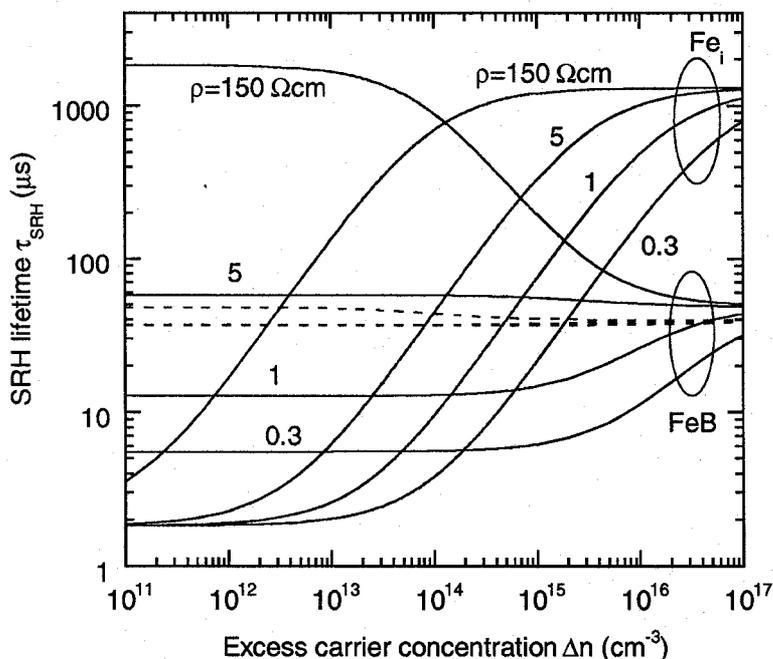


FIGURE 1. SRH lifetime curves for different Fe-related recombination centres in p-type silicon of different resistivities. Curves for FeB using Walz et al.'s values are shown as dashed lines. The lower dashed line represents the three lower resistivities, which coincide.

recombination center. These are listed in Table 1 for three cases: interstitial iron, FeB pairs with the recombination parameters used in this work, and FeB pairs with those used by Walz.

Fig 1 illustrates theoretical injection-level dependent lifetime curves for these three cases. The curves, calculated for a bulk defect concentration of 1×10¹²cm⁻³ for each of the four resistivities used in this study, reveal their different behaviors. Note in particular the lack of injection-level dependence of Walz's parameters for the FeB pair in comparison with those used in this study. However, as mentioned, Walz only measured samples in a small range of resistivities, from 1 to 20Ωcm, and over this narrow

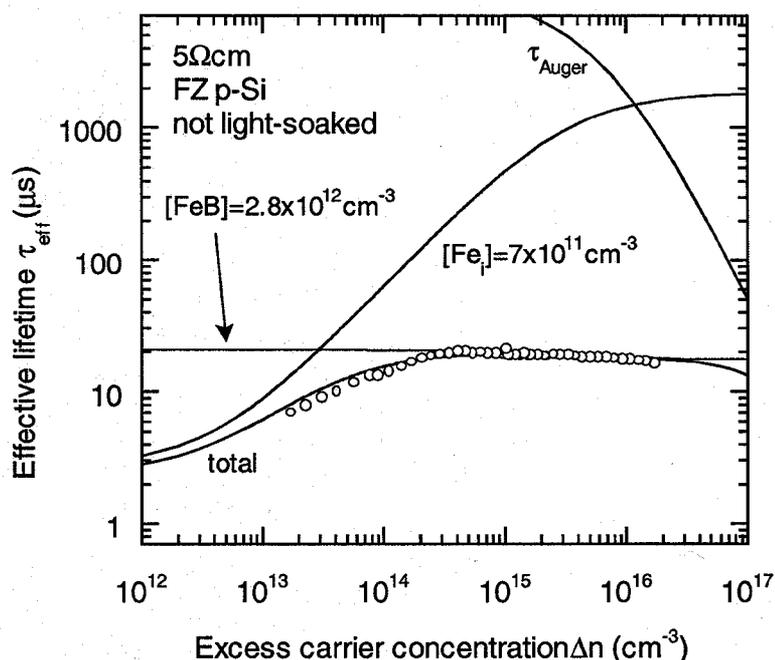


FIGURE 2. Fitting procedure for the 5Ωcm sample without light-soaking. The implanted dose was 1×10¹¹cm⁻².

range the optimum parameters found in this current study also give a mild dependence. Hence, the parameters found in this work, and those found by Walz, provide reasonable approximations to one another over the narrower dopant range. However, when data from a much larger dopant density range is examined, the cross-sections determined in this study must be used.

2.3 Modeling Procedure

The effects of Auger recombination are often important in heavily doped or highly excited silicon[14], and need to be considered here at the higher carrier concentrations. The control samples reveal that the surfaces are not significant in the iron-diffused samples studied. Therefore, the effective lifetime, comprising all of the important contributions, can be expressed as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SRH}^{Fe_i}} + \frac{1}{\tau_{SRH}^{FeB}} + \frac{1}{\tau_{Auger}} \quad (2)$$

The Auger lifetime is calculated using a Coulomb-enhanced Auger recombination model [15,16] which is valid for all injection-levels and dopant densities. Values for the Auger coefficients C_n, C_p and C_a are taken from the literature [14,17].

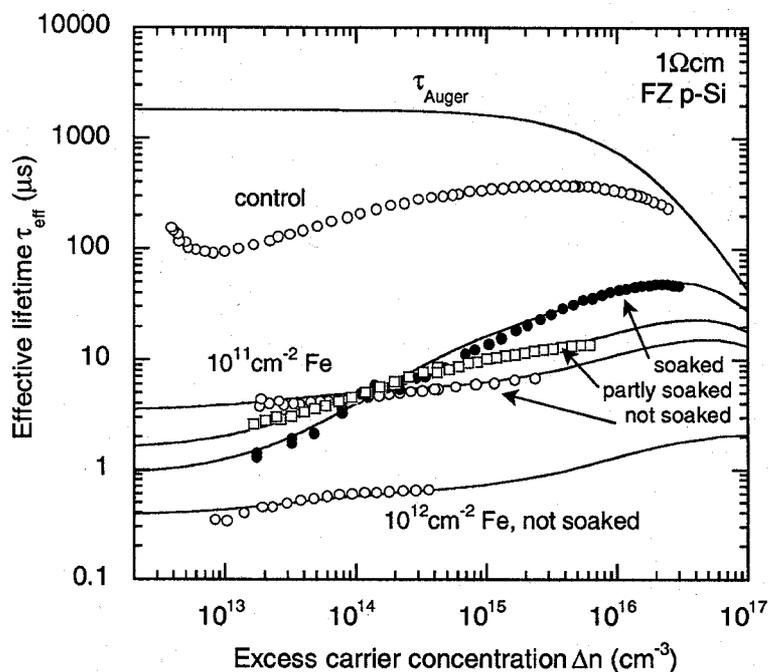


FIGURE 3. Lifetime measurements and SRH fits for $1\Omega\text{cm}$ samples implanted with iron doses of $1\times 10^{11}\text{cm}^{-2}$ and $1\times 10^{12}\text{cm}^{-2}$.

The fitting procedure proceeds as follows. Curves such as those in Fig 1 are taken for interstitial iron and FeB pairs for the appropriate resistivity. These curves are combined in a linear fashion according to Eq. 2, with a term for Auger recombination included, and compared to the measured data. The concentrations of each center are adjusted, and the shape of the FeB curve altered by changing the cross-sections, until a good fit is obtained for all the samples with a single set of cross-sections. An example of the fitting process are given in Fig 2. In this figure, data for the $5\Omega\text{cm}$ sample without light-soaking is shown, and is dominated by the presence of FeB pairs.

For all samples, the sum of the modeled interstitial iron and FeB pair concentrations is forced to agree with that expected from the implantation dose. For Fig 2, this sum equals $3.5\times 10^{12}\text{cm}^{-3}$, precisely that expected from an implant dose of $1\times 10^{11}\text{cm}^{-2}$ in a wafer of thickness 0.0285cm .

2.4 Results and Discussion

Figure 3 depicts the results for two $1\Omega\text{cm}$, iron implanted samples, with doses of 1×10^{11} and $1\times 10^{12}\text{cm}^{-2}$. There are three curves for the lighter dose corresponding to different light-soaking levels,

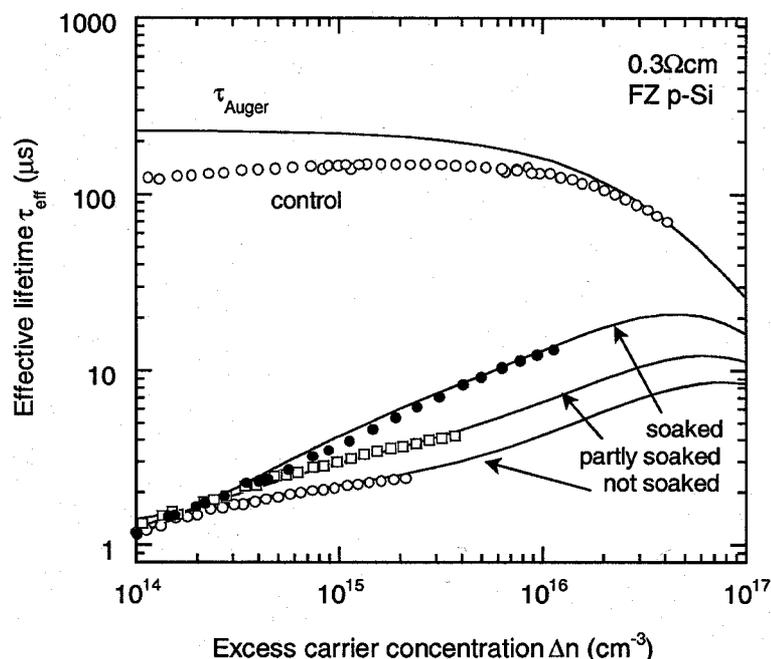


FIGURE 4. Lifetime measurements and SRH fits for the $0.3\Omega\text{cm}$ sample implanted with an iron dose of $1\times 10^{11}\text{cm}^{-2}$.

Resistivity (Ωcm)	[Fe] (cm^{-3}) from dose	Light soaking	Modeled [Fe] (cm^{-3})	Modeled [FeB] (cm^{-3})
0.3	3.5×10^{12}	none	1.0×10^{12}	2.5×10^{12}
"	"	partial	2.0×10^{12}	1.5×10^{12}
"	"	full	2.9×10^{12}	0.6×10^{12}
1	2.5×10^{12}	none	0.2×10^{12}	2.3×10^{12}
"	"	partial	1.1×10^{12}	1.4×10^{12}
"	"	full	2.0×10^{12}	0.5×10^{12}
"	2.5×10^{13}	none	0.2×10^{13}	2.0×10^{13}
5	3.5×10^{12}	none	0.7×10^{12}	2.8×10^{12}
150	2.9×10^{13}	none	0.5×10^{13}	2.0×10^{13}

TABLE 2. Modeled and implanted iron concentrations for the different resistivity samples under different light-soaking conditions.

and hence different relative populations of Fe_i and FeB pairs. The fact that these concentrations add to agree with that expected from the dose, as shown in Table 2, indicates that very little precipitation has occurred in the samples. This is further corroborated by the fact that a good fit for the heavier dose can be achieved by merely scaling up the concentrations by an order of magnitude. It is interesting to note that even in the fully light-soaked case, it was still necessary to include a small number of FeB pairs to describe the data well, indicating that either pair dissociation is not complete or that some re-pairing

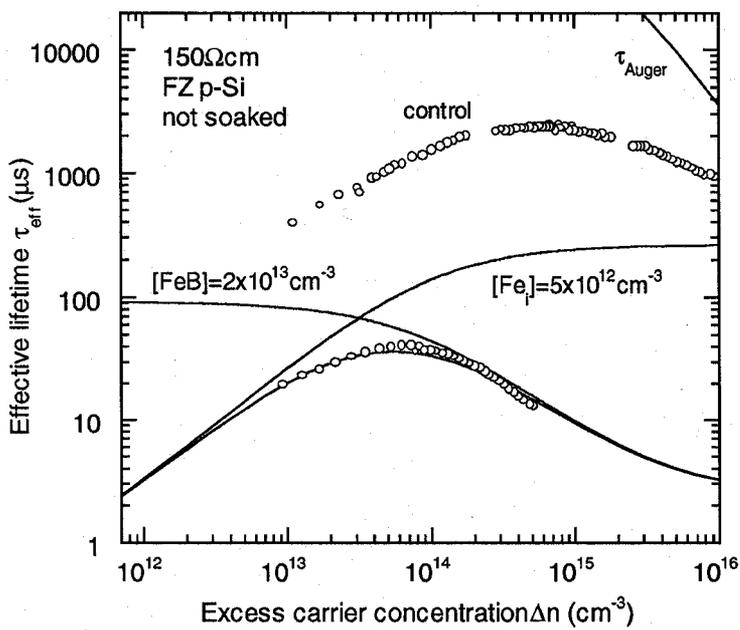


FIGURE 5. Lifetime measurements and SRH fits for the 150Ωcm sample implanted with an iron dose of $1 \times 10^{12} \text{ cm}^{-2}$.

occurs between light-soaking and lifetime measurement.

Figure 4 shows the results for the 0.3Ωcm sample, implanted with a dose of $1 \times 10^{11} \text{ cm}^{-2}$. Once again, the sum of the modeled concentrations agrees well with that obtained from the dose. For the 150Ωcm light-soaked case, the dependence becomes much more pronounced, as revealed in Fig 5. In this plot, the constituent SRH curves for the FeB pairs and Fe_i are also shown. The strong dependence of the FeB curve is clear in this case, which contrasts with the weak dependence predicted by Walz's cross-sections (see Fig 1). Note that in comparison with the 0.3Ωcm data in Fig 4, the lifetime dependence without light-soaking goes in opposite directions as the carrier density increases, again as expected from Fig 1.

The data in Fig 5 is for a sample that was implanted with a heavier dose of $1 \times 10^{12} \text{ cm}^{-2}$. For this resistivity, the corresponding wafer with the lighter dose gave lifetime data that was too close to the control sample, meaning that surface recombination impacted on the measurements.

For the fits shown, the capture cross-sections used for the FeB pairs were $\sigma_n = 3 \times 10^{-14} \text{ cm}^2$ and $\sigma_p = 2 \times 10^{-15} \text{ cm}^2$. It is possible to estimate the uncertainty in these values by adjusting them and observing the

effect on the fits. In conjunction with a typical uncertainty in the measured lifetimes of around 20%, and an uncertainty of about 5% in the dopant densities, we can state that the cross-sections should reside in the ranges $\sigma_n = (3 \pm 2) \times 10^{-14} \text{ cm}^2$ and $\sigma_p = (2 \pm 1) \times 10^{-15} \text{ cm}^2$. The value of the energy level used was Ec-0.23eV, which is within the uncertainty bounds reported by Istratov in his recent review of iron complexes in silicon[1].

As a more general observation, this work illustrates that with appropriate choices of implant dose, annealing temperature and time, and a good range of substrate resistivities, injection-level dependent lifetime spectroscopy offers an accurate alternative to DLTS techniques for determining capture cross-sections of defects in semiconductors, especially if the defect energy is known.

3. RATIO AND DIFFERENCE OF DIFFUSION LENGTHS

Zoth and Bergholz [2] found that samples dominated by Fe_i and FeB pairs could be identified by the ratio of the diffusion lengths L_1/L_0 , as measured by the Surface Photovoltage method (SPV), before (L_0) and after (L_1) thermal annealing at 210°C. Prior to annealing, the majority of the Fe is in the form of FeB pairs, whilst after annealing it is present as Fe_i. Due to constraints of the technique, SPV measurements are always performed under low-injection conditions. Since the low-injection lifetime of Fe_i is independent of the dopant density, while for FeB pairs it depends strongly on the dopant density, it follows that the ratio of the diffusion lengths is also a function of N_A . Indeed, Zoth and Bergholz found that this was true, and they reported the value of L_1/L_0 , to be about 0.5, 0.33 and 0.25 for dopant densities of 10^{16} , 10^{15} and $< 5 \times 10^{14} \text{ cm}^{-3}$.

Using the energy level and cross section data from the previous section, it is possible to calculate the diffusion length ratio L_1/L_0 as a function of the dopant density using the SRH model. Figure 6 shows the results, with Zoth and Bergholz's SPV data included for comparison. The error bars for their experimental points are only estimates. Also shown

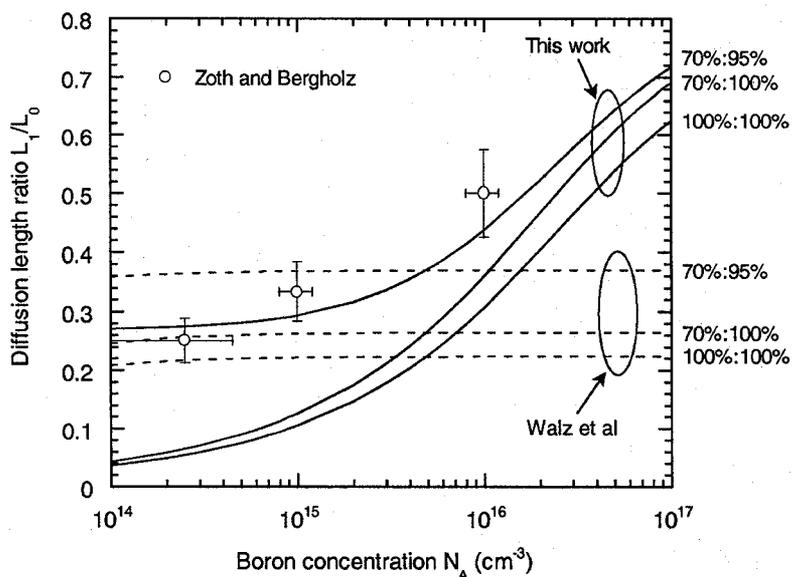


FIGURE 6. Diffusion length ratio (low-injection) after and before thermal annealing for iron-dominated p-type samples as a function of dopant density.

are curves calculated using Walz *et al.*'s values for the energy level and cross-sections of FeB pairs.

An important consideration in calculating such curves is the proportion of the total iron concentration in the form of Fe_i or FeB pairs. Even after thermal annealing, not all FeB pairs dissociate, and some will re-pair during cooling down. Zoth and Bergholz estimated that for their samples, about 70% of the available iron was present as Fe_i after the thermal treatment. Similarly, not all the iron will re-pair after a finite period of time at room temperature. The re-pairing rate is dependent on the boron concentration [2,18], and there may be as much as 5% interstitial iron in higher resistivity samples even after long periods of resting in the dark. Our data in Table 2 shows that some samples without light-soaking had only 80-90% of the iron present as FeB pairs, although they were not rested for long periods of time, and so are not directly comparable to Zoth and Bergholz's samples in terms of relative populations. Further, SPV measurements are performed under very low injection, whereas the QSSPC measurements performed here are generally around mid-injection. These higher carrier concentrations can cause FeB pair splitting, resulting in more interstitial Fe in our non light-soaked measurements than in Zoth and Bergholz's.

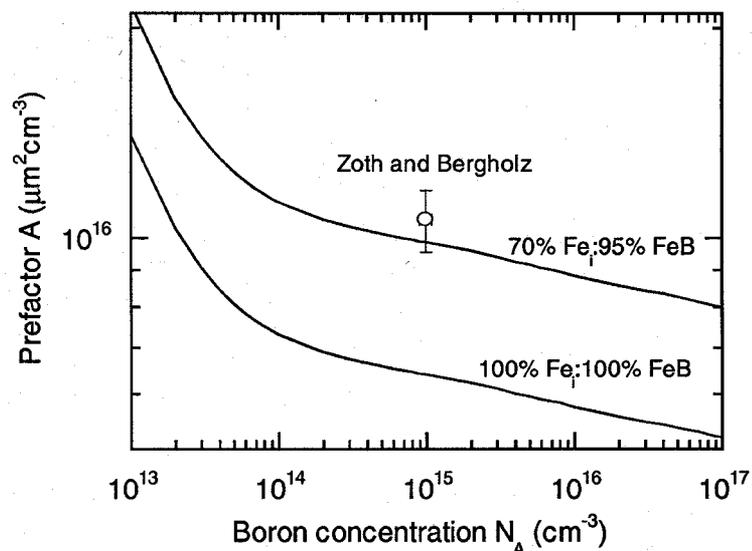


FIGURE 7. Pre-factor A for determining the absolute iron concentration in iron-dominated samples as a function of dopant density.

To illustrate the effect of these variations, Figure 6 shows the curves calculated for three different conditions: 100% Fe_i after annealing and 100% FeB before (ideal state, shown as 100%:100%); 70% Fe_i after annealing and 100% FeB before (shown as 70%:100%); and 70% Fe_i after annealing and 95% FeB before (shown as 70%:95%). This final condition is probably a good approximation of the relative populations in Zoth and Bergholz's samples, and yields good agreement with their data when using the cross-sections and energy levels used in this work. The curves reveal the importance of careful sample treatment when dissociating FeB pairs, as slight changes in relative populations can impact heavily on the results. Note that the curves from Walz's parameters do not follow the trend of Zoth's data, and are essentially flat, reflecting the fact that the low-injection lifetime for Walz's FeB center is independent of the dopant density, in contradiction to the experimental evidence presented here.

The curves in Figure 6 can be used to determine if a sample is dominated by iron. Zoth and Bergholz went on to show that in such cases, the absolute iron concentration can be determined by the following relation:

$$[Fe] = A \times \left(\frac{1}{L_1^2} - \frac{1}{L_0^2} \right) \quad (3)$$

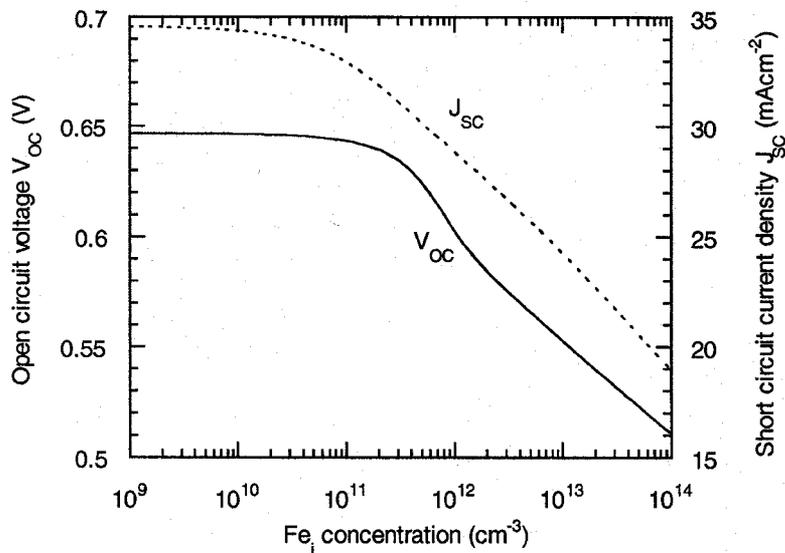


FIGURE 8. Effect of Fe_i concentration on V_{OC} and J_{SC} as modeled for a $1.5\Omega\text{cm}$ cell of thickness 0.03cm and with $J_{0e}=3\times 10^{-13}\text{ A/cm}^2$.

The diffusion lengths must be in microns, and the computed iron concentration is in cm^{-3} . The pre-factor A was found by Zoth and Bergholz to be $1.06\times 10^{14}\text{ cm}^{-3}$ for samples with $N_A=10^{15}\text{ cm}^{-3}$, although their value is often applied to wafers of different resistivities. Using the cross-sections and energy level found in this chapter, it is possible to calculate this pre-factor accurately for *any* resistivity. The result is shown in Figure 7, as well as Zoth and Bergholz's single data point. The 70% Fe_i after anneal:95% FeB before anneal curve falls within 10% of Zoth's data, and extends it to a large range of dopant densities.

4. IMPACT OF Fe_i ON SILICON SOLAR CELLS

In an illuminated silicon cell, any non-precipitated Fe will occur in the interstitial state. Using the recombination parameters in Table 1, it is possible to model the effect of Fe_i on the performance parameters of a cell [19] using PC1D [20]. Figure 8 shows the impact of differing levels of interstitial Fe on V_{OC} and J_{SC} modeled for a $1.5\Omega\text{cm}$ cell of thickness 0.03cm , and with an emitter characterised by a saturation current density of $J_{0e}=3.0\times 10^{-13}\text{ A/cm}^2$. 85% of the incoming light is assumed to be coupled into the cell. The results show that for Fe_i concentrations below 10^{10} cm^{-3} , the voltage of such a cell is dominated totally by the emitter, which caps

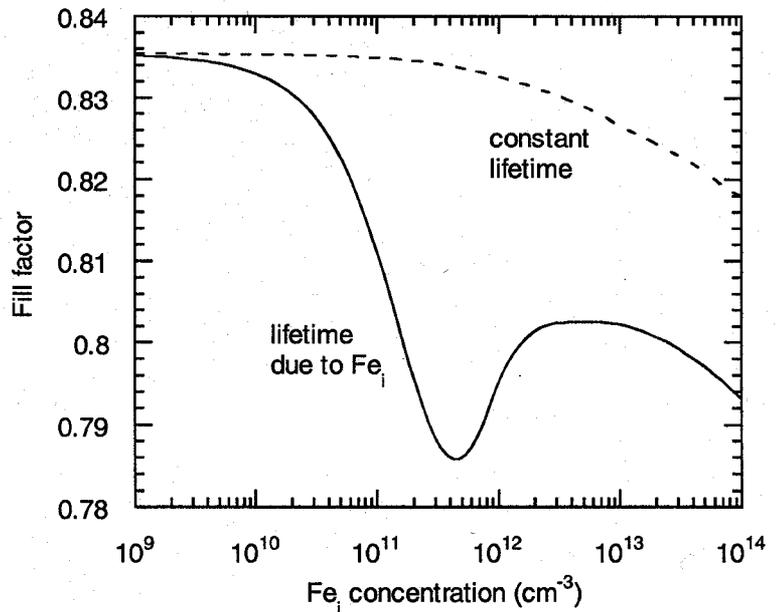


FIGURE 9. Effect of Fe_i concentration on fill factor. Also shown is the fill factor curve for a recombination centre that has an injection-level independent bulk lifetime (which is equal to the high-injection lifetime of Fe_i).

the V_{OC} at 647mV . Also, the short circuit current is essentially independent of the Fe concentration at these low Fe levels because the bulk diffusion length is many times longer than the cell thickness. As the interstitial Fe concentration increases, the current begins to fall as the low-injection diffusion length decreases below the cell thickness. V_{OC} begins to drop also as the lifetime at open circuit decreases. Note that the V_{OC} curve shows a 'kink' which is caused by the injection-level dependence of the bulk lifetime producing an accelerated decrease in the open circuit lifetime as the recombination center density increases. This kink is absent from the J_{SC} curve, because the low-injection lifetime never experiences any injection-level dependence, even at very high iron concentrations.

Of more interest however is the behaviour of the fill factor, which is shown in Figure 9. For very low Fe_i levels, the injection-level dependence of the effective lifetime, being dominated by the emitter, is very slight, and results in an ideal fill factor of 0.835. As the Fe_i concentration increases though, the fill factor begins to degrade due to the increasing SRH dependence around maximum power point. At around $5\times 10^{11}\text{ cm}^{-3}$ Fe_i concentration, the strongest part of the SRH dependence is centered near one-sun maximum power conditions, limiting the fill factor to 0.785. As

the Fe_i level increases further still, the lifetime becomes low enough to take the one-sun carrier density below the strongest SRH dependence, and the fill factor begins to recover. At these high Fe_i levels however, the voltage and current drop off very quickly due to the decreasing magnitude of the bulk lifetime.

As the Fe_i concentration increases above $1 \times 10^{13} \text{ cm}^{-3}$, the decreasing magnitude of the open circuit voltage causes the 'ideal' fill factor to decrease also, a well-known property of $p-n$ junction diodes[21]. Naturally, this effect occurs even for the case where the lifetime is injection-level independent, as shown in the figure.

The underlying reason for the dramatic injection-level dependence of the SRH lifetimes for Fe_i , and hence the poor fill factors, is the large asymmetry between the electron and hole capture cross-sections, which differ by about three orders of magnitude.

5. CONCLUSIONS

Injection-level dependent lifetime measurements can provide an accurate way of determining capture cross-sections of recombination centers. An important aspect of the method is that several samples of widely different resistivities are needed to generate reliable results. In this work, the technique was applied to the acceptor level of FeB pairs in silicon.

These cross-sections allow the recombination dynamics of Fe_i/FeB -pair systems to be accurately predicted. As an example, it is possible to determine the resistivity-dependence of the pre-factor often used to determine the Fe concentration in wafers via the difference in diffusion lengths before and after dissociation. This resistivity dependence is often overlooked.

Finally, the large asymmetry between the cross-sections of Fe_i centers results in strongly injection-level dependent lifetimes, which in turn produce low fill factors, as well as the expected drop in voltage and current.

ACKNOWLEDGEMENTS

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Electrical Behavior of Crystal Defects in Silicon Influence of a Contamination

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Introduction

Compared to microelectronic-grade Si material, multicrystalline Si (mc-Si) contains more impurities and a high density of extended crystal defects such as grain boundaries, dislocations and microprecipitates. These defects largely control the electrical properties of the material and often impact the solar cell characteristics adversely. Note that a typical $10 \times 10 \text{ cm}^2$ solar cell capable of delivering a power of about $1 W_{\text{peak}}$ may contain dislocations with a total length of a few hundred meters up to kilometers and grain boundaries with a total area comparable to the cell area.

A controlled reduction of the detrimental effect of defects on cell efficiency is impossible without detailed knowledge about the origin of the electrical activity of defects and about the way defect properties are influenced by cell processing. This requires the application of microscopic techniques since crystal defects are individuals which may differ very strongly in their electrical activity. Electron and light probe techniques, which allow to assess individual defects with respect to their electrical behavior, are well suited for this task.

In this paper we mainly report on detailed investigations of the recombination activity of defects by temperature dependent EBIC measurements. We will show that the degree of contamination of defects can be estimated. We will sketch the application of EBIC(T) analysis to gettering, hydrogenation and to problems regarding the features of dislocation-related PL and DLTS lines.

Recombination activity of crystal defects in Si: Phenomena

The recombination properties of extended crystal defects in Si are mainly defined by recombination-active impurities decorating the particular defects, i.e. the recombination activity is not an intrinsic defect property, but of extrinsic origin. Even chemico-mechanical polishing [1] may cause defect contamination and increase the defect activity.

Temperature dependent EBIC investigations of the recombination activity of dislocations clearly proved the role of defect contamination, e.g. [2]. Both the magnitude of the contrast and its temperature dependence $c(T)$ have been found to depend on the density of contamination, see Fig. 1a. The $c(T)$ behavior represents a fingerprint characterizing the degree of contamination of the crystal defects. Clean dislocations exhibit only very weak activity (type II), with a maximum at about 50 K and untraceable activity at room temperature. Weak contamination leads to an increase of the low temperature activity, still leaving the room temperature activity below detection limit (type 2). With further increase of the contamination the type of the temperature dependence changes and defect activity is detected at room temperature, too (type 1). A similar influence of contamination was observed for defects formed by oxygen precipitation in CZ-Si [3]. Finally, dislocations decorated with metal silicide precipitates have the highest activity in the whole temperature range (type I).

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Internal Schottky junctions at the metal silicide particles that attract the minority carriers and facilitate fast recombination are the cause of the strong activity (e.g. [4]).

The temperature dependence of the defect contrast $c(T)$ has been analyzed in different Labs in a simple way using Shockley-Read-Hall (SRH) theory, e.g. [5,6,7,8].

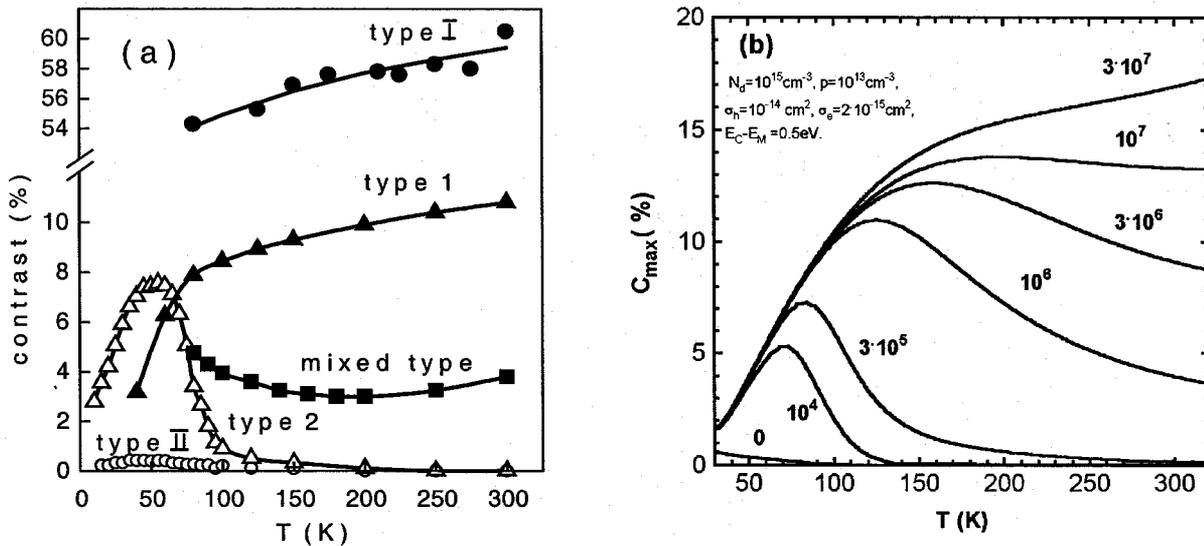


Fig. 1 Temperature dependence of EBIC contrast $c(T)$ of dislocations for different contamination levels

(a) Experimental results: change of the contrast type in the following sequence with increasing contamination level: II -> 2 -> mixed -> 1 -> I

(b) Contrast simulation using the new model, parameter line density N_M (cm^{-1}) of deep levels decorating the dislocation

Missing room temperature activity and increase of activity towards low T (type 2, type II) has been attributed to shallow states. Shallow dislocation states caused by the strain field in the vicinity of the dislocation core are in fact known. These states form 1-dimensional bands located at about 80meV from the band edges, e.g. [9]. The defect activity near 300 K was ascribed to contamination related deep centers according to SRH theory. However, the density of the deep centers at the defects could not be estimated with the simple SRH theory. Also, the simple model did not explain the evolution of the different $c(T)$ behavior with increasing contamination level.

A new model allowing quantitative access to contaminated dislocations

A model that combines the effects of shallow intrinsic defect levels and deep contamination induced centers has recently been published, see [10].

The model assumes that shallow 1-dimensional dislocation bands, induced by the dislocation strain field, and deep electronic levels, caused by segregated impurity atoms at the dislocations, can exchange electrons and holes. As a consequence, the recombination of carriers captured at the dislocation bands can be drastically enhanced by the presence of even small concentrations of impurity atoms at the dislocation core. Fig. 2 illustrates the model schematically. It shows the band scheme around a dislocation with shallow 1-dimensional dislocation bands (E_{De} , E_{Dh}) and deep contamination-related centers near the core. The main recombination channels are indicated. Charge carriers can be trapped in the shallow dislocation bands E_{De} and E_{Dh} . The probability of direct recombination of carriers between these 1D bands (path A) is low and the recombination activity of clean dislocations is very small. (Note that the energy of channel (A) $E_g - 2 \times 0.08 \text{ eV} = 1 \text{ eV}$ corresponds to the energy

of D4-band luminescence.) The recombination probability of carriers is dramatically enhanced by the mediation of the deep levels E_M . Two recombination paths can be distinguished: (B) recombination of carriers trapped in the dislocation bands via the deep levels and (C) recombination of free carriers in the valence and conduction bands by mediation of the level at E_M . The recombination channel (B) is usually stronger (compare also Fig. 3). Results of calculations based on this concept are shown in Fig. 1b. The agreement with the experimental observations is very good. All essential features are reproduced.

Model calculations show that the energy position of the deep level E_M has nearly no influence on the dislocation recombination activity in the temperature range up to 300K as long, as it is deeper than $E_C - 0.3\text{eV}$. Again, this is in accordance with our experimental finding that the type of the metal contaminant (Fe, Ni, Cu or Au) did not influence the shape of the measured $c(T)$ curve. To conclude, the new model allows a consistent interpretation of temperature dependent contrast measurements. In particular, it provides a way to estimate the active contamination level of defects which is of key importance for the assessment of the effect of processing steps such as gettering or hydrogenation. It also can help to analyze the influence of impurity decoration on the features of dislocations in PL and DLTS.

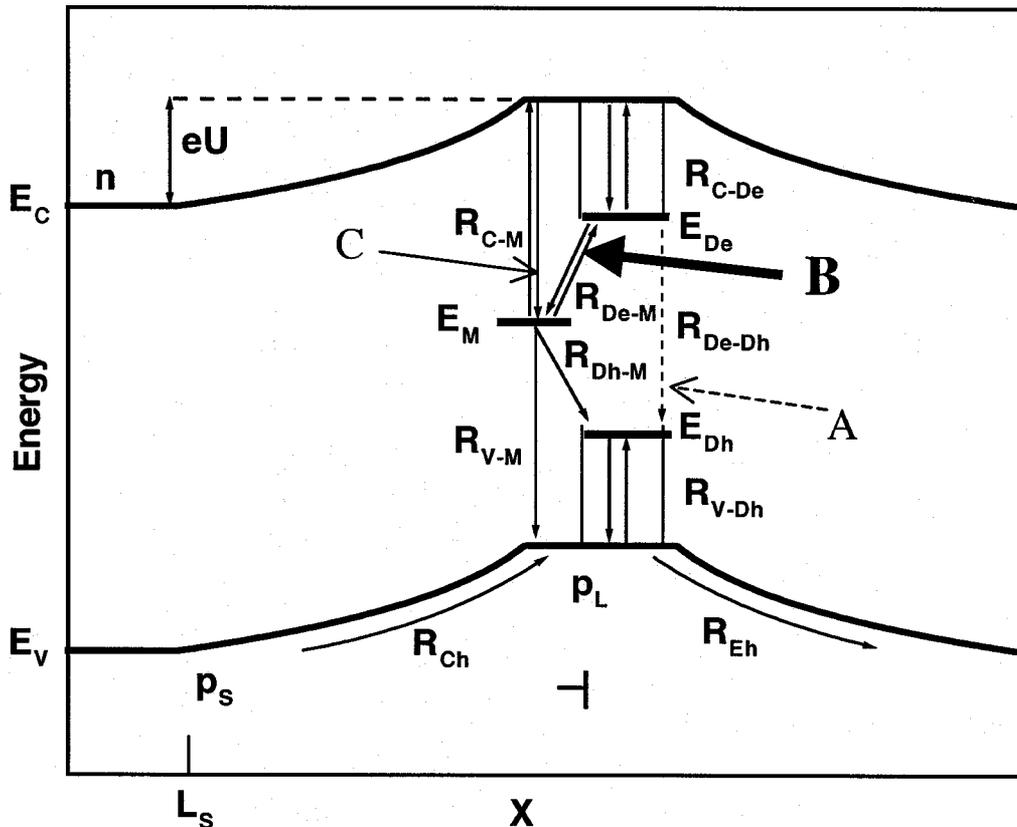


Fig. 2 Charge carrier recombination at dislocations. Recombination at clean dislocations occurs via direct exchange between the 1-dimensional dislocation bands E_{De} , E_{Dh} (A). With deep centers E_M present close to the dislocation core, recombination processes involving the deep level take over (B), i.e. $E_D \leftrightarrow E_M$, and (C), i.e. $E_{C,v} \leftrightarrow E_M$.

Influence of phosphorus gettering

Phosphorus gettering is widely known as a means for reducing metal contamination and improving the performance of solar cells. Nonetheless, quantitative data on the impact of phosphorus gettering on defects had been lacking until recently.

Here we represent results of phosphorus gettering studies in deformed FZ-Si [11]. Fig. 3 shows experimental temperature dependencies of the EBIC contrast of an individual dislocation prior to and after a phosphorus gettering treatment, respectively. The experimental curves can be nicely matched with calculated curves obtained from our model. Curve 2 in the upper diagram was calculated with the same parameters as the matching curve 1, but

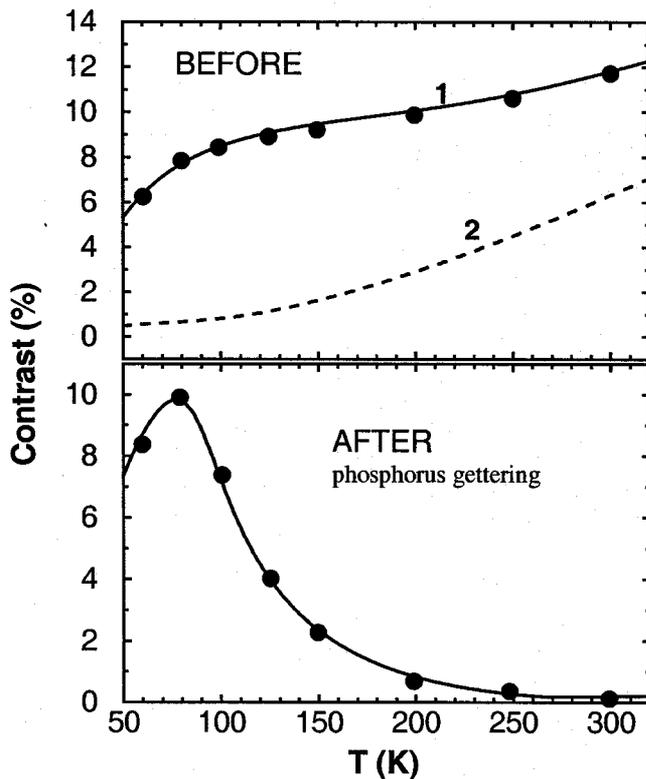


Fig. 3 Match of experimental contrast data and theoretical $c(T)$ (solid curves) for dislocations in Si prior to and after phosphorus gettering, respectively.

The curves indicate a reduction of the density of deep centers by two orders of magnitude. Curve 2 in the upper diagram was calculated without accounting for the effect of recombination path B.

assuming lack of interaction between deep levels and shallow bands (channel B). The large difference emphasizes the importance of this recombination path. The matched curves were calculated using deep level densities of $2.5 \times 10^7 \text{ cm}^{-1}$ (prior to gettering) and $3.5 \times 10^5 \text{ cm}^{-1}$ (after gettering), respectively. Although the actual figures of the deep level concentration depend also on the choice of other parameters of the model (e.g. coupling between dislocation bands and deep centers), a reduction of the dislocation contamination level by about 2 orders of magnitude can be stated.

Influence of hydrogenation

Influence of hydrogenation on the recombination activity of crystal defects in solar-grade Si has been already studied a long time ago, e.g. [12]. We analyzed the temperature dependence of the EBIC contrast at the same dislocation before and after hydrogen treatment [13]. After hydrogenation the recombination activity of the defect is strongly reduced and in most cases not detectable at room temperature. Comparing the experimental with the calculated $c(T)$ curves, we conclude that about 90% of the deep centers decorating the dislocation are passivated. However, a complete passivation of the total number of deep recombination centers, i.e. a restoration of the very low intrinsic defect activity (type II), could not be obtained, see [14]. EBIC measurements of the defect contrast as a function of temperature also provide information about the extension (penetration depth) and characteristics of the hydrogen passivation, see [15]. For block-cast mc-Si a passivation depth of about 100 μm was observed after hydrogen plasma treatment for 1 hour at 310 $^\circ\text{C}$. The extension of the

passivation was essentially the same for grain boundaries and for intra grain dislocations. There was no indication for enhanced passivation along grain boundaries as stated in earlier work. For a more detailed description about our work on hydrogenation see also [15,16].

Analysis of defect recombination behavior in mc-Si regions with high defect density

Numerous studies of mc-Si performed in different labs show that the minority carrier diffusion length decreases with increasing density of intragrain defects/dislocations. However, if we take a closer look at the data by comparing diffusion lengths obtained for a certain defect density substantial differences appear [17]. The spread in the diffusion lengths probably reflects substantial differences in the contamination state of the defects. Unfortunately, the model discussed above cannot be applied directly to assess the contamination level in most grains of mc-Si. Grains with high defect density do not allow $c(T)$ measurements at individual defects.

We will illustrate that measurements of the temperature dependence of the diffusion length $L(T)$ provide another way to estimate the defect contamination. If the diffusion length is controlled by defects a mean defect recombination strength² $\Gamma(T)$ can be calculated from $L(T)$, provided the defect density is known. $\Gamma(T)$ can be analyzed then using our new model [10], delivering information on the mean defect contamination in the respective area. Fig. 4a shows experimental diffusion length data for temperatures between 80 K and 180 K measured in two different grains, P1 and P2, of a block-cast wafer. (Measurements at higher temperatures could not be performed because the energy-dependent EBIC method [18] of determining the diffusion length is limited to values not exceeding 100 μm .)

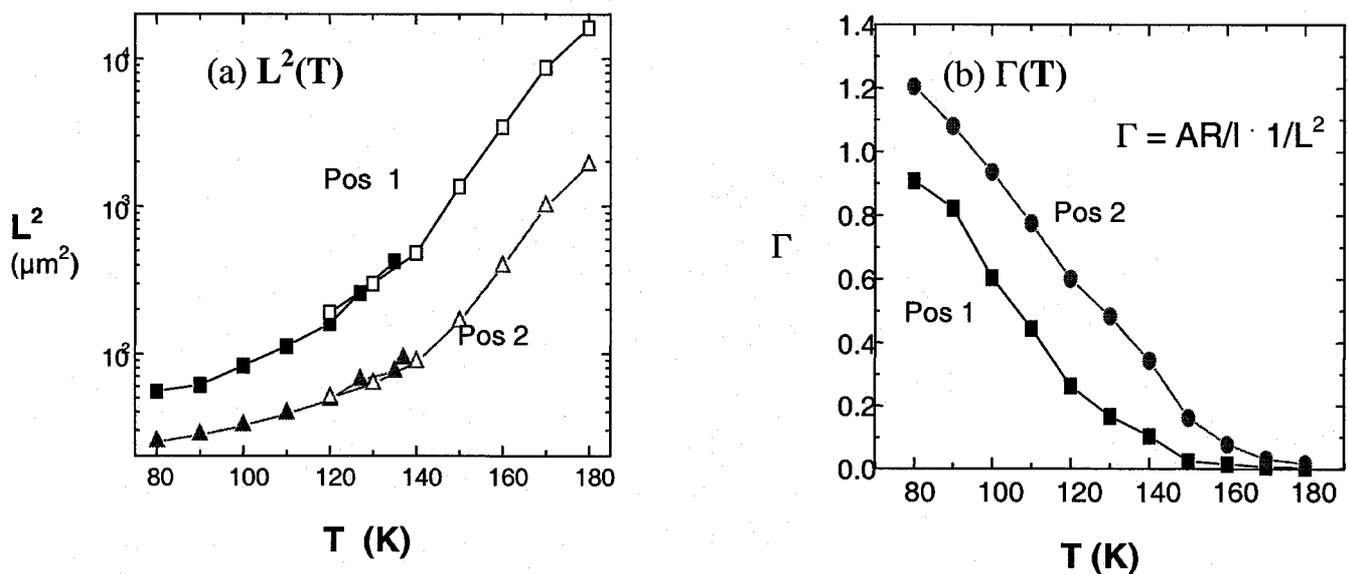


Fig. 4 Assessment of recombination behavior of dislocations by diffusion length measurements as a function of temperature: (a) $L^2(T)$ as obtained for two regions of a block-cast sample (open and solid symbols refer to two sets of measurements in the same area), (b) average recombination strength $\Gamma(T)$ of the dislocations, derived from the diffusion length.

From these data, the average recombination strength $\Gamma(T)$ of the dislocations was estimated using relation $\Gamma = 1 / (L^2 \times N_{\text{disl}})$, where N_{disl} is the total dislocation length per unit volume.

² In addition to the defect activity the conditions used for EBIC measurements (beam energy, doping etc.) influence the contrast value c . The defect strength Γ can be calculated from c by correcting the influence of the experimental conditions.

The results are shown in Fig. 4b. The dependence on temperature indicates a low degree of contamination – compare Fig. 1b. It is also found that the regions P1 and P2 differ in their average dislocation activity. In particular, the dislocation activity at P1 changes faster than that at position P2. Accordingly, this indicates differences in the dislocation contamination.

Results of **modeling the impact of dislocations on diffusion length** at 300 K are represented in Fig. 5. The total concentration of contaminants/metals in the sample is fixed (10^{12} cm^{-3}) and the dislocation density is varied. It is assumed that all contaminants are segregated to the dislocations. The calculations based on the new model give the following results. The diffusion length decreases with increasing dislocation density. It also depends on the parameter α , which describes the coupling between the shallow 1D dislocation bands and the deep level contamination at the dislocations ($\alpha = 1$: strong coupling, recombination path B acting; $\alpha = 0$: no coupling, no path B). If the dislocation density is small (10^4 cm^{-2}) the concentration of deep impurity levels at each dislocation is high and the recombination is controlled by path C because the action of path B is saturated. However, with increasing dislocation density the concentration of impurities per dislocation becomes lower and consequently, for $\alpha = 1$, the action of path B gets more and more dominant, leading to an additional decrease of diffusion length. To conclude, it is found that a given amount of impurities in the sample becomes more harmful the higher the dislocation density.

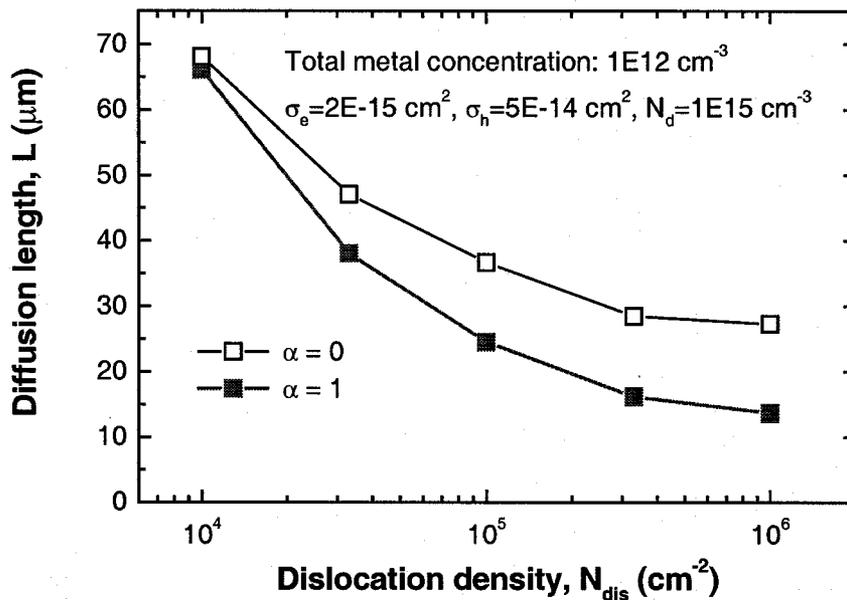


Fig. 5 Calculated dependence of the diffusion length on the dislocation density (parameters $\sigma_e = 2 \cdot 10^{-15} \text{ cm}^2$, $\sigma_h = 5 \cdot 10^{-14} \text{ cm}^2$, $N_{dop} = 1 \cdot 10^{15} \text{ cm}^{-3}$) for fixed total concentration of contaminants (e.g. metals) in the sample of $N_M = 1 \cdot 10^{12} \text{ cm}^{-3}$, $\alpha = 0$ and $\alpha = 1$.

Photoluminescence: Influence of defect contamination

Both the band-to-band and the D1 defect luminescence can be utilized for the purpose of non-contact characterization of Si at room temperature. Examples are given in several papers, e.g. [19,20]. The role of defect contamination on band-to-band and defect luminescence was an open question so far. We have compared mapping of the band-to-band and the defect (D1) photoluminescence, measured at room temperature in mc-Si, with the EBIC $c(T)$ behavior. The intensity of the band-to-band luminescence correlates with the minority-carrier diffusion length. Concurrently, the D1 luminescence band appears in regions with relatively low diffusion length and its intensity is reversed to the band-band PL intensity. Dislocation related

effects in room temperature PL were observed for both type 1 and type 2 EBIC behavior. It means that a relatively low contamination level of dislocations in the order of 10 impurity atoms per μm of the dislocation length produces D1 defect luminescence at room temperature and also degrades both the band-to-band luminescence and minority carrier diffusion length. Further details are given in [21].

DLTS C1 line: Influence of defect contamination

There is little knowledge regarding the influence of impurities on the characteristic lines which appear in DLTS. We have compared DLTS analysis of (misfit) dislocations in n-type Si with the EBIC $c(T)$ behavior. There is clear evidence that clean dislocations, demonstrating type II behavior, do not show the dislocation-related electron trap C1. At the same time, we have found that the DLTS line C1 appears when the clean dislocations are intentionally contaminated with some metals, exhibiting then type 2, mixed type or type 1 behavior, respectively. The transformation of EBIC contrast from type 2 to type 1 corresponds to an increasing contamination between about 10 and 1000 impurities per μm dislocation length. Corresponding spectra are given in Fig. 6. It is also worth to note that the C1 line is symmetric for a small contamination (type 2), but the line becomes asymmetric with increasing contamination level (type 1). Details about this work can be found in [22,23].

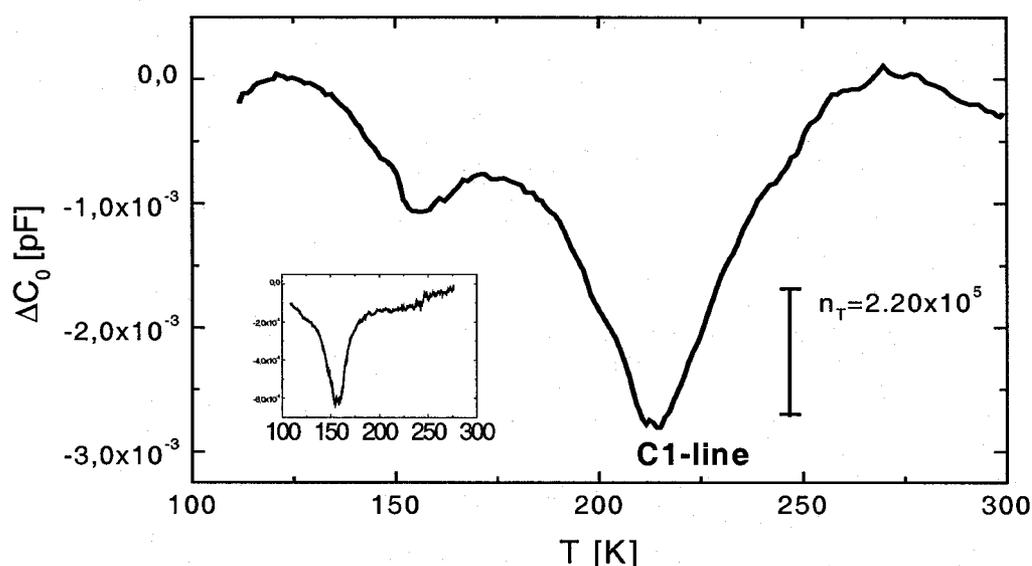


Fig. 6 DLTS of n-type Si samples containing dislocations. The samples exhibit electron traps at about 215 and 155 K. The C1 line appears only when the dislocations are contaminated, whereas clean dislocations do not show this line (see inset).

Summary and conclusions

We have shown that EBIC investigations of carrier recombination as a function of temperature allow to identify the origin of the recombination activity of defects. A new model of recombination at defects/dislocations [10] is used to analyze the $c(T)$ data. The model is capable to consistently explain all experimentally observed features by a different density of deep centers at the defect. This provides a possibility to estimate the density of deep centers at the defect from the experimental data. Examples illustrating the action of phosphorus gettering and hydrogenation on the defect activity are given. Phosphorus gettering is shown to reduce deep centers by 2 orders of magnitude. Hydrogenation is found to passivate defects down to 100 μm depth.

Measurements of the EBIC contrast require low defect densities, a condition that is usually not met in mc-Si. In that case, measurements of the diffusion length L versus temperature T can serve to determine the mean defect activity in a certain area and to estimate the mean defect contamination. This has been successfully demonstrated. It is also found by modeling

that a given metal impurity level in the sample is more harmful the higher the dislocation density. Finally, the influence of impurities on PL emission at room temperature and DLTS has been discussed.

Acknowledgements

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Restructuring of Photovoltaic R&D Programs in Japan

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Contents

- Renewable energy strategy
- Evaluation of SOG-Si program
- A new 5 year program
 - Thin film solar cells
 - Bulk-type c-Si solar cells

ABSTRACT:

Recently, the Japanese new energy policy was restructured by emphasizing the use of photovoltaics and wind energy. As for PV, an accumulated PV energy production of 4.82 GWp is expected to be introduced in 2010. Toward the government target, Japanese PV market in 2000 has grown to 129 MWp corresponding to 40 % of the world-wide cell production. The increase was realized by the government subsidy policy and development of cost-effective multicrystalline Si solar cells. However, the module price tends to be saturated. To decrease cost reduction furthermore, NEDO R&D programs were restructured especially for thin-film solar cells. A new R&D program includes advanced solar cells, innovative solar cells and systems research. In addition, the four-year R&D program for multicrystalline Si solar cells keeps on developing high-quality cast substrates and cell fabrication technologies to realize a 20 % cell efficiency.

New Energy Policy

(New energy committee under MITI, 2000)

Viewpoint under environment constraint

- International consensus : COP 3 in Kyoto
- Suppression of energy consumption —energy saving
- Short and long -range prospect of primary energy supply
 - Best mix of nuclear energy and new energy —
 - Short range (up to 2010) : what energy is used ?
 - Long-range (after 2030) : Sustainable energy society
- Prospect of power network
 - combination of central and dispersed energy systems

Potential of new energy supply in Japan

(New energy committee under MITI, Jan. 2000)

		Potential (Replaced oil)	Introduced in 2010 (Replaced oil)
Renewable energy	Photovoltaics	20 GJ	1.2 GJ
	Solar thermal	16 GJ	4.5 GJ
	Wind energy	2 GJ	0.12 GJ
Recycle energy	Not used energy	2 GJ	0.58 GJ
	Urban waste energy	10 GJ	6.62 GJ
	Waste wood, etc.	6 GJ	5.92 GJ
Biomass		7 GJ	-----
Total		64 GJ	19 GJ
(% in primary energy supply)		(10%)	(3%)

Dissemination Scenario toward 2030

I. Application areas

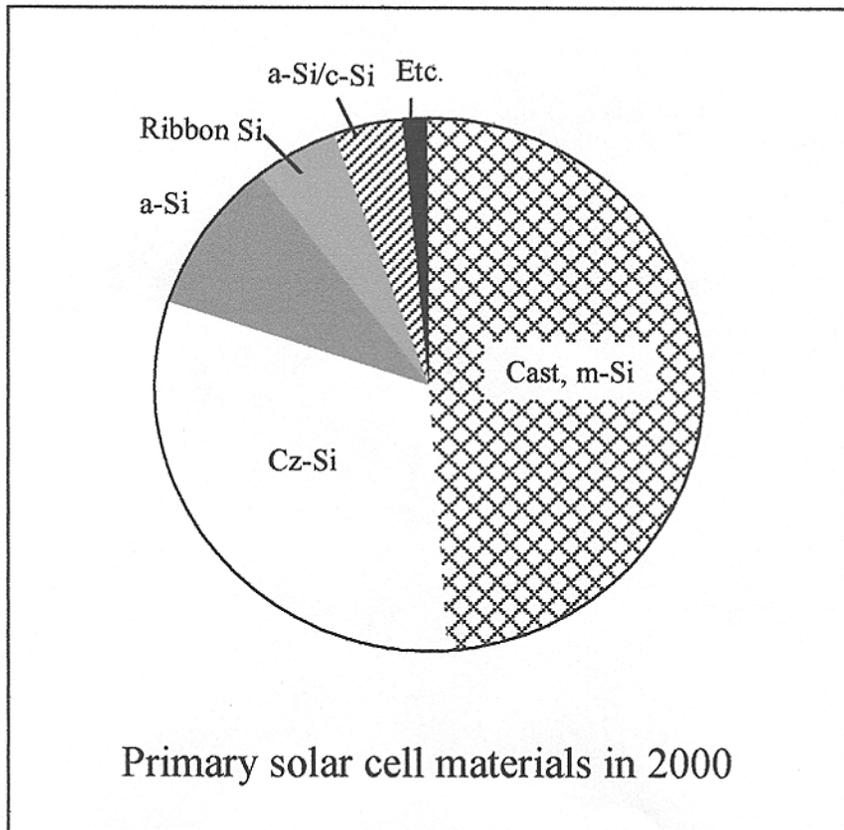
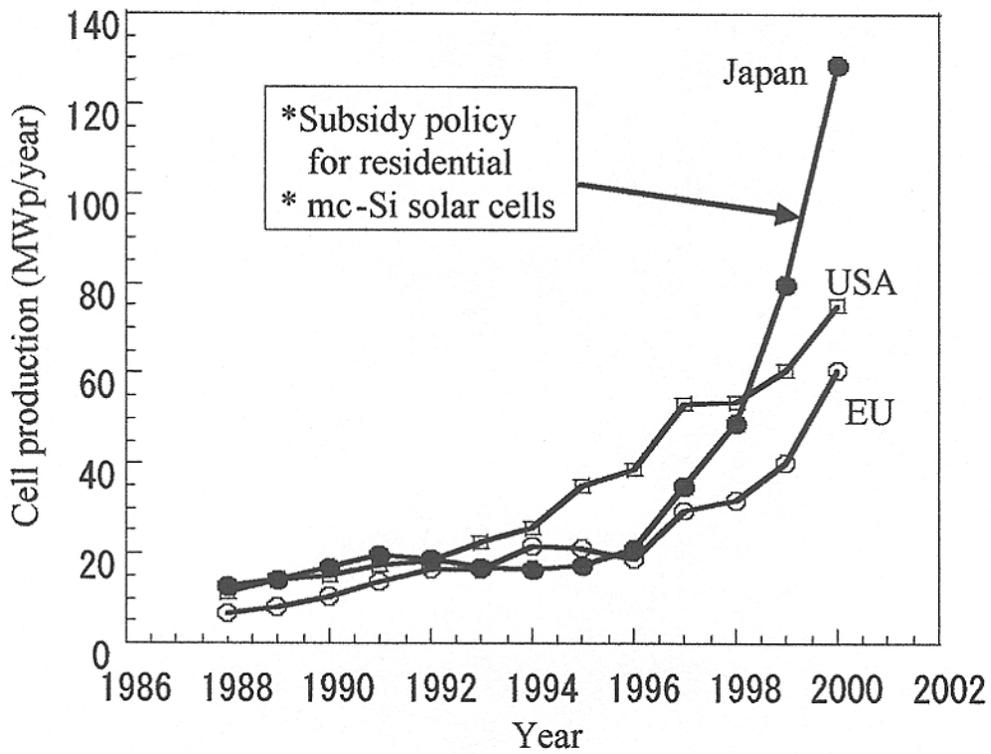
	Residential	Public	Industrial
Solar thermal	50 %of new houses	25to 50 % of new buildings	10to 20 % of new facility
Photovoltaics	15to 20 % of total houses	50to 100 % of new buildings	10to 20 % of new facility
Wind energy	Dependent on resources		
Urban waste	Highefficiency plant		
Biomass	Emergence of biomass and methane fermentation		
Cogeneration	-----	20to 30 % of new buildings	10to 20 % of new facility
Fuel cell			

Dissemination Scenario toward 2030

II. Estimated amounts

	1999		Forecast in 2010		Forecast in 2030	
	Introduced	Replaced oil	Introduced	Replaced oil	Introduced	Replaced oil
Solar thermal	-----	0.91 GJ	-----	4.50 GJ	-----	7.5 GJ
Photovoltaics	0.13 GW	0.03 GJ	4.82GW	1.18 GJ	52.5 GW	12.8 GJ
Wind energy	0.04 GW	-----	3.00 GW	1.20 GJ	2.7 GW	1.1 GJ
Urban waste energy	1.69 GW		5 GW	6.62 GJ	11.3 GW	18.8 GJ
Biomass		4.61 GJ		5.92 GJ		18.9 GJ
Co-generation	1.69 GW		4.6GW		12.6 GW	
Fuel cell	0.01 GW		2.2 GW		17.2 GW	

Yearly Cell Production in Four Regions
(P. Maycock, 2001)



**Evaluation of Mass Manufacturing Processes
for SOG-Silicon and Multicrystalline Solar Silicon Wafer**

By Kawasaki Steel and Sumitomo Sitix (FY 1999 – FY 2002)

Table 1 Developed technologies

SOG-Si pilot plant	60 tons/year
Pulling-down speed of EM casting	2.5 mm/min
Wire saw productivity (15 cm sq, 4 ingots/run)	115,000 slices/month
Cell efficiency (EMC)	13.6 % (12.8 to 13.7)
Cell efficiency (conv.)	13.7% (13.4 to 13.7)

Table 2 Estimated production cost

SOG-Si feedstock	2,300 yen/kg (79 yen/wafer)
EMC ingot	2,800 yen/kg (99 yen/wafer)
Slicing & cleaning	135 yen/wafer
Total	313 yen/wafer

Assumptions: 1000 t/y, 100 MWp/y, 15 cm sq, 250 μm

Evaluation of Current R&D Programs
(FY 1996 to 2000)

R&D for Materials

1. Substrates for thin cells → to be continued
2. SOG-Si feedstock → to be finished

R&D for solar cells

1. Amorphous Si → to be finished
2. CdTe → to be finished
3. CIS and poly-Si films → to be continued
4. III—V → to be continued
5. mc-Si → to be continued

A New 5-year R&D Program
(FY 2001 to 2005)

Targets

- * Accumulated expected production (20 times)
200 MWp (FY1999) → 5 GWp (FY2010)
- * PV electricity cost (one third)
70 yen/kwh (FY1999) → 25 yen/kwh (FY 2005)
(Module cost: 100 yen/Wp)

R&D Programs for Solar Cells

I. Advanced R&D

1. a-Si/c-Si hybrid thin cells
2. CIGS thin film cells
3. III-V concentrator cells
4. Multicrystalline Si cells (FY1999 - FY2002)

II. Innovative R&D

1. Nanostructure Si solar cells
2. SiGe-base solar cells
3. Dye-sensitized solar cells
4. Thin-film Si solar cells by Cat-CVD process
5. B-type FeSi₂ solar cells
6. Ball-type Si solar cells
7. CuInS₂ solar cells by plating process

Targets in Advanced R&D Programs
(FY2001 to FY 2005)

Solar cells	Program targets
<ul style="list-style-type: none"> • a-Si/c-Si hybrid cells • CIGS thin cells 	Module efficiency : 12 % Module size : 3,600 cm ² Production cost : 100 yen/Wp*
<ul style="list-style-type: none"> • III-V concentrators 	Cell efficiency : 40 % Production cost : 100 yen/Wp*
<ul style="list-style-type: none"> • High-efficiency mc-Si cells (FY 1999 to FY 2002) 	Cell efficiency : 20 % Wafer thickness : 150 μm Production cost : 147 yen/Wp*

* Assumed production: 100 MWp/y

**Primary Conditions to achieve 20%-Efficient
Multicrystalline Si Solar Cells**

To be achieved

Jsc=38 mA/cm², Voc=0.66 V, FF=0.79, Eff=20%

(Jsc=36.4 mA/cm², Voc=0.610V, FF=0.777, Eff=17.2%)

Key parameters

1. Higher quality cast Si : average lifetime>200μs
2. Low-cost texture technology
3. Low S at n⁺ and p⁺ surfaces: 2,000 cm/s at 2x10¹⁹cm⁻³
4. Boron BSF for thinner wafer (150μmt)
5. More effective hydrogen passivation
6. Lower shadowing loss

***How to realize government cost targets
by bulk-type c-Si approach ?***

To achieve a module cost of 147 yen/Wp
in FY 2002

- * Cell efficiency : 20%
- * Thin kerf and substrate : 150 μm

Need a new concept toward 100 yen/Wp
from FY 2003

To reduce electricity cost to 25 yen/kwh

- * Log life solar module : > 50 years (20 years)
- * High efficiency module : > 18 % (13%)

Summary

Present status

- Rapid deployment of PV market in Japan
by government subsidy policy and low bank loan.
- Prevalence of bulk-type crystalline Si module.
- Saturation of PV module price.

Future directions

- Achievement of 147 yen/Wp until 2002.
- Creation of a new concept to 100 yen/Wp in 2002.
- R&D for 50-year life solar module at 25 yen/kwh.

BEYOND WAFERS AND SILICON THIN-FILMS: THIRD GENERATION PHOTOVOLTAICS

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Most solar cells sold on the presently booming solar cell market to date have been "first generation" devices based on crystalline or "multicrystalline" silicon wafers. "Second generation" thin-film solar cells based on amorphous silicon or polycrystalline films of compound semiconductors and soon silicon, are starting to appear on the market in increasing volume and, due to inherently lower material costs, are expected to challenge "first generation" product increasingly over the next decade:

Energy conversion efficiency is a key parameter for both generations of technologies since this determines the area and hence cost for a given power rating. However, this efficiency for first and second generation technology is quite modest (less than 15%), due to the quantum nature of the conversion process (1 electron/photon) combined with other constraints. The Carnot limit on the conversion of sunlight to electricity is much higher at 95%. This leads to the possibility of a "third generation" of photovoltaic technology based on different conversion principles that allow the Carnot value to be more closely approached.

After a brief introduction to the current status of "first" and "second" generation technologies, candidates for "third generation" technologies will be outlined including hot carrier cells and a variety of schemes based on including multiple excitation processes with different energy thresholds in the one device. Low dimensional semiconductor devices feature prominently in many of these schemes for a variety of reasons to be discussed.

Electronic Transport in Amorphous / Crystalline Silicon Heterojunction Solar Cells

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Abstract

Amorphous hydrogenated silicon/crystalline silicon (a-Si:H / c-Si) heterojunction solar cells are investigated with the help of quantum efficiency, current/voltage, and capacitance/voltage measurements. The open circuit voltage and the fill factor of the a-Si:H / c-Si heterojunction solar cells under investigation are limited by recombination in the neutral zone of the crystalline Si absorber. Our best n-type a-Si:H / p-type c-Si solar has an open circuit voltage $V_{oc} = 655$ mV. This V_{oc} value already requires a recombination velocity S_{it} below 100 cm/s at the heterointerface. A further increase of V_{oc} appears only possible when changing the doping sequence to p-type a-Si:H / n-type c-Si where the band diagram is more favorable in order to minimize interface recombination.

Introduction

Heterojunction solar cells consisting of an amorphous hydrogenated silicon (a-Si:H) film on top of a crystalline silicon (c-Si) absorber are a technological alternative to c-Si solar cells with diffused pn-junctions that require a series of processing steps at high temperatures [1]. The processing of a-Si:H / c-Si solar cells is comparatively simple and the heterojunction is formed by depositing a highly doped a-Si:H layer on a crystalline silicon substrate at temperatures of 200°C or below. The high potential of such a technology was recently demonstrated by a record cell with the so-called HIT structure (Heterojunction with Intrinsic Thin layer between a-Si:H emitter and c-Si base) with a confirmed efficiency of $\eta=20.7$ % and an open circuit voltage of $V_{oc} = 719$ mV [2]. This cell type consists of an n-type c-Si absorber with a p-type a-Si:H heterojunction partner and an n-type a-Si:H back contact. In addition, the record HIT solar cell as well as its predecessors [3,4] had a textured surface to minimize reflection losses and to enhance light trapping. Obtaining the high efficiency of these a-Si:H / c-Si heterojunction solar cells still requires a relatively high number of processing steps.

The present contribution concentrates on a-Si:H / c-Si heterojunction solar cells without high-efficiency features such as surface texturing and back surface field. We analyze the electronic device properties by quantum efficiency, current/voltage, and capacitance/voltage measurements. The open circuit voltage and the fill factor of the a-Si:H / c-Si heterojunction solar cells under investigation are limited by recombination in the neutral zone of the crystalline Si absorber. Our best n-type a-Si:H / p-type c-Si solar cell prepared without high-efficiency features has an independently confirmed efficiency $\eta = 14.1$ % and an open circuit voltage $V_{oc} = 655$ mV [5].

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Solar cell preparation

The fabrication of the heterojunction solar cells starts with cleaning the c-Si wafers by ultrasonic treatment in acetone (10 min.), followed by an ultrasonic treatment in isopropanol (10 min.). Before and after each treatment, we rinse the samples in deionized water with a resistivity of 18.2 M Ω cm. Secondly, we remove the native oxide by an HF-dip (5%, 10sec). Immediately after oxide removal, we transfer the c-Si substrates into a plasma enhanced chemical vapour deposition (PECVD) chamber. The process conditions for the deposition of hydrogenated amorphous Si are: substrate temperature 150°C-160°C, deposition pressure 150 μ bar, frequency 13.56 MHz and power 4-5 W. The flow rate is 15 sccm SiH₄ for intrinsic a-Si:H and 2 % PH₃ in 16 sccm SiH₄ for highly phosphorous doped a-Si:H. The deposition rate is about 15 nm/min. The high sheet resistivity of the amorphous Si:H emitter layer imposes the use of a highly conductive and transparent contact layer to minimize resistive losses. We use an indium tin oxide (ITO) layer with a thickness of 75 - 100 nm and a sheet resistance of about 60 Ω /• deposited by radio frequency (RF) magnetron sputtering. Indium tin oxide layers are sputtered at room temperature from an In₂O₃+SnO₂ target (90/10) without oxygen addition. The argon flow rate is 20 sccm and the RF plasma power is 200 W. The ITO layer serves as a contact layer to the a-Si:H emitter and as an antireflection coating at the same time. Additionally, the ITO layer defines the cell area. A silver front grid is evaporated using a shadow mask. Contact to the c-Si absorber is provided by evaporating Pd/Al onto the full area of the back side. In case where both device contacts are placed on the solar cell front side, we etch back the a-Si:H outside the active cell area using a 3 % KOH etching solution at 80 °C for 10 s after annealing the samples at 200°C in air.

Device analysis

Compared to pn-junctions, heterojunctions as charge-separating regions in solar cells imply the drawback of possible defect states at the hetero-interface causing interface recombination as additional and possibly dominant recombination path. In most previous studies on a-Si:H / c-Si heterojunction solar cells [24,6-12] only few has been done on the determination of the recombination path that is relevant for the open circuit voltage of the devices. In the following, we concentrate on a sound analysis of the electronic transport properties of our devices by evaluation of quantum efficiency data, current/voltage and capacitance voltage curves of a-Si:H / c-Si solar cells in order to identify the dominant recombination mechanism that limits the open circuit voltage.

Quantum Efficiency Analysis

We determine losses of the short circuit current density j_{sc} in our a-Si:H/c-Si solar cells from measurements of the internal quantum efficiency Q . Figure 1 shows the internal quantum efficiency Q of (n) a-Si:H / (p) c-Si solar cells with different thicknesses of the a-Si:H emitter layer. From the curves in Fig. 2 we conclude that, apart from recombination losses in the red/infrared wavelength regime due to recombination of photogenerated charge carriers in the absorber layer, these solar cells suffer from parasitic absorption in the ITO layer. As a consequence, the maximum value of Q does not reach unity. In addition, recombination of photogenerated charge carriers in the a-Si:H emitter strongly diminishes j_{sc} . The curves a) – c) in Fig. 1 show Q of a-Si:H / c-Si solar cells with increasing emitter thickness from a) to c). An increase of the a-Si:H emitter thickness deteriorates the blue response of our solar cells significantly. Hence, the emitter thickness should be kept as thin as possible. However, the

reduction of the emitter thickness is limited by technological problems of depositing a continuous a-Si:H layer without generating shunt paths by the subsequent process steps.

Current / voltage characteristics and open circuit voltage limitations

The determination of the dominant recombination mechanism in diodes requires a proper analysis of the diode ideality factor n . As one among other [5] evaluation schemes for the diode ideality factor, we measure I_{sc} and V_{oc} under different illumination intensities as shown in Fig. 2a). Since, at open circuit conditions, no current flowing through the device, I_{sc} and V_{oc} are interconnected by the diode law with the unknown saturation current density j_0 and diode ideality factor n . By measuring at two slightly different illumination intensities, one can solve for the diode ideality factor n . Thus, Fig. 2b) shows diode ideality factors and, we find n close to unity over the voltage range that is relevant for the respective V_{oc} .

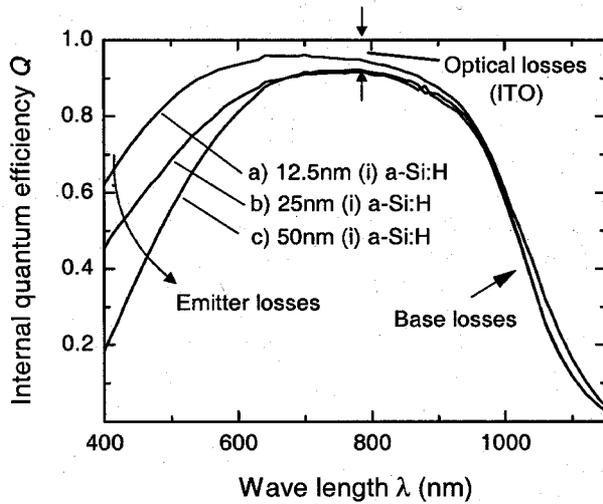


Figure 1: Internal Quantum Efficiency Q of a series of (n) a-Si:H / (p) c-Si solar cells with different thickness of the (i) a-Si:H layer (12.5, 25, and 50 nm). Apart from recombination losses in the red/infrared region (base losses), parasitic absorption in ITO (optical losses) and recombination in the amorphous silicon (emitter losses) diminish the short circuit current density j_{sc} .

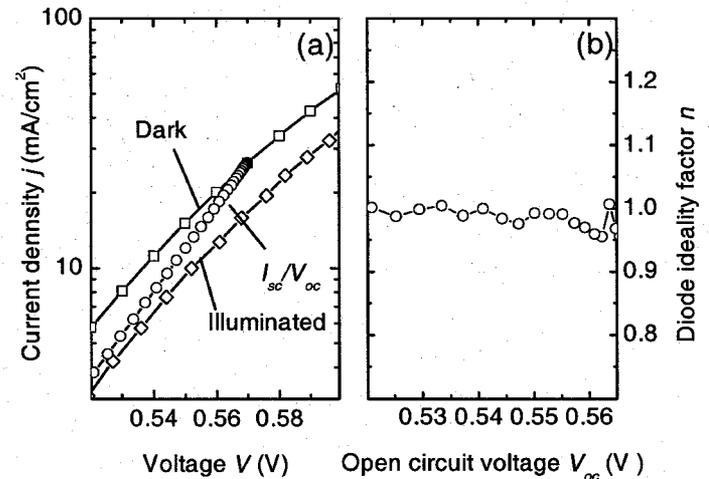


Figure 2: (a) Semilogarithmic representation of dark current density vs. voltage characteristics during illumination (after subtraction of the short circuit current density). In the same plot we draw j_{sc} vs. V_{oc} values obtained at various illumination intensities. (b) Voltage dependence of the diode ideality factor n from the semilogarithmic derivative of the j_{sc}/V_{oc} curve in (a).

An ideality factor $n = 1$ is expected for diffusion and subsequent recombination of minority carriers in the neutral zone (NZ) of the c-Si absorber as dominant transport mechanism. The open circuit voltage V_{oc} for solar cells *limited by NZ-recombination* reads (Eq. (4) in [13])

$$V_{oc} = \frac{E_g}{q} - \frac{kT}{q} \ln \left(\frac{q D N_c N_v}{N_d j_{sc} L_{eff}} \right) \quad (1)$$

where E_g equals the bandgap energy and kT/q is the thermal energy. The quantity D denotes the minority carrier diffusion constant, N_c (N_v) the effective density of states in the conduction (valence) band, L_{eff} is the effective diffusion length and N_d denotes the doping density of the absorber material. Equation (1) connects V_{oc} with material constants of c-Si and with quantities such as N_d and L_{eff} , which are accessible by independent measurements. Note that the ef-

fective diffusion length L_{eff} is a function of the minority carrier lifetime τ and the surface recombination velocity S_B at the back contact [14]. For bulk diffusion lengths $L_D = (D\tau)^{1/2}$ exceeding the thickness of the neutral region, L_{eff} is likely to be determined by S_B .

We determine the effective diffusion length L_{eff} of our a-Si:H/c-Si solar cells from the red/infrared regime of the quantum efficiency Q (c.f. Fig. 1). Plots of the inverse quantum efficiency Q^{-1} versus absorption length of the incident photons yield the effective diffusion length L_{eff} [14]. The doping density N_d is determined by capacitance/voltage (C/V) measurements. The symbols in Fig. 3 show open circuit voltages of a-Si:H/c-Si solar cells with crystalline silicon absorbers having different values of N_d and L_{eff} . The V_{oc} -limit imposed by NZ-recombination of Eq. (1) is shown as a straight line. All our a-Si:H/c-Si solar cells show experimental open circuit voltages very close to this limit. Particularly, the fact that Eq. (1) describes the open circuit voltage of our solar cells *with different N_d and L_{eff}* identifies recombination in the NZ of the absorber to be the limiting mechanism for V_{oc} .

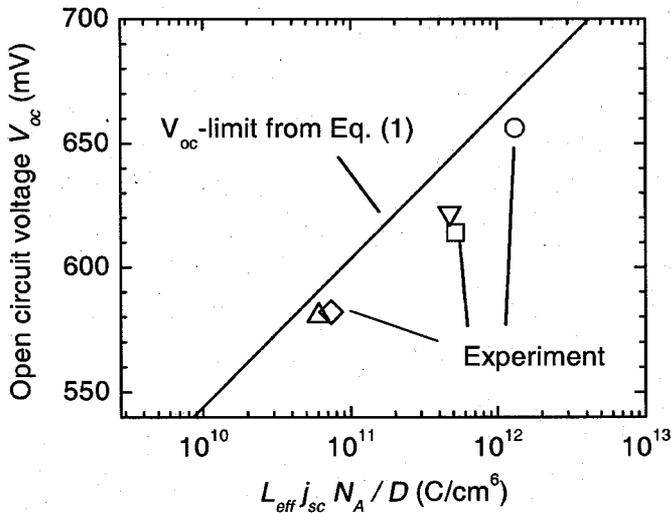


Figure 3: Open circuit voltage V_{oc} of various a-Si:H / c-Si solar cells with different c-Si absorbers (listed in Table 2). The straight line shows the V_{oc} limitation of Eq. (1).

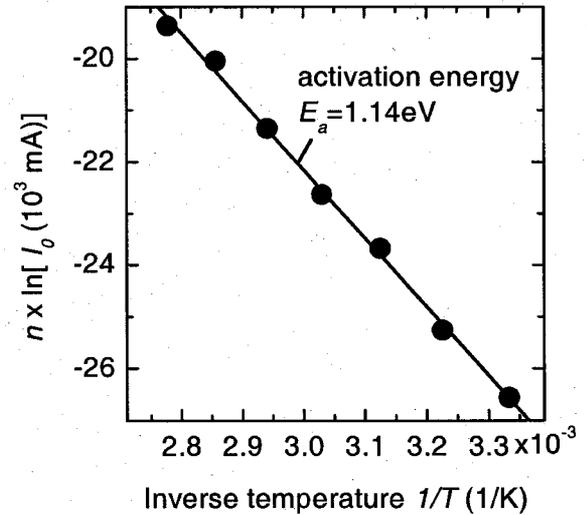


Figure 4: Temperature dependence of the saturation current density j_0 in a modified Arrhenius plot. A fit to the measured data yields an activation energy of $E_a=1.14\text{eV}$.

To strengthen this observation and definitely exclude recombination at the a-Si:H/c-Si interface from limiting V_{oc} , we also investigate the temperature dependence of the saturation current

$$I_0 = I_{00} \exp\left(\frac{-E_a}{nkT}\right) \quad (2)$$

Here, I_{00} is a weakly temperature dependent prefactor which is different for each recombination mechanism and E_a is the activation energy for the recombination process [13]. The diode ideality factor n enters into the thermal activation of the saturation current as shown in Eq. (2). Thus a plot of $n \ln I_0$ versus the inverse temperature $1/T$ yields the relevant activation energy E_a of the recombination mechanism. In the case of bulk recombination, we expect $E_a = E_g$, whereas for interface recombination we expect $E_a = \Phi_B$, where Φ_B is the effective barrier height for charge carriers from the c-Si absorber to recombine at the interface. Figure 4 shows such a plot of $n \ln I_0$ versus the inverse temperature $1/T$ for a (n) a-Si:H / (p) c-Si heterojunction solar cell. We find an activation energy of $E_a = 1.14 \text{ eV}$, which is very

close to the band gap energy $E_g = 1.12$ eV of crystalline silicon. Apart from our result that the measured open circuit voltages of our a-Si:H / c-Si solar cells are very close to the theoretical limit imposed by neutral zone recombination, this finding of E_a nearly equal to E_g is a second proof that recombination in the neutral zone of the c-Si absorber limits V_{oc} . Thus, recombination at the a-Si:H / c-Si interface is subsidiary with regard to the boundary of V_{oc} . Our best (n) a-Si:H / (p) c-Si (FZ) heterojunction solar cell with a doping density of $N_d = 5 \times 10^{16} \text{ cm}^{-3}$ of the c-Si wafer has an independently confirmed open circuit voltage $V_{oc} = 654.5$ mV, a short circuit current density $j_{sc} = 26.65 \text{ mA/cm}^2$, and a fill factor $FF = 81 \%$ [5].

Capacitance / Voltage measurements

In the previous section we have shown that recombination within the neutral zone limits the open circuit voltage V_{oc} of our a-Si:H / c-Si solar cells. Thus, the choice of the c-Si absorber material, its minority carrier lifetime and doping density, as well as the reduction of the backside recombination velocity S_B are the key to V_{oc} improvements. However, with increasing absorber quality one will approach the limitation of V_{oc} by recombination at the a-Si:H / c-Si interface. The V_{oc} limit imposed by interface recombination reads [15]

$$V_{oc} = \frac{\Phi_B}{q} - \frac{nkT}{q} \ln \left(\frac{q N_v S_{it}}{j_{sc}} \right), \quad (3)$$

where S_{it} is the interface recombination velocity. According to Eq. (3) the effective barrier Φ_B for recombination of charge carriers from the c-Si absorber at the interface should be as high as possible in order to achieve a high open circuit voltage V_{oc} . To estimate Φ_B , we need more information about the band diagram of (n) a-Si:H / (p) c-Si and its (p)/(n) counterpart.

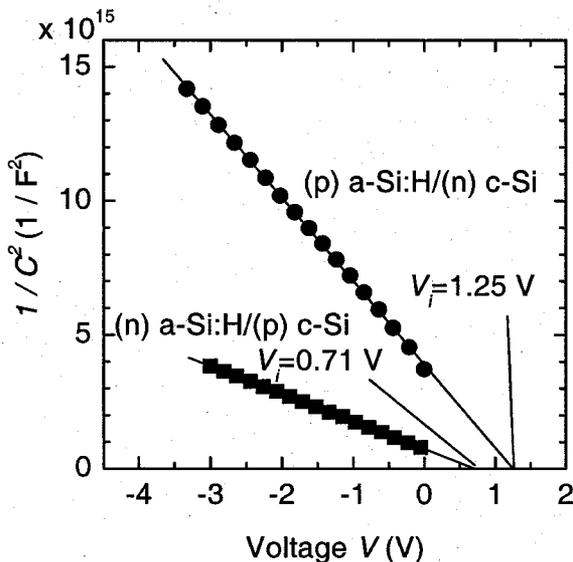


Figure 5: Mott-Schottky plots of capacitance vs. voltage data from an (n) a-Si:H / (p) c-Si (sample A in Table 2) and from a (p) a-Si:H / (n) c-Si heterojunction solar cell (sample C in Table 2). The intercept V_i with the voltage axis yields the built-in voltage. We find a significantly larger built-in voltage for the (p) a-Si:H / (n) c-Si structure compared to its counterpart.

Figure 5 compares the C^{-2} / V (Mott-Schottky) plots of a (n) a-Si:H / (p) c-Si and a (p) a-Si:H / (n) c-Si heterostructures. The data are taken at room temperature and test frequency $f = 100 \text{ kHz}$. The intercept V_i with the voltage axis equals the built-in voltage V_{bi} of the device, reduced by $2kT/q$ when neglecting interface states and a dipole effect [16]. We find an intercept voltage of $V_i = 1.25 \text{ V}$ for the (p) a-Si:H / (n) c-Si structure, a value that is considerably larger than the intercept voltage $V_i = 0.72 \text{ V}$ of the (n) a-Si:H / (p) c-Si structure. From the schematic band diagrams of Fig. 6 we find for the difference of the band discontinuities [5]

$$\Delta E_C - \Delta E_V \approx 0.56 \text{ eV}. \quad (4)$$

This simple evaluation shows that the valence band offset ΔE_V is much larger than the conduction band offset ΔE_C , which is in good agreement with the determination of ΔE_V from the current/voltage behavior at low temperatures [17]. Thus, the (p) a-Si:H / (n) c-Si structure has a higher built-in voltage at the crystalline silicon part than its counterpart. In good approximation, the Fermi level of the (p) a-Si:H / (n) c-Si structure (see Fig. 6) at the interface is close to the valence band edge resulting in an inversion layer. Thus, the effective barrier height Φ_B is given by $\Phi_B = E_g$, whereas $\Phi_B < E_g$ holds for the (n) a-Si:H / (p) c-Si structure. As a consequence, for a given interface recombination velocity S_{it} the open circuit voltage V_{oc} in the (p) a-Si:H / (n) c-Si structure will be higher than in the (n) a-Si:H / (p) c-Si counterpart (see Eq. 4). In this regard, Fig. 7 shows calculated values for the open circuit voltage V_{oc} in case of dominant interface recombination as well as for dominant neutral bulk recombination with the assumption of a doping density $N_d = 4.6 \times 10^{16} \text{ cm}^{-3}$ and an effective barrier height $\Phi_B = 0.72 \text{ eV}$ in the (n) a-Si:H / (p) c-Si structure and $\Phi_B = E_g = 1.12 \text{ eV}$ in the (p) a-Si:H / (n) c-Si counterpart.

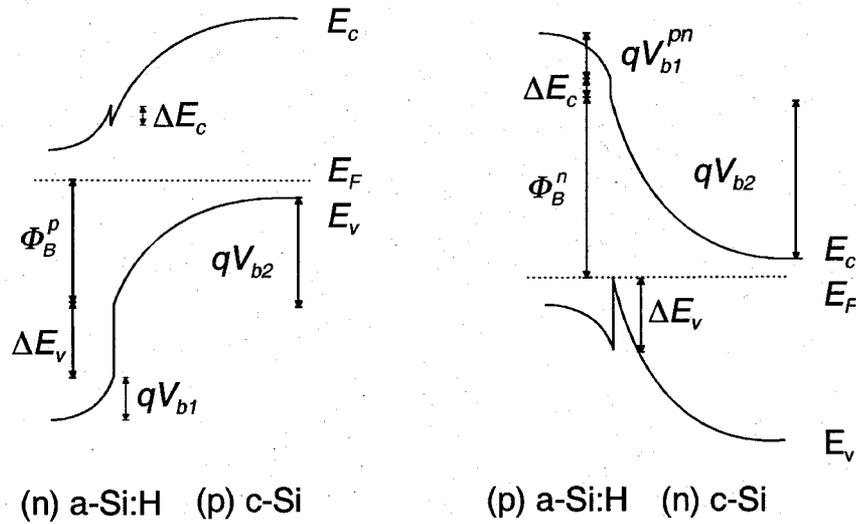


Figure 6 : Schematic band diagram of a (n) a-Si:H / (p) c-Si (left) and (p) a-Si:H / (n) c-Si heterojunction (right). The barrier height Φ_B is, according to Eq. (4), one limiting factor of the open circuit voltage in case of interface recombination. The higher built-in voltage V_{b2} and thus, the higher effective barrier height, in the (p) a-Si:H / (n) c-Si heterojunction compared to its counterpart corresponds to the capacitance/voltage measurements of Fig. 5.

Most groups working on a-Si:H/c-Si heterostructure solar cells select the (n) a-Si:H / (p) c-Si structure, often justified by the higher bulk diffusion length of electrons compared to holes. Additionally, a low-resistivity contact on moderately doped p-type c-Si is easier to achieve than on n-type c-Si where one has to use a backdiffused n^+ layer or an a-Si:H back surface field as it was done by the Sawada et al. [3]. However, the achievement of open circuit voltages in excess of 700 meV [3] appears to justify this effort. From Fig. 7, we conclude that such a high V_{OC} is hardly to obtain when using p-type c-Si, unless the interface recombination velocity S_{it} is brought to values below 10 cm/s.

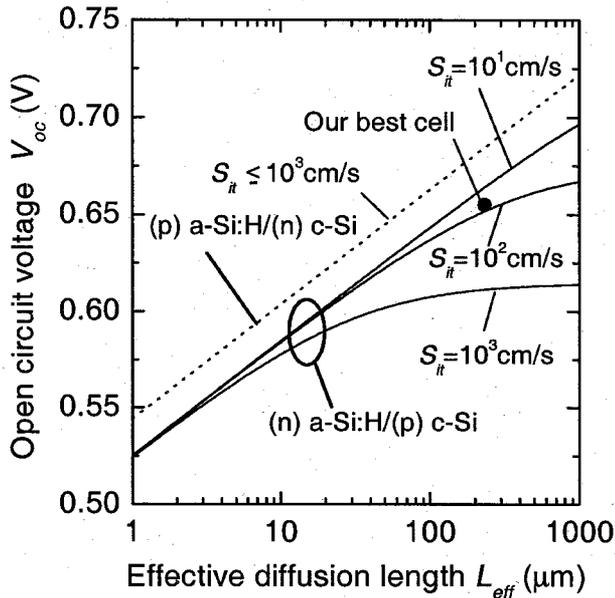


Figure 7 : Open circuit voltage V_{oc} of a-Si:H / c-Si heterojunction solar cells computed from Eqs. (1) and (3) using the built-in voltage V_{bi}^{np} and the doping $N_A = 4.6 \times 10^{16} \text{ cm}^{-3}$ from Fig. 5. Different interface recombination $S_{it} = 10^3$, 10^2 , and 10 cm/s imply differences in V_{oc} as long as the effective diffusion length L_{eff} is larger than $10 \mu\text{m}$. The data point corresponding to our best cell implies an interface recombination velocity of around 70 cm/s . The dotted line corresponds to computed values for a (p) a-Si:H / (n) c-Si heterojunction with $\Phi_B^n = 1.12 \text{ eV}$, such that even with a less favorable S_{it} of 10^3 cm/s open circuit voltages in excess of 700 mV are possible.

Conclusions

We have fabricated a-Si/c-Si heterojunction solar cells by depositing amorphous hydrogenated silicon by plasma enhanced chemical vapour deposition. Our best solar cells show a certified conversion efficiency of 14.1% without high-efficiency features such as light trapping and / or a back surface field. The dominant recombination path in our solar cells is recombination in the neutral zone of the c-Si absorber. Therefore a careful selection of the absorber doping density, both concerning maximum V_{oc} as well as high FF is indispensable. From our modeling and from capacitance / voltage measurements we find that, in the high efficiency limit interface recombination sets an upper bound to the open circuit voltage. Our best V_{oc} of 655 mV obtained from a (n) a-Si:H/ (p) c-Si heterostructure already requires a recombination velocity $S_{it} \leq 100 \text{ cm/s}$ at the a-Si:H/c-Si interface. Thus, the more favorable band diagram of the (p) a-Si:H / (n) c-Si structure (Fig. 6) used in the recent record devices [2,3] has an inherent advantage to obtain higher open circuit voltages.

Acknowledgment

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The impact of TCOs on next-generation solar cells

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Transparent conducting oxides (TCOs) are an integral part of all thin-film solar cells. They are used as window layers through which the incoming light must pass on its way to the absorbing part of the device and as conducting layers to extract the photogenerated current. The physical properties of the TCO have not, thus far, been a limiting factor to the performance of solar cells but, we assert, this is likely to change with the increasing demands off the manufacturing industry and with several other techno-economic constraints. In particular, the limited world reserves of indium, one of the important components of indium tin oxide (a traditional TCO) may necessitate the development of new TCOs. In addition, the prospective emergence of novel devices such as tandem thin-film solar cells may require enhanced properties as well as completely novel materials.

In this paper, we discuss the fundamental principles of operation of transparent conducting oxides (TCOs) and highlight the critical parameters that determine their electrical resistivity and optical transmittance, which are the quantities of importance for most practical applications such as solar cells and flat-panel displays. We then continue by reviewing work at NREL, and elsewhere, on relatively novel TCOs. In particular, we shall briefly discuss our data on cadmium stannate and cadmium oxide.

Finally, we discuss modeling of the likely performance of high-efficiency thin-film tandem solar cells. Work on these has recently been started at NREL and its subcontractors under the aegis of the Department of Energy's High Performance Initiative. The goal of this initiative is to achieve a laboratory device with an efficiency of 25% within a ten-years. Possibly surprisingly, the design of the devices and their achievable efficiency depend strongly on the quality of the TCO that will be used as a top contact and, possibly, elsewhere in the device. Without careful attention to the choice of the TCO, the 25% goal will not be attainable. In particular, we show that the carrier concentration must be minimized and the mobility kept as high as possible.

RESONANCE ULTRASONIC DIAGNOSTICS OF ELASTIC STRESS IN SILICON WAFERS

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We developed a procedure to assess elastic quality in full-size microcrystalline (mc) Si wafers using resonance acoustic effect recently observed in Cz-Si [1]. Experimentally, the acoustic vibrations in a frequency range of 10 to 30KHz are generated into a wafer, using external piezoelectric transducer. The wafer is coupled with the transducer and resonates at specific frequencies, which depend on geometry of the wafer and elastic modulus of material. The vibration amplitude and frequency are recorded in a non-contact mode using an air-coupled acoustic probe. Computer controlled system allows to scan acoustic picture in a mapping mode. In Cz-Si we observed amplification of a specific acoustic mode referred as a "whistle". A critical issue of the method is a damping of the whistle amplitude when the internal stress in a wafer due to crystal growth or thin film deposition is created. Initially, this approach was developed and tested in full-size 8" Cz-Si [2]. Mapping of the acoustic amplitude identified the whistle with high-order flexural vibrations in a thin elastic plate. Theoretical calculations of the flexural resonance are performed using a simplified model of a circular or square plate with free edge [3]. The model allowed predicting resonance frequencies in full-size wafers of different size and geometry. Feasibility experiments showed that the resonance acoustic method is applicable to Cz-Si and mc-Si wafers and solar cells.

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Handling of Crystalline Silicon Solar Cells in High Throughput Production Tools

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Introduction

The contribution of breakage-induced yield losses in manufacturing costs is well understood. Breakage data and information about the solutions implemented by cell manufacturers have a proprietary nature and are much less well known. In this paper we discuss the cell handling requirements of crystalline silicon solar cell manufacturers and review a small but significant portion of the published quantitative analytical work on this subject. In addition we present data obtained with two machines designed and manufactured by NPC and used in module assembly operations. On this basis, we propose topics where industry collaboration with the research community could result in advantages for all cell manufacturers.

Crystalline Silicon Cell Manufacturing

Shipments of Solar Electric products based on crystalline silicon solar cell materials reached 287.65 MW in 2000 [1], which accounts for over 80% of total shipments. Eight crystalline silicon cell manufacturers with capacities in excess of 12 MW account for over 75% of the shipments. As a trend towards large factories seems to be materializing, these crystalline silicon manufacturers are increasingly automating their facilities.

The prevalence of crystalline silicon technology seems to be assured well into the era of new factories with capacities in the hundreds of MW. As manufacturers expand capacity, cell handling at high throughput and low breakage emerges as a major technical barrier.

An analysis of the U.S. Photovoltaic Industry Roadmap recommendations shows that cell handling will influence the outcome of efforts to overcome technical barriers through focused R&D. A key technical barrier is “the need for an improved manufacturing infrastructure to increase throughput and yield” [2]. Development of high throughput, production-hardened cell manufacturing tools will be a key step in making solar electric power a reality for all.

Crystalline silicon cell manufacturing is converging on a set of standard production tools (see for example reference [3]) including ingot growth, wafer sawing, damage removal, diffusion, printing and firing of a Thick Film Paste (TFP) metallization and CVD of TiO_2 or Si_3N_4 . Wafers used in the solar cell industry have a wide range of sizes, typically from 100 mm to 200 mm, and thickness in the range from about 100 to over 500 microns. Cost and availability of solar-grade silicon are driving many manufacturers toward the use of thin wafers.

Production tools consist of modular units that load, process, and unload cells. After wafer sawing, cells are generally handled within and between these modules in cassettes or by belts or grippers. As manufacturing throughput increases cell accumulation in cassettes

is, where possible, being excluded. Cell testing and module assembly operations utilize similar cell handling techniques.

Cell Handling Cost Demands on Manufacturing Tools

Industry growth is posing increasing demands on production tools. As in the semiconductor industry before, the emphasis is moving from price and process performance to more inclusive metrics. In analyzing cell production tools it is useful to utilize the concept of Cost of Ownership (CoO), a SEMI standard developed by the semiconductor industry under Sematech as a decision tool and benchmark to evaluate process system options and return on capital equipment investment (see for example reference [4]). CoO is defined as "The full cost of embedding, operating, and decommissioning in a factory environment a process system needed to accommodate the required volume of product material" (SEMI Standard E-35: Cost of Ownership for Semiconductor Manufacturing Equipment). The algorithm that describes CoO includes fixed costs FC, recurring costs RC, yield cost YC, equipment life L, throughput T, yield Y and utilization U:

$$\text{CoO} = [\text{FC} + \text{RC} + \text{YC}] / (\text{L} \cdot \text{T} \cdot \text{Y} \cdot \text{U})$$

Manufacturing tools must be cost effective not only in purchase price [5] but also in tool reliability (including maintainability), throughput, and yield. We note that, in the CoO algorithm yield losses have a double impact: the yield cost YC increases total cost while the yield Y decreases the effective throughput. Breakage losses are a key factor in the cost performance of a process tool and need to be reduced well below 1% to achieve a high overall yield in a typical multi-step cell manufacturing process.

Cell manufacturers are moving toward capacity expansion increments of the order of tens of MW. To meet expansion requirements with a small number of single-string production tools, machine throughputs in processing and automation need to substantially exceed 10 m² of silicon wafers per hour. This translates into typical throughput specifications by manufacturers of well over 1,000 cells per hour, with breakage below 1% for cells with thickness as low as 100 microns. To achieve this, substantial collaboration between manufacturers, their suppliers and the research community will be needed.

Research methodology

A significant initial effort to understand and characterize the fracture mechanics of silicon wafers in a cell-manufacturing environment was conducted within the Flat-Plate Solar Array Project [6]. The first automated cell interconnect machines were manufactured by ARCO Solar and Kulicke & Soffa as part of this project. Results from this effort include the development of a standard fracture-mechanics test and analysis methodology [7]. In this method, applying stresses to silicon wafers in a four-point twisting arrangement generates fracture strength data. The data are then described by Weibull statistical analysis [8], where it is assumed that fracture at the most critical flaw under a given stress distribution leads to total failure. Weibull statistical analysis involves a plot of the fracture probability as a function of fracture strength for several production processes. Analysis of data from 3" Cz wafers provided by Motorola at each step in the cell manufacturing process was used to describe the effect of processing on fracture strength. A significant result of this work is that fracture strength increased as a result of some processes such as chemical polish, texture-etch, mesa etching, and antireflection coating. Other processes such as metallization generated or extended edge chips and surface flaws leading to a decrease of fracture strength. This research also suggested an approach to

eliminating flawed wafers, which often increase yield costs by causing other wafers to break, at critical process steps. Typically, a long tail is observed in the low-stress portion of the Weibull distribution. By applying a dynamic fatigue test to 2" Cz wafers C.P. Chen et al. [9] showed that the strength distribution was truncated by this testing suggesting that this method can be used to eliminate weak samples that can break in subsequent processing and increase yield costs.

More recently Solarex (now BP Solar) developed automated cell handling equipment for 200 micron thick 15 cm x 15 cm polycrystalline silicon wafers under a PVMat contract [10] in collaboration with the Automation and Robotics Research Institute (ARRI) at the University of Texas at Arlington. ARRI applied a four-point bend test to measure mechanical strength. Weibull analysis was used to estimate the maximum load allowed in a typical cell-handling situation. ARRI used the data to design a four-point vacuum gripper end-effector that can be used with a robot arm or a Cartesian manipulator to pick up and release wafers to and from horizontal surfaces, such as cell stacks. This end-effector was implemented in a cell matrix positioning operation in module assembly.

A survey by the ARRI of the cell manufacturing technology of eleven U.S. based companies provides an excellent review of equipment and automation strategy opportunities [11].

Current Cell Handling Achievements - NPC Production Tools

NPC Incorporated designs, manufactures and sells test and assembly tools for the Solar Electric industry that incorporate cell handling equipment operating at high throughput rates and high yield. Since 1996, through NPC America, the NPC Group has collaborated with US cell manufacturers to achieve this result. Beginning in 2001 NPC America has begun a program to work with the national laboratories and universities in the US to extend its capabilities as a supplier of both cell and module manufacturing equipment.

A cell tester (NCS-150) supplied by NPC can test cells at a rate of one cell every 2.6 seconds, or close to 1,500 cells per hour (Figure 1). Similarly, a commercial NPC tabber-stringer (NTS-150) has a rate of 600 to 800 cells per hour (Figure 2). The NPC end-effector design used in the pick-and-place mechanism of these machines, similar to that described by Solarex, insures the low breakage and high yield in testing and tabbing-stringing.

Figure 3 shows defect data from a NPC tabber-stringer machine operating since 1997. Over 150,000 10 cm by 10 cm, 180 micron thick cells were processed into over 1,500 strings of 9 to 12 cells in 14 production days. Cell breakage due to the tabbing-stringing operation itself was due to both, pre-existing cell defects and handling by the tabber-stringer. Machine-induced and cell induced breakage were below 1% on the average, reaching a daily maximum of 1%. Other defects include front and back tab peeling and tabbing ribbon misplacement. The low breakage level observed is typical of both, tabber-stringer and cell tester.

NPC has obtained promising data on breakage of very thin solar cells. For 100-micron thick cells in a cell testing operation using a customized version of the NCS-150 machine, only 3 cells were broken out of 483 tests; that is a breakage rate of 0.6% consistent with that observed in Figure 3 for 180 microns thick cells.

Figure 1: NPC Cell Selector NCS-150

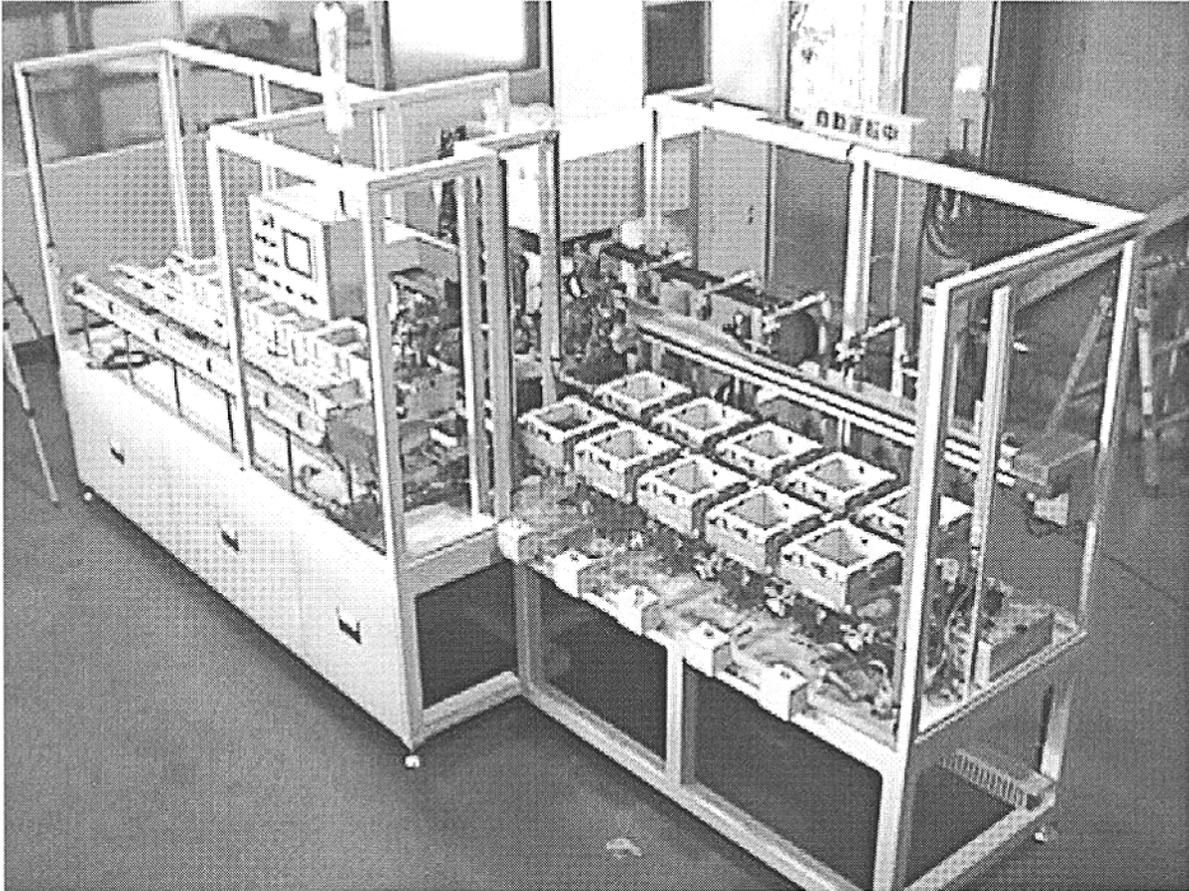


Figure 2: NPC Tabbing & Stringing Tool NTS-150

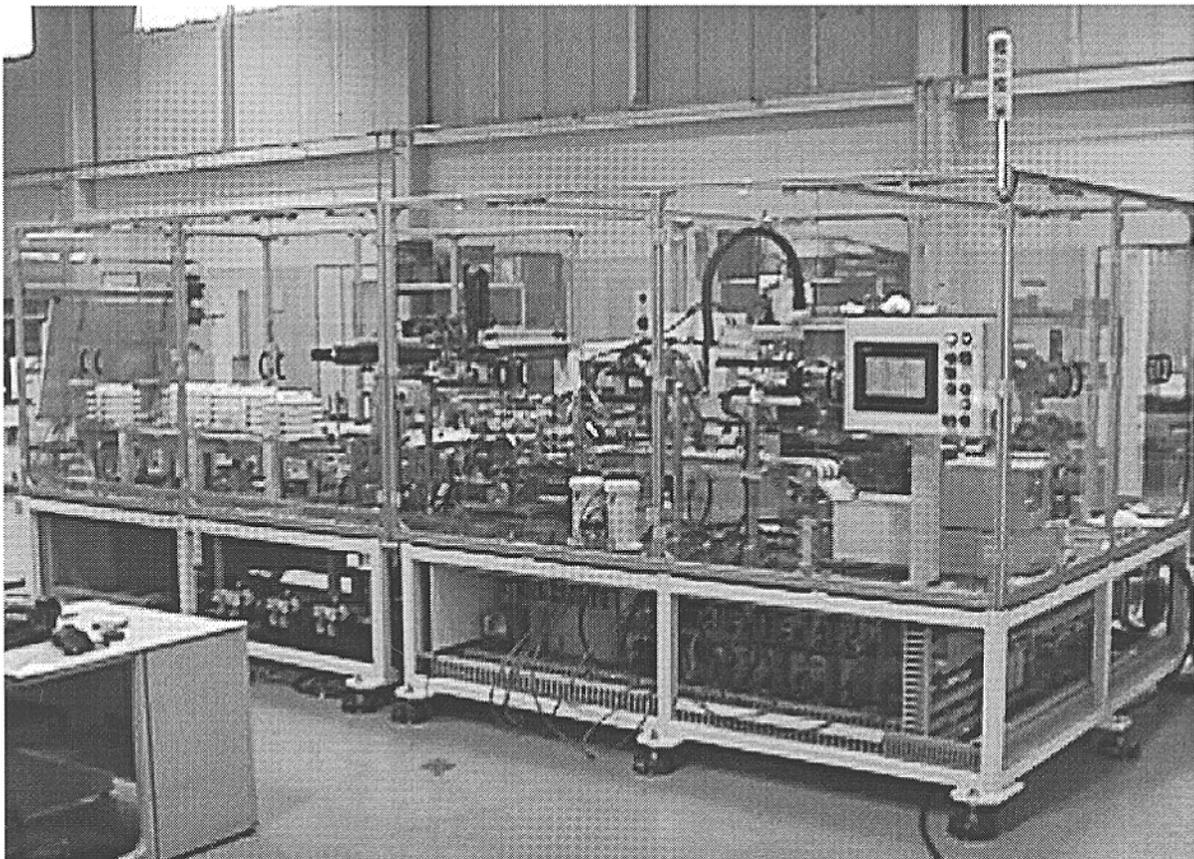
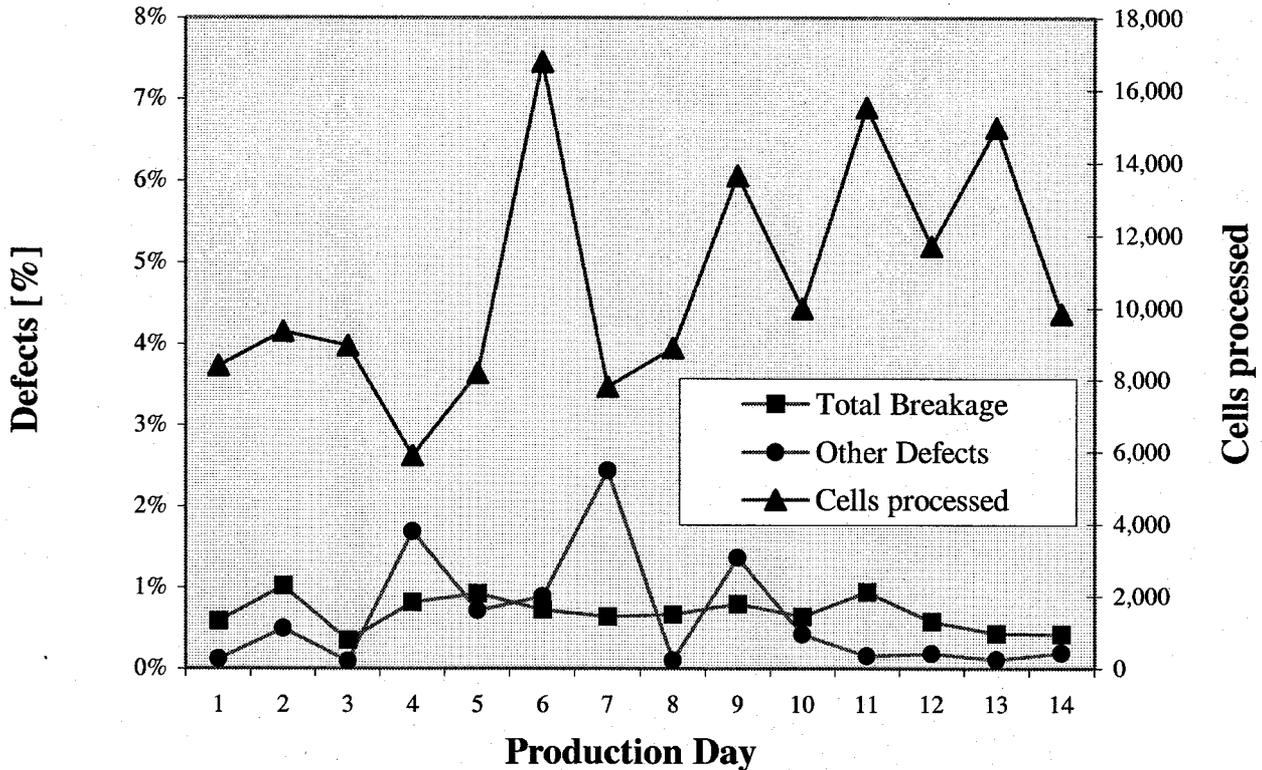


Figure 3: Breakage and defect data from NPC tabber-stringer



Clearly, machine throughput depends on both, handling and process speed. The difference between data acquisition and soldering times accounts for the difference in throughput between the NCS-150 and the NTS-150 units. We estimate that the raw cell handling speed in NPC machines is of the order of one cell every 1.5 seconds, or over 2,400 cells per hour. Further gains in machine throughput particularly for tabbing and stringing can be obtained as a result of decreasing process times. Machine throughputs in excess of a few thousand cells per hour will require innovative technology.

Conclusions and Recommendations

Methods developed in the semiconductor industry to improve benchmarking of capital equipment can be useful to the analysis of cell handling and its effect on costs. The research methodology applicable to the task of understanding and improving cell handling has been developed and is being applied.

Production tools available, exemplified by the NPC machines, can achieve cell-handling throughputs of well over 1,000 cells per hour with breakage below 1%.

Among the specific research topics that could enhance collaboration between cell manufacturers and equipment suppliers are:

- Application of the methodology developed by JPL to characterize fracture strength to the large variety of silicon wafers utilized by the industry. This would include characterization of fracture strength for each wafer as a function of process in the manufacturers plant.
- Development of new processes to decrease tool process time, as opposed to cell handling time.

- Development and use of benchmarks to assist industry decision-making on manufacturing equipment.

The establishment of a Manufacturing Center of Excellence where cell and equipment manufacturers would collaborate with the U.S. research community in the solution of common problems, consistent with U.S. Photovoltaic Industry Roadmap recommendations, would assist in implementing these steps.

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HYDROGEN IN CRYSTALLINE SILICON FOR SOLAR CELLS

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Abstract : Hydrogen is well known to produce beneficial effects in crystalline silicon. It passivates dopant atoms, it neutralizes recombination centers and it passivates the surfaces. Hydrogenation of multicrystalline silicon wafers is one of the best way to increase the material quality as well as the conversion efficiency of solar cells.

The lack of stability of such improvements was a limiting factor, but the use of plasma enhanced deposition of a hydrogen rich silicon nitride film gives rise to a dramatic improvements : an excellent antireflection coating is obtained, the emitter surface of the cell is passivated, the electrical base quality is strongly improved.

In addition, hydrogen develops interesting effects like the enhanced formation of thermal donors in oxygen rich silicon, the formation of nanocavities which induces gettering of metallic impurities, the conversion of p-type to n-type silicon.

All these effects are described and discussed in this paper and different hydrogenation techniques are proposed particularly those based on plasma ion implantation. A comparison is also done with another techniques of material improvement : the phosphorus diffusion.

1. INTRODUCTION :

It is well admitted that hydrogen has an important role in improving the electrical properties of semiconductors. It was soon established that atomic hydrogen passivates the electrical activity of both acceptor and donor dopants in silicon, as well as that of deep-level impurities. Deep-level passivation is more thermally stable than shallow-level passivation and has more practical passivation, although the passivation mechanism is not yet clearly understood.

Hydrogen diffuses easily in silicon, especially via dislocations and modifies the electrically dopant profile close to the surface or passivates the deep level associated to the dislocations. In p-type material it is in a positive charge state (H^+), while in n-type it may be in a negative one (H^-), and its motion can be influenced by internal or external electrical fields.

H^+ species is a very fast diffuser ($D \cong 10^{-10} \text{ cm}^2/\text{s}$ at room temperature) in lightly doped silicon where acceptor trapping is minimal, but the diffusivity is strongly reduced in imperfect and highly doped materials.

The passivation of deep levels by atomic hydrogen is relatively stable, as temperatures around 450°C are needed to reactivate the passivated deep levels. This is a disadvantage compared to the removing of deep-levels associated to metallic impurities resulting from external gettering treatments. However the use of Si_3N_4 layers deposited by plasma enhanced CVD in hydrogen ambient has given a new chance : such a layer behaves as an hydrogen reservoir and is an antireflection coating. Although there are still many unknowns about the

properties of hydrogen in silicon it is sure that it is needful in each processing step to use an hydrogen ambient, voluntary or involuntary. An improvement is always observed.

The present paper describes some beneficial effects of hydrogen and some peculiar properties which may be of interest for silicon solar cells.

2. HYDROGENATION TECHNIQUES :

Hydrogen can be easily introduced in an intentional and controlled manner or in unintentional ways. It is emphasized that atomic hydrogen is the active species for defect and impurity passivation as well as dangling bonds saturation.

2.1. Hydrogen plasma exposure (plasma immersion implantation)

The exposure of the wafers at a low power-density plasma is sufficient to introduce a significant dose of hydrogen which can modify the electrical properties of the samples.

The system consists of a quartz tube through which molecular hydrogen is pumped at a reduced pressure (0.3 torr – 1 l/min). The plasma is excited by capacitively or inductively coupling low frequency ($\cong 50$ kHz) or radio-frequency (13,56 MHz) power (0.1 to 1 W/cm²) via a high frequency oscillator. The samples may be heated between 100 and 400°C, and maintained in the plasma for 30 min to few hours. High doses of ions can be introduced ($> 10^{16}$ cm⁻²) [1].

However energetic ions and electrons are also produced with energies in the range 100 eV to 1 keV and therefore near-surface damages can be created.

2.2. Low energy ion beam implantation

Ions can also be implanted at low ion energy and high beam current. They are produced by a Kaufman sources [2]. Such sources have a number of advantages like control of H⁺ ion dose, dose rate and shorter exposure times (few min). However there is an extensive damage to the near surface region. High hydrogen concentrations can be incorporated up to 25 at. % ! The sample is held at elevated temperatures (up to 150°C) because of the beam heating.

2.3. High energy ion implantation

Hydrogen ions can be deeply implanted when conventional ion implanters are used with energies in the range 20 to 400 keV (the projected range is about 1 μ m per 100 keV in silicon [3]). Of course at such energies lattice damage are produced and the sample must be annealed in order to restore the crystal, but hydrogen out diffuses. However if the dose is higher than 10^{16} cm⁻², hydrogen bubbles are formed around the projected range and they can be transformed in nanocavities during subsequent annealings at temperatures higher than 350°C.

2.4 Hydrogenation by means of a silicon nitride layer

Hydrogen can also be introduced in silicon after deposition of a Si₃N₄ layer by plasma enhanced chemical vapor deposition (PE CVD) in an hydrogen ambient[4]. When this structure is annealed (or fired) at 500°C – 600°C hydrogen diffuses into silicon. Such a technique appears to be very suited for solar cells as it will be shown later.

2.5. Hydrogenation in gas flow

Hydrogenation of silicon samples may result also of a simple annealing in hydrogen gas flow or in forming gas when the samples are heated at 300°C. It was suggested that molecular hydrogen is ionised at the surface defects and ions can diffuse into the material. Unfortunately the effects are less marked compared to those of the preceding techniques, a n-type layer impedes the diffusion of hydrogen into the bulk and the technique cannot be applied to finished solar cells.

3. PASSIVATION OF DEEP LEVELS IN SILICON :

Although the mechanisms by which this occurs is not clear today, the passivation of deep levels is the most important effect for solar cells made with imperfect silicon, especially for multicrystalline silicon.

What it is expected ? Essentially the passivation of grain boundaries, of intragrain defects like dislocations, dissolved and precipitated impurities (metallic atoms ; oxygen) or impurity-crystallographic defect complexes.

3.1 Impurities

Impurities like Au, Fe, Ni and Cu are easily introduced in silicon during high temperature processing steps, or they may be present in the as-grown crystal in the form of metallic clusters, as it is generally observed in multicrystalline silicon (mc-Si).

Their passivation is achieved by immersion of the silicon wafer to a low pressure plasma. The depth to which the particular impurities are neutralized depends on the density of sites to which the hydrogen can bond, on the temperature of the sample and the duration [5]

Passivation was first ascribed to hydrogen binding to defective bonds associated with the impurities, and it was concluded that the neutralization depth was simply the incorporation depth but that was never well verified. It may be that a sufficient concentration of hydrogen is needed in order to produce a noticeable passivation and an improvement of the wafers.

Subsequent annealing of the sample in vacuum at 450°C, causes a complete reappearance of the defects states and is ascribed to the breaking of the hydrogen – impurity bond or of the dehydrogenation of dangling bonds

Metallic impurities like iron, copper, chromium, are passivated and the reduction of their recombination activity is well controlled by deep level transient spectroscopy (DLTS).

In Cz wafers, which contain interstitial oxygen atoms to concentrations about 10^{18} cm^{-3} , thermal donors are formed at 450°C and also between 550 and 800°C (new donors). It has been demonstrated that both the 450°C donors and the new ones are passivated by association with atomic hydrogen [6, 7].

Hydrogenation also reduces the electrically active concentration of the new oxygen donors, however the degree of passivation for both types of donors is relatively low compared to the passivation efficiency of other impurities and defects, which is practically complete.

3.2 Process induced defects

A wide variety of such defects is passivated by reaction with atomic hydrogen. Process steps may be sputter etching, ion implantation (beam and plasma immersion), thermal quenching, laser annealing.

The passivation of dry etching damages by low energy hydrogen implantation from a Kaufman ion source has also been reported.

3.3 Crystalline defects

Hydrogen has been found to reduce defect state densities and potential barrier at grain boundaries and dislocations improving photovoltaic cells made with multicrystalline silicon.

Dislocations are well passivated as they enhance the diffusion of hydrogen along their core [8].

3.4 Thermal stability of passivation

This stability is of a paramount importance for the applications and Table I gives a compilation of the impurities and defects in silicon susceptible to hydrogenation, their energy level in the gap, and the activation energy required for reactivation.

The table reveals that most of the defects and impurities in silicon that are passivated by reaction with hydrogen can be reactivated by a subsequent annealing above 400°C. Notice that the passivation of deep levels is thermally more stable than that of shallow level.

3.5 Prehydrogenation

Hydrogen incorporated into silicon subsequently exposed to ionizing radiations inhibits the formation of secondary point defects and gives rise to a hardening of the material.

Impurity	Trapped Carrier	Energy Level in the gap (eV)	Reactivation Energy (eV)
Cu	Holes	0.2 ; 0.35 ; 0.53	2.5
Ni	Holes	0.18 ; 0.21 ; 0.33	2.5
Fe	Holes/electrons	0.32 ; 0.39	1.5
O-V	Electrons	0.18	1.9
V-V	Electrons	0.22	1.9
Cr	Electrons	0.31	2.1
Dislocations			2.0
Grain Boundaries			2.5
B, Ga, Al			1.1 ; 1.6 ; 1.9

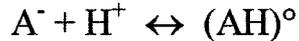
Table I – Impurities/defects in silicon which can be passivated by hydrogen, the corresponding energy level in the gap and the reactivation energy [9].

4. DOPANT PASSIVATION BY ATOMIC HYDROGEN :

Shallow acceptor passivation in silicon is a much stronger effect than that of shallow donors [10-12]. Boron was mainly concerned, and large increases of the near surface spreading resistance were observed in boron doped silicon exposed to a hydrogen plasma, but all of the shallow acceptors in silicon are passivated as over 99 % of the acceptors can be deactivated (there is no introduction of donors). In contrast, shallow donors (P ; As ; Sb) are weakly deactivated.

For n-p junction solar cells (with a p-type base) an important point is that a thin n-type layer at the surface of a p-type sample will severely impede the in-diffusion of hydrogen.

Electric fields due to reverse biases lead to dramatic changes in the passivated acceptor profiles and the diffusing species is probably monoatomic positively charged hydrogen ion. It is believed that the passivation results from the binding of hydrogen with one acceptor atom, leaving this atom three fold coordinated with its remaining Si neighbors while the deactivation of acceptors can be represented by the reaction :



5. HYDROGEN AND COUNTERDOPING OF P-TYPE SILICON :

It is known that atomic hydrogen incorporated in Cz silicon at temperatures below 500°C act as catalyst and can significantly enhance the thermal donor (TD) formation rate, as a consequence a fast doping occurs at low temperature (<500°C). Recent investigations have shown [13] that the maximal TD concentration depends on the oxygen contents in the sample, the process temperature and the hydrogen dose incorporated in the wafers.

The use of plasma implantation technique which can introduce up to 10^{19} cm⁻² hydrogen ions leads to the formation of about 10^{16} cm⁻³ TD for a few hours processing. So in the case that the acceptor concentration is less than 10^{16} cm⁻³, counterdoping of p-type silicon, and a n-p junction formation should be achieved. The p-n junctions exhibit the characteristics of linear graded junctions. Such a low temperature doping process by TDs might be used as a new technology for device structures based on Cz silicon.

When implanted at high doses ($> 3 \cdot 10^{16}$ cm⁻²) in p type silicon, hydrogen accumulation below the surface induces a direct formation of a n-type region, which the thickness is approximately that of the projected range. This counterdoping is not oxygen related because it appears in FZ wafers as well as in Cz and in multicrystalline wafers [14]. There is no relation with an eventual damage region which may be compensated by the trapping of carriers by defects. The carrier concentration at the surface is about few 10^{16} cm⁻³ and the structure behaves like a solar cell.

The spectral responses of the photocurrent look like that of finished standard solar cells except in the blue part of the spectrum and the minority carrier diffusion lengths are in the range 150 to 200µm.

The electrical quality of such a junction increases after annealing steps in neutral ambient at temperatures between 300°C and 550°C for 1 hour. However, the junction disappears after annealing at 600°C. Such a direct counterdoping is due to hydrogen itself because it does not appear in helium implanted samples under the same conditions of ion implantation.

The origin of this phenomena could be due to shallow hydrogen related donor levels in silicon which were found at 26 and 37 meV below the conduction band. Such levels were found in hydrogen implanted and in neutron transmutation doped FZ samples, grown in a H₂ atmosphere.

Above 600°C the samples were converted back to their original p-type conductivity.

6. HYDROGEN AND MECHANICAL PROPERTIES. NANOCAVITIES – EXFOLIATION :

The growth of silicon crystals in hydrogen atmosphere results in macroscopically attractive crystals, but such crystals are brittle, their resistivity is uncontrolable and anomalous etchings occurs.

The interaction of silicon with hydrogen-containing plasmas like in the reactive-ion-etching produces defects, like platelets.

Hydrogen ion implantations at energies higher than 40 keV and at dose higher than 5.10^{16} cm⁻² form blisters and result in exfoliation of the exposed crystal. Thin silicon wafers can be obtained by this technique and found applications in silicon on insulator devices (SOI).

Before the formation of blisters, hydrogen nanobubbles are created at the projected range (for exemple at 2.5 μm below the exposed surface when the ion energy is 250 keV). An annealing at $T \geq 350^{\circ}\text{C}$ out gases the hydrogen and nanocavities are formed which can be used as gettering sites for impurities. Such cavities can be made before the processing steps needed to make devices or solar cells, and protect the devices from contaminations [15].

7. APPLICATION TO SOLAR CELLS :

Hydrogenation has found applications in solar cells made with mc-Si wafers. These materials contain a lot of imperfections which can interact with hydrogen and become passivated.

Due to the reactivation of recombination centers at temperature higher than 450°C, the hydrogenation must be applied as a end of range process. Moreover in order to avoid the formation of defects on the surface emitter and to not damage the metallic contacts soft hydrogenation techniques must be used, like low energy plasma ion implantation.

However the best solution, proposed by Hezel and Jäger [4], uses the deposition of a PECVD Si₃N₄ (H) layer on the emitter surface an then the firing of the structure after the deposition of metallic fingers. Hydrogen diffuses into the bulk, the emitter surface is passivated and an efficient antireflection coating layer is made. A pilot line production was also developed by Kyocera in Japan [16].

Compared to non hydrogenated cells made with the same materials and a TiO₂ antireflection coating, there is a noticeable increase of the conversion efficiency by 2 to 3 points, at least, which is related to the increase of minority carrier diffusion lengths and emitter surface passivation.

Such improvements were observed by the IMEC and FHISE groups [17-19] with different imperfect wafers like electromagnetically cast wafers, like very low resistivity wafers and also like plasma purified metallurgical grade silicon wafers. As expected low quality materials show the biggest increase in performance.

Even more interesting is the fact, that mc-Si materials of high quality like baysix are well improved by this hydrogenation technique. Indeed the minority carrier diffusion length mean values increase from 140 to 200 μm in the center of the baysix ingots and from 200 to 250 μm in the bottom of the ingots. As a consequence the photocurrent, the photovoltage and the conversion efficiency of the finished solar cells are improved.

The electrical properties of the hydrogenated cells become very homogeneous although crystallographic defects and impurities are always present. Moreover it looks like the passivation stability of the cell is neatly improved, probably because hydrogen is encapsulated in the n-p cell by the aluminium layer on the backside and by the silicon nitrid on the front side. The hydrogenated cells can be annealed at 600°C without a significant decrease of the photovoltaic performances.

Light beam induced current (LBIC) scan maps of hydrogenated and non hydrogenated cells show that there is a drastic reduction of the recombination activity of intragrain defects, while grain boundaries are less passivated. The scan maps are very homogeneous after the treatment, and even if standard mc-Si wafers are used, like polix and baysix, conversion efficiencies higher than 16 % are obtained in 10 x 10 cm² cells.

LBIC scan maps at various wavelengths of the same sample indicate that in imperfect materials the passivation of defects is not transversally homogeneous. The passivation depth depends on the defect density, it decreases when the density increases due to the trapping of hydrogen atoms which reduces their diffusivity.

Notice that the surface passivation which results from the deposition of the SiN-H layer is of a paramount importance. Such a passivation works well also at the surface of highly doped emitters as it is shown by the comparison of the short wavelength spectral response of cells which used the conventional TiO₂ antireflection coating and those covered by the silicon nitride layer.

However, for industrial production of solar cells, a high throughput and cost effective technique is required. Until the last years, all commercially available PECVD systems for the deposition of the SiN-H layers are the so called batch-reactors, which use a large number of electrodes connected in parallel, enabling the simultaneous processing of more than hundreds wafers. Nevertheless there is a number of severe problems which limit the industrial application of the direct-plasma batch reactors [19] and the cost of the deposition is evaluated to 0.15 US \$/Wp.

Remote plasma techniques are more suited. ASE GmbH [20] is using a in line remote PECVD system into its new 13 MW/year cell production in Alzenau (Germany). This new machine is able to process more than 600 wafers of arbitrary shape per hour and reduces the cost of the SiN-H deposition by 50%.

Shimadzu Corp. has realized a in-line production machine with a deposition area of 0.93x1.28 m and a throughput of 1485 wafers of 10x10cm per hour [21].

8. COMPARISON WITH EXTERNAL GETTERING TECHNIQUES. SYNERGETIC EFFECTS :

It was reported that hydrogenation effects are more marked when aluminium-silicon alloying or phosphorus diffusion were applied to improve the base of the cells. That suggests that hydrogen in-diffusion is made easier by such treatments which are well known to inject point defects in the bulk of silicon wafers.

However progresses have been recently obtained in phosphorus diffusion gettering by a suited control of the cooling conditions. Wafers containing high densities of defects are neatly improved when the samples are slowly cooled after they have been heated at temperatures higher than 800°C. The minority carrier diffusion lengths achieve frequently the wafer thickness after a short treatment at 850°C (i.e. the temperature needed to make the junction). As the stability of the improvements due to the gettering is higher than that of hydrogenation, external gettering must always be taken in account although hydrogenation has the advantage to works efficiently at low temperatures (< 500°C) and is very suited for materials which are degraded by thermal annealings, like the electromagnetically cast wafers.

The best solution to improve imperfect wafers may be the use of an external gettering and a hydrogen passivation by the deposition of a silicon nitride layer. Both the treatments have a synergetic effect and complementary effects: the bulk defects are passivated because impurities are removed and dangling bonds are saturated, and in addition, surface recombination velocity of the emitter is reduced.

9 Conclusions

Although there are still many unknowns about the properties and effects of hydrogen in silicon, the field of hydrogen in this semiconductor (and also in other materials) is likely to be an important and very likely one for the next years. For solar cells the hydrogenation by means of the silicon nitride layer is certainly the most suited technique to improve the materials and the cell performances without a significant increase of the energy cost and production yield. Improvements due to hydrogenation

may be enhanced by the synergy which exists with external gettering treatments like phosphorus diffusion.

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INVESTIGATION OF GETTERING MECHANISMS IN CRYSTALLINE SILICON

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ABSTRACT

Accomplishments from research conducted under support of NREL subcontract XAF-7-17607-1 have been reported. In this investigation, the various aspects of the mechanisms of gettering contaminant impurities away from device active regions in Si have been systematically conducted. With these studies, our knowledge of gettering in Si has become substantially complete in the sense that interpretations of major experimental results have become self- and mutually consistent.

1. INTRODUCTION

The research program supported by NREL XAF-7-17607-1 is entitled *INVESTIGATION OF GETTERING MECHANISMS IN CRYSTALLINE SILICON*. The purpose of conducting the studies supported by this project was to obtain consistent interpretations of existing experimental results, as well as to conduct the needed new experiments, concerning the various phenomena associated with gettering in Si. The investigated gettering method is that by using an Al layer, and the involved works span from studies concerning basic point defect behaviors during gettering to studies of application of the gettering method to improve multicrystalline Si minority carrier diffusion lengths. A study of the electrical behavior of precipitated metallic impurities in Si based on the Schottky property of the precipitates, which is a newly proposed physical mechanism, has also been conducted. Moreover, A preliminary study of the effect of gettering in affecting the solar cell efficiency has been conducted.

2. SUMMARY OF TECHNICAL ACHIEVEMENT

In this section, our technical achievement are summarized in 6 entries, categorized by maintaining the coherence and integrity of the involved knowledge.

2.1. Gettering of Au From Si

An outstanding *predictive* simulation result have been obtained under support of the previous subcontract, XD-2-11004-1, concerning gettering of pre-introduced Au in Si wafers. The simulation results indicated that [1], using an Al layer deposited on *one* side of the wafer, Au will be gettered away from *both* surface regions of the wafer and the gettering effectiveness propagates from both surfaces progressively to greater depths with time. Experimental evidences which confirm the predictions has been now obtained [2]. Au was indiffused into a FZ Si wafer at 950°C for 16 hr. After removing the Au source and etching, samples from the indiffused wafer were annealed at 1000°C without or with an Al layer on one surface. For samples without Al, there is

no change in the net Au content, while the U-shaped indiffused profile becomes flatter. For samples with an Al layer, both wafer surface region Au concentrations were significantly decreased in 30 min while the wafer interior Au concentrations decreased only after annealing for longer times. A brief physical explanation of the phenomenon is as follows. It is known that Au is a substitutional-interstitial (Au_s - Au_i) species with its *indiffusion* governed by the *kick-out mechanism* which is mediated by Si self-interstitials (I). Our previous prediction of the Au gettering process assumes that during gettering by the Al-Si liquid the governing point defect species is also I . Au_s atoms can changeover to Au_i atoms to rapidly migrate out of Si into the liquid only at the two wafer surface regions, because the consumed I will be quickly replenished. In the wafer interior an I undersaturation develops which hinders the Au_s - Au_i changeover and hence the gettering process. The above reasoning is satisfactory in explaining qualitatively why with Al on only one side of the wafer, both wafer surface regions are more effectively gettered than the wafer interior. On a quantitative basis, however, the fit of the data is more satisfactory when it is assumed that during gettering of Au by Al the dominating point defect species is the Si vacancy V via the *Frank-Turnbull mechanism* instead of I which dominates under Au indiffusion conditions via the *kick-out mechanism*. For this difference in the Si point defect behavior, an explanation consistent in both thermodynamic and kinetic aspects of the problem has been proposed. A set of experimental results and fits are shown in Fig. 1.

2.2. Improvement of Carrier Diffusion Lengths in Multicrystalline Si bad Regions by Al Gettering

Another outstanding *predictive* simulation result obtained under support of the previous sub-contract, XD-2-11004-1, is concerned with the effectiveness of gettering on multicrystalline Si (using Al layers) to improve the minority carrier lifetimes of the so-called "bad crystal regions" which do not respond to gettering treatment normally employed in the solar cell fabrication process at a temperature below about 900°C for times less than 1 hr. For this problem, our simulation results indicated that a higher temperature will be helpful [3].

Multicrystalline Si for photovoltaic applications is a very inhomogeneous material with localized regions of high dislocation density and large impurity and precipitate concentrations which limit solar cell efficiency by acting as carrier recombination sites. Due to slow dissolution of precipitates in multicrystalline Si, these regions cannot be improved by conventional P and Al gettering treatments for removal of metal impurities which give good results for single crystal Si. Our previous simulation results showed that an extended high temperature Al gettering treatment can improve minority carrier diffusion lengths in these low quality regions and homogenize the electrical properties of multicrystalline Si wafers. An experiment has conducted in this performance period which showed that this is indeed the case [4], see Fig. 2.

2.3. Modeling of Void Nucleation and Growth in CZ Si

In order to reliably model the Au gettering and other processes, we need the point defect parameters I and V diffusivity and thermal equilibrium concentration values. Existing data and estimates for the I diffusivity and thermal equilibrium concentration values are fairly reliable. For V , however, only the product of the diffusivity and thermal equilibrium concentration is reliable, but not the two values individually. Formation of voids (to sizes of ~100 nm) during large diameter CZ Si crystal growth has provided an opportunity for arriving at these two V parameters.

To this end, we have modeled the nucleation and growth processes of voids under Si vacancy supersaturation conditions [5,6]. From nucleation barrier calculations, it is shown that voids can be nucleated, but not dislocation loops. The homogeneous nucleation rate of voids has been calculated for different temperatures by assuming different enthalpy of Si vacancy formation. The void growth process has been calculated using a moving boundary formulation. Matching the results of void nucleation and growth simulations and taking into account the competition between the two processes, limited time available, and the crystal cooling rate, it is shown that the experimentally observed void density and size data can be explained if the Si vacancy formation enthalpy is in the range of 2.8 to 3.4 eV and the void nucleation temperature is in the range of 970 to 1060 °C.

2.4. A Quantitative Model of the Electrical Activity of Metallic Precipitates in Si

The multicrystalline Si bad crystal region consists of dislocation entangles upon which many metal silicide precipitates are formed. It is believed that these precipitates are prominent carrier recombination centers which are responsible for the extremely short minority carrier diffusion lengths found in these regions. While the electrical activity metal atoms in Si are fairly well understood, it is somewhat surprising to note that the same is not the case for a metallic precipitate. An inferred origin of the electrical activity is those due to the so-called *interface states* which constitute as charge traps, but measured data indicates that such states cannot account for all the electrical activity of such metallic precipitates. Based on the Schottky property of the precipitate-Si system, we have formulated a quantitative model of the electrical activity of metallic precipitates in Si [7]. In this model, carrier diffusion as well as carrier drift in the Si space charge region are accounted for, and carrier recombination is attributed to the thermionic emission mechanism of charge transport across the Schottky junction rather than surface recombination at traps. It is shown that the minority carrier capture cross-section of the precipitate can be as large as the total capture cross-section of its constituent metal atoms dissolved in the Si matrix. Under weak carrier generation conditions, the supply of minority carriers was found to be the limiting factor of the recombination process. The plausibility of the model is demonstrated by a comparison of calculated and available experimental results, Fig. 3.

2.5. Variable Temperature Processes for High gettering Efficiency and Short Needed Gettering Times

Physical and numerical modeling of impurity gettering from multicrystalline Si for solar cell production has been carried out using Fe as a model impurity [8]. Calculated change of nonradiative recombination coefficient of minority carriers in the course of gettering is used as a tool for evaluating the gettering efficiency. A derivation of the capture cross-section of impurity precipitates, as compared to single atom recombination centers, is presented. Low efficiency of conventional application of gettering process is explained by the modeling results. Variable temperature gettering process is modeled and predicted to provide high gettering efficiency and short needed gettering times, Fig. 4.

2.6 Gettering and BSF Contributions to Solar Cell Efficiency

In silicon solar cell fabrication, impurity gettering from Si by an aluminum layer and indiffusion of Al for creating the back surface field (BSF) are inherently carried out in the same proc-

ess. We have modeled these two processes and analyzed their impact on solar cell efficiency [9]. The output of gettering and Al indiffusion modeling is used as an input for calculation of solar cell efficiency. The cell efficiency gain is obtained as a function of the processes duration. To check the relative contributions of gettering and BSF in improving the cell efficiency, their effects are evaluated together as well as separately. It is found that, for solar cells fabricated from low quality, multicrystalline Si, the efficiency gain is solely due to gettering. In solar cells made of high quality Si, the efficiency gain is primarily due to gettering, but the BSF may play a significant role if the cell thickness is less than about 200 μm . See Figs. 5 and 6 for these results. The two effects are found to be synergetic. The model provides a means for optimization of the temperature regime for both processes, as well as for maximization of solar cell efficiency.

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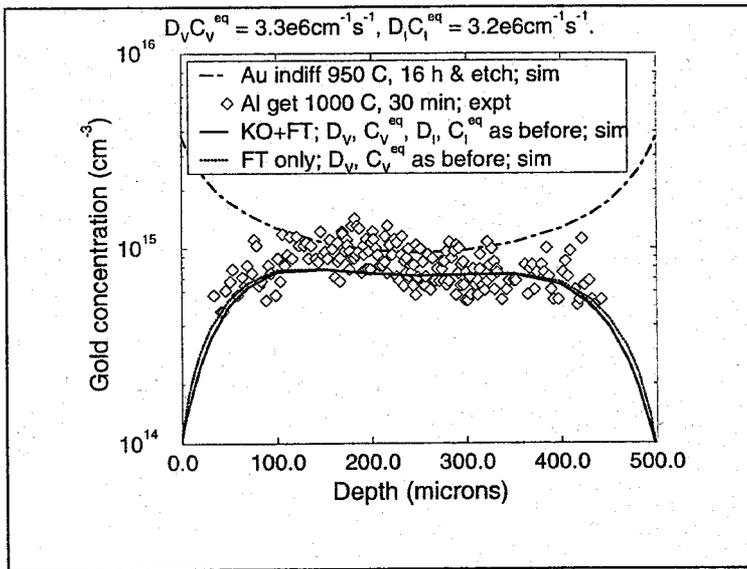


Fig. 1. Au experimental profiles fitted by *KO* and *FT* mechanisms combined. Also shown for comparison is a fit by the *FT* mechanism alone. It is seen that the two fits are very close to each other. Also shown is the simulated Au concentration profile after Au indiffusion and etching.

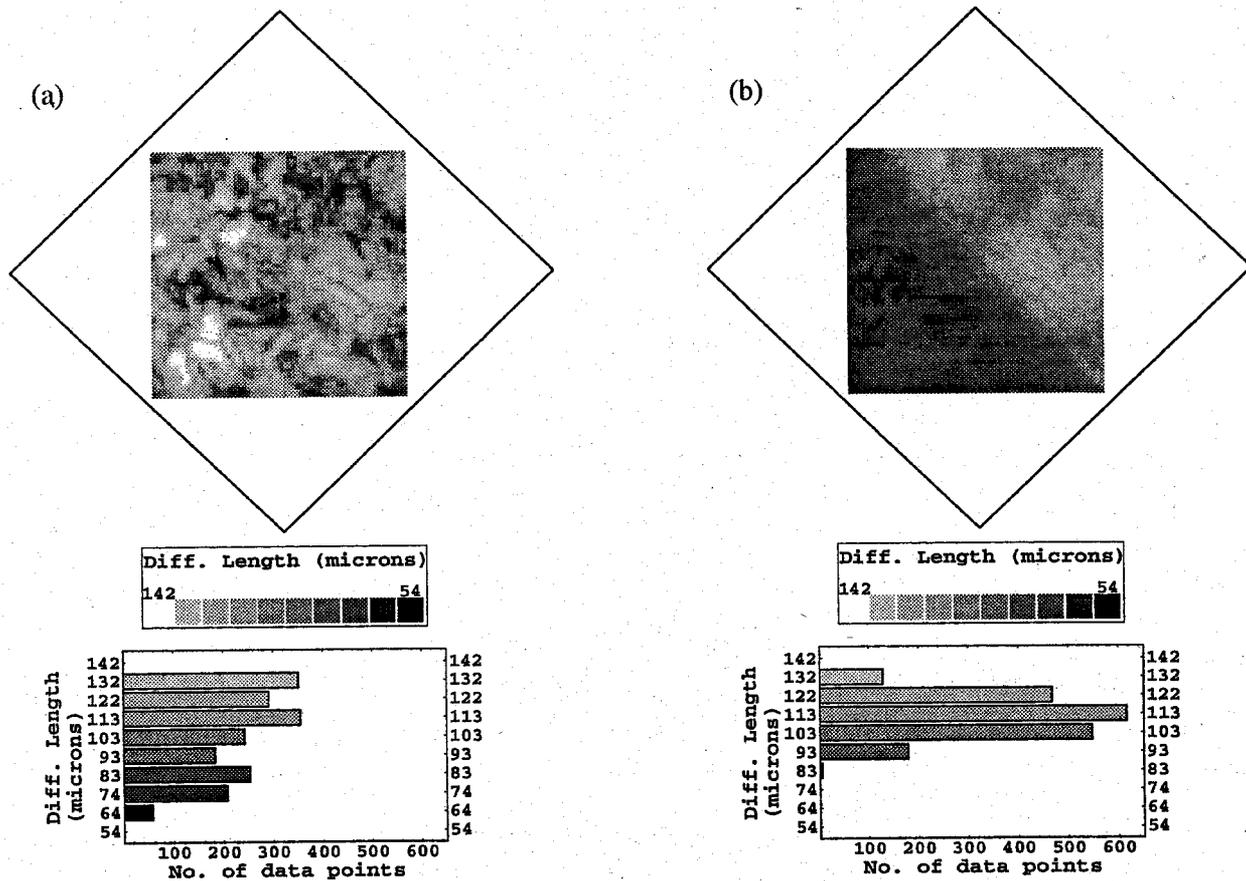


Fig. 2. (a) Initial minority carrier diffusion length map of a 4" square mc-Si wafer, accompanied by a histogram of diffusion length values in the half of the wafer that was subsequently Al gettered; (b) Diffusion length map of the same wafer after the Al gettering anneal, with a histogram of the half that had the Al gettering layer. Only about half the total wafer area could be mapped due to instrument limitations and the square outline outside the gray scale map indicates the size and orientation of the wafer relative to the actual mapped area. The same scale has been used in the adjacent figures to allow direct comparison. Diffusion lengths less than 87 μm for the initial map and less than 77 μm for the final map are unreliable and mostly overestimated as the BPC mode of the ELYMAT technique cannot measure diffusion lengths less than one-fifth the wafer thickness. In the Al gettered half, the regions that were initially of poor quality have improved sufficiently to be comparable to the good quality regions. The distribution of diffusion length values after gettering has shifted to the higher end of the scale and has a narrower width.

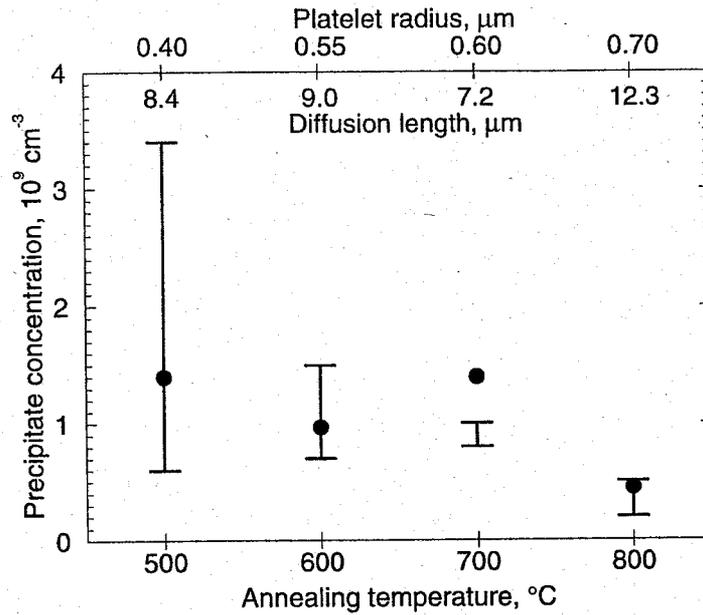


Fig. 3. NiSi_2 precipitate concentration observed in four Si samples annealed at different temperatures. Precipitate radius and minority carrier diffusion length are shown for each sample. Higher values of the range are as measured by TEM, lower values are as measured by EBIC. Experimental error span is not shown, but is present around each experimental point. Dots indicate precipitate concentration as predicted by the model.

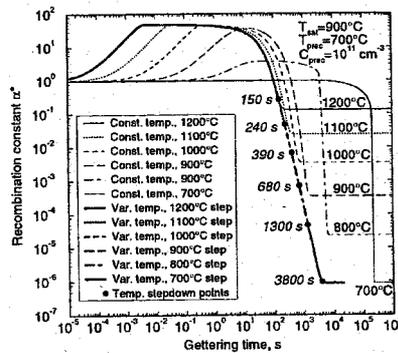


Fig. 4. Calculated relative integrated recombination constant as a function of getting times for different getting temperatures. The heavy line corresponds to a variable temperature process with temperature decreased from 1200°C to 700°C in 100°C steps, at the indicated temperature stepping-down points.

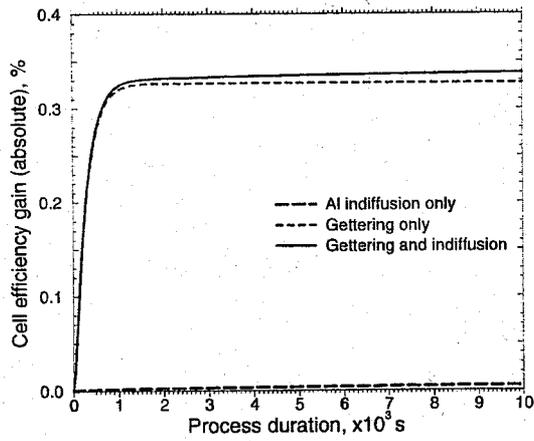


Fig. 5. Calculated dependence of high quality Si solar cell efficiency on the duration of Al gettering and indiffusion. Process temperature 1000°C. Wafer thickness 400 μm . Doping levels are optimized for the untreated cell.

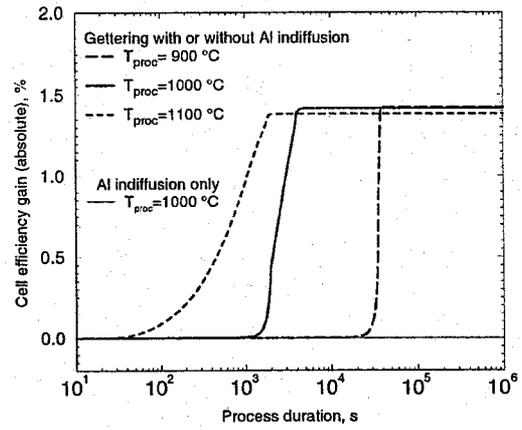


Fig. 6. Calculated dependence of low quality Si solar cell efficiency on the duration of Al gettering and indiffusion at various processing temperatures. Wafer thickness 400 μm . Doping levels are optimized for the untreated cell. Curves for gettering with Al indiffusion are not shown. They are undistinguishable from respective curves for gettering without Al indiffusion. Curves for Al indiffusion at 900 and 1100°C are undistinguishable from the curve for Al indiffusion at 1000°C.

Lifetime Enhancement and Low-Cost Technology Development for High-Efficiency Manufacturable Silicon Solar Cells

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Abstract

A low-cost, manufacturable defect gettering and passivation treatment, involving simultaneous anneal of a PECVD SiN_x film and a screen-printed Al layer, is found to improve the lifetime in Si ribbon materials from 1-10 μs to over 20 μs . Our results indicate that the optimum anneal temperature for SiN_x -induced hydrogenation is 700°C for EFG and increases to 825°C when Al is present on the back of the sample. This not only improves the degree of hydrogenation, but also forms an effective back surface field. Controlled rapid cooling was implemented after the hydrogenation anneal and contact firing to improve the retention of hydrogen at defect sites using RTP. RTP contact firing improved the performance of ribbon solar cells by 1.3-1.5% absolute when compared to slow, belt furnace contact firing. Enhanced hydrogenation and rapid heating and cooling resulted in screen-printed Si ribbon cell efficiencies approaching 15%. A combination of screen-printed Al and a two minute RTP anneal in an oxygen ambient produced simultaneously a high quality rapid thermal oxide (RTO) and an aluminum back surface field (Al-BSF) with a back surface recombination (BSRV) of 200 cm/s 2-3 Ohm-cm single and multicrystalline silicon solar cells. In addition, RTO/ SiN_x stack passivation was found to be superior to SiN_x surface passivation. RTO/ SiN_x passivation reduces the BSRV to ~ 10 cm/s on 1-2 Ohm-cm p-type single crystal Si and also lowers the J_{oc} of 40 and 90 Ohm/sq emitters by a factor of three and ten, respectively. Integration of RTP emitters, screen-printed RTP Al-BSF and RTO produced 19% and 17% efficient monocrystalline cells with photolithography and screen-printed contacts, respectively.

1. Introduction

The U.S. PV Industry Roadmap has identified the development of 18% efficient thin Si solar cells as a top R&D goal to be achieved in the next 3-10 years [1]. Si ribbon materials such as Edge-defined Film-fed Grown (EFG), dendritic web, and String Ribbon Si may offer the substrates of choice to meet this goal because thin (~ 100 μm) ribbon samples can be grown directly from the melt, eliminating losses associated with wafer slicing and etching. Although the low-cost growth of Si ribbon samples makes them attractive photovoltaic substrates, the as-grown minority carrier lifetime is typically in the range of 1-10 μs , which is not suitable for high-efficiency cells ($\sim 18\%$). In this study, several manufacturable gettering and passivation techniques, including P and Al gettering and hydrogen passivation via post-deposition anneal of PECVD SiN_x films, are examined for the improvement in the lifetime of ribbon Si materials. In addition to lifetime improvement, rapid and low-cost technologies are developed to improve front and back surface passivation for achieving high efficiency thin cells. Finally, high efficiency mc-Si and single crystal cells are fabricated and analyzed to demonstrate and quantify the positive impact of gettering, hydrogenation, and technology advancement on Si cell

efficiencies. Sections 2 and 3 of this paper show the development of low-cost rapid technologies to improve front and back surface recombination velocity, while section 4 deals with bulk lifetime enhancement and contact firing schemes.

2. Development of Rapid and Improved Al-Back Surface Field (Al-BSF) for Si Solar Cells

Figure 1 shows that RTP alloying of the screen-printed Al, with a ramp-up rate of $\geq 1200^\circ\text{C}/\text{min}$, reduces the BSRV to approximately 200 cm/s for single crystal solar cells formed on 2.3 $\Omega\text{-cm}$, p-type Si. This represents an improvement of about a factor of 10 to 1000 compared to devices with poor or no BSF. It was found that an Al-BSF formed in a belt furnace with a

somewhat slower ramp-up rate, produced a non-uniform BSF with a surface recombination velocity of 1000 cm/s. The Al-BSF formed by screen-printing and rapid alloying has been integrated into an industrial-type fabrication sequences to achieve solar cell efficiencies in excess of 17.0% on planar 2.3 $\Omega\text{-cm}$ float zone Si, a 1-2% (absolute)

improvement over analogous cells made with un-optimized Al-BSF's or highly recombinative rear surfaces [2].

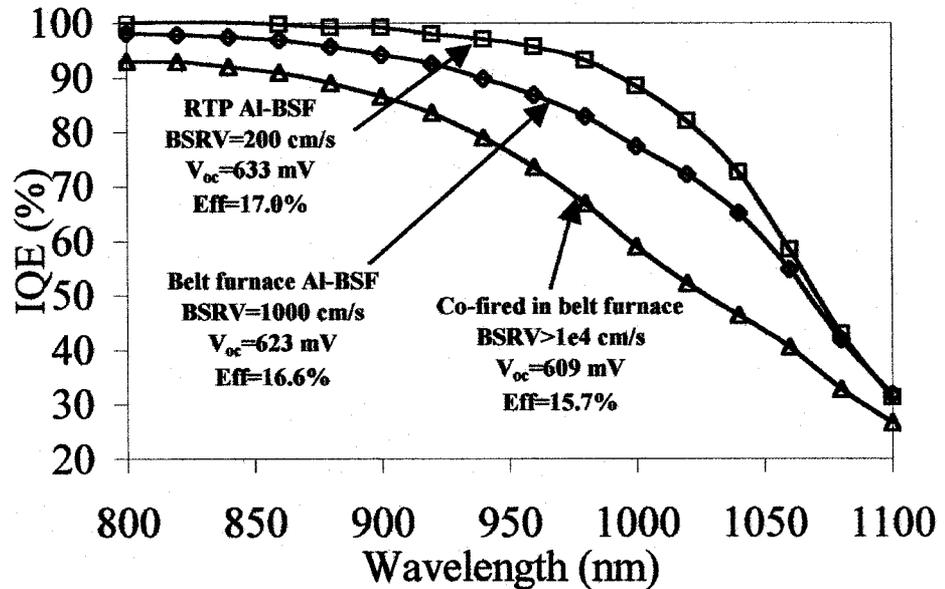


Figure 1: Impact of reduced S_b , due to RTP Al-BSF alloying on the long wavelength Interval Quantum Efficiency (IQE) of screen-printed solar cells.

3. Development of a Novel RTO/SiN Stack for Effective Front and Back Surface Passivation for Silicon Solar Cells

In an effort to develop a low-cost, rapid, and effective surface passivation scheme, which can also withstand screen-printed metal firing, we conducted a comprehensive study using several promising dielectric films. The results in Figure 2 show that the passivation quality of all the single layer films, including TiO_2 , SiN and a rapid thermal oxide (RTO), degrades severely after the firing of screen-printed contacts. In contrast, a rapid and novel surface-passivating scheme, composed of a thin (100 Å) rapid thermal oxide (RTO) capped with ~ 750 Å direct PECVD SiN, not only provides excellent front and back surface passivation and antireflection coating, but can also withstand 700-800°C screen-printed contact firing. Compatibility with this post-deposition anneal makes the RTO/SiN stack passivation scheme very attractive for next generation cost-effective, thin, bifacial solar cells where a similar anneal will be required to form front and back screen-printed contacts.

To examine the potential of this novel surface passivation scheme, bifacial, screen-printed cells were fabricated on 0.65 ohm-cm float-zone silicon with front and back RTO/SiN stack passivation, and co-firing of the front and back Ag grid through the stack. This resulted in front illuminated

efficiency of 17% and a rear illuminated efficiency of 11.6%. IQE analysis gave an effective BSRV of 340 cm/s, which was largely due to screen-printed metal of the back. In addition, direct J_{oc} measurements showed that stack passivation also reduces the J_{oc} of 40 and 90 Ohm/sq emitters by a factor of three and ten, respectively [3].

4. Understanding and Implementation of Manufacturable Defect Gettering and Passivation Technologies in Low-Cost Silicon Ribbons

To take full advantage of the reduced BSRV in the above sections, bulk lifetime for 100 μm thick material should be $\geq 20 \mu\text{s}$, resulting in a diffusion length 2-3 times the cell thickness. Unfortunately,

most mc-Si ribbon materials, which can be grown thin, show as-grown bulk lifetimes of only 1-6 μs . To raise the bulk lifetime in low-cost materials, such as dendritic web, EFG, and String Ribbon Si, to over 20 μs , we have investigated low-cost, manufacturable defect gettering and passivation treatments, including phosphorus and aluminum gettering and the post-deposition anneal of a PECVD

SiN_x film for defect hydrogenation. Figure 4 shows that the lifetime of EFG and dendritic web Si did not increase after PECVD SiN_x film deposition and anneal at 850°C in a belt furnace, while the lifetime of String Ribbon showed a moderate increase from 8.3 μs to 12.9 μs . The ~930°C P and 850°C Al gettering treatments improved the

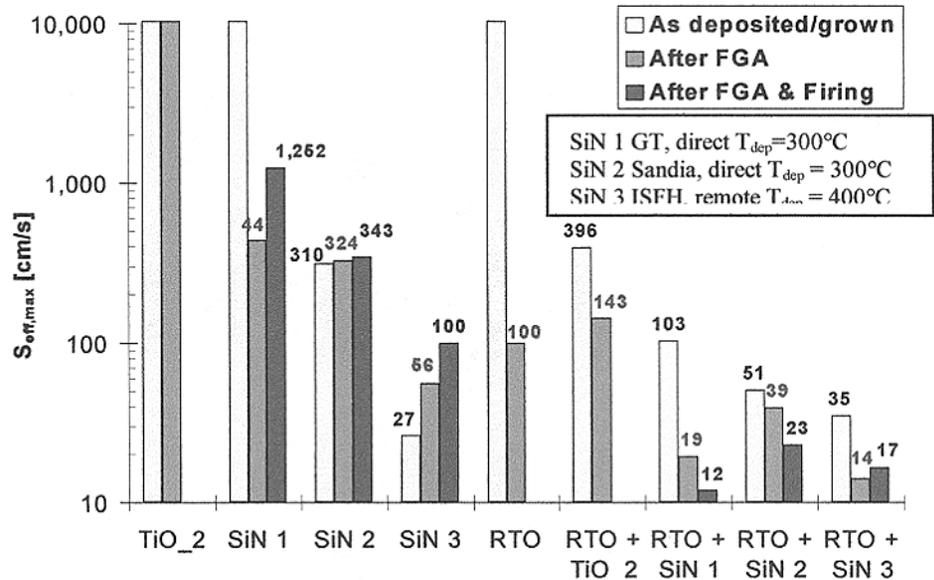


Figure 2: Impact of forming gas anneal (FGA) and a screen-printed metal firing anneal on S_{eff} .

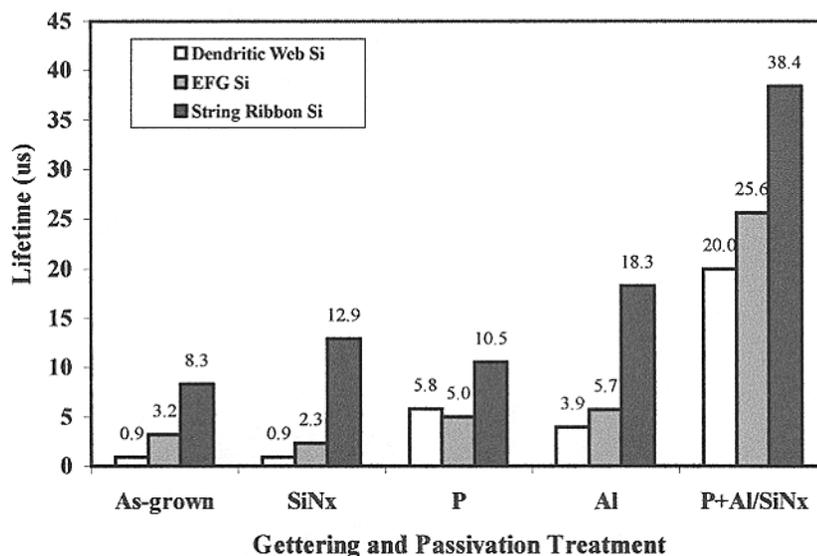


Figure 4: Al-enhanced SiN_x -induced defect passivation in Si ribbon materials.

lifetime in all three ribbon materials but were unable to raise the lifetimes over 20 μ s. To identify any interaction between the Al gettering and hydrogen passivation processes, the SiN_x-induced hydrogenation and Al gettering treatments were performed simultaneously at 850°C after the P gettering. The simultaneous anneal of SiN_x and Al increased the lifetime in EFG, dendritic web, and String Ribbon Si to 25.6 μ s, 20.0 μ s, and 38.4 μ s, respectively. The significant enhancement in lifetime achieved after the simultaneous anneal of SiN_x and Al indicates that there is a positive synergistic interaction between the SiN_x-induced hydrogenation on the front and Al-Si alloying at the back of the sample which enhances the lifetime to over 20 μ s in all three materials. Our FTIR analysis of annealed SiN films has shown that the release of hydrogen from the film increases as the anneal temperature increases [4]. We have found that the optimum anneal temperature for the Al-enhanced SiN_x-induced hydrogenation is 825°C [5], making the defect passivation treatment compatible with the formation of an effective Al-BSF. We have also found that rapid cooling after the simultaneous SiN/Al anneal improves defect passivation by improving the retention of hydrogen at the defects [5]. Based on these results and recent theoretical calculations [6,7], we have proposed a three-step physical model in which defect passivation is governed by the release of hydrogen from the SiN_x film due to annealing, the generation of vacancies during Al-Si alloying, and the retention of hydrogen at defect sites due to rapid cooling [4].

While the 850°C/ 2 min. anneal is beneficial for bulk passivation, it is not suitable for front contact firing. Therefore we have developed an RTP contact firing scheme with rapid heating, to improve the Al-BSF, and rapid cooling to improve the retention of hydrogen at the defects. Table 1 shows that RTP contact firing, with very fast heating and cooling rates, improves the performance of ribbon solar cells by 1.3-1.5% absolute when compared to slow, belt furnace contact firing, where cooling rates were <10°C/s.

The efficiency enhancement from RTP contact firing of ribbon cells is reflected in improved bulk and surface passivation (J_{sc} and V_{oc}) and contact quality (FF).

Figure 4 shows LBIC scans, made with the *PVSCAN 5000* system using a 905 nm laser, of String Ribbon cells taken from consecutive sections of the ribbon to identify defects and their activity. Note that these samples have similar crystallographic defect structures. The LBIC response in intragrain regions improved from 0.58 A/W to 0.64 A/W with RTP contact firing as opposed to slow belt firing. Fig. 4 reveals a defect whose activity decreases as the defect extends from Cell 1-3 into Cell 16-1. The cell

Contact Firing			V_{oc} (mV)	J_{sc} (mA/cm ²)	FF	Eff (%)
RTP	Float Zone	Average	621	34.2	0.777	16.5
		High	622	34.3	0.779	16.6
	EFG	Average	573	32.1	0.749	13.8
		High	585	32.8	0.757	14.6
	String Ribbon	Average	574	31.6	0.762	13.8
		High *	600	31.6	0.778	14.7
Belt Furnace	Float Zone	Average	614	33.7	0.770	15.9
		High	615	33.9	0.771	16.1
	EFG	Average	554	30.1	0.743	12.4
		High	566	30.9	0.751	13.1
	String Ribbon	Average	553	29.7	0.738	12.1
		High	575	31.1	0.747	13.4

* - confirmed by Sandia National Labs.

Table 1: Impact of RTP front contact firing on float zone, EFG, and String Ribbon Si solar cells.

efficiency data in Table 1 and LBIC analysis in Figure 4 indicate that RTP firing of screen-printed contacts is more effective in retaining the hydrogen at defects that was introduced during the 850°C Al/SiN_x anneal. Conversely, the slow ramp rates during belt furnace contact firing result in increased dehydrogenation of defects, increasing their electrical activity. We have also shown that RTP contact firing improves the quality of the Al-BSF formed in the belt furnace [8], which may also contribute to the enhancement in cell performance seen in Table 1.

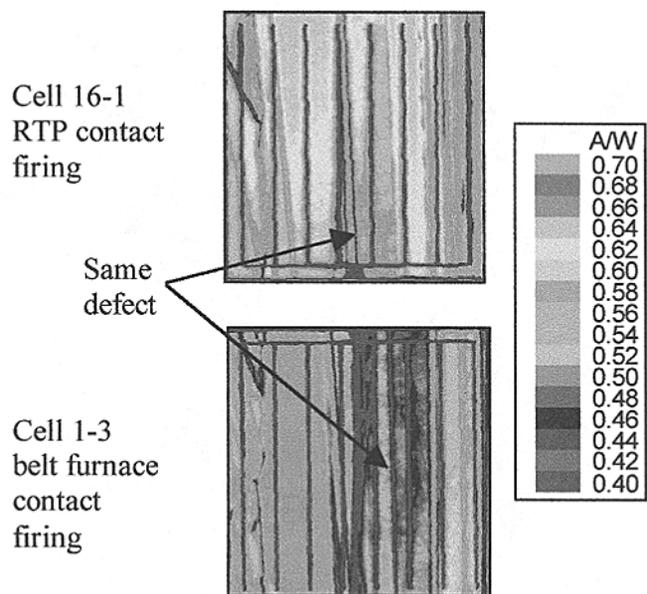


Figure 4: Improved passivation of intergrain and intragrain defects with RTP contact firing.

5. Conclusions

Several low-cost rapid technologies have been developed to enhance the bulk defect and surface passivation of Si solar cells. Formation of screen-printed Al-BSF and RTO/SiN_x stack passivation by RTP/PECVD resulted in substantial reduction in cell processing time and front and back surface recombination velocities. Cell efficiencies of 19.3% and 17% were achieved on float zone Si using photolithography and screen-printed contacts, respectively. Screen-printed bifacial float zone Si cells with RTO/SiN_x surface passivation also resulted in an efficiency of 17%. SiN_x-induced hydrogen passivation of Si ribbons has been found to be most effective when the SiN_x post-deposition anneal includes controlled rapid cooling and backside Al alloying. Vacancies generated during Al alloying enhance the dissociation of hydrogen molecules and the flux of atomic hydrogen deep into the bulk Si to improve bulk passivation. RTP contact firing was found to be more effective in preserving the hydrogen defect passivation achieved during the initial hydrogenation step and has resulted in 4-cm² screen-printed cell efficiencies as high as 14.7% on 300 μm thick String Ribbon Si and 14.6% on 300 μm EFG Si.

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SILICON RIBBONS – STATE OF THE ART AND RESULTS FROM UKN RESEARCH

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ABSTRACT: Crystalline silicon ribbon materials have a high potential to significantly reduce wafer costs in PV and therefore could lead to a reduction in Wp costs. But ribbon technologies can only be successfully implemented in the solar cell production chain if obtained efficiencies are high enough in order to benefit from their advantages (no material losses due to ingot casting and wafering, less energy consumption). Therefore detailed studies of material characteristics are necessary to develop solar cell processes adapted to the specific material needs (e.g. passivation of defects during processing). Only adapted solar cell processes based on standard mc solar cell processing techniques can use the full potential of cost reductions offered by ribbon techniques. In the first part of this paper the present state-of-the-art of crystalline Si ribbons for PV application will be addressed, the second part will present results recently obtained in this field at University of Konstanz (UKN).

1. SILICON RIBBONS

The PV industry currently faces a shift from mono to mc Si. While 85% of the module shipments (246 MW out of 288 MW) use crystalline Si technology, the largest fraction is now mc Si (54%, or 155 MW), only 31% or 90 MW are mono Si [1]. This might be caused by reduced wafering costs of mc Si in order to reduce Wp costs. But still wafering costs (silicon, ingot casting, sawing) sum up to 45-60% of the overall module costs [2], depending on the market size. This by far largest fraction of module costs is addressed when using Si ribbon techniques for wafer production. The most dominating benefit as compared to standard ingot casting techniques is the better usage of the Si material. While up to 68% of the Si is lost using ingot casting methods (30% during ingot casting, 34% during sawing, 4% during processing [3]), ribbons use >90% of the Si material for wafer production. Besides this higher yield of Si, a possible shortage of Si feedstock from the electronic industry within the next 3-5 years is another driving force to study different Si ribbon technologies for their applicability within the PV industry. Therefore, during the last decades more than 20 different ribbon technologies have been developed, some of them are listed in table 1.

Table 1: List of crystalline Si ribbon technologies introduced in the last decades [4,5].

Method			Year	Method			Year
Dendritic web	DW	M2	1963	Low angle silicon sheet growth	LASS	M3	1980
Stepanov	S	M1	1967	Interface-controlled crystallization	ICC	M3	1981
Edge-defined film-fed growth	EFG	M1	1972	Supported web	SW	M2	1982
Horizontal ribbon growth	HRG	M3	1975	Ramp assisted foil casting technique	RAFT	M3	1983
Ribbon-against-drop	RAD	M2	1976	Silicon-Film TM	SF	M3?	1983
Ribbon-to-ribbon	RTR	M1	1976	Ribbon growth on substrate	RGS	M3	1984
Silicon on ceramic	SOC	M2	1976	Horizontal supported web	HSW	M2	1985
Capillary action shaping technique	CAST	M1	1977	String ribbon	SR	M2	1987
Contiguous capillary coating	CCC	M2	1977	Two shaping elements	TSE	M1	1987
Inverted Stepanov	IS	M1	1977	Silicon sheets from powder	SSP	M1	1989
Roller quenching	RQ	M3	1979	Hoxan cast ribbon	HCR	M3	1989
Edge supported pulling	ESP	M2	1980	Hoxan spin cast	HSC	M3	1991

They can be distinguished by the form of the meniscus between solid and molten Si. M1 means a meniscus height in the order of the sheet thickness t (e.g. formed by a shaping element), M2 rises from a broad base (like the crucible melt level), M3 is characterised by a large solid/liquid interface area as compared to Wt (W = ribbon width) [4].

The meniscus M2 generally allows a greater tolerance of mechanical and thermal perturbations as compared to M1, whereas the M3 type meniscus achieves very fast growth rates through the use of a great solid/liquid interface area and an efficient extraction of the latent heat of fusion [4].

Especially the fast grown ribbon silicon contains a higher amount of crystal defects as compared to mono or ingot cast mc Si. Each ribbon has its own specialities, but generally higher dislocation densities and higher concentrations of C and/or O are observed. The grain size varies with pulling speed, too, whereas a high pulling speed normally results in smaller grains.

For a given wafer thickness high pulling speeds mean a higher throughput and lower wafer costs. But the measure for each new technology in PV will be the cost per Wp. Therefore not only wafering costs but also efficiency is very important. A significant reduction in wafering costs can permit a slightly lower efficiency and nevertheless result in an overall reduction of Wp costs.

Most of the ribbon techniques listed in table 1 have disappeared due to technical and/or financial problems over the years. Only five of them are still under extensive research/development. Table 2 contains information on these techniques.

*Table 2: Properties of the 5 ribbon techniques still under extensive research/development (year 2000).
For more details see [6].*

Material	Pull Speed [cm/min]	Throughput [cm ² /min]	Furnaces per 100 MW	Dislocation density [cm ⁻²]	Thickness [μm]	Resistivity [Ωcm]	[C] [cm ⁻³]	[O] [cm ⁻³]	As-grown diff. Length [μm]	Grain size	Status (MW)
DW	1-2	5-16	2000	10 ⁴ -10 ⁵	75-150	5-30 n-type		10 ¹⁸	<100	mono	R&D (<0.2)
EFG	1.7	165	100	10 ⁵ -10 ⁶	250-350	2-4 p-type	10 ¹⁸	<5x10 ¹⁶	10-300	cm	Prod. (12)
SR	1-2	5-16	1175	5x10 ⁵	100-300	1-3 p-type	4x10 ¹⁷	<5x10 ¹⁶	10-300	cm	Pilot (0.5)
SF	?	?	?	10 ⁴ -10 ⁵	50-100	1-3 p-type	5x10 ¹⁷	5x10 ¹⁷	<40	mm	Pilot (1-2)
RGS	600	7500	2-3	10 ⁵ -10 ⁷	300-400	2 p-type	10 ¹⁸	2x10 ¹⁸	<10	<mm	R&D

They can be found in different stages of development with only EFG in large scale production for several years yet. SR and SF have been in a pilot production phase in 2000, with SR starting large scale production in 2001. DW and RGS are still in the R&D phase, with a continuously operating RGS wafer production machine being able to produce 1 wafer/s currently under development at ECN (Netherlands).

The slower pulling speed for DW, EFG and SR limits the throughput per furnace and therefore affects the number of furnaces needed for a 100 MW production capacity. The higher throughput for EFG is caused by the closed octagon with eight faces as compared to e.g. SR or DW, where currently only one sheet (width 8 cm) is pulled out of the melt.

The number of furnaces per 100 MW is also influenced by the efficiency obtained for the ribbon silicon solar cells. Mc ribbon materials in the as-grown state tend to be of inhomogeneous crystalline quality because of specific crystal defects caused by dislocations, grain boundaries and impurities, some of them (O, C and/or metals) decorating other defects. E.g. in RGS the high O-concentration leads to small diffusion lengths of the as-grown ribbon.

Because of these defects, solar cell processing has to be adapted to the special material needs of the ribbons. The passivation of crystal defects by atomic hydrogen is of particular interest in order to increase diffusion lengths during processing. Other tools for enhancing the material quality are gettering steps (Al- or P-gettering) which are implemented in the cell process. For some ribbons synergetic effects of hydrogenation in combination with gettering steps have been observed [7-9]. Material quality can be significantly improved by these steps, and maximum efficiencies reached for the ribbons described in table 2 are listed in table 3. Efficiencies have to be looked upon separated by cell size and process complexity. The lab-type efficiency shows the potential of the ribbon technology in the present R&D phase, while the industrial process on large area cells gives a measure of efficiencies reachable in an industrial environment. Although lab-type efficiencies already demonstrated good results, research activities for a better understanding and improvement of material properties are still necessary in order to

develop solar cell processes adapted to the special ribbon material needs. This should narrow the gap between lab-type and industrial-type process efficiencies.

Table: 3: Maximum efficiencies reported for the five Si ribbons listed in table 2.

Material	η_{\max} lab-type (institution)	Cell size [cm ²]	η_{\max} industrial process (institution)	Cell size [cm ²]
DW	17.3% (EBARA+GT) [10]	2x2	14.5 (EBARA) [28]	5.2x10
EFG	16% (GT) [29]	1x1	>15%, average 14.5% (ASE) [11]	10x10
SR	16.2% (GT) [12]	2x2	14.3% (UKN) [13]	8x10
SF	16.6% (AP) [14]	1x1	12.2 (AP) [15]	240
RGS	12.5% (UKN) [16]	2x2	9.6% (UKN+IMEC) [17]	8x10

2. RIBBON SILICON RESEARCH AT UKN

Research on crystalline ribbon Si at University of Konstanz (UKN) has been carried out in the past in the frame of European and national research programs as well as in bilateral projects financed by industry. Detailed studies have been carried out on EFG, SR and RGS. As these materials are in different stages of development, the emphasis of research lies on specific topics for each material. In the following a short overview and insight of the activities currently under focus will be given.

2.1 EFG

EFG [18] by ASE is a well established material as compared to other Si ribbons. It has been used in production for several years, but nevertheless further improvements in material quality as well as in cell processing can lead to even higher efficiencies. Especially wafer regions of poorer crystal quality showing lower lifetimes can limit cell efficiencies. Therefore an effective passivation of these regions is one major topic at UKN research, apart from fundamental investigations and the development of new processing steps.

A mapping method has to be chosen, if information from areas of good and poor quality wants to be obtained. The method chosen by us was the microwave induced photoconductance decay (μ -PCD) measurement of the bulk lifetimes (Janus 300 by AMECON). Surface recombination is suppressed by an effective passivation using an J/alcohol solution for each measurement. Process monitoring sequences have been compiled in order to measure the effect of each passivation or gettering step, or any synergetic effects. Lifetimes have been measured spatially resolved on as-grown wafers, after P-diffusion, after Al-gettering, after P-Al-cogettering, after H-passivation (using remote plasma) and after illumination. Before each measurement the surfaces have been etched. In this way surface passivation was identical. On the other hand this made several (7) processing sequences necessary in order to determine possible interactions between different processing steps. The study will be presented in detail at [8], in the following a short excerpt is given. Fig. 1 shows one of the process sequences.

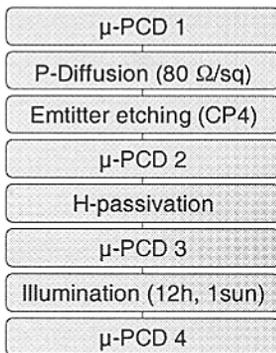


Fig. 1: One of the seven processing sequences used for process monitoring.

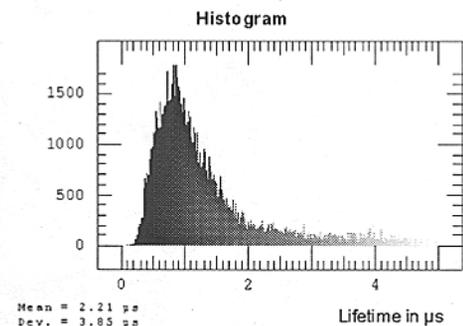
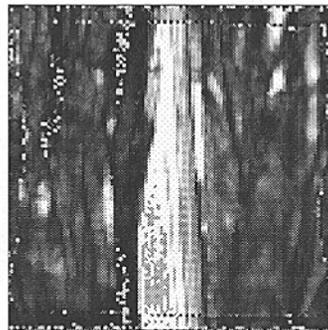


Fig. 2: Bulk lifetimes of the as-grown EFG wafer (μ -PCD 1 of Fig. 1).

The as-grown EFG wafer exhibits strong lifetime variations from $<1 \mu\text{s}$ to values $\bullet 10 \mu\text{s}$. Therefore it is necessary to adapt the fit window of the transient to the lifetime. This means that every wafer has to be measured several times with different transient fit windows for each lifetime region. The measurement in Fig. 2 is the result of only one measurement with one specific fit window length ($20 \mu\text{s}$). By using this window range, lifetimes exceeding $6 \mu\text{s}$ are not measured correctly, and lifetimes above $\bullet 10 \mu\text{s}$ can not be measured at all (grey points in the good regions of Fig. 2). This is even more important for measurements after gettering or hydrogenation steps. In these cases variations between some μs and some hundred μs lying adjacent on one wafer can be found. To measure these wafers correctly, several measurements with adapted fit window lengths for each specific region have to be carried out. An example is given in Fig. 3 ($\mu\text{-PCD 3}$ of Fig. 1), showing the same wafer as in Fig. 2 after P-diffusion, H-passivation and illumination.

The peak value (highest frequency in the histogram) could be shifted from $<1 \mu\text{s}$ (as-grown wafer in Fig. 2) to $18 \mu\text{s}$. The mean value of the distribution increases from 2.2 to $30 \mu\text{s}$ (without the inserts in Fig. 3). The measurement in Fig. 3 is put together using three measurements with different fit window lengths. The first measurement was taken with a fit window of $160 \mu\text{s}$, the two inserts with $20 \mu\text{s}$ (left) and $380 \mu\text{s}$ (bottom). In this way lifetimes can be determined correctly, although differing strongly within the wafer. In the bottom part lifetimes $>350 \mu\text{s}$ could be detected. The result before illumination is more or less identical to Fig. 3, therefore we conclude that H-passivation within the sequence given in Fig. 1 is stable under illumination.

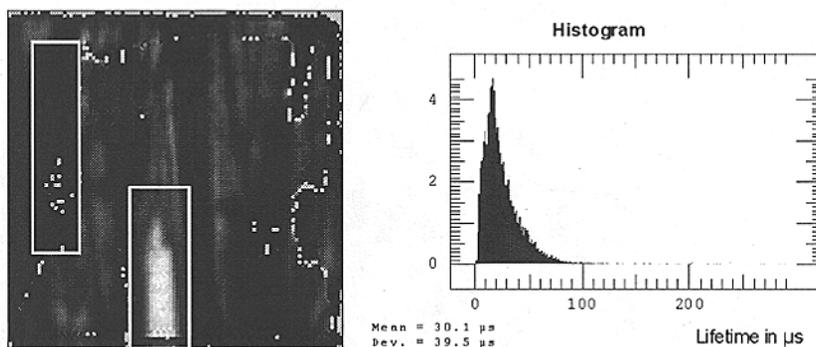


Fig. 3: Lifetimes after P-diffusion, H-passivation and illumination according to $\mu\text{-PCD 4}$ in Fig. 1. Note the different scaling as compared to Fig. 2. The two inserts are not included in the histogram.

2.2 SR

SR [19] by Evergreen Solar just made the step from pilot line to production. A new plant has been opened recently in Marlboro (MA, USA) and production is currently ramped up. In this stage it is helpful to determine the potential in efficiency of the current material used for production. In this way single processing steps can be checked and adjusted. Therefore partly processed wafers in different stages of processing have been shipped from Evergreen Solar to UKN and vice versa. Two reference batches have been processed completely at Evergreen and UKN respectively. Results from these batches are given in Fig. 4.

A gap of 1.4% absolute in efficiency could be detected between the Evergreen and UKN processes. By exchanging the single processing steps the influence of each step (diffusion, SiN, metallisation) on efficiency could be detected, which can help to increase the efficiency in production. The best cell of the UKN process showed an efficiency of 14.3% ($8 \times 10 \text{ cm}^2$) using a $40 \Omega/\text{sq}$ emitter [13]. Higher sheet resistivities should lead to efficiencies $>14.5\%$ in the near future. The best SR cell processed at Evergreen to date showed an efficiency of 13.3% ($8 \times 15 \text{ cm}^2$, [20]).

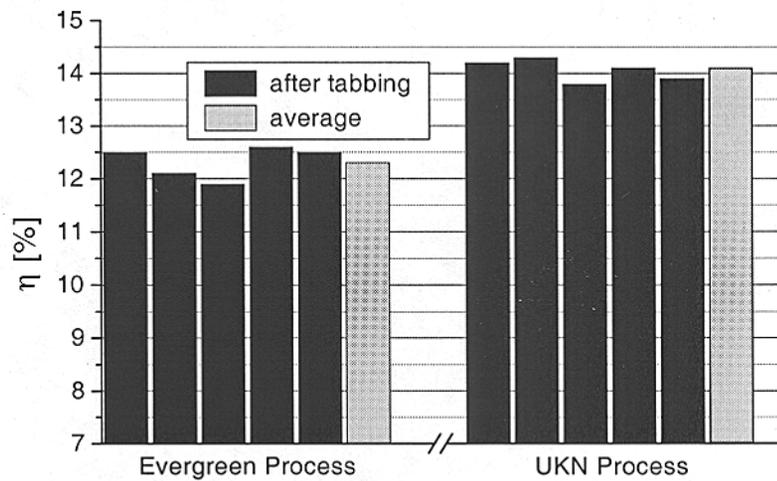
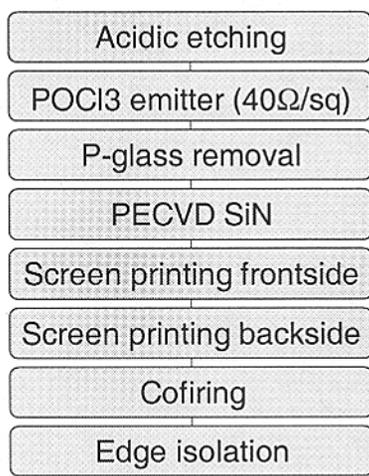


Fig. 4: Flow of the UKN process applied for the SR study (left) and results of this process in comparison to the current Evergreen process (cell size for this study: $8 \times 10 \text{ cm}^2$). An increase of 1.4% absolute in efficiency (14.1% as compared to 12.7% averaged over 5 cells) could be achieved.

2.3 RGS

RGS [21] is one of the promising ribbon techniques combining the general advantages of ribbon techniques (no Si losses) with a very high production rate. RGS was developed by Bayer AG and a new production machine is currently constructed and built up at ECN (Netherlands). This new machine will be capable of producing 1 wafer/s and is run under thermal equilibrium conditions. All wafers fabricated to date origin from a discontinuous lab-type machine producing 10 wafers per run under non thermal equilibrium conditions. This made research and development of RGS solar cells a difficult task in the past. Nevertheless extensive research has been carried out at UKN within the last five years on RGS silicon. The material from the discontinuous machine contains a high amount of O which might cause problems during solar cell processing because of the formation of electrically active recombination centres. Therefore a high temperature annealing step is applied to RGS directly after crystallisation to form large O-precipitates and reduce the amount of interstitial O [22]. The lab-type solar cell process developed at UKN and described in [23] results in two types of solar cells with examples of their typical behaviour given in Fig. 5.

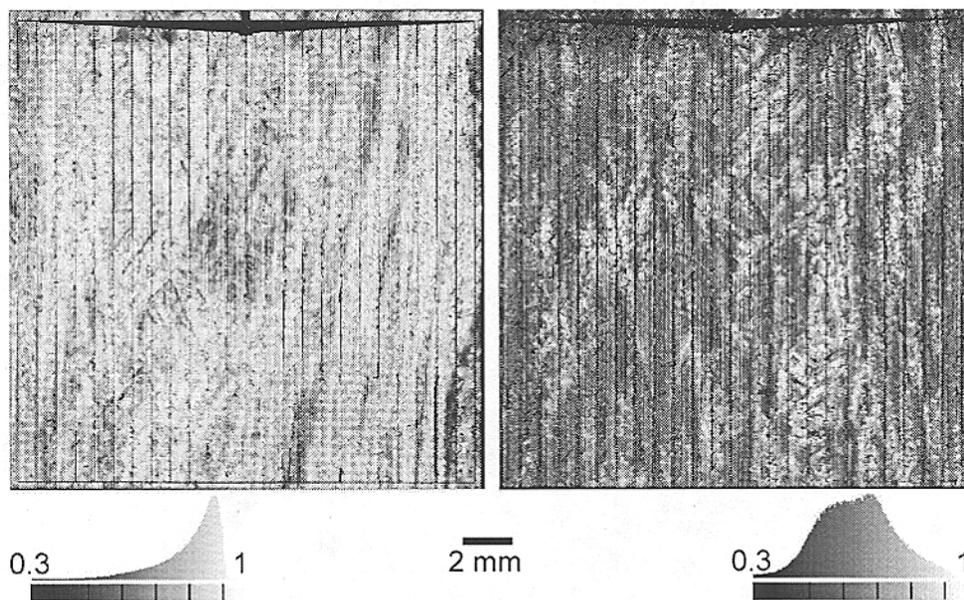


Fig. 5: IQEs of two RGS solar cells ($2 \times 2 \text{ cm}^2$) showing the same record efficiency of 12.5%. The left cell shows an extremely high J_{sc} of 34.5 mA/cm^2 but poor FF and moderate V_{oc} , the right cell shows normal J_{sc} (31.1 mA/cm^2), comparably good FF and good V_{oc} (Details in [24]).

For both cells bulk lifetimes $< 1 \mu\text{s}$ after processing have been determined. Although the cell surface was mechanically V-textured in order to enhance the carrier collection probability, the extremely high current of the cell on the left in Fig. 5 can not be explained with a conventional emitter structure. In collaboration with MPI für Mikrostrukturphysik (Halle, Germany) EBIC measurements using a special set-up have been performed on cells showing the high currents. An example of a V-grooved RGS solar cell from this investigation is given in Fig. 6. More details are given in [24].

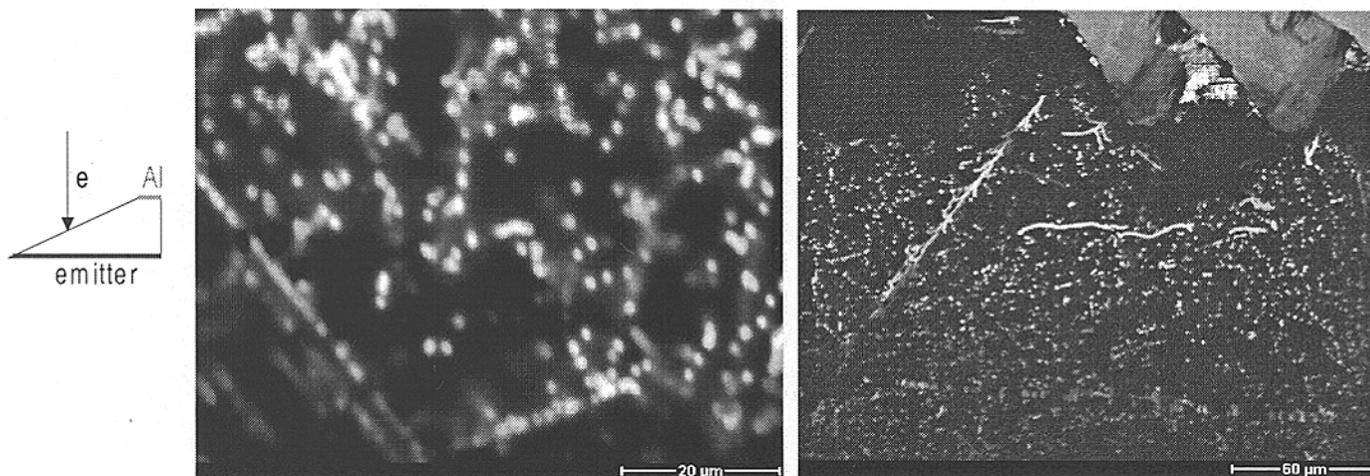


Fig. 6: EBIC measurement of an RGS solar cell region showing an extremely high current. Left: Measurement principle. Middle: EBIC measurement with the electron beam hitting the backside of the cell resolving individual current collecting channels. Right: Cross sectional EBIC measurement of the cell revealing the V-groove texture and the collecting channels within the whole bulk volume of the cell. (EBIC study carried out by M. Langenkamp, MPI Halle).

In collaboration with other institutes a lot of effort went into the investigation of the chemical and physical nature of these collecting channels. While the Halle group could show that channels are linked with dislocations [25], transmission electron microscopy and locally resolved SIMS studies revealed that closely packed precipitates along dislocation lines are found in areas of high current collection [26]. Capacitance measurements show a difference in low and high frequency signal behaviour, which is a hint that minority carriers are involved during charge reversal. Therefore we think that current collection is caused by local inversion from p-type material into n-type at the precipitates [22,30]. If the precipitates are closely packed along dislocations they form a 3-dimensional n-type network which is in contact with the front side emitter collecting current from the whole cell bulk volume despite of a small bulk diffusion length. A new method to determine mapped minority carrier diffusion constants revealed a 3-dimensional current collecting emitter structure in RGS cells, too [27].

While efficiencies are not negatively influenced by these current collecting channels, they might be a useful tool to enhance J_{sc} in a material of low lifetimes.

3. SUMMARY

Si ribbon materials have the potential to significantly reduce the W_p costs in PV. The ribbons differ strongly in throughput (pulling speed), which is linked to material quality. Generally, high speed growth method with a high throughput lead to very low wafering costs but to higher defect densities. These defects have to be handled during solar cell processing in order to reach sufficient efficiencies. While more than 20 ribbon technologies have been developed within the last decades, only a small amount of them is still under active research/development. They can be found in different stages of development with EFG already in full size production (12 MW in 2000, 20 MW planned for 2001). String Ribbon started production in 2001, while Silicon FilmTM is coming to the production phase as well. Dendritic Web and RGS are still in the R&D phase with a continuously producing RGS machine under construction at the moment. If material from this machine can be used for efficient solar cell processing this would mean a further step to a significant reduction of W_p costs by the use of silicon ribbons.

Research on ribbon silicon at UKN is currently carried out on EFG, String Ribbon and RGS material. For EFG the passivation of defects by gettering and hydrogenation techniques is a major concern. A spatially resolved process monitoring study shows the effectiveness of these steps in areas of different crystalline quality.

The standard UKN industrial-type cell process led to 14.1% average efficiency for large area String Ribbon solar cells. Using the results of an exchange of processing steps could enable Evergreen Solar to reduce the gap between the UKN results and the current industrial Evergreen cell process.

For RGS fundamental studies on lab-type material have been carried out. The lab-type solar cell process developed at UKN resulted in the highest efficiencies for RGS material to date (12.5%) and a recent focus of research was the investigation of current collecting structures in low lifetime material showing extremely high values of J_{sc} .

ACKNOWLEDGEMENTS

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Protocrystalline-Microcrystalline Phase Transitions in Si:H Materials and Their Effect on Solar Cell Characteristics

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Significant progress has been made in improving the performance and stability of a-Si:H based p-i-n and n-i-p solar cells using customized cell structures and protocrystalline intrinsic layers prepared with hydrogen dilution of silane, R. [1,2,3,4,]. Recently systematic studies using real-time spectroscopic ellipsometry (RTSE) have previously identified and described the *thickness-dependent* transition from the amorphous to microcrystalline phases for Si:H films prepared with hydrogen dilution [5,6,]. A phase diagram resulting from these studies is illustrated in Fig. 1 indicating the regimes in which predominantly amorphous and microcrystalline phases are obtained. The transition between the two phases is not abrupt and thus a mixed-phase region is included. It has also been found that the growth and evolution of the microstructure depends on the substrate material where deposition on crystalline and microcrystalline substrates, the boundary between phases is shifted to lower thicknesses [6].

Despite the merits of in-situ characterization, there is great difficulty in characterizing the electrical properties of the transition region since the resulting two constituent materials are probed in parallel using standard characterization due to the coplanar measuring configuration. It is believed that the largest improvements in the microstructure of the material are obtained at larger R (~40), thus it becomes difficult to characterize such thin amorphous films using conventional techniques.

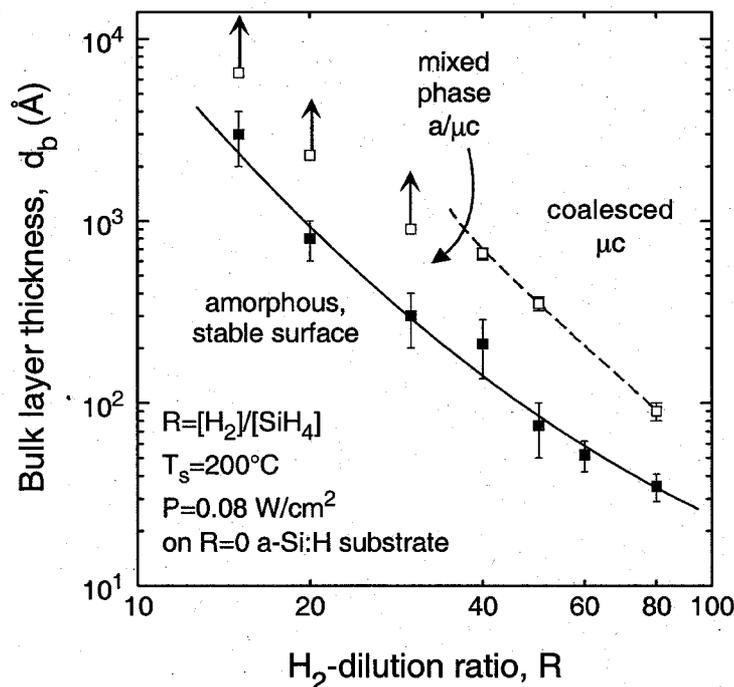


Fig. 1. Evolutionary phase boundary (solid line) separating the deposition of a-Si:H (left) and μ c-Si:H (right) as a function of layer thickness d_b and H₂ dilution ratio R on an a-Si:H (R=0) substrate.

The observed strong effect of the substrate on the microstructure of the over-deposited material also makes it very difficult to obtain meaningful correlation between properties of intrinsic films deposited on such substrates and the i-layers in cell structures which are typically deposited on doped a-SiC:H alloys or μ c-Si:H. In the work presented here such difficulties have been circumvented by characterizing the properties of the intrinsic material which are incorporated into the solar cell structures directly so that many of the ambiguities and invalid assumptions about film growth are eliminated.

The effects of the transition from the amorphous to microcrystalline phase within the Si:H layers of p-i-n solar cells have been previously observed and insights have been obtained into the properties of some structurally graded materials [2,3,]. The distinguishing characteristics of protocrystallinity, a term used to describe a-Si:H prepared close to the amorphous-microcrystalline phase boundary in deposition parameter space, are materials with improved stability under illumination and increased ordering [1,6]. RTSE studies have also indicated that the way to optimize protocrystalline Si:H p-i-n cell structures is to exploit a microstructurally engineered p/i interface region obtained by a two-step variation of the i-layer H₂-dilution ratio $R=[H_2]/[SiH_4]$. However, there has been no quantitative correlation between the evolving microstructure of the Si:H films and the mechanisms responsible for the corresponding effects on solar cell performance. In this work we present results on a variety of solar cell structures in which the effect of the transition on cell characteristics are evaluated as well as on the optoelectronic properties relevant to solar cell operation. Correlations between the material properties and corresponding cell characteristics are presented and discussed based on the combination of real time in situ studies of Si:H growth with parallel characterization and numerical modeling of the resultant cell structures.

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Le Châtelier's "Principle of Moderation" and the self-passivation of extended defects in CIS materials

Billy J. Stanbery

Introduction

Inspecting the subject list for this silicon PV materials and processes workshop reveals how keenly aware this research community is of the importance of defects and their distributions on the performance of minority carrier devices like photovoltaics. Economic necessity drives our efforts to use less energy and time in the process of fabricating PV devices, which often translates into the use of less pure and crystallographically ideal materials. To compensate, defect passivation techniques are employed, which include the incorporation of impurities specifically for this purpose and process methods (*e.g.* gettering) intended to control or modify their distribution. Comparable methods are used to optimize devices fabricated from thin films of the ternary Cu–III–VI compounds and their alloys, which will be referred to in this paper generically as CIS. However, one of the reasons that devices formed of CIS materials have attracted such great interest in the PV research community has been their apparent insensitivity to crystallographic defect concentrations and disruptions of lattice coherence that at present remain intolerable in III–V or silicon PV devices. This paper will present the author's perspective on the reasons for this difference, in the hope that it will offer some insight into approaches for improved methods for silicon PV processing.

The basis for the ensuing analysis of defect structures and passivation in CIS materials is the author's recently developed statistical thermodynamic model for the point defect structure of CIS¹. It is the first associated solution model for the phase equilibria and defect concentrations in α -CIS, and is based on the combination of published phase diagram studies² and *ab-initio* quantum mechanical calculations of defect formation enthalpies in CuInSe₂³ with the author's entropy calculations. A novel method was developed to solve problems of this sort, combining a lattice cluster expansion with the stoichiometric reaction analysis approach. The computation of equilibrium crystallographic defect concentrations using reaction analysis methods was pioneered in the 1950's by Schottky⁴ and Kröger⁵ (among others), and are sometimes referred to as quasichemical reaction methods. Although that terminology will be used here, note that the author's method is not based on Guggenheim's "quasichemical approximation" for computing configurational entropy.⁶ Le Châtelier's "Principle of Moderation" in chemical equilibrium theory may be stated as:⁷ "If an attempt is made to change the pressure, temperature, or concentration of a system in equilibrium, then the equilibrium will shift, if possible, in such a manner as to diminish the magnitude of the alteration in the factor that was varied." This paper will argue that the intrinsic self-passivation mechanisms in CIS materials may be understood as a consequence of Le Châtelier's "Principle of Moderation" in the context of the author's quasichemical reaction model for CIS defects.

Characteristic Point Defect Structures in CuInSe_2

In an elemental semiconductor like pure silicon, relatively few intrinsic isolated point defect types can form compared to multinary compounds: vacancies, interstitials, and electronic defects (charged lattice defects and electrons or holes in the conduction or valence bands, respectively). Defect complexes can also form by the interactions of these fundamental defects with each other. The introduction of foreign atoms to the lattice of an elemental semiconductor enables the possibility of forming a vastly greater number of defects. Despite this conceptual possibility of combinatorial explosion most impure elemental crystals are dominated by just a few of these because their formation energies are sufficiently non-degenerate. Absolute defect concentration levels in impure silicon are constrained by the solubility limit of the foreign atoms imposed by the segregation of secondary phases. Except in the case of aliovalent impurities (*e.g.* germanium), this limits foreign impurity concentrations to $\leq 1\%$ at. In either case the ability of the silicon lattice to accommodate isolated point vacancies is orders of magnitude less than this. Similarly, most III–V compounds are intolerant of high point vacancy concentrations. In excess of these limits, amorphous domains, microvoids, cracks, or (sub-) grain boundaries form by the aggregation and strain-induced generation of the isolated point defects. In both impure silicon and binary compounds, the corresponding multinary phase diagrams mirror the ability of their lattices to accommodate defects in the breadth of their respective homogeneity ranges. This is on the order of 10^{-6} in the case of GaAs, and comparable in silicon.

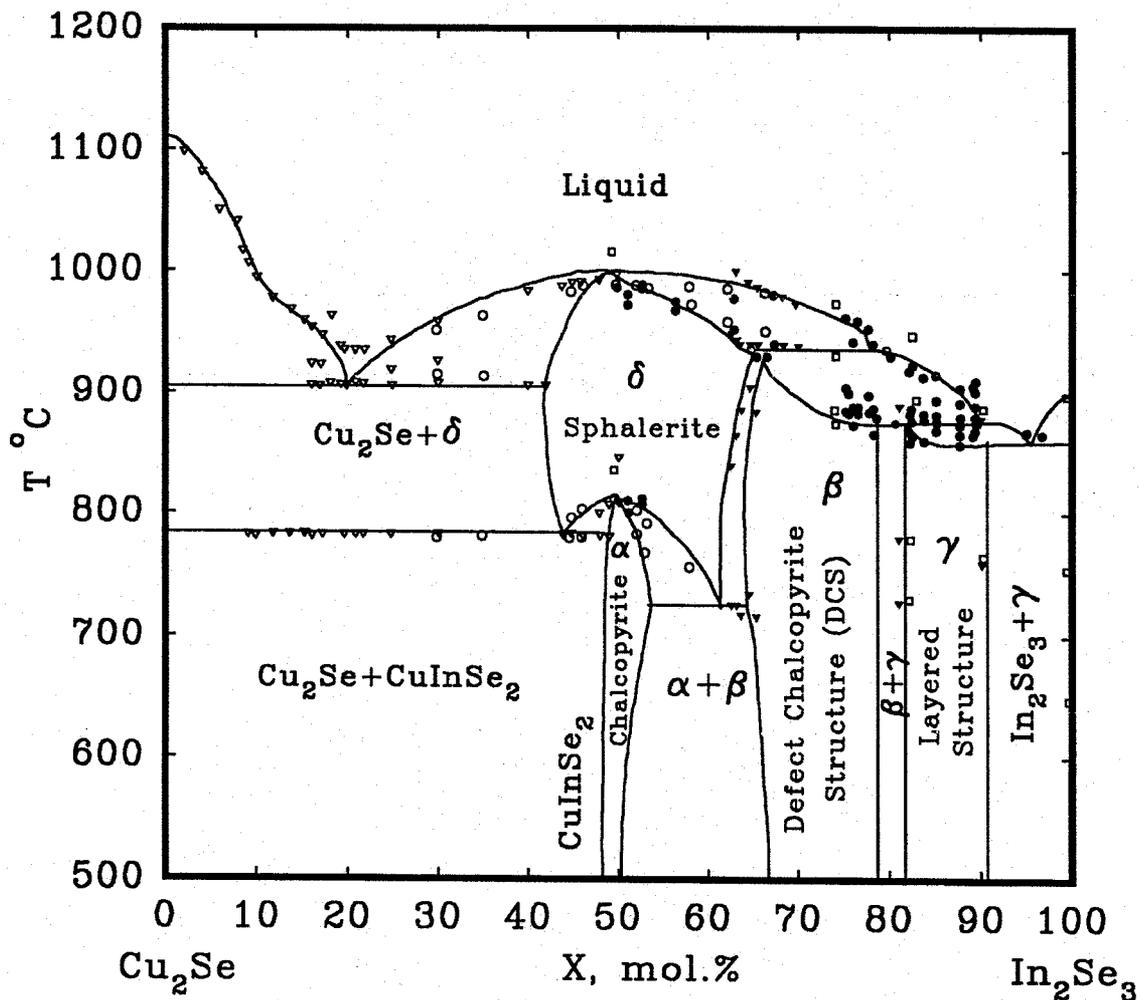


Figure 1 Assessed phase diagram along the Cu_2Se – In_2Se_3 pseudobinary section of the Cu–In–Se chemical system.²

Figure 1 shows the pseudobinary section of the Cu–In–Se ternary phase field. The α -CIS phase corresponds to the compound CuInSe_2 and crystallizes in the chalcopyrite structure, characterized by tetrahedral coordination of every lattice site to its nearest neighbors, as in silicon. It is distinguished from the zincblende structure of the binary Grimm-Sommerfeld compounds⁸ (e.g. GaAs or CdTe) by ordering of its *fcc* cation sublattice into two distinct sites, one occupied in the ideal structure by copper and the other by indium. Note the breadth of the α -CIS phase, which, depending on temperature, is on the order of 1%. Thus the intrinsic defect structures of the CIS lattice enable it to accommodate composition variations comparable to the foreign impurity concentration limits characteristic of silicon. In fact, both this author's computational defect model and recent experimental results⁹ agree that stoichiometric CuInSe_2 is itself unstable with respect to secondary phase segregation. In other words, all single-phase α -CIS is nonstoichiometric in equilibrium, or conversely, stoichiometric single-phase CuInSe_2 does not exist in equilibrium. What mechanisms provide CIS this property without inhibiting good minority carrier transport?

One principle that helps to understand the answer to this question was first elucidated by Groenink and Janse,¹⁰ who outlined a generalized approach for atomistic analyses of the defect chemistry of ternary compounds. They showed that the electroneutrality condition implies that for any given combination of the thermodynamic variables the concentrations of some pair of defects with opposite charges will be much higher than the concentrations of all other charged defects (presuming none are energetically degenerate). Groenink and Janse referred to these as the “majority defect pair.” Note that this conclusion neither implies nor presumes that the distributions of members of this pair are spatially correlated on the lattice, *i.e.* they do not necessarily form a complex. The author's computational defect model for the CIS lattice employs 24 different point defects and defect complexes, but as expected, majority defect pairs dominate the computed equilibrium defect concentrations. The dominant defect pair, however, changes with composition. The thesis of this paper can be fully described by the behavior of these defect pairs alone, so the others will not be discussed.

Within the single-phase homogeneity range of α -CIS along the pseudobinary section shown in Figure 1 the dominant defect pair is comprised of the ionized copper vacancy, V'_{Cu} , and the complex formed by the association of a copper vacancy with an indium antisite, $(V_{\text{Cu}} \oplus \text{In}_{\text{Cu}})$. In the Kröger-Vink notation employed above, the superscript indicates the defect's charge state and the subscript indicates the “normal” occupant of its lattice site in the ideal crystal. An accent means that the defect is negatively charged (an acceptor), a dot means that it is positively charged (a donor), and an “x” (not used above) means that the defect is neutral. Note that these effective charges are strictly speaking the deviation of the charge density on that lattice site from its normal state in the ideal lattice. The circle-plus symbol is used here to denote a complex. These donors and acceptors are found in nearly equal concentrations at all temperatures within this composition range, and the concentration of each increases almost linearly with the excess In_2Se_3 mole fraction. If the proportion of In_2Se_3 exceeds the single-phase composition limit of α -CIS, another phase forms in equilibrium, β -CIS, yielding a two-phase mixture. The mechanism by which this secondary phase forms is quite remarkable: when their concentration exceeds a certain threshold, the excess dominant defect pairs in α -CIS combine to create a neutral complex, $(2V_{\text{Cu}} \oplus \text{In}_{\text{Cu}})^x$. The Madelung interaction between these cation neutral defect complexes (NDC) makes it energetically favorable for them to aggregate and form the secondary β -CIS phase,

which in equilibrium precipitates as a crystallographically coherent superstructure of the chalcopyrite structure.

Thus α -CIS is electrically compensated at equilibrium, irrespective of its extent of deviation from stoichiometry on this pseudobinary section. For any composition along the pseudobinary section each type of atom could in principle be in a constant (its normal) valence state, as they are in the endpoint compositions Cu_2Se and In_2Se_3 . The mechanism by which nonstoichiometry is accommodated by the lattice for all compositions on the pseudobinary section in the α , β , and mixed $\alpha+\beta$ phase domains can be described by quasichemical reaction theory *via* the extent of the formation and dissociation reactions for the cation NDC:



This reaction does not change the valence states of any of the atoms on the lattice, and all of the disorder needed to accommodate nonstoichiometry of the crystalline compound along the pseudobinary section occurs on the cation sublattice. Furthermore, ab-initio quantum mechanical calculations have shown that the ground state and lowest excited electronic energy levels associated with this NDC lie within the valence and conduction bands of CuInSe_2 , respectively, hence its formation does not create any defect levels within the bandgap.³

The situation is necessarily different for compositions within the ternary phase field that are off the pseudobinary section. In those cases the stoichiometry imbalance would yield a net charge on the lattice if every atom were in its normal valence state, so charged defect states are inevitable. Two cases must be distinguished, depending on whether there is an excess of the metals or an excess of selenium relative to the pseudobinary section. In the former case the dominant defect is the selenium vacancy and single-phase α -CIS is *n*-type. Since only *p*-type CIS is used for solar cell absorbers, that case will not be discussed further here. In contrast, when excess selenium is incorporated into the lattice, it is accommodated by cation sublattice disorder alone. The nature of that disorder is easily understood as a consequence of the extremely high formation energy for the indium vacancy and selenium interstitial or antisite defects. If an excess pair of selenium atoms is incorporated, they will attach in their crystallographically proper positions to an ideal chalcopyrite CuInSe_2 lattice and thereby effectively create a pair of vacancies on the cation sublattice, one ideally occupied by indium and the other by copper. Since the indium vacancy is so energetically unfavorable, the lowest energy configuration turns out to be transfer of a copper from elsewhere on the lattice, yielding two copper vacancies and one copper antisite. Thus, the V'_{Cu} and Cu_{In} defects are the dominant defect pair when the CuInSe_2 compound's composition is slightly selenium-rich. In this case, however, they are created in roughly two-to-one ratios so the crystal is not completely compensated and the ionized copper vacancy shallow acceptor dominates, yielding *p*-type CIS.

When the lattice is both selenium-rich and indium-rich, as in device-quality CIS materials, further interactions between this V'_{Cu} and Cu_{In} dominant defect pair and the cation NDC occur, which mostly eliminate the compensation due to the Cu_{In} donor. This is important for devices, and explains the relative insensitivity of CIS device performance to stoichiometry variation within the limits imposed by the constraint that the absorber films must be both selenium and indium-rich. It also demonstrates that a certain degree of compositional control is in fact the method by which deleterious point defects are circumvented in CIS devices. It does not alone explain these

materials' apparent insensitivity to grain boundaries, dislocations, and other extended defects that would require intentional passivation in silicon. The ubiquity of the ionized copper vacancy in CIS, and recognition that its predominance persists over the wide compositional range actually found in CIS PV device absorbers is, however, an essential piece of the answer to this puzzle.

Ionic Transport in CIS

Historically, CIS was first investigated as a candidate material for thin film PV devices in an effort to solve a technological problem associated with its predecessor, Cu_2S . Copper sulfide thin film cells tended to fail under bias due to shunting, which occurred because of the formation of copper nodules within those films. From a thermochemical perspective, this represents phase decomposition of the compound into a two-phase mixture of $\text{Cu}_{2.8}\text{S}$ and nearly pure copper. Researchers suggested at that time that the addition of indium to the lattice might stabilize the crystal with respect to such decomposition,¹¹ which has proven true. Both $\text{Cu}_{2.8}\text{S}$ and $\text{Cu}_{2.8}\text{Se}$ are superionic conductors,¹² in which copper can diffuse easily, with very little driving force required. The addition of indium diminishes, but does not eliminate the mobility of copper on the lattice, even at room temperature.¹³

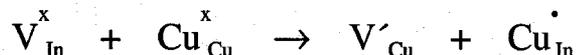
Recently the consequences of this remnant ionic conductivity have been recognized as the most likely explanation for the widespread observation of copper depletion at the surface of device-quality CIS absorber films. The investigators who first observed this believed that device performance was improved by processes that formed a secondary (indium-rich) β -CIS phase layer at the surface of the absorber.¹⁴ It has been subsequently shown that the properties of the copper-deficient surface layer on CIS absorber films are substantially different than those of the equilibrium β -CIS phase.¹⁵ The latter authors hypothesized that field-induced migration of copper ions away from the free surface, driven by the field resulting from pinning of the Fermi level there, leads to the observed surface copper depletion. Their conjecture is consistent with the considerable body of literature on field-enhanced electromigration of copper in CIS,^{16,17} which without exception conclude that a vacancy mechanism is most likely.

Self-Passivation of Extended Defects in CIS

Whereas the silicon lattice is characterized by strongly covalent bonding, the CIS lattice is characterized by bimodal bond heterogeneity. The In–Se bonds are strongly covalent in character, but the Cu–Se bonds are predominately ionic.¹⁸ Experiments on the synthesis of CIS by annealing of Cu_xSe_y and In_xSe_y thin film bilayer precursors show only limited interfacial reactions between these binaries at temperatures of 350°C or less.¹⁹ The crystallographic structures of all the binary indium selenides are characterized by hexagonal stacking of the selenium sublattice, whereas that of the ternary α and β -CIS phases are *fcc*. Apparently this structural transformation represents a kinetic barrier to the incorporation of copper onto the lattice of binary indium selenides, despite the manifest high mobility of copper in copper binary compounds and CIS.

These facts lead the author to characterize the structure of CIS as an In–Se framework that is relatively rigid and immobile at temperatures below about 350°C, filled with an adaptive pool of copper counterions. Persistent extended crystallographic defects such as dislocations must

involve disruption of the covalent In–Se sublattice. Such perturbations of crystallographic ideality may be frozen in during cooldown after CIS compound formation, but two mechanisms remain by which the system can respond to these perturbations to minimize its free energy: electronic and copper-related defect formation. Indium sublattice vacancies are the single most energetically unfavorable point defect on the lattice, so the quasichemical reaction



is a reaction that yields an increase in the extent of formation of the dominant defect pair in indium and selenium-rich CIS materials like those used for devices. Neutralization of the only other indium cation point defect, the antisite, by association with the ubiquitous copper vacancy defects to form the NDC has already been described, and is given by the reaction



Neither of these reactions is frozen out at low temperatures because they only involve the redistribution of the demonstrably mobile copper atoms. Deep-level indium-related point defects associated with extended lattice defects that would otherwise act as recombination centers (V_{In}^x and $\text{In}_{\text{Cu}}^{\cdot\cdot}$) are passivated by the redistribution of copper to yield more benign defects. The physical mechanism driving their diffusion is electromigration under the influence of the locally strong fields created by charging of those deep-level defects themselves.

Conclusions

The author hopes that the foregoing analyses have made the thesis of this paper self-evident. If one views extended defects in the covalent indium-selenium sublattice of CIS as a perturbation of the ideal lattice which is kinetically frozen into CIS crystals during cooldown after their synthesis, the result is an increase in the concentration of indium-related defects above their equilibrium value. Le Châtelier's "Principle of Moderation" states that the equilibrium will shift to diminish the magnitude of this increase, if possible. It is possible in CIS, because the ionic character of copper bonding in these materials enables its mobility to persist at room temperature and to respond to the influence of fields generated by deep level defects. The concentration of deep level defects is thus moderated by increases in the extents of the quasichemical reactions given above, whose reaction products are relatively benign neutral or shallow centers.

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Methods in Microelectronics for Rapid Thermal Annealing of Implanted Dopants

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Rapid thermal annealing (RTA) with a short dwell time at maximum temperature is used to reduce the diffusion of implanted dopants and to form shallow junctions in CMOS transistors. Advanced methods use "spike anneals," wherein high temperature-ramping rates are used for both heating and cooling, while also minimizing the dwell time at peak temperature. Current implementations heat single wafers with incandescent or electric arc lamps, or use a steady heat source with rapid wafer transfer. Since junction profiles are sensitive to annealing temperature, the challenge in spike annealing is to maintain temperature uniformity across the wafer and repeatability from wafer to wafer. Deviations of wafers' emissivities from that of bare Si are incorporated in sophisticated techniques for accurate temperature measurement and control. Examples will be discussed for annealing of low energy implants of B in crystalline Si for junction formation and B in polycrystalline Si for gate electrode formation.

I. Introduction

Ongoing advances in techniques for rapid thermal annealing of implanted dopants are being driven by the reduced dimensions of CMOS transistors in integrated circuits with successive technology generations [1]. Rapid thermal annealing proves to be indispensable in forming the source and drain contact junctions, shallow extension junctions between the channel and contacts, and electrically active polycrystalline silicon gate electrodes. These process applications require exquisite control of wafer temperature because diffusion and electrical activation of the dopants have high thermal activation energies, $\sim 3 - 5$ eV. Rapid thermal methods are also used to form, anneal, or reoxidize gate dielectrics such as nitrided SiO_2 and metal oxides with high dielectric constants. Other, less critical applications include, for example, making contacts by silicide reactions with deposited metal films, such as Co, and annealing of deposited films, such as insulator layers, TiN barrier layers, and Cu interconnect films. This paper considers activation of implanted dopants in Si wafers by infrared-based methods in state of the art microelectronics production. Results are presented for activating boron implanted in crystalline Si wafers and deposited polycrystalline Si (poly-Si) films. The former case deals with the phenomena of transient enhanced diffusion (TED) [2], which is inherently undesirable in the quest for shallow junction formation in advanced transistors. In the latter case, there is grain boundary enhanced diffusion of dopants in

poly-Si, which is desirable because a high concentration of active carriers throughout a poly-Si film is required to maximize the depletion capacitance of the gate electrode.

Formation of ultra-shallow junctions for the extension regions of the transistors is a major challenge, owing to the solid state diffusion of the implanted dopants during the course of thermal treatment. Transient enhanced diffusion, which is a temperature-dependent effect for implants of B and P species, is caused by coupled diffusion of the dopant with non-equilibrium excess Si interstitial distributions. Equilibrium dopant diffusion is recovered as the excess Si interstitial population is dissipated. Although the detailed mechanisms of TED may vary with dopant type, energy, and dose, the general observation is that the TED processes have low or negative activation energies. Thus it is energetically advantageous to electrically activate the dopants by reaching the anneal temperature as quickly as possible. Transient diffusion phenomena are the main reasons why slower batch furnace diffusion has been replaced by single-wafer RTA methods. The goal in junction formation is to achieve a low sheet resistance with a high concentration of electrically active dopants, with as little dopant diffusion as possible.

RTA methods use infrared heating that is characterized by near thermal equilibrium across the thickness of the wafer [3,4]. Several methods that originated in the 1970's, such as laser thermal annealing [5] and flash annealing [6], may eventually prove to be needed to suppress the dopant diffusion effects. Here, a high optical flux is utilized for faster heating and to either briefly melt the surface of the wafer or selectively raise the surface temperature. The rapid quenching can lead to lattice defects and dopant metastability, and consequently junction leakage and dopant redistribution during subsequent thermal processing steps. Consequently, these alternative techniques are still in the research and development stage.

P-type MOS devices (PMOS) are particularly challenging, owing to controlling (1) TED effects of B in crystalline Si and (2) B penetration through gates oxides from poly-Si electrodes [7]. Thus motivated, these two critical applications are selected for this presentation.

II. Rapid Thermal Annealing Procedures

A method denoted infrared spiking was implemented at AT&T during the 1960's in the manufacture of transistors by rapidly inserting and withdrawing Si wafers in a horizontal furnace. With modern adaptation to vertical orientation, this technique now utilizes the uniformity and reproducibility inherent in a steady heat source. Figure 1 illustrates the method [8]. The wafer is transported by rapid elevation in a bell jar heated with a vertical temperature gradient. Temperature is measured by a pyrometer that detects wafer radiance and emissivity, which is derived from the reflectivity. Wafer temperature is controlled by feedback to the motor controlling the elevator height.

Heating by an array of incandescent lamps, though now a popular method, was motivated originally because of reproducibility and uniformity problems with horizontal furnace method [3]. Figure 2 illustrates the method with wafer heating from the top side and wafer temperature measurement from the bottom side [9]. The heating lamps are arranged in a 2-dimensional array and are connected in annular zones that are controlled by independent, emissivity correcting temperature probes. Wafer rotation is used for azimuthal uniformity. Figure 3 illustrates a method where the lamps are arranged rows with the filaments parallel to the wafer and more efficiently surround

the wafer with heating radiation [10,11]. Figure 4 shows a method using a single high-power arc lamp within a reflector designed to uniformly heat the wafer and utilizes wafer imaging to map temperature [12]. Other methods, not shown, consist of either placing a wafer on a hot plate or capturing the wafer between two temperature-controlled plates [13]. Several of the methods use He gas to assist thermal conduction in heating and/or cooling.

FIG. 1. Schematic illustration of bell jar furnace with vertical wafer motion to control heating and cooling. Temperature and wafer emissivity are derived from reflectivity and radiance measurements. After Axcelis Technologies.

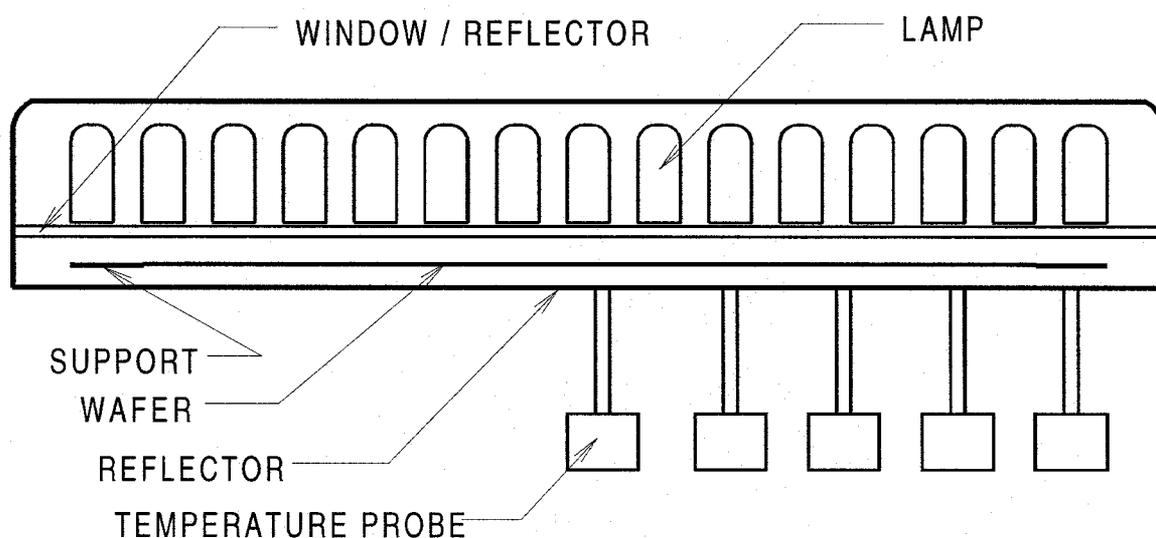
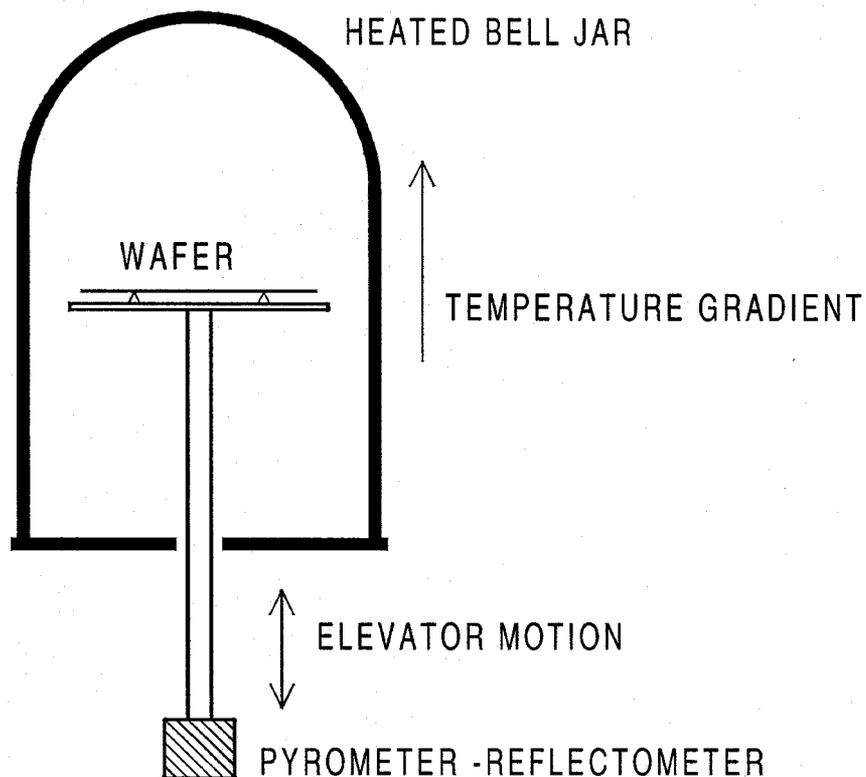


FIG. 2. Rapid thermal annealing chamber with a two-dimensional array of incandescent infrared lamps and temperature sensors for annular zone temperature control. Wafer is supported by a rotating ring. Schematic cross sectional view. After Applied Materials.

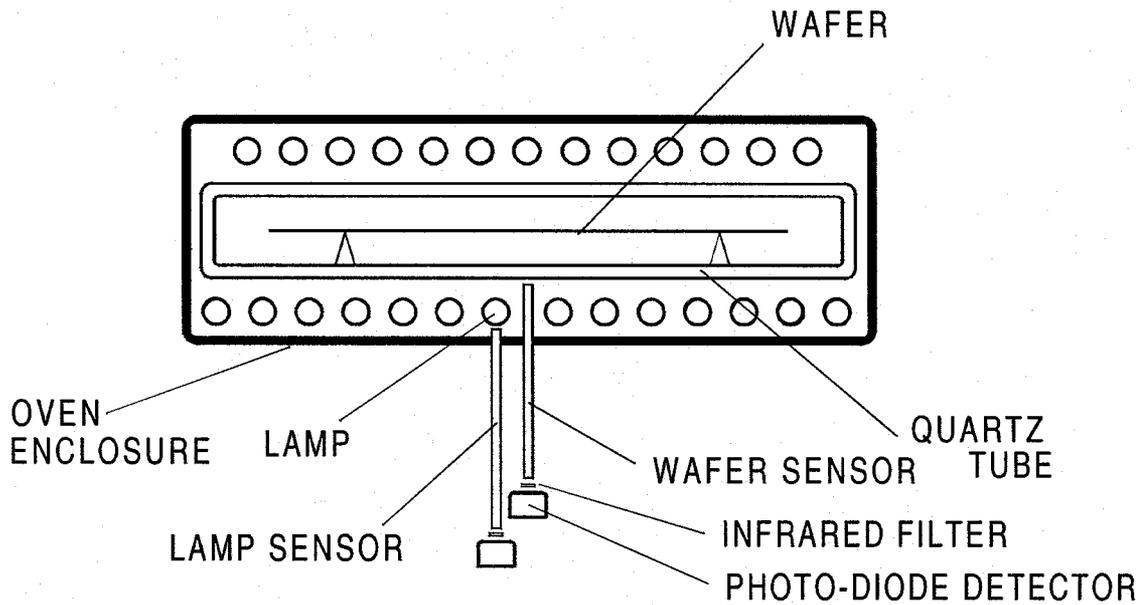


FIG. 3. Annealing chamber with dual-side heating with linear incandescent lamps, cross sectional view. Pyrometry method uses modulated lamp power and dual probes to determine wafer emissivity and temperature. After Mattson Technology, Steag AST Elektronik, and Bell Labs.

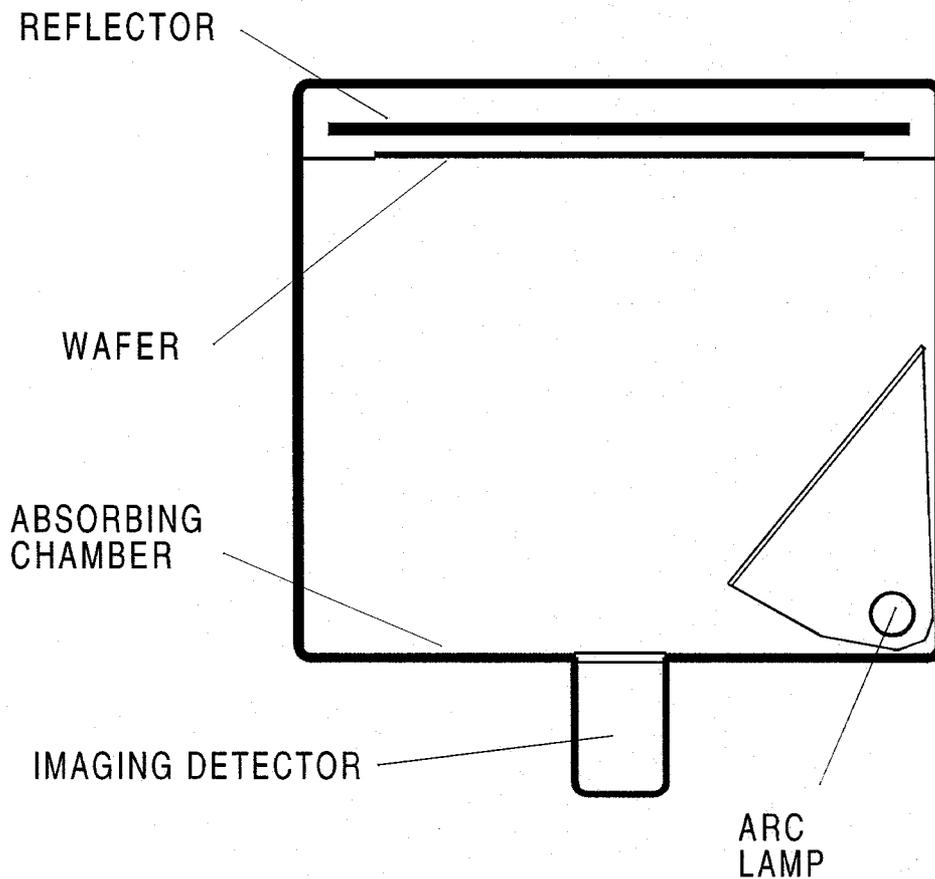


FIG. 4. Schematic of chamber with a single arc lamp in a reflector housing for heating wafer in absorbing chamber. Imaging detector utilizes full view of the wafer. After Vortek Industries.

The “spike anneal” RTA method pertains to minimizing the soak time at high temperature. Applications of the technique, which has advantages in controlling dopant diffusion in shallow junction formation [14], are discussed in the next sections. The various heating methods mentioned above have different temperature vs. time capabilities and limitations. Heating rates depend on the intensity and wavelength of the infrared radiation source, the switching time from heating to cooling, as well as radiative and convective dissipation of wafer heat during cool down. Figure 5 shows temperature vs. time traces for spike anneals obtained by the four of the methods. The arc lamp method produces the sharpest spike, owing to the inherent $\sim 10 \mu\text{s}$ response time of the lamp. The other methods produce spikes with more rounded peaks. Wafers are cooled by turning off the heating lamps or by withdrawing the wafer from the heater environment. Initial cooling at high temperature is by radiative heat transfer. Cooling can be accelerated by thermal conduction and gas convection at lower temperatures, e.g., by using He gas as the exchange medium.

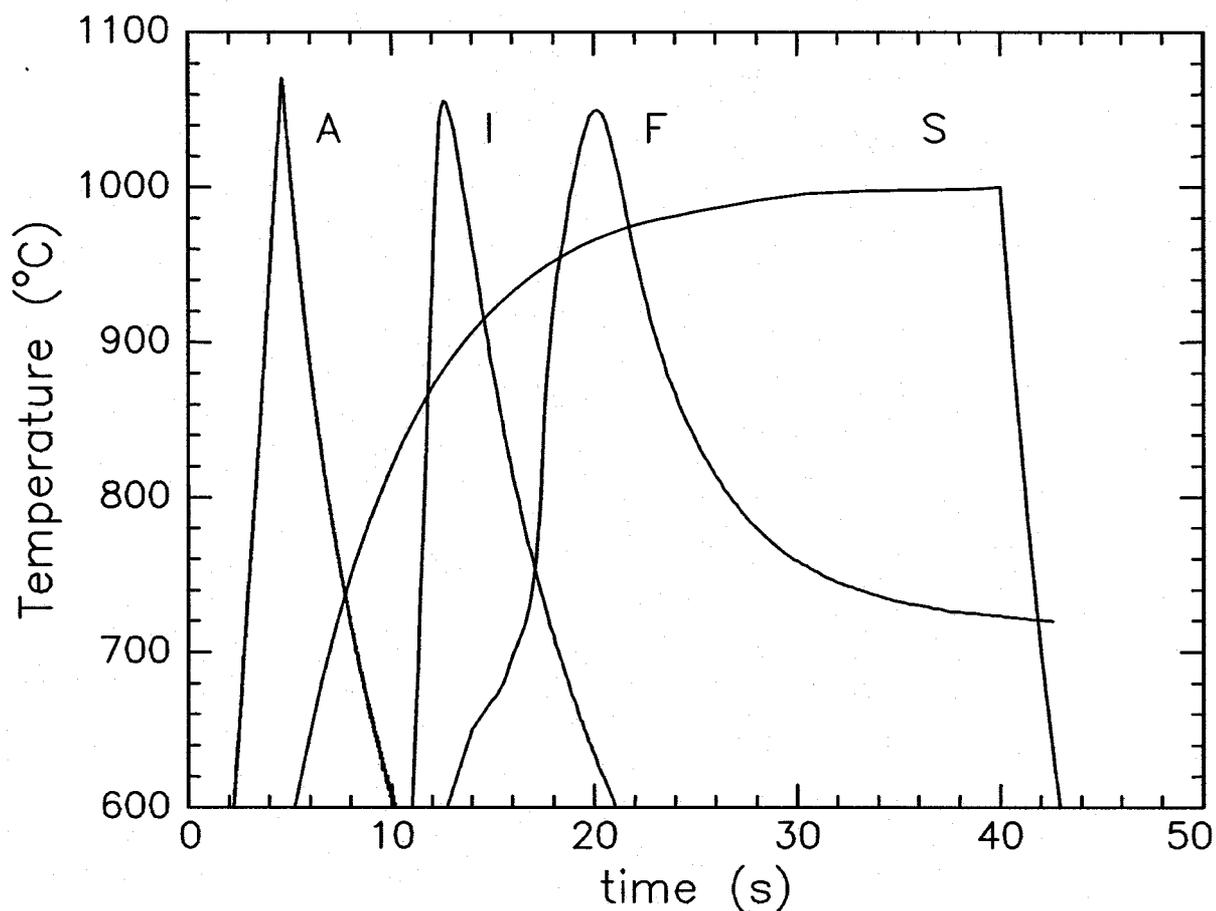


FIG. 5. Temperature sensor signal vs time for four RTA methods. A, arc lamp (e.g., Fig. 4); I, incandescent lamp with 2-sided heating (e.g., Fig. 3); F, bell-jar furnace (e.g., Fig. 1); and S, hot plate method. Preheat region below 600°C varies among methods. Origin of time is start of heating cycle in each case.

III. Dopants in Crystalline Si

The shallow junction extensions for p-channel transistors are formed by low energy B implantation followed by an activation anneal. A typical implant condition is 500 eV in energy and 10^{15} cm^{-2} in dose and is studied by uniformly implanting an n-type Si wafer. Figure 6 shows B concentration profiles in Si obtained by secondary ion mass spectroscopy (SIMS) after annealing this implant at various temperatures and times. The annealing method shown in Fig. 3 was used, where the temperature was ramped up at $150 \text{ }^\circ\text{C/s}$ and down at approximately $80 \text{ }^\circ\text{C/s}$.

A substantial portion of the B remains within 5 nm of the surface as an electrically inactive silicon boride phase [15]. This surface region of high boron concentration acts as a solid source of B, which diffuses more deeply into the crystal Si with increasing diffusion time. In this experiment, the anneal temperatures were reduced with increasing anneal times to yield comparable results for the sheet resistance, R_S . The sheet resistance is a measure of the portion of B that is electrically activated. Similar behavior is observed in the Hall coefficient, which yields the average sheet carrier density. Analysis of the electrical and SIMS data are presented in Table I. The junction depth parameter, X_J , is defined as the depth at which the B concentration equals 10^{18} cm^{-3} . The TED effect and differences between electrical activation and dopant diffusion lead to a 45% variation in the diffusion depth, which is much greater than the 9% variation observed

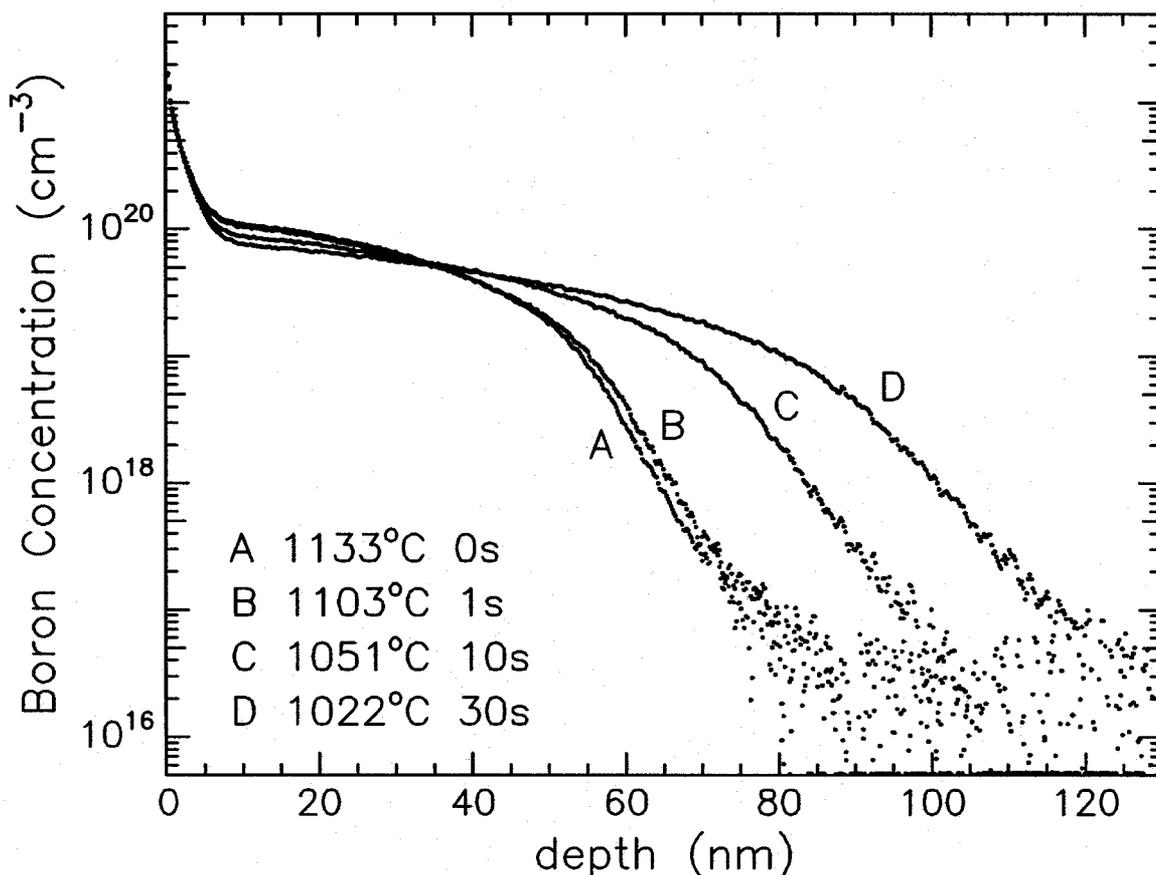


FIG. 6. Boron concentration in Si, from SIMS, of a 500 eV 10^{15} cm^{-2} B implant annealed in $\text{N}_2 + 0.1\% \text{ O}_2$ at temperatures and times given in the legend inset.

Table I. Sheet resistance and junction depth parameters for 500 eV 10^{15} cm^{-2} B implant at given anneal temperatures and times. Letter codes correspond to traces in Fig. 6.

	Temperature ($^{\circ}\text{C}$)	Time (s)	R_S (Ω/Sq)	X_J (nm)
A	1133	0	268	64
B	1103	1	256	66
C	1051	10	251	84
D	1022	30	245	101

for R_S . One concludes from the above data that a spike anneal, corresponding to nominally "0" time at temperature, provides the minimum dopant diffusion for a given R_S .

Electrical activation and diffusion of the B exhibit different effective activation energies. This is examined in Figs. 7 and 8 for a 1000 eV B implant. The anneal temperatures and times are both varied as in the previous case, but for this study the objective is to yield the same areal

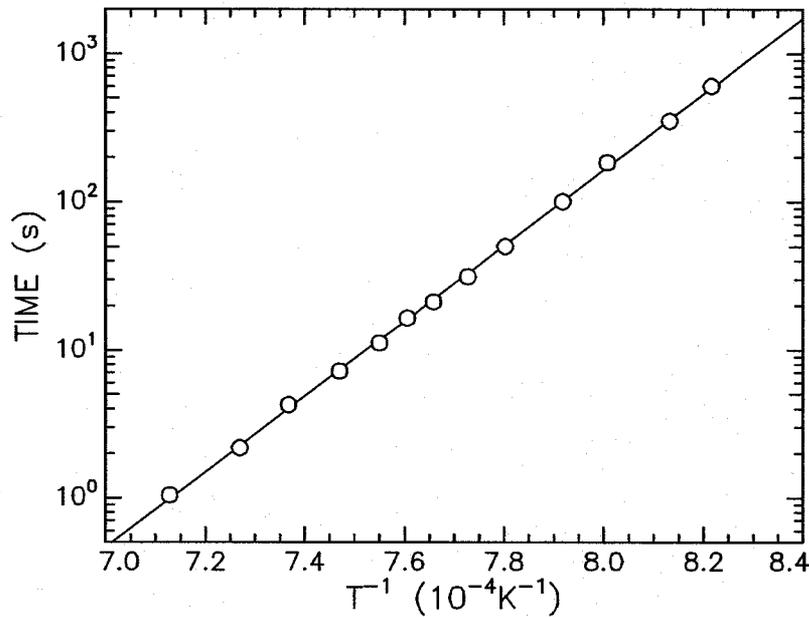


FIG. 7. Arrhenius plot of the time to reach a sheet carrier density of $6.5 \times 10^{14} \text{ cm}^{-2}$ for a 1000 eV 10^{15} cm^{-2} implant. Line is a fit to obtain the thermal activation energy for electrical activation, 5.1 eV.

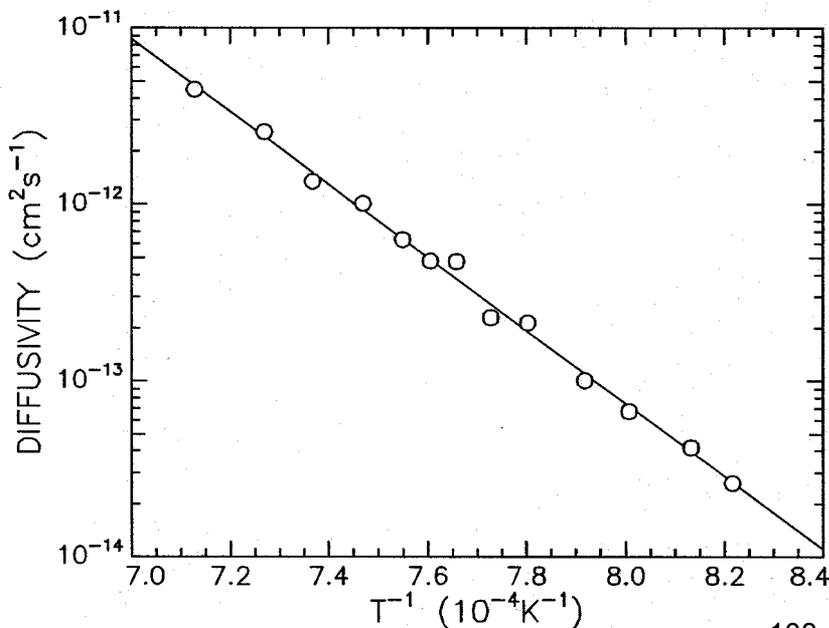


FIG. 8. Arrhenius plot of the mean diffusivity of B in crystalline Si for annealing a 1000 eV 10^{15} cm^{-2} implant. Temperatures and diffusion times (Fig. 7) correspond to a constant sheet carrier density of $6.5 \times 10^{14} \text{ cm}^{-2}$. Line is a fit to obtain the thermal activation energy for diffusion, 4.0 eV.

concentration of hole carriers, $6.5 \times 10^{14} \text{ cm}^{-2}$, as determined from the Hall effect. The Arrhenius fit of the temperature-time relationship in Fig. 7 indicates an effective activation energy of 5.1 eV. The thermal diffusivity of B, interpreted as an average over the anneal cycle, is shown in Fig. 8 and is fitted with an effective activation energy of 4.0 eV. The approximately 1 eV lower activation energy for diffusion indicates that spike anneals, with short time at high temperature, are favorable for suppressing diffusion of the B dopant.

The TED effect causes diffusion to be dependent on ramp rate when the ramp rate is sufficiently slow. This was studied for the 500 eV B implant by using spike anneals with a range of ramp-up rates from 50 to 400 °C/s, and the same cooling rate of approximately 100 °C/s. The arc lamp heating method was used to produce sharply peak spikes for each anneal. Cooling occurs by free wafer radiation absorbed by the chamber. To compensate for the decrease in the effective time near the peak temperature with increasing ramp-up rate, the peak temperature was adjusted to yield a constant value of sheet resistance, $R_s = 550 \text{ } \Omega/\text{Sq}$. The results for X_j determined from SIMS profiles are shown in Fig. 9. The data show that the diffusion depth is nearly independent of ramp rate in the range of 100 to 400 °C/s. However, the diffusion depth is 12% deeper for the 50 °C/s ramp rate. One concludes from these observations that that ramp rate higher than 50 °C/s should be sufficient to suppress TED for this shallow B implant.

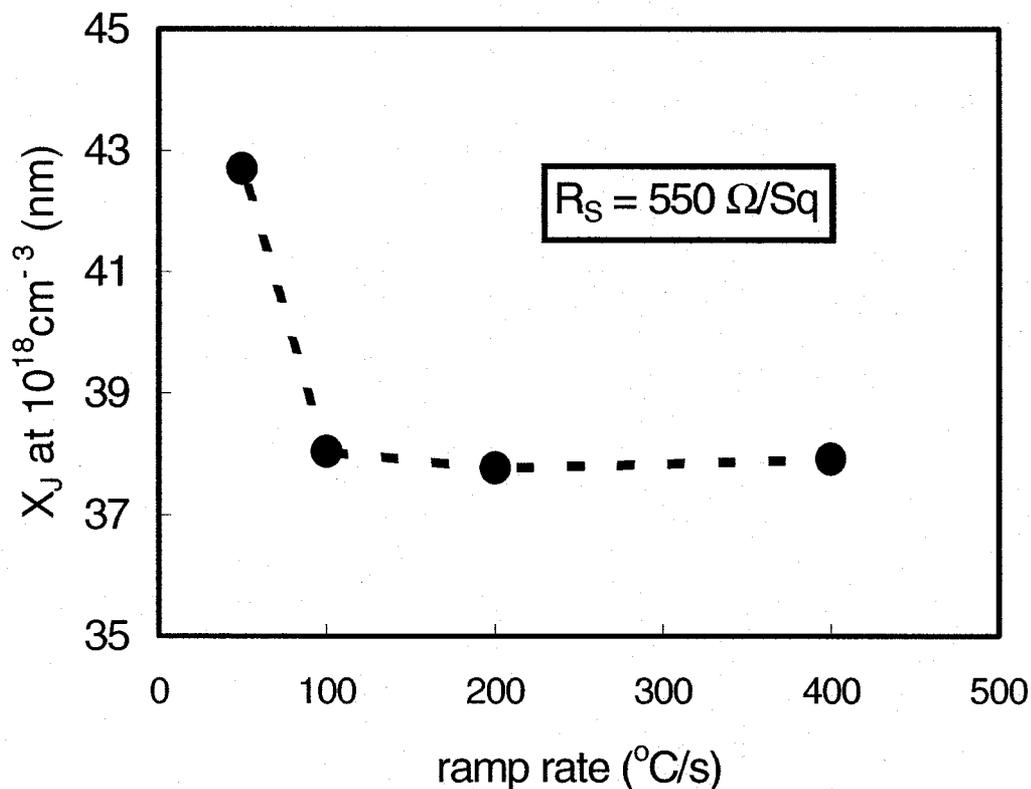


FIG. 9. Junction depths from SIMS analysis for a 500 eV, 10^{15} cm^{-2} B implant spike annealed at ramp rates of 50, 100, 200, and 400 °C/s. The corresponding peak temperatures are 1041, 1058, 1069, and 1079 °C, respectively, and were adjusted to yield the indicated value of sheet resistance.

IV. Dopants in Polycrystalline Si

Gate structures in CMOS transistors are prepared in most commercial applications by depositing poly-crystalline or amorphous Si films over the gate dielectric and implanting a dopant, B for p-type PMOS and P for n-type NMOS. To prevent doping the crystalline Si channel, the range of the implant is chosen to be substantially within the Si film thickness, particularly when implanting poly-Si, owing to statistical variations in ion channeling. The objectives of thermal treatment are to diffuse the dopant across the thickness of the film and produce a high concentration of hole carriers, especially at the interface with the gate dielectric. The case of PMOS devices with SiO₂ gate dielectrics have a noted problem when B penetrates through the oxide into the Si channel. The unwanted channel doping causes threshold voltage shifts and is observed as a shift in the flat band voltage, V_{FB} , in MOS capacitance measurements.

Figure 10 illustrates the result of implanting B at 5 keV and $5 \times 10^{15} \text{ cm}^{-2}$ dose in 200-nm Si films grown by chemical vapor deposition in either the amorphous or polycrystalline state followed by RTA at 1010 °C for 10 s. Owing to grain boundary enhanced diffusion, the B concentration in the poly-Si material becomes uniform across the film thickness. For the amorphous-Si film, although polycrystalline grains are nucleated and grow during the anneal, there is less grain boundary diffusion and the B concentration profile retains a vestige of the as-implanted peak. The structure in the concentration profile at a depth of 0.2 μm , which is near the gate oxide interface, is caused by the relative sensitivities in SIMS to B in Si vs. SiO₂, as well as a B concentration peak in the poly-Si near the interface and B in the oxide.

The mean diffusivity of B in the poly-Si film can be estimated from diffusion lengths deduced from the SIMS profiles and effective times at anneal temperature. Results obtained for spike and soak anneals are shown for as-deposited amorphous-Si films in Fig. 11. The phenomenological thermal activation energy obtained from the Arrhenius fit is 3.29 eV. This interpretation of course ignores the physical details of the diffusion mechanism, which involves diffusion of B within the grains, between grains and grain boundaries, and within grain boundaries.

Transport of implanted B in amorphous-Si films is also detected by electrical measurements. Figure 12 shows the results of an experiment with a B implanted 10-nm amorphous Si film deposited over a 2.4 nm SiO₂ film thermally grown on a p-type wafer. The average carrier concentration in the bulk of the film was determined from the sheet Hall coefficient and the film thickness. The carrier concentration in the film near the oxide interface was determined from MOS capacitance-voltage (C-V) measurements under depletion bias for the poly-Si gate electrode. The anneals used the spike method at various peak temperatures. While the active carrier concentration in the poly-Si film increases with spike anneal temperature, the concentration at the oxide interface increases more rapidly, owing to dopant diffusion, and appears to reach a plateau maximum. The maximum could indicate saturation in B solubility or it could be due to diminished sensitivity of the C-V method at high carrier concentration in poly-Si.

Boron penetration through the gate oxide is illustrated by the data of Fig. 13, which shows the flat band voltage, V_{FB} , from C-V measurements as a function of the carrier density at the poly-Si / oxide interface. The implicit variable is the anneal time at 1010 °C. The theoretical V_{FB} depends logarithmically on carrier concentration, and is approximately 0.27 V at a carrier

concentration in the poly-Si of 10^{20} cm^{-3} . At low carrier concentrations, which are produced for anneals of 1 s or less, V_{FB} is depressed by Fermi level pinning at grain boundaries in the poly-Si. At high concentrations, which correspond to anneals from 30 to 60 s, B diffusion through the oxide dopes the crystalline Si and leads to large increases in V_{FB} . The diffusivity of B in SiO_2 , determined from the V_{FB} measurements, show an activation energy in the vicinity of 3.8 eV. Spike anneals can be used to activate B implanted poly-Si below the threshold for B penetration for films near 100 nm in thickness, by taking advantage of the rapid grain boundary diffusion mechanism.

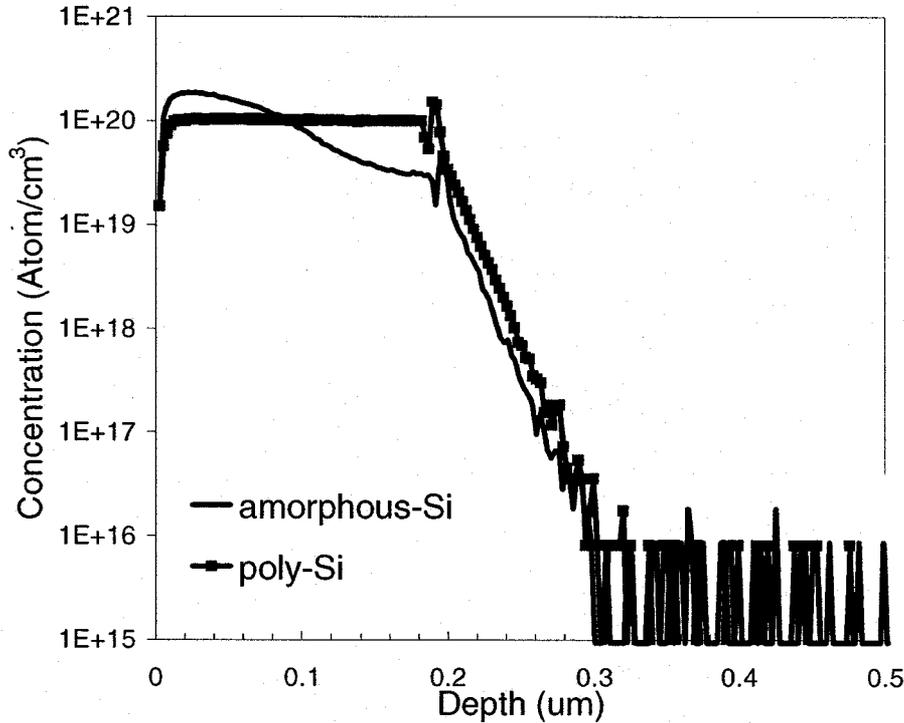


FIG. 10. SIMS measurement of B profiles in 200 nm poly-Si films after 1010°C 10-s anneals. Amorphous or polycrystalline Si is implanted with ^{11}B at 5 keV and $5 \times 10^{15} \text{ cm}^{-2}$. Gate dielectric is 1.7 nm SiO_2 .

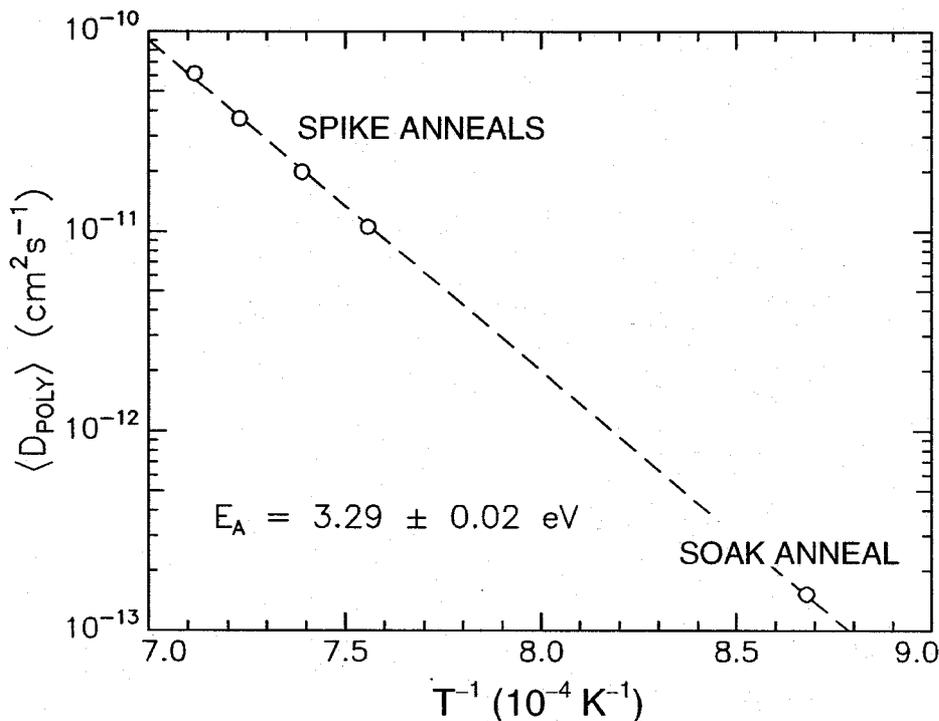


FIG. 11. Mean diffusivity of B in 200 nm polycrystalline Si films, deposited as amorphous Si, implanted with B at 5 keV and $5 \times 10^{15} \text{ cm}^{-2}$ dose, and annealed by spike and soak methods. Arrhenius fit yields the effective activation energy shown.

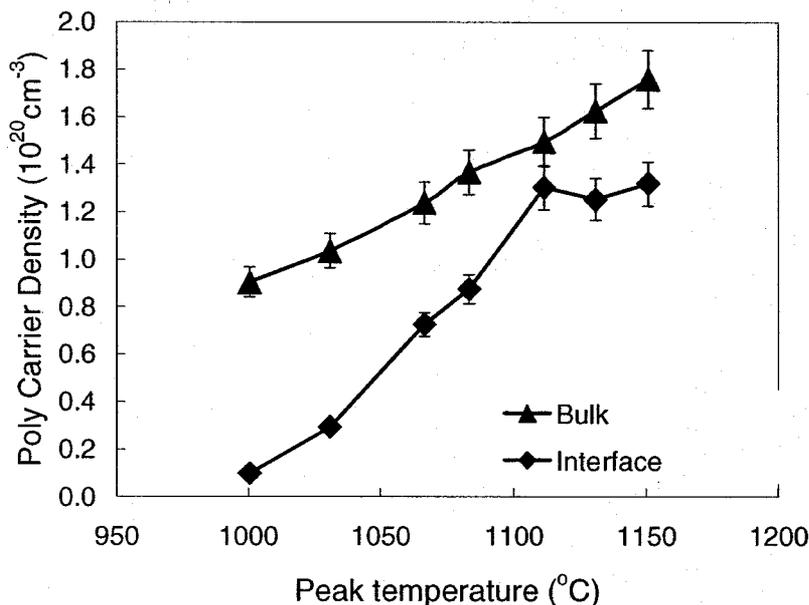


FIG. 12. Hole carrier densities in 100 nm poly-Si films after spike thermal annealing. Bulk density is average over film from Hall effect measurement. Interface density is from poly-depletion capacitance. Films deposited as amorphous Si and implanted with ^{11}B at 5 keV energy and $3 \times 10^{15} \text{ cm}^{-2}$ dose. Gate insulator is 2.4 nm SiO_2 .

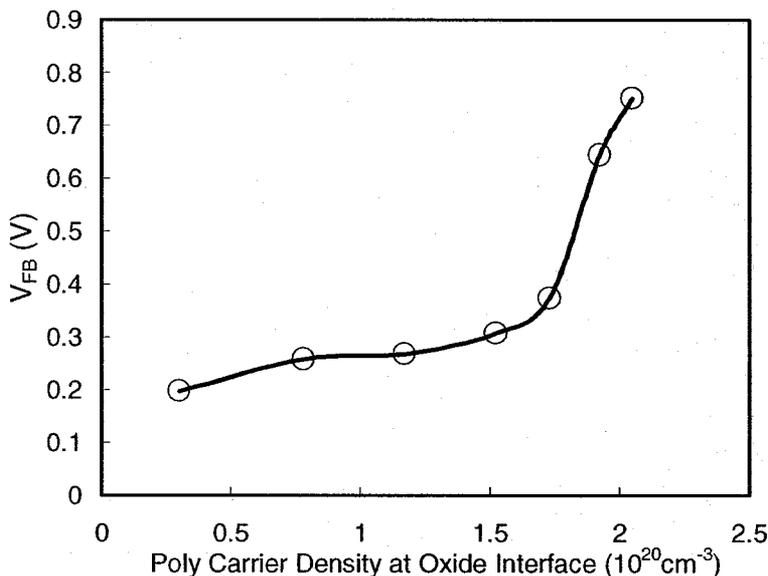


FIG. 13. Flat band voltage in PMOS capacitors with 2.4-nm gate oxide, 100-nm poly-Si gate electrode (deposited as a-Si, 5 keV and $3 \times 10^{15} \text{ cm}^{-2}$ ^{11}B implant) and p-type epitaxial Si wafers. Poly carrier density is derived from poly-depletion capacitance. Results were obtained by varying anneal times from spike to 60 s at 1010 °C. Curve, a guide to the eye, shows an inflection at theoretical work function difference of 0.27 V.

V. Conclusions

Rapid thermal annealing is currently implemented for Si for microelectronics fabrication with either fixed-temperature furnaces or susceptors and wafer movement during heating, or programmable infrared sources in the form of arrays of incandescent lamps or an electric arc lamp. Applications for activating implanted B in junctions and poly-Si gates for p-type MOS have been reviewed. The spike anneal method is shown to help control the effects of B diffusion.

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Rapid Thermal Processing for High Throughput Silicon Solar Cell Production

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RAPID THERMAL PROCESSING AND LOW THERMAL BUDGET PROCESSING

Crystalline silicon solar cell technology includes several steps, where wafers are heated. At least two processes at higher temperatures are mandatory: emitter formation by diffusion and contact formation by firing. Depending on the particular manufacturing process, additional steps like oxidation might add to the time, the wafers go through fairly high temperatures. As high temperatures we define temperatures above 600 °C, since most diffusion and defect (re)formation processes in silicon need at least 600 °C. So below this temperature, the property of most silicon materials is not influenced a lot. Another reason to classify thermal process steps is cost: High temperature steps are more expensive not only because of increased energy consumption, but also because of higher equipment costs. The basic idea of rapid thermal processing (RTP) is to do all high temperature treatments fast. The reduction in process time can be up to two orders of magnitude: from hours to seconds. This not only allows shorter furnaces with the same or even increased throughput (and therefore less floor space is needed), it also increases flexibility of the process and enables a faster response to any change in process results (and therefore improves quality management).

The main difference of RTP to conventional thermal processing is the different photon spectrum. In RTP the energy transfer to the wafer is essentially dominated by high energy photons. In solar cell processes usually the incoherent light of tungsten halogen lamps and sometimes additionally UV light from quicksilver lamps is used. While the temperature of the lamps equals appr. 2500 K the wafer is only heated up to its specific temperature between 600 and 1200 °C. This is usually reached by cooling lamps and reactor walls and leads to the fact, that the wafer is not in thermal equilibrium with its surrounding. This in turn makes it difficult to measure the real wafer temperature. RTP is usually applied in terms of cold wall processing. In this case the temperature of the reactor walls usually does not exceed 250 °C, preventing impurities to ablate during the process [1].

Due to the processing not in thermal equilibrium, heating and cooling of silicon wafers can be done with of up to 200 K/sec. So besides short process times, fast temperature ramps are an important characteristic of RTP. Both factors are crucial with respect to the impact of the thermal treatment to the wafer material. In order to quantify this, the term thermal budget is defined as the integral of process temperature over process time [2]: $\text{thermal budget} = \int T dt$

In conventional processing the thermal budget is rather high: parasitic thermal budget due to long heating and cooling before and after the process, respectively, add to the thermal budget of the process itself. In RTP not only the process time is shorter, due to the fast ramps the thermal budget

is further reduced almost to the product of process temperature and time, even though the temperature is normally a little higher than in conventional processes.

A priori it is not clear which thermal budget is best with respect to solar cell efficiency, since impurity formation and diffusion compete with gettering and annealing. Moreover, thermal budget as a value is not everything: The temperature profile, i.e. the speed of temperature ramping (up and down) and the process temperature and time itself - the quality of the thermal budget -, is most important and influences materials a lot (and differently). Nevertheless, low thermal budget processing is preferable, since parasitic processes (other than what the heat treatment is meant for), especially during heating or cooling, are reduced. A special parasitic process in high temperature steps is inherently suppressed: contamination. While in conventional processing the thermal equilibrium of wafer and surrounding requires special efforts to reduce contamination from particles ablated from the (hot) furnace walls, this is suppressed in RTP due to cold wall processing.

RTP IN SILICON SOLAR CELL TECHNOLOGY

It has been shown that lab-type silicon solar cells with efficiencies up to 18.4 % and 17.5 %, respectively, on Cz-Si can be produced by applying RTP (Table 1). While the corresponding process time was still 10 minutes for emitter diffusion and oxidation in the first case [3], a record small thermal budget of only 5 s of diffusion at 930 °C and 30 s of oxidation at 950 °C characterizes the latter [4]. On multicrystalline silicon (mc-Si) solar cells with an efficiency of 16.7 % have been reported, where diffusion (RTD) and oxidation (RTO) have been performed in less than 1.5 min [5].

Table 1. Best RTP processed lab-type solar cells on industrial Cz-Si and mc-Si, respectively.

Material	RTD [°C], [sec]	RTO [°C], [sec]	Area [cm ²]	Voc [mV]	Jsc [mA/cm ²]	FF [%]	Eff. [%]	Ref.
Cz-Si	?, 450	900, 150	1				18.4	Doshi [3]
	?, 450	900, 150	1	607	37.5	79.0	18.0	Doshi [3]
	930, 5	950, 30	22	623	35.5	79.2	17.5	Peters [4]
mc-Si	900, 25	900, 60	22	626	33.8	78.8	16.7	Noel [5]

Recently, Rapid Thermal Firing (RTF) of screen printed contacts, i.e. contact firing using RTP, has been demonstrated to allow fill factors above 80 % on 4 cm² [6] and 78 % on 97 cm² [7], respectively. Due to the large number of parameters influencing the results a thorough optimization of the process had to be carried out by means of Design of Experiment methods. The developed process is highly reproducible. The thermal budget amounts to only 10 sec above 600 °C including an only 1 s plateau at peak temperature. It has been shown that a sufficient lateral homogeneity of contact properties can be realized and RTP-specific edge effects can be suppressed [7]. The total process time at the moment is 60 s, but there is still potential for further reduction. It is interesting to note, that not only emitters from a conventional in-line furnace, but also RTP diffused shallow emitters can be contacted by RTF (Table 2).

Table 2. Solar cells processed with Rapid Thermal Firing (RTF).

Diffusion process	Material	Area [cm ²]	Voc [mV]	Jsc [mA/cm ²]	FF [%]	Eff. [%]
conventional, in-line	Cz-Si	97.2	611.3	32.71	77.9	15.6
	mc-Si	97.2	597.8	29.69	77.4	13.7
RTD	Cz-Si	96.0	605.3	30.35	78.2	14.4

So it has been demonstrated, that solar cells with very good performance can be made by rapid thermal processing. All high temperature processes, for diffusion, oxidation, and contact firing, are developed to a stage, where the next step would be the transfer into production.

RTP OF MULTICRYSTALLINE SILICON

The most interesting field of industrial application of RTP is the production of solar cells from multicrystalline silicon. Here, the possible positive effect of fast heat treatments to the material swings the decision whether to use RTP or not.

We have made solar cells from RGS* silicon ribbon material in a simple cell technology for material characterization with and without a pre-gettering step at 920 °C for 2 hours. The cells have been diffused either in a conventional tube furnace at 820 °C for 1 hour, or with RTP at 920 °C for 30 seconds (Table 3). The RGS material strongly improves by gettering: The open-circuit-voltage V_{OC} of conventionally diffused cells increases 19 mV, the short-circuit-current J_{SC} increases 9.3 mA/cm² and the overall efficiency boosts from 5.5 % to 8.1 % (even though the fill factor FF decreases). However, the RTP diffused solar cells without pre-gettering show even higher V_{OC} and outperform the conventionally diffused cells with an efficiency of 8.4 %. Solar cells made with a 2 h long gettering treatment can not catch up with these values. So it looks like defect generation is successfully suppressed in RGS by RTP, while during the gettering heat treatment defects form, which are not completely gettered.

Table 3. Solar cells made from RGS silicon ribbon material with and without pre-gettering treatment, processed with conventional and RTP diffusion, respectively.

Gettering [°C]	Diffusion [°C]	Area [cm ²]	Voc [mV]	Jsc [mA/cm ²]	FF [%]	Eff. [%]
—	CP: 820, 1h	4	483	16,7	68.2	5,5
920, 2 h	CP: 820, 1h	4	502	26,0	62.4	8,1
—	RTP: 920, 30 s	4	523	21,5	74.7	8,4
920, 2 h	RTP: 920, 30 s	4	486	24,3	62.6	7,3

* Ribbon Growth on Substrate

Another material we have investigated so far with regard to RTP effects is EFG⁺ silicon ribbon material. Again, we have made solar cells for material characterization purposes either with conventionally or RTP diffused emitter. To improve material quality, we have additionally performed remote plasma hydrogen passivation (RPHP) and measured the cells before and after passivation, as well as after additional antireflection coating (Table 4). While RPHP increases the efficiency of the solar cells in all cases, it is remarkable that RTP diffused solar cells without RPHP show better performance than conventionally diffused ones with RPHP.

Table 4. Solar cells made from EFG silicon ribbon material, processed with conventional (CFP) and RTP diffusion (RTD), respectively. The cells were measured in different stages: after diffusion and metallization, after additional hydrogen passivation (RPHP), and after additional antireflection coating (ARC).

Diffusion.	Status	Area [cm ²]	Voc [mV]	Jsc [mA/cm ²]	FF [%]	Eff. [%]
CFP		22	499.4	18.0	73.5	6.6
	+ RPHP	22	514.6	18.5	74.7	7.1
	+ RPHP + ARC	22	533.5	28.2	73.9	11.1
<i>best cell</i>	+ RPHP + ARC	22	546.0	29.8	76.3	12.4
RTD		22	530.7	20.7	76.4	8.4
	+ RPHP	22	542.3	21.3	76.9	8.9
	+ RPHP + ARC	22	554.3	30.7	77.0	13.1
<i>best cell</i>	+ RPHP + ARC	22	558.3	31.8	76.4	13.6

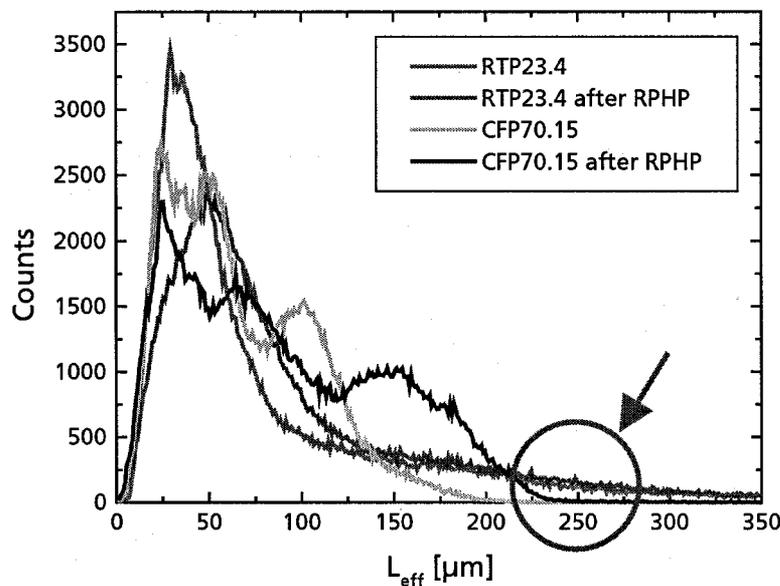


Figure 1. Diffusion length distribution of EFG solar cells processed with conventional (CFP) and RTP diffusion, respectively, before and after hydrogen passivation (RPHP).

⁺ Edge-defined Film-fed Growth

The improvement due to RPHP comes from an improvement of the diffusion length distribution (Figure 1): The number of unit-areas with low diffusion lengths of minority charge carriers decreases in favor of the number of areas with high diffusion lengths. Comparing conventionally and RTP diffused EFG solar cells, very high diffusion lengths do only appear in RTP cells. Again, this is an indication of a suppressed defect formation due to RTP, similar to the results with RGS material.

In an optimized solar cell process emitter diffusion and oxide passivation have been performed by RTP. The Rapid Thermal Oxidation (RTO) at 1000 °C for 30 sec leads to a very good surface passivation. EFG solar cells with additional RPHP treatment and antireflection coating have achieved efficiencies of 14.9 % (Table 5). This not only proofs the potential of RTP on EFG, it also shows, that EFG is suitable for processing at temperatures above 950 °C (which is important in terms of oxide passivation and shorter high temperature treatments at elevated temperature).

Table 5. Solar cells from EFG silicon ribbon material made with optimized process including RTP diffusion (RTD) and oxidation (RTO).

Diffusion	Status	Area [cm ²]	Voc [mV]	Jsc [mA/cm ²]	FF [%]	Eff. [%]
RTD	+ RTO (1000°C, 30 s)	4	552.2	22.0	76.9	9.3
	+ RTO + RPHP + ARC	4	585.7	33.2	76.7	14.9

RTP IN INDUSTRIAL PRODUCTION

The transfer of RTP to industrial solar cell production depends mainly on the development of suitable equipment. In principle, there are two possible routes: (i) Implementation of RTP functionality into in-line conveyor belt furnaces conventionally used in some solar cell fabrication lines or (ii) increasing the throughput of RTP reactors conventionally used for single wafer processing in the semiconductor industry. The first route seems to be straight forward, but implies the availability of a low contamination, low thermal mass transport system and the realization of sufficient temperature homogeneity in an open-tube type of furnace with non-equilibrium heating. The second route implies the feasibility of large-area RTP and a suitable handling system. However, the advantage is the consequent perpetuation of the closed, cold-wall reactor concept assuring fully controlled, "real" RTP.

First prototypes following the first route are build and currently under test [8]. The key feature of these furnaces, besides a cold wall RTP zone, is the transport system made of strings from ceramic fibres (Figure 2) [9]. The transport bases on the walking beam principle: The strings perform a rectangle movement. During the movement in forward direction, the according pair of strings is higher than the pair of strings going backwards. The wafers always sit on the upper pair of strings and are transported in forward direction. The wafers are transferred from one pair of strings to the other by their up and down movement. This system has no revolving parts; the strings always re-

main in the furnace. Contamination from outside the furnace is therefore suppressed. Moreover, the transport system has a very low thermal mass. Fast heating and cooling ramps are therefore possible, in contrast to conventional metal belt systems.

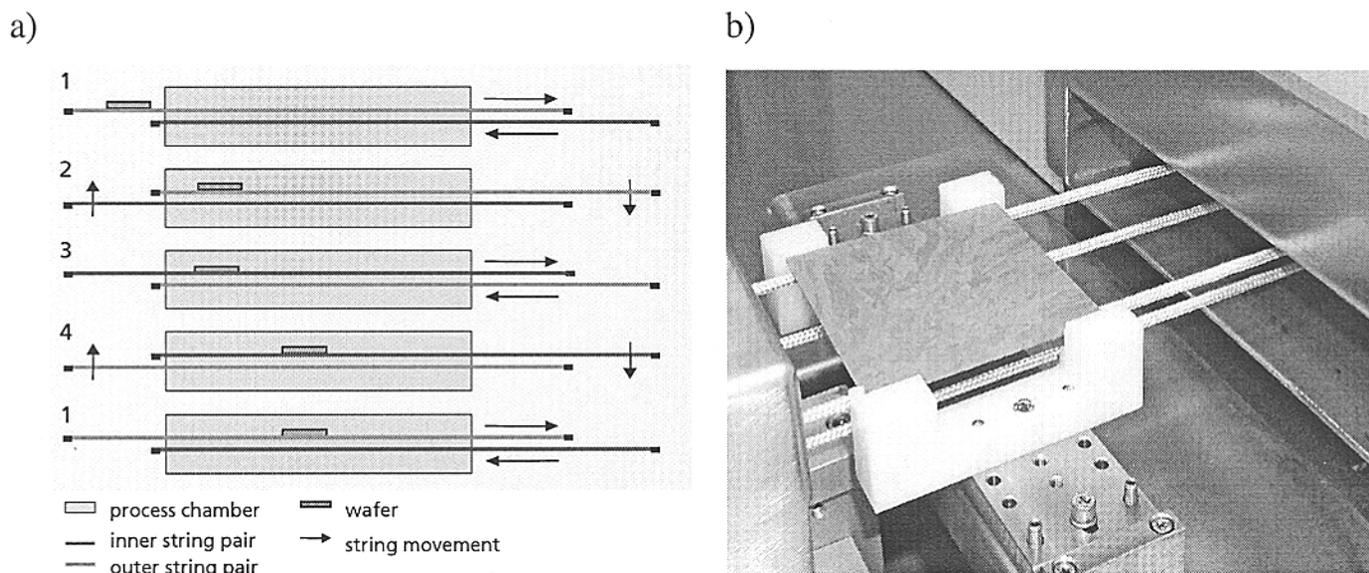


Figure 2. Novel transport system with low thermal mass based on the walking beam principle. a) Schematic diagram of the movement of strings from ceramic fibres. b) Picture of the system.

Another transport system being evaluated is based on the air track principle: Small jets of air form a cushion supporting and transporting the wafers [10]. This system has no moving parts, reduced contamination and minimal thermal mass (if preheated air is used).

Equipped with the walking beam transport system made from ceramic strings first in-line open-tube RTP furnaces have been built. They can be run in quasi-continuous mode and flashing in the cold-wall RTP zone (ensuring temperature ramps over 200 K/s) or in continuous mode (ensuring a throughput of 900 wafer/h, single track). First solar cells diffused in such an in-line RTP furnace within two minutes (60 sec diffusion time) and with contacts fired in an approx. 60 sec RTF step show good performance [8] (Table 6).

Table 6. First solar cells on 1 Ω cm Cz silicon diffused in the novel in-line RTP furnace [8]. (Values are taken in the undegraded state without current mismatch. *Special process with CP133 damage etch, RTO passivation, and TiO₂/MgF ARC.)

Process	Area [cm ²]	Rsh [Ohm/sq.]	Voc [mV]	Jsc [mA/cm ²]	FF [%]	Eff. [%]
<i>evap. contacts</i>						
single wafer RTP	21.2	75-80	627	35.6	79.1	17.6 *
in-line RTP	92	60-80	625	35.0	78.6	17.2
<i>printed contacts</i>						
in-line RTP	23	18-23	603	28.9	75.3	13.1
in-line RTP	23	35-40	609	31.3	75.8	14.4

Besides RTP diffusion, oxidation by RTO is also possible in the in-line RTP furnace. After only two minutes RTO at 1010 °C a 6.86 ± 0.27 nm oxide has been grown on a 4" wafer (Figure 3). This corresponds to a temperature homogeneity of ± 10 K. Even more noticeable is the good surface passivation achieved: Surface recombination velocities S_{eff} of 160 cm/s after 2 min RTO at 1010 °C and even down to $S_{\text{eff}} = 30$ cm/s after 2 min RTO at 950 °C have been measured after an annealing at 400 °C in N_2/H_2 for 45 min.

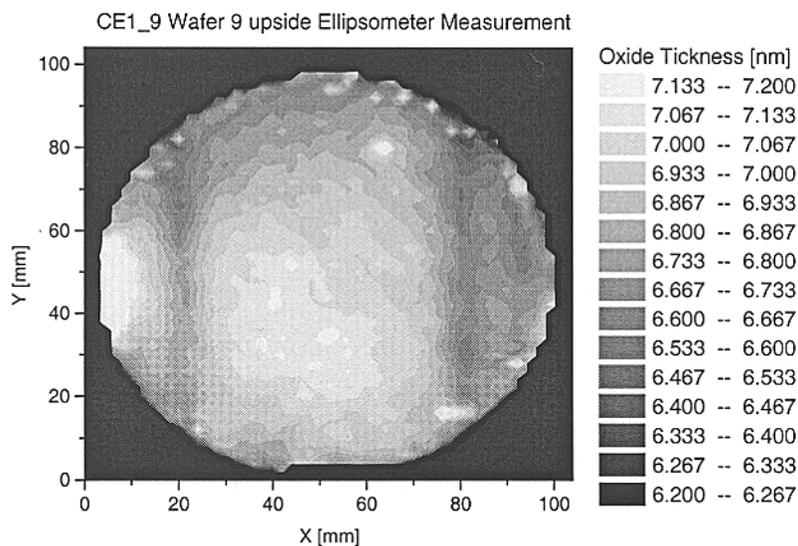


Figure 3. Ellipsometry mapping of a 4" wafer after 2 min RTO in the in-line RTP furnace.

CONCLUSIONS

There are several benefits in the use of Rapid Thermal Processing (RTP) in industrial production: (i) Rapid processing means high throughput with less equipment, which reduces the cost. (ii) Rapid thermal processing also means low thermal budget, which is good for the conversion efficiency of at least some silicon materials, e.g. RGS and EFG, and therefore reduces the cost per W_p . (iii) In addition, RTP equipment needs less floor space and is expected to need shorter maintenance time (cooling down and heating up times are reduced dramatically), which again reduces costs. (iv) Due to the low thermal masses involved in RTP, processes are more flexible and a fast response to (intentional or unintentional) changes in the preceding process steps is possible. The RTP technology may therefore further reduce the cost of PV power.

All high temperature processes necessary in solar cell production, i.e. diffusion, oxidation, and contact firing, can be substituted by corresponding processes based on the RTP technology. It has been demonstrated, that solar cells with very good performance can be made by RTP and the next step, the transfer into production, is under way.

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Monitoring physical parameters of Si solar cells in PV manufacturing

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INTRODUCTION

The silicon photovoltaic (Si-PV) industry is expanding very rapidly. Many PV manufacturers are now eager to implement process-monitoring techniques that can be compatible with advanced processing approaches and high throughput. Typically, the PV industry has used material and device characterization techniques developed for the microelectronics industry. These methods are slow and expensive and, in most cases, are not suitable for solar cell manufacturing. Some of the techniques for process control in the Si-PV industry are discussed in previous papers [1,2]. Although the PV industry is updating its equipment for electrical characterization of cells and modules, it continues to use very rudimentary approaches for monitoring physical parameters of solar cells. Such physical parameters include texture quality, AR coating parameters, metallization area and height, and the quality of the back contact. For many process steps, the only monitoring may involve visual examination of a small fraction of wafers. For example, there is little or no evaluation of surface properties related to sawing and texturing of wafers. Likewise, companies that use silicon ribbon have no simple way to monitor physical characteristics of their ribbons. Perhaps the most monitored process steps in solar cell fabrication are the damage etching, metallization, and AR coating. The former two are mostly done by weighing the wafers to determine thicknesses of the wafer removed and the weight of the metallization, while the latter is done by visually observing the color of the AR coated wafer.

The PV industry needs fast methods for characterization of the physical parameters of solar cells to monitor and control wafer/cell production processes. Considering that a typical manufacturing company may process 50,000 to 100,000 wafers a day, the monitoring methods must be rapid to meet the demands of such a high throughput. Furthermore, each measurement must yield meaningful results. For example, because the physical parameters of wafers/cells exhibit strong spatial variations, a meaningful parameter may be “average” values over the entire cell/wafer.

PV REFLECTOMETER—principles and system configuration

Optical reflectometry is well suited for monitoring physical parameters of solar cells. Indeed, reflectance measurements are routinely used for determining texture quality and AR coating thickness in solar cell fabrication. These measurements are made either by a technician (human eye) or by instruments such as spectrometers, ellipsometers, and colorimeters. In the former case these measurements are qualitative, but the measurements can be performed on planar, rough, or textured wafers. In the later case, they are quantitative but require a one-side-polished test wafer

that must be run along side with the production wafers. Quantitative measurements are typically performed on a small area. Because the physical properties of solar cells can be quite non-uniform, a single measurement may not be very meaningful for process control.

Recently we have described a new reflectometer that offers many advantages for a monitoring solar cell fabrication processes [3,4]. The reflectometer is designed to make measurements of the entire wafer/cell, thus enabling it to “average” the parameter values. Figure 1 is a schematic of the PV Reflectometer. It consists of a highly absorbing spherical dome, about 12-18 inches in diameter, with openings at the top and at the bottom. The bottom opening terminates in an optical baffle that houses a platform to support the test wafer. The dome has four sets of diverging lights located on the upper side that illuminate the test wafer. Separate controllers balance the intensities of the lights. The entire system is designed to eliminate all possible

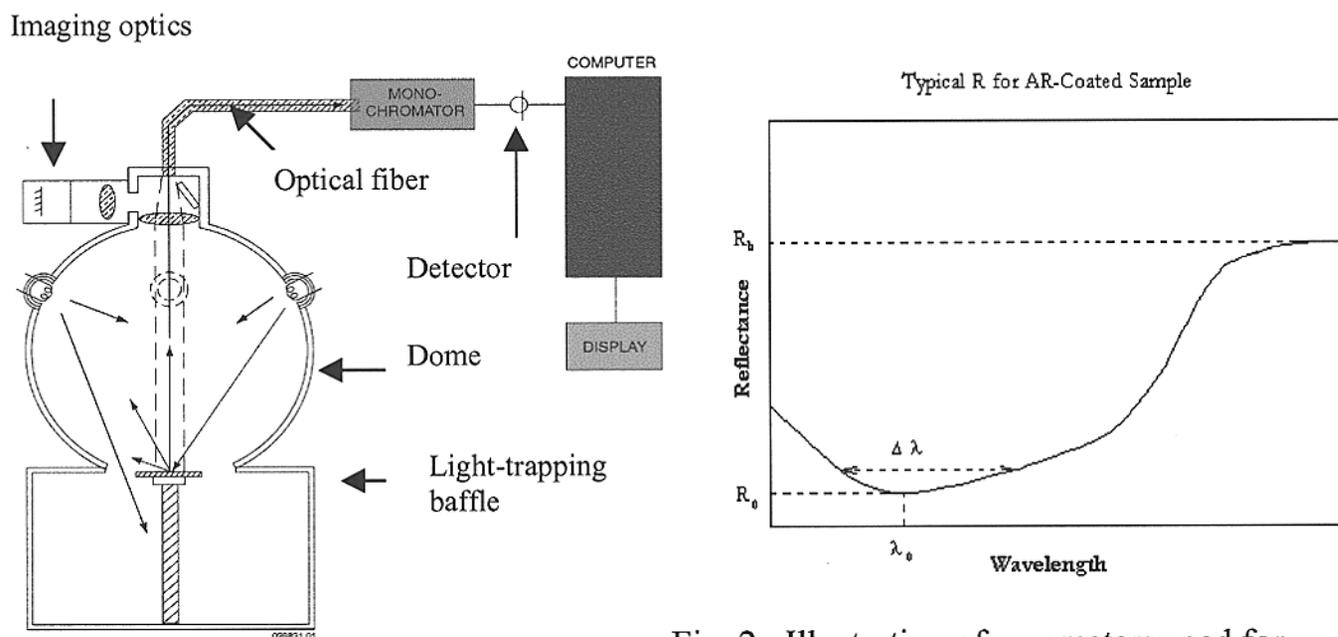


Fig. 1. A schematic of the P -Reflectometer.

scattering of the light except by the test wafer. The top-side of the dome has a lens and an aperture assembly that couples the light reflected from the sample into a monochromator through an optical fiber. The monochromator drive, data taking/handling, calibration, and system control are done by a computer that generates the reflectance (R) vs. wavelength (λ) plot for the test sample. The system operates in a broad spectral range that allows reflections from the front and the back-side of the cell to be monitored. The setup shown in Fig. 1 includes only the illumination source for measurement of the diffuse reflectance for rough or textured wafers/cells. A slightly different illumination source is used for planar cells.

Figure 2 is a sketch of a typical R vs. λ plot of a textured and AR-coated cell with front and back metallizations. Different segments of the curve are used to derive various optical parameters of the cell. This procedure is briefly described below.

- λ_0 (wavelength of minimum reflectance) determines the thickness of the AR coating.

- The value of R_0 —reflectance at λ_0 — is used to determine the parameters related to the metallization. If the reflectance minimum is not a null, the deviation from the zero-value implies that the cell is metallized. By calibrating the system, it is possible to relate this value to the characteristics of the front metallization, the fractional area of the cell covered by the metal and its thickness. In a simple case where the thickness of the metal is very small (as in the case of an evaporated metallization), R_0 is proportional to the fractional area of the front metallization. However, for thick metallization done by screen-printing, R_0 includes contributions from the width as well as the height.

In previous papers we have shown that the reflectometer can accurately measure texture quality, AR coating thickness, and metal area of wafers and wafer based cells. Several improvements in the system have extended its application to ribbon based Si solar cells. The new addition to the reflectometer are: (1) a “specular reflectance” attachment, (2) a high-speed diode array spectrometer, (3) a new design to make the system portable, and (4) calibration procedure for characterizing metallization of different PV manufacturers. Here we will emphasize application of the specular reflectance and issues related to calibration of metal area and height. The specular-source attachment consists of a set of four lights, similar to the diffuse reflectance source, which can illuminate the entire cell at a near-normal incidence. This configuration of lights increases the signal/noise of the specularly-reflected light.

RESULTS AND DISCUSSION

It is fruitful to recapitulate the methodology for characterization of solar cell metallization. The cell is first illuminated by side-to-side light sources and the reflectance R_{ss} Vs λ is measured. Next the cell is illuminated under front-to-back illumination and R_{fb} Vs λ is again measured. From these measurements one can separate contributions to the reflectance due to scattering from the horizontal (R_a) and the vertical parts (R_b) of the metallizations. Figures 3a and 3b illustrate these parameters and the illumination conditions. A theoretical analysis for a most practical, rectangular metallization, can be simplified and approximated to yield values of R_a and R_b in terms of measured reflectance as:

$$R_a = (R_{fb} + R_{ss}) / 2 \dots\dots\dots (1)$$

$$R_b = (R_{fb} - R_{ss}) / 2 \dots\dots\dots (2)$$

A detailed theory of the metallization parameters shows that R_a and R_b depend not only on the width and the height, but also on the surface roughness of the wafer.

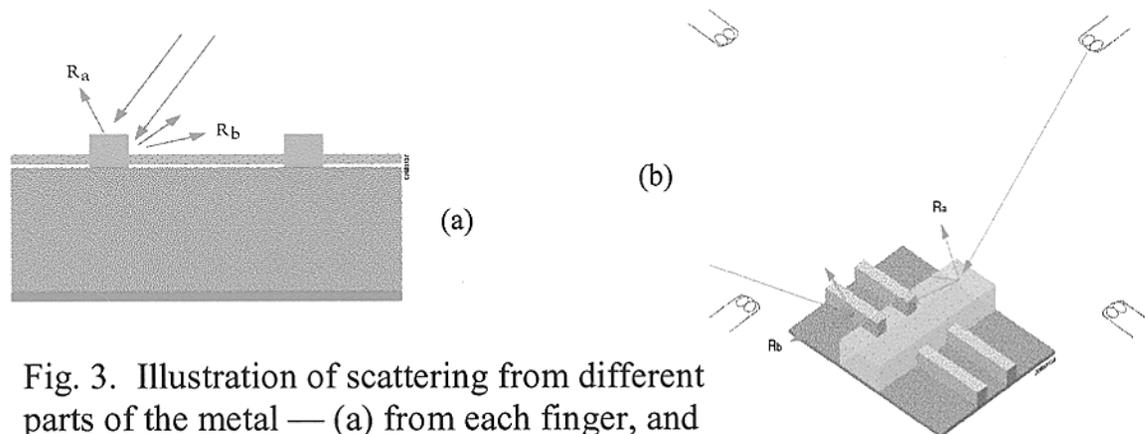


Fig. 3. Illustration of scattering from different parts of the metal — (a) from each finger, and (b) metal pattern

Figure 4 shows a comparison of the specular and diffuse reflectance plots of EBARA solar cell under side-to-side and front-to-back illumination conditions. It is important to point out that the reflectance values are in arbitrary units. These plots show the following features:

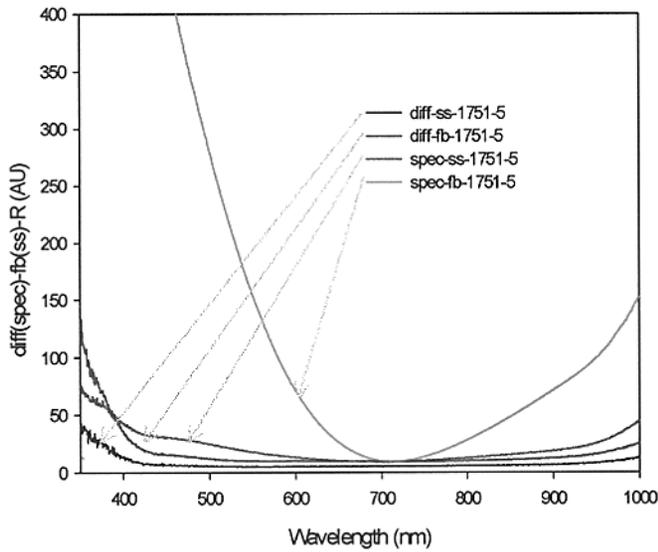


Figure.4. Reflectance plots of an EBARA ribbon cell

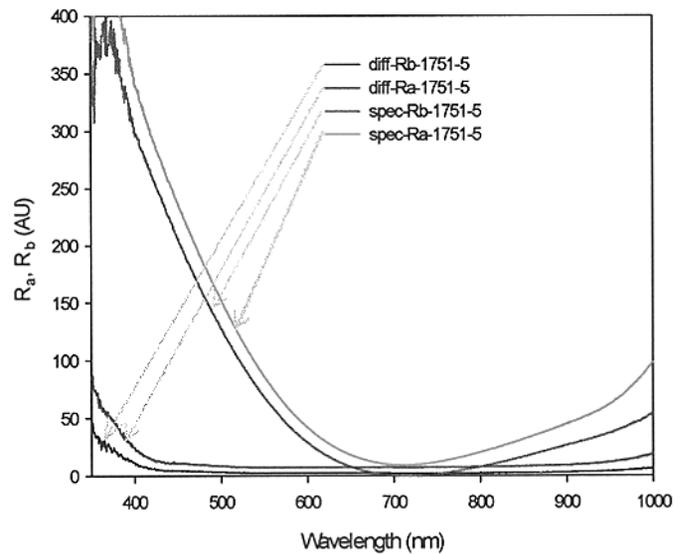


Figure 5. $(R_{fb} + R_{ss})/2$, and $(R_{fb} - R_{ss})/2$ plots corresponding to the reflectance of Figure 4 of EBARA cells.

1. All reflectance plots exhibit a minimum that identifies the thickness of the AR coating. The thickness of SiN AR coating is about 870 Å.
2. Diffuse reflectance (measured by both ss and fb illumination) is considerably lower than the specular reflectance, indicating a planar, smooth surface of the ribbon.

R_a and R_b , described by equations 1 and 2, are calculated from the reflectance plots (these are approximation for simple grid and bus configurations). Figure 5 shows these plots. An important feature of these plots is that R_a and R_b are nearly wavelength-independent in the majority of the wavelength range. The metal area is proportional to R_a and the metal height to R_b . The proportionality constant can be determined by calibration. There are a number of ways to perform calibration. Because the scattering from the metallization pattern depend on the surface quality of the metal, the calibration coefficient may be different for different manufacturers.

One way to perform calibration is to process cells with different metallization parameters. Alternately, one can use production cells and characterize them by a conventional procedure and by the PV reflectometer. Here we describe the results from a later approach. We have measured average areas and the average heights of metallization of cells obtained from different vendors. A Dektak profilometer was used for these measurements. These values were compared with the results with those obtained from PV Reflectometer. Figure 6 and 7 show R_a and R_b against average metal area and metal height obtained from Dektak measurements.

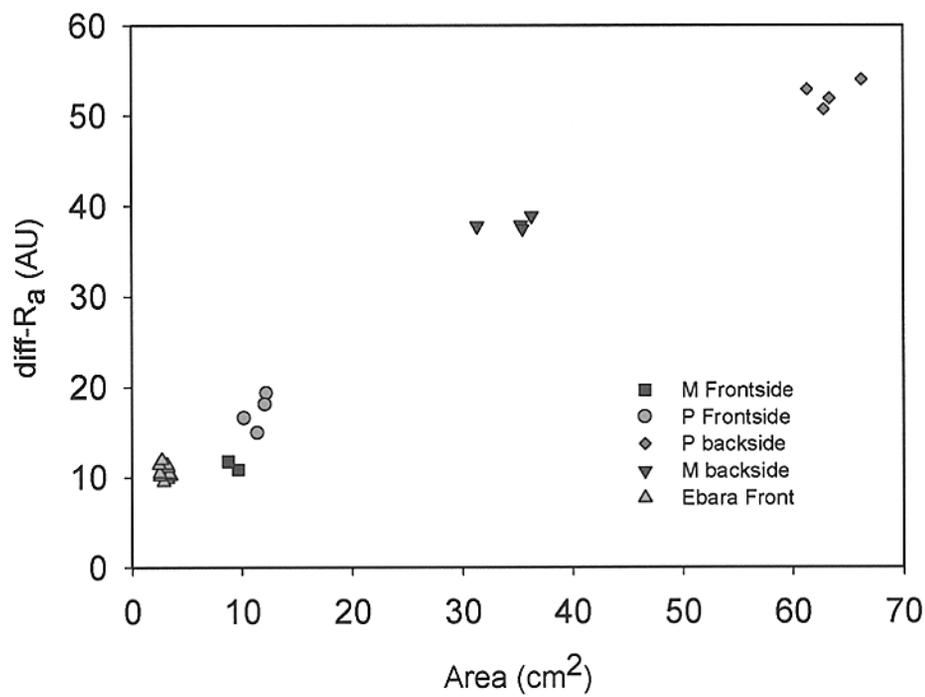


Fig. 6. A comparison of metal area obtained by PV Reflectometer and Dektak, for different solar cells

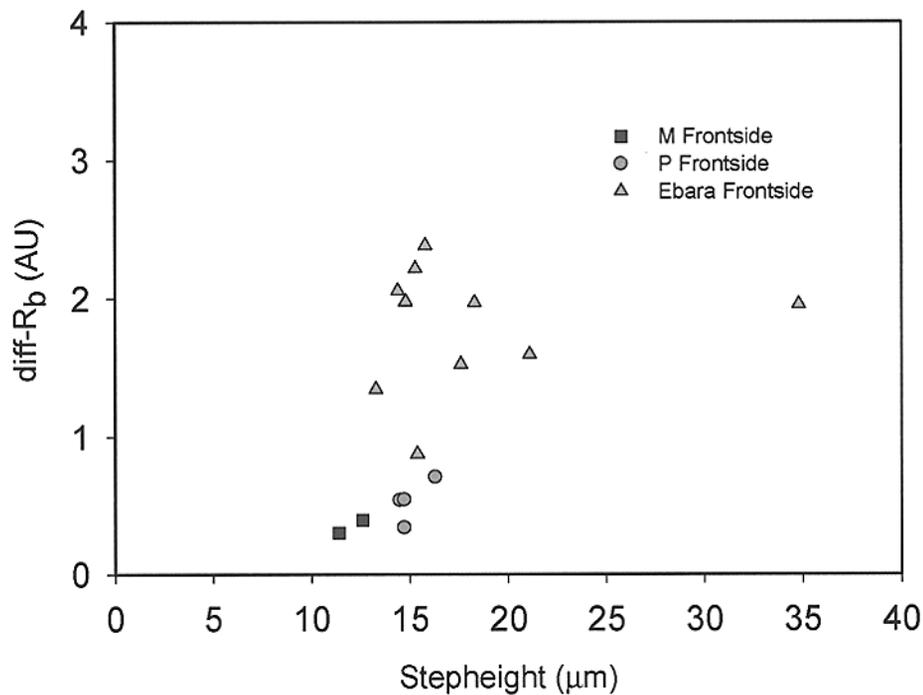


Fig. 7. A comparison of metal height obtained by PV Reflectometer and Dektak, for different solar cells

Figure 5 is a fairly linear relationship between the reflectometer data and the actual metallization area. Deviations from the linearity can primarily be attributed to differences in the surface quality of the metal on each cell. From Figure 6 we see that the reflectometer signal is quite low

until the step height reaches about 10 μm . This leads to a sensitivity of about 5 μm in step height under these measurement conditions. This sensitivity can be greatly enhanced by balancing the light sources and lowering the background scattering.

Figures 7 and 8 provide the calibration for the PV Reflectometer. With this calibration the reflectometer can be used as a tool to quantitatively characterize the metallization. However, for process monitoring in a production facility, it is sufficient to measure R Vs λ with combined ss and fb illumination to determine metal area. To monitor the metal height, one needs two measurements to display $(R_{fb} - R_{ss})/2$. Figure 8 shows R (measured under combined illumination) of ASE Americas ribbon cells that were fabricated to have different metal area. Figure 9 shows $(R_{fb} - R_{ss})/2$ for five EBARA cells indicating a tight distribution of metal height.

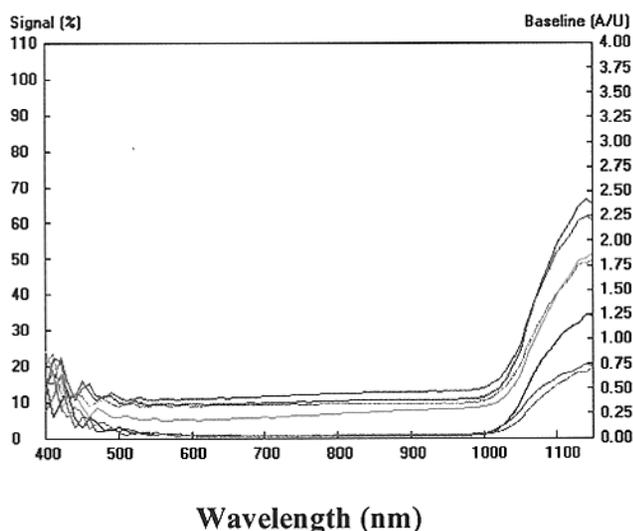


Figure 8. Measured R Vs λ with simultaneous ss and fb illumination for ASE ribbon cells of different metallization area

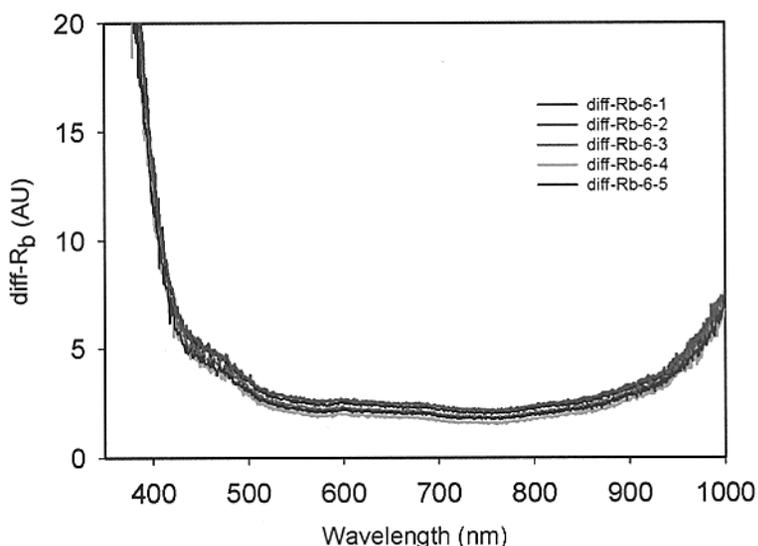


Figure 9. $(R_{fb} - R_{ss})/2$ Vs λ for five EBARA ribbon cells

CONCLUSION

Several improvements in the PV Reflectometer have extended its applications to ribbon cells. There is an excellent correlation between the metallization parameters determined by reflectometer and Dektak measurements. Further design improvements are being incorporated to make the system portable and increase its sensitivity to measure the metal height.

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Cu Metallization in Microelectronics
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Cu damascene interconnect has been identified in the International Technology Roadmap for Semiconductors to be a key enabling technology for developing integrated circuits beyond the current 0.18 micron technology. Since the announcements by IBM and Motorola in September 1997 of Cu damascene interconnect products, the semiconductor industry has focused their efforts in development of the Cu interconnects. In the last two years, the implementation of low k dielectrics to replace Si dioxide introduces a new class of interlevel dielectrics that is thermomechanical weak as compared to Si dioxide. This presents additional technical challenges to the development of Cu metallization. Cu interconnects in the dual damascene configuration have several unique innovations in technology, including the damascene structure, electroplating of Cu, CMP and barrier layers. These enable the Cu metallization to become more cost effective and with better performance as compared with the AlCu metallization. This also gives rise to significant technical challenges in materials, processing and reliability. This presentation will discuss the Cu metallization with oxide and low k dielectrics first from the performance and cost perspective, which will be followed by a comparison of process integration for Cu and AlCu metallization. This will conclude with a discussion on the yield and reliability issues of Cu metallization.

Self-Doping Silver Contacts for Silicon Solar Cells

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ABSTRACT

A contact system for silicon solar cells is described in which silver is coated with a layer of dopant and alloyed with silicon, thereby simultaneously doping the silicon substrate and forming a low-resistance ohmic contact to it. The concept has been demonstrated using evaporated silver with commercially available phosphorus and boron liquid dopants. Silicon surface topography, along with I-V and SIMS analyses all indicate that the Ag-Si eutectic temperature (835°C) must be exceeded and the dopant coating must be present for the contact to be self-doping. The concept has also been implemented in the form of screen-printable silver pastes with phosphorus. A fritless version of the paste exhibited only $3 \text{ m}\Omega\text{-cm}^2$ contact resistance directly to $7 \text{ }\Omega\text{-cm}$ n-type dendritic web silicon. For contacting lightly-doped n^+ layers ($< 100 \text{ }\Omega/\square$) through SiN_x , a fritted version is used. The resultant contact metal is highly conductive ($3 \text{ }\mu\Omega\text{-cm}$) and solderable. No carrier lifetime degradation associated with the alloying process has been observed in dendritic web silicon solar cells.

INTRODUCTION

Most commercial one-sun silicon solar cells employ screen-printed silver contacts. Usually, a silver paste is fired through an anti-reflective (AR) coating, such as TiO_2 or SiN_x , at a modest temperature ($\approx 750^\circ\text{C}$) to contact the underlying silicon. Such contacts can be applied and fired in cost-effective, high-throughput processes with acceptable shadowing losses ($\approx 7\%$). However, in

order to achieve a low series resistance, the surface of the silicon must be heavily doped, with a typical sheet resistance of $\approx 45 \text{ }\Omega/\square$. This heavy doping, which is needed beneath the metal contact, is undesirable between the metal contact fingers because it compromises the blue response and V_{oc} of the cell.

This paper presents an approach for achieving a "selective emitter" (heavy doping beneath metal, light doping beside metal) which requires no extra processing steps and is self-aligning, and in which the dopant required beneath the silver contact is present as an integral component of the silver-dopant system. The dopant is introduced into the silicon via an alloying reaction at a processing temperature above the silver-silicon eutectic temperature of 835°C , in much the same way that aluminum dopant is introduced into silicon via an alloying reaction above the 577°C aluminum-silicon eutectic temperature. In fact, aluminum has been used as a "carrier" to introduce boron into silicon in order to increase the dopant concentration in the p^+ region [1,2]. The approach presented here shares some similarity with alloyed silver contacts reported for sputtered layers of silver-antimony [3] or silver-boron [4], but with a simpler and more practical material system.

The Ag-Si phase diagram in Fig. 1 shows a simple eutectic at 835°C , with 96.9% Ag (weight) and 3.1% Si (weight) eutectic composition. Also shown are the melting points of Ag (961.93°C) and Si (1414°C). From this diagram it can be seen that the eutectic material will have two regions (phases): a major region which is nearly

pure Ag and a minor region which is nearly pure Si.

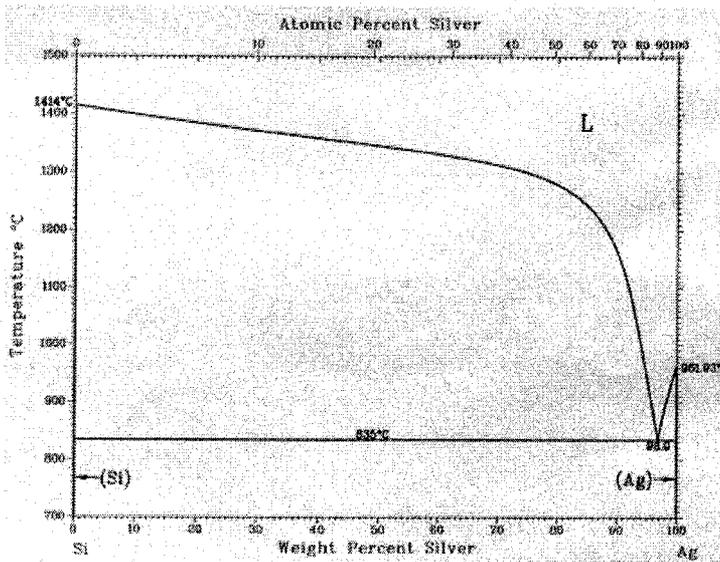


Fig. 1. Ag-Si phase diagram. (R. W. Olesinski and G. J. Abbaschian, 1989)

The phase diagram also gives a way of determining the amount of silicon that a given thickness of silver will dissolve. It thereby provides a means for estimating eutectic layer thickness and n^+ junction depth for the case where Ag is in contact with an n-type substrate and is coated with an n-type dopant. The ratio of thickness of silicon dissolved (t_{Si}) to thickness of silver deposited (t_{Ag}) at an alloying temperature (T) is given by:

$$\frac{(t_{Si})}{(t_{Ag})} = \frac{(\rho_{Ag})}{(\rho_{Si})} * [w_{Si}(T) / (100\% - w_{Si}(T))] \quad (1)$$

where ρ_{Ag} is the density of silver (10.5 g/cm^3), ρ_{Si} is the density of silicon (2.33 g/cm^3), and $w_{Si}(T)$ is the weight percent of silicon at the processing temperature. With $w_{Si}(T = 835^\circ\text{C})$ of 3.1% from the phase diagram, the thickness ratio is calculated from Eq. (1) to be 0.144. Thus, the Ag-Si eutectic layer will be 1.144 as thick as the Ag layer since it includes the original Ag layer.

The depth of the n^+ junction that would be found beneath the Ag region of the eutectic layer depends on the temperature at which the alloying was done, as indicated by Eq. (1). (The n^+ region is that labeled "heavily-doped epitaxial layer" in Fig. 2b.) For example, at 900°C , w_{Si} is 4.0%

(from the left liquidus branch of the phase diagram since excess Si is available for the limited Ag to dissolve) and t_{Si}/t_{Ag} is 0.188 from Eq. (1), while at 1000°C , w_{Si} is 5.8% and t_{Si}/t_{Ag} is 0.278. The depth of the junction beneath the Ag region for a contact alloyed at temperature T is then given by:

$$x_j(T) = \Delta t_{Si}(T) = \{ [t_{Si}/t_{Ag}](T) - [t_{Si}/t_{Ag}](T_{eutectic}) \} * t_{Ag} \quad (2)$$

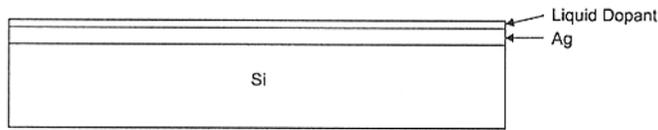
Eq. (2) shows that $x_j(T = 900^\circ\text{C})$ is $0.044 * t_{Ag}$ and $x_j(T = 1000^\circ\text{C})$ is $0.134 * t_{Ag}$. For example, a $10 \mu\text{m}$ thick Ag layer will dissolve $1.88 \mu\text{m}$ of Si at 900°C and create a junction depth of $0.44 \mu\text{m}$ upon epitaxial regrowth, while at 1000°C a $10 \mu\text{m}$ thick Ag layer will dissolve $2.78 \mu\text{m}$ of Si and create a junction depth of $1.34 \mu\text{m}$.

PROOF OF CONCEPT: EVAPORATED SILVER WITH PHOSPHORUS AND BORON LIQUID DOPANTS

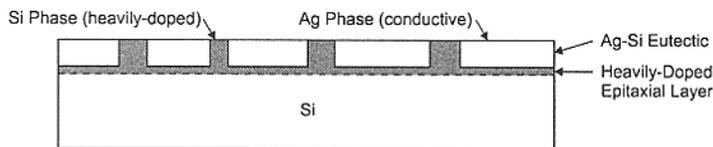
Key elements of the system are illustrated in Fig. 2. Si is contacted by a layer of Ag which, in turn, is coated with a layer containing a dopant. If the temperature of this structure is raised above the Ag-Si eutectic temperature (835°C), Ag can alloy with Si to form a liquid pool containing Ag, Si, and the dopant. While cooling to 835°C , the Si regrows by liquid phase epitaxy and incorporates dopant atoms into the epitaxial Si layer. When the temperature drops below 835°C , the liquid pool solidifies abruptly into two distinct regions, a Si phase which also contains dopant and a Ag phase which is electrically conductive and contains some dopant as well.

Proof of concept was initially made using evaporated silver, coated with a layer of commercially available liquid dopant (phosphorus or boron) [5]. Dendritic web Si substrates, nominally $100 \mu\text{m}$ thick, were used. Alloying was carried out in an RTP unit. An SEM image of the Ag surface after alloying is given in Fig. 3. Two distinct regions are clearly evident, as expected

from the phase diagram and the schematic of the Ag-Si eutectic layer of Fig. 2b. Auger spectroscopy with depth profiling was used to show that the darker regions are Si and the lighter regions are Ag. There is a three-fold symmetry to the patterns of Fig. 3, including some nearly complete equilateral triangles, which reflects the (111) surface orientation of the Si web substrate.



a) Starting structure, showing Ag coated with a layer of liquid dopant.



b) Final structure after alloying, showing heavily-doped Si layer formed by epitaxial regrowth and two-phase eutectic region.

Fig. 2. Key elements of Ag-based self-doping contact system to produce a heavily-doped Si region in intimate contact with a Ag region.

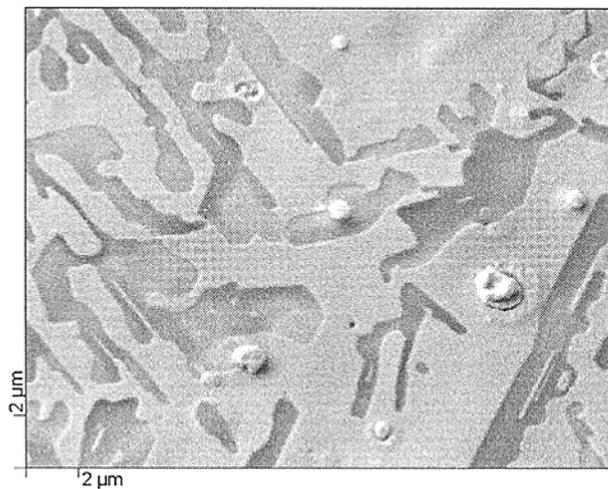
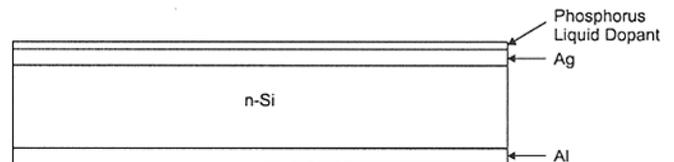
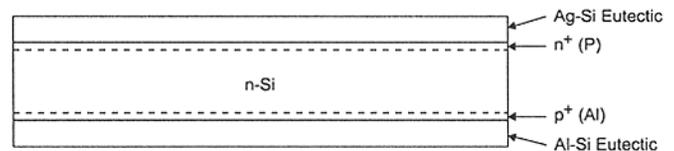


Fig. 3. SEM image of metallized surface after heat treatment above the Ag-Si eutectic temperature in RTP to achieve alloying (Ag not removed). The microstructure of this region reflects the eutectic composition via dark regions (Si phase) and light regions (Ag phase), as determined by Auger spectroscopy. Small particles ($\approx 1 - 2 \mu\text{m}$) of Ag are also present on the surface. Length of image $\approx 23 \mu\text{m}$. (A. Swartzlander, NREL)

The formation of a p-n junction diode in a single high-temperature step is depicted in Fig. 4. Such a diode was fabricated using dendritic web Si doped with Sb to $20 \Omega\text{-cm}$, evaporated Al, and evaporated Ag coated with a P liquid dopant. The resultant I-V curve is given in Fig. 5, indicating good ohmic contact to the $20 \Omega\text{-cm}$ substrate. Upon etching the Ag from the diode, the underlying Si surface exhibits a distinct topography associated with the formation of the Ag-Si eutectic, as indicated in Fig. 6. The light linear features are the Si columns, as shown in Figure 2b. These are raised above the Si floor which had been covered with the Ag portions of the eutectic layer prior to Ag etching. Note that triangular features are evident, again reflecting the (111) Si surface. Probing such a Si surface by SIMS gives the profile for P and Ag of Fig. 7. The measured depth of P ($0.4 \mu\text{m}$) is consistent with calculated values based on the silver-silicon phase diagram, while the measured concentration of P is consistent with a low-resistance contact. Ag is also detected within the Si, but does not seem to interfere with the quality of the contact or the diode.



a) Starting layered structure, with P as the n-type dopant source and Al as the p-type dopant source.



b) Final structure after alloying to produce a Ag/n⁺np⁺/Al device.

Fig. 4. Formation of a p-n junction diode with self-doping contacts using a single high-temperature step.

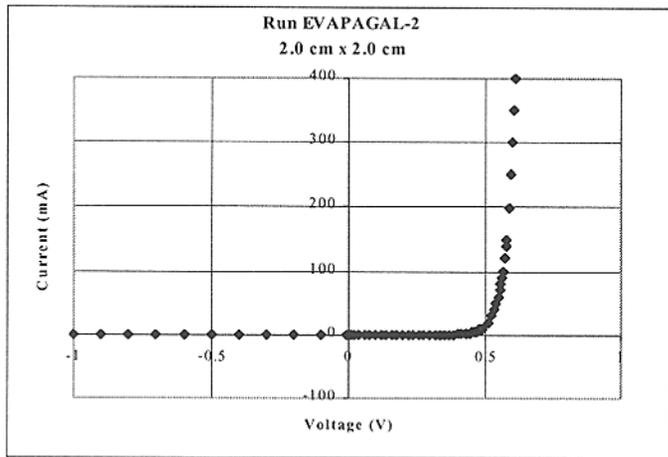


Fig. 5. I-V curve of liquid P dopant/Ag/n-Si/Al structure after heat treatment in RTP above the Ag-Si eutectic temperature. The curve suggests appreciable doping of Si with P, thereby creating a low-resistance ohmic contact to the n-type substrate and a Ag/n⁺np⁺/Al structure.

To illustrate the versatility of the Ag-based self-doping contact system, P liquid dopant was applied to one Ag surface and B liquid dopant was applied to the opposite Ag surface, as indicated in Fig. 8. After RTP alloying the rectifying I-V curve of Fig. 9 was obtained, indicating the formation of a Ag/n⁺np⁺/Ag structure in one high-temperature step. In this case the p-n junction was formed by alloying Ag with Si in the presence of B dopant, while ohmic contacts followed from the creation of the n⁺ and p⁺ layers in intimate contact with the Ag-Si eutectic layer.

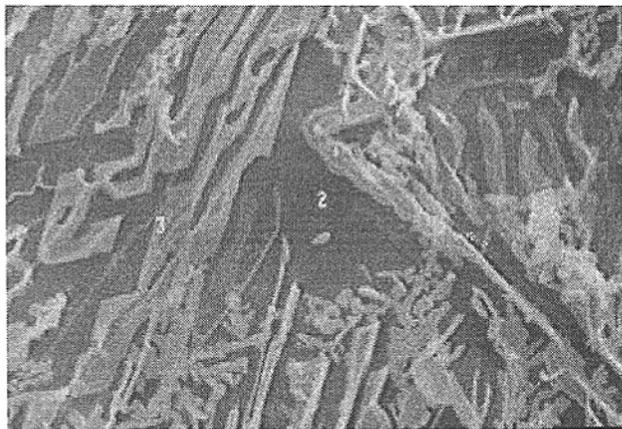


Fig. 6. SEM image of dendritic web Si surface in n⁺np⁺/Al structure after Ag was removed by etching. Note presence of surface features (height ≈ 2 μm), indicating alloying between Ag and Si. Length of image ≈ 110 μm.

SIMS Depth Profile

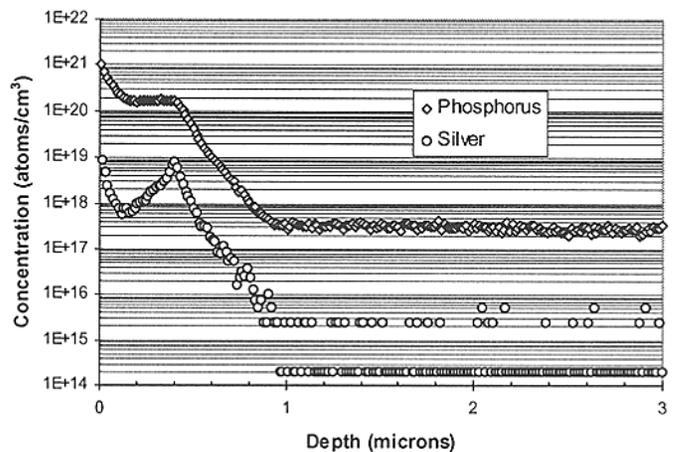


Fig. 7. SIMS P and Ag depth profile after stripping Ag metal from Ag/n⁺np⁺/Al structure alloyed above the Ag-Si eutectic temperature. Data show P at a concentration of at least $2 \times 10^{20} \text{ cm}^{-3}$ to a depth of 0.4 μm and Ag at a maximum concentration of $9 \times 10^{18} \text{ cm}^{-3}$ to a depth of 0.4 μm. P and Ag fall below the SIMS detection limit at a depth of 1 μm. (S. Asher, NREL)

Some Ag/n-Si/Al samples were prepared with no dopant coating on the Ag layers. After RTP heat treatment above the Ag-Si eutectic temperature, I-V curves showed very high series resistance ($> 1 \text{ k}\Omega\text{-cm}^2$). This demonstrates that self-doping action does not occur because of the Ag itself, but only if a dopant coating is applied to the evaporated Ag surface. Other samples, prepared with P dopant coating on the Ag layers, underwent RTP heat treatment below the eutectic temperature. I-V curves again showed very high series resistance, SIMS showed no appreciable incorporation of P into Si, and the Si surface remained unaltered (planar). It appears that the necessary and sufficient conditions for achieving a self-doping contact to Si using evaporated Ag are:

1. The Ag surface must be coated with a dopant source;
2. The processing temperature must exceed the Ag-Si eutectic temperature so that alloying of Ag with Si occurs.

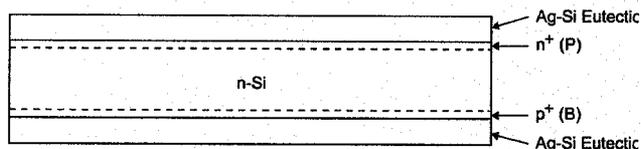
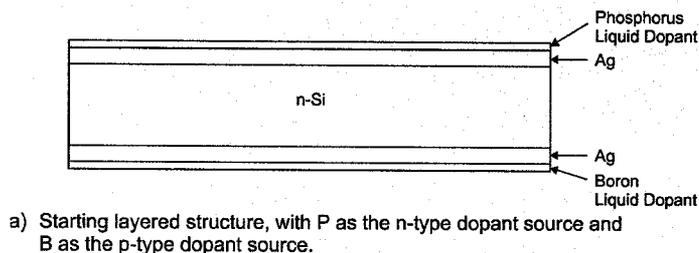


Fig. 8. Formation of a p-n junction diode with Ag-based self-doping contacts using P and B liquid dopants in a single high-temperature step.

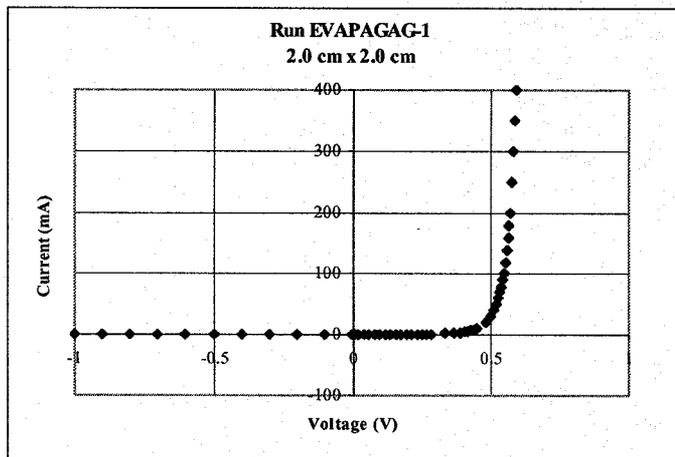


Fig. 9. Diode structure ($Ag/n^+np^+/Ag$) obtained with phosphorus liquid dopant on one Ag surface and boron liquid dopant on the other Ag surface, processed above the Ag-Si eutectic temperature in an RTP. This result illustrates the versatility of the Ag-based self-doping system in providing both n-type and p-type dopants.

TRANSLATION TO FRITLESS SILVER PASTE

The self-doping alloyed Ag contact system has been implemented in an experimental screen-printing paste by DuPont Microcircuit Materials. This fritless paste is designated by DuPont as PV167, and contains Ag particles with integral P dopant.

Work with the PV167 paste confirmed its ability to serve as a self-doping contact material. A fully metallized $Ag/n^+np^+/Al$ diode was fabricated using dendritic web Si blanks in one high temperature step in an RTP, as in Fig. 4. The source of Al for the diode was a commercial Al paste and the source of Ag was the PV167 paste. A diode I-V curve, similar to that of Fig. 5, was obtained. The diode exhibited good ohmic contact and very low leakage current as indicated by its high shunt resistance.

The ability to print and alloy patterns using the PV167 Ag paste was also demonstrated. A contact resistance test pattern comprising a series of Ag bars 1 mm wide and 25 mm long was printed on 7 Ω -cm n-web (no diffused layer) and alloyed in an RTP. This gave a measured contact resistance by the current transfer length method (TLM) of 3 $m\Omega$ - cm^2 for the PV167 paste. Upon removing the Ag bars by etching, the underlying web Si surface has the appearance given in Fig. 10. Note the numerous surface features, including some triangles or triangular segments, which indicate alloying with the (111) web Si. It appears that some, but not all, of the Si surface has participated in an alloying reaction. Associated SIMS P depth profiles are given in Fig. 11. Each profile covers an area 50 μm square, with all four profiles taken within a 300 μm square. The variability in the P profiles is consistent with the variability in the pattern of alloyed areas, although all four profiles show adequate P for a good ohmic contact. Apparently the Ag particles in the paste create ohmic links to the Si substrate at many discrete locations. This is somewhat different from the continuous alloying observed for the evaporated Ag sheets, as indicated in Fig. 6.

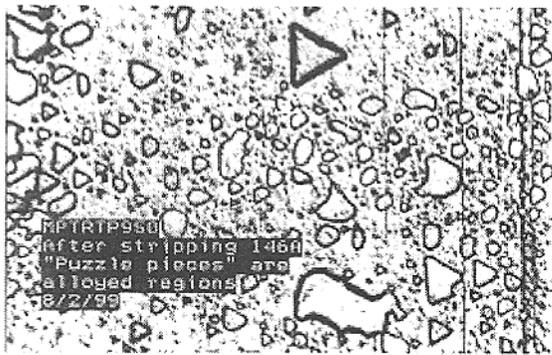


Fig. 10. Optical image of dendritic web Si surface with PV167 Ag stripped after alloying. Length of side of triangle in upper center is 140 μm .

The ability of the PV167 paste to create a self-doping contact was further demonstrated by converting the surface of a p-type ($0.36 \Omega\text{-cm}$) dendritic web Si substrate to n-type upon alloying. The creation of an n^+ p junction on a p-type substrate indicates the formation of an n^+ layer beneath the PV167 metal, as desired. This was confirmed by removing the Ag metal and type testing the underlying Si with a hot probe. The sheet resistance was measured to be in the range 4 - 28 Ω/\square . For comparison, a second p-type web blank was printed with another DuPont experimental Ag paste, which is similar to the PV167 paste but without the integral P dopant, and alloyed. Upon stripping the Ag, the underlying Si tested p-type, as expected, since the experimental paste had no source of P.

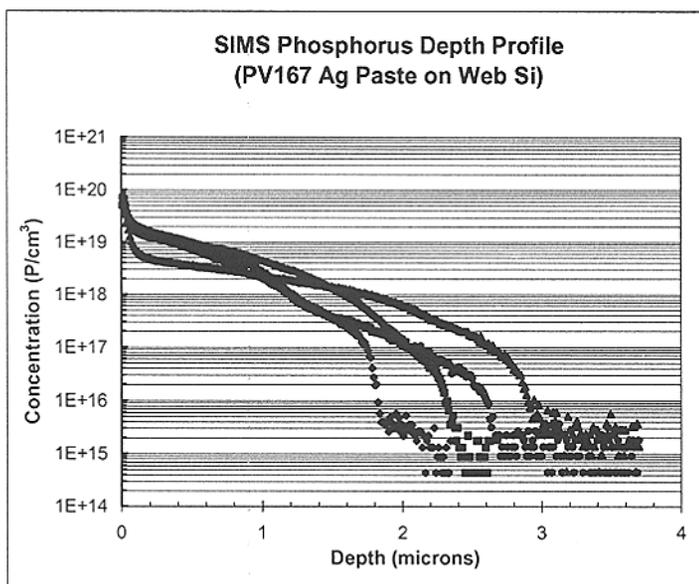


Fig. 11. SIMS P depth profiles in dendritic web Si after alloyed PV167 Ag, applied directly to Si, was removed by etching.

EXTENSION TO SILVER PASTE WITH FRIT

The fritless PV167 paste is useful for cells where Ag contact is made directly to Si, as is the case for an interdigitated back contact (IBC) solar cell [3]. However, in most cases a Ag contact is printed on an AR coating, such as SiN_x , and must fire through that coating to make contact with the underlying Si. For this purpose, a glass frit was added to the PV167 paste and designated DuPont PV168 experimental Ag paste. Such paste has been applied to dendritic web silicon solar cells having an aluminum alloy back p-n junction, known as “PhosTop” cells at EBARA Solar [6]. These cells have a $\text{Ag}/n^+\text{np}^+/\text{Al}$ structure, with a PECVD SiN_x AR coating covering an n^+ phosphorus-diffused layer with sheet resistance up to 100 Ω/\square . The PV168 paste is fired through the SiN_x layer in a belt furnace. The appearance of the Si surface beneath the PV168 Ag is shown in Fig. 12. A SIMS P depth profile for such a surface is given in Fig. 13, with a peak concentration of $3 \times 10^{18} \text{P}/\text{cm}^3$. The true local peak concentration may be somewhat higher if some of the surface within the 50 μm square SIMS analysis area was not alloyed.

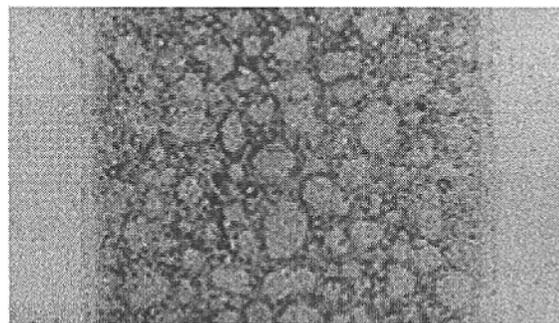


Fig. 12. Optical image of dendritic web Si surface with PV168 Ag stripped after contacting Si through SiN_x . Stripe width is 1000 μm (originally covered by PV168 Ag).

Contact resistance of PV168 Ag fired through SiN_x AR to an underlying n^+ layer is found to be acceptably low for n^+ layers having sheet resistance values up to 100 Ω/\square . An example is shown in Fig. 14, where the measured contact resistance to a 73 Ω/\square n^+ layer is only

0.26 mΩ-cm². Such a value makes a negligible contribution to cell series resistance. As n⁺ sheet resistance values increase toward 100 Ω/□, measured contact resistance tends to rise. A value of 12 mΩ-cm² has been measured with the n⁺ sheet resistance at 93 Ω/□. Even such a value, however, will cause a decrease in FF of less than 0.01 for normal grid patterns.

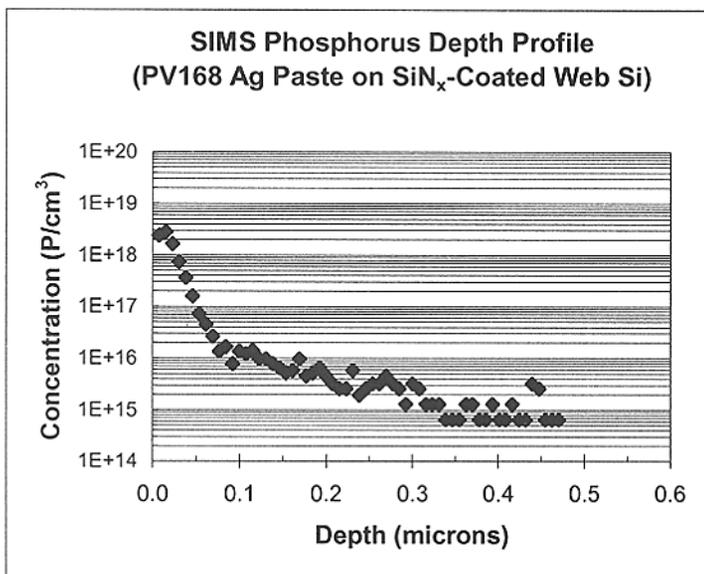


Fig. 13. SIMS P depth profile in dendritic web Si after PV168 Ag, which contacted 9 Ω-cm web Si through SiN_x, was removed by etching.

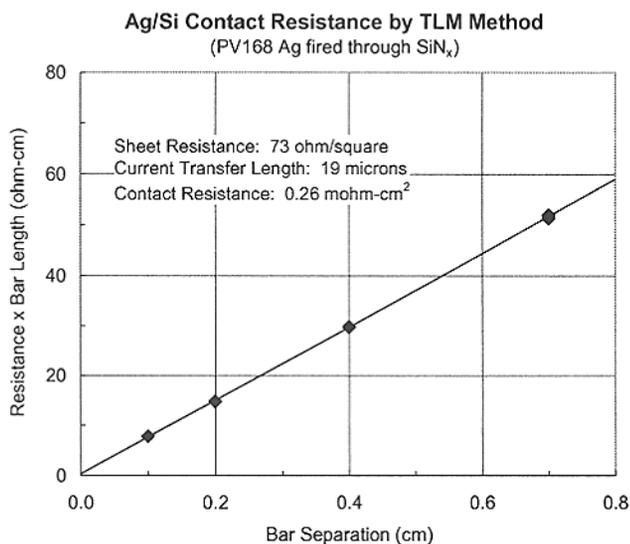


Fig. 14. Plot of TLM data for PV168 Ag contacting a 73 Ω/□ web Si surface through a SiN_x layer to give a contact resistance of 0.26 mΩ-cm².

Contact resistance measurements to date indicate that PV168 Ag, fired through SiN_x AR

coating, is not able by itself to make good ohmic contact to a 9 Ω-cm web Si substrate. Some n⁺ diffused layer to aid in forming the ohmic contact appears to be needed when SiN_x is present. However, the doping in this layer can be relatively light, in that 100 Ω/□ appears to be adequate. This ability to utilize n⁺ layers having relatively high sheet resistance has an important practical implication for dendritic web silicon solar cells as well. No edge parasitic junction removal step is needed, since the parasitic junction does not form at the edges of cell blanks for such lightly-doped diffused layers.

Currently, best results are obtained in the 70-80 Ω/□ range for the n⁺np⁺ back junction web cells with PV168 front Ag contacts. For example, cell 0315-57 had an area of 33 cm² (3.3 cm × 10.0 cm) and was fabricated on a dendritic web Si substrate Sb-doped to a nominal value of 20 Ω-cm with nominal thickness of 100 μm. Measurements at Sandia National Laboratory gave an efficiency of 14.4%, with J_{sc} of 31.5 mA/cm², V_{oc} of 0.607 V, and FF of 0.755. A series resistance of 0.753 Ω-cm² and a shunt resistance of 3.12 kΩ-cm² were determined from the Sandia dark I-V data. Cell fabrication began with a rectangular web blank, and there was no edge junction removal step. The front n⁺ sheet resistance had a target value of 75 Ω/□.

Fig. 15 gives a plot of measured reflectivity (solid triangles), external quantum efficiency (open squares) and internal quantum efficiency (solid squares) for a web cell with PV168 front Ag contacts. The IQE data show a good response at short wavelengths because of the lightly-doped n⁺ layer. The response at longer wavelengths is also noteworthy, since it indicates a minority carrier diffusion length that is several times the silicon thickness. This means that the Ag alloying conditions are consistent with relatively high diffusion length in the finished cell. An improved surface passivation is needed to fully exploit the benefit of PV168 Ag paste, as applied to PhosTop web cells. At 100 Ω/□ the contacts remain good, but J_{sc} and V_{oc} fall off because of the loss of

surface passivation with reduced n^+ doping. Note also that reflectivity loss is appreciable at 12%. Efforts to improve the surface condition and reduce reflectivity are underway.

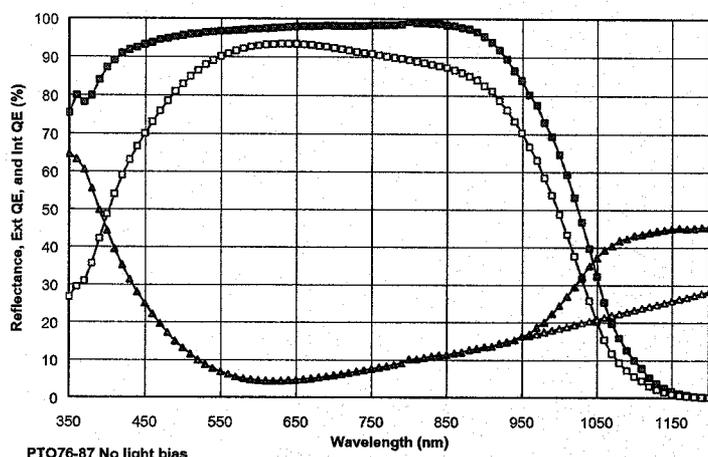


Fig. 15. Reflectivity, EQE, and IQE of web cell with PV168 Ag paste contacting $75 \Omega/\square$ (nominal) n^+ layer through SiN_x in a belt furnace above the Ag-Si eutectic temperature. (D. Ruby, Sandia)

Measured bulk resistivity of the PV168 Ag contact material is quite low at $3 \mu\Omega\text{-cm}$, and the surface is solderable. The production worthiness of dendritic web PhosTop cells having a PV168 front Ag contact was examined. Cells were connected by soldering into strings using an automatic interconnect machine. These strings were then connected in parallel and laminated with a glass superstrate to create an 80 W module. No unusual problems arose in the fabrication of prototype modules from these cells.

CONCLUSIONS

From this work the following conclusions can be drawn:

1. A self-doping Ag contact system for dendritic web Si solar cells can be realized with evaporated Ag, provided the Ag is coated with a dopant source (P or B) and the processing temperature exceeds the Ag-Si eutectic temperature of 835°C ;
2. Such a contact system can be implemented in a fritless screen-printing paste with Ag and integral P (DuPont PV167) which is completely self-doping;

3. Ag paste with integral P and with frit (DuPont PV168) that can fire through SiN_x AR coating in a belt furnace and adequately contact n^+ layers up to $100 \Omega/\square$ is also possible;
4. Minority carrier diffusion length in dendritic web Si "PhosTop" cells remains high (several times the $100 \mu\text{m}$ substrate thickness) through the process which uses fritted Ag paste (DuPont PV168) above the Ag-Si eutectic temperature of 835°C in a belt furnace.

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ACKNOWLEDGMENTS

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Thick Film Conductor Technology for Solar Cells

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Thick film conductor paste materials used for metallizing solar cells are a versatile family of pseudoplastic fluids that can be applied to cells in a number of ways such as screen-printing, pen writing, pad printing, decal transfer, etc. For the majority of crystalline Si cells, the thick film conductor is fired to effect an ohmic contact to the cell and/or to produce a back surface field. The pastes contain various inorganic and organic constituents to achieve the printing and firing objectives. In this paper I will describe the relationship of paste constituents to paste performance objectives.

Thick Film Compositions

Thick film pastes are commonly described in terms of an inorganic solids phase dispersed in an organic vehicle phase. Each paste is designed to optimize both its printing and final (functional) performance for the intended application. The vehicle phase is selected to

- develop appropriate rheology at appropriate rheology,
- achieve desired drying rate, and
- impart green strength if needed (handling and additional printing prior to firing).

Vehicle constituents are polymeric resins, solvents, and dispersing additives.

The solids phase is designed to

- develop appropriate rheology,
- supply the conductive phase (usually Ag, Al, or mixtures),
- make ohmic contact to the Si by firing through barrier layers into the emitter but not through it,
- produce a back surface field to the Si by recrystallizing Al doped Si epitaxial layer,
- form a durable, adhesive bond to the Si, and
- provide a solderable surface for ribbon attachment (Ag or Ag/Al).

The solids phase is composed of silver particles of various sizes and shapes, aluminum particles, glass frit particles of various chemistries and sizes, and other additives.

Screen Printing of Conductor Pastes

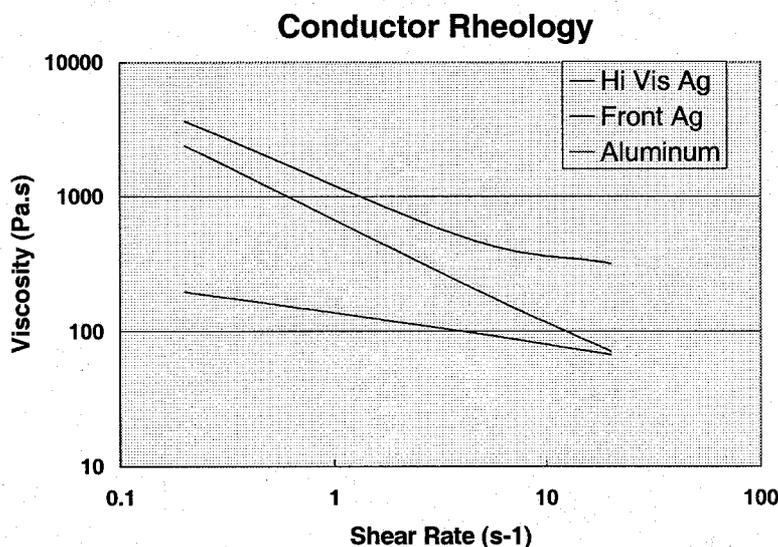
Screen-printing is the patterning method of choice for most thick film pastes, as it provides the lowest cost means to applying thick film conductors. Screen printing can be done quite rapidly and can deposit thick layers vs. other printing methods such as pad printing. The ability to reproducibly deposit the paste increases yields and thereby decreases manufacturing cost. Printing can in some cases be done with screens that have several patterns per screen. This further increases throughput.

Some reasons screen-printing is chosen are:

- High throughput
 - Fast printing
 - High material transfer
 - High paste laydown (print thickness)
 - Multi-up printing (screens with multiple patterns)
- Good yields
 - Repeatable pattern formation
- Low cost per pattern
 - Low equipment cost
 - Low maintenance cost
 - High throughput.

Screen-printing is typically done with pseudoplastic materials. Pseudoplastic rheology (viscosity that decreases with increasing shear rate) enhances material transfer through the screen and enables pattern definition by limiting material spreading. Figure 1 shows the viscosity – shear rate relationship for two silver conductor pastes used in printing fine lines vs. an aluminum paste used for printing a large area.

Figure 1



The pastes' pseudoplastic behavior is derived from both inorganic and organic constituents. The inorganic materials (silver and glassy particles) set up most of the paste's "structure" that is broken apart under the shearing stress. More structure and thereby more pseudoplasticity is formed as solids content increases. High viscosity organic additives such as high molecular weight polymers will also contribute to the rheology but more often as a viscosity modifier – shifting the viscosity curve upward without changing the slope of the curve.

There are many screen printing process variables that determine the quality of the printed pattern. Some of the variables are screen quality (material, wire or thread diameter, tension, emulsion), squeegee quality (shape, hardness, edge condition), printer set up parameters (snap off, pressure, downstop), and printer run parameters (speed, paste dispense onto screen, screen cleaning practice). All variables need to be controlled to obtain high yield fine line patterning.

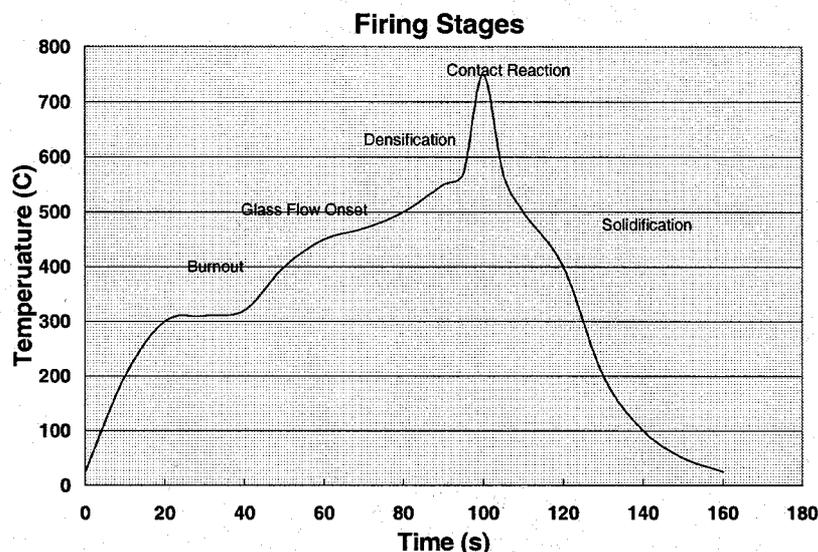
Drying of Conductor Pastes

Thick film pastes need to retain solvent during printing. Excessive solvent loss will lead to inadequate paste transfer manifest as line breaks or variable paste laydown. Periodic addition of fresh paste to a screen that is in continuous use will maintain sufficient solvent in the paste to achieve stable, consistent printing. In the event the process is stopped, some pastes will need to be removed from the screen followed by a cleaning of the screen to remove dried paste from the mesh. Other pastes are designed to remain wet even during such prolonged idle conditions. This eliminates the need to remove paste and clean the screen. The slow drying solvents used in the "more forgiving" pastes have the disadvantage of being difficult to dry in a drying oven.

During drying the solvent is intentionally removed from the printed thick film. Pastes that are designed for maximum drying rate typically contain fairly fast drying solvents and have low vehicle content (relatively high solids). Effective removal of solvent is necessary to obtain adequate green strength. There is a drying process window defined on the low energy end by need to remove solvent and on the high end by the need to leave the resin in the paste. Loss of resin will potentially foul the dryer exhaust and also lead to lower green strength.

During firing the conductor paste experiences a series of transformations (see Figure 2) enroute to the final state. The first transition is vehicle (organic binder) burnout at 250 to 350C. The printed paste is transformed into a film consisting of loosely bound solids. The film will not survive any scrubbing or scratching in this state. Typically this is a very short phase in the "life" of the film, as the film reaches the glass transition temperature within seconds after burnout is completed.

Figure 2



The second transition is glass transition and softening. The glass powders in the film begin to flow upon softening above 400C and wet the conductive (silver) particles and the substrate (Si or coated Si). The glass liquid phase assists the sintering of silver particles, interacts with the substrate to effect ohmic contact to the n+ layer, and solidifies to form a glass bond to the substrate.

The third transition is the densification of the silver by liquid assisted sintering. The film will partially densify above 500C under solar cell firing conditions. The degree of densification will be affected by the surface energy of the silver particles, silver diffusivity in the glass frit, and by the thermal energy of the firing cycle. As the silver microstructure is maturing, the paste is concurrently interacting with the substrate. The interaction can be thought of as a high temperature form of etching of barrier layers that enables silver to contact n+ Si. Firing conditions are set and paste compositions are developed to optimize the interaction and produce the right balance of low contact resistance and high shunt resistance. These conditions and compositions will vary with different cell designs (coated vs. uncoated; emitter thickness).

The fourth transition is solidification of the soft glass to form the adhesive bond to the substrate. In the case of aluminum paste the Al-Si eutectic solidifies by epitaxial regrowth of p+ Si and Al. In this transition, the wafer is put under stress due to mismatch of thermal expansion between the Si and the thick films. The stress will increase as the expansion mismatch increases and as the film thickness increases. Some highly stable interfacial layers inhibit the Al-Si interaction and thereby degrade Al layer adhesion.

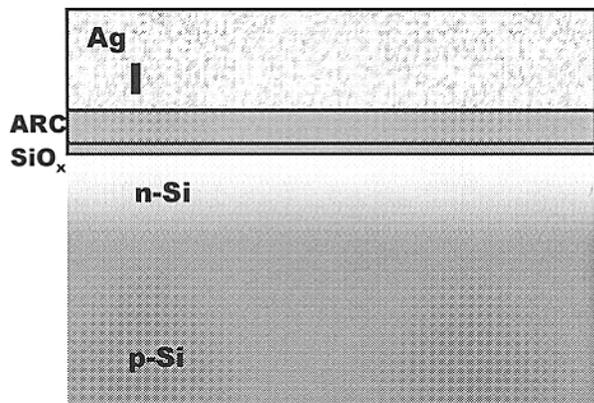
Functional Performance of Conductor Pastes

Electrical Contact

Conductive silver pastes printed on the illuminated surface are designed to make low resistance contact to the emitter after penetrating various barrier layers.

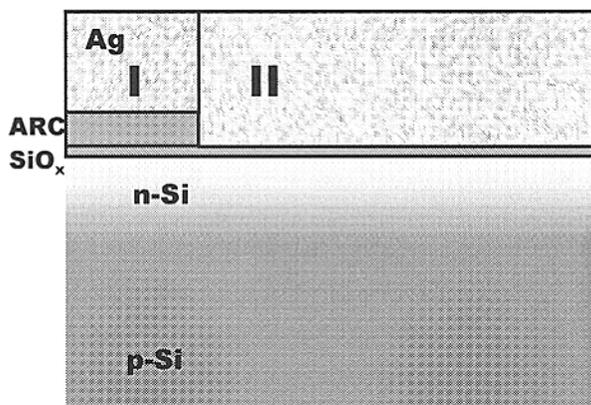
Figures 3 through 6 show the stages of silver paste interaction with a coated Si solar cell.¹ The ideal state is achieved in Stage III in which paste has penetrated the coatings but has not shunted the cell. This becomes more of a challenge as emitter thickness decreases.

Figure 3 Stage I : No contact of Ag with Si



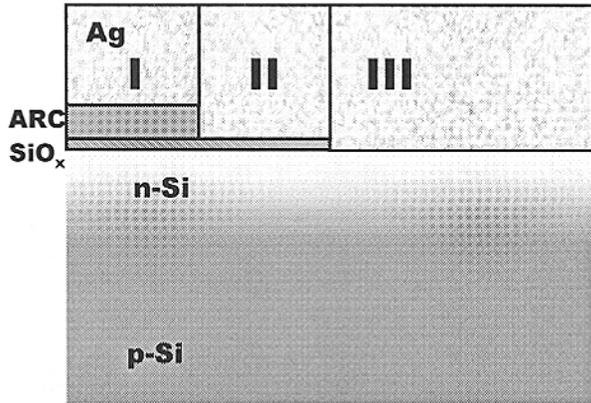
In stage I the silver is underfired or is insufficiently reactive with the barriers. No contact is made to the Si.

Figure 4 Stage II : Partial dissolution of ARC but no penetration through native SiOx layer – poor or no contact



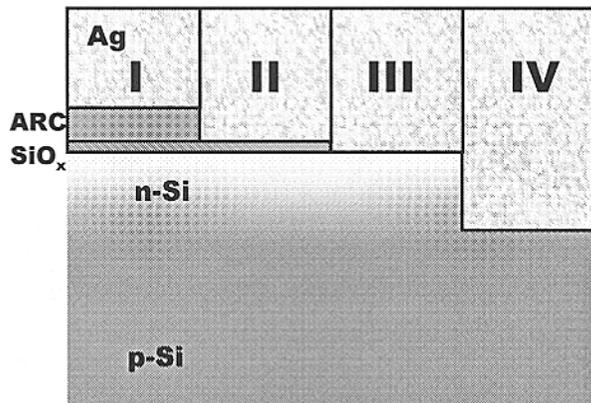
In stage II the silver is still underfired but not so severely. It makes limited area, high resistance contact to the Si.

Figure 5 Stage III : Penetration of ARC enables contact between Ag and Si



In Stage III the silver has made extensive area contact to the Si and has achieved minimum contact resistance.

Figure 6 Stage IV : Etching of the Si by the inorganic constituents, contact resistance increases, junction degradation



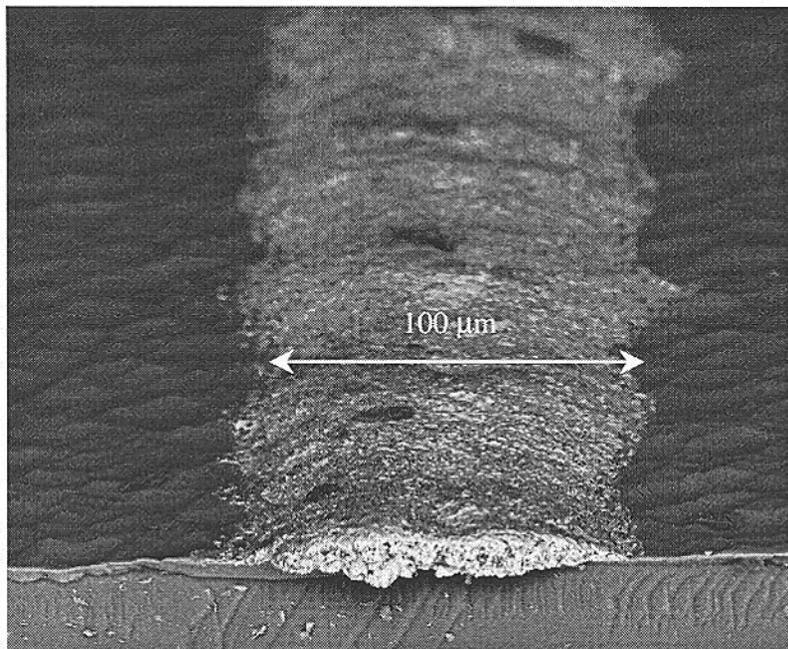
In Stage IV the silver is overfired or over reactive and has etched the Si emitter thereby damaging the emitter or shunting the cell. A managed reactivity silver paste system has been developed to achieve optimal matching of silver to cell design and firing process.²

Aluminum pastes also interact with p type Si to form an Al doped Si layer that makes a built in field at the back of the cell.

Fine Line Printing

Silver pastes are printed to a narrow width to minimize shadowing and thick to decrease resistance of the narrow fingers. Figure 7 shows a 100 μm wide silver line.

Figure 7



Soldered Adhesion

Silver pastes accept (are wetted by) solder. Tinned copper ribbon soldered to silver achieve peel strengths in the range 300 to 600 grams at each solder joint. Soldered adhesion is affected by the composition and quantity of glass in the silver. In well-designed pastes, the glass forms the adhesive bond to the Si without flowing onto the silver surface. The paste must do this in the firing window defined by the electrical contact requirements.

Both firing and solder reflow processes influence soldered adhesion. The glass in the pastes must flow in a very short time during typical solar cell firing. Solder reflow must be achieved in a short time to avoid leaching silver. Reflow conditions should be set to avoid thermal shock of the Si.

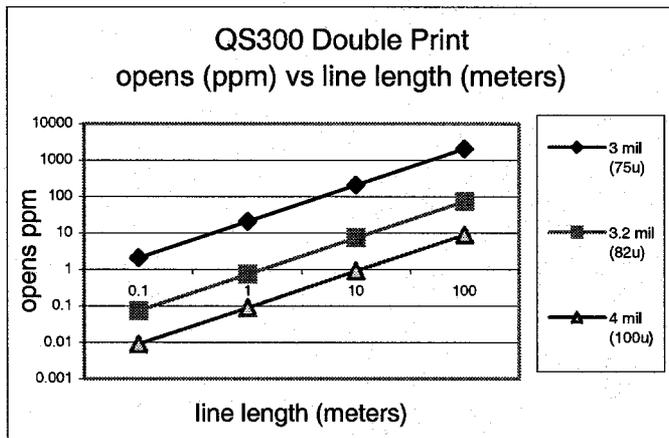
Future Improvements to Conductor Pastes

Conductor pastes are under development to provide optimal contact to Si₃N₄ coated Si. Improvements in front contact compositions are expected to push fill factors up to the high 70% range (e.g. 78%).

Printing process improvements coupled with special paste compositions can achieve standard screen print linewidths of 75 μm at high production yields (see Figure 8).

Double printing of the fingers will decrease line resistance (increase aspect ratio) and improve line continuity.³ This process is currently in mass production.

Figure 8



¹ Advances in Front Side Thick Film Metallisations for Silicon Solar Cells, Richard J.S. Young, Alan F. Carroll 16th EPVSEC, Glasgow, 2000

² DuPont Solamet Photovoltaic Materials System

³ Next Generation Ceramic Multilayer Systems, R. Bacher, Y.L. Wang, M.A. Skurski, J.C. Crumpton, K.M. Nair,

Thick Film Solutions for High Efficiency, Low Cost Solar Cell Processing

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Abstract:

Reductions in the fabrication and raw material costs of solar modules are critical to the commercial viability of photovoltaic energy. Although, the front and the back contact materials contribute to less than 2 % of the overall cost of solar power, they play a critical role in the possible cost reduction. The front and the back contact materials strongly influence the energy conversion efficiency. Any improvement in the conversion efficiency leads to a proportionate decrease in the cost of the module. Similarly, as the volume of solar cells being manufactured increases, cell line processing efficiency becomes critical. Thick film materials that improve process efficiency or increase throughput lead to a significant decrease in manufacturing costs. This paper presents recent developments in thick film materials which offer, high conversion efficiency on a variety of substrate materials and anti-reflective coatings, and improvements in process throughput.

A solar cell can be modeled as a diode with a parasitic series and shunt resistance. To obtain high Efficiency and Fill Factor, the shunt resistance should be as high as possible and the series resistance should be as low as possible. To obtain a low series resistance, the bulk resistivity of the contacts, the contact resistance and the resistivity of the semiconductor should all be low. Shunt conductivity is a result of the defect formation by impurities near the p-n junction area. Typical thick film materials for front contact formation are mixtures of silver powder, glass, oxides, dopants and a polymeric carrier. The chemistry of the front contact materials is optimized to obtain low contact and bulk resistivity but high shunt resistivity. Our studies show that glass chemistry and dopants play a critical role in achieving these goals. The back contact materials are mixtures of silver or aluminum powder, glass, oxides and a polymeric carrier. A typical aluminum conductor used for BSF formation is fired above its melting point; the inter-diffusion of aluminum and silicon lead to the formation of the p^+ layer. However, the reaction between aluminum and silicon that leads to the formation of a low melting eutectic alloy may result in bead formation. The formation of beads greatly reduces manufacturing throughput because they cause substrate breakage during subsequent handling processes. Through optimization of aluminum powder characteristics and the glass and oxide chemistry, the beading may be eliminated.

There are two or three contact materials used to fabricate a typical solar cell, a front contact silver, a back contact silver aluminum for full grid coverage or as a solderable busbar, and a back contact aluminum for BSF formation. Traditionally each material must be screen printed, dried at 150°C to remove solvents and then fired or co-fired at approximately 800°C. For sequential processing with all three contact materials, up to nine processing steps may be required. Each processing step requires manual or automated movement or handling to the next station, each movement introduces the possibility for substrate breakage. New material systems have been developed that eliminate the drying processes for the thick film materials. The new materials may reduce handling up to 33% and increase manufacturing throughput.

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Introduction

PV demand for reject silicon from the electronics industry is expected to exceed the supply (8,000 metric tons/yr) by a factor of 2 to 4 by the year 2010 [1]. The cost of readily available electronic-grade polycrystalline silicon (EG-Si) is considered to be too high by many Si PV manufacturers. A number of research efforts are underway around the world to explore potentially lower-cost alternatives to the semiconductor-industry Siemens C process for making polycrystalline Si feedstock. However, it may be some time until these new approaches reach market viability. Many of the approaches focus on upgrading or purifying metallurgical-grade silicon (MG-Si). A method under investigation by Crystal Systems (Salem, MA) treats molten MG-Si with a sequence of gaseous and slagging processes to reduce impurities. It has been particularly successful with boron impurity removal [2], although residual levels of phosphorous are higher than desired so far. The success with boron removal, historically considered to be one of the most difficult impurities to remove from silicon because of its low volatility and low segregation coefficient, could open the way to interim utilization of a heretofore unusable segment of the scrap EG-Si supply. This is heavily boron-doped single-crystal, wafer, and epitaxial-wafer reject material. We grew Czochralski (CZ) and float-zone (FZ) crystals using Crystal Systems-treated MG-Si and particularly their treated highly boron-doped p-type EG-Si reject material as the feedstock. Crystal growth observations, characterization of the grown crystals and device performance of wafers from them are presented.

Feedstock Material

Crystal Systems, working under a DOE-NREL PVMaT subcontract, is developing gaseous and slagging melt treatments focused toward an eventual cost-effective process for making solar-grade silicon (SoG-Si) feedstock from MG-Si. In using these treatment sequences on MG-Si, boron levels could be reduced from 20–60 ppma to ~0.3 ppma (1 Ω -cm), but phosphorous and carbon removal remain a problem. Their successful treatment process for boron removal was recently applied to a category of electronics' industry silicon scrap previously unacceptable for PV feedstock use because of its high boron content (50-400 ppma). The available amount of this material is estimated to be equivalent to 100-200 MW/year. The Crystal Systems process can reduce its boron content by several orders of magnitude, to ~1 ppma (0.4 Ω -cm, or about $5 \times 10^{16} \text{ cm}^{-3}$). Batch sizes of 60 to 140 kg have been treated. Although an integrated treatment procedure might process liquid silicon directly as it is tapped from the arc furnace, followed by in situ slow directional solidification of a multicrystalline ingot for wafering into cell blanks, the smaller scale initial experiments considered only the melt treatment step. Solid MG-Si or boron-doped reject EG-Si was loaded into a crucible and melted, treated, and solidified, but the directional solidification was suboptimal for direct ingot use because a dual-use furnace with proper features for both treatment and directional solidification has not yet been implemented. The solidified, treated silicon was core drilled to form rods for FZ feedstock and one-piece crucible charges for CZ feedstock. The shaped pieces were degreased and 3:1:2 mixed-acid etched prior to crystal growth.

Crystal Growth

Float-Zone Growth

FZ growth was carried out on both treated MG-Si and treated scrap EG-Si using RF heating with a stationary one-turn coil in an argon ambient to minimize heater or crucible sources of O, C, and other impurities. The feedstock diameter was about 27 mm, and crystals of this diameter or somewhat larger were grown. The typical growth rate was 3 mm/min with a 13-16 rpm crystal rotation rate and a 2-3 rpm feed rod rotation rate (crystal on the bottom, moving downward). A sequence of photos for FZ growth using one of the treated reject EG-Si feedstock cored rods is shown in Fig. 1. A clean initial melt allowed good seed contact and initiation of dislocation-free (DF) growth. DF growth was maintained for about half the ingot

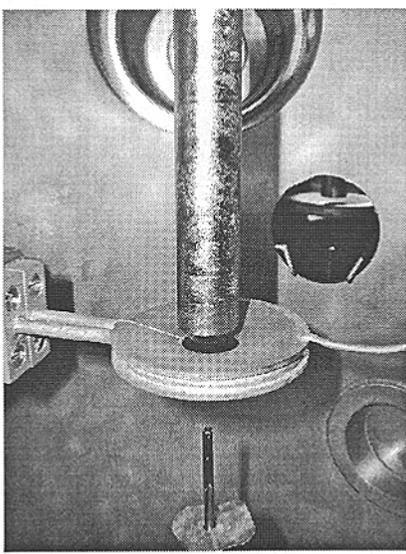


Fig. 1a. FZ Pre-growth setup

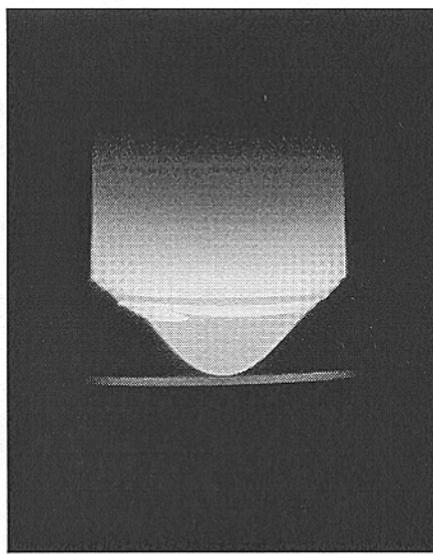


Fig. 1b. Initial FZ melt

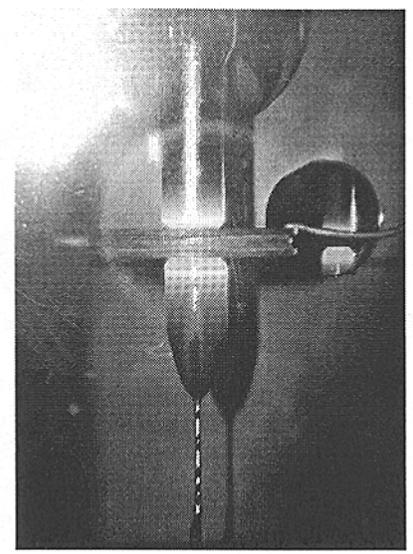


Fig. 1c. Full body $\langle 100 \rangle$ FZ growth

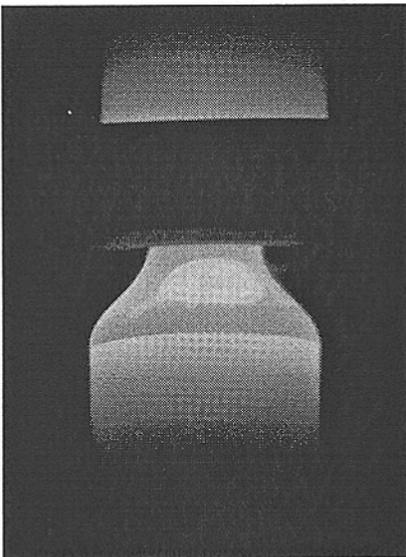


Fig. 1d. Floating particle clumps

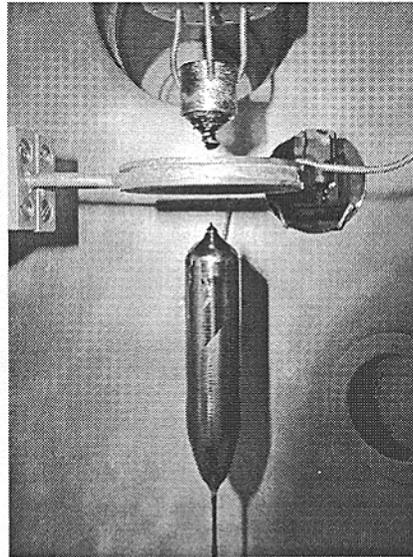


Fig. 1e. Finished FZ crystal

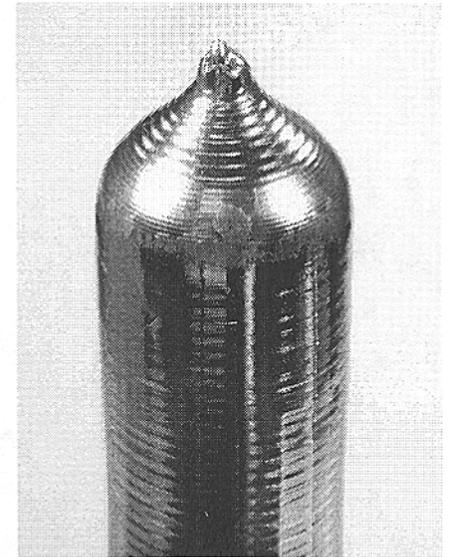


Fig. 1f. Freeze-out particle clumps

length, then twins and eventually grain boundaries formed. Later, floating clumps of particulates could be observed on the melt and these grew in size and froze onto the ingot surface at the tail-end termination of growth. A similar situation was seen with treated MG-Si feedstock, but generally in a more severe form with DF growth terminating earlier and more massive particle clumps on the melt and freeze-out.

Czochralski Growth

Figure 2 shows a sequence of photos similar to Fig. 1, but for CZ growth from treated, high B-content, reject EG-Si material. As for FZ growth, a clean initial melt allows seeding and necking to initiate DF growth. One of three crystals grown from the treated EG-Si feedstock remained dislocation-free through the length of the crystal (Fig. 2e). The other two first initiated twins and later grain boundaries after roughly half of the melt was solidified, and clumps of particles (Fig. 2f) can be seen on the frozen melt residue from these, similar to ones observed in FZ growth. CZ growth was not attempted from treated MG-Si.

Crystal Characterization and Diagnostic PV Device Results

A closer view of a particle clump formed on the surface of a FZ crystal grown from treated MG-Si is shown in the Nomarski photomicrograph of Fig. 3. The hexagonal morphology of the particles is consistent with that of SiC. Investigation of particle surfaces by electron probe micrograph analysis (EPMA) found high levels of C, but not always in a 1:1 atomic ratio with Si. This may be due to the easy wetting of SiC by liquid Si and resultant thin Si residues on the particle surface. Other circumstantial evidence for SiC particle composition is the fact that the crystallographic failure mode associated with the onset of the particles is usually twinning. It is generally agreed that twins can be caused by particles or patches of SiC [3].

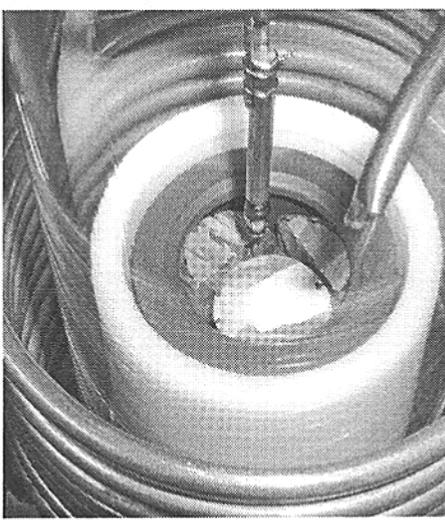


Fig. 2a. CZ pre-growth setup

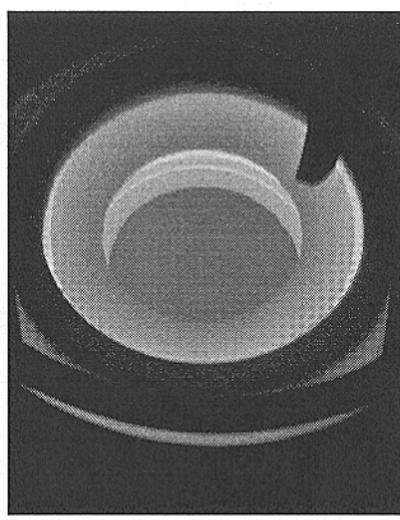


Fig. 2b. Initial CZ melt

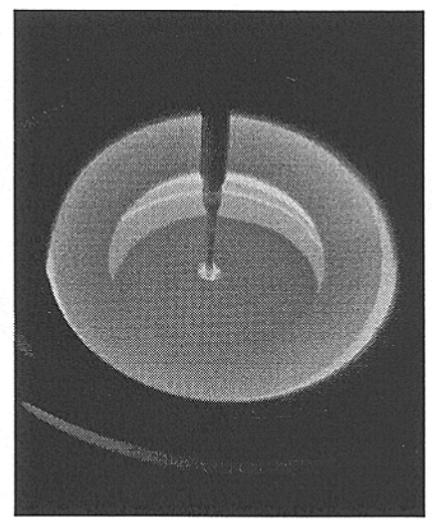


Fig. 2c. CZ neck growth

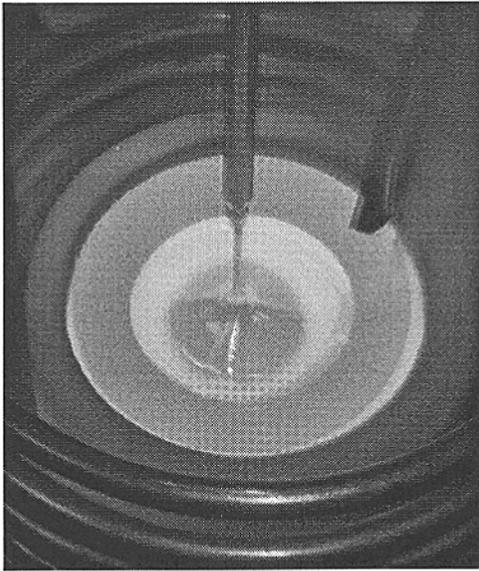


Fig. 2d. Full body CZ growth

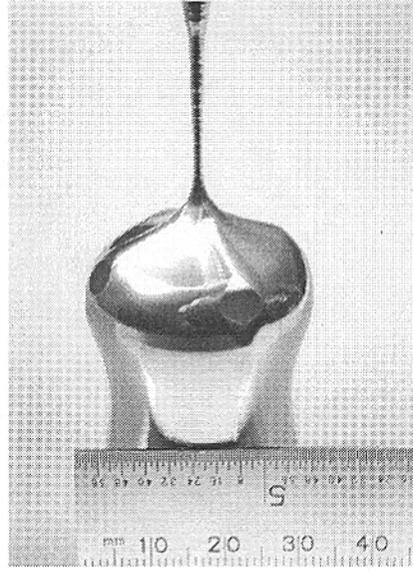


Fig. 2e. Finished <100> CZ crystal

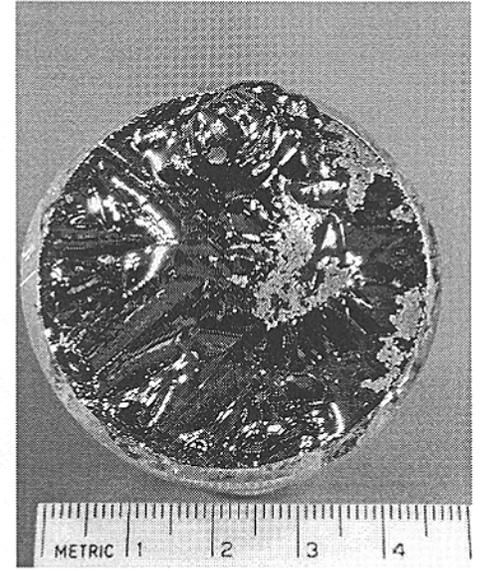


Fig. 2f. Freeze-out particle clumps

Bulk determinations of C and O content in treated high-B, EG-Si feedstock, CZ and FZ ingots grown from it, and a CZ ingot grown from high-purity EG feedstock doped p-type to $0.7 \Omega\text{-cm}$ were made by Fourier transform infrared spectroscopy (FTIR). The results are shown in Table I. Higher levels of C are seen in the treated EG-Si and the CZ crystal grown from it than in the CZ crystal grown from high-purity EG-Si. Oxygen levels are comparable. Free carrier absorption in this relatively heavily B-doped material causes a steeply sloped baseline in the vicinity of the C and O absorption peaks and introduces some uncertainty in the C and O values. The resistivity of a segment from treated high-B, EG-Si feedstock was $0.4 \Omega\text{-cm}$, p-type, and CZ and FZ crystals grown from other segments of treated high-B, EG-Si feedstock also had resistivities of $\sim 0.4 \Omega\text{-cm}$, p-type.

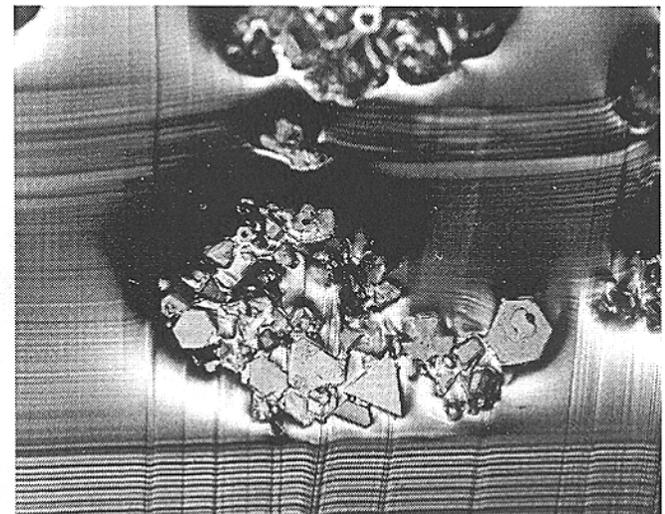


Fig. 3. Optical photomicrograph of a particle clump (the picture shows a 1-mm region)

Minority charge-carrier lifetime τ was measured by the photoconductive decay (PCD) method on the same segments and ingots using a 1064-nm light source. The treated feedstock had a lifetime of 0.3-0.9 μsec . The CZ ingots had lifetimes of 7-10 μsec (treated reject high-B,

Table I. Properties and Diagnostic Solar Cell Performance of Treated, High-B Reject EG-Si Feedstock, CZ and FZ Crystals Grown from It, and a CZ Control Crystal Grown from doped EG-Si Feedstock

Sample	Source	C (cm ⁻³)	O (cm ⁻³)	ρ (Ω -cm)	Lifetime (μ s)	Cell Efficiency with ARC* (%)
3-28M5D	Treated hi-B EG-Si feedstock	4x10 ¹⁷	6x10 ¹⁷	0.4	0.3 - 0.9	8.3
CZ-010309	CZ from treated hi-B EG-Si feedstock	1x10 ¹⁷	1x10 ¹⁸	0.4	7 - 10	14.0
FZ-010222	FZ from treated hi-B EG-Si feedstock	4x10 ¹⁷	<1x10 ¹⁷	0.4	130	13.8
CZ-010302	Control CZ from EG-Si feedstock	5x10 ¹⁶	1x10 ¹⁸	0.7	15 - 22	14.1

*ARC – Antireflection Coating

EG-Si feedstock) and 15-22 μ sec (high-purity EG-Si feedstock), respectively, and the FZ crystal lifetime was 130 μ sec. Table I also shows parameters for 1-cm² diagnostic solar cell devices fabricated on wafers cut from a segment of the treated reject high-B, EG-Si feedstock (3-28M5D), CZ and FZ ingots grown using the treated feedstock, and a CZ ingot grown using high-purity EG-Si feedstock. This small sampling of device performance indicates that devices made directly on as-treated feedstock have a little over half the efficiency of devices made from control CZ samples. However, devices on CZ and FZ crystals grown from the Crystal Systems-treated reject hi-B EG-Si feedstock have comparable PV performance (14.0% and 13.8% efficiency respectively) to that of CZ control samples (14.1%).

Summary and Discussion

Silicon FZ and CZ crystals were grown and characterized, and diagnostic solar cell devices were made, using a new type of SoG-Si feedstock developed by Crystal Systems. The SoG-Si is obtained by gaseous and slagging treatments of melted, heavily boron-doped (~200ppma) reject EG-Si from the electronics industry to reduce the boron content to about 1 ppma. The feedstock produced clean melts and dislocation-free growth could be initiated by both methods. In a number of growth runs, crystallographic structure was lost after about half the melt was solidified by an apparent mechanism of high carbon content eventually reaching supersaturated levels and precipitating SiC. This is probably not a serious issue for multicrystalline growth methods, especially those with a submerged solid/liquid interface. It would be problematic for single-crystal growth. The treated MG-Si had a more definite SiC formation problem, and single crystal growth could not be initiated with that material. Efforts are under way by Crystal Systems to reduce the C content in both treated hi-B reject EG-Si and MG-Si, as well as the P-content in treated MG-Si.

The PV conversion efficiencies of 1-cm² devices made from CZ crystals we grew using the new treated hi-B EG-Si reject feedstock (14.0%, AR-coated) were up to 99% as high as those from CZ crystals we grew using EG feedstock. Devices with an efficiency of 8.3% were also made directly on wafers cut from the treated hi-B EG-Si feedstock. Only a few cells have been processed. Device parameters for this material have not yet been optimized, and additional diagnostic device fabrication, analysis, and verification is under way.

Acknowledgements

We thank NREL's Measurements and Characterization teams for assistance with PCD, FTIR, and EMPA analysis. This work was supported by DOE contract DE-AC36-99GO10337.

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Introduction

Of the more than 300 MW of photovoltaic modules sold per year, about 85% are made from silicon. Manufacturers have repeatedly expressed concern about the future supply of low-cost feedstock as this market continues to grow by more than 30%/year. A projection by one of the large polysilicon manufacturers indicates that PV demand for reject Si from the electronics industry will exceed the supply (8,000 metric tons/yr) by a factor of 2 to 4 by the year 2010 [1]. This does not represent a fundamental material shortage problem, because the technology, quartzite, and coke needed to make feedstock are in abundant supply. The issue is to supply feedstock with the necessary purity (~99.999%) at an acceptable cost. We report research on four novel methods for purification of metallurgical-grade silicon (MG-Si): (1) repetitive porous MG-Si etching, gettering, and surface-removal of impurities; (2) MG-Si gaseous melt-treatment in collaboration with Sandia National Laboratories (SNL); (3) MG-Si purification by recrystallization of Si from MG-Si/metal solutions; and (4) iodine chemical vapor transport purification of MG-Si.

1. Porous MG-Si etching, gettering, and surface-removal of impurities

This approach is based on earlier findings [2] that porous-silicon (PS) etching of the surface of a heavily boron doped Si wafer, followed by an elevated-temperature gettering step, causes an enhanced boron concentration near the wafer surface. The concept is that removing this accumulation layer followed by repetition of the steps a number of times, n , would lower the impurity content of the bulk interior of a granular sample. The objective of our work was to determine the required value for n using 500- μm thick, 20-mm x 20-mm wafers cut from as-received large chunks of MG-Si.

A treatment cycle started with porous Si etching, which creates preferential sites for impurity gettering, at room temperature using HNO_3/HF (1/100) for 6 min. Second, to facilitate diffusion of impurities to energetically favorable sites at surface, annealing was carried out for 30 min at 950°C in an argon ambient using a standard horizontal diffusion furnace. Third, the porous Si surface layer containing accumulated impurities was converted to SiO_2 by oxidation at 950°C using an O_2 ambient and a prescribed temperature (T) vs. time (t) cooling profile. Finally, the impurity-containing oxide layer was removed by dipping in a 10% HF solution for 10 min. We repeated the treatment cycle up to five times. Impurity analysis at various stages was done by secondary ion mass spectrometry (SIMS) for six elements (Al, B, Cr, Cu, F, and Fe) to a depth of about 3 μm . A typical SIMS profile is included in Figure 1, which shows that impurities generally collected near the surface. By integrating the SIMS data, we determined an impurity area density from 0.25 μm to 2 μm . Figure 2 is a plot of the impurity area density as a function of processing steps (after oxide removal). The projected number of cycles that would be necessary to meet the minimum purity requirements for solar-grade silicon (SoG-Si) with this impurity-gettering process is from 800 to more than 10,000 (Table I), and thus is unrealistic even with the margin of error arising

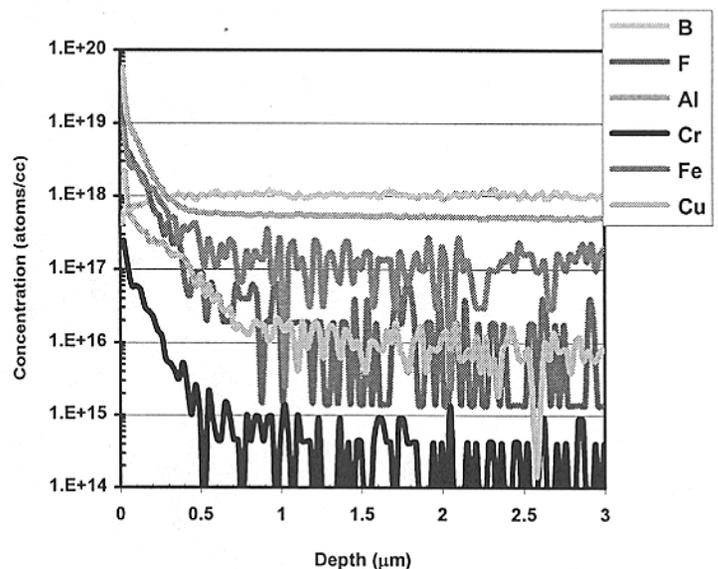


Fig. 1. SIMS profile for MG-Si after one complete cycle.

Table I. Area Density Calculation Summary for Al, Cu and Fe

Area Density (cm ⁻²)			
Cycle #	Al	Cu	Fe
1	6.18E+13	1.68E+13	6.54E+12
2	8.44E+15	6.77E+12	1.85E+14
5	1.76E+14	9.16E+12	1.74E+14
Bulk (100µm)	2.50E+18	8.00E+16	3.00E+18
# of Cycles Needed	8.65E+02	2.29E+05	2.05E+04

from the difficulties of measuring surface segregation with the SIMS technique.

2. MG-Si gaseous melt treatment

Based on thermochemical calculations for gaseous melt treatments to purify liquid MG-Si at Sandia National Laboratories (SNL) [3], we collaborated with SNL to perform small-scale tests of a few of the promising predictions at NREL prior to larger tests planned at SNL. We focused on boron removal from high-purity silicon melts doped with 20 ppm or 2×10^{18} atoms·cm⁻³ B. In separate experiments, four different gases [argon (Ar) for a control, Ar bubbled through distilled water, Ar bubbled through 37% ammonia solution, and ultra-high purity N₂] were introduced at about 1.5 liter/min through a quartz tube placed 2 mm above the melt for a treatment time of 2 h. The original plan was to bubble the gases through the melt, but melt splashing was problematic with our small-scale apparatus. The melts were then directionally solidified at a cooling rate of 1° C/min in a temperature gradient. Bulk resistivity measurements were made on pieces of the solidified melt to determine B concentration.

Figure 3 summarizes the resistivity measurements for each test. The most effective melt treatment was moist Ar from a distilled water bubbler. There was a 40% reduction of boron for a 2-h run. More B reduction is necessary for MG-Si purification, which could be achieved by processing the melt for longer times and bubbling the gas through the melt instead of directing it at the surface to improve the purification efficiency.

3. Purification by recrystallization of Si from MG -Si/metal solutions

During directional solidification of silicon, impurities contained in the melt incorporate into the silicon lattice at reduced levels according to the segregation determined by their respective impurity-silicon binary

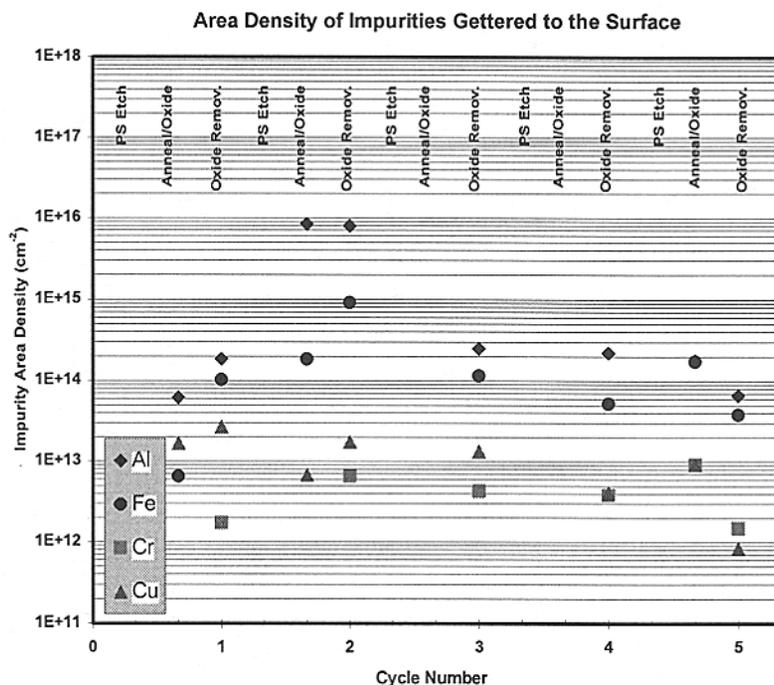


Fig. 2. Plot showing the area density of impurities after various processing steps over many cycles: PS etch, anneal/oxide, and oxide removal.

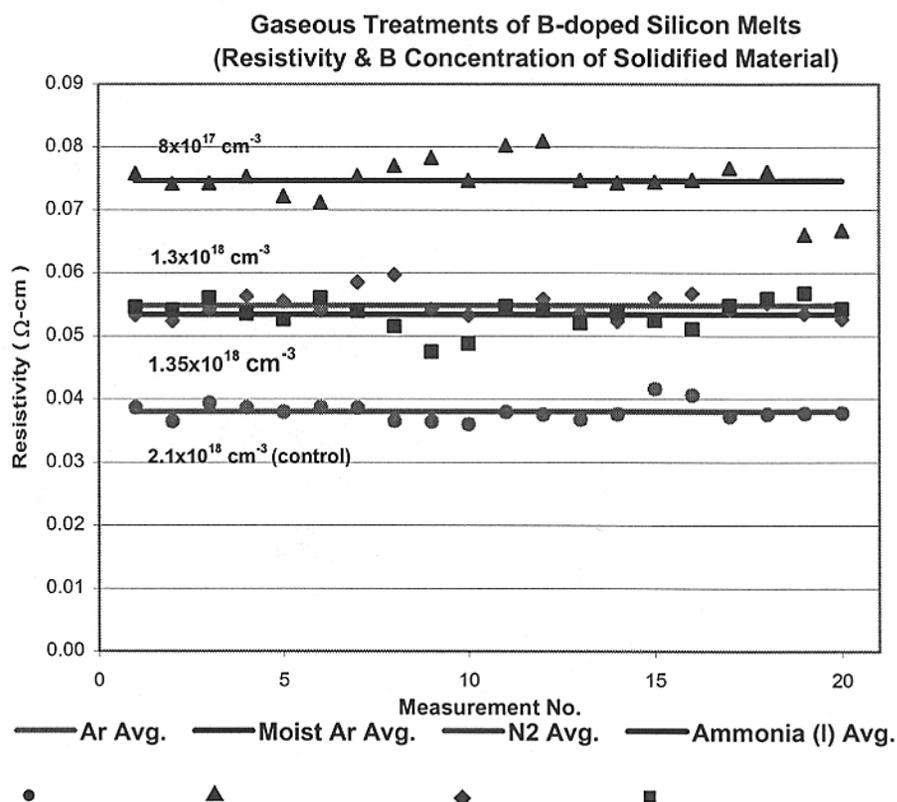


Fig. 3. Bulk 4-probe resistivity averaged over 20 measurements

solubilities. However, if we use metals as solvents to dissolve silicon, recrystallization takes place at a much lower temperature. Most impurities exhibit retrograde solubility in silicon with peaks around 1300°C. Some of the most harmful elements in metallurgical-grade silicon, such as Ni, Co, Fe, and Cr, have their solubility in silicon decreased by more than one order of magnitude (from that at the silicon melting point) if the crystallization is done at temperatures below 800°C. Many metals (e.g., Ag, Al, Au, Cu, Ga, In, Sb, Sn, Zn, etc) form eutectics with silicon at much lower temperatures than the silicon melting point. Those with minimal detrimental effects on cell performance and with moderate slope of the liquidus line are preferred.

An example of this approach is presented here for the Al-Cu-Si ternary solution. When solidifying Si from this system, the chemical potentials of respective elements in the liquid phase must be equal to those in the solid phase. The chemical potential of an individual element is determined by its activity (the ratio of an element's fugacity in the mixture at equilibrium to its fugacity in a pure state), which is the product of its activity coefficient and composition fraction. Using the regular solution model, the activity coefficient of element 1 may be given by

$$\gamma_1 = \exp\left\{\frac{\Omega_{12}(x_{12})^2 + \Omega_{13}(x_{13})^2 + (\Omega_{12} + \Omega_{13} - \Omega_{23})x_2x_3}{RT}\right\}, \text{ where } \Omega \text{ is the interaction parameter between two elements,}$$

defined by heat of mixing, $\Delta H_{mix} = \frac{x_1x_2}{x_1 + x_2} \Omega_{12}$. The segregation coefficient for an element is thus the ratio of

its activity coefficient in the liquid phase to that in the solid phase. Because the silicon crystal is almost pure (to 10^{-3}), the Si activity is approximately unity by definition, and so is its activity coefficient. Thus the composition of silicon in the liquid phase may be written as a function of the three interaction parameters,

$$x_{Si}^l = \exp\left\{-\frac{\Omega'_{SiAl}(x_{Al}^l)^2 + \Omega'_{SiCu}(x_{Cu}^l)^2 + (\Omega'_{SiAl} + \Omega'_{SiCu} - \Omega'_{AlCu})x_{Al}^lx_{Cu}^l}{RT}\right\}.$$

Therefore, the interaction parameters can be determined by trying solutions of different compositions to get the same growth temperature. From our earlier work [4], these values at $T=1173\text{K}$ are $\Omega'_{SiAl} = 2.430RT$, $\Omega'_{SiCu} = 2.469RT$, $\Omega'_{AlCu} = -0.103RT$. The activity coefficient for Al in the liquid can now be written as

$$\gamma'_{Al} = \exp\left[\frac{\Omega'_{SiAl}(x_{Si}^l)^2 + \Omega'_{AlCu}(x_{Cu}^l)^2 + (\Omega'_{SiAl} + \Omega'_{AlCu} - \Omega'_{SiCu})x_{Si}^lx_{Cu}^l}{RT_e}\right] = \exp\left[2.43(x_{Si}^l)^2 - 0.103(x_{Cu}^l)^2 - 0.142x_{Si}^lx_{Cu}^l\right].$$

Because all metal impurities are always very diluted in a crystalline silicon matrix, from Henry's law, activity coefficients for metal elements including Al in solid silicon may be treated as constant. Thus by doing one experiment, one may obtain the activity coefficient in the liquid.

$$\gamma_{Al}^s = \frac{x_{Al}^s \gamma'_{Al}}{x_{Al}^l} = \frac{x_{Al}^l \exp\left[2.43(x_{Si}^l)^2 - 0.103(x_{Cu}^l)^2 - 0.142x_{Si}^lx_{Cu}^l\right]}{x_{Al}^s} = 8991.$$

The segregation coefficient of Al for growth of silicon from Al-Cu-Si mixture is finally obtained,

$$k_{Al} = \frac{x_{Al}^s}{x_{Al}^l} = \frac{\gamma'_{Al}}{\gamma_{Al}^s} = \frac{\exp\left[2.43(x_{Si}^l)^2 - 0.103(x_{Cu}^l)^2 - 0.142x_{Si}^lx_{Cu}^l\right]}{8991}.$$

In short, because both Ω'_{SiAl} and Ω'_{SiCu} are large positive numbers, Si-Al and Si-Cu interactions are repulsive in nature (with higher heat of mixing). Ω'_{AlCu} is negative, however, implying an attractive interaction between Al and Cu (with lower heat of mixing). Therefore, Cu in the growth solution will not only dilute Al, but will also retain Al in the liquid, thus providing greater control for Al doping. This phenomenon will be explored using a similar analytical approach for additional silicon/metal solvent combinations to reduce incorporation of more detrimental impurities using a less harmful metal as a solvent.

4. Iodine chemical vapor transport (ICVT) purification of MG-Si

This purification technique arose from our work on growth of thin-layer Si at atmospheric pressure [5]. Iodine reacts with Si to form SiI_4 , which reacts further with silicon to form SiI_2 . SiI_2 decomposes easily at high temperatures, with a silicon deposition rate $>5\mu\text{m}/\text{min}$ when the source Si temperature is $>1200^\circ\text{C}$ and the substrate temperature is 1000°C . With MG-Si as the source material, impurities may be effectively

removed in several ways: (1) During the initial reaction between iodine and MG-Si, the formation of impurity iodides will be advanced or retarded depending on their free energies of formation. (2) Purification of SiI_4 by distillation in a cyclic process will cause metal iodides with vapor pressure lower than that of SiI_4 to remain at the bottom of a distillation tower, and those with higher vapor pressure to rise to the top. For example, at one atmosphere, carbon tetraiodide boils at 19°C higher than SiI_4 and phosphorous triiodide at 63°C lower. These large differences permit easy separations. (3) During the deposition of silicon from SiI_2 some metal iodides have a large negative value of standard free energy of formation, so they are more stable than SiI_2 and SiI_4 . These iodides will form readily in the gas phase, but have only a small tendency to be reduced again in the deposition zone.

Because SiI_4 distillation [step (2) above] has been studied [6], we only need to investigate purification by the initial reaction between iodine and MG-Si and the final deposition of silicon from SiI_2 [steps (1) and (3) above]. We first grew $\sim 100\text{-}\mu\text{m}$ -thick epitaxial layers of Si by ICVT from a MG-Si source onto high-purity, single-crystal substrates. Impurity levels in these layers are shown in Fig. 4; they were analyzed by SIMS and glow discharge mass spectroscopy (GDMS), with MG-Si source material impurity levels determined by GDMS. Also shown is the permissible range of impurities in SoG-Si, dependent on growth method. Next, multiple large area substrates were used for ICVT growth of thick layers that were harvested and melted as feedstock for Czochralski (CZ) crystal growth (Fig. 5) and analysis. All major impurities are reduced by several orders of magnitude except for B (and P, not shown). Addition of the distillation step (2) should reduce B and P to the SoG-Si specification.

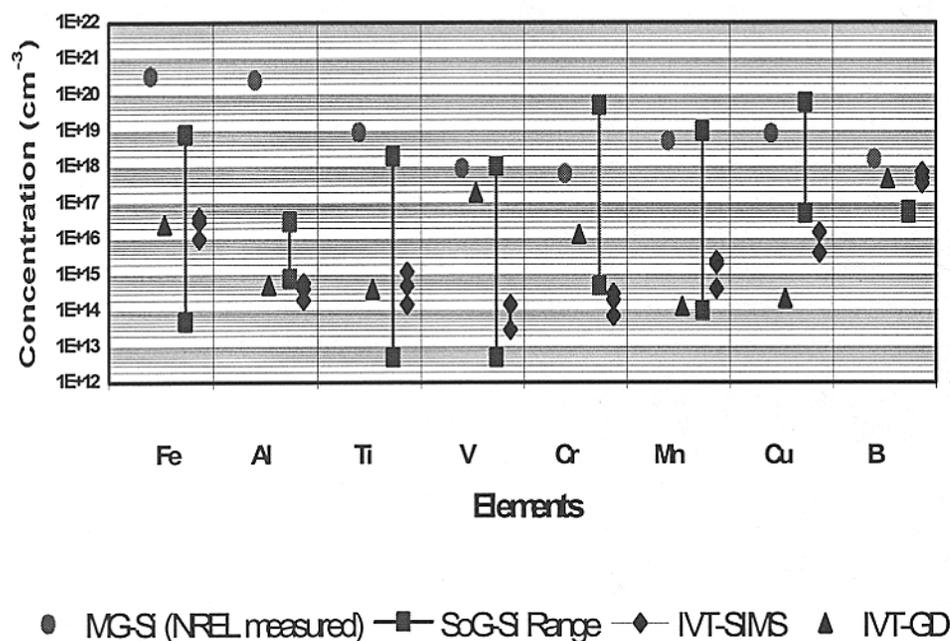


Fig. 4. Impurity contents in the MG-Si source material and in an epitaxial silicon layer grown by ICVT

technique. The crystal was highly compensated, with $\rho = 0.4 \Omega\text{-cm}$, p-type, near the seed end and $0.3 \Omega\text{-cm}$, n-type, near the tail end. Diagnostic solar cells from seed end wafers had an efficiency of 9.5% (see Fig. 6).

Summary and Discussion

Of the four novel MG-Si purification methods we have presented here, the ICVT technique is particularly attractive because it offers fast deposition rates and atmospheric-pressure operation. We have demonstrated a very effective reduction of metallic impurities by several orders of magnitude using this process. Coupled with the SiI_4 distillation step [step (2) mentioned above] to remove B, P, and C, this could lead to a very practical and economical method for manufacturing SoG-Si feedstock. Unlike the current silicon chlorosilane process for silicon feedstock, SiI_4 distillation is much less complicated (no multiple $\text{SiH}_n\text{Cl}_{4-n}$ intermediate compounds). And unlike the earlier SiI_4 -only based process that requires a vacuum



Fig. 5. A 14-mm-diameter $\langle 100 \rangle$ CZ crystal grown from ICVT-purified MG-Si

Table II shows the GDMS analysis of impurities in the MG-Si source and in the CZ crystal grown from ICVT-purified silicon. All metal impurities are below the detection limits of the GDMS

system, our atmospheric pressure ICVT method is much faster and more convenient. A patent application is in process based on this work [7]. We were able to grow small CZ crystals from the limited amount of Si produced in our lab-scale ICVT reactor. Despite compensation from phosphorous, and even without the SiI₄ distillation step, a diagnostic PV cell efficiency of 9.5% was obtained.

Porous-silicon etch/gettering removal of impurities, although effective in the near surface region, appears to be impractical for bulk purification because of the large number of process cycles that would be required. Gaseous melt treatment with moist argon showed promise for reducing boron levels, but would require longer treatment times and more efficient exposure to the liquid silicon than we used in our lab experiments. We have laid the modeling groundwork for investigation of MG-Si purification via recrystallization of silicon from MG-Si/metal solutions, and have done a few experimental tests that show promise. However, considerable experimental work remains before a thorough assessment of this approach can be made.

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Table II. GDMS Analysis of Impurities in MG-Si Arc Furnace Material and in a CZ Crystal Grown from ICVT-Purified MG-Si (without the SiI₄ distillation step)

Element	CZ-Si from ICVT [ppma]	MG-Si source [ppma]
B	4.157	14.548
C	14.264	107.565
O	17.554	66.706
Mg	<0.001	8.204
Al	<0.005	520.458
Si	Matrix	Matrix
P	6.801	21.762
S	<0.044	0.096
K	<0.007	<0.036
Ca	<0.007	44.849
Ti	<0.001	47.526
V	<0.001	143.345
Cr	<0.001	19.985
Mn	<0.001	19.938
Fe	<0.005	553.211
Co	<0.002	0.763
Ni	<0.002	22.012
Cu	<0.001	1.724
Zn	<0.002	0.077
As	<0.002	0.007
Sr	<0.0003	0.353
Zr	<0.0003	2.063
Mo	<0.001	0.790
I	<0.0002	<0.001
Ba	<0.0002	0.266
W	<0.0003	0.024

< implies a level below the indicated detection limit.

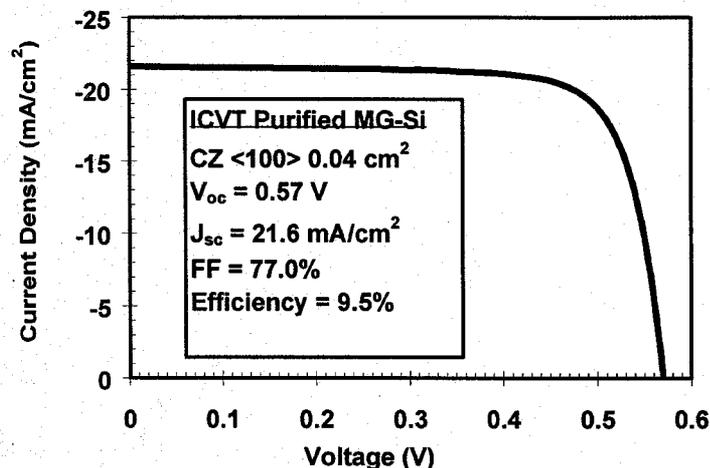


Fig. 6. Diagnostic solar cell parameters for a wafer from a <100> CZ crystal grown using ICVT-purified MG-Si

Thin Layer Si Growth by Atmospheric Pressure Iodine Vapor Transport

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Introduction

The pursuit of thin-layer silicon solar cells has developed into three distinct approaches in the last few years [1], namely, nanocrystalline thin films, polycrystalline thin layers, and single-crystal layer transfer. Whereas progress in the first and last categories has been significant, efforts in the second approach have been limited by grain size and deposition rate dictated by the commonly used (chloro)silane-based chemical vapor deposition technique. However, the recently developed atmospheric pressure iodine vapor transport (APIVT) [2] may provide a much-needed method for depositing polycrystalline thin layers. In addition to being an open deposition system with potential for continuous processing, low capital cost, and no need for expensive effluent treatment, APIVT most importantly has the advantages of high deposition rates (up to 5 $\mu\text{m}/\text{min}$) and large grain sizes ($\sim 20 \mu\text{m}$) at about 900°C on foreign substrates.

Fast deposition and good crystallinity of silicon layers can only be achieved with a high nutrient concentration and near-equilibrium growth process at relatively high temperatures, such as with liquid phase epitaxy [3][4]. Nucleation on non-silicon substrates, however, requires a process with sufficient driving force (non-equilibrium growth) to overcome the nucleation barrier, such as chemical or physical vapor deposition (CVD or PVD). However, the commonly used CVD or PVD techniques provide too much a driving force for deposition so that the achievable grain sizes are invariably inadequate for solar cell applications.

Silicon deposition from silicon-iodine compounds was previously studied for high-purity polycrystalline silicon feedstock production, as well as for epitaxial silicon growth. These techniques may be divided into three categories, namely pyrolytic decomposition of SiI_4 [5], hydrogen reduction of SiI_4 [6], and a disproportionation reaction between SiI_2 and SiI_4 [7]. Iodine vapor was found to readily react with silicon to produce SiI_4 at approximately 600°C. When SiI_4 vapor at low pressure (<10 mtorr) is heated to a temperature higher than 800°C, it will decompose to yield solid silicon and iodine vapor. At higher pressures (~ 100 torr), silicon deposition by hydrogen reduction may be possible. At temperatures over 1000°C and in the presence of SiI_4 and excess silicon, significant quantities of SiI_2 can be generated [8]. The disproportionation reaction between SiI_2 and SiI_4 to transport silicon through a temperature gradient in a sealed vessel was shown to occur over a wide pressure range (15-10,000 torr) [8], to have a pressure-dependent transport direction [7], and to have potentially high deposition rates [9], although some suggested serious difficulty in nucleation when a silicon substrate is covered by silicon oxides [8]. The same reaction may be carried out in an open system by using a carrier gas stream to move SiI_2 (an eventual product of iodine and silicon) from the source region to the deposition region, but growth rate is reduced due to dilution, and effluent treatment must be provided.

All growth systems at pressures below or above one atmosphere require either a vacuum system that is capable of dealing with the corrosive nature of iodine or a sealed (load-locked) vessel, which are cost prohibitive for low-cost and large-scale production of solar cells. However, chemical vapor transport using the disproportionation reaction offers the possibility of atmospheric pressure operation. Furthermore, the difficulty in nucleation on silicon oxides provides an opportunity for large-grain growth on foreign substrates. Here we present some silicon thin-layer growth results using the APIVT technique, as illustrated in Fig. 1. The actual experimental set up may be found elsewhere [2].

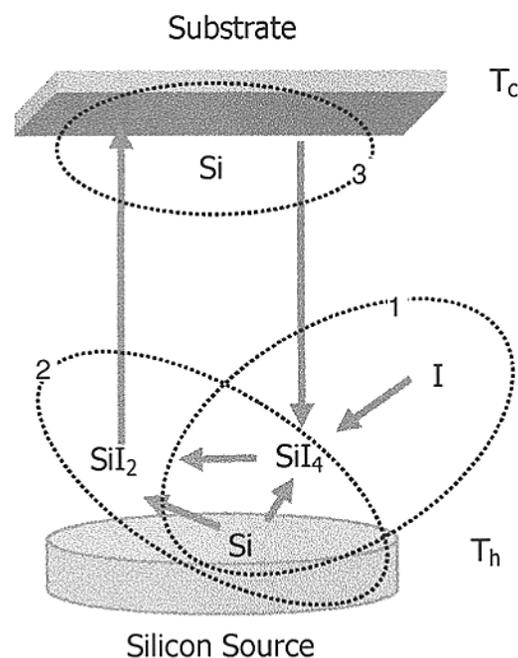


Fig. 1. The disproportionation reaction for transporting silicon

1. Transport direction

The direction in which silicon is transported is an important issue because it determines the requirement on substrate materials and crystal growth driving force. A high- to low-temperature transport is preferred because it allows the substrate to remain at a relatively low temperature while still achieving enough free energy driving force to facilitate nucleation. At low initial iodine pressures (<10 mtorr), low- to high-temperature transport consistently occurs [5], and involves SiI_4 pyrolytic decomposition. At high pressures (>3800 torr), high to low temperature transport was demonstrated due to the disproportionation reaction [8]. However, for the intermediate pressure regime (near atmospheric), conflicting results were reported. In one instance, low- to high-temperature transport was demonstrated for pressures up to more than 500 torr [9]. In another, the opposite was reported for total pressures higher than 30 torr and up to one atmosphere [10]. Thermal equilibrium calculations [11] seem to support the later case.

Our atmospheric pressure growth experiments definitely show high- to low-temperature silicon transport, although a minimum substrate temperature of about 800°C was needed to initiate nucleation on Corning Vycor® high-temperature glass or Corning LGA-139® substrates, while the source silicon was kept at 1000°C. A set of experiments with different source silicon to iodine ratios of 1:5 (excess iodine) and > 1:2 (excess silicon) were carried out to determine the gas species' effect on deposition. We found no silicon deposition with excess iodine, in which case only SiI_4 would be formed, whereas fast deposition was obtained with excess silicon where SiI_2 should be present. This result confirms that the pyrolytic decomposition of SiI_4 does not occur at one atmosphere with appreciable yield, at least in a high- to low-temperature transport configuration. Only the disproportionation reaction between SiI_2 and SiI_4 is responsible for silicon transport from high to low temperature at a total pressure of one atmosphere.

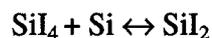
Because the reactor is an open-tube type, total pressure is the only measurable parameter. Nonetheless, the sum of partial pressures of SiI_2 and SiI_4 should be very close to the total pressure due to the gravity segregation effect that is visibly identifiable. The silicon iodides are much heavier than the protective hydrogen gas curtain, and are balanced with the outside ambient.

2. Nucleation versus grain size

For a given growth temperature, grain sizes in a polycrystalline film may be determined by nucleation density because subsequent growth is epitaxial on these nuclei. Nucleation theory [12] implies that the higher the free energy driving force in a crystal growth process, the smaller the critical nucleus size will be, and thus the denser the nucleation sites will be. Silicon film deposition by physical methods (sputtering, thermal evaporation) usually result in very small-grain polycrystalline or even amorphous structures unless a very high substrate temperature is used; this is due to a large chemical potential difference between the gas phase source and the final deposited state. Even the commonly used chemical vapor deposition method using chlorosilanes or monosilane cannot achieve adequate grain sizes because of the high free-energy driving force (non-equilibrium process). On the other hand, near-equilibrium growth processes such as liquid phase epitaxy or solution growth have too small of a free-energy driving force to overcome the nucleation barrier on foreign substrates, despite the fact that these techniques are capable of high growth rates. The rate of deposition is determined by both the free-energy driving force and the concentration (density) of available silicon atoms.

An ideal situation would be to have enough free-energy driving force to overcome the nucleation barrier but not enough to form excessively dense nucleation sites. The ability to nucleate on non-silicon surfaces is not a given characteristic of the iodine growth process [8]. In fact, a thermally grown silicon oxide layer was used as a mask to epitaxially grow silicon selectively only on the non-masked silicon surfaces [10]. However, with increased temperature difference between the source and substrate, the free energy driving force is higher, and adequately sparse nucleation densities would be possible.

Another likely mechanism that leads to adequately sparse nucleation is the reversible nature of the disproportionation reaction. At equilibrium, initially realized near the source, the reaction



reaches a dynamic balance. Then SiI_2 is transported to the substrate region by diffusion and convection, where SiI_2 is supersaturated at the lower substrate temperature. The reaction then goes to the left, and silicon atoms or clusters will adsorb to the substrate surface. Now, locally excess SiI_4 pushes the reactions to the right, so small nuclei are etched back. Only larger nuclei are able to grow from the incoming adatoms.

Nucleation is an adsorption process that is determined by the interaction between the incoming silicon atom or a silicon atom cluster and the substrate surface. Obviously, it depends on the substrate material, because the nucleation barrier (energy barrier for adsorption) is material dependent.

3. Highly [110]-textured and randomly oriented polycrystalline Si films on glass substrates

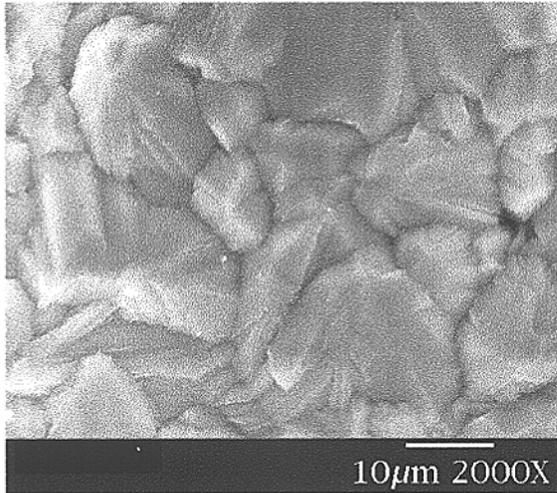


Fig. 2. Typical grain structure of an APICVT deposited Si film obtained at 900°C

Polycrystalline silicon grains as large as 20 μm are easily obtained, as shown in Fig. 2. Higher substrate temperatures favor larger grain growth, similar to any other crystal growth process. APICVT-grown films typically have grains with random orientations. By modifying the deposition conditions, it is possible to achieve highly [110]-oriented films. Fig. 3 shows X-ray diffraction peaks from two samples, both deposited on high-temperature glass, in comparison to standard silicon powder peaks. All the peaks were normalized to the standard [111] peak. The solid line is for a sample that was deposited under normal conditions, which showed almost random orientations, with slight [110] texturing. The dashed line, on the other hand, is a sample deposited under a different condition, but with similar grain size and thickness. This sample demonstrates a [220] intensity nearly 4.5 times of the standard peak. This clearly shows that this silicon layer is highly [110]-oriented.

Transmission electron microscopic (TEM) observation indicates that more than 90% of the grains are within about 5° of the <110> axes. Two of the perfectly [110]-aligned grains actually allow one to see a high-resolution image of the grain boundary with dislocation cores (Fig. 4).

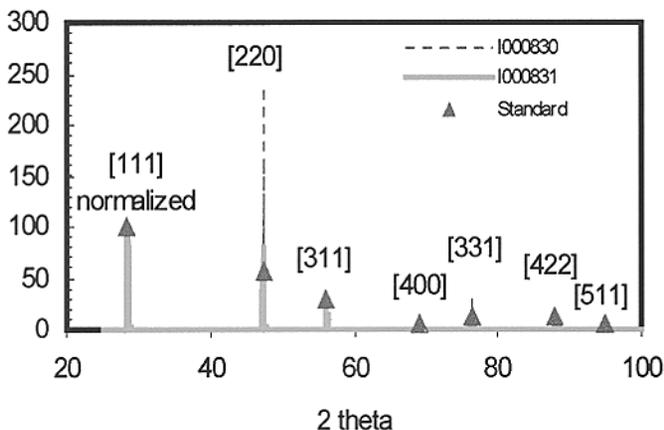


Fig. 3. XRD peaks of silicon films deposited with different conditions

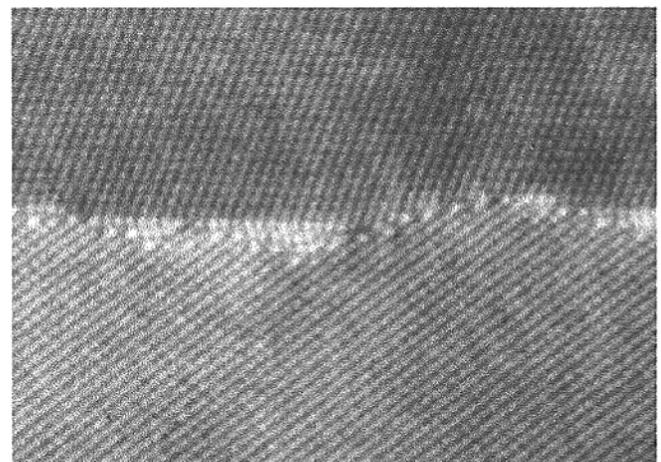


Fig. 4. High-resolution image of two perfectly [110]-aligned grains

4. Epitaxial growth

When a silicon substrate is used, epitaxial growth can take place if a clean interface is maintained. This allows us to obtain high-quality active layers on low-cost metallurgical-grade silicon substrates. Epitaxial layers also give us a measure of the solar cell performance limitations of this material independent of any grain size effect. TEM studies of the layers indicate very low density of crystallographic defects (such as stacking faults and dislocations) compared to the underlying substrate, as shown in the high resolution TEM image in Fig. 5. The right side to the dark boundary (interface) is the substrate.

As shown in Fig. 6, a 20-μm thick epitaxial layer grown on a heavily doped single-crystal Si wafer (~0.01 Ω-cm) exhibited $V_{oc} = 0.56V$, $J_{sc} = 14.8 \text{ mA/cm}^2$, $FF = 79\%$, and $Eff. = 6.5\%$ (full area, no AR coating), compared to 0.59V, 17.6 mA/cm², 80%, and 8.2% for a standard CZ control cell. The relatively low current could be attributed to both the small layer thickness and a relatively short diffusion length due to contamination of the iodine source.

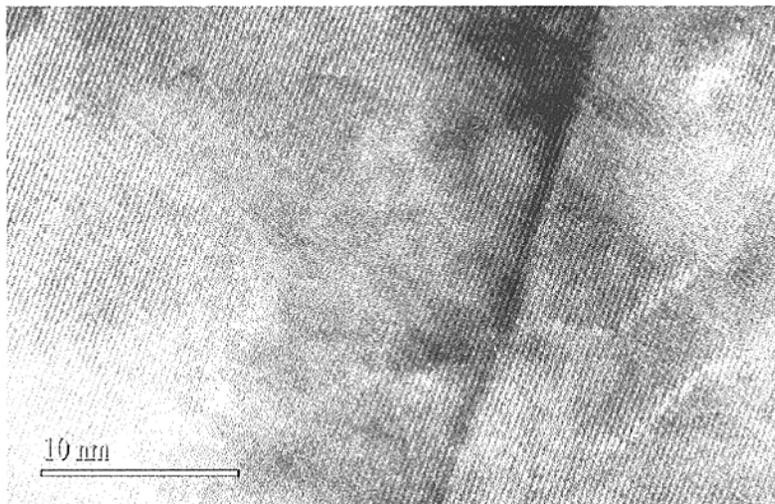


Fig. 5 High resolution TEM image

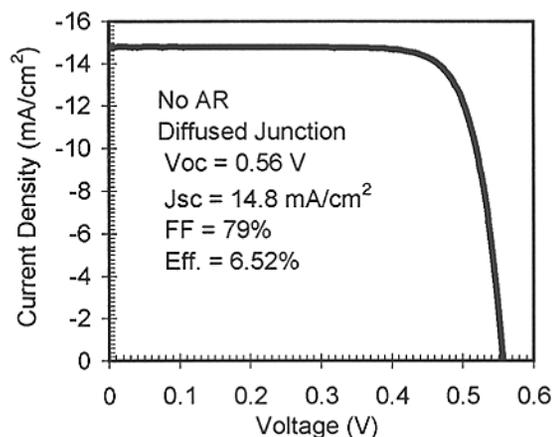


Fig. 6 Diagnostic solar cell result

Summary

The APIVT technique produces continuous polycrystalline silicon layers at high deposition rates (up to 5 $\mu\text{m}/\text{min}$) with large grain sizes ($\sim 20 \mu\text{m}$) at approximately 900°C, on non-silicon substrates such as mullite, Corning Vycor[®] high-temperature glass, or Corning LGA-139[®] glass ceramics. Random-oriented or highly [110]-textured films can be obtained. Epitaxial growth on single-crystal Si substrates show a very low density of lattice defects. Compared to silicon deposited by other techniques, such as rapid thermal chemical vapor deposition (RTCVD), the APIVT technique obtained much larger grain sizes on similar substrates at a deposition temperature a few hundred degrees lower, which is critical to minimize impurity contamination and to lessen the substrate requirement. This new technique overcomes the usual cumbersome operation of a conventional chemical vapor transport or deposition system requiring either a closed system or an open system requiring effluent treatment.

Acknowledgement

We would like to thank Dr. Dieter Ast of Cornell University for providing the Corning LGA-139[®] glass ceramics substrates. We also thank Dr. Yanfa Yan and Rick Matson for electron microscopic characterizations of the materials. This project was supported by the U.S. Department of Energy under contract No. DE-AC36-99-GO10337 to the National Renewable Energy Laboratory.

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Wire Surface Kinetics in Hot-Wire Chemical Vapor Deposition

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ABSTRACT

The technique of threshold ionization mass spectrometry has been used to measure wire-desorbed radicals present during hot-wire chemical vapor deposition growth. For temperatures in excess of 1500K, Si is the predominant radical desorbed from the wire, with a minor contribution from SiH₃. The alloying of filaments, caused by low temperature (<1200K) exposure to silane gas consists of the production of free silicon and a silicide phase (WSi₂) at the filament surface, which can be removed by high temperature baking in vacuum.

INTRODUCTION

Synthesis of large-grained polycrystalline silicon at low temperatures with high throughput is critical to enabling a future thin-film silicon photovoltaics technology. A promising approach for low temperature, high throughput film growth is hot-wire chemical vapor deposition (HWCVD). Fundamental questions remain, however, on the nature of the reactions occurring at the filament surface. These surface reactions produce radicals that may act as the primary film precursors (low pressure regime) or may react in the gas-phase (high pressure regime) to produce other film precursors. The film precursor can have an important effect on the resulting film microstructure (e.g. rough, island growth versus epitaxial growth), as the study by Ichikawa *et al.*¹ suggests. Additionally, work by Thiesen *et al.*² suggest that the predominance of the SiH₃ radical explains, in part, their ability to obtain low temperature epitaxial growth. Recently, it has been demonstrated that filament age has an effect on the resulting film's electronic properties³, speculated to be related to differences in radical chemistries associated with aged versus new filaments. No studies have probed, however, whether such differences exist, and if so, what they might be.

EXPERIMENT

Measurements were performed in a UHV chamber with a base pressure of order 10⁻⁸ Torr. Operating pressures of approximately 5x10⁻⁶ Torr were used, with a dilute (1%) mixture of SiH₄ in He (i.e. SiH₄ partial pressures of 5x10⁻⁸ Torr). A straight tungsten filament of 0.5 mm diameter was used and the temperature was determined by use of a single wavelength optical pyrometer. Radical measurements were made with the use of a quadrupole mass spectrometer, with the capability of tunable electron energy to enable threshold ionization measurements.

RESULTS AND DISCUSSION

The distribution of monosilicon radical species as a function of wire temperature (1300-2500K) is shown in Fig. 1; measurements were made with a wire having no previous silane exposure. Similar to other studies⁴⁻⁶, we find that Si is the predominant radical desorbed from the filament for wire temperatures above 1500K. Above 1800K, a saturation in the Si signal is noted, with a slight decrease above 2300K, an effect also observed in previous work.⁴⁻⁶ The explanation of this phenomena is possibly the competition between desorption (evaporation) and decomposition⁷. It should be noted that the temperature dependent data taken in this study were collected with decreasing temperatures, from 2500K to 1300K. It was believed that starting at the lowest temperatures, at which point a silicide or Si film is believed to form⁴, would lead to a bias in the high temperature data if much of this silicide or Si film remained at high temperatures. In fact, a hysteresis in the Si signal was observed when data was first taken with sequentially decreasing temperatures followed by an increasing temperature cycle, consistent with the evaporation of free silicon from the wire surface. It is clear from the preceding that the Si signal is strongly dependent on the complex changes that occur at the wire surface over this temperature regime.

The second most abundant radical evident from Fig. 1 is SiH₃, in agreement with the study by Doyle *et al.*⁴. Over the entire temperature range investigated (1300-2500K), this radical signal shows a small activation energy of 8 kcal/mole. As it is believed that the formation of this species is due simply to a H atom exchange at the surface, such a small activation energy is believed to be reasonable⁴. In addition, the Arrhenius behavior observed over such a wide temperature regime suggests the formation of SiH₃ is less sensitive to wire conditions than Si. A recent report by Duan *et al.*⁶ suggest that disilicon species (Si₂H_x) are the second most abundant species (next to Si), followed by SiH₃. The presence of Si₂H_x is believed, however, to be related reactions at the walls of the chamber⁶.

The radicals SiH and SiH₂ were detected in small quantities (<8% of Si), marginally larger than the isotopic contributions from ²⁹Si (4.7%) and ³⁰Si (3.1%). It is believed that the production of these radicals should be minimal, as SiH₄ must react with two or more reconstructed surface dangling bonds to produce them, which is highly exothermic⁴. The study by Inoue *et al.*⁵ shows, in addition to Si and SiH₃, the presence of SiH₂, which becomes the predominant radical below 1700K. In their study, both SiH₂ and SiH₃ signals show precipitous drops above 1700K, an effect not observed with any radicals in previous studies. If the radical formation process occurs through sequential surface reactions, as the authors speculate, then these effects could be explained as resulting from surface decomposition of these radicals. It is noteworthy that the SiH and SiH₂ radical signals appear to exhibit a small activation energy similar to SiH₃, which suggests that their formation is governed by a H abstraction process as well.

A recent study by Mahan *et al.*³ focused on the effect of filament alloying on the electronic properties of hydrogenated amorphous silicon films. They speculate that the differences in film electronic properties were most likely related to differences in radical chemistries associated with a 'virgin' filament versus an alloyed filament. As a means of investigating whether there is a

discernable difference in radical chemistry depending on the condition of the filament, we have made radical measurements on both new and aged filaments. The aging treatment consisted of 'baking' the filament at a temperature of 1300K in the presence of 0.2 mTorr SiH₄ for a period of 15 minutes. X-ray photoelectron spectroscopy (XPS) measurements were then performed on this alloyed filament, the results of which are shown in Fig. 2. The silicon content was determined to be approximately 78% (at the typical XPS penetration depth of ~100 Å), which is consistent with the coexistence of solid Si and the WSi₂ phase; the chemical shifts in the XPS data are also consistent with the oxides of both Si and W, although this contribution is expected to be small, considering the oxygen background levels. The processes that occur during filament 'aging' thus appear to be the conversion of elemental W into silicide (believed to embrittle the wire and ultimately cause wire failure), along with Si deposition on the wire. Evidence for the latter can be seen in Fig. 3, which shows a mass spectrum acquired with the aged filament, with and without SiH₄ present. In the absence of SiH₄, an appreciable Si signal is still observed (with negligible contributions from other radicals), likely resulting from evaporation of previously deposited Si.

The temperature dependence of the Si radical signal for the two cases of a new versus aged filament is shown in Fig. 4. Contrary to the results for the new filament, in which all silicon hydride radicals were observed (Fig. 1), only Si was observed from the aged filament. The signal levels of Si at low temperatures from the aged filament are initially more than an order of magnitude smaller than those from the new filament. As the temperature increases, the signal from the aged filament shows a small activation energy of 20 kcal/mole, while the signal from the new filament saturates. At the highest temperature (~2400K), the Si signals from the two filaments become comparable. The sharp contrast in signals from these two wires lends further support to the idea that the hot-wire process is catalytic⁸. In particular, the observed behavior is consistent with the known effect of alloying on growth rate³, suggesting that the growth of a silicide acts to poison the catalyst (W) and reduce its activity. At higher temperatures, the convergence of the Si signals suggests that this silicide and solid Si adsorbed at the wire surface have been effectively 'baked off', thus restoring the catalytic activity of the wire.

CONCLUSIONS

We find Si to be the predominant radical produced in a HWCVD system for wire temperatures in excess of 1500K. For temperatures below 1500K, the SiH₃ radical becomes predominant. These results are in qualitative agreement with previous studies of radical chemistry at the wire. Temperature dependent radical measurements were found to depend on the temperature cycle, consistent with the deposition and subsequent desorption of free Si from the wire surface. Measurements using XPS, along with mass spectra acquired using 'aged' filaments suggests that the mechanism for this 'aging' process consists of the conversion of elemental W into WSi₂, along with the deposition of free Si at the surface. It was revealed, however, that this 'aging' is to some extent reversible, and the catalytic activity (as present in new filaments) can be restored by a high temperature bake-out.

ACKNOWLEDGEMENTS

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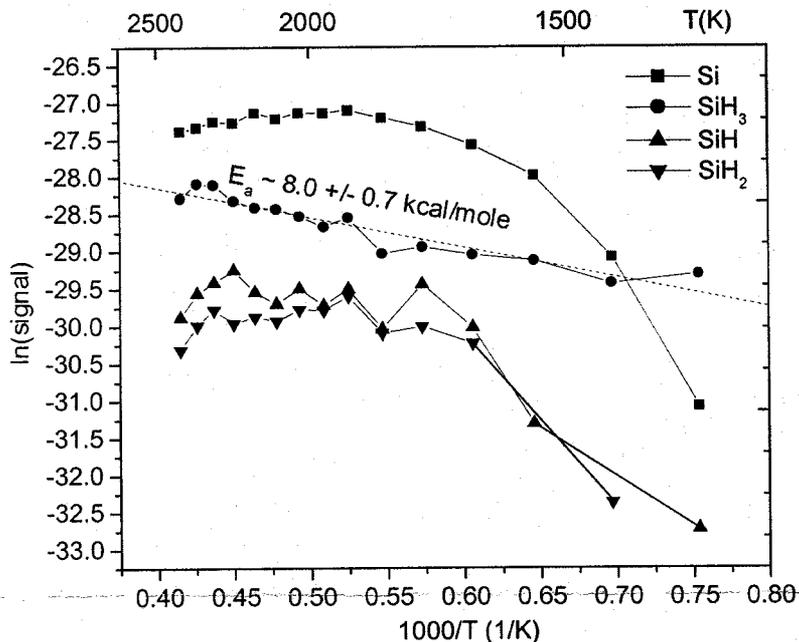


Fig. 1: Low pressure radical species measurements.

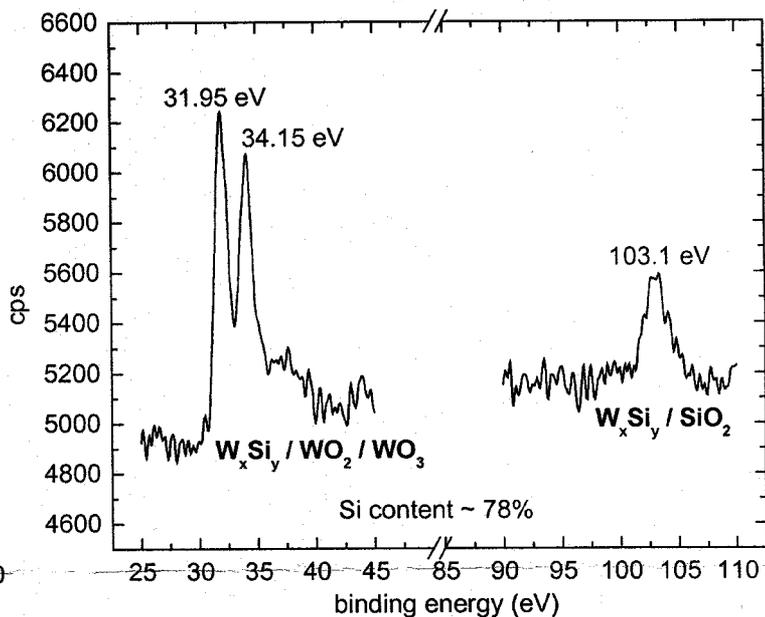


Fig. 2: XPS data (Si and W signals) acquired on a used wire.

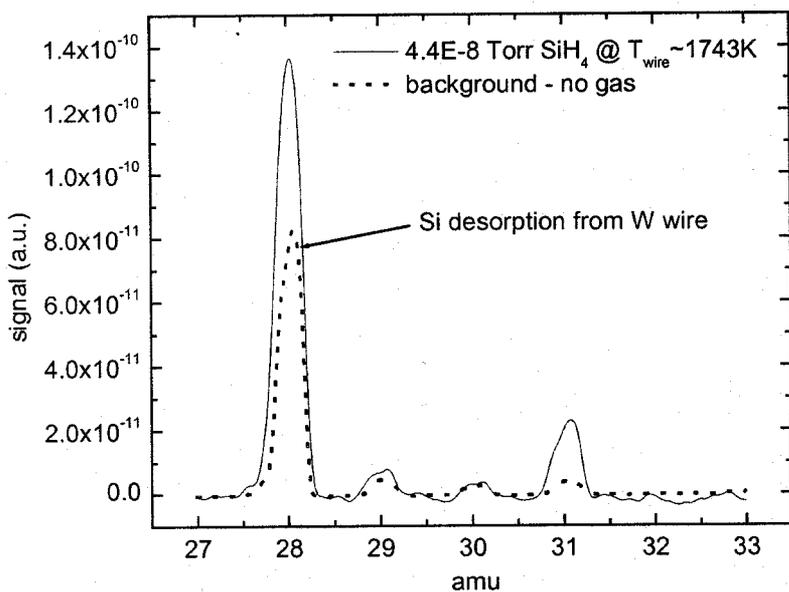


Fig. 3: Evidence for Si incorporation by W wire. (Note: wire baked at 1273K in 0.2mTorr SiH₄ for 15min prior to measurements)

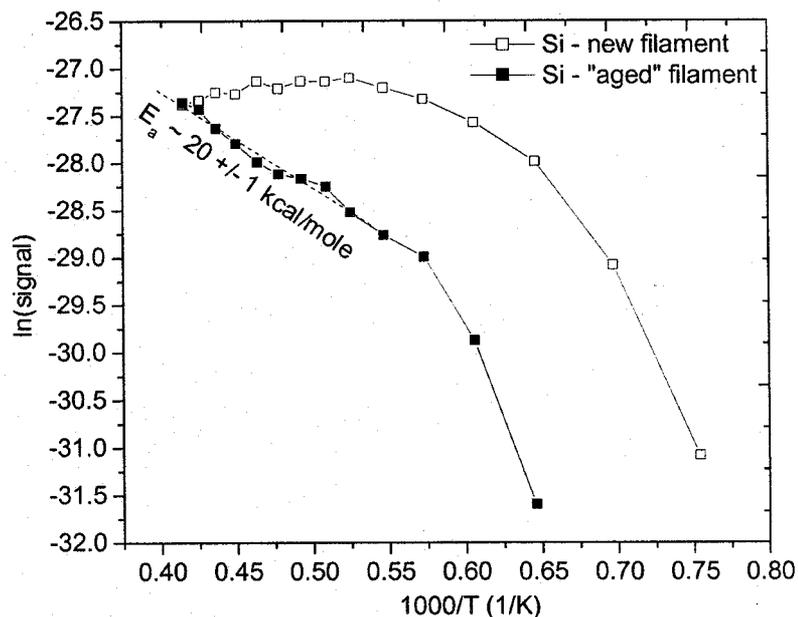


Fig. 4: Si signal as a function of wire temperature for both new and "aged" filaments.

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Guidelines for more accurate determination and interpretation of effective lifetime from measured quasi-steady-state photoconductance

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This paper clarifies three measures that should be taken to more accurately calculate and interpret the effective lifetime (τ_{eff}) from quasi-steady-state photoconductance: 1) In order to account for the dependence of photogeneration on the illuminating spectrum and the test wafer reflectance, the correct value is assigned to the effective optical transmission. 2) In order to account for the dependence on the illuminating spectrum of the constant of proportionality between the short-circuit current of the reference cell and the total photon flux, we introduce a spectral correction factor. 3) Once the correct value of τ_{eff} has thus been found, the solution to the time-dependent continuity equation is applied to assess the error in the commonly used expression $1/\tau_{\text{eff}} = 1/\tau_b + 2S/W$, relating τ_{eff} , bulk lifetime (τ_b), and surface recombination velocity (S). An example illustrates that ignoring these three guidelines can cause S to be underestimated by over 40%.

1. Introduction

The quasi-steady-state photoconductance (QSSPC) technique is very effective for determining the minority-carrier lifetime of photovoltaic-grade multicrystalline silicon materials [1, 2]. In the analysis of a quasi-steady-state photoconductance (QSSPC) measurement, in which the time-derivative of the average excess carrier concentration (n_{av}) is negligible, the effective lifetime (τ_{eff}) is inversely proportional to the average generation rate (G_{av}) in the test wafer [3]:

$$\tau_{\text{eff}}(n_{\text{av}}) = \frac{n_{\text{av}}(t)}{G_{\text{av}}(t) - \frac{dn_{\text{av}}(t)}{dt}}. \quad (1)$$

Thus in order to calculate τ_{eff} accurately, G_{av} must be correctly computed from the measured short-circuit current of the reference solar cell. We illustrate this procedure by referring to the commonly used Sinton data analysis spreadsheet [4], in which G_{av} is proportional to the value assigned to the effective optical transmission (EOT):

$$G_{\text{av}} = \text{Suns} \times \text{EOT} \times (38 \text{ mA/cm}^2) / (q \times W), \quad (2)$$

where q is the electronic charge, W is the wafer thickness, and (EOT) must be correctly adjusted from 1 according to the deviation of the generation current from 38 mA/cm^2 [4]. While an illustration of the dependence of EOT on wafer thickness and surface coating can be found [4], a description of the calculation of EOT does not appear to exist in the literature. Another point worthy of clarification is the interaction between the spectral response of the reference cell and the spectrum of illumination. Since the constant of proportionality between the short-circuit current (J_{sc}) of the reference cell and G_{av} depends on the spectrum of illumination [5], we introduce a spectral correction factor (SCF) to generalize the standard data analysis for arbitrary spectra. While improper assessment of EOT and SCF introduces error in the calculation of τ_{eff} , the subsequent use of the following approximate equation can introduce error in the calculation of τ_b or S , assuming one of the two is known:

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_b} + \frac{2S}{W}. \quad (3)$$

The accuracy of Eq. (3) should be evaluated by comparison with the solution to the continuity equation for exponentially decaying illumination intensity, discussed elsewhere [6]. In order to describe the accurate calculation and interpretation of τ_{eff} , this paper elucidates the theoretical determination of EOT and SCF, applies the solution of the continuity equation to evaluate the accuracy of Eq. (3), and uses measured data to illustrate the importance of these steps to the computation of τ_{eff} .

2. Theoretical calculation of effective optical transmission

Defining $N_{\text{abs}}(\lambda)$ as the incident photon flux spectral density *that gets absorbed in the wafer*, and assuming that each photon absorbed generates one electron-hole pair, then Eq. (2) can be rewritten as

$$EOT = \frac{\int N_{\text{abs}}(\lambda) d\lambda}{\text{Suns} \times (38 \text{ mA/cm}^2) / q} \quad (4)$$

Suns can be written as the ratio of the incident photon flux N_{ph} to the photon flux in 1 Sun, which from 300 nm to 1200 nm is $(46.9 \text{ mA/cm}^2)/q$:

$$EOT = \frac{46.9}{38} \times \frac{\int N_{\text{abs}}(\lambda) d\lambda}{\int N_{\text{ph}}(\lambda) d\lambda} \quad (5)$$

In order to find $N_{\text{abs}}(\lambda)$ as a function of $N_{\text{ph}}(\lambda)$, we integrate the generation rate [7] to obtain

$$N_{\text{abs}}(\lambda) = \frac{N_{\text{ph}}(\lambda)[1 - R(\lambda)][1 + R(\lambda)e^{-\alpha(\lambda)W}](1 - e^{-\alpha(\lambda)W})}{1 - [R(\lambda)e^{-\alpha(\lambda)W}]^2} \quad (6)$$

Equation (8) neglects any reflection off the surface the wafer is resting on. Using Eqs. (5) and (6), EOT can be calculated for any wafer whose $R(\lambda)$ and W are known, given that $N_{\text{ph}}(\lambda)$, the photon flux spectral density of the lamp, is also known.

3. Spectral correction factor for the calculation of τ_{eff} under arbitrary illumination spectra

Experimentally, the value of Suns in Eq. (2) is found by its proportionality with the voltage (V) across a small resistor (R) through which J_{sc} of the reference solar cell flows. Assuming illumination with the AM1.5 spectral content, it can be shown that

$$\text{Suns} = \left(qAR \times \int n_{\text{AM1.5}}(\lambda) \text{EQE}(\lambda) d\lambda \right)^{-1} V, \quad (7)$$

where $n_{\text{AM1.5}}(\lambda)$ is the photon flux spectral density of 1 Sun, AM1.5; EQE is the external quantum efficiency of the reference cell; and the factor in parentheses is provided in the spreadsheet as the V/Sun factor. This factor is assumed to have been obtained empirically under 1 Sun, approximately AM1.5 illumination. Note that Eq. (7) is accurate only under AM1.5 illumination. Under an arbitrary spectrum of illumination, $n_{\text{AM1.5}}$ must be replaced by n_{spec} , the photon flux spectral density of the illuminating spectrum, normalized to 1 Sun intensity. Thus we define the spectral correction factor as

$$SCF = \frac{\int n_{\text{AM1.5}}(\lambda) \text{EQE}(\lambda) d\lambda}{\int n_{\text{spec}}(\lambda) \text{EQE}(\lambda) d\lambda}, \quad (8)$$

so that Eq. (7) can be correctly generalized for illumination by an arbitrary spectrum as

$$Suns = SCF \times \left(qAR \times \int n_{AM1.5}(\lambda) EQE(\lambda) d\lambda \right)^{-1} V, \quad (9)$$

where *Suns* is taken to indicate the factor by which the total incident photon flux differs from that of 1 Sun, regardless of the incident spectrum. Thus, we multiply by SCF so that the *V/Sun* factor, in parentheses in Eq. (9), can be left unmodified. At last, define the modified spectral correction factor $SCF' = SCF \times EOT$ so that Eq. (2) can be revised to

$$G_{av} = SCF' \times Suns \times (38 \text{ mA/cm}^2) / (q \times W). \quad (10)$$

Thus, EOT is replaced by SCF' in the data analysis spreadsheet to account for spectral effects.

Equation (8) is used to calculate SCF for the white light of the Quantum Qflash T2 lamp, whose spectral irradiance was measured at NREL. We use the EQE of a cell measured at ISE; the reference cell in our laboratory, though from the same manufacturer, is expected to behave similarly though not identically. Equation (8) gives $SCF = 0.913$ for the full spectrum of the flash lamp shining through two diffusor plates; this value depends only on the illuminating spectrum and is independent of the test wafer. Figure 1 shows that the use of SCF improves the strongly predicted agreement between transient and QSSPC lifetime data for a wafer with $S < 50 \text{ cm/s}$ [8]. In all cases, we use the calculated $EOT = 1.08$ for this nitride-coated wafer.

EOT is computed from Eqs. (5) and (6) as a function of wafer thickness using the measured reflectance of three common surface coatings. $SCF' = SCF \times EOT$ is plotted in Fig. 2. We recommend that in accordance with Eq. (10), the calculated SCF' be used in place of EOT in the data analysis spreadsheet. Assuming that the reflectance curves on which Fig. 2 is based are typical of the specified anti-reflection coatings, SCF' can be read from the figure for use in data analysis.

4. Comparison of $1/\tau_{eff} = 1/\tau_b + 2S/W$ with solution to time-dependent continuity equation

Assuming τ_{eff} is measured and τ_b is known, the error in *S* resulting from the use of Eq. (3) in QSSPC is obtained by comparison with the solution to the time-dependent continuity equation. Figure 3 shows that Eq. (3) underestimates *S* by more than 25% when $S > 10000 \text{ cm/s}$, for a $300 \text{ }\mu\text{m}$ wafer. Thus, once τ_{eff} is obtained by correctly accounting for photon absorption and spectral response through EOT and SCF, care must be taken to use Eq. (3) only when justified by the solution to the continuity equation [6].

5. Effects of ignoring EOT, SCF, and continuity equation on lifetime data analysis

To illustrate the importance of EOT, SCF, and the use of the full solution to the continuity equation in place of Eq. (3) for high *S*, we take the example of a heat-exchanger method (HEM) multicrystalline silicon wafer coated with SiN_x . Assume knowledge of $\tau_b = 48.3 \text{ }\mu\text{s}$ and $W = 0.325$. Equation (5) is used to correctly calculate $EOT = 1.05$, and Eq. (8) is used to correctly calculate $SCF = 0.913$, resulting in $SCF' = 0.959$. Then $\tau_{eff} = 4.90 \text{ }\mu\text{s}$ is determined from the measured photoconductance, using Eqs. (10) and (1). The solution to the continuity equation [6] gives $S = 3340 \text{ cm/s}$. If Eq. (3) were used instead of the solution to the continuity equation, we would instead find $S = 2980 \text{ cm/s}$, an underestimate, as predicted by Fig. 3. If all three guidelines in this paper were ignored, leaving $EOT = 0.65$ as a default instead of taking into account the anti-reflection coating, implicitly assuming $SCF = 1$, and using Eq. (3) instead of the solution to the continuity equation, we would find $S = 1910 \text{ cm/s}$, over 40% lower than the correctly obtained $S = 3340 \text{ cm/s}$. These results are summarized and expanded in Table 1.

Parameters influencing determination of G_{av}	Resulting τ_{eff} (μs)	S (cm/s) from approximate Eq. (3)	S (cm/s) calculated from full solution [6]	Remarks
EOT = 0.65, SCF = 1	7.23	1910	2020	Default EOT, default SCF
EOT = 1.05, SCF = 1	4.47	3300	3760	Correct EOT, default SCF
EOT = 0.65, SCF = 0.913	7.92	1720	1800	Default EOT, correct SCF
EOT = 1.05, SCF = 0.913	4.90	2980	3340	Correct EOT, correct SCF

Table 1. Impact of correct determination of EOT and SCF on τ_{eff} determined from photoconductance data for a nitride-coated HEM wafer. S is calculated from τ_{eff} using either the approximate Eq. (3) or the full solution to the continuity equation for exponentially decaying illumination intensity [6]. S = 3340 cm/s is the result of correctly following the three guidelines described in this paper.

6. Conclusions

This paper clarifies methods to circumvent three errors that may commonly affect the calculation and interpretation of τ_{eff} . The calculation of EOT from measured wafer reflectance and lamp irradiance has been described in this paper and illustrated by examples. The spectral correction factor and its determination are introduced in this paper to generalize the standard data analysis spreadsheet for arbitrary spectra. SCF = 0.913 for the flash lamp as a result of its deviation from the AM1.5 spectrum. While the use of SCF' = SCF \times EOT permits the accurate calculation of τ_{eff} , it must be interpreted correctly: the solution to the time-dependent continuity equation demonstrates that $1/\tau_{eff} = 1/\tau_b + 2S/W$ underestimates S by more than 25% when $S > 10000$ cm/s. An example in this paper illustrates that ignoring all three guidelines can cause an error of 40% in S inferred from lifetime data.

7. Acknowledgements

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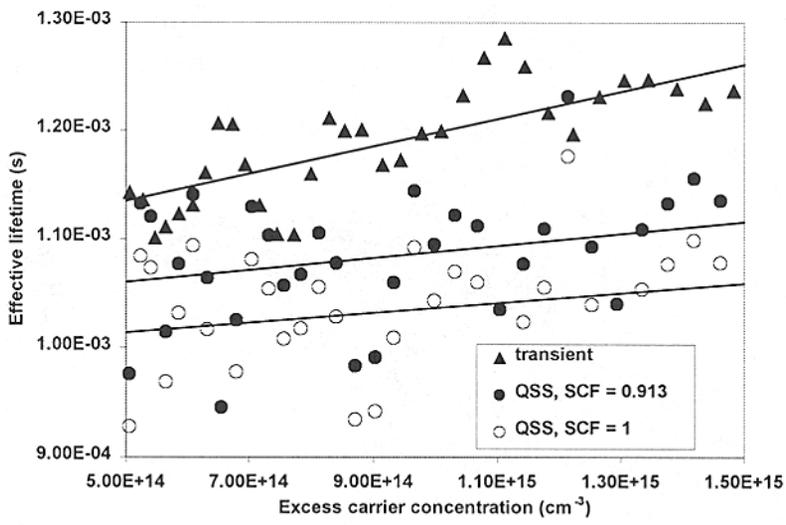


Figure 1. Improvement in the predicted agreement of transient and QSSPC lifetime data upon using $SCF = 0.913$ calculated by Eq. (8); $SCF = 1$ indicates that SCF is neglected.

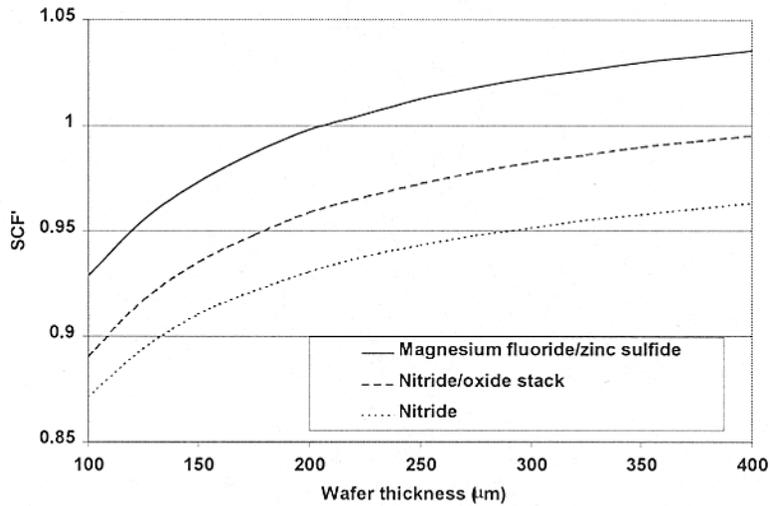


Figure 2. SCF' calculated using measured wafer reflectance, reference cell EQE, and flash lamp spectral irradiance. The value read off this figure should be used in place of EOT in the data analysis spreadsheet.

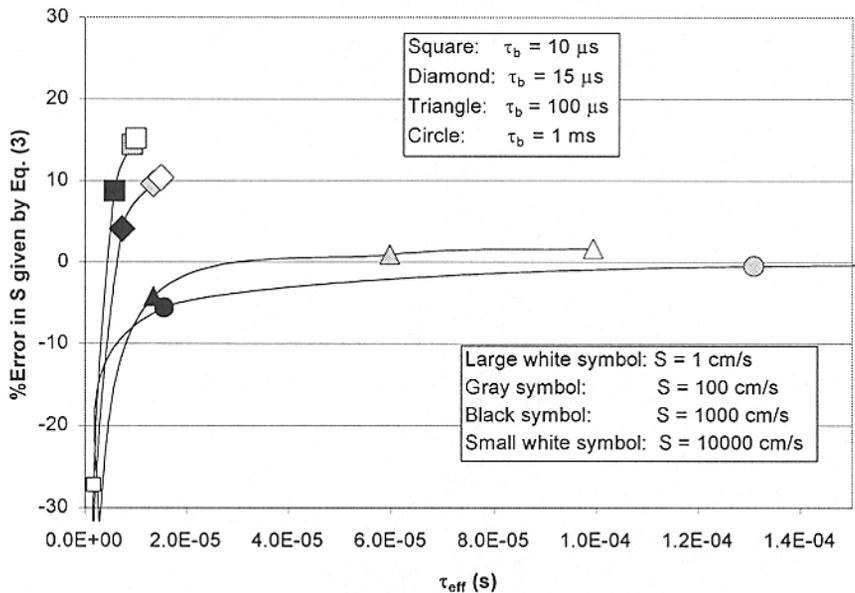


Figure 3. Percentage error in S given by Eq. (3), compared with actual S value used in accurate computation of τ_{eff} according to [6]. The parameters used include a 2.3 ms lamp time constant, $N_{ph}(\lambda)$ of the Qflash T2 lamp, $W = 300 \mu m$, $D = 30 cm^2 s^{-1}$, and $t = 2.3 ms$ after the onset of illumination.

Impact of copper on minority carrier diffusion length in p-type and n-type silicon

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Copper is one of the most common metal contaminants in silicon. The detrimental impact of copper on semiconductor devices was recognized already in 1960 by Goetzberger and Shockley [1]. However, systematic studies of the properties of copper in silicon were complicated by the lack of measurement techniques to reliably detect copper in trace concentration in silicon. Therefore, until recently, Cu in Si was much less understood than, e.g., Fe in Si. In particular, literature data on the impact of copper on minority carrier diffusion length were controversial. It was found [2, 3],[4-8] that intentional Cu contamination up to the level of 10^{11} - 10^{13} cm^{-3} had very little or no effect on the minority carrier lifetime in p-type silicon, or even improved it, whereas high copper concentrations in-

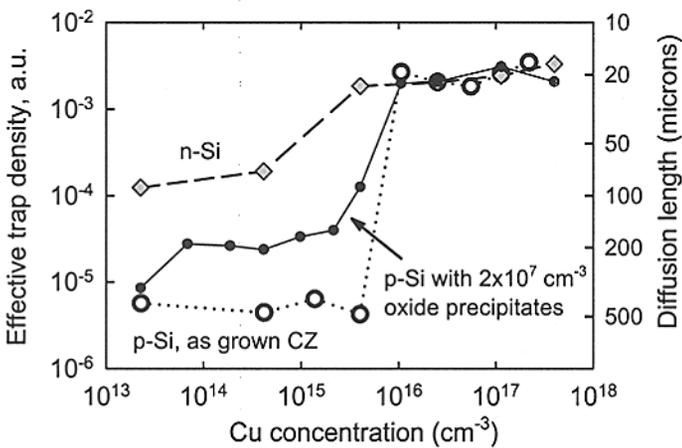


Fig. 1. Dependence of minority carrier diffusion length on Cu contamination level in 10 Ohm-cm FZ-grown n-Si samples (diamonds), and in 10 Ohm-cm p-Si, as-grown CZ (open circles) and with 2×10^7 cm^{-3} of internal gettering sites (black circles), as determined from optical precipitates profiler measurements.

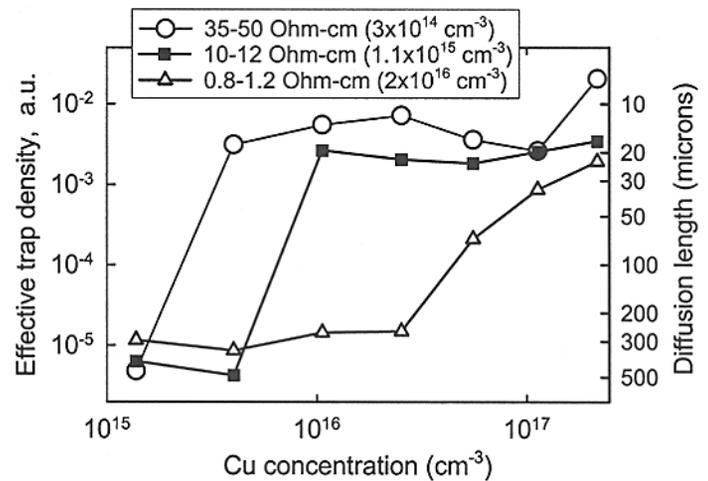


Fig. 2. Dependence of minority carrier diffusion length on Cu contamination level in p-type silicon samples with different boron doping level.

evitably led to significant degradation of minority carrier diffusion length [9]. In contrast, a strong effect of Cu on lifetime in n-Si was observed even at low Cu contamination levels [4, 10, 11]. To the best of our knowledge, a consistent explanation was suggested neither for this difference in recombination activity of copper in n-Si and p-Si, nor for its weak impact on lifetime in p-Si at low Cu concentrations.

The results of our experiments for copper diffusion temperatures between 450°C and 950°C are presented in Figs. 1-3. We found it instructive to plot the data in Figs. 1-3 against the effective density of recombination sites (left vertical axis), which is proportional to $1/L^2$, where L is the minority carrier diffusion length. This proportionality holds because according to the Shockley-Read-Hall statistics, the density of recombination centers is proportional to $1/\tau$ (assuming that there is only one

predominant type of lifetime limiting defects in the sample), whereas the minority carrier lifetime, τ , is proportional to L^2 . The corresponding values of the minority carrier diffusion length, L , are given in Figs. 1-3 on the right vertical axis.

Fig. 1 presents three curves, one for n-type silicon, and two for p-type silicon, as grown CZ and with internal gettering (IG) sites. Initially, our discussion will be confined to the curves obtained on the n-Si (diamonds) and p-Si without intentionally formed IG sites (open circles). It is seen from Fig. 1 that in n-type silicon, the effective density of recombination centers increases almost linearly with the indiffused Cu concentration, whereas in p-type silicon the effective density of recombination centers remains very low at low Cu concentrations and experiences a sharp increase at a Cu concentration of approximately 10^{16} cm^{-3} . This critical Cu concentration matches the threshold concentration of copper that has to be reached in $10 \Omega \times \text{cm}$ p-Si to start forming Cu-precipitates in the bulk, which was reported in our recent publication [12]. The existence of a threshold Cu concentration for the formation of Cu precipitates was explained as follows [12]. Precipitation of copper in the bulk of the wafer is unlikely at low copper concentrations because of the large nucleation barrier for the formation of Cu precipitates, which is due to (i) strong compressive strain, caused by large volume expansion [13] during the formation of copper silicide, and (ii) electrostatic repulsion between the positively charged Cu-precipitates and the ionized, interstitial Cu_i^+ ions [14]. Copper precipitates were shown to be positively charged in p-Si and negatively charged or neutral in n-Si [9]. The charge state of copper precipitates is determined by the Fermi level position, which depends on the concentration of shallow acceptors (boron) compensated by shallow donors (mainly interstitial copper). If the interstitial copper concentration exceeds the boron concentration, conductivity type inversion occurs. As soon as the Cu_i^+ concentration becomes sufficient for the Fermi level to exceed the electro-neutrality level of the precipitates at approximately $E_C - 0.2 \text{ eV}$ [9], the charge state of copper precipitates changes from positive to neutral or negative, and the electrostatic precipitation barrier disappears or even changes sign to attraction. In n-type silicon, a much lower Cu concentration is required to initiate nucleation of the precipitates since the Fermi level is close to the electro-neutrality level even for

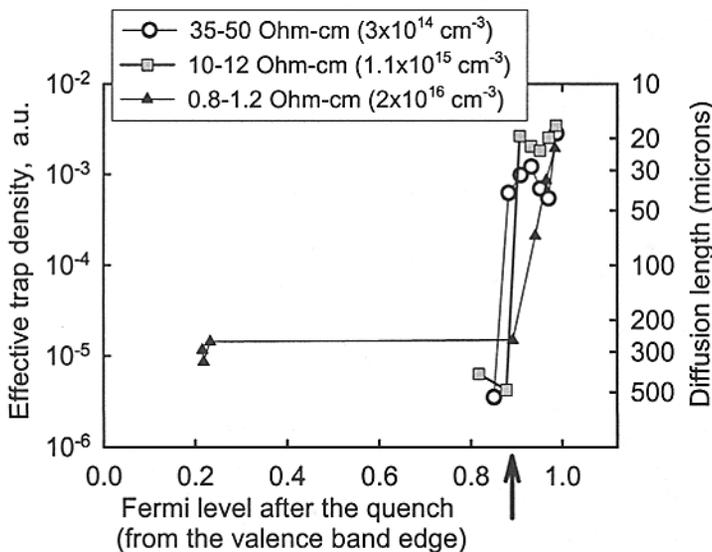


Fig. 3. The same data as in Fig.2, plotted against Fermi level position in the sample at room temperature immediately after the quench. The arrow indicates the position of the electroneutrality level of copper precipitates.

very low copper concentrations. EBIC measurements of Cu-contaminated samples indicated that Cu precipitates are very efficient recombination centers [15]. This can be explained by a combination of two factors, the positive charge of Cu precipitates in p-Si, which increases their capture cross-section for minority charge carriers, and the effective recombination of these charge carriers through the bandlike states associated with Cu precipitates [9, 14]. Therefore, it is reasonable to assume that the step in minority carrier lifetime (Fig. 1) is caused by recombination of the charge carriers at copper precipitates. These precipitates are formed at high density as soon as the Fermi level position in the sample reaches the electroneutrality level, thus reducing the total barrier for nucleation and growth of Cu precipitates.

To further test this model, we investigated the effect of Cu on minority carrier diffusion length for samples with three different resistivities (35-50 Ohm-cm ($\langle B \rangle = 3 \times 10^{14} \text{ cm}^{-3}$), 10-12 Ohm-cm ($\langle B \rangle = 1.1 \times 10^{15} \text{ cm}^{-3}$), and 0.8-1.2 Ohm-cm ($\langle B \rangle = 2 \times 10^{16} \text{ cm}^{-3}$)). This experiment enabled us to compare the minority carrier diffusion length in samples with the same starting copper concentration, but with different Fermi level position. Results are presented in Fig. 2, which shows that the position of the step in the effective density of recombination sites depends on the doping concentration. A higher concentration of Cu is required to cause the step-like transition in the effective density of recombination sites in the samples with a higher boron doping level. However, the position of the room-temperature Fermi level calculated for the moment immediately after the quench for Cu concentration corresponding the position of the step in Fig. 2 is the same for all three types of samples, see Fig. 3. This allowed us to conclude that all three samples have experienced the same dominant defect reaction. Furthermore, the defect reaction responsible for the observed step in the effective density of copper-related recombination sites most probably is the formation of copper precipitates which starts as soon as Fermi level reaches the electroneutrality level of copper precipitates.

Thus, at low copper concentrations, very few or no precipitates are formed. As discussed in our recent publication [16], complexes of interstitial copper are unstable, and outdiffusion of copper to the wafer surface is the predominant defect reaction of Cu in p-type silicon. Since only a small fraction of Cu is left in the bulk, its impact on minority carrier diffusion length is small, and may even result in passivation of electrically active defects provided that complexes of Cu with these defects are less recombination active than the original defects. However, when the critical copper concentration is reached, copper starts forming recombination active precipitates everywhere in the bulk. As these precipitates are very efficient lifetime killers, the minority carrier diffusion length decreases drastically. In n-type silicon, the Fermi level is very close to the electroneutrality level of copper precipitates, and nucleation of copper precipitates occurs much easier. Therefore, the effect of copper on minority carrier lifetime at low copper concentrations is greater in n-Si than in p-Si.

Even with this qualitative understanding, the details of the behavior of copper and its effect on diffusion length on the quantitative level may vary from wafer to wafer depending on its thermal history, concentration of lattice defects, other impurities present in the wafer, and its surface condition. It is instructive to compare two dependencies presented in Fig. 1, taken on boron-doped CZ samples with the same resistivity in the presence (filled circles) and absence (open circles) IG sites. The curve obtained on the sample with IG sites shows the same step-like behavior as the curve obtained on as-grown CZ sample, but the step is much smoother and its height is lower. This can tentatively be explained by heterogeneous precipitation of copper at lattice defects (e.g., dislocations or stacking faults) associated with the oxide precipitates, which results in a small increase in the effective trap density at sub-critical Cu concentration range between 10^{13} and 10^{15} cm^{-3} . As the Cu concentration reaches 10^{16} cm^{-3} , the effective trap density becomes approximately equal to that for as-grown CZ sample. This indicates that precipitation of Cu at oxide precipitates does not seem to be playing a significant role in determining the minority carrier diffusion length at copper concentration above the critical copper concentration.

These experiments were followed by studies of the impact of even lower concentrations of copper on minority carrier diffusion length in p-type silicon. In our experiments with copper contamination levels around $2.3 \times 10^{13} \text{ cm}^{-3}$, which corresponds to the diffusion temperature of 450°C , we observed that minority carrier diffusion length in the samples contaminated with copper was close to the diffusion length in as-grown samples, and was noticeably higher than in control samples, which were annealed and quenched at the same temperature as Cu-contaminated samples, but were not intentionally contaminated. Obviously, the decrease of diffusion length in control samples was caused

by contaminants, inadvertently introduced during sample preparation and anneal. However, the improvement in the diffusion length in Cu-contaminated samples, as compared to the control samples, can only be explained by passivation action of copper. Indeed, copper is in many respects similar to hydrogen: it is also always positively charged in silicon, and it has very high diffusion coefficient. We suggest that the passivating effect of Cu in silicon is due to the formation of complexes of Cu with the other lattice defects, which are more recombination active than their complexes with Cu. Such defects can be dislocations, punched out by oxide precipitates, or microscopic lattice defects, e.g., voids.

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Application of X-Ray Fluorescence Microprobe technique for the analysis of fully processed solar cells

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XRF studies of metal impurities in multicrystalline silicon, performed by our group in the past, involved extensive sample preparation, which included chemical cleaning of the samples and removal of a metal contact used for their pre-characterization by LBIC or EBIC. An important step of the experiment was to create markers on the sample surface to establish one-to-one correspondence between the XRF-map and the recombination activity/thermography map. Features revealed by selective etching, such as grain boundaries, and scratches on the sample surface were used as such markers. However, this involved tedious and often destructive sample preparation. Therefore, it was important to develop a procedure for analysis of impurities in fully processed solar cells without etching or scratching the samples.

In this article, we report the results obtained on solar cells fabricated at Fraunhofer Institute for Solar Energy Systems using BaySix material. The processed solar cells were square in shape with sides measuring 47 mm. This relatively small size enabled us to install the whole cell in the sample holder, although only a small area of the cell (on the order of 0.01-0.02 mm²) could be scanned within a reasonable period of time. The top grid consisted of thin contact strips made of evaporated TiPdAg, additionally electroplated with Ag, with approximately 2.2 mm between them. The cells were pre-characterized by LBIC. To analyze the distribution of metal impurities in the cells, they were installed in an XRF microprobe system, ALS beamline 10.3.1, without any preliminary surface preparation, to check whether the fluorescence map of a metal from the contact grid on the cell surface (evaporated TiPdAg, additionally electroplated with Ag) could supply sufficient features to be used to pinpoint the area of the scan and to link it to optical and EBIC micrographs.

We found that contact stripes generated a fluorescence signal, which consisted of a background signal and a number of overlapping peaks with energies of around 1.5keV (close to the K_α Al) and around 3 keV (L_α-L_β Ag). No signal was found for the most intense K_α Ti line indicating a full absorption of the radiation in the upper silver layer. L_α-L_β Ag lines interfere strongly with the Ar lines. We found that the XRF-image giving the most topographical details of the metal stripe contacts can be obtained using the spectral area around 1.5 keV, although the element which originates the signal in this area is not known precisely. Fig. 1 presents two complimentary maps with sensitivity tuned for silicon and for aluminum. The contact stripe is clearly seen, with a strong contrast between the stripe and the silicon. A dotted line in Fig. 1 schematically indicates the position of a grain boundary which we observed also in an optical microscope.

Fig. 2 is a comparison of an XRF scan of the same area of the cell as presented in Fig. 1 (note that the scan presented in Fig. 1 was taken with the sample orientation 180 degrees rotated

from its position in Fig. 2). The characteristic features (uneven edge) of the contact strip, indicated by the arrows in the XRF image, can also be clearly seen in the optical micrograph. This unambiguous correlation of characteristic features of the contact strip edges in optical and XRF maps has been successfully used in this set of experiments for locating the same area of the sample both on the XRF beamline and in the optical microscope. Interestingly, the grain boundary, which is well seen in the optical microscope, is not detectable in the XRF image.

The area of the cell mapped in Figs. 1,2 was selected using LBIC map of the whole cell, shown in Fig. 3. On the LBIC map we selected a small area which contained a defect cluster with significantly lower diffusion length than in the nearby area. The blown-up image of the cluster is shown in the upper right corner of Fig. 3. The location of this enlarged area of the solar cell on the overview LBIC map is shown by a rectangle (left-hand side of Fig.3). The image in the right bottom corner of Fig. 3 is the optical image of the area of the cell. The whole area of this optical image corresponds to the area within the rectangle on the enlarged LBIC image in the upper-right corner of Fig. 3. Finally, the area which was actually scanned by XRF, approximately 150×100 microns, is shown by a rectangle in the optical image.

The XRF map of copper distribution in this area of the cell is shown in Fig. 4; the XRF map of iron distribution in the same area of the cell is presented in Fig. 6. Fig. 5 is the energy scan of the XRF signal from copper precipitate located at the bottom of Fig. 4. This scan indicates that the precipitate consists of copper with inclusions of iron. Indeed, the location of this precipitate can also be traced as a weak contrast on the iron map, Fig. 6. Note that the two iron precipitates visible as dark spots in Fig. 6 are located in different spots than the copper precipitate.

In summary, we have demonstrated that our XRF tool is suitable for analysis of metal impurity clusters in processed solar cells without chemical etching. The metallization grid on the cell surface does not significantly interfere with the measurements and can even be used as a marker to accurately pinpoint the location of the area of interest on the cell. Our results confirm that iron and copper clusters are indeed found in low lifetime regions of solar cells. A copper precipitate was found on the grain boundary, and it was found that copper has co-precipitated with iron.

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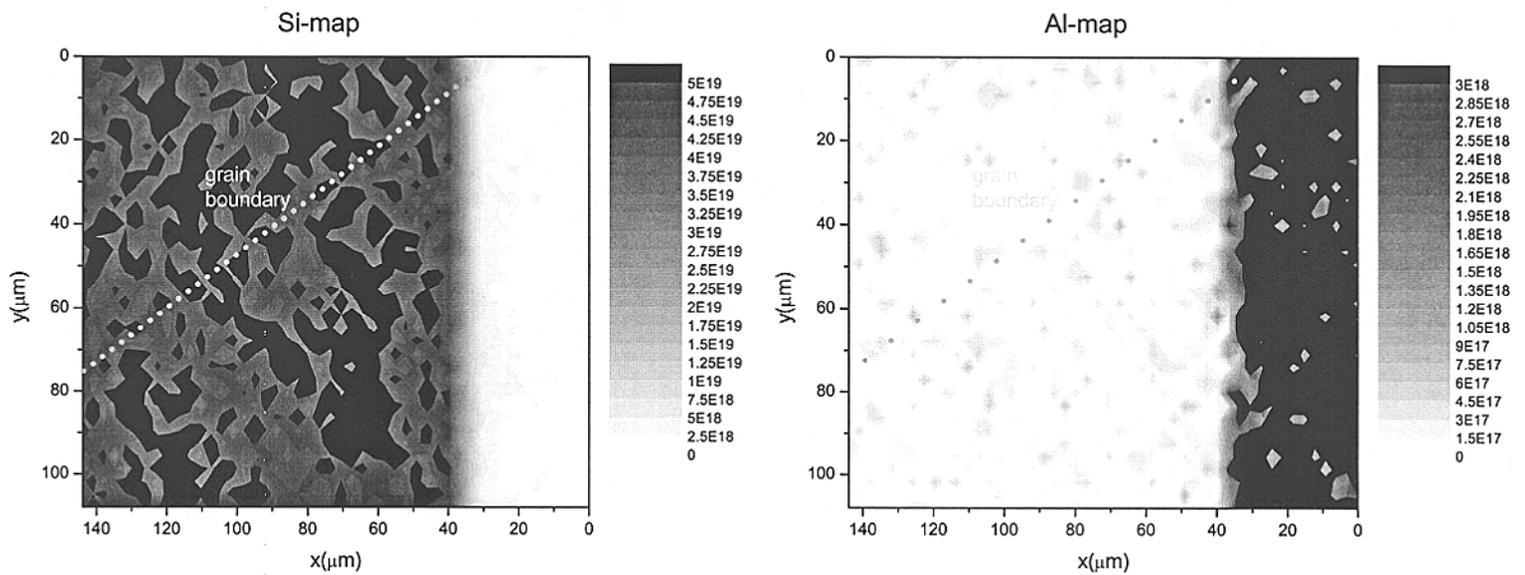


Fig. 1. XRF scans of the same area of the wafer, tuned to sensitivity to the silicon peak (on the left) and the Al peak (which strongly overlaps with numerous heavy metals constituting the contact strips). The contact strip is clearly seen. The silicon fluorescence signal under the contact strip is attenuated by the metal. A dotted line schematically represents the location of a grain boundary, which is shown in greater detail in the following figures.

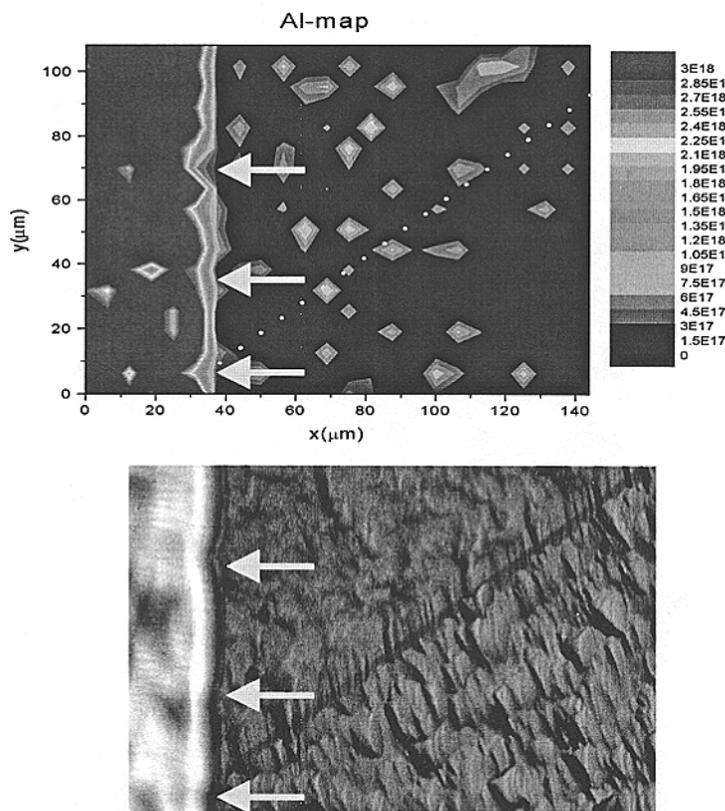


Fig. 2. Comparison of the same area of the cell imaged by XRF and optical microscopy. Features at the edge of contact stripes can easily be identified by both techniques.

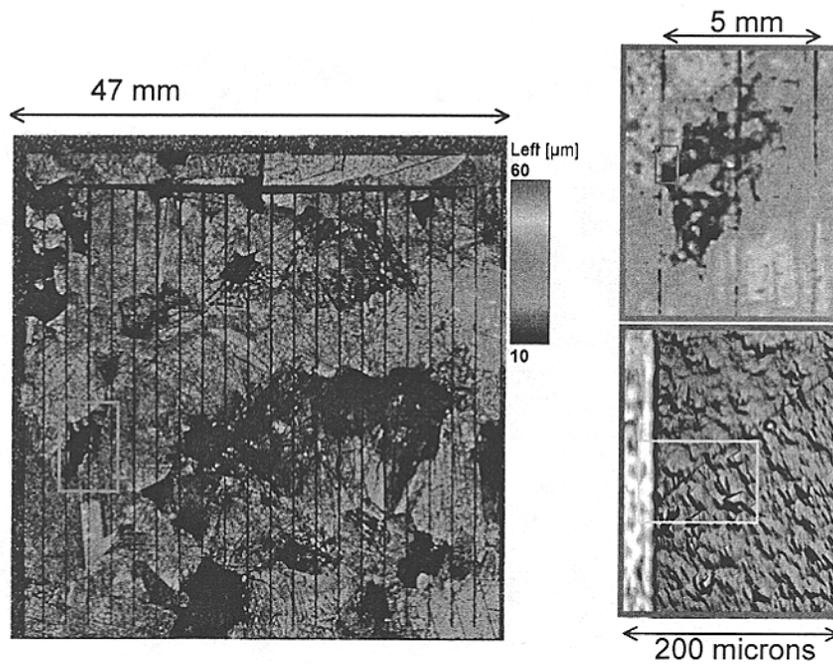


Fig. 3. LBIC image of a solar cell (on the left) with an area of local low minority carrier diffusion length shown on a large scale in the top right corner of the figure. This area is shown on a large-scale LBIC image by a rectangle, which encompasses 2,3, and 4-th contact strips from the left. The red rectangle on the blown-up LBIC image shows the boundaries of the optical image (presented in the right bottom corner of the figure). The boundary of a contact strip and a grain boundary can be well seen in the optical image. The yellow rectangle indicates the area scanned with XRF (it is the same area as mapped in Fig. 2).

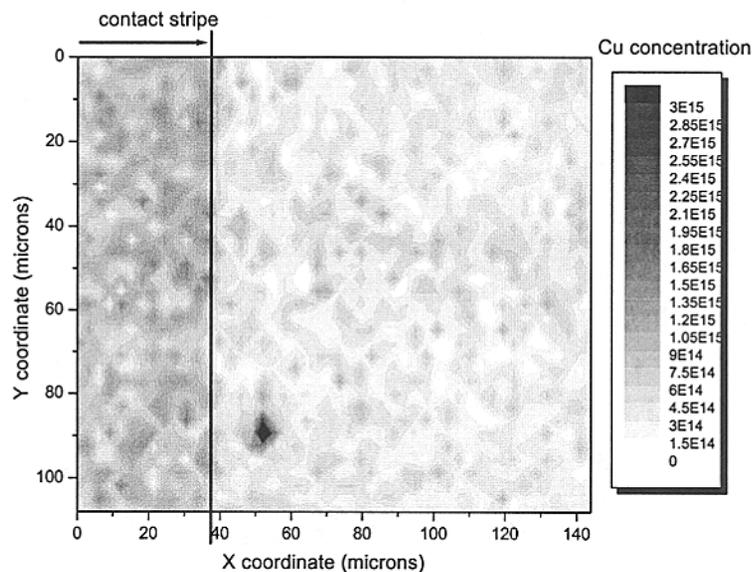


Fig. 4. XRF scan of copper distribution in the local low diffusion length area of the cell. The optical image of this area is shown in Fig. 9. A copper precipitate with a strong XRF peak was found at the location of a grain boundary.

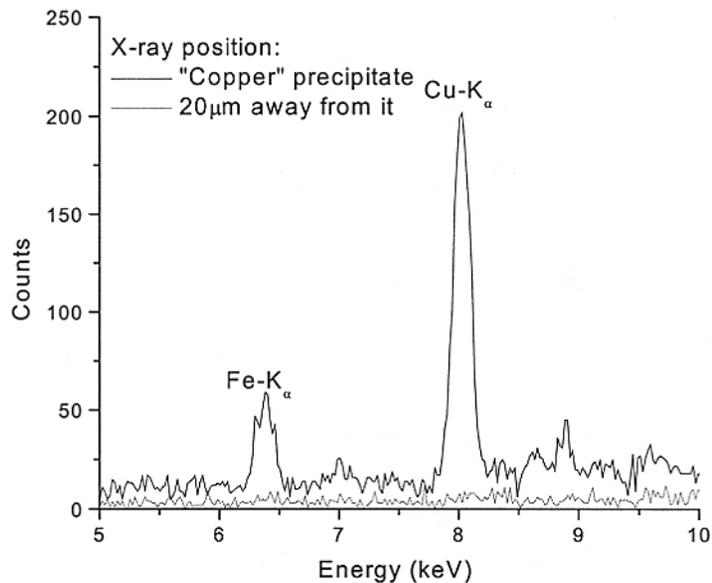


Fig. 5. Energy scan of the XRF signal from the copper precipitate identified in Fig. 4 showed that copper has co-precipitated with a small amount of iron. A red line illustrates the background signal, measured at an arbitrary location about 20 microns away from the Cu precipitate.

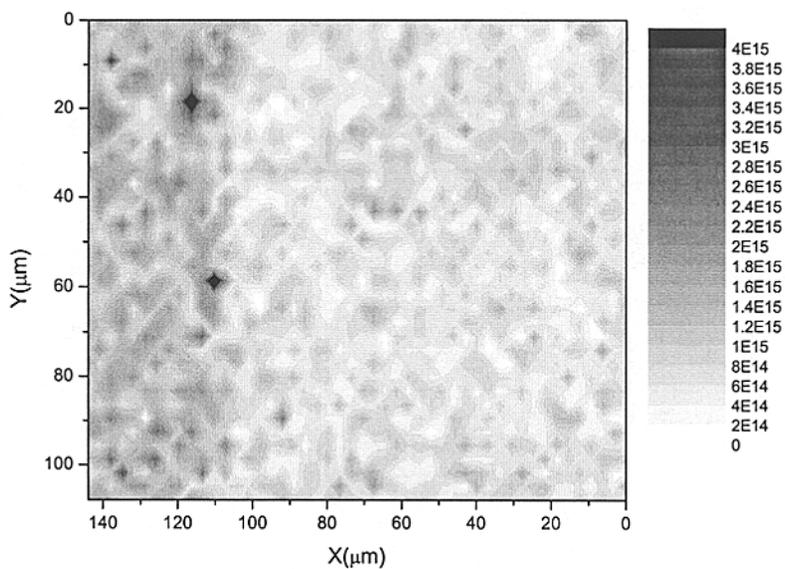


Fig. 6. XRF scan of iron distribution in the local low diffusion length area of the cell. The mapped area is identical to that presented in Fig. 5. The optical image of this area is shown in Fig. 3. Two iron precipitates are found in the area away from the grain boundary. The location of copper precipitate visible in Fig. 3, which, as follows from Fig. 4, also contains some iron, can be seen in this figure as a weak green contrast at the same spot as in Fig. 3.

Scale-up of the CSI B-Removal Process for the Production of Solar Grade Silicon

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ABSTRACT

A simple process to remove boron (B) from molten silicon has been developed. With this approach, B has been reduced to 0.3 ppma, using commercially-available, as-received metallurgical grade (MG) silicon, and has been reduced by several orders of magnitude in heavily B-doped electronic grade silicon scrap. Based on specific mechanisms for B removal, the parameters for scale-up of simple moist gas blowing through a molten silicon bath (CSI B removal process) have been applied in increasing charge size. The charge size was successfully scaled up from 1 kg to > 150 kg, with the best results fitting the same scaling law parameters. However, limitations to the simultaneous application of flow, lance depth, and melt surface area limited the scale-up to 50 kg with the most optimum parameters. Larger melts were processed at a lower than optimum surface area-to-volume ratio, due to limitations of the present modified crystal growth furnace. Methods for maintaining the optimum parameters at larger charge sizes are discussed. The target of 1 ppma B from 60 ppma MG silicon is achievable in 6 hours of refining.

INTRODUCTION

The photovoltaic (PV) industry is going through rapid growth; annual worldwide production of PV modules is projected [1,2] to grow to 18 GW by 2020 from <0.3 GW in 2000 [3]. Consensus indicates that such growth will cause demand to outstrip supply of PV silicon meltstock. Currently, excess capacity, rejects and scraps from the semiconductor industry are being used as feedstock. Metallurgical grade (MG) silicon with purity levels of <99.5% is produced in very large quantities at low cost. The high impurity levels do not allow it to be used as feedstock for production of solar cells. The predominant impurities are Al (1200-4000), Fe (1600-3000), Ti (150-200) and Ca (600) ppma. The boron (B) and phosphorus (P) levels are generally not analyzed, but are in the 20-60 ppma range. Except for B and P, most impurities have a segregation coefficient of 10^{-5} ; for Al it is 10^{-3} . Therefore, most impurities except B and P can be easily removed by directional solidification. To produce solar grade (SoG) silicon feedstock, a directional solidification step is an effective step for purification of most impurities. Since the MG silicon will be melted, it will be desirable to reduce B and P by refining in the molten state and follow it with directional solidification. It is necessary to develop an upgrading process in the molten state which is focused on removal of B and P, and follow the refining by a directional solidification step.

Several approaches have been pursued to produce additional sources of feedstock from MG silicon, but none of these processes are commercialized because they could not economically remove B and P from the MG silicon. Recently, the only major effort pursued to upgrade MG silicon for PV applications was by Kawasaki Steel Corporation supported by NEDO in Japan. This process involved reduction of P from high purity molten MG silicon by e-beam melting under vacuum followed by a first directional solidification step, then remelting, followed by B reduction of molten silicon with Ar plasma and water vapor, and finally a second directional solidification step to produce SoG silicon [4]. Kawasaki Steel Corporation showed that such material could be used for PV applications and a pilot production facility was set up to demonstrate the process [5]. However, the combination of e-beam melting, vacuum operation, Ar plasma, and several directional solidification steps may make it a high cost approach.

In contrast, the CSI process is to melt commercially available MG silicon, reduce impurities (with special consideration for reducing B and P) in a refining step, and then directionally solidify the silicon. This PVMaT-supported program built on previous work at CSI [6], and achieved significant reduction of impurities on charge sizes ranging from 1 to 150 kg, and included processing of charge sizes up to 300 kg. In particular, the program

achieved a B reduction in MG silicon to 0.3 ppma, P was reduced to ~ 7 ppma, and most other impurity elements have been reduced to levels of < 0.1 ppma.

B and P were early identified as the main problematic components needed to be reduced during the pyrometallurgical refining stage, as the balance of components that were left after pyrometallurgical refining were shown to be efficiently removed by directional solidification. Of the two, B is the most problematic because of its unfavorable segregation coefficient (0.8), and because it is not as likely as P to be removed by vacuum processing, slagging, etc. Attention was focused on B removal via moist reactive gas blowing [7].

Later in this program, after the B removal process was well defined, a potential new source for SoG silicon was identified – namely, heavily B-doped electronic-grade silicon scrap from the semiconductor industry [8]. So far, this material could not be used as feedstock for PV because of very high B-doping. The CSI process was applied to this heavily B-doped electronic-grade silicon scrap source, and B was reduced by several orders of magnitude. This paper discusses issues arising from the scale-up from 1 kg to > 150 kg of this process for removing B from MG and heavily B-doped electronic-grade silicon scrap.

INITIAL WORK

The CSI B-removal process involves melting commercially-available MG silicon or heavily B-doped electronic-grade silicon scrap under vacuum, then refining using moist gases through a lance on the surface of molten silicon (with emphasis on B and P removal) followed by directional solidification. Parameters that were identified at the start of the program as being of potential significance included chemical composition of the main reactive gas component, moisture content, bath temperature, active surface area of melt (accounting for slag coatings of surface), melt depth, melt stirring, lance height, lance diameter, gas flow velocity, and the specific utilization factor (flow rate/mass of melt). Initial runs were made on a 1 kg scale to evaluate the potential mechanisms for B removal. After several scoping experiments at 1 kg, the process was transferred to a modified Heat Exchanger Method crystal growth furnace (Figure 1). The HEM furnace is used in the production of silicon ingots and gives good directional solidification – an attribute that is very effective at removing most impurities from MG silicon.

During the 1 kg scoping runs, the importance of temperature and gas chemistry was made clear. Also, it was found that for a given set of processing parameters, the kinetics of B removal were first order with respect to the B concentration in the silicon, or [B]. That is, the rate of reduction of B is proportional to [B] at any given time. This is the expected relationship for this dilute solution of B in the melt and in the vapor, where the activity in both phases is directly proportional to [B], and is expressed as

$$\frac{d[B]}{dt} = -k[B] \quad (1)$$

where k is the equilibrium constant; rate expression can be integrated to yield concentration as function of time:

$$[B] = [B^{\circ}]e^{-kt} \quad (2)$$

where $[B^{\circ}]$ is the B concentration at the beginning of processing. It has been found to be convenient and illustrative to express the empirically derived rate constants in terms of a half-life, $t_{1/2}$, that is, the time needed to reduce [B] in half. This is solved for in terms of the [B], $[B^{\circ}]$ and t data by noting that

$$\log\left(\frac{[B]}{[B^{\circ}]}\right) = -2.303(kt) \quad (3)$$

and that when the half-life condition is fulfilled

$$\log\left(\frac{1}{2}\right) = -2.303(kt_{1/2}) \quad (4)$$

Dividing 3 by 4, and rearranging results in the half-life parameter:

$$t_{1/2} = kt \frac{\log\left(\frac{1}{2}\right)}{\log\left(\frac{[B]}{[B^0]}\right)} \quad (5)$$

In order to scale-up the process, a HEM furnace was modified to allow reactive gas processing. Figure 1 shows a standard HEM furnace used for all experiments of > 1 kg in this program. Figure 2 shows in schematic form the modifications made to allow the safe processing of reactive gases but retain the effective directional solidification aspects of the HEM technology. Although this furnace allowed significant progress to be made in developing and scaling up the process, various aspects of the furnace did not allow the unlimited scale-up of the charge to maximum size and still allow the optimum combination of refining.

In the course of the scale-up, numerous operational parameters that limited the effectiveness of the B refining included the formation of slag coatings, lance accretion formations, bath skulling, reflux of recondensed B, and excessive splashing of silicon out of the crucible.

Because the operational issues were often of a complicated nature, the operating envelope needed to be identified individually at each scale-up step. This is reflected in Figure 3, which shows the B half-life versus charge size. The scatter to the higher values reflects overcoming the operational parameters mentioned above, and the experiments needed to identify the operating envelope that resulted in the best values achievable with the present furnace design.

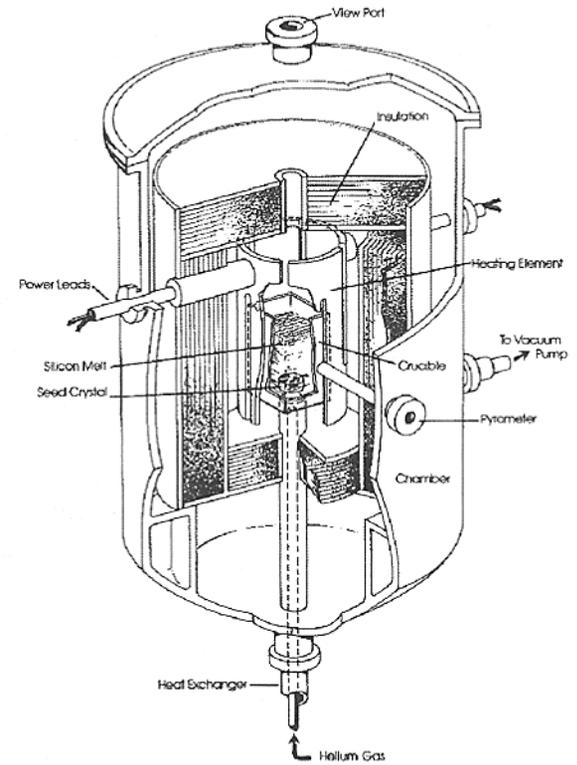


Figure 1. A schematic of the HEM furnace. A similar furnace was modified to allow the molten state refining of MG and heavily B-doped electronic-grade silicon scrap.

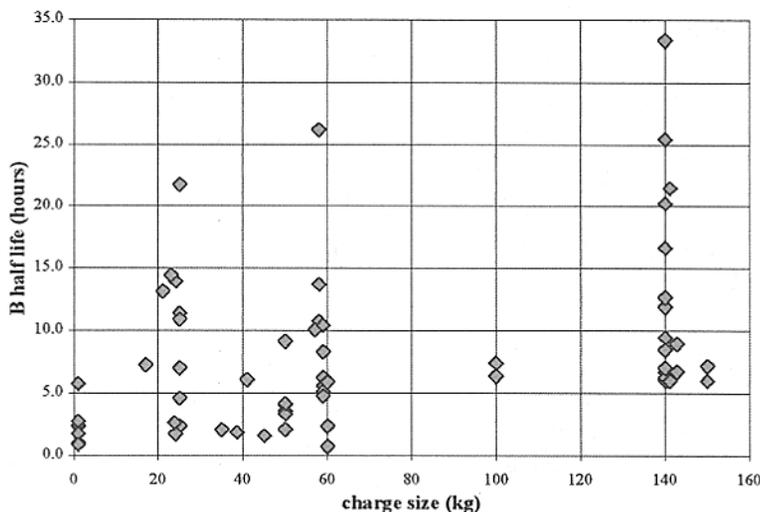


Figure 2. B half-life versus MG silicon charge size.

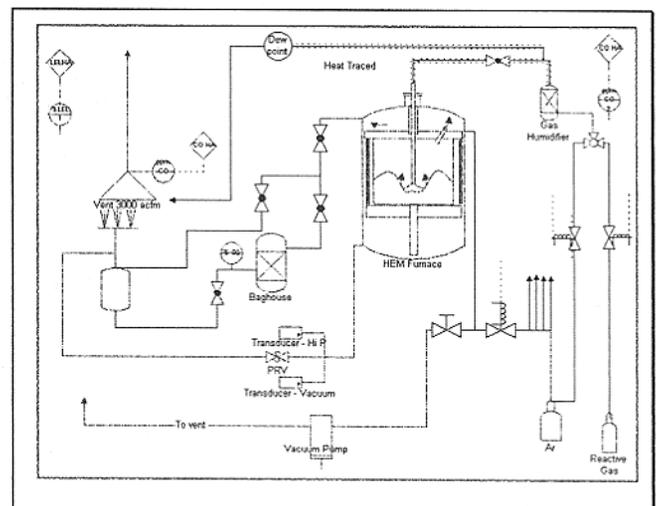


Figure 3. Schematic of modified HEM furnace for refining MG silicon.

In order to determine the most important scaling parameters, these data were sorted to eliminate data with operational problems. The non-scaling effect of temperature was accounted for in the resulting Figure 4, which shows these B half-life data plotted for each charge size against refining temperature. It is clear from these data that the rate of B removal is strongly dependent on temperature, but is independent of charge size between 1 and 50 kg, and between 100 and 150 kg. Data for 100 and 150 kg charge sizes was for a limited temperature range. The curve connecting the best values for the 1 and 50 kg scales is clearly different from the best results between 100 and 150 kg.

During these experiments, many experimental parameters were varied at each charge size to delineate the mechanisms of B removal and the scaling parameters. For instance, over the range of flows used, the rate of removal was found to be nearly independent of flow. However, as is apparent in Figure 4, some parameter was not scaled appropriately, resulting in two different trends. Above 50 kg, the only important parameter that could not be scaled up in the present furnace is the active surface area-to-volume ration. Because of the need to avoid excessive splashing of molten silicon in this furnace, only impinging flows were used. The active surface area is thus the melt surface area, defined by the crucible area, and the active surface area-to-volume ratio is simply the melt depth. As the melt sizes were scaled to greater than 60 kg, the melt depth increased. This effect is shown in Figure 5, where the rates are normalized to the surface area-to-volume ratio. This normalization moves the > 100 kg data to lie on the same trend as the 1 and 50 kg sizes, indicating that all of these data follow the same scaling law. The temperature effect is of the expected magnitude predicted by thermodynamic modeling of the gas/liquid interface responsible for the B removal.

SCENARIO FOR LARGE SCALE PRODUCTION

This experimental process resulted in a half-life of approximately two hours for a 50 kg MG silicon charge. A similar experiment was done with 50 kg of heavily B-doped electronic-grade silicon scrap with B concentration approximately 4 to 10 times that of MG silicon. A similar half-life was obtained. This refined material was used as feedstock for the Float Zone (Fz) and Czochralski (Cz) crystal growth and evaluated for solar cell performance. Test solar cells fabricated at NREL demonstrated 7.3%, 12.5% and 13.4% efficiency for as-received, Fz and Cz grown crystals using this refined material [9]. In the semiconductor industry, large amounts of heavily B-doped material are available as scrap that cannot be utilized in its present form by the PV industry. The combination of availability of this surplus material and the B-removal process developed could be exploited to become an additional source of silicon feedstock available to the PV industry to produce about 200 MW of modules on an annual basis.

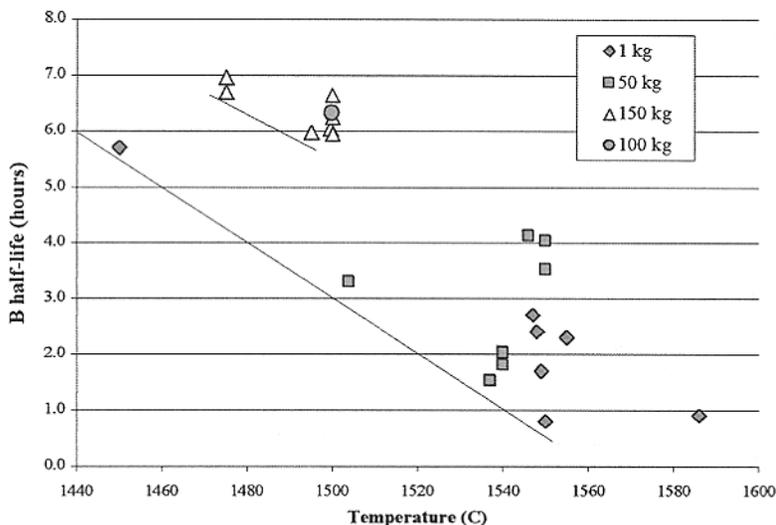


Figure 4. Half-life vs charge size showing best results lying on a single trend for 1 to 50 kg, and a second trend for 100 – 150 kg.

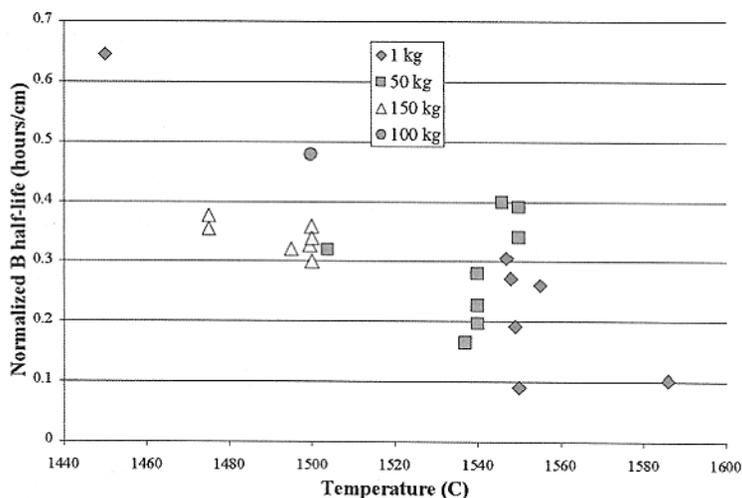


Figure 5. Normalized half-life vs temperature for results various charge sizes. The points represent data from 1 to 150 kg charges.

Present work shows that the best rates of B removal achieved so far are independent of the flow but are affected by the surface area-to-volume ratio of the melt, and the temperature. It is well established in the metallurgical industry that increased splashing and vigorous gas flow can enhance gas/liquid reaction rates. Numerous ways in which this can help remove B from silicon include increasing the surface area-to-volume ratio of the melt by injecting gases in bubbling mode, either through a submerged lance or using a porous plug gas diffuser. The lance diameter is another parameter that can have significant effects during submerged injection. This has the effect of increasing the gas residence time and maximizing the surface area of the gas in contact with the melt.

Another important parameter that will clearly enhance the rate of B removal is increased temperature. At MG silicon plants, the MG silicon is typically tapped at temperatures exceeding 1600°C. It is envisioned that one route to upgrading MG silicon to SoG silicon is to process tapped molten MG silicon at these elevated temperatures at the MG silicon plant, thus minimizing the time needed for B removal and the energy and time associated with the remelting MG silicon for refining. This approach will further simplify the production of SoG silicon, reduce costs and improve quality of the product.

By maintaining a high active surface area-to-volume ratio, stirring of the bath, and by processing at high temperature, the expected B half-life will remain low as the charge size is scaled up. Figure 6 shows the calculated time dependent removal of B from a 500 kg charge using two different B contents corresponding to MG silicon with 20-60 ppma B (60 ppma used), and highly doped electronic grade silicon with 50-400 ppma (400 ppma B used). These calculations assume the scale-up has been such to achieve the 1 hour half-life on the 500 kg scale. The target of 1 ppma is reached in less than 6 and 9 hours, respectively. Lower values of B can be achieved by extending the processing time.

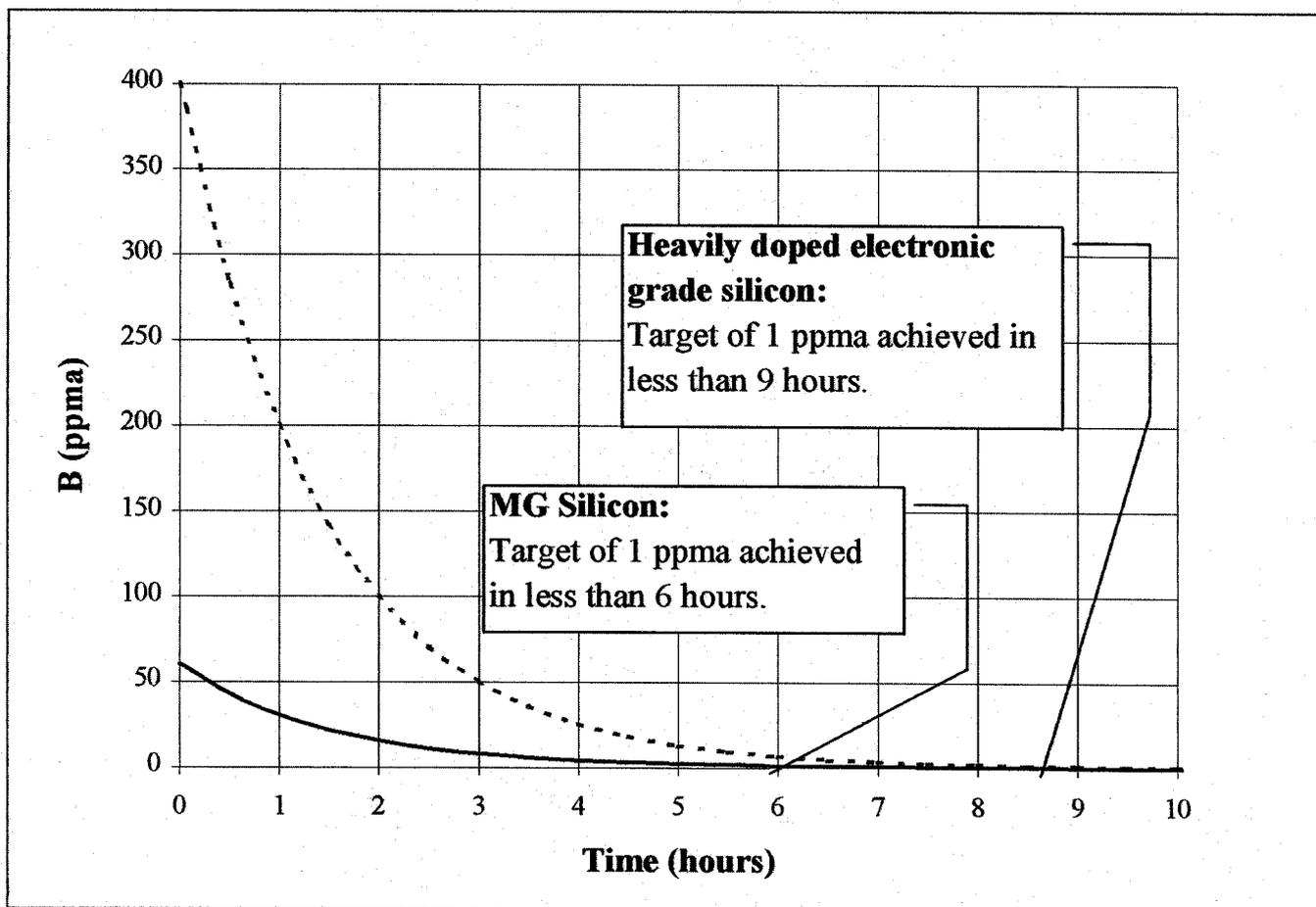


Figure 6. Time dependent removal of B from two different initial B concentrations, corresponding to MG silicon and heavily B-doped electronic-grade silicon scrap. The target of 1 ppma is reached in from <6 to < 9 hours when the processing is done in a way to achieve the 1 hour half-life for B.

CONCLUSIONS

Development of SoG silicon feedstock is the most important problem facing the PV community so that the projected growth of the industry can be maintained. The most direct approach is to upgrade MG silicon so that a nearly inexhaustible supply of feedstock can be developed and the dependence on the electronics industry is curtailed. The goal of the present program was to upgrade commercially-available MG silicon by reducing B and P in the molten state followed by directional solidification. The refining procedures developed included reaction with moisture, gas blowing, slagging, etc., consistent with processes used in an MG silicon production plant. Refining from 1 to 150 kg charge sizes showed that a simple moist gas blowing operation reduced the B level from 20-60 ppma to < 0.3 ppma and the P level from 20-60 ppma to < 8 ppma. Other impurities were reduced to below 0.1 ppma.

The scaling parameters were analyzed. In particular, the surface area-to-volume ratio of the melt and the temperature has been found to be very important to the efficient application of this process. These variables may be easily maintained at their optimum value by appropriate changes in furnace design. The CSI B-removal process developed is consistent with the facilities in an MG silicon production plant. Therefore, it is transferable to the MG silicon plant for large-scale manufacture of SoG silicon.

The CSI B-removal process was also tested on low-cost silicon scrap available from the semiconductor industry that contained significantly higher B concentration, 50-400 ppma. This material represents a new supply of silicon feedstock for the short term by application of the CSI B-removal process.

ACKNOWLEDGMENT

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In this work a diagram method is presented for investigation of recombination processes through defects. It is suggested that the defects do not influence each other directly, e.g. do not exchange by free carriers. There are no other limitations related to the material or origin of the defects.

Traditional method is based on numerical solution of the system of kinetic equations, describing behavior of the ensemble of the defects, taking part in generation-recombination processes and inter-center transitions at free carrier injection, illumination etc. It has been shown that the presented diagram method is an alternative method for finding the non-equilibrium stationary distribution function F_i of the defects on states and the temp of generation-recombination transitions. It is based, on one hand, on possibility of presentation of the set of quantum states of the defect and the allowed transitions between them in natural schematic form, being in principle a graph. On the other hand, it is based on the deep informal relation between structural features of the allowed transition scheme of a defect and possibility to find it in one or another state, i.e. relation with distribution function of the ensemble of defects. Note that in the traditional approach this relation remains in a shadow. It has been shown that due to these relations the graph theory, having a well developed apparatus of combinatorial and structural analysis, is an ideal instrument for solution of the carrier recombination problem: many establishments and problems of the theory of recombination phenomena are perfectly formulated in the diagram method and are completely solved by the visual graphical constructions avoiding solution of any system of kinetic equations. Particularly, the stationary non-equilibrium distribution function can be constructed using a set of all rooted oriented trees covering the state digraph G , and temp of generation-recombination transitions can be built with the aid of all functional graphs covering G .

It is well known that the traditional analysis of the kinetics of defects with many states and complicated system of permitted transitions is accompanied by some difficulties related to numerical simulations, which makes up the researcher to simplify the transition scheme neglecting those of them characterized by relatively small probabilities. However, it may lead to losing of some important features of the defect. In the theory of dynamical systems this phenomenon is known as a problem of structural stability of the models. This problem can be easily solved within the diagram method.

Combination of practicality and universality of the method allows one to hope that it shall be a useful tool for investigation of recombination processes.

1. Introduction

Investigation of recombination processes through defects is one of the important problems at present. Traditionally theoretical investigation of these processes is based on solution of the system of kinetic equations, describing behavior of the ensemble of the defects. This approach is useful when studying the simple defects. However if the defect have many states and complicated system of permitted transitions then the traditional approach meet some difficulties related to numerical simulations, which makes up the researcher to simplify the transition scheme neglecting those of them characterized by relatively small probabilities, which may lead to losing of some important features of the defect. The latter is known as the problem of structural stability of the models in the theory of dynamical systems.

In this work a diagram method of investigation of recombination processes through defects is presented, which is based on possibility of presentation of the set of quantum states of the defect and the allowed transitions between them in natural schematic form and on the deep informal relation between structural features of the allowed transition scheme of a defect and possibility to find it in one or another state. Stationary non-equilibrium distribution function has been constructed using a set of all rooted directed trees covering the state digraph G , and net rate of generation-recombination transitions has been built with the aid of all functional graphs covering G . The problem of structural stability of the recombination problem can also be easily solved within the diagram method.

2. Digraph of states

Let the defect can be in either of the M possible quantum states forming a set $\{|i\rangle\}_{i=1}^M$. Origin of the defects and their states can be various: they can involve impurity atoms and intrinsic defects; they can be point defects and number of their charge states is not limited; quantum states may be basic or excited, different configurations of the defect, different states of the atomic multiplets, or electron-hole pairs bound to the defect, etc. Mechanisms of permitted transitions between the defect states can also be arbitrary. However, it is important, that the defects must not effect each other directly neither by strong field (electric, magnetic, mechanical stresses), nor by carrier exchanges due to tunneling.

Within the proposed diagram approach each of the defect state $|i\rangle$ is putted in accordance to the i -th vertex of the digraph G and each permitted transition from the state $|i\rangle$ to the state $|j\rangle$ is denoted by the arc $i \rightarrow j$. The latter is ascribed a weight ω_{ij} , which is equal to the probability of the transition per unit time. The digraph constructed by this way, visually reflecting all characteristics of the defect, is called the digraph of states G . For example, Fig. 1 shows digraph of states G of a bistable defect, which can be in two different configurations K_1 and K_2 . In each of the configurations the defect can be in two different charged states q_0 and q_1 , where q_0 corresponds to defect state without an electron and $q_1 = q_0 - 1$ corresponds to that with an additional electron. Many double defects in silicon such as Fe_iAl_s , Fe_iGa_s , Fe_iIn_s , B_iO_s [1,2] are of this type of bistable defects. The transitions $1 \leftrightarrow 3$ and $2 \leftrightarrow 4$ corresponds to transformations of configuration of the defect with conservation of its total charge, while those $1 \leftrightarrow 2$ and $3 \leftrightarrow 4$ are accompanied by recharging of the defect without changes of configuration. The other possible transitions $1 \leftrightarrow 4$ and $2 \leftrightarrow 3$, which would be accompanied by transformation of both configuration and charge, have been neglected. Each of the arcs $i \rightarrow j$ in the figures 1 to 3 have been marked by corresponding weight ω_{ij} , which for non-degenerate case and when the Auger effects are neglected have the form

$$\omega_{12} = C_n^{12} n + E_p^{12}, \quad \omega_{21} = C_p^{21} p + E_n^{21}, \quad \omega_{34} = C_n^{34} n + E_p^{34}, \quad \omega_{43} = C_p^{43} p + E_n^{43}. \quad (1)$$

Here n and p are the concentrations of free electrons and holes, $C_{n,p}^{ij}$ and $E_{n,p}^{ij}$ are the specific probabilities of carrier capture by the defect and of emission from the defect level into the allowed bands.

Probabilities of configurational transitions ω_{13} , ω_{31} , ω_{24} and ω_{42} are defined by mechanisms resulting in the jumping of the defect's components between different positions in the crystal lattice.

3. Non-equilibrium distribution function

Kinetics of distribution of the defects on their states are described by the system of equations

$$(a) \quad \dot{N}_i = -\left(\sum_{j \neq i} \omega_{ij}\right)N_i + \sum_{j \neq i} \omega_{ji}N_j \quad (i=1 \dots M), \quad (b) \quad \sum_{i=1}^M N_i = N_{\text{tot}}, \quad (2)$$

where N_i is the concentration of the defects in i -th state, N_{tot} is the total concentration of the defects. Distribution function of the defects on their states gives portion of the defects corresponding to each of the states $F_i = N_i / N_{\text{tot}}$, and at stationary conditions it is described by the system of equations

$$(a) \quad -\left(\sum_{j \neq i} \omega_{ij}\right)F_i + \sum_{j \neq i} \omega_{ji}F_j = 0 \quad (i=1 \dots M), \quad (b) \quad \sum_{i=1}^M F_i = 1. \quad (3)$$

Solution of the system of equations can be found, without solving the system, directly from the digraph of states G . For this aid one should find first all directed trees $\{T_\alpha^{(i)}\}$ covering G and rooting into vertex i , for every $i=1 \dots M$. Definition and properties of such trees is given in [3]. Then the weight $[T_\alpha^{(i)}]$ of each tree $T_\alpha^{(i)}$ can be found by multiplying the weights of all arcs entering into it (4a), which allows one to find the tree-weight $[i]$ of every vertex i by summing the weights of all the trees rooting into the corresponding i -th vertex (4b). At last, a portion F_i of the defects in the state i ($i=1 \dots M$) will be equal to the relative portion of the tree-weight $[i]$ of i -th vertex from the total weight of all vertexes of digraph G (4c):

$$(a) \quad [T_\alpha^{(i)}] \equiv \prod_{j \rightarrow k \in T_\alpha^{(i)}} \omega_{jk}, \quad (b) \quad [i] \equiv \sum_{\alpha} [T_\alpha^{(i)}] \quad (i=1 \dots M), \quad (c) \quad F_i = \frac{[i]}{\sum_{j=1}^M [j]} \quad (i=1 \dots M). \quad (4)$$

For example, four covering directed trees $T_{1 \dots 4}^{(1)}$ [Fig. 2(a)] grow into the 1-st vertex of the digraph G [Fig. 1] with weights $[T_1^{(1)}] = \omega_{34}\omega_{42}\omega_{21}$, $[T_2^{(1)}] = \omega_{31}\omega_{42}\omega_{21}$, $[T_3^{(1)}] = \omega_{31}\omega_{43}\omega_{21}$, $[T_4^{(1)}] = \omega_{31}\omega_{43}\omega_{24}$. Hence, the tree-weight of the vertex 1 is $[1] = \omega_{34}\omega_{42}\omega_{21} + \omega_{31}\omega_{42}\omega_{21} + \omega_{31}\omega_{43}\omega_{21} + \omega_{31}\omega_{43}\omega_{24}$. On four oriented directed trees grow into each of the other three vertexes of the digraph G [Fig. 2 (b-d)]. One can believe that these vertexes have the following tree-weights: $[2] = \omega_{12}\omega_{42}\omega_{34} + \omega_{31}\omega_{12}\omega_{42} + \omega_{43}\omega_{31}\omega_{12} + \omega_{13}\omega_{34}\omega_{42}$, $[3] = \omega_{12}\omega_{24}\omega_{43} + \omega_{42}\omega_{21}\omega_{13} + \omega_{21}\omega_{13}\omega_{43} + \omega_{13}\omega_{24}\omega_{43}$, $[4] = \omega_{12}\omega_{24}\omega_{34} + \omega_{31}\omega_{12}\omega_{24} + \omega_{21}\omega_{13}\omega_{34} + \omega_{13}\omega_{34}\omega_{24}$. Then the components of the distribution function can be written by (4c) as:

$$\begin{aligned} F_1 &= (\omega_{34}\omega_{42}\omega_{21} + \omega_{31}\omega_{42}\omega_{21} + \omega_{31}\omega_{43}\omega_{21} + \omega_{31}\omega_{43}\omega_{24}) / D, \\ F_2 &= (\omega_{12}\omega_{42}\omega_{34} + \omega_{31}\omega_{12}\omega_{42} + \omega_{43}\omega_{31}\omega_{12} + \omega_{13}\omega_{34}\omega_{42}) / D, \\ F_3 &= (\omega_{12}\omega_{24}\omega_{43} + \omega_{42}\omega_{21}\omega_{13} + \omega_{21}\omega_{13}\omega_{43} + \omega_{13}\omega_{24}\omega_{43}) / D, \\ F_4 &= (\omega_{12}\omega_{24}\omega_{34} + \omega_{31}\omega_{12}\omega_{24} + \omega_{21}\omega_{13}\omega_{34} + \omega_{13}\omega_{34}\omega_{24}) / D, \end{aligned} \quad (5)$$

where the denominator D equals to the sum of nominators of the four fractions. Some of the probabilities ω_{ij} are given in (1).

4. Stationary rate of the generation-recombination processes

The net rate of generation-recombination transitions at stationary state can be considered as the resulting rate of exchange by electrons between the defect levels and the conduction band or that of by holes between the defects and the valence band per unit volume:

$$U = \sum_{i=1}^M \sum_{j \neq i} N_i \omega_{ij} \nu_{ij}, \quad (6)$$

where ν_{ij} is the mean number of electrons transferred from the conduction band into the defect, transforming the latter from the state $|i\rangle$ into the state $|j\rangle$. Note that $\nu_{ij} > 0$, if number of the conduction band electrons decreases because of the transition, $\nu_{ij} < 0$ if it increases and $\nu_{ij} = 0$ if it does not change. It should be noted that only the mean values ν_{ij} must be used in (6), because any of the transitions of the

defect $|i\rangle \rightarrow |j\rangle$ can occur by different mechanisms characterized by their own probabilities $\tilde{\omega}_{ij}$ and numbers of electrons $\tilde{\nu}_{ij}$ captured by the defect from the conduction band or emitted to it. Certainly, the total probability of the transition ω_{ij} equals to the sum of the probabilities $\sum \tilde{\omega}_{ij}$ corresponding to all of the mechanisms. Then mean numbers ν_{ij} , evidently, can be found by formulas

$$\nu_{ij} = \frac{\sum \tilde{\omega}_{ij} \tilde{\nu}_{ij}}{\omega_{ij}}. \quad (7)$$

The summation in the numerator is carried out over all possible channels of the transition $|i\rangle \rightarrow |j\rangle$. Note that distinct from the integer quantities $\tilde{\nu}_{ij}$, the mean value ν_{ij} can be not integer.

To illustrate the above discussion, let us consider ionization of a donor $|1\rangle \rightarrow |0\rangle$ transferring of its electron either to the conduction band with probability $\tilde{\omega}_{10} = E_n$, or to the valence band with probability $\tilde{\omega}_{10} = C_p p$. In the first case number of electrons in the conduction band increases to 1, so for the channel one can put $\tilde{\nu}_{10} = -1$. In the second case, number of electrons in the conduction band is unchanged and, therefore, $\tilde{\nu}_{10} = 0$. The number of electrons ν_{10} transferring on average from the conduction band into the donor per each ionization transition will be equal to

$$\frac{E_n \cdot (-1) + C_p p \cdot 0}{E_n + C_p p} = -\frac{E_n}{E_n + C_p p}$$

To find the net rate U directly from the digraph of states G , one should construct all functional digraphs (Φ -graphs) Φ_k covering G (definition and properties of the functional digraphs can be found in [3]), then to find the weight $[\Phi_k]$ for each of them by multiplying the weights ω_{ij} of all arcs entering into it (8a), the total variation of number of electrons ν_k taking place during the cyclic series of transitions of the defect along the cycle C_i belonging to Φ_k (8b). After that one can find U by (8c):

$$(a) [\Phi_k] \equiv \prod_{i \rightarrow j \in \Phi_k} \omega_{ij}, \quad (b) \nu_k = \sum_{\substack{l \rightarrow m \in C_i \\ (C_i \in \Phi_k)}} \nu_{lm}, \quad (c) U = N_{\text{tot}} \cdot \frac{\sum_k \nu_k [\Phi_k]}{\sum_{j=1}^M [J]}. \quad (8)$$

For example, the digraph G shown in Fig.1, has 14 Φ -graphs of $\Phi_{1...14}$, covering it [Fig. 3]. Φ -graph of Φ_1 contains the cycle $C_1 = 1 \rightarrow 3 \rightarrow 4 \rightarrow 2 \rightarrow 1$, Φ_2 contains that of $C_2 = 1 \rightarrow 2 \rightarrow 4 \rightarrow 3 \rightarrow 1$, the Φ -graphs of $\Phi_{3...5}$ contain the cycle $C_3 = 1 \rightarrow 2 \rightarrow 1$, $\Phi_{6...8}$ contain the cycle $C_4 = 3 \rightarrow 4 \rightarrow 3$, $\Phi_{9...11}$ contain $C_5 = 1 \rightarrow 3 \rightarrow 1$ and $\Phi_{12...14}$ contain $C_6 = 2 \rightarrow 4 \rightarrow 2$. Since the inter-center transitions $1 \leftrightarrow 3$ and $2 \leftrightarrow 4$, forming the cycles C_5 and C_6 , respectively, do not change number of electrons in the conduction band, then $\nu_{13} = \nu_{31} = \nu_{24} = \nu_{42} = 0$ and, consequently, $\nu_5 = \nu_{13} + \nu_{31} = 0$ and $\nu_6 = \nu_{24} + \nu_{42} = 0$. This means that the Φ -graphs of $\Phi_{9...14}$ do not give contribution to the carrier recombination rate U . The rest coefficients ν_i and weight of each of the Φ -graphs of $\Phi_{1...8}$ have been found as:

$$\begin{aligned} \nu_1 &= \nu_{13} + \nu_{34} + \nu_{42} + \nu_{21} = 0 + \frac{(+1) \cdot C_n^{34} n + 0 \cdot E_p^{34}}{\omega_{34}} + 0 + \frac{0 \cdot C_p^{21} p + (-1) \cdot E_n^{21}}{\omega_{21}} = \frac{C_n^{34} n}{\omega_{34}} - \frac{E_n^{21}}{\omega_{21}}, \\ \nu_2 &= \nu_{12} + \nu_{24} + \nu_{43} + \nu_{31} = \frac{(+1) \cdot C_n^{12} n + 0 \cdot E_p^{12}}{\omega_{12}} + 0 + \frac{0 \cdot C_p^{43} p + (-1) \cdot E_n^{43}}{\omega_{43}} + 0 = \frac{C_n^{12} n}{\omega_{12}} - \frac{E_n^{43}}{\omega_{43}}, \\ \nu_3 &= \nu_{12} + \nu_{21} = \frac{(+1) \cdot C_n^{12} n + 0 \cdot E_p^{12}}{\omega_{12}} + \frac{0 \cdot C_p^{21} p + (-1) \cdot E_n^{21}}{\omega_{21}} = \frac{C_n^{12} n}{\omega_{12}} - \frac{E_n^{21}}{\omega_{21}}, \\ \nu_4 &= \nu_{34} + \nu_{43} = \frac{(+1) \cdot C_n^{34} n + 0 \cdot E_p^{34}}{\omega_{34}} + \frac{0 \cdot C_p^{43} p + (-1) \cdot E_n^{43}}{\omega_{43}} = \frac{C_n^{34} n}{\omega_{34}} - \frac{E_n^{43}}{\omega_{43}}; \end{aligned}$$

$[\Phi_1] = \omega_{13} \omega_{34} \omega_{42} \omega_{21}$, $[\Phi_2] = \omega_{12} \omega_{24} \omega_{43} \omega_{31}$, $[\Phi_3] = \omega_{12} \omega_{21} \omega_{31} \omega_{42}$, $[\Phi_4] = \omega_{12} \omega_{21} \omega_{43} \omega_{31}$, $[\Phi_5] = \omega_{12} \omega_{21} \omega_{34} \omega_{42}$, $[\Phi_6] = \omega_{34} \omega_{43} \omega_{13} \omega_{24}$, $[\Phi_7] = \omega_{34} \omega_{43} \omega_{21} \omega_{13}$, $[\Phi_8] = \omega_{34} \omega_{43} \omega_{12} \omega_{24}$. Then putting the expressions for $\nu_{1...4}$ and $[\Phi_{1...8}]$ into (8c) one can find the expression for U :

$$U = N_{\text{tot}} \cdot \frac{\nu_1[\Phi_1] + \nu_2[\Phi_2] + \nu_3([\Phi_3] + [\Phi_4] + [\Phi_5]) + \nu_4([\Phi_6] + [\Phi_7] + [\Phi_8])}{D}$$

This expression can be further simplified for the case when the probabilities of the configuration transformations ω_{13} , ω_{31} , ω_{24} and ω_{42} are unaffected by the external excitation, so that the equilibrium relations between them are still valid $\omega_{31} = (g_1/g_3)\exp(E_0/kT)\omega_{13}$ and $\omega_{42} = (g_2/g_4)\exp(E_1/kT)\omega_{24}$, where $g_{1...4}$ are the degeneracies of the states of the bistable defect, E_0 and E_1 are the activation energies of configuration transformations of the defect without an electron and that with an electron, kT is the thermal energy

$$U = N_{\text{tot}} \cdot (np - n_i^2) \cdot A/D, \quad (9)$$

where

$$A = \left[\frac{g_1}{g_3} \exp(E_0/kT) C_n^{12} C_p^{43} + \frac{g_2}{g_4} \exp(E_1/kT) C_n^{34} C_p^{21} \right] \omega_{13} \omega_{24} + C_n^{12} C_p^{21} (\omega_{31} \omega_{42} + \omega_{43} \omega_{31} + \omega_{34} \omega_{42}) + C_n^{34} C_p^{43} (\omega_{13} \omega_{24} + \omega_{21} \omega_{13} + \omega_{12} \omega_{24})$$

At high levels of bipolar injection of carriers, when $n \approx p \rightarrow \infty$, recombination rate U linearly increases with increasing the injection level n and, respectively, carrier lifetimes τ_p and τ_n go to their constant value:

$$(a) U \approx \gamma \cdot n, \quad (b) \tau_p \approx \tau_n \approx n/U \approx \gamma^{-1}, \quad (10)$$

where

$$\gamma = N_{\text{tot}} \cdot \frac{C_n^{12} C_p^{21} (C_n^{34} \omega_{42} + C_p^{43} \omega_{31}) + C_n^{34} C_p^{43} (C_n^{12} \omega_{24} + C_p^{21} \omega_{13})}{(C_n^{12} + C_p^{21})(C_n^{34} \omega_{42} + C_p^{43} \omega_{31}) + (C_n^{34} + C_p^{43})(C_n^{12} \omega_{24} + C_p^{21} \omega_{13})}$$

5. Conclusion

In this work diagram method of investigation of recombination processes has been presented. Distinct from the traditional approach based on solution of the system of kinetic equations describing the ensemble of defects and free carriers, the diagram method is based on possibility of visual presentation of the set of possible quantum states of the defect and permitted transitions between them in schematic form as well as on deep informal relation between structural features of the transition scheme of the defect and probability to find it in one or another state. It was shown that the graph theory, having a well developed apparatus of combinatorial and structural analysis, is a powerful tool for investigation of carrier recombination processes: many establishments and problems of the theory of recombination phenomena are perfectly formulated in terms of graph theory and are completely solved by the visual graphical constructions avoiding solution of any system of kinetic equations. Particularly, the stationary non-equilibrium distribution function can be constructed using a set of all rooted directed trees covering the state digraph G , and the net rate of generation-recombination transitions can be built with the aid of all functional graphs covering G .

The results have been applied to the configurational bistable defects. Analysis was made for high injection levels and asymptotic expressions for carrier recombination rate and carrier lifetimes have been found.

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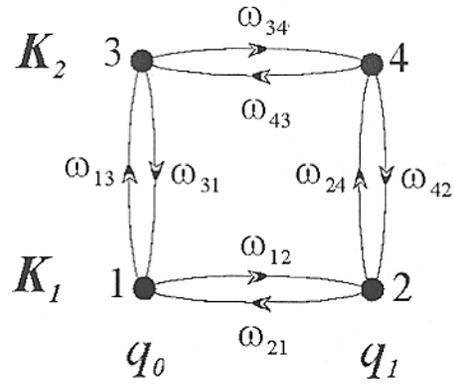


Fig. 1. Digraph of states G of a bistable defect, which can be in two configurations K_1 and K_2 , and charge states q_0, q_1 . ω_{ij} are the probabilities of transitions between the states of the defect.

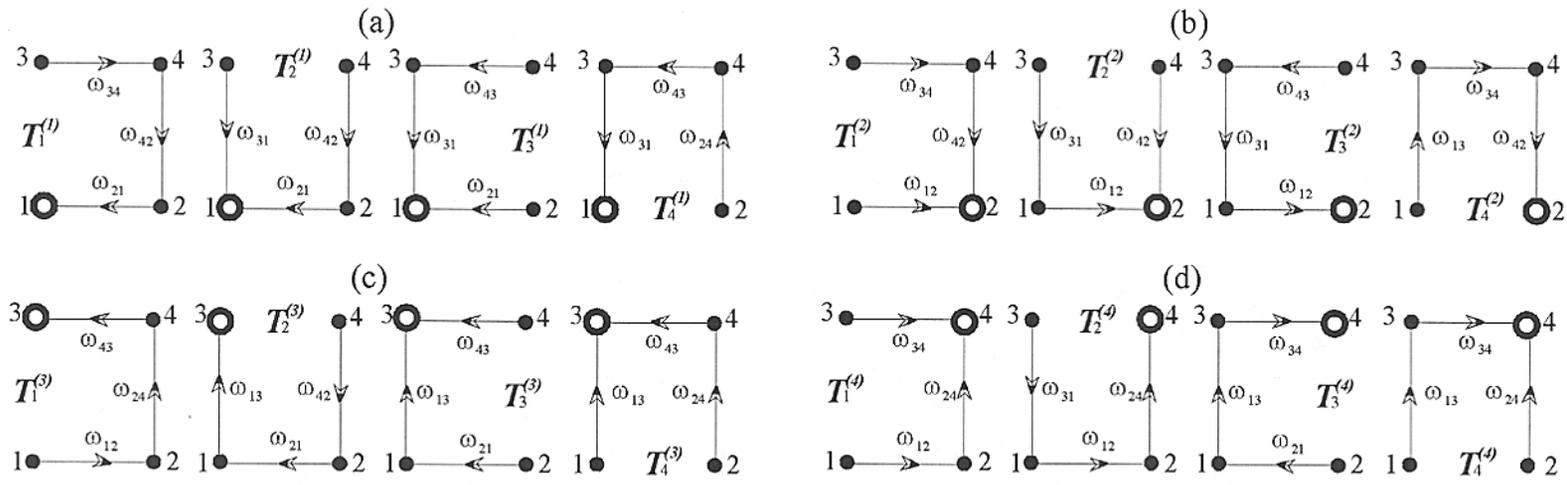


Fig. 2. All directed trees covering the digraph G , shown in Fig. 1. On each of the figures root vertex, which the corresponding directed tree grow in, has been released.

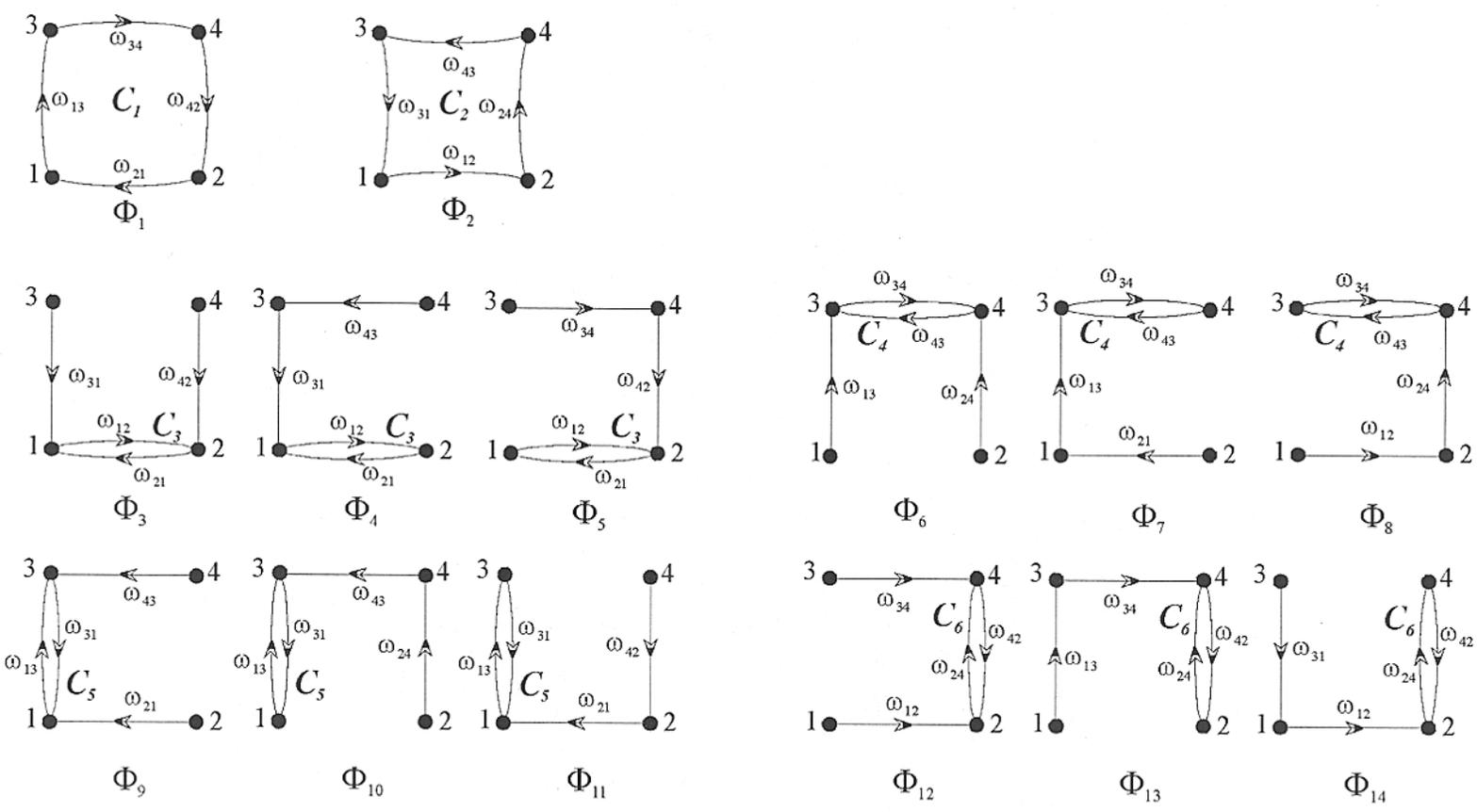


Fig. 3. Fourteen functional digraphs $\Phi_{1...14}$, covering the digraph G . Each of them contains one of the cycles $C_{1...6}$.

DEVELOPMENT OF A TECHNOLOGY OF SILICON PRODUCTION BY RECYCLING PHOSPHORUS INDUSTRY'S WASTES

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Abstract

A technology of silicon production by recycling wastes of phosphorous industry is suggested. The process of aluothermic reduction of silica from the waste was thermodynamically modeled and tested experimentally. The process is energy saving because of exothermic nature of the reaction. The technology open the way to phosphorous industry wastes utilization.

Keywords: Silicon production, Wastes recycling, Thermodynamic modeling

1. Introduction

Increasing demands of semiconductor and solar cell industries for suitable purified silicon promote investigations of various silicon production processes to achieve sufficient purity levels [1]. Such processes typically involve some sort of treatment of molten silicon with metals, slag and exposing to various gases action [2]. Also there are some methods of silicon purification by acid-leaching of silicon powder as well as unidirectional solidification of silicon. However, in spite of all these approaches, there is a demand for a high purity silicon production method from available natural resources by more economically effective way than is available by conventional techniques.

In this paper an economically effective process for silicon production by recycling of phosphorous industry wastes is presented. The process achieves silicon purification of about 99.99 wt.% level or higher.

2. Process background

The most widely used silicon production processes are based on the purification of inexpensive but impure silicon which is obtained in large quantities by carbothermal reduction of quartz, and on the production of pure silicon by use of purified carbon and quartz in carbothermal reduction process. Another method of pure silicon production is a process of quartz sand reducing with aluminum in a slag medium based on alkaline earth metal silicates [USA patent # 4,457,903]. The slag thereby simultaneously serves as a solvent for the aluminum oxide that forms and as an extraction medium for impurities.

The electric furnace method of phosphorus production that is generally used in industry produces a large quantities of slag, which predominantly consists of calcium silicate [3]. The phosphorus waste comprising of the silicon dioxide, the alkaline earth metals, calcium, magnesium and other substances may be used as a raw material for silicon recovering by aluminum. This technology of silicon extraction from phosphorus industry wastes based on the aluothermic processes has been tested experimentally in laboratory conditions.

A prominent feature of this new low-cost raw material - phosphorous industry slag utilization technology is in extraction of intermediate silicon-contained alloy. This alloy is convenient both for further silicon cleaning and preparing highly reactive metal powder for silane synthesizing. [Preliminary patents of Kazakstan: "A method of silicon obtaining" No. 4627 (1997) and "A method

The technological stages of semiconductor silicon production by phosphorous industry wastes recycling are shown in Figure 1. The effectiveness of the chemical refining and silane synthesis depends on the initial input feed and conditions of the aluothermic reduction process.

2.1 Raw Material

The phosphorous slag is a complex mixture with the composition shown at Table I. Due to phosphorous production technological demands, the waste has a stable composition.

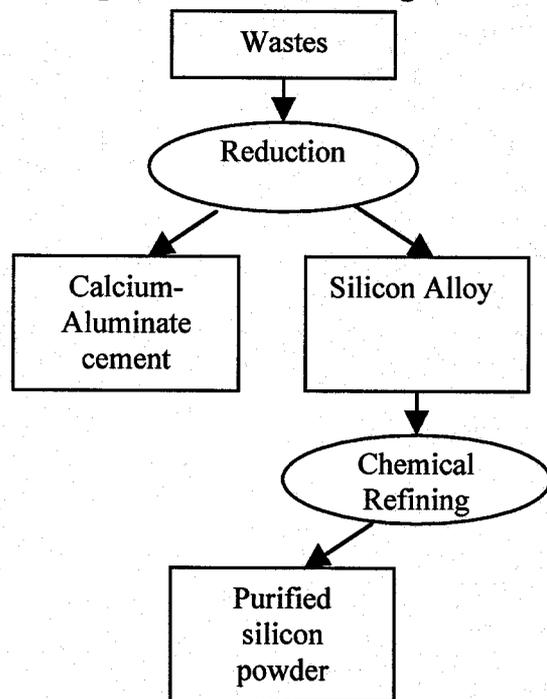


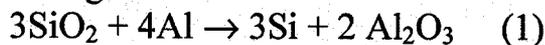
Table 1
Phosphorous industry wastes composition

—	Component of the slag	Mass %
1	SiO ₂	45 – 47
2	CaO	43 – 45
3	Al ₂ O ₃	3.2 – 3.6
4	MgO	2.2 – 2.5
5	P ₂ O ₅	0.8 – 1.3
6	F ₂	2.2 – 3.0
7	Fe ₂ O ₃	0.35-0.45
8	MnO	0.1 – 0.5
9	S	≈0.07

Figure 1: Main technological stages of silicon production from phosphorus wastes.

2.2 Advantages of Phosphorous Slag Aluothermic Reduction

The phosphorus slag is introduced into a reaction vessel, which preferably is graphite and heated by induction. The presence of calcium and fluorine compounds decreases the melting temperature (down to 1200-1300°C) and reduces the viscosity of the slag. Then the commercially available granular aluminum of purity 99,86 %, is added to the molten slag and heated to reduce the silicon dioxide by the formation of aluminum oxide. The quantity of aluminum must be enough to provide complete reduction of the SiO₂ in the slag. Good results are obtained when the slag and aluminum are mixed in a proportion corresponding to reaction:



The reaction is initiated at 1275°C, and subsequently the temperature rises due to exothermic nature of the reaction up to 2000°C.

Because of the exothermic nature of the reduction process, the reactor needs external heating only for slag melting and reaction initiation. This allows considerable energy savings in comparison with regular carbothermic process.

When the reaction material has completely reacted, the produced metal and secondary slag are cast in the graphite molds in which the cooling rate is relatively slow. The mixture of silicon and secondary slag can be easily separated, due to difference in densities. So that of the slag begins to settle in the graphite mold, the silicon formed collects on the surface of the slag. Oxide impurities, which are formed as a result of reaction with atmospheric oxygen on the surface of the silicon that has formed, dissolves excellently in the surrounding slag. Therefore it is possible to perform the

process in an open system, with air being admitted.

Secondary slag is another valuable output product of the aluminothermic reduction, because this slag contains calcium-aluminate compounds suitable for production of high quality cements.

2.3 Silicon-Contained Alloy And Secondary Slag

The results of analyses of elemental and phase composition of silicon-contained alloy and secondary slag are given in Table 2 and Table 3. It is seen that the silicon-contained alloy is Si-Ca-Al one with the typical composition Si (80%), Ca (8.4%) and Al (~3.5%). The composition varies depends on reaction conditions: temperature, reaction rate, initial slag compositions. The secondary slag consists of calcium-aluminate compounds.

Table 2

Main components of the silicon-contained alloy and secondary slag. Results of chemical analyses.

Alloy		Slag	
Element	Content, weight %	Element	Content, weight %
Si	80	Si	6.9
Ca	8.4	Ca	19
Al	3.5	Al	32.5

Table 3

Phase composition of the silicon-contained alloy and secondary slag. X-ray analyses of phases.

Alloy		Slag	
Phase	Content, weight %	Phase	Content, weight %
Si	80	$\text{Ca}_2\text{Al}_2\text{SiO}_7$	40-45
CaAl_2Si_2	13	CaAl_4O_7	40-45
CaSi_2	7	Others	10-20

2.4 Thermodynamic Modeling Of The Aluminothermic Reduction Process

For the thermodynamic modeling of the process a TERRA software based on ASTRA-4 package [5] was used. The software is developed for high-temperature process simulation in multi-component heterogeneous systems. The program is based on the principle of maximum entropy for isolated thermodynamic systems in equilibrium and has own thermodynamic database for 3200 substances.

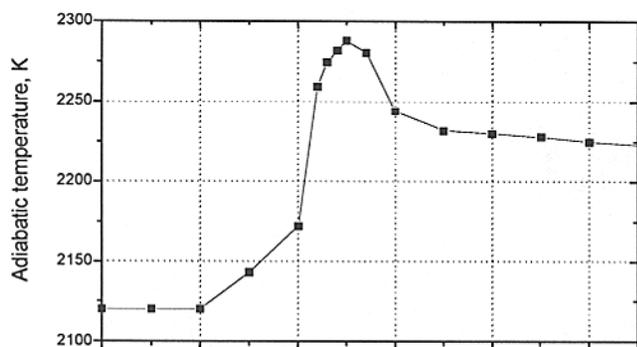


Figure 2. Adiabatic temperature dependence

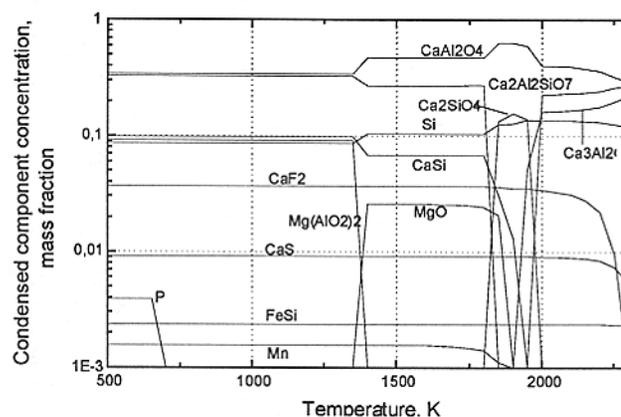


Figure 3. Condensed phase components dependence on the process temperature

Aluminothermic reduction of silicon was simulated for phosphorous industry wastes (PIW) of composition presented in Table 1. Lets denote as $\alpha=1$ the aluminum portion which is necessary add to PIW, according (1), to reduce all silicon contained. Calculations were made for aluminum portions varying in the range $0.8 < \alpha < 1.35$.

A calculated dependence of adiabatic temperature that is reached as result of exothermic reducing reaction on adding aluminum portion is presented in Figure 1.

At the Figure 2 condensed phase components dependence on the process adiabatic temperature is shown. The calculation was made for $\alpha=1$. At the adiabatic temperatures the condensed phases consist of silicon and cement - typically a mixture of CaAl_2O_4 , $\text{Ca}_2\text{Al}_2\text{SiO}_7$, $\text{Ca}_3\text{Al}_2\text{O}_6$. Also there are CaS and FeSi present in the condensed phase with total fraction about 1%. All condensed fractions at the adiabatic temperature are in the liquid phase, except a refractory component CaS. All P, Mg, and Mn containing components are transformed into gas phases at the temperatures even below the adiabatic one.

The process of cooling from thermodynamic equilibrium point at adiabatic temperature was modeled numerically. The process is modeled supposing that the interaction between components at the temperatures above the melting point takes place rapidly, in contrast with reactions when the components which are became solid. So, components once below their melting point were excluded subsequently from the numerical simulation process. Using this procedure, the process of alumothermic reducing was analyzed with the aim of maximizing silicon producing

It was found that "purest" silicon will be obtained by adding aluminium portion of $\alpha=0.95$. "Purification" depends on cooling conditions - slowing of the cooling increases the purification, especially at the temperatures above 1850K when most components are in liquid phase. Undesirable impurities inherited from phosphorus technology, like P_2O_5 , MgO, MnO and others, are removing into gas phase at even much lower temperatures than the adiabatic, which can be theoretically reached due to the intensive exothermic figure of the reaction.

It was also found numerically, that the maximum silicon yield is expected at $\alpha=0.95$ with the level of 80% of all silicon contained in the slag. This level was confirmed experimentally (see results in Table 2,3) when the reducing process was carried out freely without an attempt to prolong the cooling stage.

3. Chemical refining

As is mentioned above, a metal obtained by alumothermic method from phosphorous slag contains up to 10% ___ and that allows better purification of silicon [USA patent #4 539 194]. The ingots obtained after cooling are mechanically crushed. The size of the resulting clumps is not critical. Generally good results are achieved with a few centimeters size.

The silicon lumps are leached with a dilute inorganic acid such as, for example, hydrochloric acid, hydrofluoric acid, nitric acid or mixtures thereof. This leaching results in rapid cracking of the metal grains along the grain borders.

Leaching is carried out at a temperature ranging from room temperature to 80°C, generally employing acids in an aqueous solution at 2.5-10% concentration and ratios by weight between the acid solution and the silicon between 1.5 and 5. The duration of leaching is an inverse function of the temperature and will usually range from 20 to 50 hours.

After the unwanted impurities are dissolved, the solvent and dissolved fines of smaller particles size then 0.06 mm are decanted. The remaining material is screened on 1.0 mm and must be thoroughly washed in distilled or ion exchanged water. As a result of such operations we have obtained the silicon powder with purity of 99,99% and higher.

Silicon powder characterization by using the mass spectrometry reveals that the concentrations of impurities are as follows: (element - Concentration): Fe < 0.2 ppm; Al - 40 ppm; B - 10 ppm; P < 0.5 ppm; Mn < 0.2 ppm; Cu < 0.3 ppm; Cr < 0.2 ppm; Zr < 0.2 ppm; V < 0.1 ppm; Ti < 6 ppm; Ni < 0.2 ppm; Ca - 70 ppm; Mo < 0.3 ppm. Other impurities levels are less than 0.1 ppm. The additional refining is possible by reactive gas blowing of the molten charge.

4. Conclusions

The advantages are presented of a non-chlorine environmentally benign technology using an attractive mixture of raw materials. The demonstration of the decrease in boron and other impurities allows us to suggest new enormous feedstock for semiconductor silicon production. However detailed studies of the process peculiarities are still necessary.

5. Acknowledgements

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Rapid ARC Formation Using a Simple and Versatile Etching Process

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Abstract

Highly uniform films with excellent anti-reflection (AR) properties can be formed on any silicon substrate using a simple electrochemical etching technique. This process selectively removes silicon atoms from the sample surface, forming a layer of porous silicon (PSi) with adjustable optical, electrical, and mechanical properties. This investigation has focused on the formation of thin film PSi layers on the surface of solar cells without disturbing the underlying junction characteristics. Significant performance improvements have been achieved in single layer PSi films by systematically optimizing light trapping and AR effects while maintaining the electrical properties of these cells. We have also studied the potential application of gradient index of refraction PSi layers for solar cell AR applications. Demonstrated reflectivities comparable to vacuum deposited double layer AR coatings have been achieved in single graded index layers formed using this simple electrochemical technique. The etching process may also prove effective in sample cleaning, impurity removal, and grain boundary passivation in applicable manufacturing environments.

1. Introduction

Porous silicon has been widely studied since the early 1990's, due primarily to interest in its development as an efficient light emitting material for optoelectronic applications [1], but had been applied to solar cell research as early as 1982 [2]. The light trapping and anti-reflection properties of PSi, in addition to its simplicity of formation and broadly tunable morphology, make it particularly well suited for photovoltaic applications. It has been used as a single or multilayer antireflective coating by exploiting the tunability of the film's effective index of refraction [3,4]. Demonstrated reflectivities tend to average between 10%-15% over the spectral range 300nm-1200nm, but average reflectivities as low as 2% have been shown with graded index layers [5]. Improvements of 50% in I_{sc} have also been demonstrated while maintaining fill factor and V_{oc} [6].

PSi results from the electrochemical dissolution of a silicon substrate in the presence of a hydrofluoric acid (HF) electrolyte and positive charge carriers (holes). Randomly formed pits in the surface form pores that propagate into the substrate when the dissolution reaction is favored at the pore tips. As illustrated in figure 1, this condition exists when current is passed through the electrochemical cell, where holes propagating toward the substrate surface first encounter fluorine ions at the pore tips. If all holes are consumed at the pore tips, the upper porous matrix is protected from dissolution, and a stable PSi layer can be formed [7]. The porosity (percentage of empty space) of the PSi formed at the pore tips is proportional to the current density through the cell at that time. Since the porosity at a given depth is controlled by the electrochemical current density, dynamic control of the current during the etch can produce porosity gradients or alternating layers

of varying porosity within the film [8]. Porosity changes correspond to changes in the effective index of refraction through the effective medium approximation, and therefore the engineering of porous layers with desirable optical properties can be achieved.

The morphology of the porous silicon matrix that remains after electrochemical etching is not only dependent on current density and substrate doping, but is also effected by the HF electrolyte concentration, the duration of the etch, temperature, and ambient lighting conditions during the etch. Within this large parameter space, the resulting structure can have feature sizes that vary over a wide range, from nanometers to microns, depending on the nature of the etch. From the physical optics point of view, structures with sizes larger than the wavelength of incoming light enhance light trapping by reflecting incoming radiation in random directions [9]. Structures much smaller than the incoming wavelength alter the effective index of refraction of the film and allow it to be tuned between that of crystalline silicon (c-Si) and air [10]. Direct control of the effective index of refraction depth profile by the etching current density provides an excellent opportunity to form graded-index ARCs with properties superior to discrete layer coatings [11]. Graded-index ARCs can eliminate or limit the large discontinuity in index of refraction at solar cell surfaces that is responsible for reflection losses. As mentioned earlier, wide bandwidth graded-index PSi ARCs with extremely low reflectivity have been demonstrated [5].

Although PSi is not presently utilized in an industrial solar cell setting, it offers several potential applications. The combination of a controllable index of refraction with the light trapping characteristics of PSi enables the simultaneous texturization and anti-reflection (AR) coating of solar cells. These are two discrete process steps in commercial products, provided an effective texturization process exists for a given substrate. Porous silicon texturing can be applied to a broad range of crystalline, microcrystalline, and multicrystalline silicon substrates [12], unlike anisotropic alkaline etching which is specific to (100) oriented substrates for pyramid-like structuring. The formation of PSi also involves the consumption of a portion of the surface layer of the solar cell and can therefore also be effective in the removal of dead layers remaining after diffusion [13] or preferential removal of grain boundary material [14]. There is also evidence that thin PSi ARCs can be “fired through”, making this material compatible with commercial screen printing metalization [15].

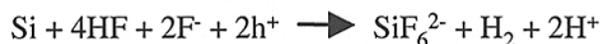
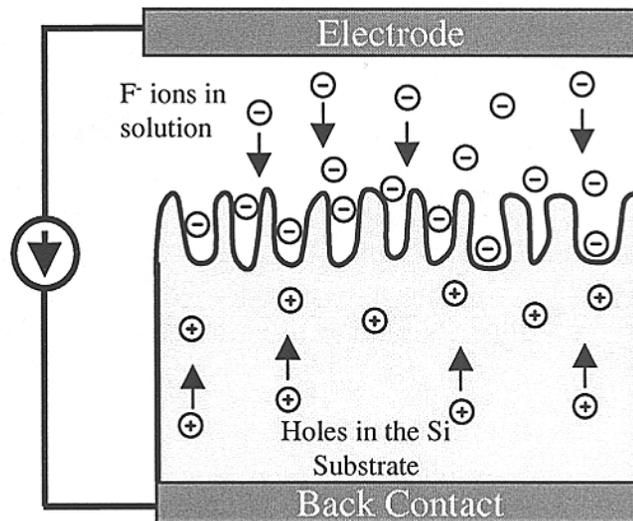


Figure 1. Holes drifting toward the substrate surface drive the electrochemical process that forms porous silicon. These holes are most likely to react with fluorine ions at the bottoms of pores or pits, deepening these features and creating a porous surface film.

In this investigation we have focused on thin (<200nm) PSi films that consume as little of the emitter region of our cells as possible. Substantial improvement in the I_{SC} of a commercial device has been achieved by the incorporation of a thin PSi film after dopant diffusion. In addition, the formation of graded-index PSi ARCs was investigated and simulated.

2. Experiment

A matrix of PSi samples was prepared using string ribbon polysilicon [16] solar cells. These substrates had diffused phosphorous emitters with a junction depth of 350 nm and back contacts formed with a fired Ag paste. Etching current densities varied from 0.5-10 mA/cm² with etching times of 10 and 30 seconds. For electrical characterization of these devices, Ti/Pd/Ag contacts were evaporated and patterned with a liftoff procedure.

A second set of etches were conducted on 0.01 Ω -cm p-type silicon wafers to study the formation of gradient index of refraction films. A computer was interfaced with the etching current supply that allowed the current to be continuously varied during the etch. Each etch started with a given current density that was gradually reduced to zero in a specified period of time. The current density was either decreased linearly in time or with a power law dependence. Initial current density ranged from 5 mA/cm² to 160 mA/cm², with etching time of 5 sec to 40 sec and various time dependencies. These current density functions form PSi with low index of refraction near the air interface of the film, and PSi of higher index of refraction at the silicon substrate interface.

The reflectivity of each sample was measured with a Perkin-Elmer UV/VIS/IR spectrophotometer using an integrating sphere to measure the total specular and diffuse reflected light. Scanning Electron Microscope (SEM) cross-sectional images of several samples were taken with a Zeiss Leo SEM to determine film thicknesses. Light IV measurements were made using a 1000W mercury-xenon lamp as the excitation source.

3. Results

The reflectivity of several string ribbon substrates is plotted in figure 2. From this data it can be seen that substantial reductions in reflection losses can be achieved with brief etching treatments. The reflection minima of these thin films can be tuned across the visible spectrum with these constant current treatments and substantial improvement can likely be gained using variable current techniques as will be discussed later.

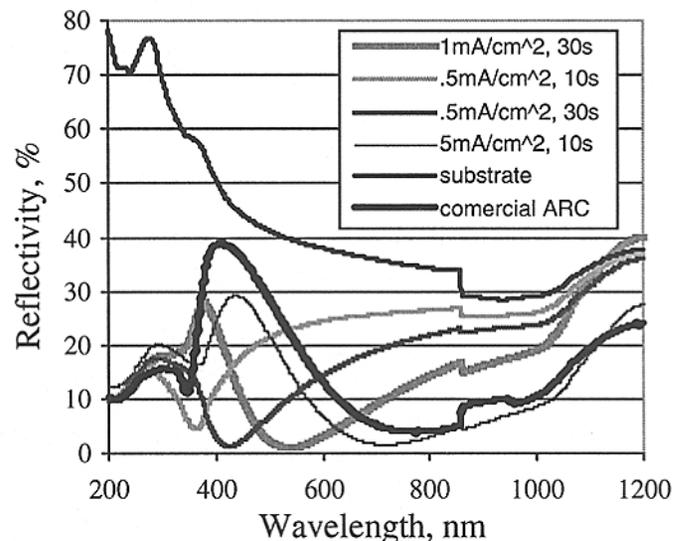


Figure 2. Various PSi treatments of string-ribbon grown polysilicon substrates show considerable reflectivity reduction when compared to an uncoated solar cell. The reflectivity spectra of a commercial cell with a single layer AR coating is also included.

After evaporating tri-layer Ti/Pd/Ag front contacts, the light IV data shown in figure 3 was measured. The addition of a PSi layer in samples B and C increased both the open circuit voltage and the short circuit current, leading to a considerable increase in power output for these samples. The increased power output of these devices is a direct result of the increased coupling of optical power into the samples by the PSi AR coating. Fill factor also increased in sample C, relative to the reference, indicating that the PSi layer introduces no substantial ohmic losses. This demonstration of considerable efficiency improvement without degradation of the electrical properties of a PSi AR device is a strong indication of the potential applicability of this material to commercial solar cells.

Substantial reduction in reflectivity was observed in all graded index samples relative to a control sample that was etched at a constant current density as shown in Figure 4. In this figure, the gradient index films exhibit reflectivities less than 10% across the range from 300nm to 1200nm, while a single film of similar thickness shows much higher reflectivity.

4. Conclusions

This investigation has demonstrated the feasibility of integrating PSi AR layers into commercial polycrystalline silicon solar cells. Light IV data have indicated that thin PSi layers do not degrade the electrical characteristics of a commercial solar cell while providing significant efficiency increases due to their AR properties. The simplicity of PSi formation and compatibility with both crystalline and randomly oriented polysilicon materials also these layers an economically viable solution for low cost, large area photovoltaic applications. Additional improvements in the AR properties of PSi films by

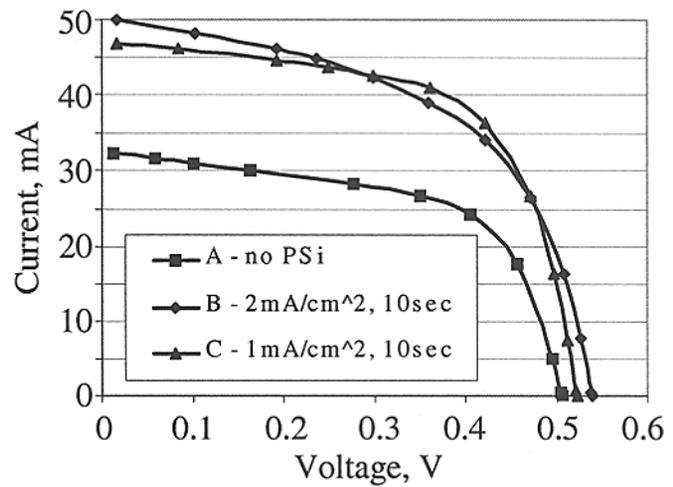


Figure 3. These light IV curves illustrate the strong increase in I_{SC} observed in PSi AR coated cells.

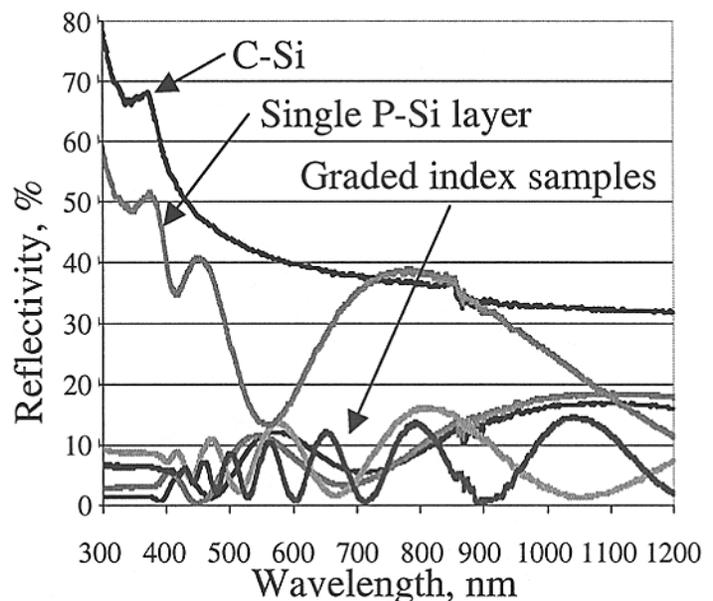


Figure 4. The reflectivity spectra for several gradient index PSi layers formed on a p+ wafer substrate are shown relative to a comparable thickness standard single layer film.

forming gradient porosity layers have also been studied and show excellent promise for further improvement in these devices.

Acknowledgements

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CRYSTALLINE SILICON TECHNOLOGIES IN CIS COUNTRIES

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I. INTRODUCTION

The main objective of the National Solar Energy Programs of CIS countries is to achieve cost-competitiveness of solar energy technologies comparing with traditional fossil fuel energy technologies in order to enhance the pace of rural electrification in CIS countries in a cost-effective reliable, environmentally benign, sustainable manner.

On the basis of the analysis of a modern technologies, cost of manufacture and market of solar modules the nearest (2 US\$/Wp) and long-term goal (1 US\$/Wp) for the decrease of the production cost of silicon solar modules are formulated. For realization of the specified objective the search of the new ways and directions in technology, the development of new principles, ecologically pure methods and designs of installations are proposed allowing to lower expenses on manufacture of system components, to increase efficiency of solar cells up to 20 %, to exclude pollution in production process, to lower the cost of solar grade silicon. Major factor, constraining development of the photovoltaic market, in CIS countries is limitation of resources of polycrystalline silicon feedstock of and its high cost 50-70 US\$/Wp, which is much higher than uranium fuel for nuclear power stations. As the content of silicon in earthcrust exceeds the contents of uranium in 100000 times and crystalline silicon is not ecologically dangerous product, such high silicon cost should be explained only by absence of cost-effective silicon technology. The existing traditional technologies of crystalline silicon with use of chlorosilane cycles have a low silicon yield, the high energy consumption, they are dangerous and are unacceptable for large-scale application in the future. Ecologically pure chlorless technologies of raw solar grade silicon will be investigated and developed, to lower the energy consumption in 10 times, to increase a silicon yield during manufacture from quartz in 5 times, to lower raw feedstock silicon cost to 5-15 US\$/kg.

II. CRYSTALLINE SOLAR GRADE SILICON

In the reduction of the solar electricity cost two main options are competing semiconductor material and concentration. Crystalline silicon has acquired a domineering role in the photovoltaic industry.

Considering that one kilogram of silicon in a solar cell will generate at one-sun irradiant 400 MWh of electricity in the course of 30 years, we can easily determine the oil equivalent of this silicon. Directly calculating the 400 MWh of electricity that can be produced by oil with a heating value of 43 7 MJ/kg, we find that 33 MT of oil is equivalent to one kilogram of silicon. Assuming the efficiency of an oil-fired thermal power station to be 33 %, one kilogram of silicon in terms of generated electricity is equal to about 100 MT of oil. For this reason, silicon is frequently referred to as the oil of 21-st century profitable as investment in the oil industry.

The principal limitation for high PV cost reduction is the high cost of the solar grade monocrystalline silicon - 90 to 120 dollar/kg. Therefore, development of new technologies of production of silicon, providing a radical reduction of its cost, is the problem number one in the list of solar energy technologies [1]. The situation with solar silicon can be compared with the situation with aluminum after its discovery in 1825, when it cost like silver and used for ornaments.

Only after the development of the technology of electrolysis in 1886 aluminum became a cheap and practicable material.

The content of silicon in the earth-crust is 29,5 % ($8 \cdot 10^{18}$ t) and exceeds the content of aluminum by 3,35 times. Solar polysilicon with a purity of 99,99 % costs more than uranium for nuclear power plants, though the content of silicon in the earth-crust exceeds the content of uranium by 100,000 times.

The world trustworthy reserves of uranium are estimated as 2,763,000 MT. The uranium fuel cycle, including the production of uranium hexafluoride, is considerably more complicated and dangerous as compared with the chloro-silane method of production of solar silicon. Taking into account the scattering and low content of uranium in the earth crust as compared with silicon, it is difficult to understand, why uranium fuel for nuclear reactors and silicon for solar power plants have the same cost. There are several reasons explaining such a situation. Billion sums are invested in the development of the technology and production of uranium, they were allocated mainly to military programs, and the production ten years ago of uranium exceed the production of solar silicon by six times (Table 1) [2].

Table 1

Comparative characteristics of energy materials for nuclear and solar power plants

Parameter	Uranium	Silicon
Content by mass in Earthcrust (%)	0,0003	29,5
World trustworthy reserves (10^1 MT)	2763	> 25 million
Annual production (10^1 MT)	45	1000 (metallurgical) 7 (semiconductor)
Cost (US\$/kg)	40-60	1 (metallurgical) 90 - 120 (solar monocrystalline)
Energy equivalent for 30 years (MWh/kg)	3000	400
Power plant life (year)	30	50- 100

The chlorosilane technology of production of solar polysilicon developed about 35 years ago practically has not changed up to nowadays, preserving all the negative features of chemical technologies of the fifties: a high energy consumption a low yield of silicon, an ecological danger (Table 2).

Table 2

Solar grade silicon technologies

	Traditional technology	New technology
Process of purification	Chemical, distillation of trichlorosilane	Physical, distillation of monosilane
Energy consumption (kWh/kg)	250	15-30
Silicon yield (%)	6-20	80-95
Cost of polysilicon (US \$/kg)	50- 100	10- 15
Ecological characteristic	Hazard	Clean

The conventional technology of semiconductor silicon production includes the transferring of metallurgical silicon into volatile compounds (usually chlorosilanes), the purification of chlorosilanes by rectification, the hydrogen reduction of purified compounds into silicon and the ingots growth. This scheme is similar for electronic quality and solar grade silicon, so the conventional technology of solar grade silicon uses the same processes as electronic quality silicon.

Factories in Bratsk and Irkutsk, Siberia, Kamenezk-Uralsk, the Urals and Dnepropetrovsk, Ukraine manufactures the metallurgical quality silicone. New company "Silicon" (Director N.I. Baboon) invested 2.0 million US\$ to the project of utilization of its own Shilkinsky quartzite deposit on Krasnojarsk region and of manufacture of high purity metallurgical silicon in Abakan, Republic Khakassia of Russia. The total cost of the project 11.85 million US\$ for production of 21,600 thousand MT per year by 2001 and income 42,768 million US\$ in 2000. The production cost is 0,7 US\$/kg and expected profitability 50 %. This project and others must attract the interest of investors because the projects have the guaranty of Government, investors are invited to become a founder of the company and to be the exporter on the external market finished products of the company.

The principal material for production of silicon-silica in the form of quartzite or quartz sand makes up 12 % of the lithosphere mass. Russian quartzite is among the purest in the world (Table 3). The Boron concentration in Russian quartz, measured by Prof J.G. Grabmaier (Simens AG) is less than 0,1 ppmw [3]. Available quartz deposits in Russia are sufficient for production of silicon and solar photovoltaic plants with a capacity of over 1,000 GW.

Table 3

Impurities in natural Russia quartzites for different deposits (in ppm)

Deposits			
Impurity	The Urals	Buryatia	Irkytsk-region
P	0,04	2,00	0,04
B	0,06	0,01	0,04
Al	10,00	4,00	100,00
Cu	0,04	0,90	0,20
Ti	1,00	0,90	2,00
Ni	0,10	0,30	3,00
Fe	10,00	1,00	2,00
Na	3 00	10,00	-
Cr	0,10	0,10	0,20
Ca	3,00	0,30	9,00
Mn	0,05	0,10	004

A high binding energy of Si-O - 464 kJ/mole causes high expenditures of energy on the reducing reaction of silicon and its subsequent purification by chemical methods -250 kWh/kg, and the silicon yield is 6 to 20%.

The specified goals PV module cost reduction can be realized at the cost of the crystalline silicon wafer 0.8-1 US dollars on peak watt (nearest goal) and 0.3-0.25 US dollars on peak Watt (long-term goal) and the cost of polycrystalline solar grade silicon 25 US\$/kg (nearest goal) and 10 US\$/kg (long term goal) [4].

Since 1970 investigations were carried out in Russia, Germany, Japan, Norway and USA in creation of new technologies of production of silicon excluding the chlorosilane cycle. In 1990 the efficiency of cells made by using new solar grade silicon technology was 14.2% as compared with 14.7% of cells made of chlorosilane silicon [3] Now three new chlorless technologies of solar grade silicon are ready for final development and commercialization.

III. CARBOTHERMIC REDUCTION TECHNOLOGY FOR THE PRODUCTION OF SOLAR GRADE SILICON FEEDSTOCK USING HIGH PURITY RUSSIAN QUARTZ.

The proposed method of solar silicon production based on the direct carbothermic reduction of high pure natural raw materials with the applying of specially designed technique and raw materials ensuring the sufficient purity of the resulting product.

The analysis shows that natural quartz and carbon black can be used without special additional chemical purification.

The solar silicon production is proposed to realize in new arc furnace by carbothermic reduction of natural high purity quartz. As a reduction material it is supposed to use natural graphite or soot carbon (variant 1) or natural gas (variant 2). The closed reaction chamber ensures the high ecological parameters of the process and decreases the electrical energy consumption in 10 times per solar silicon mass unit. The lowering of labor-intensity and increasing the silicon output up to 80 % will allow to decrease the solar polysilicon cost to US\$ 15 per kg.

The two stage carbothermic reduction process using carbon at the first stage and silicon carbide as a reducing agent at the second stage was developed jointly by Russian and Ukrainian scientists in 1983 - 1989 [5]. In 1990-1993 the ROTD activity was conducted jointly with Prof. J.P Grabmier (Simens AG).

The development of equipment and technology for carbothermic reduction of solar grade silicon is provided by VIESH, Moscow, "Sibterm Ltd ", Irkutsk, "Redmet-service Ltd.", Moscow, "Silicon", Moscow - Krasnojarsk, "Solar grade silicon of Siberia", Irkutsk etc. The Government of Burjatia offered to provide guaranty investments to starting solar grade silicon production in Ulan-Ude with utilization of Cheremshanskoe deposit of high purity quartz.

The equipment was developed and the samples of solar grade silicon are manufactured which confirmed the correctness of the proposed technology.

For starting up solar grade polysilicon production at the level of 40 MT per year 3 million USD is required.

THE PRODUCTS AND CO-PRODUCTS AVAILABLE:

- 99,999 % purity raw solar grade silicon for ingots growth.
- crushed high purity silicon dioxide for optical devices (optical fibers, optical glass) manufacturing;
- soot carbon with the 99,9 % purity in powder or in grains for the needs of polygraphic, paint, electrochemistry and rubber industries

THE MAIN ADVANTAGES OF THE SUGGESTED TECHNOLOGY ARE:

- the low cost of solar silicon (2-3 times less then produced by conventional method);
- the reducing of energy consumption for solar silicon production (in several times),
- the use of patent-clear technologies;
- the ecological safety of technological process.

IV. CHLORLESS TECHNOLOGY OF HIGH PURITY SOLAR GRADE SILICON FEEDSTOCK.

The technical silicon of 96 - 98 % purity will be used as starting material. The synthesis of Silicon feedstock has to proceed in accordance with following scheme [6]:

- a) Purification of crushed metallurgical silicon with using of alkaline solution.
- b) Preparation of the homogeneous mixture of silicon powder with a catalyst.
- c) Alcosilicification of silicon by alcohol and picking of triethyl silane from the reaction mass.
- d) Producing of monosilane by using of catalytic disproportionation of a triethyl silane.
- e) Adsorption purification of monosilane with using of the hard sorbents.
- f) Producing of raw silicon by pyrolysis of monosilane.

Each process was tested in the terms of experimental production. Process (d) has an exceptional selectivity to synthesis of monosilane and prevents the formation of the volatile compounds with the bad impurities in silicon. This situation makes easier the purification of the monosilane.

Process (a) and (c) is connected with using of closed cycle of treatment with regeneration of the applied acids and alcohol. All technologies used the available large scale producing cheap raw materials metallurgical silicon and absolute alcohol.

ADVANTAGES:

The specific feature of the offered technologies is using the cheap initial materials, excluding of unhealthy chloride substances and producing of the non-expensive high quality raw silicon. The dependence of PV industry from production and use of electronic grade silicon can be lowered.

V. SOLAR GRADE SILICON TECHNOLOGY, BASED ON RICE HUSK TREATMENT.

The rice husk is used as an initial raw material. In this case the process of producing of raw silicon concludes the following basic stages:

- a) Chemical treatment of the rice husk for separating of the organic impurities and producing of the food and medicine preparates (for example vanillin, csilit.).
- b) Fast pyrolysis of the rice husk in a controlled ambient for producing of a mixture of amorphous SiO₂ and carbon.
- c) Preparation of a monocharge (granulation)
- d) Carbothermal reducing of silicon in the arc discharge furnace.

The following problems will be solved:

- a) Using of the rice wastes.
- b) Pollution during the non-chloride synthesis of monosilane can be reduced in comparison with the standard chlorosilane technology.

The annual world volume of production of the rice husk is the tens of million MT. So this product is an unlimited raw source for silicon production.

VI. PLASMA TECHNOLOGIES FOR MANUFACTURING OF SOLAR GRADE SILICON.

Thermodynamic calculations have shown the possibility of high temperature impulsed processing of silicon from gaseous silicon compounds with chlorine, fluorine and hydrogen. One alternative technology to the Simens process is developing by Prof. I.A. Kossy and V.V. Kostin in General Physics Institute of Russian Academy of Sciences [7]. They proposed to use ultra high frequency ($\lambda = 4-15$ cm) plasma thermo-nonequilibrium discharge for low temperature (300 °C), high productivity decomposition and reduction of silicon compounds [6]. The plasma discharge can be easily realized in a fluidized-bed reactor. The plasma is formed by using microwaves radiation focusing in a kind of coherent beams or using another kind of special plasma surface discharge. The fundamental difference between proposed method

and plasma discharge using in amorphous silicon production that new technique can be realized at barometric (atmospheric) pressure. It allows increasing the velocity of reaction and the productivity of the process more than 100 times.

Very high electron temperature of plasma (up to 12000 °C) and high local density of energy up to MW/cm results in essential acceleration of chemical reactions. Also chemical reactions can be realized which are impossible to realize in thermo-equilibrium conditions. Thus, high efficiency of molecules dissociation is reached and because of low gas temperature 300 °C the reverse reactions have a small velocity. The equipment produced by an industry has high efficiency (50-90%).

The other features of the process are low energy consumption (20-40 kWh/kg), high pureness because of "cold wall" processing and considerable decrease of hydrogen consumption in reduction processes.

The special pilot equipment with capacity 100 kg/year can be made within 15-20 years with the estimated cost of the project 300 thousands US dollars.

Another proposed technology includes heating of monosilane through fast pressing in special chemical reactor with high rate of monosilane decomposition. The expansion of the reacting gaseous mixture proceeds its fast cooling. High temperature of gas exists during 1 ms, the walls of the reactor are cold and it is possible to avoid pollution of reaction products.

It is proposed to use closed type modified furnace with direct current plasmotrones. In this furnace patented in Russia the discharge is not formed between the electrode and the sole as in alternative current traditional furnace, but between coaxial disposed tubular graphite electrodes. This new plasmotrone design provides stable electronic controlled melting process in the garnisage crucible, low noise and pollution level and the possibility of continuous operation of a furnace.

VII. THE TRADITIONAL SILICON TECHNOLOGIES

The volumes of production of monocrystalline silicon, polycrystalline silicon feedstock and semiconductor quality trichlorosilane in 1991 and in 1998 are presented in Tables 4, 5.

Before 1991 all production of trichlorosilane was installed in Ukraine and Kyrgyzstan. In 1995 the Federal Program "Silicon of Russia" was supported by the Decree of the President of Russian Federation and Resolution of Russian Government.

Table 4

Crystalline silicon production in CIS countries in 1991, metric tons

Products	Russia	Ukraine	Kyrgyzstan
Monocrystalline silicon	225	335	68
Polycrystalline silicon feedstock	390	705	—
Semiconductor quality trichlorosilane	—	15445	—

Three projects are offered to start large-scale trichlorosilane and silicon production. One of the projects is connected with production of silicon in Baltic silicon valley in Nuclear Power Plant, Leningrad region. The project total capacity is 1000 MT per year. The project is proposed by Academician the Nobel Prize laureate A. M. Prochorov and Ellina - NT, Ltd in Moscow (Table 5). The potential investor from Oman is negotiated.

The second big project is offered by SI 1 Ltd in Moscow Region and Novocheboksary. The annual capacity is 1500 MT. The potential investor from Germany is negotiated.

Table 5

Silicon manufacturing facilities in CIS countries

#	Facility	The volume of production in 1998, metric tons		
		C-Si	Si-Feedstock	trichlorosilane
Russia				
1	Podolsky chemical metallurgical factory, Russia, Moscow Region	200	100-200	—
2	Non - ferrous metals factory, Krasnojarsk, Siberia	20 " ^	—	—
3	"Silicon Ltd" founded by Mining and Chemical combine, Krasnojarsk, Siberia	—	100	—
4	Intertechnology Ltd., Moscow	50 (3.5 M wafers)		
5	Elma, Zelenograd, Moscow Region	25		
6	Luch, Moscow Region	6		
7	Keuh, Moscow Region	25		
8	"Solar grade silicon of Siberia", Joint stock company, Irkutsk, Siberia			
9	Joint stock company "Silicon", Moscow, Krasnojarsk			
10	Si Ltd, Moscow			
11	Ellma - NT Ltd, Leningrad region			
12	"Chimprom", Joint stock company, Novocheboksary	—	—	2000 not started
Ukraine				
13	Titan - magnesium Combmat, Zaporizhzhya		750	20000
14	The pure metals factory, Svetlovodsk	50	—	—
15	Chemical - metallurgical plant, Donetsk	25	—	—
16	Crystall Ltd, Kiev			
Kyrgyzstan				
17	Mining Metallurgical factory, Bishkek region	36	—	—
18	Tash - Kумыr factory of semiconductor materials, Oschskaja region, Phase of construction and renovation	—	500 not started	5000

The third project is offered by Ministry of Nuclear industry for Nuclear facilities in Krasnojarsk and Cheljabinsk. Completed project 1000 MT of polysilicon and associated 20000 MT trichlorosilane is estimated to cost 200 million US\$. This project is sponsored by the DOE IPP Program.

Japanese firm Sumitomo is imported silicon from Kyrgyzstan and Ukraine. Kyrgyzstan is planning to start production of polysilicon and trichlorosilane in Tash-Kumyr factory. The capacity is 500 MT polysilicon and 5000 trichlorosilane per year.

Kazakhstan and Uzbekistan are also offered the projects to start silicon production for electronics and PV industry. Institute of Physics and Technology in Almaty proposed a project "Development of Scientific Basis and Technology for silicon production from the wastes of phosphorous industry". The wastes resources are estimated as more than 10 millions MT. The content of silicon dioxide is 45 %. This technology using aluminothermic exothermic process wastes + Al = Si (99,9%) + high quality cement. Monosilane synthesis and refine methods will be applied for adaptation of the developed technology to industrial standards. "NATO Program for Peace" is asked for financial support of this project.

VIII. CONCLUSIONS

Russia and other CIS countries have large resources of high purity quartz, well developed silicon industry, vast scientific technological potential, highly qualified and low labor cost specialists and cheap energy to produce cost-competitive semiconductor and solar grade silicon with annual capacity more than 1500 MT.

The traditional chlorosilane technologies of crystalline silicon have a low silicon yield, the high-energy consumption, they are ecologically dangerous and consequently are unacceptable for large - scale application in the future.

Research and Development of new solar grade silicon technologies must attract the interest of investors as well as the governments of Russia and other CIS countries since solar photovoltaic energy conversion will have a strategic role and will be one of the greatest challenges of 21 century.

New environmentally friendly solar grade silicon technologies are ready for final development and commercialization.

Principal feature of this techniques is exemption of the chloride products from processing cycle, absence of noncommercial wastes and utilization of widely spread raw materials, like high purity quartz, carbon soot, metallurgical quality silicon and alcohol.

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QUANTITATIVE MODELLING OF NUCLEATION KINETICS IN EXPERIMENTS FOR POLY-Si GROWTH ON SiO₂ BY HOT-WIRE CHEMICAL VAPOR DEPOSITION

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ABSTRACT

We apply a rate-equation pair binding model of nucleation kinetics¹ to Si islands grown by hot-wire chemical vapor deposition on SiO₂ substrates. Previously, we showed an increase in grain size of polycrystalline Si films with H₂ dilution (H₂:SiH₄), which we attribute to atomic H etching of Si monomers during the early stages of nucleation rather than stable Si clusters, decreasing the nucleation density.² Atomic force microscopy measurements performed at low substrate coverage show a sublinear increase in the nucleation density with time, implying a fast nucleation rate until a critical density is reached, after which grain growth begins. The cluster density decreases with increasing H₂ dilution, due to etching, and with increasing temperature, due to enhanced Si monomer diffusivity on SiO₂. From temperature-dependent cluster density measurements, we estimate the activation energy for surface diffusion of Si monomers on SiO₂ to be 0.47 ± 0.09 eV. Simulations of the temperature-dependent supercritical cluster density give an estimated activation energy of 0.42 ± 0.01 eV and an estimated surface diffusion coefficient prefactor of 0.1 ± 0.03 cm²/s. H₂-dilution-dependent simulations of the supercritical cluster density show an approximately linear relationship between the H₂ dilution and the etch rate of clusters.

INTRODUCTION

A major driving force behind research and development in the photovoltaics industry is a reduction in cost of the finished module. Since more than half the cost of a finished module comes from the material itself, thin-film crystalline silicon is an attractive technology. In 1999, Kaneka Corporation demonstrated a 2 μm-thick poly-Si solar cell with V_{oc} of 0.539 V and a record 10.7% efficiency.³

Hot wire chemical vapor deposition (HWCVD) is an attractive method for fast growth of polycrystalline Si over large areas for thin film photovoltaics applications.^{4,5} A key issue is to identify growth conditions that produce the largest possible grain size at a given growth temperature with low intragranular defect density. Hydrogen is known to play a critical role in the development of a crystalline microstructure in both polycrystalline^{6,7} and epitaxial⁸ films grown by HWCVD at low temperatures and high growth rates compared to PECVD. The role of atomic H produced by the wire in Si etching and its effect on the resulting film microstructure are investigated through experimental measurement and quantitative modelling of the nucleation kinetics of Si on SiO₂.

EXPERIMENT

In all experiments, performed at pressures of no higher than 1×10^{-6} Torr, a W wire of 0.25 mm diameter 2.5 cm from the substrate was resistively heated to 2000°C. The wire radiatively heated substrates of 100 nm SiO₂ on Si to 300°C; higher substrate temperatures were achieved with a resistive substrate heater in combination with the wire. H₂ dilutions are referenced to 1 mTorr of SiH₄ in 99 mTorr He; all gases are ultrahigh purity. A translatable shutter between the wire and substrate enabled multiple growth experiments to be performed on each substrate under identical gas ambient and wire temperature conditions, and provided a definite start and endpoint for film growth.

RESULTS

Previously, evidence for atomic H etching of Si was demonstrated by H₂-dilution-dependent measurements of the net Si growth rate with a quartz crystal deposition monitor at the substrate position as well as by a separate experiment which measured the flux of SiH₄ with a differentially-pumped quadrupole mass spectrometer with orifice at the substrate position.² A decrease in growth rate and corresponding increase in SiH₄ flux with increasing H₂ dilution were attributed to atomic H etching of Si species from the substrate and chamber walls and recombination of these species in the gas phase. Further evidence for etching was provided by transmission electron microscopy of continuous films grown on SiO₂ at 20:1 H₂ dilution, in which no initial amorphous layer was present. These findings were explained by a competitive etching mechanism in which atomic H etches crystalline Si more slowly than it etches amorphous Si.⁷

In subsequent experiments, the nucleation density at low Si coverage on SiO₂ was determined using AFM, as illustrated in Figure 1 (a), for H₂ dilutions between 0 and 80:1 in the region nearest the wire. As seen in Figure 2, the nucleation density increased sublinearly with time, implying an initially high nucleation rate until a critical cluster

$$\frac{1}{\tau_a} = Y\Phi_H f_{n1}. \quad (5)$$

Simulation predicts a maximum monomer concentration on the order of 10^6 cm^{-2} and a monomer coverage fraction f_{n1} of 10^{-9} . Φ_H is on order $10^{16} \text{ cm}^{-2}\text{s}^{-1}$. The etch rates (on the order of 10^6 s^{-1}) predicted by the simulation in turn predict a reasonable etch yield of Si by atomic H of $Y=0.1$, and show an approximate linear relationship with H_2 dilution, shown in Figure 4. This suggests that atomic H etching of monomers, rather than competitive etching of supercritical amorphous and crystalline nuclei, may be the dominant process governing the low-coverage nucleation kinetics.

CONCLUSIONS

An increase in grain size of polycrystalline Si films with H_2 dilution can be attributed to atomic H etching of Si monomers, decreasing the nucleation density. Through temperature-dependent nucleation-density measurements, the activation energy for diffusion of Si monomers on SiO_2 is estimated to be $0.47 \pm 0.09 \text{ eV}$. To our knowledge, this is the first estimate for this activation energy given in the literature.

The experimental nucleation density measurements can be understood within the framework of a rate-equation pair-binding simulation. Modelling of the temperature-dependent cluster density measurements give $D_0=0.1 \pm 0.03 \text{ cm}^2/\text{s}$ and $E_a=0.42 \pm 0.01 \text{ eV}$, which is within the error in the experimentally determined value. Monomer etching by atomic H is simulated by changing the adatom stay time τ_a , and the simulated etch rates vary approximately linearly with H_2 dilution.

ACKNOWLEDGEMENTS

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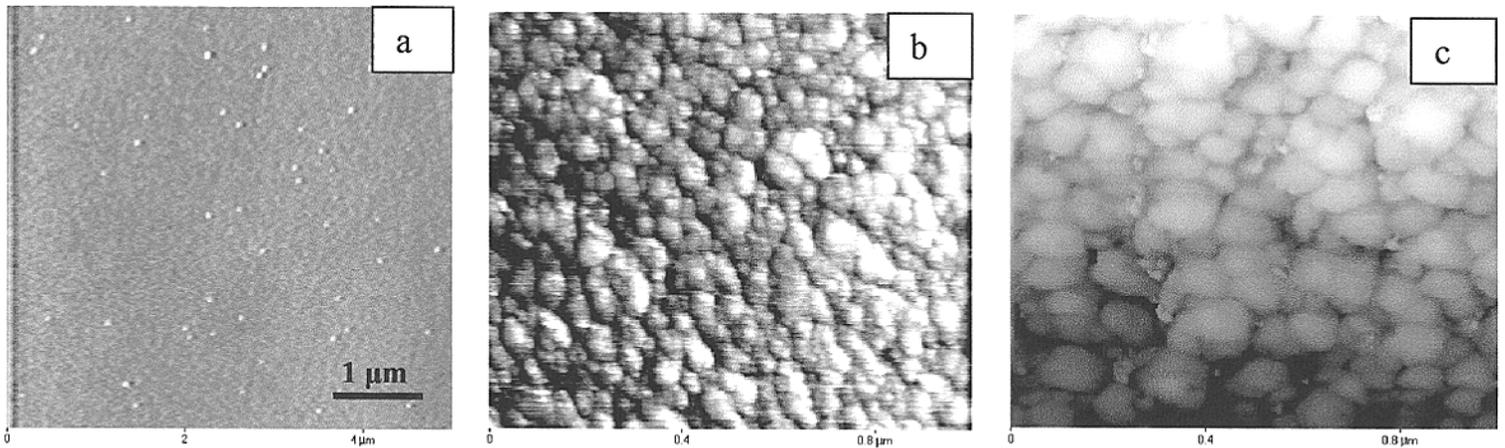


Figure 1. (a) AFM image of a HWCVD film grown at 20:1 H_2 dilution for 90 s, illustrating the nucleation phase; bright features are 35 nm in height. (b) Post-coalescence $1 \mu\text{m}^2$ image of a continuous poly-Si film grown at 0 H_2 dilution; grain size is 40 nm. (c) Post-coalescence $1 \mu\text{m}^2$ image of a continuous poly-Si film grown at 20:1 H_2 dilution; grain size is 85 nm.

density is reached, at which time the nucleation rate is sharply reduced and grain growth begins. The cluster density was greatest for no added H₂ and decreased with H₂ dilution. This result is consistent with the AFM micrographs in Figure 1 (b) and (c), which show an increase in grain size of continuous films (~200 nm) from 40 nm with no H₂ dilution to 85 nm at a H₂ dilution of 20:1.

The nucleation density also decreased with increasing temperature due to enhanced diffusivity of Si on SiO₂, as in Figure 3 (a). From temperature-dependent nucleation density measurements performed at substrate temperatures of 300-450°C, we estimate the activation energy for surface diffusion of Si on SiO₂ to be 0.47 ± 0.09 eV.

MODELLING

We quantitatively model the observed nucleation kinetics of Si on SiO₂ through a rate-equation pair binding framework developed by Venables [1], which assumes that only Si monomers n_1 are mobile on the surface. The equations governing the density n_j of clusters of size j are

$$\frac{dn_1}{dt} = R - \frac{n_1}{\tau_a} - \frac{d(n_x w_x)}{dt}, \quad (1)$$

$$\frac{dn_j}{dt} = 0 \quad (2 \leq j \leq i), \quad (2)$$

$$\frac{dn_x}{dt} = \sigma_i D n_1 n_i - 2n_x \frac{dZ}{dt}. \quad (3)$$

Equation (1) describes the evolution of the monomer population n_1 due to arrival of atoms from the gas phase at rate R , evaporation with time constant τ_a , and incorporation into existing clusters, where $n_x w_x$ is the total number of atoms in existing clusters. Equation (2) gives a thermodynamic equilibrium between subcritical clusters, and Equation (3) gives the supercritical cluster density n_x in terms of a nucleation rate $\sigma D n_1 n_i$ and a coalescence rate proportional to the rate of change of the substrate coverage Z by stable clusters. Equations (1) and (3) are coupled by the interaction between nucleation and growth, whereby adatoms incorporate into stable clusters by nucleation, diffusion capture, and direct impingement, so that

$$\frac{d(n_x w_x)}{dt} = \frac{n_1}{\tau_n} + \frac{n_1}{\tau_c} + RZ \quad (4)$$

where $\tau_c = \sigma_x D n_x$. The nucleation term τ_n is unimportant numerically and can be ignored; the capture numbers σ and the diffusion coefficient $D = D_0 \exp[-E_a/kT]$ are given by the solution of the two-dimensional diffusion equation on the substrate.

For a critical cluster size $i=1$, which predicts the lowest monomer density on the surface, and a rate $R=5 \times 10^{10} \text{ cm}^2 \text{ s}^{-1}$ corresponding to experiment, we estimate the diffusion coefficient prefactor D_0 and the activation energy E_a for Si diffusion on SiO₂ by using the model to fit the temperature-dependent nucleation density measurements, as in Figure 2 (b). The data are best approximated with values of $D_0=0.1 \text{ cm}^2/\text{s}$ and $E_a=0.42 \text{ eV}$. Increasing E_a causes the linear regime of the simulated supercritical cluster density curves to persist for longer times; increasing D_0 causes the family of curves to display an increased supercritical cluster density. The simulated curves fit the experimental data within a factor of two; simulation parameters were chosen so as to generally overestimate the experimental cluster densities, as supercritical clusters which cannot be resolved with the AFM likely exist on the substrate. The simulated value of E_a is within the error of the least-squares fit used to determine E_a experimentally.

To model the effects of hydrogen dilution at substrate temperatures of 300°C and 400°C, the adatom stay time τ_a was modified to account for the etching of monomers from the substrate by atomic H. The results are shown in Figure 4. The difference in the values of τ_a at identical dilution for the two temperatures suggests a temperature-dependent reactive etching mechanism for Si monomers by atomic H. The rate at which adatoms are etched from the substrate by atomic H should be proportional to the etch yield Y of Si by atomic H, the flux Φ_H of atomic H at the surface, and the fraction f_{n1} of the substrate covered by monomers, such that

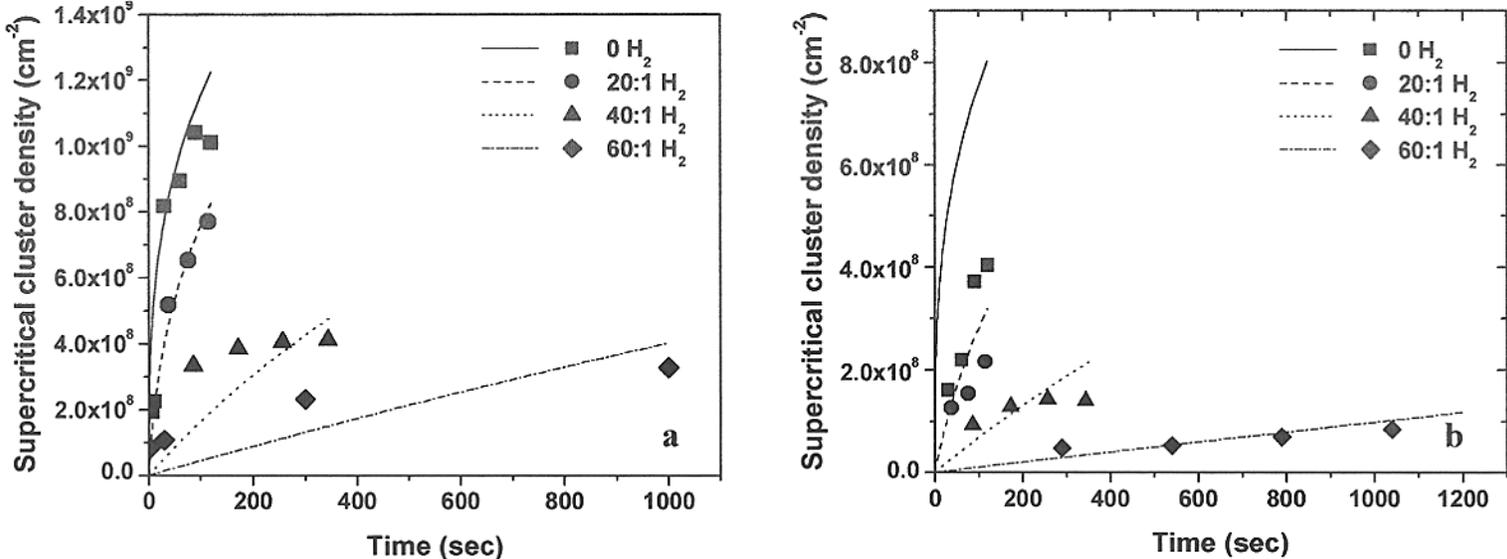


Figure 2. Experimental (points) and simulated dilution-dependent cluster density measurements at (a) 300°C and (b) 400°C.

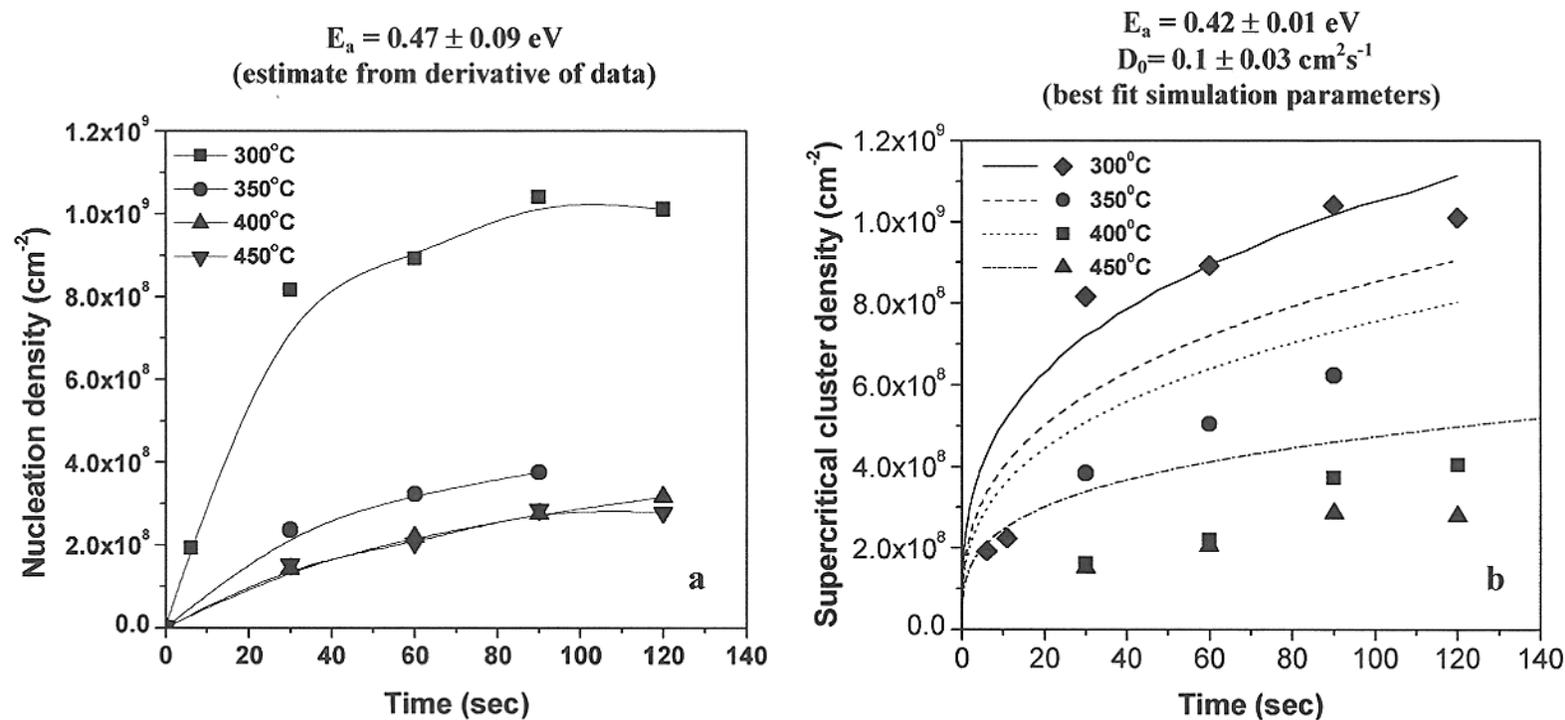


Figure 3. (a) Experimentally-determined temperature-dependent nucleation densities; the lines are a guide to the eye. (b) Comparison of simulated (curves) and experimentally-determined temperature-dependent supercritical cluster densities.

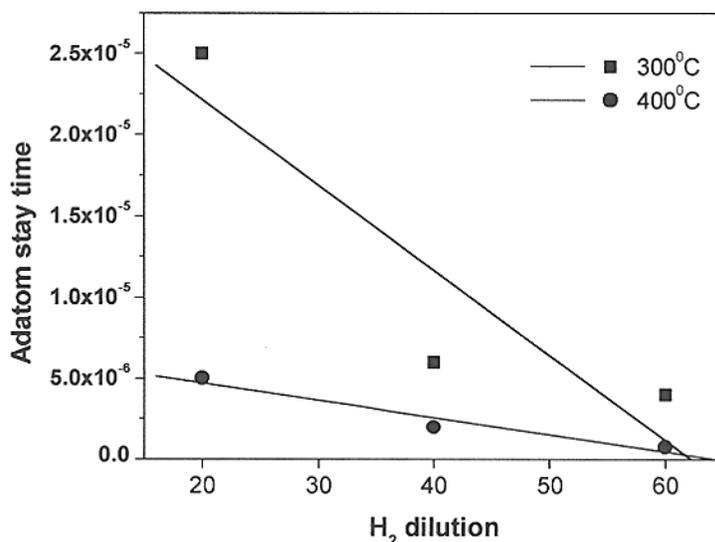


Figure 4. Variation of simulation parameter τ_n , representing adatom stay time, with H₂ dilution.

Influence of copper on the carrier lifetime of n-type and p-type silicon

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Abstract. Controlled contamination by ion implantation and careful surface passivation has been used to study the effect of copper on the recombination rate of charge carriers in silicon wafers. Our results confirm that copper strongly reduces the lifetime of n-type silicon, which approximately follows an $N_{\text{Cu}}^{-0.55}$ dependence on the copper dose. The effect of copper on p-type silicon, commonly used for solar cells, has been found to be as severe as on n-type silicon, when wafers having a similar dopant concentration are compared. The lifetime of copper contaminated silicon, both n-type and p-type is correlated to the phosphorus or boron concentration, respectively, with decreasing lifetimes corresponding to increasing doping levels. The fact that both the copper dose and the dopant concentration have a strong effect on the lifetime is an essential consideration for future studies of copper in silicon.

1. Introduction

Understanding the electronic consequences of copper contamination has become very important for integrated circuit technology and for silicon solar cells. Copper contamination is likely to occur during the wafering of photovoltaic silicon. A 1980 study of the effect of various impurities on the conversion efficiency of silicon solar cells [1] concluded that copper was the least damaging transition metal and indicated that concentrations of up to 10^{17}cm^{-3} could be tolerated. This presumed innocuity prompted the growth of silicon layers from copper solutions to develop thin film solar cells [2]. There is growing evidence, however, that copper has serious negative effects on carrier recombination. Experimental work by Naito et al. [3], cited in a recent review [4], found that copper contamination degraded the lifetime of n-type silicon by almost two orders of magnitude for a surface impurity concentration of 10^{13}cm^{-2} . Surprisingly, the effect of copper on p-type silicon was found to be much weaker, with a factor of three reduction at a 10^{13}cm^{-2} dose and no degradation for lower contamination levels. Zhong et al. [5] did notice a factor of ten drop in the lifetime of p-type wafers having a $6 \times 10^{13}\text{cm}^{-2}$ surface copper concentration. Rotondaro et al. [6] found that copper degraded the lifetime of n-type silicon drastically, from 700 μs to 20 μs , but did not practically affect p-type wafers. This was also the qualitative result of Henley et al. [7], who nevertheless observed that the lifetime of p-type

silicon dropped, and drastically so, after optical or thermal activation. Thermal and optical activation were later found to be equivalent [8], with a total degradation of the lifetime of p-type silicon occurring after 15 min at 300°C. Tarasov et al. [9] further verified the irreversibility of the lifetime degradation after light activation, which is a distinctive feature that may be used to discern between copper and iron, since the latter permits a recovery of the lifetime after several hours in the dark. In addition, they measured an increasing degradation of the minority carrier diffusion length of p-type silicon with increasing copper dose. This recent evidence together with that presented in this paper, strongly suggests that the earlier preconception that p-type silicon was practically impervious to copper is wrong.

In this paper we investigate the following questions: how much copper is required to produce a noticeable degradation of the lifetime and how strong the effect is as the concentration of copper is augmented, whether p-type silicon is degraded by the presence of copper and what influence may wafer doping have.

2. Experimental techniques

CZ n-type, 5-10 Ωcm , 350 μm thick silicon wafers and FZ p-type and n-type wafers of various resistivities were used in the experiments. Copper doses of 10^{12} , 10^{13} and 10^{14}cm^{-2} were ion implanted at 80keV into the silicon wafers. Following Cu implantation, the

wafers were RCA cleaned, annealed at 850 °C for 1h in argon and pulled out of the furnace to room temperature without any particular quenching. This annealing step serves the dual purpose of healing the implantation damage and distributing the copper uniformly across the wafer. Approximately 10 μ m of silicon were subsequently etched off each side of the wafers in a nitric:HF solution. This helps to further eliminate residual implantation damage and possible copper pile-up at the surface [5]. Finally, SiN was deposited on both sides in a PECVD reactor at 400°C (deposition time approximately 5 min per side) to provide good surface passivation. Lifetime measurements were then performed as a function of the excess carrier concentration using the quasi-steady-state photoconductance technique [8]. Control wafers were included in every experiment to verify that no unwanted contamination occurred during the annealing step and that the surface passivation was of sufficient quality.

3. Dependence of the lifetime on copper dose

To study the effect of copper contamination level, we initially used 7.5 Ω cm, 350 μ m thick CZ n-type, silicon wafers. Although the out diffusion of copper from the wafers cannot be completely excluded, earlier neutron activation analysis of Cu implanted and annealed wafers indicated that this effect is very small in our experimental conditions [9]. A dose of 10¹³cm⁻² can therefore be expected to produce a total copper concentration in the range of 3x10¹⁴cm⁻³ in these wafers, which is relatively high, by comparison to the dopant density of approximately 6x10¹⁴cm⁻³. Such a copper concentration produced a ten fold reduction of the minority carrier lifetime, from about 1ms of the non-contaminated wafer to approximately 100 μ s. A lower dose of 10¹²cm⁻² resulted in less degradation, while for a dose of 10¹⁴cm⁻² the lifetime dropped to approximately 10 μ s. Fig.1 gives the low injection lifetime measured for wafers implanted with copper doses of 10¹², 10¹³ and 10¹⁴ cm⁻². The line fit corresponds to a $N_{Cu}^{-0.55}$ lifetime dependence, where N_{Cu} is the copper dose. Considering the the SRH lifetime should, in principle, follow an inverse dependence on the trap concentration, the observed dependence suggests that there probably is a varying degree of copper precipitation with increasing dose. Compared to the control wafer, shown as the left-most point in Fig.1, this strong dependence of the lifetime

on copper dose is a clear evidence of the detrimental effects of copper contamination.

Some experiments were repeated up to three times, and the lifetime of samples implanted with the same copper dose was not perfectly repeatable. This variability, which is represented by the error bars in Fig.1, is attributed to slightly different cooling rates between the three experiments. Copper precipitates rapidly [7] and slight changes in the cooling rate are likely to affect the number of recombination centres that form in the bulk of the wafer. Variations in the implanted dose or unintended contamination are not believed to be responsible, since both were carefully controlled. The variability observed for the non-implanted control samples is attributed to a slightly different surface passivation quality; this is, nonetheless, relatively unimportant in these experiments.

A similar degradation of the lifetime with increasing copper concentration can be expected for p-type silicon. Tarasov et al. [9] indeed observed such behaviour through minority carrier diffusion length measurements of lowly doped 27 Ω cm p-type silicon, particularly when the wafers were furnace annealed at 1000°C and quenched into liquid nitrogen. Compared to a control sample, degradation factors of 2.5, 4-12 and 37 times were found for surface copper concentrations of 10¹²cm⁻², 10¹³cm⁻² and 10¹⁴cm⁻², respectively.

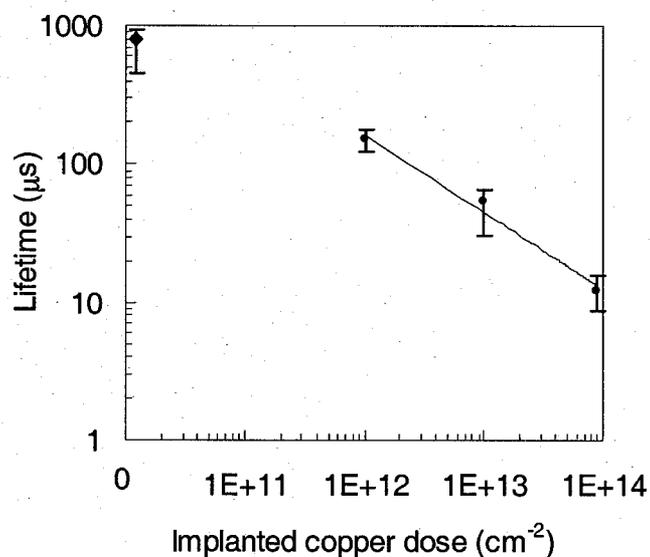


Figure 1. Minority carrier lifetime measured for copper contaminated n-type 7.5 Ω cm CZ silicon wafers. The left-most data point corresponds to the non-implanted control wafers.

4. Injection level dependence of the lifetime

Fig.2 presents the lifetime as a function of injection level for copper contaminated wafers from a single, simultaneous experiment. A strong lifetime dependency with excess carrier concentration is present for the 10^{12}cm^{-2} and, to a lesser extent, for the 10^{13}cm^{-2} Cu dose. The lifetime increases with increasing excess carrier concentration, reaches a maximum at approximately $5 \times 10^{15}\text{cm}^{-3}$ (note that the dopant density is $6 \times 10^{14}\text{cm}^{-3}$) and drops thereafter due to Auger recombination. This behaviour is typical of Shockley Read Hall recombination when the capture cross sections of electrons and holes are strongly asymmetric and the energy level is within a broad range around the middle of the band gap (that is, excluding shallow levels). Previous research [4,6] has identified two main trap energy levels for copper in n-type material, one at $E_c - 0.16\text{eV}$, believed to be due to free interstitial copper with an electron capture cross section of $3.3 \times 10^{-17}\text{cm}^2$ and a second level at $E_c - 0.4\text{eV}$ due to copper precipitate related defects, with an electron capture cross section of $2 \times 10^{-10}\text{cm}^2$. There is little information on the hole capture coefficients and this makes it difficult to accurately model the measured injection level dependence of the lifetime. Nevertheless, preliminary theoretical analysis suggests that copper related centres with deep or intermediate energy levels dominate carrier recombination in these wafers. A second, shallower level, seems to be present in the high resistivity samples, but is not the dominant centre at injection levels of practical interest.

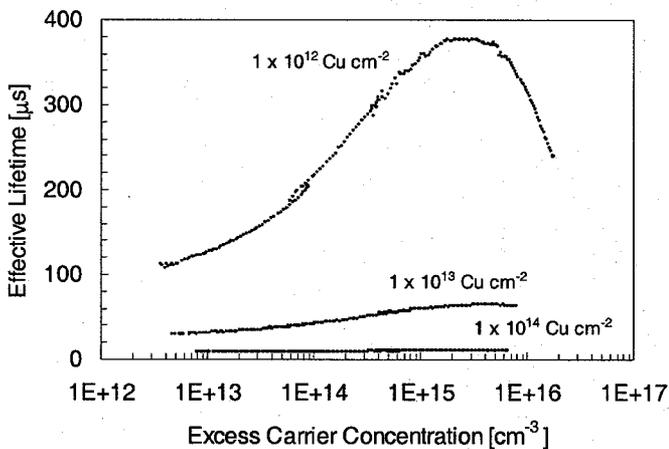


Figure 2. Effective lifetime of n-type 7.5 Ωcm silicon as a function of excess carrier concentration for implanted copper doses of 10^{12} , 10^{13} and 10^{14}Cu cm^{-2} .

As the copper dose is increased, the dependence on excess carrier concentration is less marked. This may indicate a change in the dominant recombination centres (different capture cross-sections, different energy level, or both). It can be expected that the proportion of precipitated copper increases with its concentration.

5. Doping dependence of the lifetime of copper contaminated wafers

Given that copper reduces the lifetime to quite low values, it may be expected that the lifetime of equally contaminated wafers would be dominated by the Cu-related centres and be practically independent of the original, pre-contamination lifetime of the wafers. To investigate this we used phosphorus doped wafers with resistivities between $0.75\Omega\text{cm}$ and $75\Omega\text{cm}$ and corresponding initial lifetimes between $330\mu\text{s}$ and more than 1ms. Companion wafers were contaminated with a copper dose of 10^{13}cm^{-2} . A similar experiment was conducted with float zone p-type wafers with resistivities from $0.3\Omega\text{cm}$ to $70\Omega\text{cm}$. The p-type control wafers presented lower lifetimes than what is customary for this type of material and may be affected by a non-optimal SiN surface passivation. Nevertheless, the passivation quality is sufficient to reveal the effect of copper contamination.

Both the n-type and p-type wafers showed a strong reduction of the lifetime due to copper contamination, but the higher resistivity wafers were able to better maintain a reasonable lifetime than the lower resistivity ones. As Fig. 3 shows, there is a correlation between the low injection effective lifetime and the density of dopant atoms (either phosphorus or boron) in the wafer. Such correlation can be expected for SRH centres that are not too deep, but are in the transitional region between deep and shallow. The recombination strength of such intermediate centres increases considerably with doping concentration. Note that the observed dependence is not wholly attributable to the effect of copper, since the control wafers also show a trend to lower lifetimes with increasing doping. The results indicate, nevertheless, that there is a synergistic effect between copper contamination and wafer doping.

The degradation of p-type silicon is even stronger than for n-type material with a similar dopant concentration. This contradicts most previous reports [3,5,6] that copper contamination had little effect on p-

type silicon wafers. Although qualitatively in agreement with our results, the lifetimes in [9] are quantitatively lower. For a copper dose of 10^{13} cm^{-2} (measurement technique not specified) the latter researchers measured lifetimes of $0.7\mu\text{s}$ and $9.3\mu\text{s}$ for a doping density of $5 \times 10^{14} \text{ cm}^{-3}$, while our measurement for a similar wafers is in the vicinity of $100\mu\text{s}$.

It is important to note that, in the light of the evidence in [7,8] that the lifetime of p-type silicon is considerably reduced after thermal or optical activation, our lifetime values should be considered characteristic of the activated state of the copper-related recombination centres, due to the deposition of a surface passivating SiN layer at 400°C . Such annealing temperatures are also common in device processing, as a forming gas anneal to reduce interface states or a sintering of the metal contacts. For the typical resistivity used for silicon solar cells, p-type $1 \Omega\text{cm}$, copper can produce a very serious degradation of the minority carrier lifetime, from more than $120\mu\text{s}$ to slightly less than $10\mu\text{s}$. The degraded lifetime is, of course, relevant to solar cell operation.

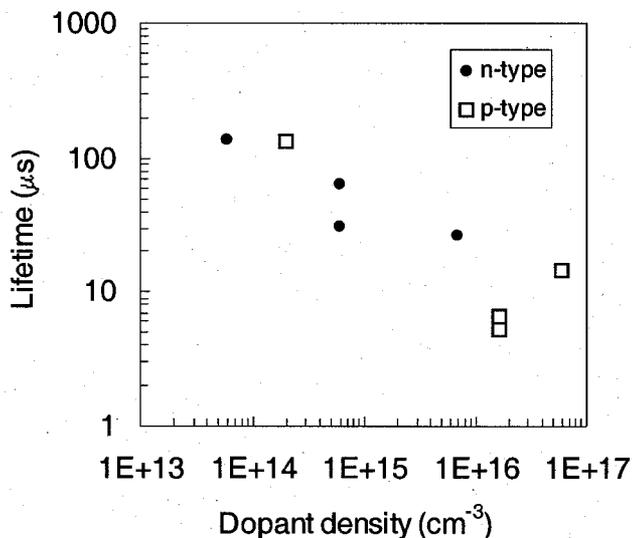


Figure 3. Dependence of the lifetime on the dopant concentration of n-type and p-type silicon wafers contaminated with a 10^{13} cm^{-2} copper dose.

6. Conclusions

Our experiments clearly show that copper contamination strongly degrades the minority carrier lifetime of both n-type and p-type silicon. This is contrary to previous findings that p-type silicon was almost insensitive to copper contamination and

stresses the importance of avoiding copper contamination in commonly used photovoltaic silicon materials. The reason for early researchers not having observed a strong degradation may be the recent evidence that the copper-related recombination centres dominant in p-type material are activated by light or temperature. Compared to other metals like iron, the levels of copper required to produce a drastic reduction of the lifetime are relatively high and relatively acceptable lifetimes are still found for heavily contaminated silicon. For example, the lifetime of $1\Omega\text{cm}$ p-type silicon is nearly $10\mu\text{s}$ for a copper concentration of approximately $3 \times 10^{14} \text{ cm}^{-3}$, which is consistent with a diffusion length of $160\mu\text{m}$. Higher copper doses degrade the lifetime even further, and a saturation of this trend was not yet found for a concentration of $3 \times 10^{15} \text{ cm}^{-3}$. It is also important to note that the lifetimes that can be achieved for a particular copper concentration are very different depending on the resistivity of the wafer, with lower lifetimes corresponding to lower resistivities. This is an important fact that has been generally overlooked. The fact that both the copper dose and the dopant concentration have a strong effect on the lifetime is important for future studies of copper in silicon. A multi-factorial study complemented with a detailed analysis of the injection level dependence of the lifetime could increase the limited present knowledge of this important metal impurity.

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A COMPACT, CONTACTLESS LIFETIME TESTER USING THE RESONANT-COUPLED PHOTOCONDUCTIVE DECAY TECHNIQUE

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We have developed a contactless technique that has proven extremely useful for measuring recombination lifetimes in all classes of semiconducting materials. These include Se, Ge, SiC, GaAs, InGaAs, CdTe, CdS and many other compound semiconductors. The technique is versatile as to allow measuring sample size ranging from small-area epitaxial thin films to large diameter (8-10 inches) used in silicon integrated circuit applications. The compact system uses a mini-YAG laser with fixed wavelengths of 1064 and 532 nm. It is designed for silicon wafer diagnosis but can be used for all of the semiconducting materials.

The resonant-coupled photoconductive (RCPCD) system is a contactless, nondestructive method that can be used to determine the recombination lifetimes of both direct- and indirect-bandgap materials. Because the semiconductor bandgap is not a factor in the application of the technique, bandgaps as small as 0.1 eV have been measured. The measurement is very rapid, producing immediate feedback of the minority-carrier properties. A companion laboratory system provides instant, real time lifetime analysis in fractions of a second. Thus, it is suitable for laboratory, processing, or production environments.

Theory of Operation

The RCPCD apparatus includes a semiconductor sample stage that is positioned at variable distances from an antenna. The sample is placed on an adjustable stage such that the sample becomes part of a coupled antenna array. The sample absorbs and reradiates the primary electromagnetic waves (EMW) in phase with the driving antenna. The intensity of the re-radiated EMW is a function of the dark and excess carrier concentration. The driving antenna absorbs the photogenerated EMWs and transforms the energy into an ac voltage

in the detecting circuit. Thus, the induced voltage is proportional to the amplitude of the electric vector that is the component of the secondary EMWs. The antenna is part of a high-Q tuned circuit with dissipative (real resistance) being the radiation resistance of the array (antenna plus sample). The network is driven through a directional coupler and the mechanical positioner is adjusted for each sample so that the reflected power is zero. The drive frequency is chosen to be near the half-power point of the resonant circuit so that a small change in sample conductivity produces a large change in reflected power.

In the detection circuit, the reflected voltage is amplified and sent to a high-frequency mixer. There, it is mixed and matched in phase with a reference signal. Thus, the detection circuit is phase-locked to the driving circuit so that only those EMWs are detected that are in phase with those produced by the driving circuit. The mixer creates a dc signal proportional to the excess carrier density and sends it to a wide-band dc amplifier to increase the amplitude. The output of the dc amplifier is sent to a digital storage oscilloscope, where it is digitized in memory and sent to a computer for further processing and displaying of the minority-carrier lifetime. An analysis of this system shows that the response is linear over more than three orders of magnitude of the photoconductive signal.

Sensitivity

Measurements with high quality float zone-grown wafers indicate that a meaningful signal could be obtained with an energy flux as small as 6×10^{10} photons/pulse cm^2 . These data were obtained using a pulsed light source (20 pps) and a photon energy of about 1.2 eV. The average incident power in the pulse train is about $0.3 \mu\text{w}/\text{cm}^2$ or about six orders of magnitude less than that of the solar spectrum at AM1.5.

Ancillary Data

An analysis of the measurement shows that the photoconductive signal is given by the following equations. The RCPCD apparatus measures the transient

ambipolar photoconductivity $\Delta\sigma(t)$ following pulsed excitation, which can be written as:

$$\Delta\sigma = q(\mu_n + \mu_p)\rho(t) \quad 1)$$

Here, μ_n (μ_p) are the electron (hole) mobilities, and $\rho(t)$ is the photocarrier concentration. For pulsed, monochromatic light, we can write the photoconductivity as:

$$\Delta\sigma(t) = qI_0(\mu_n + \mu_p)(1 - \exp(-\alpha d))\exp(-t/\tau) \quad 2)$$

Here, α is the absorption coefficient, d is the wafer thickness and I_0 is the number of photons/cm² in the pulse. Also, μ_n and μ_p are the electron and hole mobilities, respectively. Using the mobility ratio b ;

$$b = \frac{\mu_n}{\mu_p} \quad 3)$$

The ratio is about 4.0 for silicon, and using strongly absorbed light, such that αd is a large number, we can simplify the above and write the following expression for the initial pulse height.

$$V(0) = qI_0\mu_n\left(1 + \frac{1}{b}\right) A_{\text{sys}} \quad 4)$$

Here, $V(0)$ is the initial pulse voltage and A_{sys} is the measurement system constant. By measuring the pulse energy and using a standard, characterized crystal to calibrate the system constant, A_{sys} one can measure the mobility in any sample from the pulse amplitude. Knowing the mobility and lifetime, the electron diffusion length is easily calculated. Using the same approach, the integrated area under the decay curve is proportional to the square of the diffusion length. In this case, a standard can also be used to calibrate the system constant (B_{sys}) with a wafer of known parameters.

$$L_n^2 = B_{\text{sys}} \int_0^{\infty} V(t)dt \quad 5)$$

Comparison with Microwave Reflection

The standard technology for measurement of silicon lifetime is currently microwave reflection. The table below shows a comparison of the RCPCD system with commercial microwave reflection systems.

Characteristic	μ-PCD	RC-PCD	Comments
Contactless measurement	Yes	Yes	Important for production-line applications
Sensitivity (minimum detectable photons/pulse-cm ² for pure silicon)	5×10^{13}	6×10^{10}	Allows more accurate determination of material quality over wider range of materials
Dynamic range (i.e., $\Delta n/n$ maximum*)	0.05	1000	Critical for determining lifetimes over a wide range of injected and doping carrier densities; for modeling device operation; and for injection-level spectroscopy
Dark Carrier Compensation	No	Yes	The sample-antenna positioning is an operation that balances out the dark conductivity of the sample, thus improving instrument signal-to-noise
Measurement Reliability	High	High	
Sample type: wafers	Yes	Yes	Sample type and configuration flexibility
Sample type: thin films	Yes	Yes	
Sample type: ingots	No	Yes	
Measurable semiconductor materials	All	All	Applicable to a wide range of materials
Penetration depth of probe (max limit of probing depth – 0.1 ohm-cm to 10 ohm-cm)	150 – 2000 μ m	800 – 10000 μ m	Flexibility in probing large-volume samples such as thick wafers and ingots. Particularly relevant for heavily doped wafers.
Largest conductivity for which measurement possible. (ohm-cm) ⁻¹	1.0	100	Allows determination of material quality for a wide range of materials from undoped to extremely heavily doped
Minimum lifetime resolution	1 ns	5-20 ns	
One-Sided (probe field and optical pump incident from same side of sample)	Yes	Yes	Allows better characterization of recombination; and allows sample to be immersed in an electrolytic bath
Mobility and diffusion length can be obtained from measurement	No	Yes	Especially useful for photovoltaic applications

In summary, the RCPCD technique is versatile and applicable to a wide range of materials. Data acquisition is very rapid (several seconds or less) and is therefore adaptable to production environments.

Calibration and Error Analysis of High Accuracy Residual Stress Polariscopes

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Abstract

This research addresses the non-contact measurement of in-plane residual stress in thin silicon sheet by an infrared transmission system. Silicon is transparent to near infrared light and the transmission of IR can be used to construct birefringence fringe patterns in large-area sheet samples.

Birefringence caused by residual stresses is proportional to the thickness of the sample and the stress level. The fringe order is low for silicon samples with low residual stresses. A new near infrared phase stepping polariscopes with a high fringe multiplier using a pair of partial mirrors has been developed to overcome this difficulty. The sensitivity of the system can be increased by one to two orders of magnitude.

The system error of the mismatch of two quarter-waveplates, analyzer, and digitalization error of the camera is analyzed and calibrated by four-point bending with series of loads for different multiplication factors. The results demonstrate that the system resolution is ~ 1.0 MPa. Preliminary residual stress results for $\langle 111 \rangle$ silicon grown by the dendritic WEB technique will be presented.

Key words: polariscopes; phase stepping; error analysis; system calibration.

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Keywords : silicon, gold, gettering, nanocavities, self-interstitials, implantation, helium, hydrogen

Abstract. In Cz wafers, the trapping of gold by defects and nanocavities formed by implantation of He⁺⁺ or H⁺ ions at 250 keV and at a dose of $3 \cdot 10^{16}$ cm⁻² followed by subsequent annealing(s) at 750°C for 1 hour, is investigated. Deep level transient spectroscopy profiles show that substitutional gold concentration decreases near the cavity band. Gold profiles obtained by secondary ion mass spectroscopy show that there is a strong trapping of gold in the cavity band in all samples and it is shown that nanocavities may be used to protect the wafers from contaminations during processing steps.

Introduction

The use of light ions like He⁺⁺ or H⁺ has given rise to very efficient gettering processes, which are due to the creation of nanocavities [1 to 6]. Indeed, the solid solubility of noble gases like helium or hydrogen is very low in silicon ($< 10^{16}$ cm⁻³) and so, bubbles form when the dose of ion implantation leads to a bulk concentration higher than this value. Then, nanocavities are formed after subsequent annealing at a temperature between 300°C and 700°C [7] because in this temperature range, helium or hydrogen tends to diffuse from the bubbles. The internal surfaces of the cavities, probably covered by unsaturated silicon bonds, behave as efficient trapping sites. Moreover, gettering also occurs when the wafers are annealed during the processing steps and contamination by fast diffusers could be markedly reduced as these atoms may be trapped by the nanocavities. In this work, metallic contamination will be simulated by in-diffusion of gold atoms and the gettering of these atoms by nanocavities is investigated.

Experimental

P type Czochralski (Cz) grown monocrystalline silicon wafers, boron doped, were used. Doping level was around $3 \cdot 10^{15}$ cm⁻³ (5 Ωcm). First, the front surface of the wafers was implanted with helium or hydrogen ions at a dose of $3 \cdot 10^{16}$ cm⁻² and an energy of 250 keV. Nanocavities were formed by annealing at 750°C for 1 hour in argon flow. They were located at a projected range (Rp) of 1.15 μm and 2.5 μm for He and H ion implantation, respectively. Then the samples were voluntarily contaminated by sputtering of a gold layer on the back surface and subsequent annealing at 750°C for 1 hour in argon flow.

For samples A, the formation of cavities and the gold in-diffusion were achieved in the same annealing run. For samples B, first the cavities were formed by annealing at 750°C for 1 hour, then gold was deposited and in-diffused at 750°C for 1 hour.

Substitutional gold concentration [Au_s] profiles were investigated by deep level transient spectroscopy (DLTS) applied to metal-insulator-semiconductor (MIS) diodes. The diodes were made by deposition of a 0.25 μm thick aluminium layer while the ohmic contact was obtained with InGa paste. In order to plot a depth profile of substitutional gold, the samples went through a series of etching steps with a CP4 solution from the front and the back surfaces. After each etching step, the diodes were made again on the new etched surface. Gold concentration profiles were also measured by secondary ion mass spectroscopy (SIMS) with a CAMECA IMS 4f apparatus.

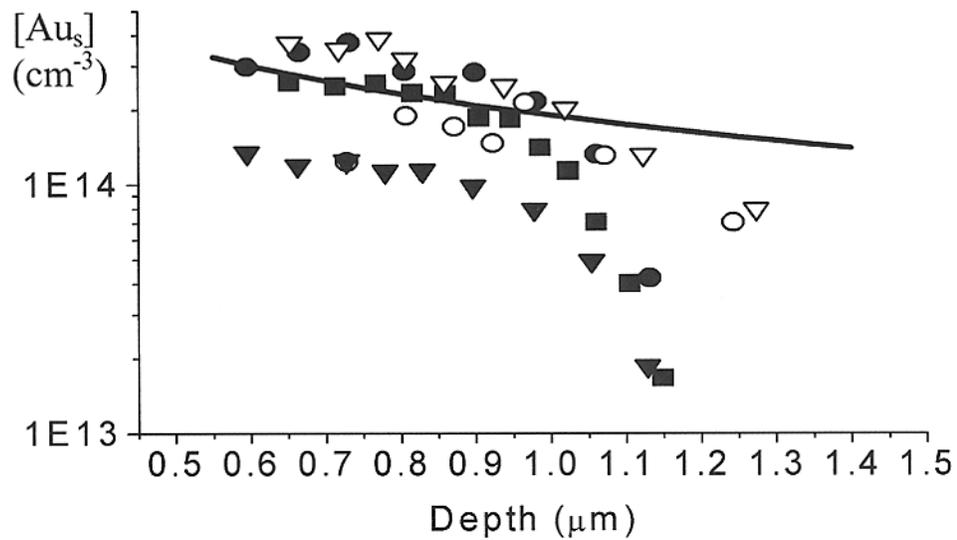


Fig. 1: Substitutional gold atoms profile between the front surface and the cavity band in hydrogen ion implanted samples (full dots samples A; empty dots: samples B). Computed gold profile is given by solid line

Results and discussion

The expected theoretical profile in contaminated defect free samples (not implanted) calculated from the kick-out mechanism [8,9] indicates that gold concentration should increase near the front surface. On the contrary, the measured substitutional gold concentration $[Au_s]$ decreases strongly near the cavity region located at $2.5 \mu\text{m}$ below the implanted surface. It should be noticed that this measured decrease is the same for samples A and B.

The depth distributions of $[Au_s]$ in helium and hydrogen implanted samples were found to be similar. Thus, the cavities formed in the implanted zone cause the decrease of $[Au_s]$ even in the presence of a constant gold source (the gold layer remains on the backside surface during the annealing).

It is possible to evaluate by DLTS the gold concentration between the implanted surface and the cavity region. As shown in Fig. 1, near the front surface, $[Au_s]$ is close to the computed values whereas in the depth, it decays faster than it is predicted by the kick-out mechanism. In this region, a small difference is observed between samples A and B: for samples A, the gold profile decay seems to be faster.

In helium implanted samples, substitutional gold is not detected between the surface and the cavity band even near the surface. One reason could be the smaller value of R_p and thus the stronger effect of the cavity band. Another reason could be a higher trapping of gold in this region due to a higher density of implantation induced defects in the case of He^{++} implantation.

SIMS profiles of He^{++} and H^+ implanted Cz samples are given in Fig. 2 and 3, respectively. An accumulation of gold atoms in the cavity band is revealed and no gold is detected beneath the cavities. Moreover, in He^{++} implanted Cz samples, a large concentration of gold is found between the implanted surface and the cavity band and in such region, $[Au]$ is higher in samples A than in samples B by one order of magnitude at least. This correlates well with the small $[Au_s]$ obtained by DLTS and indicates that gold atoms are probably trapped or precipitated.

Even though the SIMS oxygen background level was very high (around 10^{18} cm^{-3}), oxygen accumulations were detected in the Cz samples at a depth corresponding to the cavity layer. The preceding results show that the nanocavity band located beneath the implanted frontside surface of a silicon wafer traps gold atoms introduced from the backside surface. The gettering of metallic atoms was already observed in samples which were contaminated before helium or

hydrogen implantation [7,10], but our results suggest that wafers which were first implanted and then contaminated can also be protected from contamination.

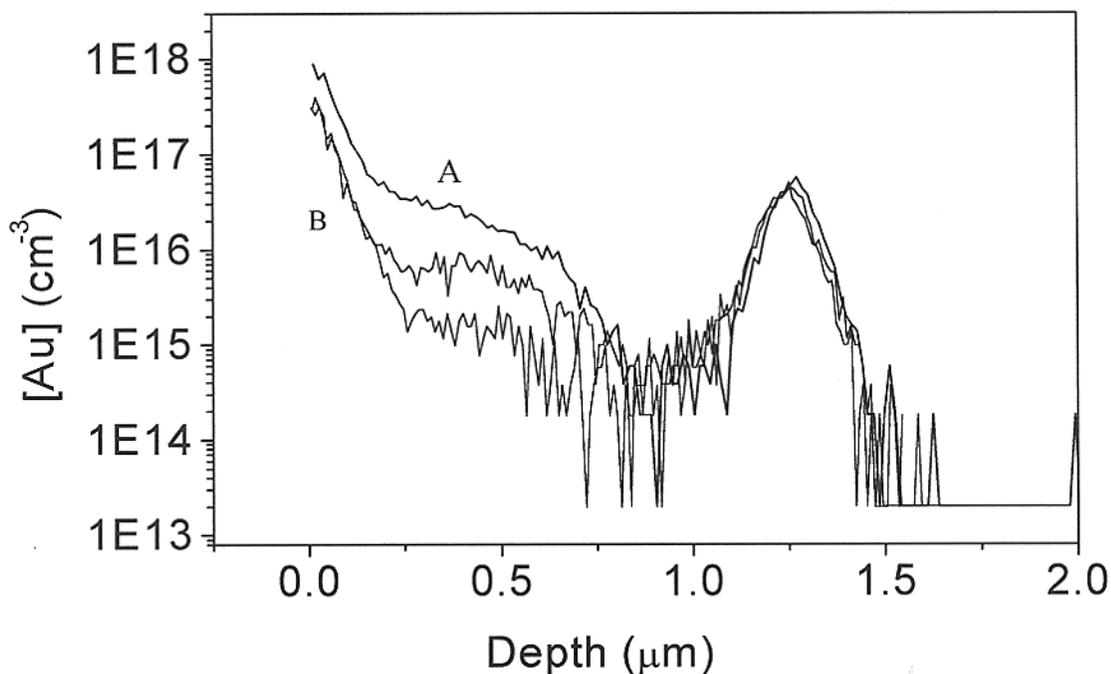


Fig. 2 : SIMS gold profile of He ion implanted samples A and B

There is no difference in the gold profiles beneath the cavity band, obtained for the samples A and B, this could be explained by the assumption that cavity formation occurs towards the end of the heating phase or at the beginning of the annealing.

As shown in [11], cavity formation is very fast and can occur even at very low temperatures like 350°C. Therefore, as the DLTS gold profiles have the same shape and [Au_s] reaches the calculated value 50 μm beneath the cavities in these samples, the cavity formation and the subsequent self-interstitial emission, which do not occur at the same moment in the samples A and B, do not seem to have a great influence on the kick-out mechanism and consequently on the [Au_s] concentration.

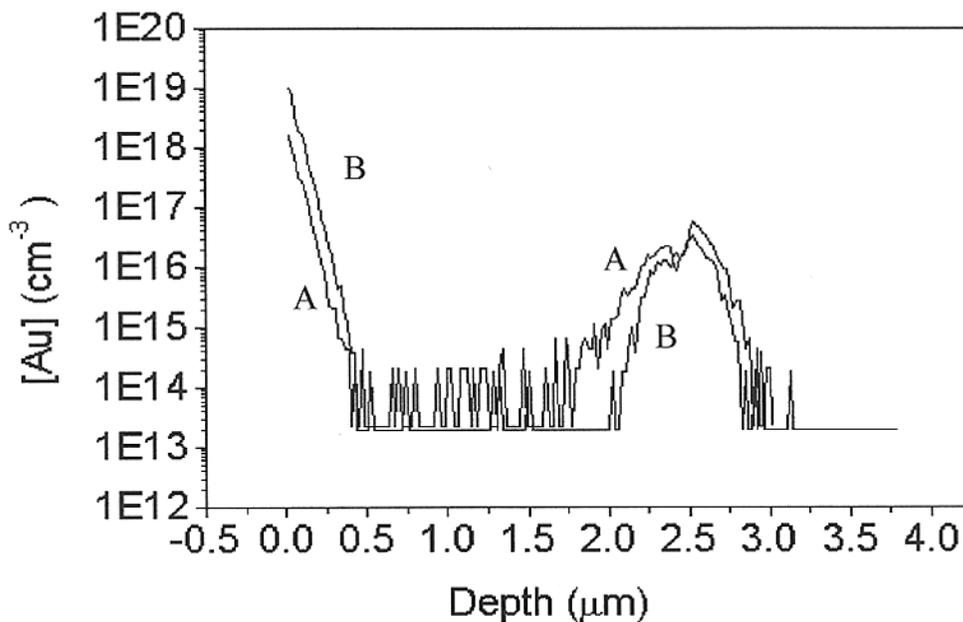


Fig.3 : SIMS gold profiles of hydrogen ion implanted samples A and B

However, as mentioned above, the cavity formation and the associated self-interstitial emission do not seem to have a great influence on the kick-out mechanism in samples A and B and we assume that there is probably another source of self-interstitials in excess which induce the $[Au_s]$ decrease. These self-interstitials may result from the gold precipitation on the cavity walls and/or on the dislocations formed near the Rp region. Indeed, Wong-Leung et al. [12], working under similar conditions (H^+ implantation at 96 keV at a dose of $3.10^{16} \text{ cm}^{-2}$ and annealing treatments at 650°C or 850°C for 1 h), have observed, using transmission electron microscopy, that some cavities were filled with Au-rich precipitates.

Moreover, the gold concentration profiles obtained by SIMS for He^{++} implanted samples A and B differ by one order of magnitude. In samples B, the cavities which have been formed before the gold in-diffusion behave like a diffusion barrier and reduce the gold content in the front region.

Conclusion

The nanocavity band created by high dose hydrogen or helium implantation behaves as a trapping region for gold atoms. Trapping efficiency is more marked in the case of He^{++} implantation because of the participation of residual implantation induced defects and the formation of oxygen-vacancy complexes in oxygen rich Cz samples. It is believed that gold trapping is related to a precipitation which in turn injects self-interstitials in the bulk. As a consequence, $[Au_s]$ decreases near the cavity band even though there is a constant source of gold atoms. Moreover, such bands of nanocavities behave as diffusion barriers for gold atoms.

As conventional ion implantation is long and expensive, it may be replaced for photovoltaic applications by plasma immersion ion implantation which is more suitable for large solar cells because of high dose rate and short implantation time [14, 15].

Aknowledgements

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COUNTERDOPING OF P -TYPE SILICON BY HYDROGEN ION IMPLANTATION

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Abstract

Hydrogen ion implantations at an energy of 250 keV and a dose of $3 \cdot 10^{16} \text{ cm}^{-2}$ were applied to float zone (FZ), Czochralski (Cz) grown silicon wafers and to multicrystalline (mc-Si) samples. It was found that after annealing at $350 < T < 550^\circ\text{C}$ for 1h a n-p junction is formed and a photovoltaic behaviour is observed. Spectral responses show that the photocurrent in the near infrared part of the spectrum is comparable to that of standard silicon solar cells. The depth of the junction is about $2\mu\text{m}$ and C-V measurements show that the junction is graduated. Hydrogen plasma immersion leads to similar results. The conversion of p-type to n-type silicon is explained by the formation of shallow donor levels associated to a high concentration of hydrogen.

Keywords : Silicon, ion implantation, hydrogen, n-p junction.

1. Introduction

In hydrogen ion implanted silicon it should be emphasized that hydrogen can exist in two distinct states : one of these is strongly bonded to the lattice and certainly includes those atoms which have passivated dangling bonds. The second more mobile type, could be weakly bonded interstitial hydrogen, accumulated within a few hundred angstroms below the free surface in concentrations higher than the solubility limit (up to 10^{20} cm^{-3}), as reported in [1]. Such interstitial hydrogen can react with impurities, or following the Wolkenstein's theory can also behave as a donor [2]. Such a behaviour was observed in proton implanted silicon at doses in the range 10^{16} to 10^{17} cm^{-2} and shallow donors (26 meV ionisation energy) were related to hydrogen [3;4]. Shallow donor formation was also proposed [5] to explain the formation of an n-p junction in multicrystalline silicon after hydrogen implantation by means of a Kaufman ion source.

It was demonstrated that implanted hydrogen can convert p-type silicon in n-type by the enhanced formation of thermal donors after interaction with interstitial oxygen atoms [6]. The conversion occurs when large doses of hydrogen ions ($> 10^{16} \text{ cm}^{-2}$) are implanted by conventional implanters or by plasma immersion while the temperature T of the wafers is maintained relatively low. Such conductivity type conversions may find some applications because they can reduce the thermal budget needed to make deep junctions for power devices. Solar cells can be made with multicrystalline silicon materials for which the electrical properties are degraded by annealings at temperatures higher than 600°C .

The transformation to n-type of a part of the wafer by hydrogenation could replace the phosphorus diffusion to make a n-p junction and in addition the introduction of hydrogen in the multicrystalline silicon could improve the material by the passivation of extended crystallographic defects and impurities. To do that ion implantations can be used.

It is well known that implantations of H^+ ions at doses higher than $2 \cdot 10^{16} \text{ cm}^{-2}$ lead to the formation of gas bubbles at the projected ion range R_p . These bubbles are transformed into nanovoids when hydrogen out-diffuses during an annealing at $T > 350^\circ\text{C}$. It may be possible to use such implantations to convert a near-surface region in n-type and to in-diffuse hydrogen in the bulk.

In the present paper we show that the H^+ implantation creates n-type regions and forms n-p junctions in silicon crystals.

2. Experimental

Monocrystalline silicon samples, float zone (FZ) and Czochralski (Cz) grown wafers were investigated. They were p-type boron doped to $4 \cdot 10^{13} \text{ cm}^{-3}$ (FZ), $3 \cdot 10^{15} \text{ cm}^{-3}$ (Cz). The samples were implanted with H^+ and He^{++} ions, at an energy of 250 keV and at a dose of $3 \cdot 10^{16} \text{ cm}^{-2}$. Hydrogen plasma immersion was also used.

Mesa structures ($5 \times 5 \text{ mm}^2$) were obtained by chemical etching of the implanted surface. An ohmic contact was made on the backside by the deposition of a 250 nm thick aluminium layer, followed by an annealing at 350°C for 30 min. On the front surface, the electrical contact is obtained by In-Ga paste.

Photocurrent spectral responses of the mesa structures were measured between 400 and 1100 nm. Minority carrier diffusion lengths in the p-type region were evaluated from the near infrared spectral response. A four point probe resistivity tool was used to evaluate the resistivity of the n-type region.

3. Results

Monocrystalline H^+ implanted samples exhibit a photovoltaic behaviour after the formation of the ohmic contact. Fig.1 and 2 give the photocurrent spectral response of the investigated FZ and Cz samples and that of a conventional cell made by phosphorus diffusion. The polarity of the photovoltage, as well as a hot probe test, indicate that the region beneath the implanted surface is converted to n-type. Notice that the photocurrent intensity in the near infrared part of the spectrum is close to that of a diffused n-p junction. The photocurrent between 400 and 500 nm is very low, suggesting that the junction depth is about $2 \text{ }\mu\text{m}$, that is approximately the projected range of the H^+ ions.

Such a conversion to n-type is not found in He^{++} implanted samples which experienced implantations under the same conditions.

In Fig. 1 and 2 the photocurrents of the implanted structures are lower than that of a conventional solar cell after the first annealing at 350°C to make the ohmic contact. However, subsequent annealings at 450, 500 and 550°C for 1h increase progressively the photocurrent, which becomes comparable to that obtained from a conventional finished solar cell under the same illumination conditions, in the near infra-red part of the spectrum.

C-V curves indicate that a step junction is obtained after the annealing at 350°C for 30 min which is needed to form the ohmic contact, and the neat donor density is about $2.5 \cdot 10^{17} \text{ cm}^{-3}$. During the subsequent annealing treatments the junctions become graduated.

After an annealing at 600°C for 1h, the photovoltaic behaviour disappears because the n-type region is converted back to its original p-type conductivity [4].

Similar results have been found in wafers implanted by plasma immersion, but the junction depth is larger..

To reduce the junction depth, the implanted surface of the samples annealed at 550°C is chemically etched with CP4 during two etching steps of 5 s. The spectral response was measured after each etching step. It is found that the photocurrent increases after each etching step for Cz samples but disappears after a new etching step of 5 s, which corresponds to the removing of about 2.5 to 3 μm. After the second etching step one sample experienced an additional short (2 s) etch. A high density of defects is revealed on the surface which are probably due to the cavities formed during the annealing steps.

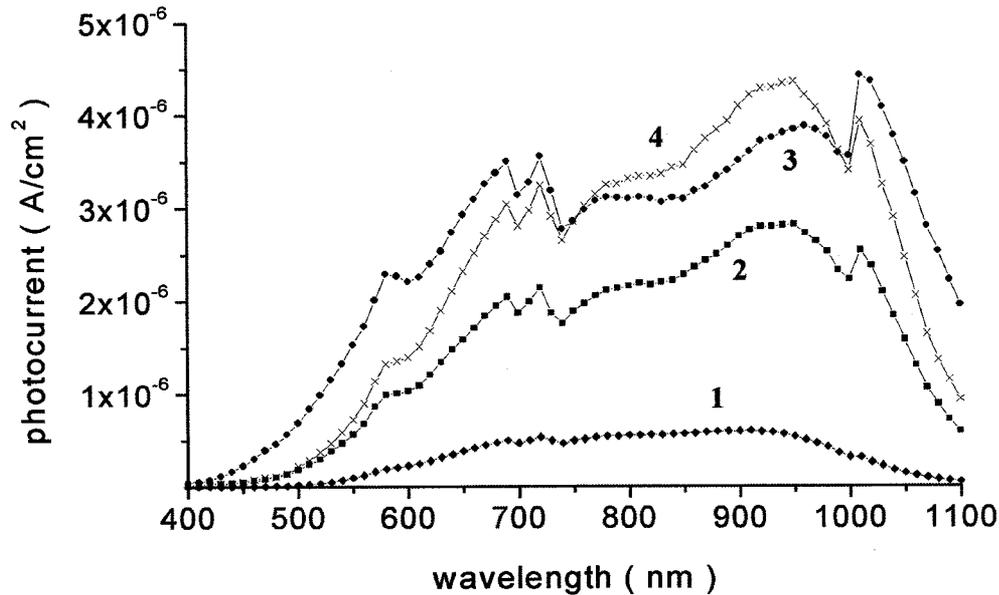


Fig 1. Photocurrent spectral responses of a FZ sample after various annealing steps : (1) as implanted ; (2) after annealing at 450°C for 1h ; (3) after annealing at 550°C for 1 h ; (4) phosphorus diffused FZ solar cell

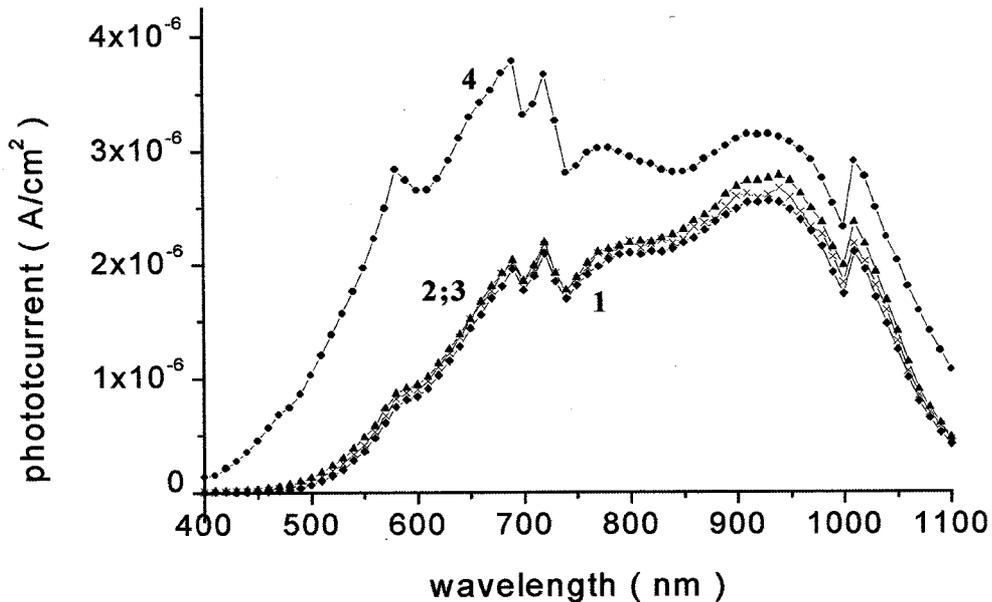


Fig 2. Photocurrent spectral responses of a Cz sample after various annealings steps: (1) as implanted; (2) after annealing at 450°C for 1h; (3) after 550°C for 1h; (4) phosphorus diffused Cz solar cell

The preceding results may be related to drastic changes of the region beneath the hydrogen implanted surface of the samples in which nanocavities are formed and a high concentration of hydrogen is present. The observed formation of a n-p junction is related to hydrogen as it does not appear in the samples implanted with helium ions under the same conditions. Thus the formation of an amorphous region due to a high concentration of crystalline defects induced by the implantations cannot explain the results, like the compensation of acceptors near the surface because the surface resistivity is relatively low ($1 \Omega\text{cm}$ in Cz wafers) and the conductivity is n-type.

The interaction of hydrogen with oxygen to form thermal donors could explain the junction formation in Cz samples, because in such samples the oxygen concentration is higher than $7 \cdot 10^{17} \text{cm}^{-3}$, but not in FZ samples. Moreover, as reported in [7], the formation of thermal donors enhanced by implanted hydrogen ions occurs during an annealing at 450°C . In our samples the n-type region appears after an annealing at 350°C and is reinforced after subsequent annealings in the range 350°C to 550°C .

Thus it is believed that the most likely explanation of the formation of a n-p junction is the formation of shallow donors beneath the implanted surface at a depth which corresponds to the projected range of hydrogen ions. Such a formation is related to the high dose of hydrogen ions and related to the formation of nanocavities in FZ like in Cz samples.

Conclusion

Hydrogen ion implantations at high doses in p-type crystalline silicon convert the near-surface region to n-type. Such a conversion is related to the high dose of hydrogen which induces the formation of shallow donors. After low temperature annealing steps an n-p junction is formed for which the photovoltaic properties are close to that of conventional solar cells made by phosphorus diffusion. These junctions may be suited to the preparation of cells with imperfect silicon wafers which are degraded by the annealing step associated to the phosphorus diffusion.

Aknowledgements

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Light Induced Degradation in Manufacturable Multi-crystalline Silicon Solar Cells

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Abstract

Traditional Czochralski grown Si solar cells are known to suffer from light induced degradation (LID) which adversely affects the minority carrier lifetime. Multi-crystalline Si has also been shown to show a similar degradation/recovery cycle after a phosphorus gettering step. In this paper, promising ribbon and cast multi-crystalline Si are examined for light induced degradation. High oxygen materials ($\geq 10^{18} \text{cm}^{-3}$) like dendritic web, Baysix Cz, and conventional Cz show similar degradation/recovery, HEM cast multi-crystalline with modest oxygen content ($2.5 \times 10^{17} \text{cm}^{-3}$) shows small LID, and EFG and string ribbon silicon with low oxygen content ($< 2.5 \times 10^{17} \text{cm}^{-3}$) show no LID. In addition light induced degradation is investigated at elevated temperatures. It is shown that bulk lifetime is degraded at 400°C under tungsten halogen lamp illumination in a belt furnace suggesting that at 400°C LID is greater than any annealing. At higher temperature belt processing under lamp ($>400^\circ\text{C}$) the net LID is partially reduced. On the other hand bulk lifetime is annealed in a conventional furnace at 400°C with no lamp illumination.

Introduction

Czochralski grown Silicon is known to suffer lifetime degradation and thus efficiency degradation under carrier injection. Light induced degradation (LID) was first studied by Fischer and Pschunder in 1973, after being recognized by Crabb in 1972 [1,2]. A great deal of attention has been directed at investigating ways to suppress or avoid LID especially since 1998 when Abe and Saitoh organized an international joint research focused on determining the cause of LID and how to avoid it in solar cell processing [3]. The trap formation has been shown to result from a boron-oxygen complex [4-7]. Various heat treatments have been implemented to improve the stabilized degraded lifetime of Cz wafers that suffer from LID [8]. Hydrogenation has also been shown to improve the stabilized degraded lifetime [8]. The effects of efficiency degradation can be reduced by wafer thinning, which improves the effective diffusion length ratio to device thickness to improve collection probability [9,10]. There is still much to be discovered about the trap responsible for LID. This paper analyzes the process conditions under which a sample will exhibit the degradation/recovery cycle in an industrial process. Different promising multi-crystalline Si materials with similar resistivity but varying oxygen content are analyzed for degradation along with the conditions under which degradation occurs for traditional high O_i content Cz Si.

Experimental

All materials listed in Table 1 received a light P diffusion of $\sim 150 \Omega/\text{sq.}$ at 925°C and a 20nm oxide for passivation using the DOSS technique [11]. Then a 80nm SiN_x layer was deposited by PECVD at 300°C on top of the 20nm oxide to obtain a stack passivation.

This provided a stable surface passivation for ease of measurement and was monitored by a 2.3 Ωcm FZ wafer. Effective lifetime measurements were then made following light exposure and forming gas annealing at 400°C.

Table 1.

Material	Thickness	Resistivity	Oxygen (O_i)
Float Zone SEH	300 μm	2.3 Ωcm	undetected
Cz Baysix	400 μm	0.9 Ωcm	10^{17} to 2×10^{18}
HEM	250 μm	1.5 Ωcm	$< 2.5 \times 10^{17}$
Boron Web	102 μm	3.0 Ωcm	$> 1.0 \times 10^{18}$
Magnetic Boron Web	93 μm	9.3 Ωcm
Gallium Web	97 μm	22.0 Ωcm
Evergreen Ribbon	350 μm	3.0 Ωcm	$< 5.0 \times 10^{16}$
EFG	350 μm	3.0 Ωcm	$< 4.0 \times 10^{17}$

In addition, some additional Baysix Cz wafers were used to test degradation as a function of belt annealing (lamp illuminated heating) and furnace annealing (dark heating). The furnace anneal uses heating coils to achieve temperature allowing for samples to be heated essentially in the “dark”. The belt furnace used in this study uses a bank of tungsten halogen lamps above and below samples to achieve the desired temperature. In all the experiments a very high lifetime ($> 1\text{ms}$) FZ (1.0 Ωcm) wafer was used for monitoring the change in surface passivation, if any, due to light exposure and/or annealing.

Results and Discussion

a.) Light Induced degradation in promising Multi-crystalline Si materials

After the light phosphorus diffusion samples were exposed to light for degradation and subsequently annealed in the tube furnace at 400°C for 15 minutes in Forming Gas for lifetime recovery. Figures 1-3 show the resulting effective lifetimes at $1 \times 10^{15} \text{cm}^{-3}$

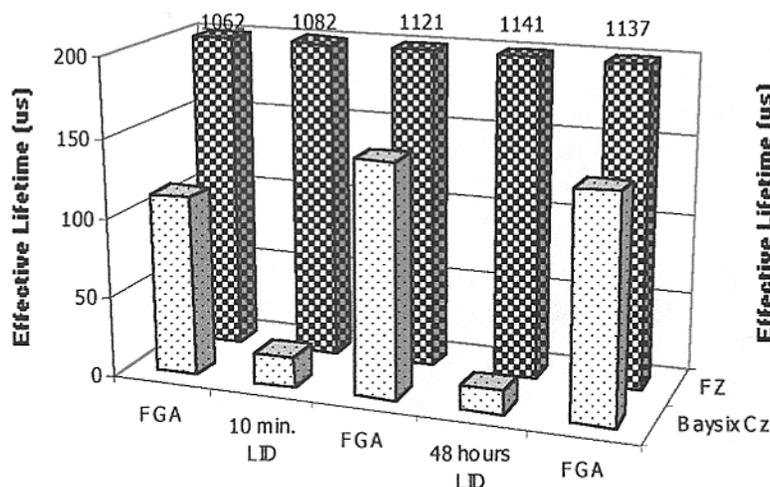


Figure 1. 2.3 Ωcm FZ and 0.9 Ωcm Baysix Cz under illumination and a 400°C forming gas anneal.

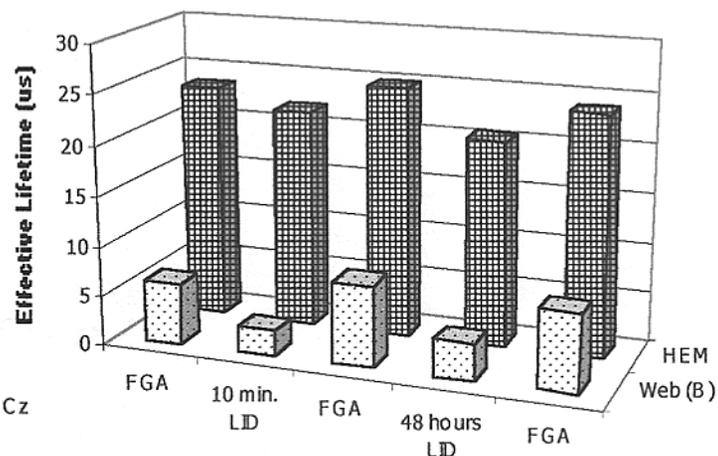


Figure 2. 1.5 Ωcm HEM and 3 Ωcm B Web under illumination and a 400°C forming gas anneal.

injection level for all the materials listed in Table 1. Effective lifetime

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s} \quad (1)$$

which includes bulk lifetime (τ_b) and surface lifetime (τ_s). Figure 1 shows the effective lifetime for FZ and Cz Si. FZ maintains a stable effective lifetime of 1.2 ms and the Cz exhibits the traditional degradation recovery cycle. Figure 2 shows the degradation/recovery cycle for B doped dendritic web and HEM multi-crystalline Si. Figure 3 shows the low oxygen multi-crystalline Si ribbon materials EFG and String Ribbon that show no degradation. This information is consistent with the oxygen and boron data in Table 1, i.e., both oxygen and boron need to be present in sufficient amounts in order for degradation to occur. Fig. 2 demonstrates that even samples with lifetimes under $8\mu s$ can exhibit degradation. Figure 4 shows the normalized degradation for each material as function of the O_i content. The resistivity of each material is 1-3 Ωcm and is not considered in the figure. However, both single and multi-crystalline Si materials show an increase in normalized degradation with an increased oxygen concentration.

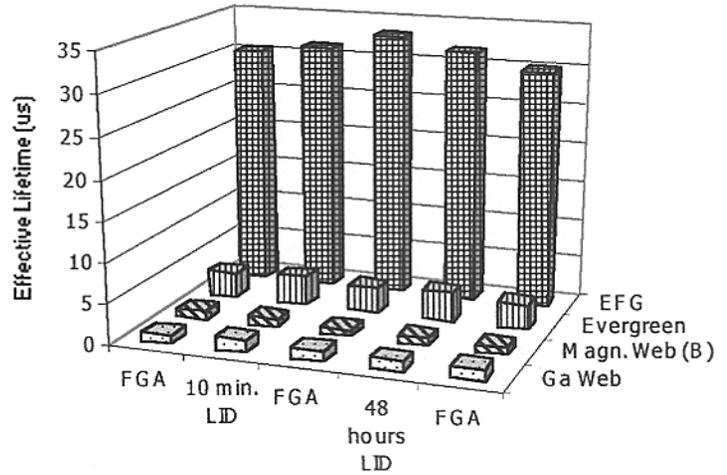


Figure 3. 3 Ωcm EFG, 3 Ωcm String Ribbon, 9.3 Ωcm magn.- B Web and 22 Ωcm Ga Web under illumination and a 400°C forming gas anneal.

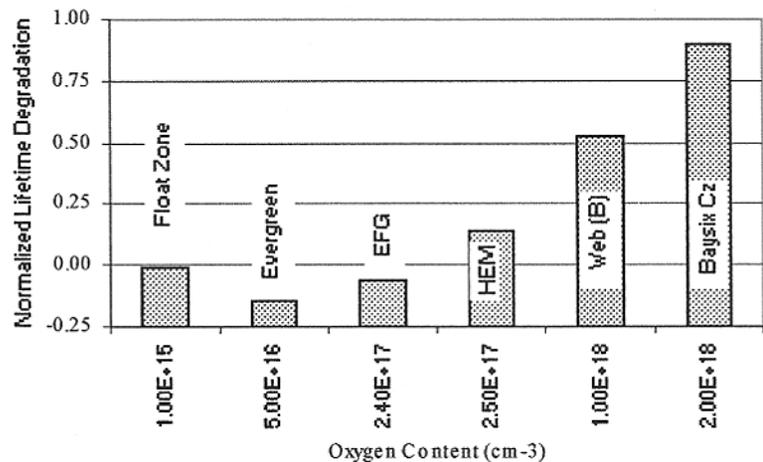


Figure 4. Normalized effective lifetime of manufacturable solar grade materials and their oxygen content

b.) Illuminated and Dark Annealing of LID

A study was conducted to compare illuminated annealing of LID in a belt furnace and dark annealing in a conventional tube furnace. In this study we examine degradation at elevated temperatures. It is commonly known that degradation occurs in the presence of light and that the lifetime is recovered by an anneal at 200°C and above. In an effort to further understand the trap responsible for LID, we performed a study comparing what happens to LID when light is used to heat the sample versus dark annealing. In the lamp heated belt furnace there may be a competition between degradation and recovery. In the conventional tube furnace we only have the recovery agent present. A high quality SiN_x / SiO_2 stack passivation was used to eliminate surface effects. This is supported by Figure

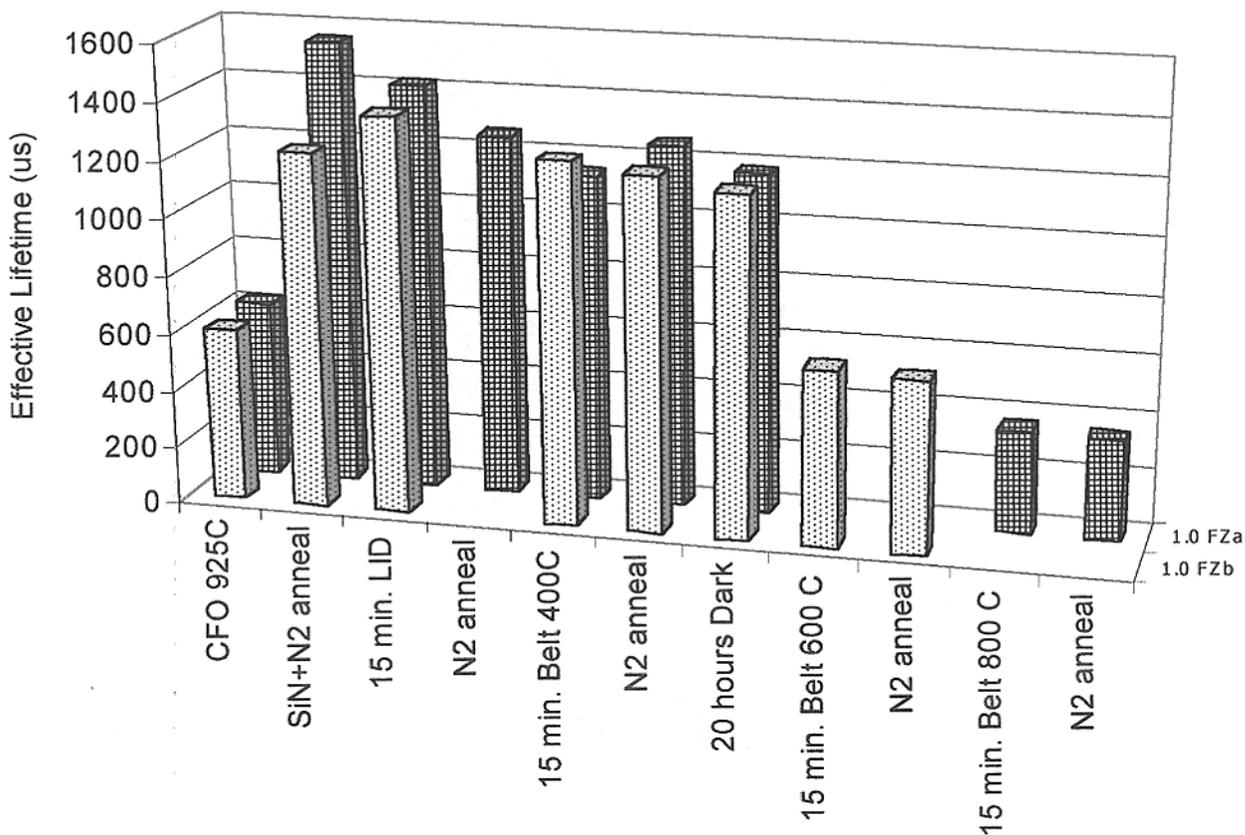


Figure 5. 1.0 Ωcm SEH FZ with a SiN_x / SiO₂ stack passivation. External stimulus applied is on the x-axis and measured effective lifetime is on the z-axis and the sample is on the y-axis. Bars on graph are in sequential order and therefore some x-axis labels do not apply for each sample.

5 which shows that effective lifetime for a 1.0 Ωcm SEH FZ wafer remains very high under various illumination and annealing conditions. The sample lifetime was measured immediately after a furnace oxide growth at 925°C and then a 80nm PECVD SiN_x layer deposited at 300°C. Following Nitride deposition the sample was annealed in N₂ at 400°C in a conventional furnace tube and re-measured. The samples were then degraded and annealed sequentially as shown Fig. 5. Surface passivation remains stable until the Belt furnace was raised to 600°C, the effective lifetime decreased to half the initial value and remained stable after additional N₂ anneal at 400°C. The surface passivation for FZ-b remained quite stable until the Belt furnace was raised to 800°C. The effective lifetime was then decreased to one-third the initial lifetime to 360μs and remained stable after additional N₂ anneal at 400°C. Thus surface passivation due SiN_x/SiO₂ stack remains sufficiently high to analyze PV grade materials by effective lifetime.

Figure 6a shows the effective lifetime of Baysix Cz samples subjected to the degradation/recovery sequence and the resulting effective lifetimes. The Cz samples show the expected cycle for the dark anneal at 400°C and 15 minutes or longer light soaking conditions. Results differ in Figure 6b when the LID Cz Si samples are subjected to illuminated heating/annealing. At 400°C under the tungsten halogen lamps in the belt furnace the samples show a similar degradation to 15 minutes light soaking in open air by a 300 W halogen lamp at 6 inch spacing. Cz samples that were degraded to 35μs showed no recovery in the illuminated belt furnace at 400°C. The effective lifetime is completely recovered in all Cz samples subjected to a 400°C belt anneal after a

subsequent N₂ anneal at 400°C in the dark. Figure 6b shows that there is LID during

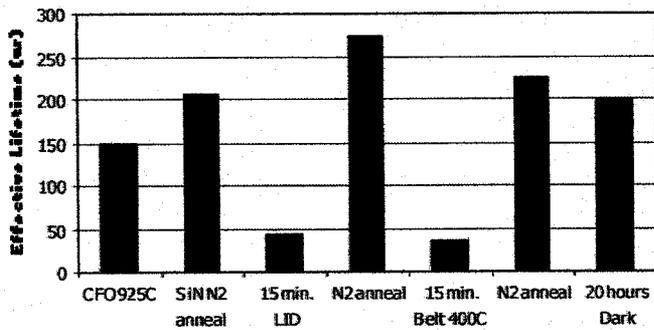


Figure 6a. 0.9 Ωcm Baysix Cz with a SiN_x / SiO₂ stack passivation. External stimulus applied is on the x-axis and measured effective lifetime is on the y-axis.

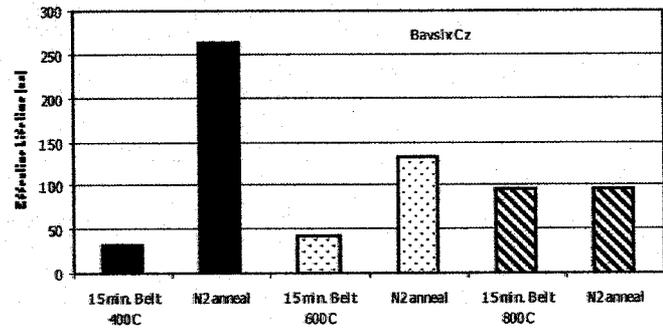


Figure 6b. 0.9 Ωcm Baysix Cz with a SiN_x / SiO₂ stack passivation. External stimulus applied is on the x-axis after N₂ anneal and measured effective lifetime is on the y-axis.

processing in the lamp heated belt furnace and the net LID is lower for higher temperature processing. Effective lifetime after 400°C heat treatment in the belt is about 1/3 the effective of lifetime of the 800°C anneal. After N₂ anneal the sample processed at 400°C fully recovers, while the effective lifetimes in 600°C and 800°C processed samples do not fully recover, possibly due to the decrease in surface passivation shown by the FZ wafers. However the 600°C sample recovers 90μs of effective lifetime due to the subsequent dark N₂ anneal, suggesting that LID remained after the 600°C process. On the other hand the 800°C showed no lifetime recovery after the subsequent dark anneal, suggesting that degradation and recovery is masked by the surface passivation. Partial recovery in these samples may be due to cooling in the dark after the sample exits the illuminated zone.

Conclusion

Light induced degradation in promising solar grade materials has been shown to occur in samples that have sufficient amount of boron and oxygen present for degradation. Both in single and multi-crystalline Si LID is proportional to the oxygen content. Cz and web Si show higher LID, HEM multi-crystalline Si shows some LID, and low oxygen Si ribbons show no LID. These results are consistent with the fact that LID is controlled by the oxygen and boron concentration and not by crystal defects and structure. In addition, light induced lifetime degradation is shown to occur at elevated temperatures during the processing in a lamp heated belt furnace. Degree of degradation is a function of the processing temperature.

Acknowledgements

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Lifetime Enhancement During Processing of Porous Silicon Cells

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ABSTRACT

Porous silicon (PS) induced lifetime enhancement was investigated in dendritic web and string ribbon silicon. As-grown lifetime in web was $<1 \mu\text{s}$, which improved by a factor of 3.27 due to $860^\circ\text{C}/2 \text{ min}$ heat treatment. The same heat treatment after PS formation increased the lifetime by a factor of 8.33, indicating that PS alone is quite effective in raising the lifetime of web. Al gettering by itself raised the lifetime of as-grown web by a factor of 15, but the simultaneous annealing heat treatment increased the lifetime by a factor of 42, indicating a positive synergistic interaction between PS and Al. Finally, simultaneous phosphorus and Al diffusion, after PS formation, raised the as-grown web lifetime by a factor of 58. String ribbon Si, which has a low oxygen content and responds more favorably to hydrogenation, did not show much improvement due to PS+Al. Instead it showed greater response to SiN+Al treatment, suggesting that Al+PS induced lifetime enhancement is due to gettering and not hydrogenation. Screen-printed PS coated $100 \mu\text{m}$ web cells were formed by a single step firing and back diffusion with efficiency of 12 %. Cell analysis showed that process optimization can raise that efficiency by 2-3 % absolute.

1 INTRODUCTION

Porous silicon has certain properties that make it very attractive for solar cell applications. Porous silicon has been proven to be a good antireflection (AR) coating for Si solar cells [1]. Moreover, due to the porous nature of the surface, it can be used for surface texturing of single or multicrystalline Si materials [2]. Porous silicon can also act as a surface passivating layer, since it has a larger bandgap than silicon ($>1.40 \text{ eV}$).

It has also been shown that porous silicon could be used as an extrinsic gettering method on metallurgical-grade silicon [3]. Most of the work reported on porous silicon has been through the use of electrochemical etching to form the porous silicon layer that is not as suitable for industrial applications. In this paper, porous silicon is formed using a cheap and simple wet chemical etching process that takes only few seconds. Gettering and hydrogenation ability of PS is determined through a systematic study of lifetime enhancement in dendritic web silicon, which has a high oxygen content, and low-oxygen string ribbon which responds strongly to hydrogenation. In addition, solar cells are fabricated with SiN and PS AR coating.

2 EXPERIMENTAL

A simple and low-cost chemical etching was used to form the porous silicon layers on both surfaces of the material. The PS layer was formed in a few seconds (~ 10 sec), using $\text{H}_2\text{O}:\text{HNO}_3:\text{HF}$ solution in the ratio 10:9:3. The Si samples were cleaned using an RCA sequence before the initial as-grown lifetime measurement by the quasi-state photoconductance (QSSPC) technique [4]. After the desired heat treatment, all the layers (aluminum, porous silicon, SiN or any diffusion layer) were etched from the sample and the bulk lifetime was measured again using the photoconductance technique. Silicon nitride was deposited using PECVD at 300°C , with a refractive index of 1.98 and a thickness of 850 \AA , which densifies to 780 \AA and 2.03 index of refraction after all the firing steps. Aluminum back-surface field (BSF) was formed by screen-printing Al on the back and firing it in the belt furnace at 860°C for 2 minutes. The phosphorus was diffused using a phosphorus solid-source placed on top of the Si sample as it travels through the belt furnace. For the lifetime studies, heat treatments involving phosphorus diffusion were performed at 860°C for 6 minutes, while all other heat treatments were performed at 860°C for 2 minutes. However, for cell fabrication, simultaneous diffusion of screen-printed Al on the back and solid source phosphorus on the front was achieved in the belt furnace at 880°C for 20 minutes in order to obtain $\sim 45 \text{ } \Omega/\text{sq}$. emitter.

3 INDIVIDUAL AND COMBINED EFFECTS OF PHOSPHORUS, ALUMINUM AND POROUS SILICON TREATMENTS

Figure 1 shows the effect of various heat treatments, individually and in combination. Normalized lifetime represents the change in lifetime divided by the starting lifetime ($\Delta\tau/\tau_s$). Fig. 1 shows that PS, Al, PS+P, P+Al treatments improve the sub-microsecond lifetime of a $1.3 \text{ } \Omega\text{-cm}$ web by a factor in the range of 3 to 15. However, the PS+Al combination increased the bulk lifetime by a factor of ~ 42 , which is greater than the sum of individual effects of PS and Al. This indicates a positive synergistic interaction between Al and PS. Finally, simultaneous diffusion of SP Al on the back and solid-source P on the front of the PS layer at 860°C for 6 min improved the bulk lifetime by a factor of 58, resulting in an absolute lifetime of 17.9 on $1.3 \text{ } \Omega\text{-cm}$ p-type web Si. The same treatment improved the bulk lifetime of a $5 \text{ } \Omega\text{-cm}$ p-type web Si by a factor of 59, resulting in a final lifetime of $45 \text{ } \mu\text{s}$.

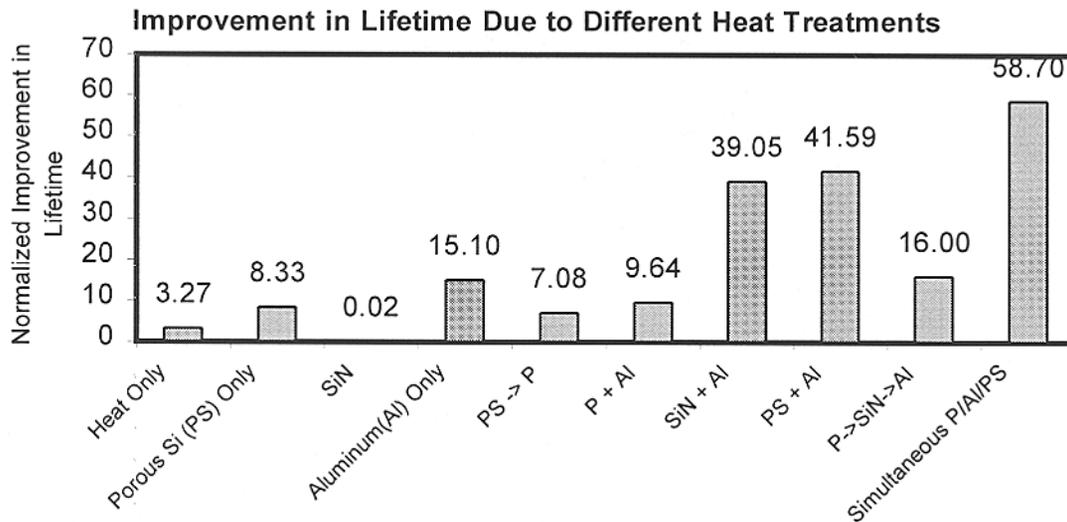


Figure 1. Normalized improvement in lifetime due to individual and combined effects of PS, Al, and P.

In the literature [5], the synergistic effect of aluminum and porous silicon has been attributed to enhanced defect passivation due to hydrogen diffusion from the porous Si surface. Hydrogen diffusion can be enhanced due to vacancies generated by Al alloying at the back. It is important to note that unlike other ribbon materials, dendritic web has a high oxygen content, which is known to hinder hydrogenation. This is supported by the fact that SiN induced hydrogenation has little effect on web bulk lifetime. On the other hand, SiN+Al heat treatment is found to be very effective for lifetime enhancement in low-oxygen string ribbon silicon, which is known to improve significantly with hydrogenation [6]. Notice that PS+Al treatment has a much less effect on lifetime of string ribbon relative to SiN+Al treatment. This suggests that PS+Al does not provide as good a source of hydrogenation as the SiN+Al treatment. Hence, the significant lifetime enhancement in high-oxygen dendritic web silicon due to Al+PS treatment is attributed to gettering of impurities rather than defect passivation due to hydrogen. More work is needed to prove this point.

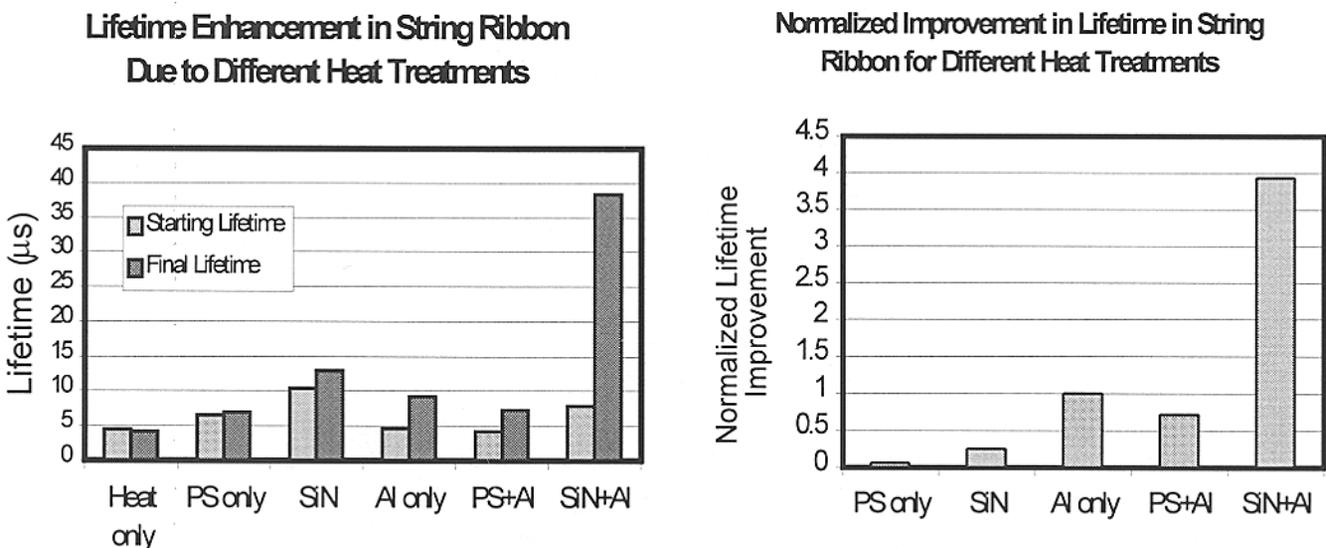


Figure 2. Porous Si and Al heat treatments for string ribbon materials.

4 FABRICATION AND ANALYSIS OF PS CELLS ON WEB SILICON

Manufacturable screen-printed n^+p-p^+ solar cells were fabricated with PS or SiN AR coating on 0.6 Ω -cm. SP Al BSF and solid-source phosphorus emitter were formed simultaneously, after the PS formation, to maximize the bulk lifetime. Notice that, unlike most prior investigations, the PS layer was formed before and not after the diffusion. Finally, the screen-printed Ag contacts were fired through the PS layer. Conventional SiN AR coated cells were also fabricated for comparison. As shown in Table I, PS cells gave 12 % efficiency while the SiN coated cells were 13 %, primarily due to the difference in J_{sc} . IQE and reflectance analysis, Fig. 3, showed that the IQE of both cells were quite similar and the difference in J_{sc} can be totally accounted for by the higher reflectance of PS cells. This is because PS reflectance properties changed during the diffusion process. We need to tailor the starting PS layer reflectance so that after diffusion and contact firing, which can change the porosity and thickness of the PS layer, we get 10 % reflectance instead of 18 % obtained in this experiment. In addition, diffusion for the PS cell was done at 880°C for 20 minutes to obtain the right emitter sheet resistance, while the lifetime enhancement studies were done at 860°C for 6 minutes. Further process optimization is needed to obtain appropriate reflectance, sheet resistance and lifetime in the finished PS devices.

Table I. Comparison of SiN and PS cell performance.

Cell ID	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF	Eff(%)	R_s (Ω -cm ²)	R_{sh} (Ω -cm ²)
P0.6 PS	602	26.32	0.757	12	0.98	3111
P0.6 SiN	606	28.41	0.753	13	0.9	3665

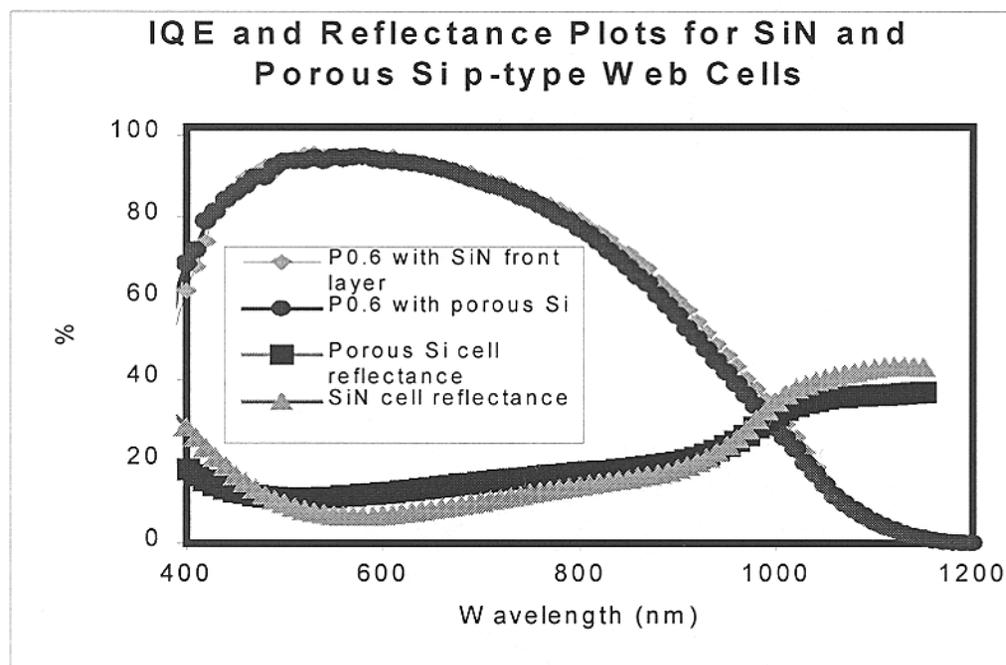


Figure 3. Internal quantum efficiency plots of a PS and a SiN coated cell.

5 CONCLUSIONS

This study shows that PS is capable of enhancing bulk lifetime of mc-Si materials and this improvement is amplified by the presence of Al on the back during the heat treatment. Porous silicon induced enhancement is material specific. It appears that materials like web, which respond strongly to gettering, show greater improvement due to PS+Al treatment. Materials like string ribbon, which respond positively to hydrogenation, showed better response due to the Al+SiN treatment than the Al+PS treatment. This suggests that PS induced lifetime enhancement is due to gettering, resulting from the stress and damage induced impurity sink in the PS layer. Screen-printed PS cells were fabricated by simultaneous front and back diffusion, after the PS formation. Initial results on PS cells are encouraging. Further, process optimization may close the gap between SiN and PS cells.

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Temperature-Dependent Cross-Sectional EBIC Study of Hydrogen Passivation of Defects in mc-Silicon

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Introduction

It is well established that hydrogenation reduces the density of deep level point-like defects [1] as well as the recombination activity of the extended defects at room temperature in mc-Si [2]. From the application point of view it is important to know the depth profile of the passivation of defect recombination activity down to a depth of about the diffusion length of minority carriers in defect-free silicon which is typically in the order of several hundreds of microns. The measurement of the Electron-Beam-Induced Current (EBIC) offers excellent ways for qualitative and quantitative characterization of the recombination activity of individual defects. Limitations of conventional “plan-view” EBIC regarding the information depth arise from the penetration depth of the electron beam, which is about 10 μm at 40 keV in silicon. However, for depth profiling of hydrogen passivation the measurement of the EBIC along a cross-section of the sample can overcome this limitation [3 - 5].

According to the previous experimental data [6, 7] and to the recent theoretical results [8, 9] EBIC measurements at room temperature allow to detect defects with a high local density of deep electronic states (e.g., at strongly contaminated dislocations) exhibiting rather strong recombination activity. Defects of low activity can only be detected at sufficiently low temperature [6, 7]. Accordingly, EBIC measurements in a wide range of temperature are required to obtain sufficient dynamic range to study samples with defects of various recombination activities. Moreover, it was demonstrated [6,8-9] that the shape of temperature dependence of the EBIC defect contrast $c(T)$ between 80 and 300 K depends on the degree of contamination and reveals information about defect levels involved in the recombination process.

The recombination activity of an extended defect, γ , is defined as the difference of the recombination rates of the excess carriers in close vicinity of the defect and far away from it [10]. The local density of the excess minority carriers in the vicinity of the defect, which is maintained by the carrier diffusion, decreases when γ increases. As the result, the EBIC contrast, c , of any extended defect is generally a sub-linear function on its own recombination activity, or “recombination strength”. For one-dimensional defects like dislocations the diffusion limitations are small and a linear approximation ($c \sim \gamma$) can be used in most practical cases. For a plane defect like grain boundary (GB) the diffusion limitation is sufficient beginning from rather small contrast values [11].

The GB recombination activity is characterized by the recombination velocity at the GB plane, v_s , or the reduced “surface” recombination velocity $s = v_s/D$, that is proportional to the dislocation density in the GB plane [12]. Our analysis of the theoretically calculated $c(s)$ dependence for an accelerating voltage of 30 kV and $L_D = 10 - 50 \mu\text{m}$ [11] showed that proportionality between c and s holds only for $c < 0.1 - 0.2$. For larger c values, the $c(s)$ dependence becomes close to logarithmic and saturates for $s > 10 \mu\text{m}^{-1}$. The latter value is the upper limit for the transformation of experimental c into s values.

In this paper we will present and discuss the results of our study of the depth profiling of the recombination activity of different extended defects in mc-Si treated in the remote hydrogen plasma by means of temperature-dependent EBIC measurements.

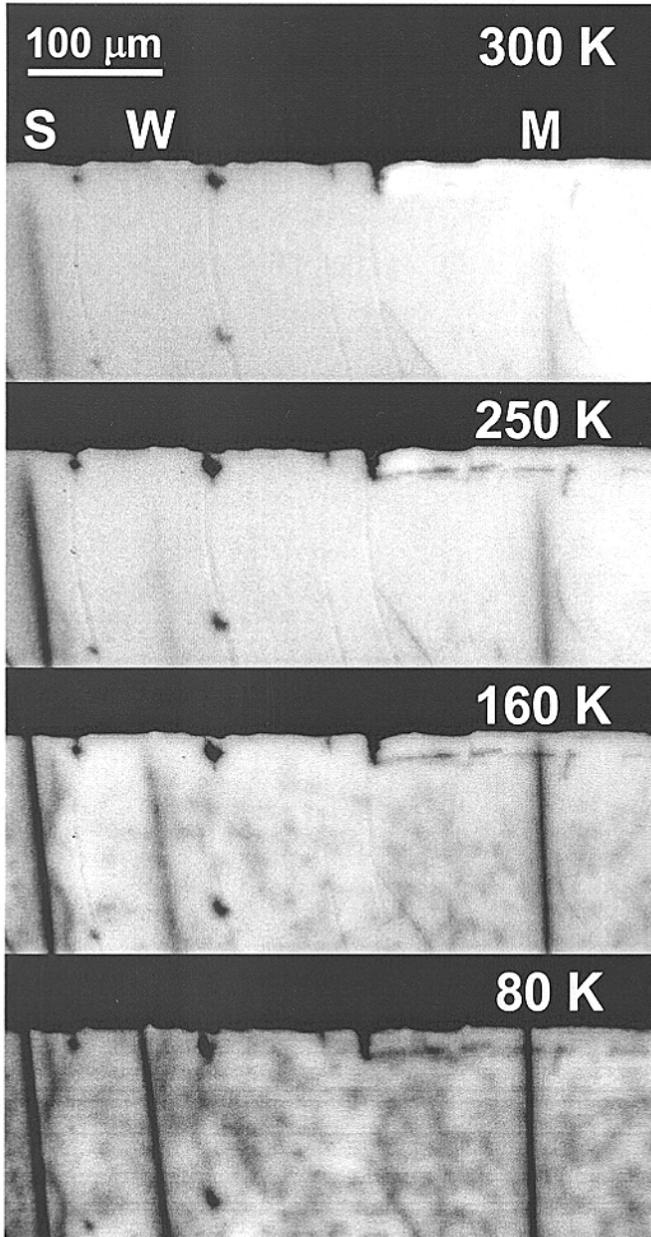


Fig. 1
EBIC micrographs (30 keV, 50 pA) taken at $T = 300$ K, 250 K, 160 K and 80 K at the cleaved surface of a mc-Si wafer. The figure shows the upper half of the wafer cross section after remote hydrogen plasma treatment from the top. Three dark lines are visible that represent grain boundaries of different recombination activity (denoted S, M, and W). Intragrain dislocations can be seen as well. The contrast of the grain boundary near the wafer surface is clearly reduced which is best visible at intermediate temperatures.

The apparent recombination activity at GB-M, GB-W and at intragrain dislocations increases with decreasing temperature in the whole temperature range whereas it exhibits saturation below 200K at GB-S. GB-W and intragrain defects could not be detected by EBIC at room temperature, but became visible in the images at $T < 250$ K.

Experimental

As-grown p-type mc-Si (Silso[®], Wacker) grown by block casting was used in all experiments. After RCA cleaning, the samples were hydrogenated in an electron cyclotron resonance (ECR) plasma reactor for one hour at the temperature of 310 °C. After having removed about 5 microns of the sample surface by chemical etching, Schottky and ohmic contacts were formed by subsequent titanium and aluminum deposition on the cleaved surface and by rubbing In/Ga eutectic on the wafer's back surface, respectively. All measurements were performed at the cleaved surface using an accelerating voltage of 30 keV and a beam current of 50 pA.

Results

Grain boundaries. Fig. 1 displays a representative subset of a temperature series of EBIC micrographs taken at a cross-section of a wafer treated in hydrogen plasma. The images showing the upper half (front) of the same cleaved surface region were taken at a temperature of 300 K, 250 K, 160 K, and 80 K. The three vertical dark lines indicate enhanced carrier recombination at GB-S, GB-M, and GB-W according to their strong, medium and weak activity (contrast) at room temperature, respectively.

Both the grain boundary and the intragrain defect activity are significantly reduced near the surface indicating the passivation of the defects by hydrogen. The temperature range where the passivation effect is best visible depends on the initial activity of the defect. As it was found from the EBIC images measured in steps of 10 K passivation is best visible in the range of 200 - 300 K for GB-S, $T = 140 - 300$ K for GB-M, and $T = 100 - 250$ K for GB-W and for intragrain dislocations. One can note that the lower temperature limit for the detection of the passivation effect increases with increasing initial defect activity. On the other hand, the apparent passivation depth decreases with decreasing temperature for all of the defects.

The temperature dependence of the apparent passivation depth indicates that the dependence of

the apparent recombination activity of the defects on the density of recombination centers is non-linear and becomes weaker with decreasing temperature.

Our experimental contrast data were transformed into the reduced "surface" recombination velocities at the GBs by using the calculated c vs. s plot in [11], assuming a minority carrier diffusion length of $50 \mu\text{m}$. The temperature behavior of s of GB-W and GB-S as derived from the $c(T)$ behavior Fig. is shown in Fig. 2. Note, that near room temperature the reduced "surface" recombination velocity shows a reduction by a factor 3 - 4 near the surface compared to the bulk for both GB-S and GB-W. The shapes of the $s(T)$ curves of GB-S and GB-W are rather similar. It seems that they are just shifted to each other.

Typical depth profiles of s along the cleaved surface after hydrogenation recorded at sample temperatures of 275, 220, and 100 K, respectively, are shown in Fig. 3. These profiles are presented for the GB-M but are representative also for the other two GBs observed. The profiles provide information about the passivation depth. There is a strong decrease of the recombination activity towards the wafer surface, which was not found in

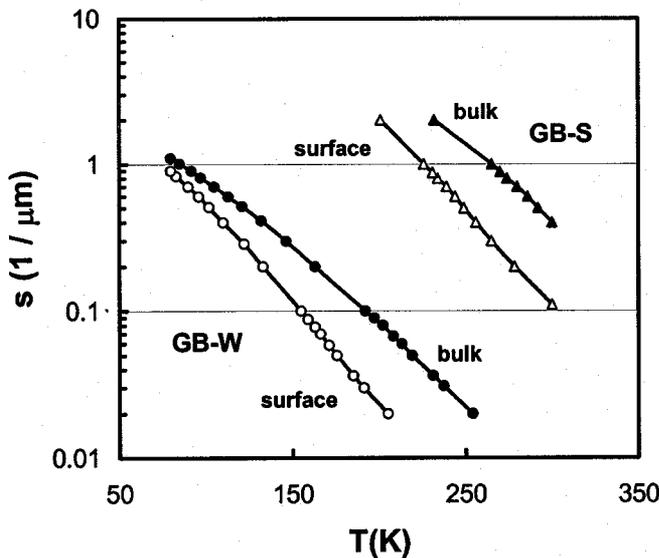


Fig. 2. The reduced "surface" recombination velocity (s) of the grain boundaries GB-S and GB-W (see Fig. 1) exhibiting strong and weak recombination activity at room temperature, respectively, as a function of the sample temperature (T). The figure was derived from the contrast data (c) presented in Fig. 2 using Donolato's c vs. s plot [10]. The recombination velocity is lowered near the surface as compared to the bulk value and s increases with decreasing T for both GBs.

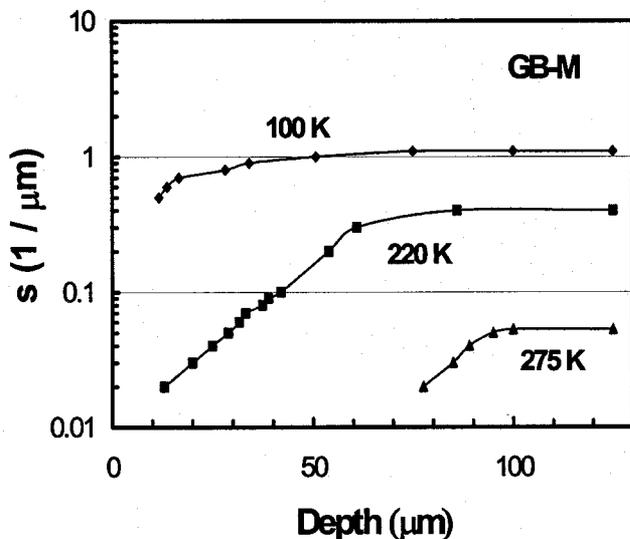


Fig. 3. Impact of the hydrogen plasma treatment on the depth profile of the reduced GB recombination velocity s as determined for GB-M at three sample temperatures. At all three temperatures s is nearly spatially independent in the bulk and decreases towards the surface indicating reduction of recombination center density.

parallel samples that had not been exposed to the hydrogen plasma but otherwise been treated identically. In the sample interior the recombination activity remains nearly unchanged. At 275 K the reduced GB recombination velocity starts to decrease at a depth of about 100 μm . This indicates the depth extension of the hydrogen passivation. At about 60 - 70 μm below the surface s drops below $s = 0.02$ which represents the method's detection limit. At $T = 220$ K s begins to drop at a depth of 80 μm . There is nearly no detectable contrast near the wafer surface. At 100 K the reduced recombination velocity starts to decrease from its bulk value at 50 μm .

Intragrain defects. Fig. 4 displays typical depth profiles of the EBIC signals measured at an identical area in between the grain boundaries. The profiles were recorded at 275 K and 120 K, respectively. To obtain more reliable results the EBIC signal was averaged over a width of about 100 μm perpendicular to the depth direction. At 275 K the EBIC signal is constant in the bulk since the intragrain defects exhibit no contrast near RT. Upon cooling, the intragrain defects become

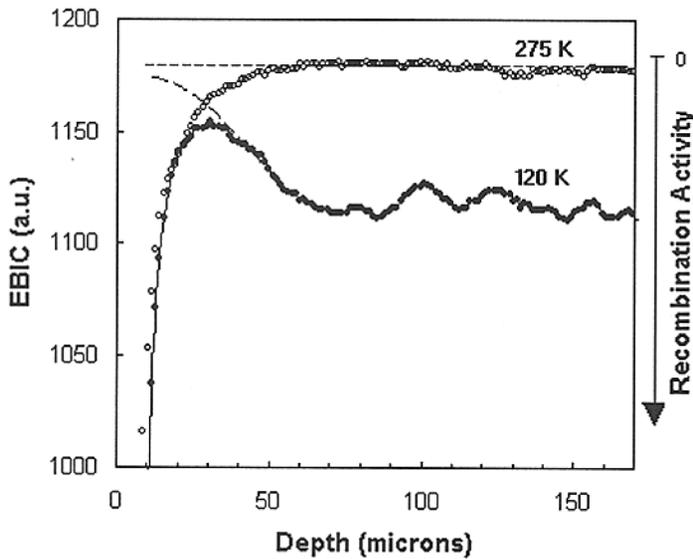


Fig. 4. EBIC intensity measured in an intragrain area along the cleaved surface at 275 K (open circles) and 120 K (solid circles), respectively. An electron beam of 30 keV and 50 pA was used. The measured profiles are extrapolated (broken lines) to visualize the expected behavior in case of negligible recombination at the wafer surface.

more and more active and can be detected as dark contrast in the EBIC micrographs (see Fig. 1). The increasing defect activity causes a reduction of the overall EBIC signal. This is the reason for the fluctuations measured at 120 K the bulk region (see Fig. 4).

Both EBIC signals are dropping towards the wafer surface. The EBIC profile measured at 275 K decreases monotonically whereas the profile at 120 K shows a maximum EBIC at a depth of about 30 μm . From this maximum the low-temperature profile decreases towards the sample interior until it reaches the bulk value at about 80 μm . Going from the maximum towards the surface, the EBIC curve decreases and approximately meets the 275 K profile. The EBIC profiles measured at untreated samples also show a decreasing signal towards the wafer surface. Therefore, we conclude that the decrease of the 275 K profile over a region of about 50 μm results from enhanced carrier recombination at the wafer surface and is not due to a variation of the materials' properties in this region. The relative increase of the EBIC signal observed at $T = 120$ K results from a decreasing recombination activity near the surface compared to the sample interior. It reflects the partial passivation of intragrain defects. The observation of the local maximum in the low-temperature profile is a result of superposition of the effects of recombination at the wafer surface and defect passivation.

Discussion

The cross-sectional EBIC measurements reveal a significant reduction of the recombination activity for both GBs and intragrain defects near the wafer surface. The apparent passivation depth is found to be temperature dependent. It decreases with decreasing temperature. The recombination activity of the defects increases simultaneously. For example, for the GB-M (see Fig. 4) an apparent

change of the passivation depth with temperature was observed from 100 μm at $T = 275\text{ K}$ to about 50 μm at $T = 100\text{ K}$. From the data for the diffusion coefficient of hydrogen in silicon [1] a hydrogen penetration of 60 – 190 μm is expected for the treatment applied (1 hour at 310 °C). This is in good agreement with the experimental passivation depth obtained from EBIC contrast measurements at $T = 275\text{ K}$.

The temperature dependence of the apparent passivation depth indicates that the dependence of the recombination activity of defects on the density of recombination centers becomes weaker with decreasing temperature. There are at least two reasons that could be responsible for such a behavior. The first one is a decrease of the minority carrier density due to diffusion limitations that cause the dependence of the contrast vs. “surface” recombination velocity as reported in [10] and as discussed above. This could play a role at GB-S, i.e., the GB with the strongest recombination activity, where EBIC contrast was observed to saturate at low temperatures (see GB-S in Fig. 2). Within the temperature range investigated in this study a saturation of the EBIC contrast was not observed for defects exhibiting weak activity (GB-W, intragrain dislocations). A second reason could be the dependence of the defect’s recombination activity itself on the density and the energetic distribution of the main recombination levels. Obviously, a simple recombination statistics assuming only one kind of recombination level cannot explain the experimental observations.

Recently, a new statistical model of the recombination at dislocations was developed by *Kveder et al.* [9]. This model considers all possible recombination channels through both the shallow and the deep levels as well as the presence of an energetic barrier for carrier capture at the dislocation. The diffusion reduction of the minority carrier density in the vicinity of dislocation is also taken into account. It predicts that the recombination activity is a linear or a super-linear function of the density of deep levels at high temperatures. The dependence on the deep level concentration at low temperatures is much weaker. Both predictions of the theoretical model are qualitatively confirmed by our experimental findings.

At room temperature the EBIC contrast of defects of weak activity is below the detection limit. To observe EBIC contrast the sample temperature has to be reduced. With decreasing temperature the contrast increases and, at the same time, the sensitivity to changes of the deep level concentration diminishes. Accordingly, at low temperature the depth profile of the deep level concentration leads only to a small change of the EBIC contrast. Therefore, visualization of the passivation effect requires a compromise between high temperatures for best sensitivity to deep levels and low temperatures for contrast detection of defects exhibiting weak activity. In view of the above arguments, the passivation depth measured at the higher temperature is closer to the real penetration depth of hydrogen.

The recombination activity of all kinds of defects in our sample increased when the temperature was decreased. In the frame of the theoretical model [8, 9] this corresponds to a density of deep levels of less than $10^6 - 10^7$ per cm of dislocation length. The recombination activity is also expected to remain independent on the deep level density at $T = 80\text{ K}$ only when the latter exceeds about $10^5 - 10^6\text{ cm}^{-1}$. A reduction of the recombination activity by a factor 3 - 4 near room temperature was found between the surface and the bulk of passivated samples which also well agrees with the rough estimation made above.

From our present experimental data no dependence of the passivation effect on type and activity of the defect could be found. From Fig. 2 it becomes evident that all defects respond nearly equally to the hydrogen treatment irrespective of their initial room temperature activity. GB-S exhibits substantial contrast already at room temperature while GB-W becomes visible only at low T . Although there is a large difference in the room temperature activity, the activity of the GBs shown in Fig. 3 is reduced at the surface by about the same factor. Additionally, the slopes of the correspondent curves are nearly the same. These results suggest that the degree of contamination as well as of hydrogen passivation is nearly the same for all investigated grain boundaries and the

intragrain defects. The difference in the recombination activity is, hence, only due to a different dislocation density within a GB.

Summary and Conclusions

We have demonstrated that the depth profile of hydrogen passivation of the defects of various initial recombination activity can be characterized by cross-sectional EBIC measurements in the temperature range of 80 - 300 K. The recombination activity of both intragrain defects and GBs was reduced by hydrogen plasma treatment down to a depth of about 80 - 100 μm . From the analysis of the temperature dependence of the recombination activity of the defects we conclude that the passivation effect is due to a reduction of the density of deep (most likely contamination-induced) defect levels. The degree of contamination as well as of hydrogen passivation was suggested to be nearly the same for all investigated grain boundaries and the intragrain defects

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Metallizations by Direct-Write Ink Jet Printing

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Abstract:

Direct-write technologies offer the potential for low cost, materials efficient deposition of contact metallizations. We report on the ink jet printing of metal organic decomposition (MOD) inks with and without nanoparticle additions. Near bulk conductivity of printed and sprayed metal films has been achieved for Ag and Ag nanocomposites. Good adhesion and ohmic contacts with a measured contact resistance of $400 \mu\Omega \cdot \text{cm}^2$ have been observed between the sprayed silver films and heavily doped n-type layer of Si. Ink jet printed films show adhesion differences as a function of the process temperature and solvent.

Introduction:

A key issue in the development of photovoltaic cells is the development of low cost materials-efficient process methodologies. Atmospheric process approaches potentially offer these advantages. Ink jet printing as a derivative of direct-write processing offers the additional advantages of low capitalization, very high materials efficiency, elimination of photolithography and noncontact processing [1]. The latter could be important with the current thrust to produce very thin cells, for example Si cells less than 100 μm thick are a current goal.

Conceptually, for Si solar cells, all device elements except the Si could be directly written or sprayed, including contact metallizations (front and rear), transparent conductors and antireflection coatings. Our initial thrust has been in the area of developing contact metallizations. As the thickness of Si cells falls below 100 μm , contact grids for the front and rear contacts can be ink jet printed, even on the rough surface of polysilicon, without contacting the thin, fragile substrates. At present, ink jets are capable of line resolutions $< 20 \mu\text{m}$, which is at least two times better than the current state of the art obtained by screen printing [2]. In addition, it is an inexpensive, atmospheric process and can be an environmentally friendly, no-waste approach.

Our specific goals are to develop inks and optimize printing parameters for highly conductive lines, achieving low contact resistance, good adhesion and high resolution.

Approach:

Overall, we have chosen to use combinations of organometallic metal precursors with metal nanoparticles. This allows essentially a mix-and-match approach between the MOD precursor and various nanoparticles which can be tailored for a particular application, i.e. doping level, thickness, process temperature etc. We use organometallic precursors as a both metal-forming component of the ink and as a "glue" to bond the nanoparticles together. The dry organometallic compound (such as silver(hexafluoroacetylacetonate)(1,5-cyclooctadiene) or Ag(hfa)(COD)) is dissolved in

an organic solvent such as toluene, ethanol or butanol. The ink is inkjet printed on a heated substrate in a desired pattern. A silver film forms upon solvent evaporation and decomposition of the printed precursor at elevated temperature ($\sim 300^{\circ}\text{C}$). Gaseous byproducts of decomposition leave the system, providing contamination-free metal films. In order to increase the silver loading of the ink and obtain higher deposition rates, silver or other metal nanoparticles may be added to the ink along with the organometallic precursor. In this configuration, silver particles comprise the main conducting volume of the resultant coating while the organometallic constituent acts as a glue for the silver particles, providing enhanced electrical and mechanical bonding of the metal particles with the substrate and between themselves. Fine, deagglomerated nanoparticulate metal powders must be used in this ink so as to avoid clogging the 10 – 50 μm orifice of the ink jet. In addition, active constituents, such as adhesion promoters, surface activators, precursors of n-dopants for selective emitters, or possibly nanosized glass frits, may be added to the ink in order to achieve the required electronic and mechanical properties of the contact.

For initial evaluation of new ink compositions, we have used spray deposition. In this technique, droplets of ink are deposited on heated substrates using an airbrush. This deposition technique is very similar to ink jet printing, but simpler and more robust. The relatively large nozzle opening of the airbrush makes it more difficult to clog. The main difference from the ink jet is that spray deposition is best suited for deposition of continuous films over large areas and is not spatially selective.

Experimental and Results:

Spray deposition:

a) Ag Metalorganic ink.

A saturated solution of Ag(hfa)COD in toluene, filtered through a 0.2 μm syringe filter, was used as the organometallic Ag ink [3]. The ink was initially sprayed on heated substrates in air using a hand-held Vega 2000 airbrush. During depositions the substrates were attached to a heated copper plate maintained at 400°C using metal clips. Smooth dense grainy coatings were obtained on glass and silicon substrates as can be seen in the SEM pictures in Figure 1(left).

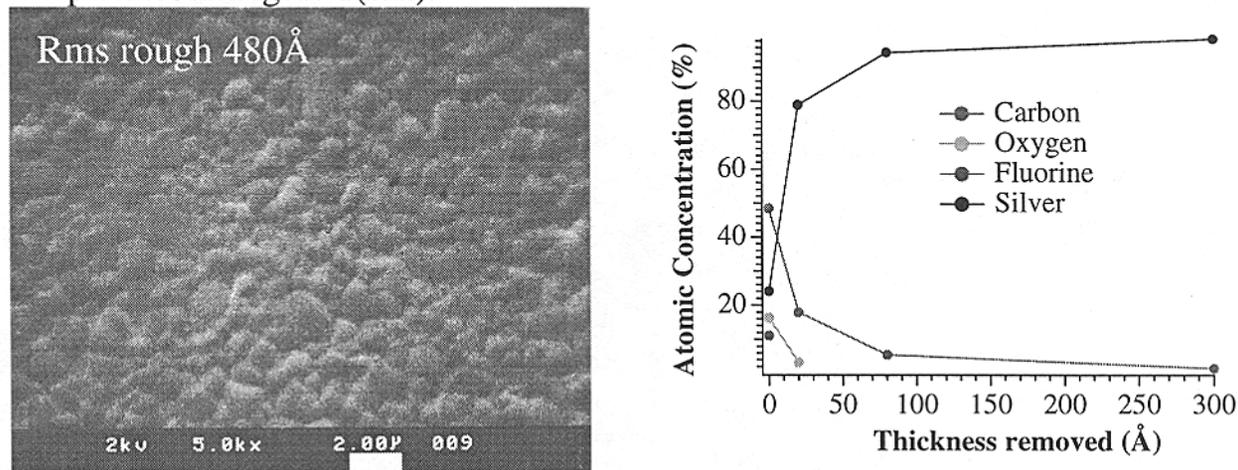


Figure 1. SEM image (left) and results of an XPS analysis (right) of Ag film spray printed on Si using ink prepared from Ag(hfa)(COD).

The thickness of the coatings deposited ranged from 0.1 μm to 4 μm . According to X-ray Photoelectron Spectroscopy (XPS), the chemical content of the coatings was pure silver once the depth was greater than approximately 100 \AA . A significant level of oxygen, fluorine and carbon impurities detected at the film surface is most likely due to post-deposition surface contamination and it rapidly decreases with depth during ion milling, as shown in Figure 1(right). XRD analysis confirmed that the coating as-deposited consisted primarily of (111) oriented silver grains with a small fraction with a (100) and (110) orientation. The adhesion strength of the sprayed 3.4 μm thick silver coating on Si was twice as good as that of conventional screen printed contacts. Conductivity of the sprayed silver layer ($2 \mu\Omega\cdot\text{cm}$) was very near that of bulk silver. Significantly, we were able to achieve ohmic contact (Figure 2) with a relatively low contact resistance ($400 \mu\Omega\cdot\text{cm}^2$) [4] between the sprayed silver coating and n-type layer of a diffused p-n junction solar cell from Evergreen Solar. The contact resistance was measured using the Transfer-Length Method (TLM) [5]. The silver pads for TLM were fabricated from the sprayed coatings using photolithography followed by an etch with 50 % nitric acid.

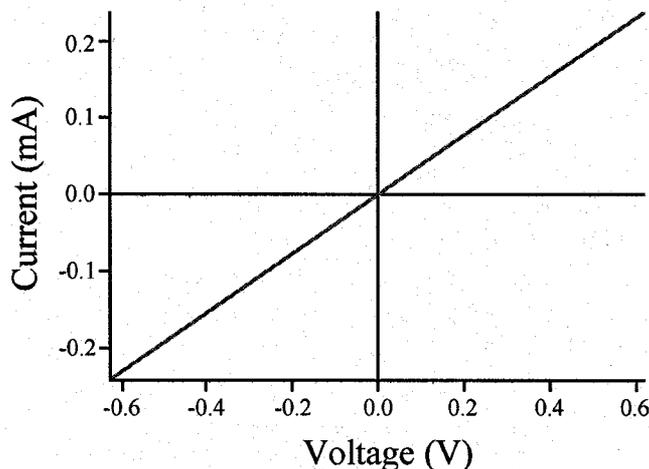


Figure 2. I-V curve for Ag(hfa)(COD) derived contact on n-type Si

These results are significant because contacts with high adhesion strength and good electronic properties were achieved with a simple, one-step, low temperature deposition process. This is in contrast to typical screen printed coatings, which require addition of glass frits to promote adhesion and high annealing temperatures ($\sim 700^\circ\text{C}$), or vacuum deposited coatings, which are expensive and require an additional adhesion layer, to achieve similar results.

b) Ag Nanoparticle/Metalorganic ink.

Composite nanoparticle/metalorganic ink was prepared by mixing 1.0 g Ag nanoparticles in a solution formed by dissolution of 1.0 g Ag(hfa)(COD) in 4 ml ethanol (1:3.9 molar ratio). This precursor was spray printed on a glass substrate heated up to 300°C . As-deposited, the 10 μm thick silver layer had a relatively porous grainy structure (Figure 3).

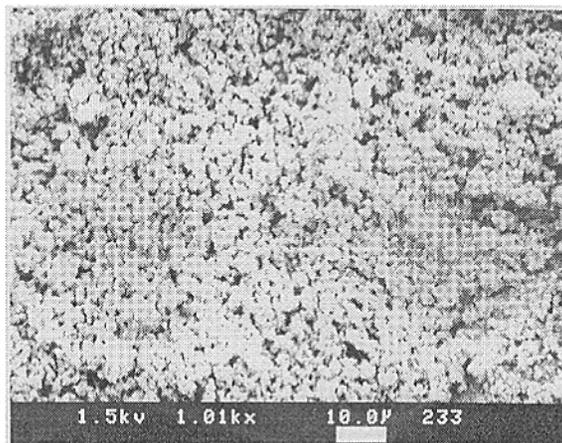


Figure 3. SEM image of Ag film on glass spray printed at 300°C

The layer in figure 3 was characterized by good adhesion to a Pyrex microscope slide, which was confirmed with the Scotch tape pull test (15-20lb/in). The high initial resistivity of the as-deposited silver layer ($58 \mu\Omega\text{-cm}$) dropped to $2.4 \mu\Omega\text{cm}$, near the value for bulk silver, after annealing for 30 minutes in air at 400°C. The high deposition rate along with the excellent conducting properties of the deposited silver layer from the composite ink are encouraging and we are planning to proceed to the next step – to evaluate the “printability” of the composite ink by inkjet. The primary concern is that agglomerates of the Ag particles may clog the small 50 μm orifice of the current inkjet. Also we need to optimize the ink composition to achieve stable particle suspension. When the Ag particles are simply mixed in to the organometallic ink, they tend to sediment on the walls of the container. This may require a capping agent for the Ag nanoparticles, which would potentially solve both the agglomeration and printing problems at the same time.

Direct Write Ag by Ink Jet Printing

a) Epson printer

Simple test patterns were printed with an Epson Stylus Color 740 piezoelectric inkjet printer on glass and Si substrates using Ag(hfa)(COD) based organometallic ink, Figure 4. The existing cartridges on the ink jet were removed, cleaned and refilled with the Ag precursor ink. The ink was printed on a CD label writer and substrate heating was provided with a heat gun.

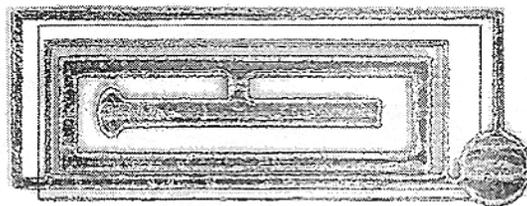


Figure 4. Silver test pattern printed with an ink jet printer using Ag(hfa)(COD) based ink.

The ink was prepared according to the recipe above with ethanol replacing toluene as the solvent. Toluene was found to be incompatible with the plastic of the ink cartridges. The glass substrate was heated using a heat gun prior to deposition in order to facilitate solvent evaporation and to prevent the ink from running on the surface. Three layers were printed on top of each other to build a reasonably thick silver coating. After each printed layer the glass slide was heated with the heat gun until the printed pattern took on a metallic appearance. At the end of the deposition, the sample was annealed in air at 300°C for 20 minutes in a quartz tube furnace. This final annealing eliminated dark brown spots that could be seen in the coating just after the deposition. We assume that these were Ag(hfa)(COD) spots that decomposed forming Ag during the annealing step.

The average thickness of the trilayer coating was $\sim 2000 \text{ \AA}$, giving a deposition rate of $\sim 700 \text{ \AA}$ per layer. The surface morphology of the ink jet printed silver observed by AFM closely resembles the silver layers deposited by spraying as above (Figure 5).

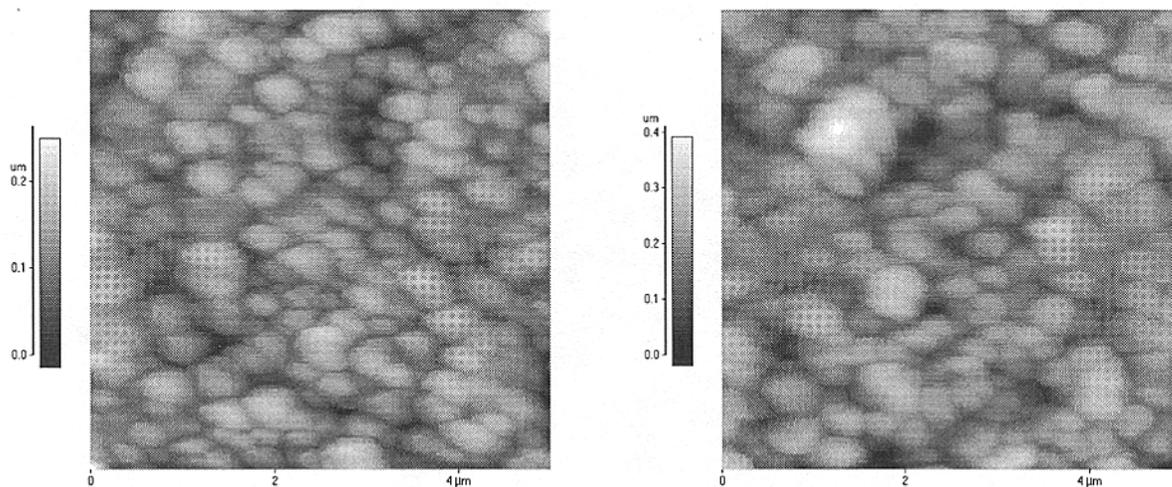


Figure 5. Ag film on glass spray deposited (left) and inkjet printed after heating (right).

The resistivity of the coating measured by the 4-probe technique was $\sim 5 \mu\Omega \cdot \text{cm}$, which is a little over a factor of two higher than the resistivity of bulk silver. Good adhesion of the silver coating to the glass slide was confirmed with the Scotch tape pull test. The disadvantage of using the commercial Epson printer is in lack of control over the printing conditions used. The Epson is optimized for water-based color inks. Using the same printing conditions with the ethanol-based ink resulted in reduced line quality. A single line printed on a glass slide (Figure 6) was 200 μm wide. It was observed that the silver accumulated at the edges of the line.

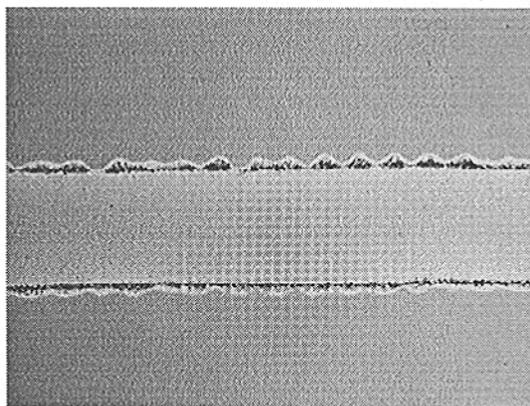


Figure 6. Single line pattern printed with the Epson ink jet printer using Ag(hfa)(COD) based ink. The width of the line is 200 μm .

This phenomenon may be understood by considering the dynamics of liquid perturbation during the processes of drop evaporation [6]

b) Microfab Ink Jet System

The new Microfab system is essentially a drop on demand piezoelectric ink jet where user control of waveform, frequency, amplitude, line pressure and orifice size are all possible. Drops form by voltage pulses applied to a piezoelectric actuator that creates an acoustic wave in the body of a glass capillary filled with ink. The stimulated waves break the ink meniscus off the tip of the jet at the frequency of the pulse generation. By controlling the parameters of the voltage pulse, printing variables such as the frequency of drop generation, the volume/size of the drops and the speed of the drop at ejection can be controlled. Other advantages of the new system are that the jet system does not have plastic parts and thus gives us more freedom for choosing solvents and printing at higher temperatures. Heads are available for high temperature and nitrogen purged printing. For the initial printing experiments however, we used the same ethanol-based ink as employed in the Epson experiments above. Because of the relatively low boiling point of the ethanol, we had to choose a high pulse frequency (1500 Hz) and a relatively low substrate temperature (150 °C) to maintain an uninterrupted jet of drops. Single-line patterns were written on a heated glass substrate by linear motion of the inkjet print-head attached to the computer controlled X-Y table. The jet-to-substrate distance was maintained at ~1 cm. In order to convert printed precursor lines to metallic silver, the printed substrates were heated with a heat gun to above the decomposition temperature of the organometallic compound. The lines obtained had better silver film uniformity and the same (200 μm) line width as those printed with the conventional Epson printer. Figure 7 illustrates a line printed with the Microfab system. The Ag is uniform across the line width. The orifice size in the Microfab inkjet system is 2.5 times larger than that of the Epson printer (50 μm vs. 20 μm), and yet the widths of the lines obtained were the same. The larger orifice size, which also delivers larger drops, gave a more uniform line with better resolution (relative to orifice size) because the Microfab system can tolerate higher substrate temperatures. At higher substrate temperatures solvent evaporation occurs more rapidly and the ink does not have time to spread as much, leading to higher resolution. These results indicate that the Microfab inkjet should be capable of much better resolution if a smaller orifice is used. (Note that heads are available from Microfab

with orifices down to 10 μm .) In our most recent printing experiments, we were able to achieve 100 μm wide lines by switching to butanol-based inks. Replacing ethanol with butanol, a solvent with higher boiling temperature, allowed a reduced drop ejection rate, higher substrate temperature and shorter jet-to-substrate distance to be used. The combination of these changes resulted in better resolution by a factor of two. An additional benefit of using the butanol-based ink is that we were able to print on a substrate heated to well above the decomposition point of the organometallic compound, thus eliminating the need for a post-deposition annealing step.

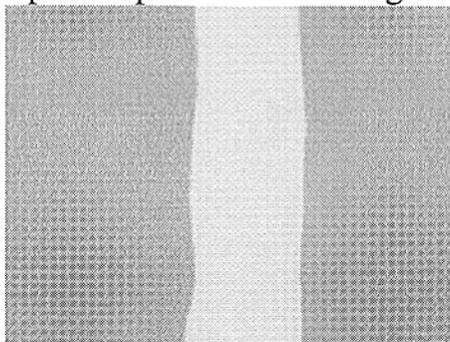


Figure 7. Single line pattern printed with Microfab ink jet printer using Ag(hfa)(COD) based ink. The width of the line is 200 μm .

Conclusion:

We have demonstrated that direct MOD or composite nanoparticle /MOD deposition of Ag on glass and Si produces films with conductivity comparable to vacuum deposited materials. Ink jet printing of the precursors produced line resolutions comparable to those obtained by current screen print technology by a non-contact approach. The deposition rates can be very high, especially for the composite inks. By going to smaller orifice size, we anticipate factors of 2 or greater improvement in resolution with the possibility of one pass processing. We are also investigating other metallizations by this approach.

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Shunt Detection in Solar Cells with the Corescanner and Lock-in Thermography: A Comparison

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Abstract: The Corescanner has been recently introduced as a simple and cheap instrument to map Contact RESistance of the front side metallisation. Additionally, the Corescanner may be used to localize shunts according to the Parallel Resistance Analysis by Mapping of Potential method (PRAMP). Until now shunts have been imaged most clearly using infrared (IR) lock-in thermography, which is quite an expensive technique. In this contribution PRAMP and lock-in thermography are directly compared by investigating an identical sample. It turned out that the sensitivity of PRAMP is not as high as that of lock-in thermography, and PRAMP cannot detect shunts below metallisation, in contrast to lock-in thermography. These conclusions show that the Corescanner is suited for solving most processing problems causing strong local shunts, whereas the lock-in thermography is best for a complete determination of all shunts.

1. Introduction

As many previous investigations have shown, the electronic properties of solar cells are rarely homogeneously distributed. As a rule, both photocurrent collection properties and I-V characteristic may be position-dependent, leading to position dependent values of the short circuit current density (J_{sc}) as well as of the open circuit voltage (V_{oc}) and of the fill factor (FF) of the cells. While inhomogeneities of J_{sc} may easily be mapped by Light Beam Induced Current (LBIC) techniques under short circuit conditions, inhomogeneities of the I-V characteristic, leading to an inhomogeneous distribution of V_{oc} and FF, may not easily be mapped since the current is flowing through the whole cell when a bias is applied. One possible way out is to separate the cell area into small pieces and to map the characteristics of these cell fractions separately (Sopori [1], Hässler et al. [2]). This procedure, however, requires an extensive structuring procedure, thereby destroying the original cell. Moreover, edge leakage currents may obscure the local characteristics, and it may be a problem to separate cell fractions below grid metallization lines and to investigate the edge of the cell [2]. Therefore it is highly desirable to have a method for investigating shunting phenomena non-destructively on solar cells which have been fabricated without special preparation.

2. Shunt detection by lock-in thermography and Corescanner (in PRAMP mode)

One of the options to image shunts non-destructively is to evaluate the heat dissipated at the shunt positions under an applied bias in the dark. If the solar cell is biased near its maximum power point (approx. 0.5 V forward bias for typical crystalline silicon cells), the situation under operation is simulated, hence the shunt currents are flowing as during operation of the cell. If the emitter potential can be assumed to be position-independent in first approximation, the locally dissipated heat is proportional to the locally flowing current density. Hence, a thermographic inspection should reveal the local distribution of shunting currents in the cell. The problem with this approach is that 1. the temperature contrasts are very weak being typically in the order of 1

mK and below, and that 2. due to the large heat conductivity of silicon the thermal contrasts tend to "smear out" laterally, leading to a poor spatial resolution of the investigation. Both problems may be solved by using lock-in thermography instead of stationary one. In lock-in thermography a repetitively pulsed bias is applied to the sample and the resulting periodic temperature modulation at the surface is detected and averaged over many pulse periods using lock-in techniques. This technique has been used first successfully for shunting investigations in contact mode by mechanically scanning a thermistor across the surface of the cell (Dynamic Precision Contact Thermography, DPCT, Breitenstein et al. [3]). Meanwhile a non-contacting variant of lock-in thermography using a highly sensitive infrared (IR) thermocamera has been developed (Breitenstein et al. [4, 5]), which has led to the development of the commercially available lock-in thermography system TDL 384 M 'Lock-in' by Thermosensorik GmbH Erlangen / Germany [6]. Here the solar cell is imaged by a thermocamera and the incoming frames are digitally processed to perform the lock-in correlation procedure of every image pixel on-line. After an acquisition time of some minutes the dominant shunts become clearly visible as bright spots in the T-modulation amplitude image.

It was mentioned that the emitter surface potential should be constant "in first approximation" for performing lock-in thermography. However, in second approximation it is not constant anymore around local shunts, since owing to the finite emitter layer conductivity there is an inevitable voltage drop on the current path to the shunt. Hence, if a solar cell is forward biased in the dark and the potential is mapped sufficiently precise across the emitter, the potential map should also reflect the presence of local shunts in the emitter area. This is the physical basis of the new technique called Parallel Resistance Analysis by Mapping of Potential (PRAMP, Van der Heide et al. [7]). This technique is one of the two that the Corescanner instrument uses to investigate resistance problems on solar cells; the other measurement mode of the Corescanner is called Specific Contact Resistance Analysis by Mapping of Potential (SCRAMP). Both PRAMP and SCRAMP are patented [8] and an industrial version of the Corescanner is currently being developed by ECN (Van der Heide et al. [9, 10]), and will soon be available.

In a PRAMP investigation a constant forward bias is applied to a solar cell in the dark, and a tungsten probe is scanned across the surface to map the local emitter potential. In order to penetrate an isolating antireflection coating, the tungsten probe scratches the surface to a certain degree during the measurement. The result of a PRAMP scan is a potential map where local shunts are visible as local potential minima.

In principle PRAMP should lead to similar results as lock-in thermography does. Bright spots in the lock-in thermograms should correspond to dark spots in the potential maps. Our main question is whether shunts below grid lines are visible in the PRAMP image since the metallic grid lines have a much lower resistance than the emitter layer. Therefore in this contribution the techniques will be compared by investigating an identical sample successively by using both techniques. The sample investigated here is an experimental multicrystalline solar cell suffering from serious shunting problems (shunt resistance $390 \Omega\text{cm}^2$).

3. Results

The following procedure was performed for the investigated solar cell: First, lock-in thermography measurements (a survey image over the whole cell and a detailed image) were made in the virgin state of the cell before the PRAMP measurement (Fig. 1). Then different PRAMP measurements were performed with the Corescanner, both scanning the whole cell and the region of the detailed imaging (Fig. 2). Finally, the same regions were imaged again by lock-

in thermography (Fig. 3). If there were any degradation of the shunting behaviour of the cell due to the PRAMP investigation, this should be visible in the comparison between Figs. 1 and 3. The regions of the detailed investigations are always indicated in Figs. 1 to 3. In the thermograms in Fig. 1 a strong shunting region is visible in the lower left corner and a weaker one in the upper left corner, directly at the edge. As can be seen in the contrast enhanced image (c), both major grid lines are showing an increased injection current density, and around the central part of the cell a number of minor shunts are visible. The contrast enhanced detail image (d) shows that there are actually several minor shunts in the detail region.

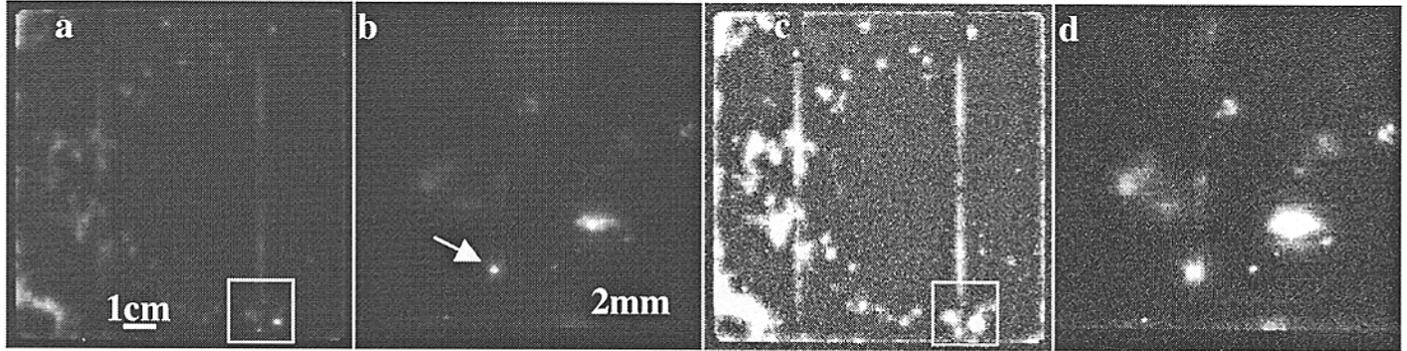


Fig. 1: Lock-in thermograms before the PRAMP investigation. (a) survey, (b) detail, (c) survey; contrast enhanced, (d) detail; contrast enhanced

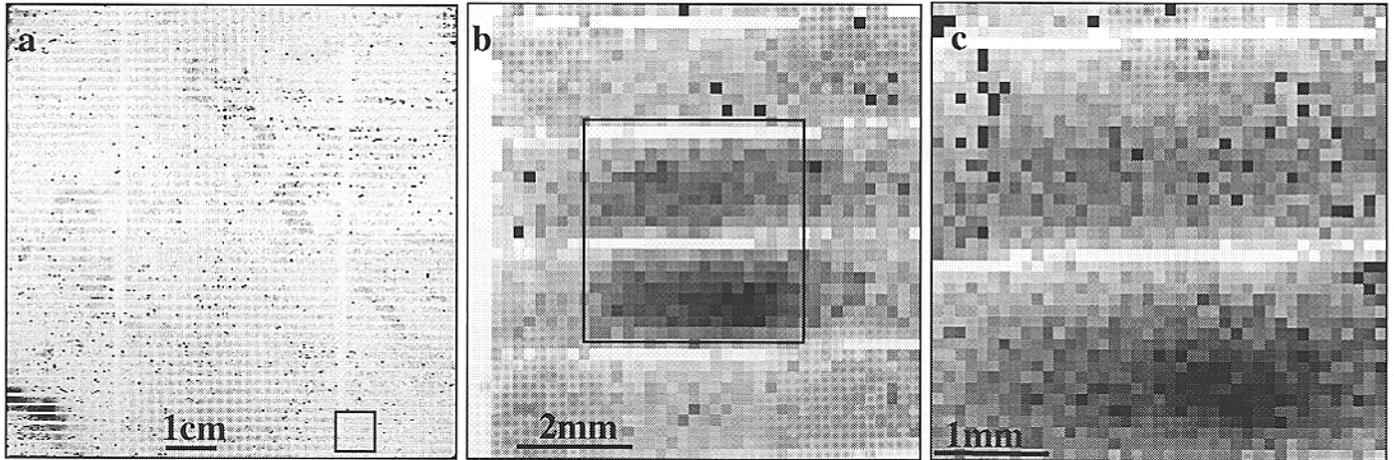


Fig. 2: PRAMP potential map: (a) survey, (b) detail 1, (c) detail 2

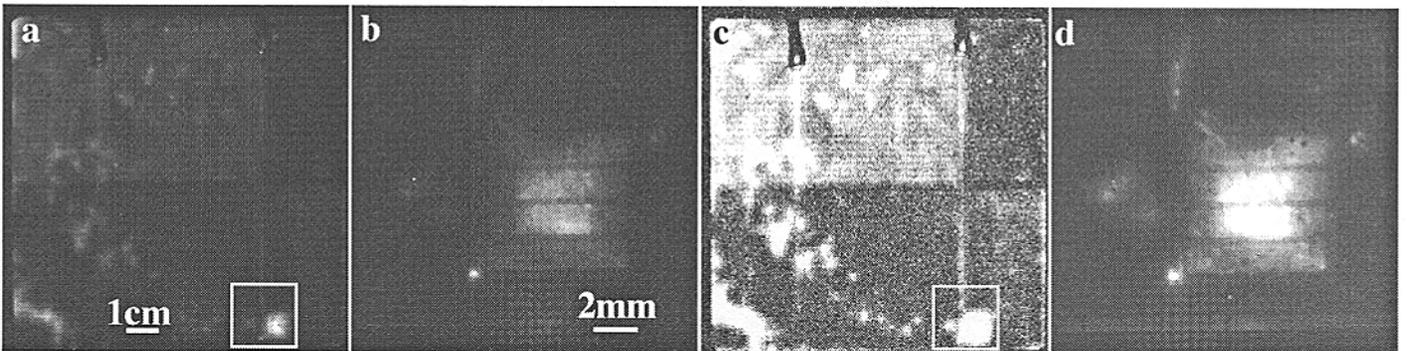


Fig. 3: Lock-in thermograms after the PRAMP investigation: (a) survey, (b) detail, (c) survey; contrast enhanced, (d) detail; contrast slightly enhanced

The PRAMP investigation also clearly reveals the strong shunts in the upper and lower left corners. The spatial resolution of thermography is better than that of PRAMP. However, there are considerable differences in the weaker contrast features. They may come from the fact that Fig. 2 (a) was measured at an applied voltage of only 0.2 V, contrary to the thermograms which all have been measured at 0.5 V. In the detailed potential map in Fig. 2 (b), which also was measured at

0.5 V, in the lower part the strongest shunt of the detailed thermogram in Fig. 1 (b) is visible. However, the weaker shunts, which are clearly visible in thermography, remain invisible in PRAMP. This holds especially for the second (lower left) shunt in Fig. 1 (b), which is lying below a major grid line (see arrow in Fig. 1 b). Generally, the regions which have been slightly damaged by PRAMP are visible as bright regions in the lock-in thermograms made after scanning. This can be seen by comparing Figs. 1 (c) and 3 (c), which are displayed in the same scaling, and becomes visible most clearly in Fig. 3 (d), where the regions scanned in Figs. 2 (b) and (c) can easily be seen.

The accuracy of the PRAMP investigation could be enhanced by converting from a d.c. to an a.c. (lock-in) technique. Hence, as in lock-in thermography, the bias may be applied as a pulsed bias, and the surface potential signal may be measured using lock-in techniques. This could improve the accuracy of the measurement by a factor of 10, which should be sufficient to investigate also weaker shunts. An alternative to the PRAMP method could be to detect the pulsed surface potential capacitively similar as in the surface photovoltage (SPV) technique.

4. Conclusions

The demonstrated results allow to draw the following conclusions:

1. The Corescanner can image local shunts by PRAMP when they are reducing efficiency and when they are not located below metallization grid lines.
2. Weak shunts and shunts below metallization grid lines remain invisible in PRAMP investigations. However, weak shunts between grid lines that cannot be detected by PRAMP are of limited importance regarding efficiency, unless they have a high density (see e.g. Langenkamp and Breitenstein [11]). Shunts under the grid lines could be of considerable magnitude before they are detected by PRAMP due to the electrical conductivity of the grid lines. Therefore, shunts occurring during metallisation can not be detected by PRAMP, in contrast to lock-in thermography.
3. Unlike thermography, PRAMP is a slightly intrusive measurement technique, which results in an increased shunting after measuring.

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Etch Pit and EBIC Correlations of High Purity Dislocated FZ Silicon

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1. Introduction

An essential requirement for high efficiency photovoltaic devices is substrate material with a long diffusion length. Since Czochralski wafers are known to suffer from carrier lifetime degradation due to bulk recombination at oxygen precipitates, using low oxygen content wafers grown by the float zone (FZ) process is a more suitable choice as starting material. Unfortunately, an inherent disadvantage of high yield loss due to breakage and mechanical failure is associated with FZ silicon. The incorporation of low concentrations of nitrogen during FZ growth has however been shown to dramatically improve the strength, while simultaneously producing material with high minority carrier lifetimes [1]. Efforts underway at NCSU related to oxygen precipitates are described in a companion paper at this workshop (Rozgonyi *et al.*). Since dislocations are also anticipated to be a dominant factor impeding carrier lifetimes, the present work focuses on the electrical and structural properties of dislocations deliberately grown into ultra pure FZ material.

2. Experimental

High purity $\langle 111 \rangle$ FZ silicon produced at NREL was sliced into a series of radial sections. The crystal was lightly gallium doped, with a resistivity varying between 2 and 9 ohm-cm. Near-surface defects were revealed by Wright-Jenkins [2] etching of the surfaces for three minutes, followed by Nomarski differential interference contrast optical microscopy. Corresponding room temperature Electron Beam Induced Current (EBIC) measurements were performed using aluminum Schottky diodes. Profiling of individual defects below the surface was determined by varying the Schottky diode bias to change the space-charge depth below the contacts.

3. Results and Discussion

Nomarski as well as EBIC measurements were performed on two wafers originating from different regions of the ingot, which had different dislocation densities. Initially, in order to delineate dislocations on the sample, the wafer farthest from the crystal seed was preferentially etched. Fig. 1(a) shows a Nomarski image of the etched surface following deposition of the Al Schottky contact. A high density of dislocations can be seen exiting the wafer surface. The dislocations are most likely occupying a $\{111\}$ habit plane, moving along a $\langle 110 \rangle$ direction [3]. In addition to these "threading" dislocations, a low concentration of extended dislocations lying parallel to the wafer surface are also observed (see Fig. 1(a)) due to the near-surface strain produced by the dislocation causing a variation in the surface etch rate. The "planar" dislocation gradually exits the $[111]$ surface leaving a surface pit.

EBIC measurements on the same region revealed that both dislocation types act as very strong recombination centers (see Fig. 1(b)). Fig. 1 clearly illustrates how the dark regions of high recombination correspond to the etch features seen in Fig. 1(a). The contrast of the planar dislocation can also be seen to decrease as it gradually recedes into the material.

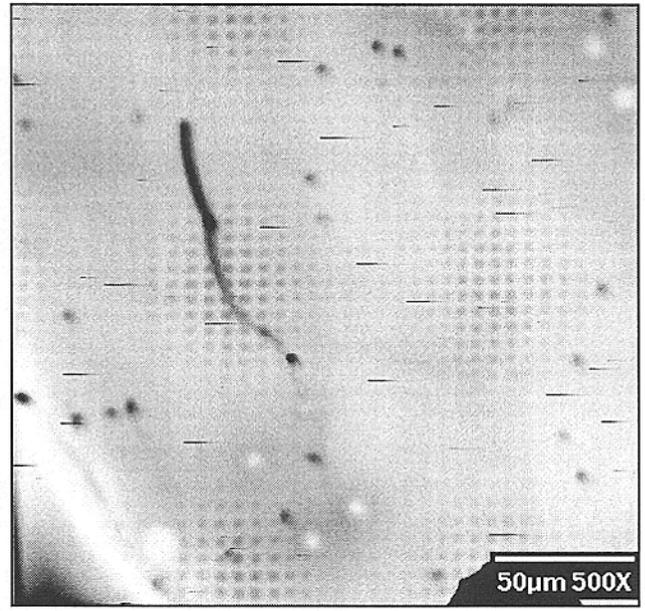
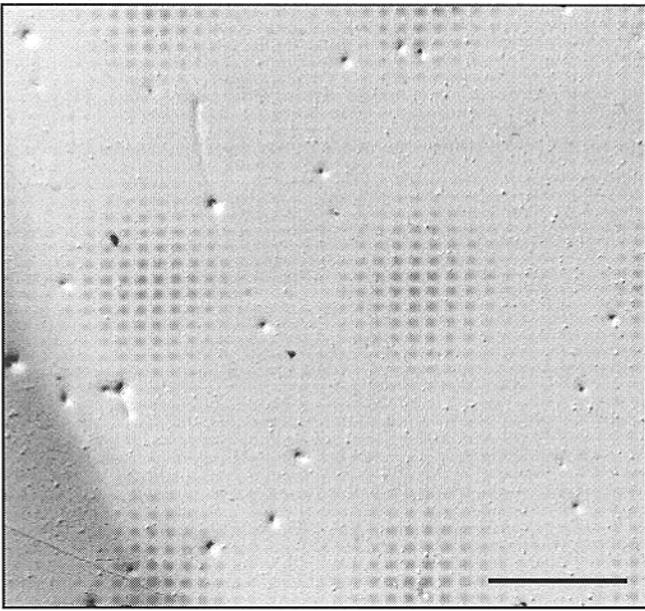


Figure 1 Nomarski (a) and EBIC/SEM (b) images of threading and planar dislocations exiting from the [111] surface.

Since the wafer in Fig.1 was etched in order to correlate the optical and EBIC images, the possibility of Cu contamination from the Wright etch arose. In order to exclude this possibility, EBIC measurements were repeated on an unetched wafer closer to the seed crystal. Fig. 2(a) shows the dislocations in this wafer to exhibit the same electrical active as those in Fig. 1. In addition, the EBIC images in Figs. 2 (a) and (b) were obtained with and without a reverse bias applied to the Schottky contact, respectively. Increasing the reverse bias from 0 to 1 V resulted in a dramatic reduction in the contrast of the planar dislocation, which most likely lies within the depletion region under a 1 V bias. However, the contrast associated with the threading dislocations exiting the surface remained unaffected by the change in space-charge depth. This again confirms that the planer dislocations only occupy the planes parallel to the surface and that the edge dislocations extend along the $\langle 111 \rangle$ growth direction.

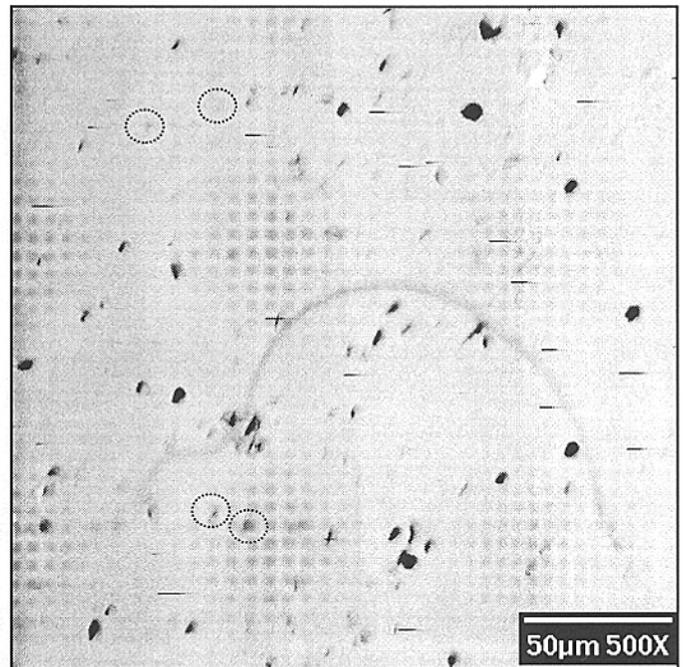
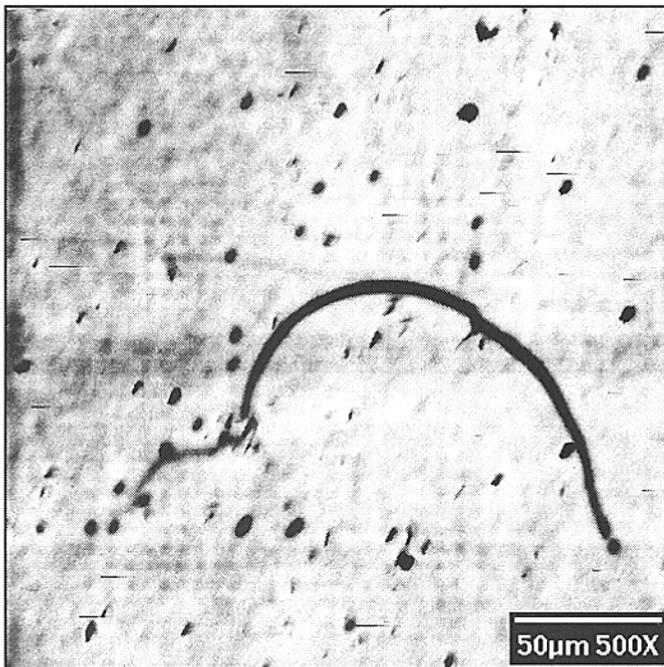


Figure 2 EBIC/SEM images illustrating the bias dependence of dislocations (a) without, and (b) with a 1 V reverse bias applied to the Schottky contact. The regions within the dotted circles are believed to contain prismatic dislocation loops.

It is interesting to note that some of the point-like recombination regions observed in Fig. 2(a) are absent in the reverse biased image (indicated by the dotted circles). These recombination centers are also believed to lie within the depletion depth and are likely to be small prismatic dislocation loops without any significant threading component.

In the case of impurity free silicon (in which instance the dislocation will not be decorated), the dislocations are not expected to act as carrier recombination centers at room temperature [4]. However, in the case of material with a high density of point defects, the agglomeration of these defect along the dislocations would result in charging, and consequently in the trapping of free carriers [5].

4. Conclusions

Since the material investigated is expected to be of high purity, the electrical activity exhibited by the dislocations at room temperature suggests that the recombination is most likely due to point defect related complexes at the dislocations. This is in contrast to prior work on the electrical activity of epitaxial misfit dislocations for which EBIC contrast was only obtained at cryogenic temperatures, unless the dislocations were deliberately decorated with metallic impurities [4].

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In-line Testing of Minority-Carrier Lifetime

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Abstract— The measurement of minority-carrier lifetime has emerged as a common and very useful method for process optimization and diagnostic studies. This paper will discuss the requirements for an instrument to perform these task inline in an automated production setting. Initial work towards this goal will be described.

I. Introduction

The typical manufacturing processes for solar cells generally do not include much in-process monitoring of the electronic properties of the silicon wafer. Although high-efficiency solar cell processes on float-zone wafers have long used extensive process control using minority-carrier measurements, this has generally not been true in typical large-scale production of terrestrial cells. This fact has been primarily due to the difficulties encountered in the interpretation of the data from lower-quality silicon substrates.

This paper describes the basic attributes required for a tool to be useful as an in-line process monitor in production lines. A successful implementation of this tool into production would allow process control and continuous optimization using the techniques developed in numerous recent R&D studies.

II. Basic Requirements for a Useful Tool.

The process steps where useful information might be obtained from an inline process monitor are shown in Table I. Of these steps, the most informative might be measurement of the incoming wafers, and measurement directly after the phosphorus diffusion.

We propose that for use in industrial silicon solar cells, an inline tool for measuring minority-carrier lifetime must have the following attributes.

- 1) Accurate resolution of minority-carrier lifetime in the range of 0.1- 50 μ s.
- 2) Measurement of the lifetime in the minority-carrier density range of interest, preferably the injection level present in functioning solar cells between the maximum power point and the open-circuit voltage.
- 3) Accurate discrimination of minority-carrier lifetime in wafers with widely varying trapping effects.
- 4) The method should be contactless.
- 5) The measurement must be fast, in the range of 30 wafers a minute.
- 6) The instrument must be capable of unattended operation, in a rugged environment without temperature control.

Table 1.

Process step	Electronic Process monitors	
	Sheet resistance	Lifetime
Incoming wafers	X	X
Etching		X
Phosphorus Diffusion	X	X
Passivation &AR		X
Back metal/anneal	X	X
Front Metal/anneal		X

This poster will present the latest results towards achieving these goals by adapting a standard laboratory instrument that applies the Quasi-steady-state photoconductance method described in references 1-5.

II. Quasi-Steady-State Photoconductance

In this method, a light is incident simultaneously on the wafer and a reference cell. The photoconductance in the wafer is determined by a contactless inductive technique. The incident light intensity is determined by a calibrated reference solar cell.

The lifetime is then calculated as:

$$1) \text{ Effective Lifetime} = \frac{K * \text{Photoconductance}}{(\text{Incident Light Intensity})}$$

where K is a slowly varying function of the mobility of electrons and holes as well as the optics of the wafer under test. The principles of steady-state photoconductance lifetime measurement are detailed in (1-5).

The effective lifetime is a combination of surface and bulk properties of the wafer. Various techniques can be applied to separate and evaluate the bulk and surface properties(6,7).

This instruments used in this work (12) have demonstrated the first two criteria, the capability to measure lifetime at a specified carrier density in the lifetime range of interest.

At low minority-carrier injection levels, the effective lifetime is dominated by trapping effects. These have been discussed in (8-11), where a classic model from Hornbeck and Haynes was applied to modern multicrystalline wafer data. This lifetime at low apparent carrier density is actually the lifetime of the trapped minority carriers rather than free minority carriers in the conduction band.

The importance of this effect is shown for an unpassivated multicrystalline wafer in Fig. 1. In

the minority-carrier density range of interest, a correction of the trapping effects is absolutely necessary. Without correction, the minority-carrier lifetime would be overestimated by a factor of 30 at a minority-carrier density of $1 \times 10^{14} \text{ cm}^{-3}$.

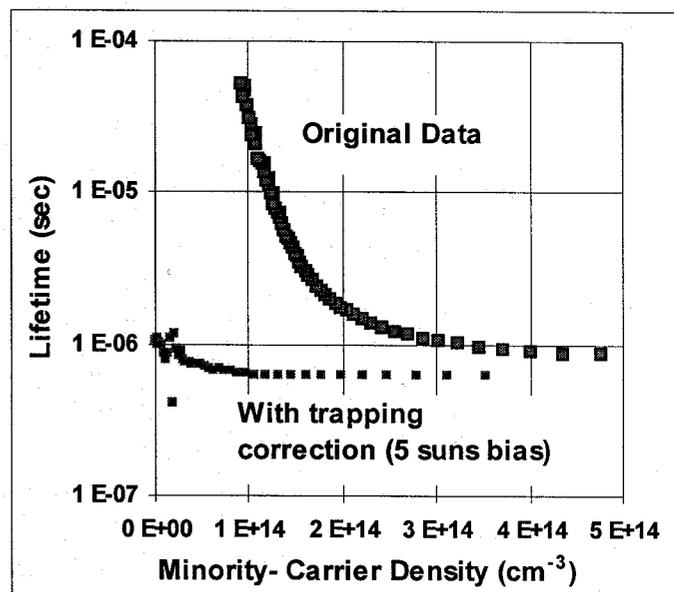


Fig. 1. Analyzed photoconductance data from an unpassivated multicrystalline wafer. Without correction of trapping effects, the results in the minority carrier density range of interest for solar cells are highly inaccurate.

This can be dealt with by fitting a trapping model to this data as demonstrated by MacDonald et al.(9). Alternatively, with steady-state data as shown in Fig. 1, a "bias light" method can be used to minimize the effect of the trapping on the calculated lifetime. A comparison of the simplified method with the full model is described in Ref. (10). The understanding presented in these references guide the development of data analysis suitable for quickly evaluating industrial wafers at the various stages of solar cell fabrication.

The instruments used in this study (12) are contactless. In R&D use, the wafer is simply placed onto a stage directly above the sensor. For industrial applications, this can cause wear and potential wafer contamination. Figure 2 shows that the instruments can be used in a truly non-contact mode, with a specified spacing between

the wafer and the sensor head. This spacing can be as much as several millimeters.

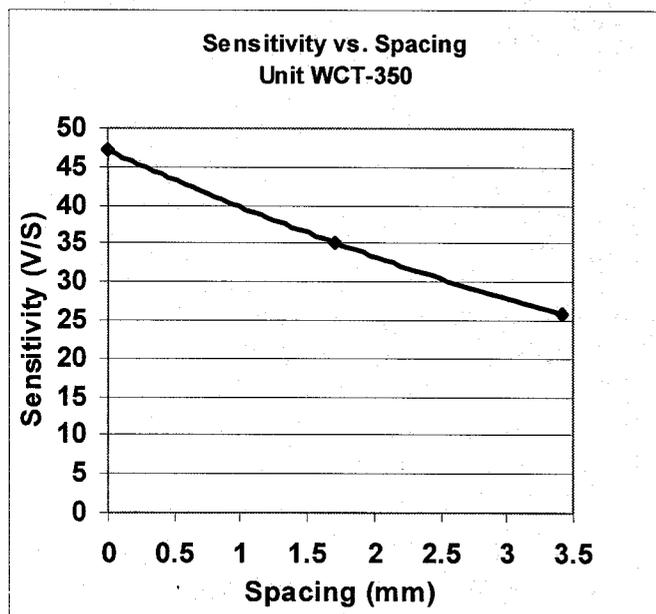


Fig. 2. A characterization of an instrument indicating the sensitivity to measuring conductance as a function of distance between the wafer and the instrument. For a flexible, truly non-contact implementation, the wafer can be separated from the instrument by several millimeters.

A characterization of repeatability and performance vs. temperature is shown in Figure 3. 15,000 measurements were taken for a single wafer over an ten hour period. The ambient temperature was allowed to vary over 6 °C. The resulting measurements indicated a standard deviation on the mean of 0.75%.

I. CONCLUSIONS

The development of tools for measuring the minority-carrier lifetime in a production environment could be quite useful for process optimization and control. The development of such a tool is in progress. Initial results have given a proof of concept for a rapid, contactless measurement with a capability of 1800 wafers per hour.

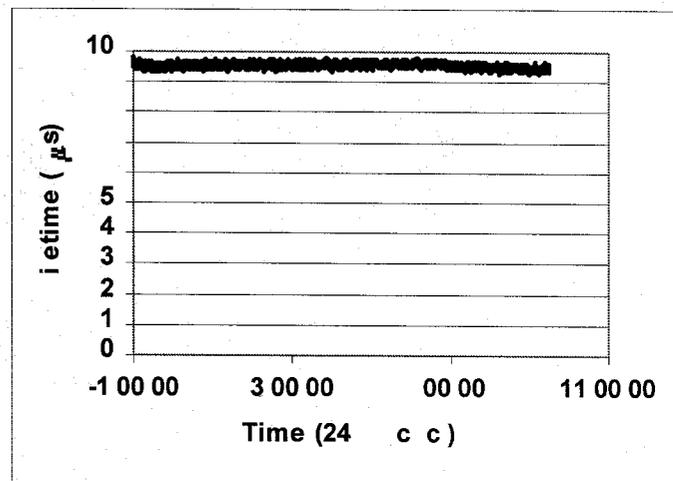


Fig. 3. 15,000 consecutive measurements on one wafer without operator intervention.. The standard deviation on the mean value for the measurement was $\pm 0.75\%$. The ambient temperature was varied from 15 C to 21 C over an 10-hour period.

Measurements taken during an ambient temperature excursion of 6 °C indicate that a standard deviation in the lifetime measurement results of less than $\pm 0.75\%$ is maintained.

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Room-Temperature Mapping of Defects in mc-Si Wafers and Solar Cells

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During crystal growth and processing of microcrystalline Si (mc-Si) wafers the dislocations are created as a means to partially relieve residual thermal-elastic stress. It is known, that presence of dislocations degrades the electronic quality of mc-Si. Strong inhomogeneity in mc-Si wafers gives rise to distinct regions of a high and low minority carrier lifetime. The low lifetime regions corresponding to an enhanced carrier recombination at defects deteriorate solar cell efficiency serving as current shunts. We applied the scanning room temperature photoluminescence (PL) and EBIC techniques to study recombination centers located in areas of mc-Si wafers with enhanced recombination activity of defects. By comparing room temperature PL mapping at band-to-band and defects band emission with the distribution of dislocations measured by light scattering technique (PVSCAN 5000), we found that the defect PL band at 0.8eV positively correlates with dislocations. Concurrently, at low temperatures a characteristic quartet of the dislocation D-lines is observed in low lifetime regions. One of these lines, D₁, can be tracked as temperature is increased and linked to the 0.8eV defect band at 300K. Using temperature dependent EBIC, we found that 0.8eV PL band originates from dislocations with weak contamination level down to a few tens impurity atoms per μm of the dislocation length. This study reveals that dislocations moderately contaminated with point defect precipitates (presumably, heavy metals) are a primary recombination centers in mc-Si solar cells.

EFFECT OF ALUMINUM-INDUCED GETTERING AND BACKSIDE SURFACE FIELD ON THE EFFICIENCY OF SILICON SOLAR CELLS

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ABSTRACT

In silicon solar cell fabrication, impurity gettering from Si by an aluminum layer and indiffusion of Al for creating the back surface field (BSF) are inherently carried out in the same process. We have modeled these two processes and analyzed their impact on solar cell efficiency. The output of gettering and Al indiffusion modeling is used as an input for calculation of solar cell efficiency. The cell efficiency gain is obtained as a function of the processes duration. To check the relative contributions of gettering and BSF in improving the cell efficiency, their effects are evaluated together as well as separately. It is found that, for solar cells fabricated from low quality, multicrystalline Si, the efficiency gain is solely due to gettering. In solar cells made of high quality Si, the efficiency gain is primarily due to gettering, but the BSF may play a significant role if the cell thickness is less than about 200 μm . The two effects are found to be synergistic. The model provides a means for optimization of the temperature regime for both processes, as well as for maximization of solar cell efficiency.

I. INTRODUCTION

Transition metal atoms and their silicide precipitates are carrier recombination centers in Si. They decrease the minority carrier lifetimes which in turn lower the solar cell efficiency. In electronic grade Czochralski (CZ) or float zone (FZ) Si, these metals are dissolved and can be gettered rapidly.^{1,2} In low-cost multicrystalline Si, they are present in both dissolved and precipitated form. Gettering using an Al layer provides a means to minimize the impurity content without incurring significant expenses increase in commercial solar cell production using multicrystalline Si. However, gettering of precipitated impurities requires significantly longer time because the precipitates serve as sources which release impurities into the solid solution very slowly during gettering.²⁻⁵ Via modeling, it has been shown that the process time can be greatly reduced by choosing a proper temperature regime.⁶ In order to optimize the process, it is important to know how the impurities remaining in Si affect the performance of solar cells. Since the recombination centers located at different depth have a different influence on the cell performance, it is necessary to know the depth profiles of impurity concentration for accurate analysis. During gettering, indiffusion of Al into Si also occurs, giving rise to a gradient of p-dopant concentration near the back surface in cells with a p-type base which leads to the back surface field (BSF). The BSF provides an additional driving force for transporting electrons to the front surface, improving their collection and hence increasing the efficiency of the cell.⁷ Previous attempts to separate effects of gettering and BSF did not include modeling of the gettering process.⁸ In order to optimize the process of Al gettering and indiffusion to obtain maximum efficiency enhancement due to both gettering and BSF, a model incorporating both of these processes has been developed. The model allows to predict the resulting solar cell efficiency enhancement at a given stage of the process.

II. MODELING

In order to see how gettering and Al indiffusion influence the resulting cell performance, the process model was combined with a solar cell device model which calculates the efficiency of the resulting cell. Both Al concentration and minority carrier recombination rate as functions of depth are used as input data for cell efficiency modeling. The cell efficiency is calculated based on impurity concentration and precipitate size profiles. For dissolved impurity atoms, the measured values of the minority carrier capture cross-section were used.⁹ For precipitates, carrier capture cross-section was calculated as a function of precipitate size, concentration, Schottky barrier height between the precipitate and Si, Si matrix dopant concentration, and carrier generation rate.¹⁰ Depth profiles of impurity concentration and precipitate sizes at any instant during gettering is obtained as described elsewhere.⁶ Al indiffusion depth profiles is obtained as a solution of the diffusion equation. For cell efficiency modeling, we formulated the problem by emphasizing the physical factors involved, instead of using commonly available simulation programs which contain empirical factors with their physical origins not clear. The solar cell is treated as a p-doped base and n-doped emitter with an abrupt p-n junction. The photo-excitation of carriers is assumed to be weak, i.e., 1 sun. To calculate the solar cell efficiency, a computer program has been written based on physical modeling. This program accepts the recombination coefficient values as a function of depth, $r(x)$, which are output of the gettering and precipitate electrical activity models.^{6,10} Minority carrier recombination due to dissolved and precipitated impurity as well as Auger recombination (doping-dependent¹²) were all taken into account. Thus, the recombination coefficient was calculated as a function of doping type and level, precipitate concentration and size, generation rate, and dissolved impurity concentration. Aluminum indiffusion profiles were calculated and used to obtain the values of p-dopant concentration as a function of depth to obtain the BSF intensity, Auger recombination coefficient, and the semiconductor resistivity.

For this study, Fe was used as the sample impurity. Two types of wafers were considered, low quality and high quality. In low quality multicrystalline wafer cases, Si is assumed to be saturated with Fe at 1100 °C. The thermal equilibrium between the solution of Fe in Si and FeSi precipitates is reached at 700 °C with a precipitate density of 10^{10} cm^{-3} . Thus, the solid solution is saturated with Fe at 700°C, and the rest of the Fe is contained in FeSi precipitates. Wafers of the high quality type (e.g. dislocation-free electronic grade Si) are saturated with Fe at 700 °C and contain no precipitates. It is further assumed that in Si there are other Shockley-Reed-Hall recombination centers besides Fe and they are not affected by gettering. They limit the minority carrier diffusion length to 100 μm in low quality wafers and to 1000 μm in high quality wafers. The former is based on the measured values in multicrystalline Si substrates.^{2, 3, 12} The diffusion length limit in high quality Si is chosen to be sufficiently high so as not to affect the performance of solar cells significantly, but at the same time to remain within reasonable limits. In reality, the minority carrier diffusion length in high quality FZ Si is limited by the Auger rather than by the Shockley-Reed-Hall recombination if the material is doped to concentrations typical for a solar cell base. Additional parameters used are: surface recombination velocity at the back side is 10^6 cm/s , surface recombination velocity at the front side is 10^4 cm/s , wafer thickness is 400 μm , depth of the p-n junction is 0.5 μm , junction width is 0 (abrupt), front grid spacing is 4 mm, reflectivity of the back surface is 0.7, cell operation temperature is 300 K. Doping levels were optimized for maximum power output. Note that the optimum doping levels are different for Al-treated and untreated cells. The temperature of the gettering process modeled is 1000 °C. Various

deviations from the parameters listed above were considered: excessive and insufficient doping of the p-base, different wafer thickness, and different processing temperature. In order to find out whether the efficiency change should be attributed to the gettering or to the BSF, the cell device modeling was carried out in three ways: either only Al indiffusion occurs, or only gettering occurs, or both.

IV. RESULTS AND DISCUSSION

Results of the modeling are shown in Figs. 1 and 2. Gettering provides a significant efficiency increase, more than 0.3% absolute for the cells built on high quality substrates and more than 2.5% absolute for the cells built on low quality substrates. The magnitude of the effect strongly depends on the background recombination constant, which is due to recombination centers that cannot be gettered, e.g., that due to the presence of Ti.

In experiments^{1, 2, 13} it was found that gettering can significantly increase minority carrier lifetime in high quality substrates, but not so in low quality substrates. This is apparently because gettering of precipitated impurities requires long gettering time and high temperature. In Fig. 2 the solar cell efficiency is shown as a function of process duration at various temperatures for low quality substrates. The required process duration is much longer at lower temperatures. The process can be completed in about 20 minutes at 1100 °C. However, at 900 °C, it takes about 10 hours before any efficiency improvement can be noticed. Moreover, if slowly diffusing impurities, such as Cr, are present in Si, the process will become even slower. Therefore, a high temperature process is needed for effectively getter precipitated impurities from silicon. On the other hand, impurities such as Cu and Ni have relatively high solubility and diffusivity in Si. To remove these metals from Si efficiently, low temperature gettering is necessary. At lower temperature their segregation coefficient between Al and Si is higher, which allows to achieve lower residual concentration of these impurities in Si. Thus, only a process with the temperature ramped down from a high to a low value can ensure successful gettering.

As the calculations show, Al indiffusion provides no efficiency gain in the case of low quality substrate. In the case of high quality 400 μm thick substrate and optimum base doping, the efficiency gain due to Al indiffusion is only 0.005% absolute. However, the BSF can partially compensate for an insufficient doping of the base. In the case considered, with a fixed p-doping level, which is 3.0 times lower than the optimum, the BSF increased the efficiency by 0.047% absolute, but still well below the level achieved with the optimum base doping. On the other hand, if the base doping is excessive (in the case considered, 3.0 times higher than the optimum), the BSF provides no positive effect. Aluminum indiffusion provides an increased efficiency gain, 0.03% absolute, in high quality substrates if gettering occurs simultaneously, as compared to 0.005% without gettering. Nevertheless, in either case the improvement is almost negligible.

These observations can be understood by considering mechanisms limiting solar cell efficiency. Whereas gettering increases carrier diffusion length in the base bulk, the BSF reduces effective back surface recombination velocity and provides an additional driving force for the diffusion of minority carriers from the vicinity of the back surface towards the p-n junction. If the base thickness is significantly smaller than the minority carrier diffusion length, minority carriers generated near the back surface are likely to reach the p-n junction without recombining in the bulk. Then a reduction of the back surface recombination will result in an increase of the number of carriers collected at the p-n junction and higher cell efficiency. At the same time, any

further reduction of the bulk recombination will have little effect on the cell efficiency. On the other hand, if the base thickness is significantly larger than the minority carrier diffusion length, the recombination of minority carriers occurs mostly in the bulk, and only a small fraction of minority carriers reaches the p-n junction from the vicinity of the back surface. In this situation, a decrease of the back surface recombination velocity affects the collection of minority carriers at the p-n junction very little, and the BSF benefit is small. The role of gettering, on the contrary, is significant, since any increase of the minority carrier diffusion length in the base bulk directly affects the collection of carriers at the p-n junction. Thus, the larger is the cell thickness, the greater is the role of gettering and the smaller is the role of BSF in improving the cell efficiency. These conclusions are illustrated in Figures 3 and 4, where the calculated efficiency gain after 10^4 s of processing is plotted versus thickness for high and low quality Si cells, respectively. The curves are plotted for hypothetical cases wherein only gettering or only Al indiffusion takes place, as well as for the realistic case of simultaneous gettering and Al indiffusion. The efficiency gain in the last case is greater than the arithmetic sum of gains in the first two cases, i.e. the effects are synergetic. This can be explained by the fact that the carriers moving towards the p-n junction from the vicinity of the back surface are subject to consecutive surface and bulk recombination. The probability that they do not recombine and reach the p-n junction is a product of the probabilities that they do not recombine at the surface and in the bulk, i.e. they are multiplicative rather than additive.

In Figure 5, the cell efficiencies before and after Al treatment are plotted versus wafer thickness. It can be seen that not only does the Al treatment increase the efficiency of cells of a given thickness, but also shifts the optimum thickness towards larger values. Thus, the Al treatment allows to use thicker multicrystalline Si wafers and decrease breakage loss resulting from their brittleness.

V. CONCLUSIONS

In conclusion, we have developed a combined model of Al impurity gettering, back surface field formation, and solar cell operation. The modeling shows that gettering can significantly increase the efficiency of solar cells built on both high and low quality substrates. Gettering of impurities from low quality Si requires long process duration and/or high temperature. The Al indiffusion induced back surface field, which is formed simultaneously with gettering, also provides some efficiency improvement, but it becomes significant only in cells built on high quality substrates thinner than $200\ \mu\text{m}$. However, Al indiffusion can partially compensate for a lower than optimum doping level of the cell p-base.

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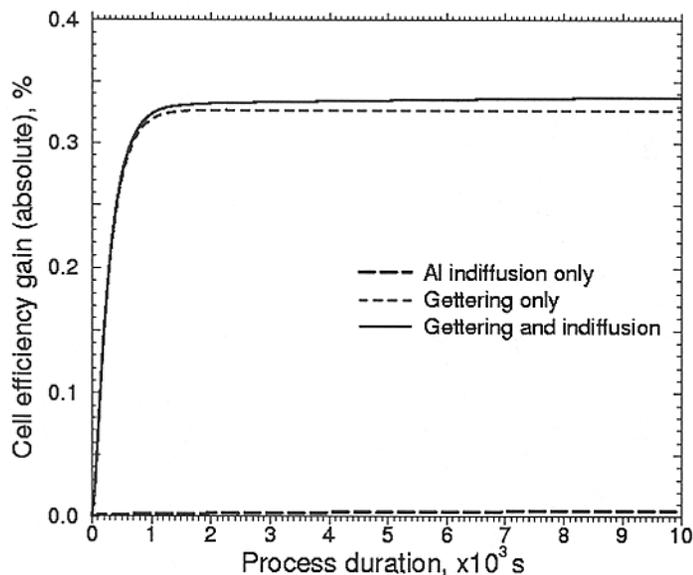


Fig. 1. Calculated dependence of high quality Si solar cell efficiency on the duration of Al getting and indiffusion. Process temperature 1000°C. Wafer thickness 400 μm . Doping levels are optimized for the untreated cell.

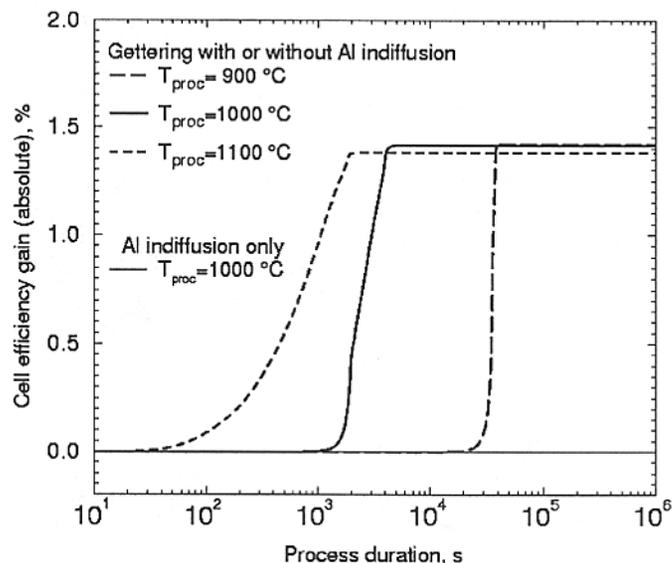


Fig. 2. Calculated dependence of low quality Si solar cell efficiency on the duration of Al getting and indiffusion at various processing temperatures. Wafer thickness 400 μm . Doping levels are optimized for the untreated cell. Curves for getting with Al indiffusion are not shown. They are undistinguishable from respective curves for getting without Al indiffusion. Curves for Al indiffusion at 900 and 1100°C are undistinguishable from the curve for Al indiffusion at 1000°C.

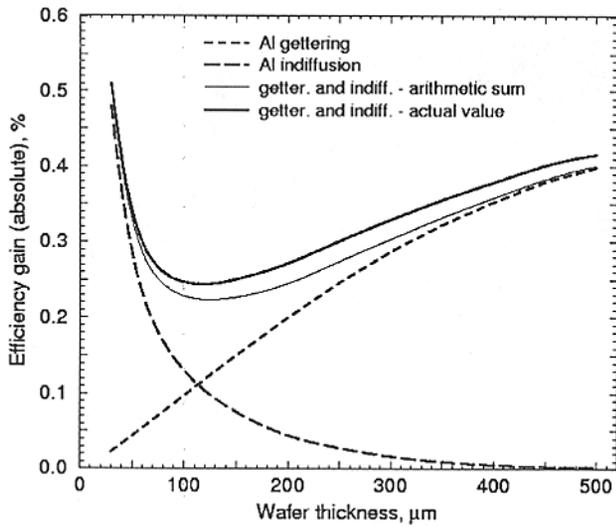


Fig. 3. Calculated high quality Si solar cell efficiency gain due to Al gettering and indiffusion as a function of wafer thickness. Process duration 10^4 s, process temperature 1000°C . Doping levels are individually optimized for each wafer thickness value and each set of process conditions.

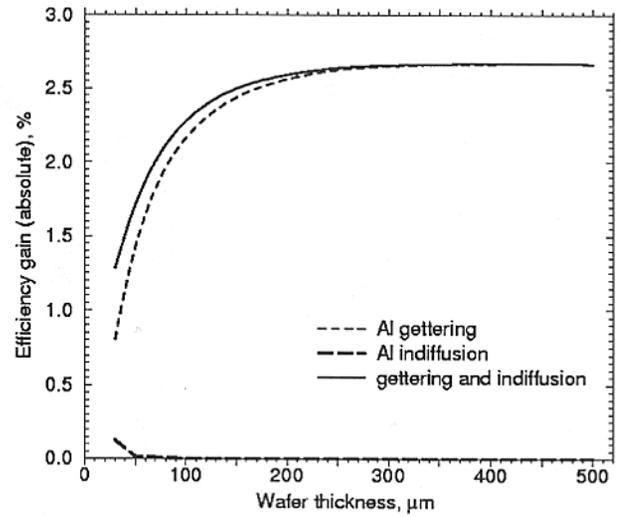


Fig. 4. Calculated low quality Si solar cell efficiency gain due to Al gettering and indiffusion as a function of wafer thickness. Process duration 10^4 s, process temperature 1000°C . Doping levels are individually optimized for each wafer thickness value and each set of process conditions.

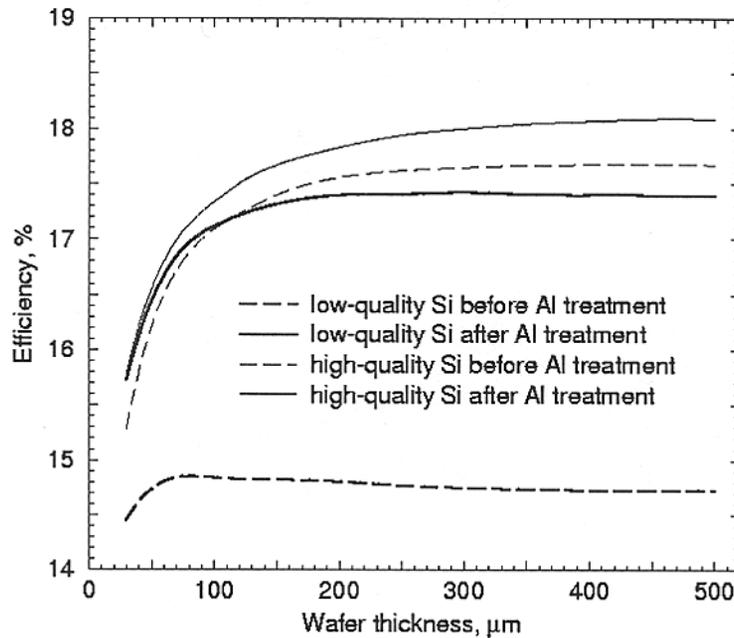


Fig. 5. Calculated Si solar cell efficiency as a function of wafer thickness before and after Al treatment for high and low quality Si. Al treatment includes gettering and indiffusion for 10^4 s at 1000°C . Doping levels are individually optimized for each wafer thickness value.

Boron and Phosphorus Dopant Diffusion in Crystalline Si by Rapid Thermal Activation

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Crystalline Si was doped with high concentrations of B and P near the surface by low energy ion implantation and electrically activated by rapid thermal annealing (RTA) and the special case of spike annealing. Diffusion depths were determined by secondary ion mass spectroscopy (SIMS). Electrical activation was characterized by sheet resistance, Hall coefficient, and reverse bias diode leakage. While both species show transient enhanced diffusion (TED), electrical activation strongly increases with dose for P implants and comparatively weakly for B implants.

I. Introduction

Low energy ion implantation and RTA is the current method for forming junctions in the source and drain regions of complementary metal-oxide semiconductor (CMOS) transistor circuits. Diffusion and electrical activation of implanted B and P dopants in crystalline Si are examined for possible relevance in solar cell applications, where alternatives to ion implantation may be considered. During annealing, dopants experience an enhanced diffusion if any excess Si interstitials exist in the silicon crystal. For implanted dopant species excess Si interstitials evolve from the residual implant damage until the damage is annealed out. The resulting enhanced diffusion is thus transient. In the case of boron, excess interstitials can also be generated by formation of a boron silicide phase if the surface boron concentration is high enough [1]. The phenomenon is referred to as boron enhanced diffusion (BED) and occurs for both ion-implanted B and for a B film deposited on the surface. Variations of the latter doping method could be integrated into the fabrication of back surface field contacts in solar cells. Although enhanced diffusion of any kind is unfavorable for shallow junction formation in advanced transistor designs, the enhanced diffu-

sion could be beneficial for junction formation in solar cell devices. However, solar cell fabrication using this technique would need an anneal at a temperature in the range of 900 to 1100 °C. High temperature annealing may also be advantageous for increasing the solid solubility of the dopants.

II. Boron Implants

Figure 1 shows the B concentration profiles determined by SIMS after annealing ^{11}B implants at four energies from 500 eV to 5 keV. The RTA step used incandescent lamps for heating. The SIMS profiles are characterized by peaks within 10 nm of the surface and diffusive tails. Most of the boron in the peaks near the surface is electrically inactive and believed to be in the form of clustered B or a silicon boride phase which can form if the peak concentration exceeds a few atomic percent as is the case for 0.5 keV B. The B diffusivity estimated from the diffusion tails is greater than the equilibrium diffusivity of B at the anneal temperature. This was examined quantitatively by Agarwal et al. from the diffusion broadening of B marker layers grown in Si samples by molecular beam epitaxy [1]. Figure 2 shows the diffusivity enhancement factors for various B implant energies for RTA at 1050 °C and 10 s. The trend towards enhanced diffusion even at zero implant energy and range was verified by depositing a B film on the surface. The remaining enhanced diffusion in the absence of implant damage is BED caused by excess Si interstitials associated with high concentrations of B in Si.

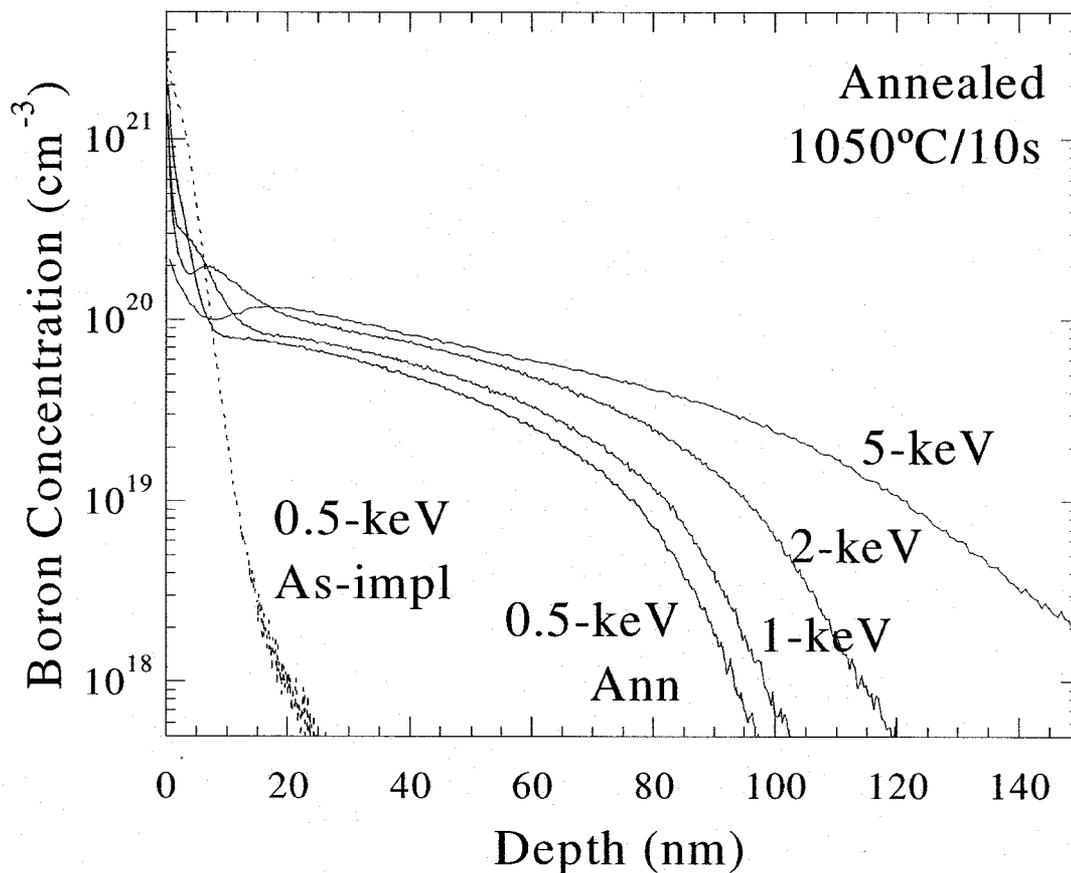


FIG. 1. Boron concentration vs depth in crystalline Si for ^{11}B implants of 10^{15} cm^{-3} dose at energies of 0.5, 1, 2, and 5 keV and annealed at 1050 °C for 10 s. The as-implanted profile is shown for the 0.5 keV implant.

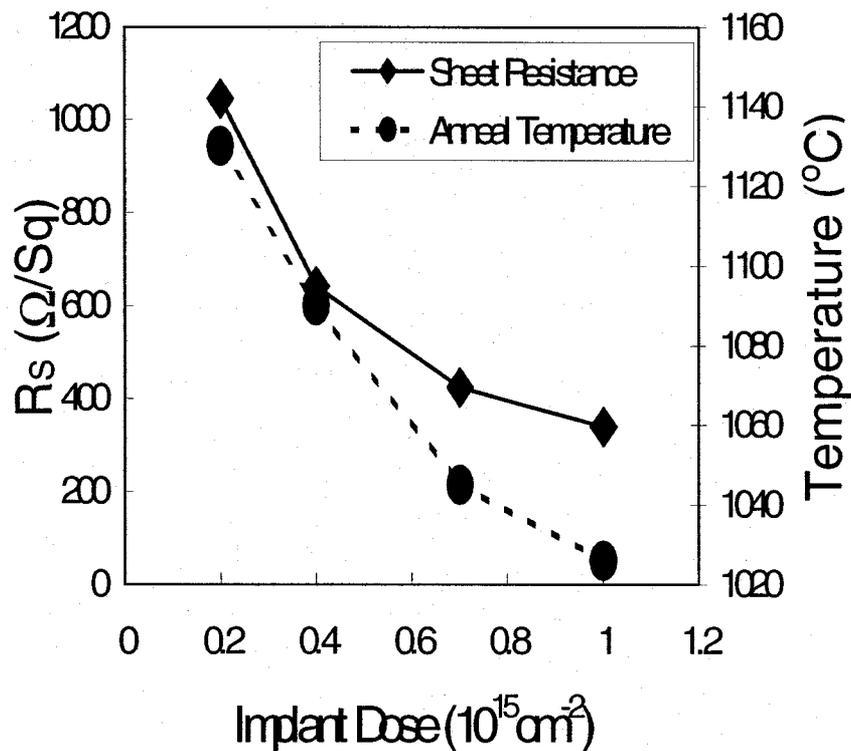


FIG. 2. Boron diffusivity enhancement factor for 10^{15} cm^{-3} ^{11}B implants as a function of implant range for energies from 0.5 to 5 keV. The enhancement was determined from diffusion broadening of a grown-in B marker located at a depth of 150 nm (Ref 1).

Given that the diffusion of implanted B dopants is not in thermal equilibrium, it is nonetheless instructive to consider a phenomenological mean diffusivity estimated from the diffusion depth and the anneal time. This was examined in an experiment where the diffusion temperatures and times were mutually varied under the constraint that a constant portion of B becomes activated [2]. The experiment used a 750 eV, 10^{15} cm^{-2} B implant and anneal times that were decreased as the anneal temperatures were increased. Figure 3 shows the results for the mean diffusivity and the associated anneal times on Arrhenius scales. The activated fraction is 53%. The activation times are the effective times at temperature and include corrections for the temperature transitions during heating ($\sim 150 \text{ }^{\circ}\text{C/s}$) and cooling ($\sim 80 \text{ }^{\circ}\text{C/s}$). What is notable in these results is the 1 eV difference in thermal activation energies, E_A , wherein the diffusivity shows a lower E_A than the activation time. Thus, increasing the temperature and compensating by reducing the anneal time favors electrical activation over diffusion, and vice versa.

Anneals with the shortest time at temperature, denoted “spike anneals”, are expected to minimize the diffusion associated with electrically activating a given portion of the dopant [3]. The results of a study of the temperature and dose dependence for spike anneals of a 500 eV B implant are shown in Fig. 4. Here, an electric arc lamp was used to produce spike anneals with 400 $^{\circ}\text{C/s}$ heating rates. The general trend of the data is that the activated fraction of the B increases monotonically with temperature and remains relatively insensitive to the implant dose. Although BED was found to increase with implant dose in a previous study [1], the variability in diffusivity appears to have minor influence on the electrically active fraction.

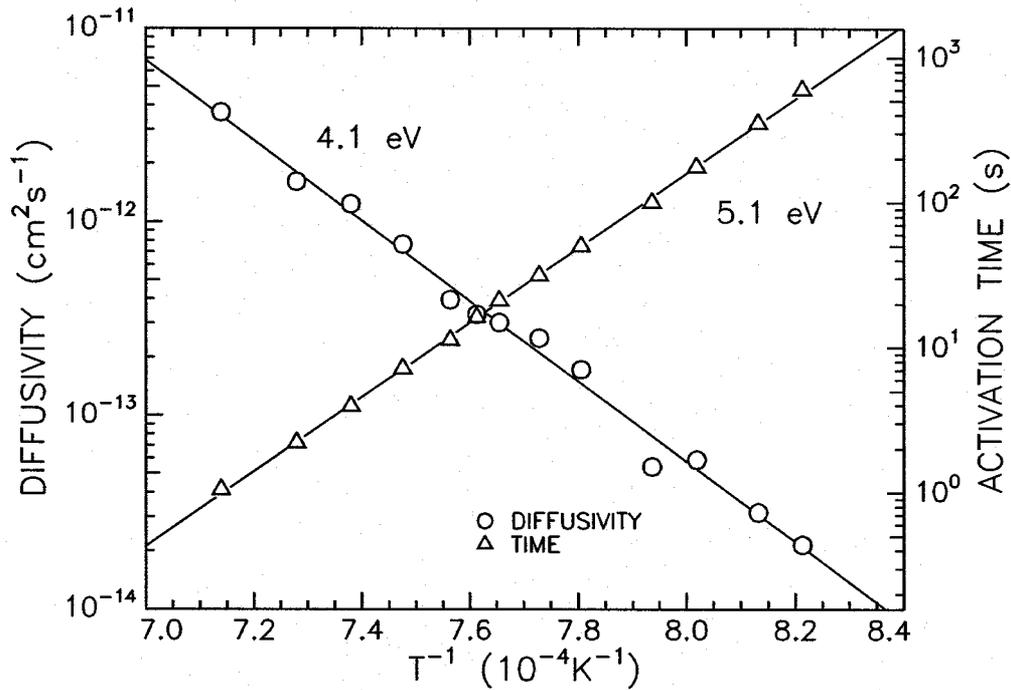


FIG. 3. Arrhenius plots of mean B diffusivity and time to activate a fixed sheet carrier density of $5.3 \times 10^{14} \text{ cm}^{-2}$, for a 750 eV B implant at 10^{15} cm^{-2} dose. Dashed lines are fits with the activation energies shown.

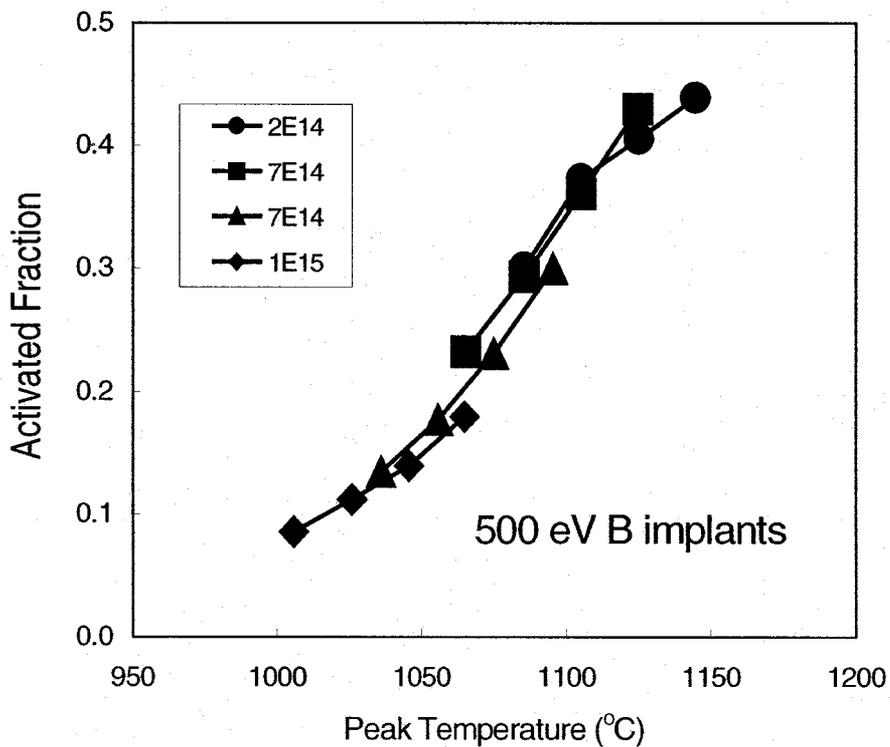


FIG. 4. Activated fraction (Hall carrier density / implant dose) vs. arc-lamp spike anneal temperature for 500 eV B implants at four doses indicated (cm^{-2} units).

Activation of implants can leave residual lattice defects near the range of the implanted ions. For anneals generating sufficient dopant diffusion, the defects should be largely contained within high carrier concentration region, and thus have minimal influence on junction properties. This was examined for the above anneals by diode leakage currents measured at a reverse bias of $-1V$. The substrate is n type with a doping level in the 10^{14} cm^{-3} range. The measurements used wet chemically etched diode mesas, approximately 1 mm in diameter. Up to four diodes were measured for each implant/anneal combination and data for statistical outliers were discarded. Figure 5 shows that there is a trend for the junction leakage to decrease with increasing anneal temperature. Higher leakage at some of the lower spike anneal temperatures is possibly related to defects in the junctions.

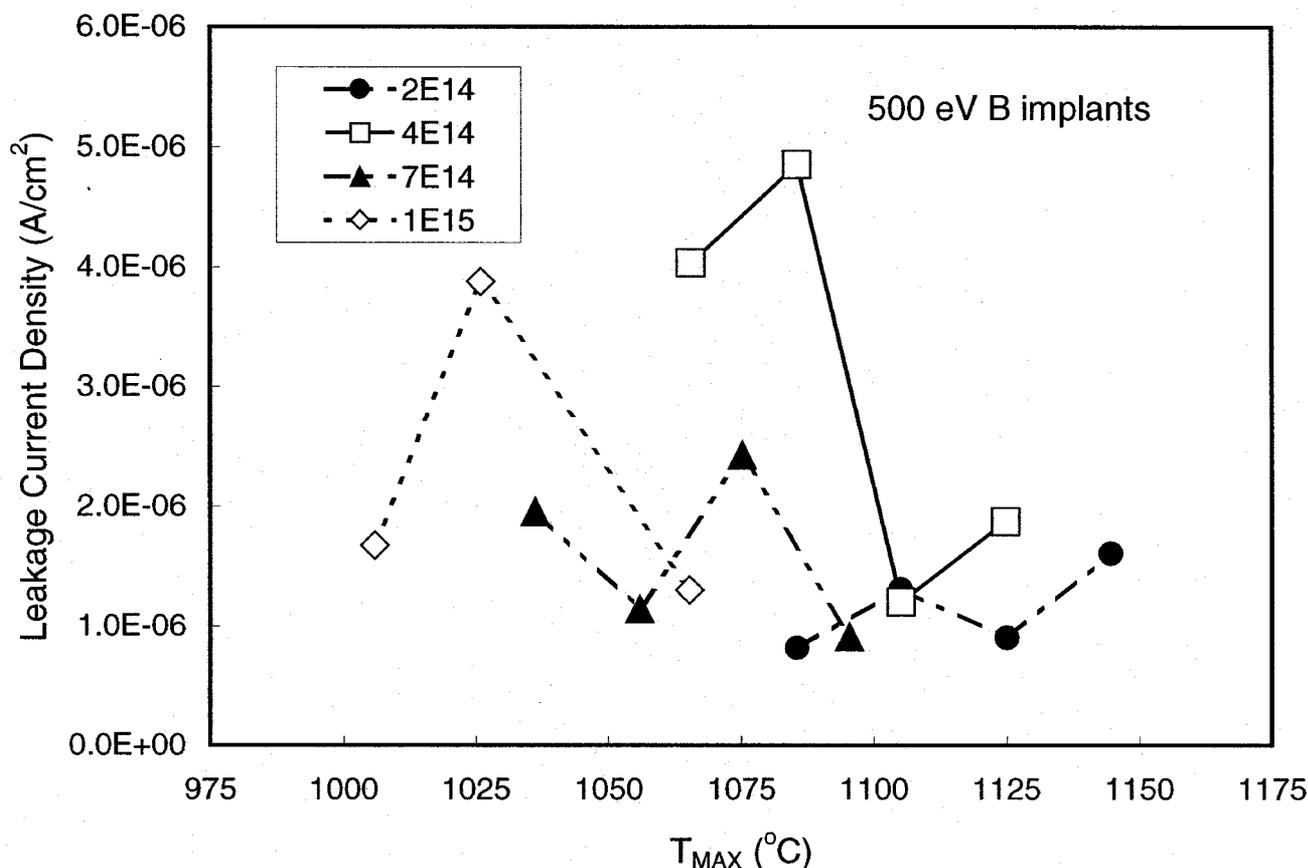


FIG. 5. Reverse bias diode leakage current density (at $-1V$ bias) vs. arc-lamp spike anneal temperature for 500 eV B implants at four doses indicated (cm^{-2} units).

III. Phosphorus Implants

The experimental picture for low energy P implants is not as well studied as the case for B. For example, it is not known if there is an analog to BED, even though excess Si interstitials contribute to enhanced diffusion of P. Figure 6 shows that the behavior of P implants with spike annealing is quite different from the case of B implants. The data for the activated fraction at various doses do not overlap as they do for the B implants, and thus exhibit a strong dependence

on implant dose. Thus the activation of P varies more rapidly than linearly with implant dose. The diffusion associated with electrical activation of approximately 25% of the P dopant was examined by SIMS measurements and the data are shown in Fig 7. The diffusion depths are fairly insensitive to dose. Using the Bell Labs / Agere Systems process simulator PROPHET to emulate coupled diffusion between P and Si interstitials, we estimate that there is an excess Si interstitial population of 6 to 10 % of the implanted P dose.

The variation of sheet resistance and temperature with implant dose, for anneals that activate ~25% of the P, are shown in Fig. 8. Transient enhanced diffusion permits a rapid reduction in sheet resistance while simultaneously reducing the anneal temperature as the P dose is increased. Results for the reverse bias diode leakage current densities plotted in Fig. 9 systematically show maxima near 25% activation (compare Fig. 6). The leakage maxima indicate the presence of lattice defects, which may need to be taken into account in modeling TED of P.

IV. Conclusions

Transient enhanced diffusion and dopant activation effects were examined for low energy B and P implants. For spike annealing, the activated fraction depends mainly on temperature for B implants, but for P implants it is also strongly enhanced with increasing P dose.

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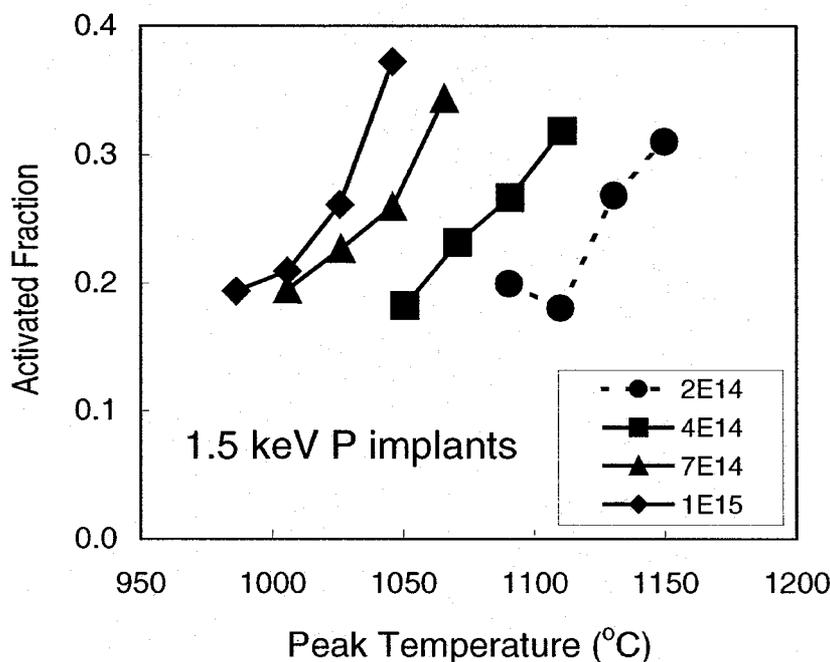


FIG. 6. Activated fraction (Hall carrier density / implant dose) vs. arc-lamp spike anneal temperature for 1.5 keV P implants at four doses indicated (cm^{-2} units).

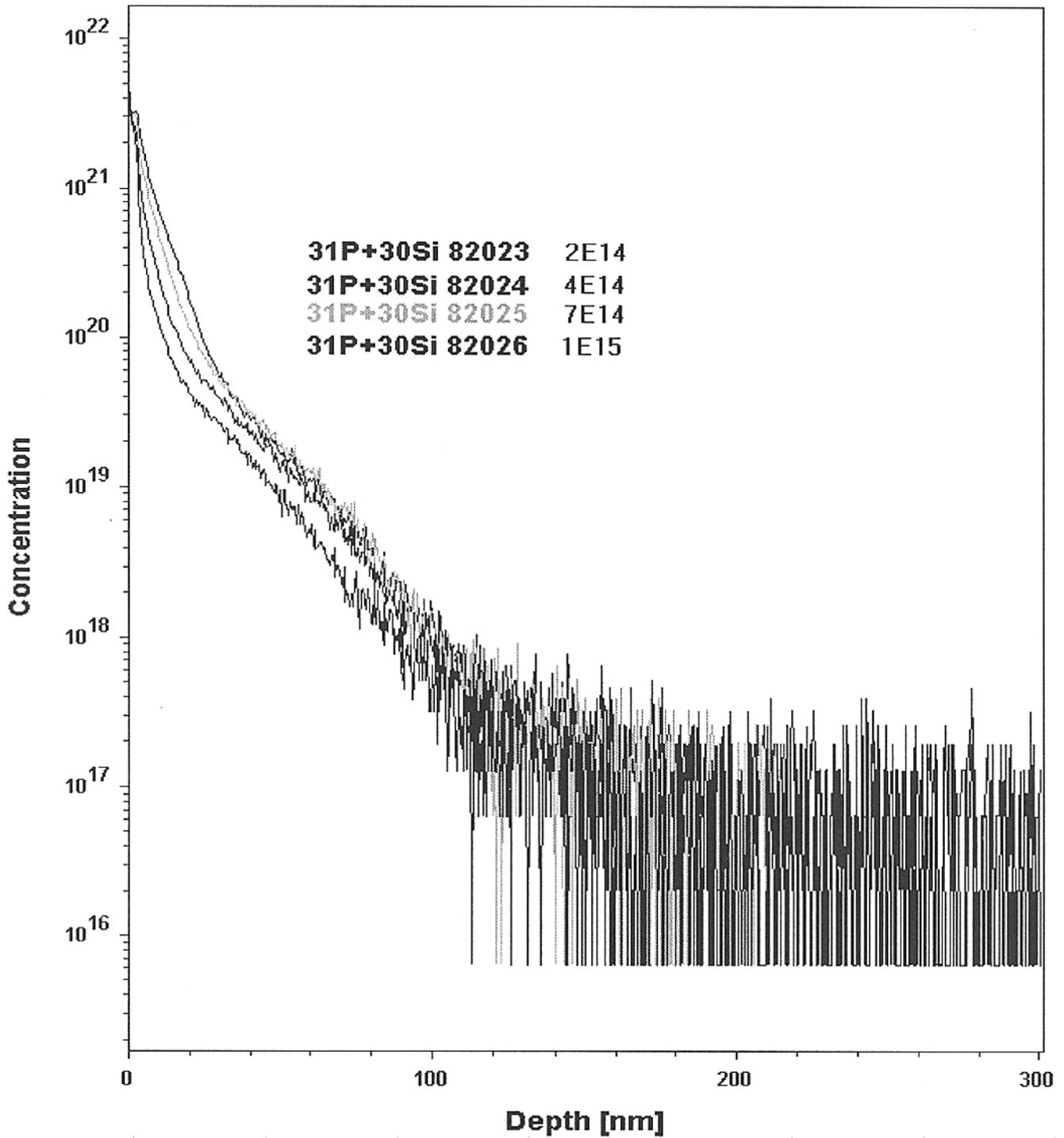


FIG. 7. SIMS measurements of ^{31}P (includes ^{30}Si) profiles for 1.5 keV P implants after spike annealing. The doses are 0.2 , 0.4 , 0.7 , and $1.0 \times 10^{15} \text{ cm}^{-3}$. The respective anneal temperatures are 1131 , 1091 , 1046 , and $1026 \text{ }^\circ\text{C}$, and correspond electrical to activation of $\sim 25\%$ of the P. To aid in distinguishing traces, note that concentration near the surface increases monotonically with increasing dose.

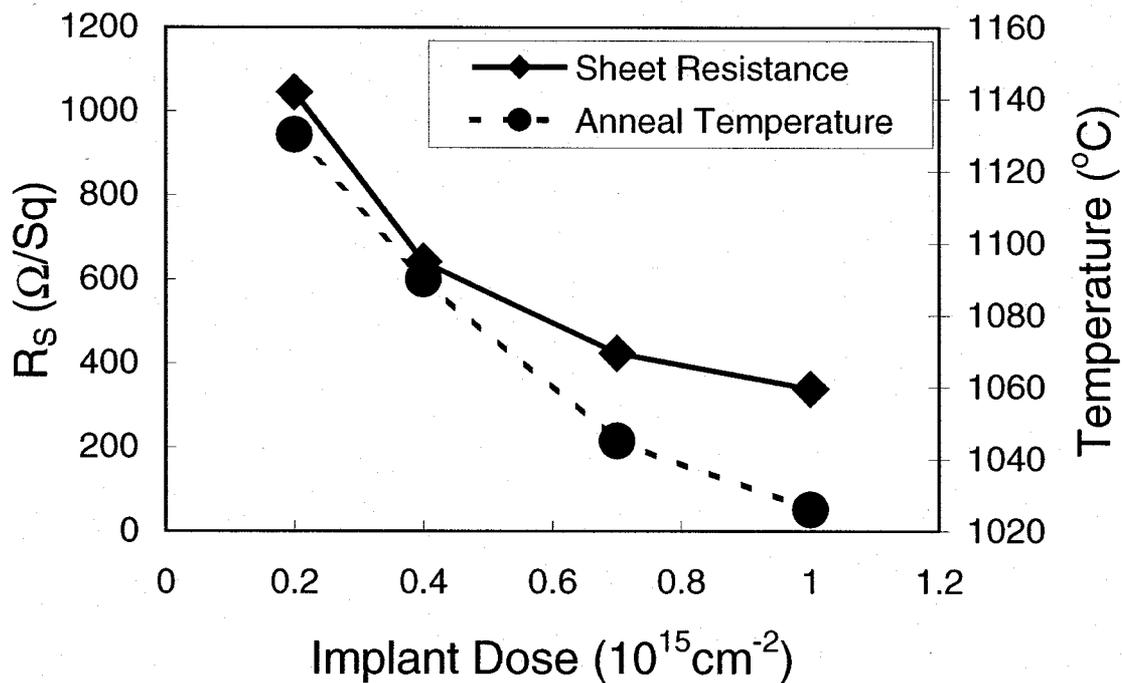


FIG. 8. Variation of sheet resistance and anneal temperature with P dose for arc-lamp spike anneals that activate $\sim 25\%$ of the dose for 1.5 keV P implants.

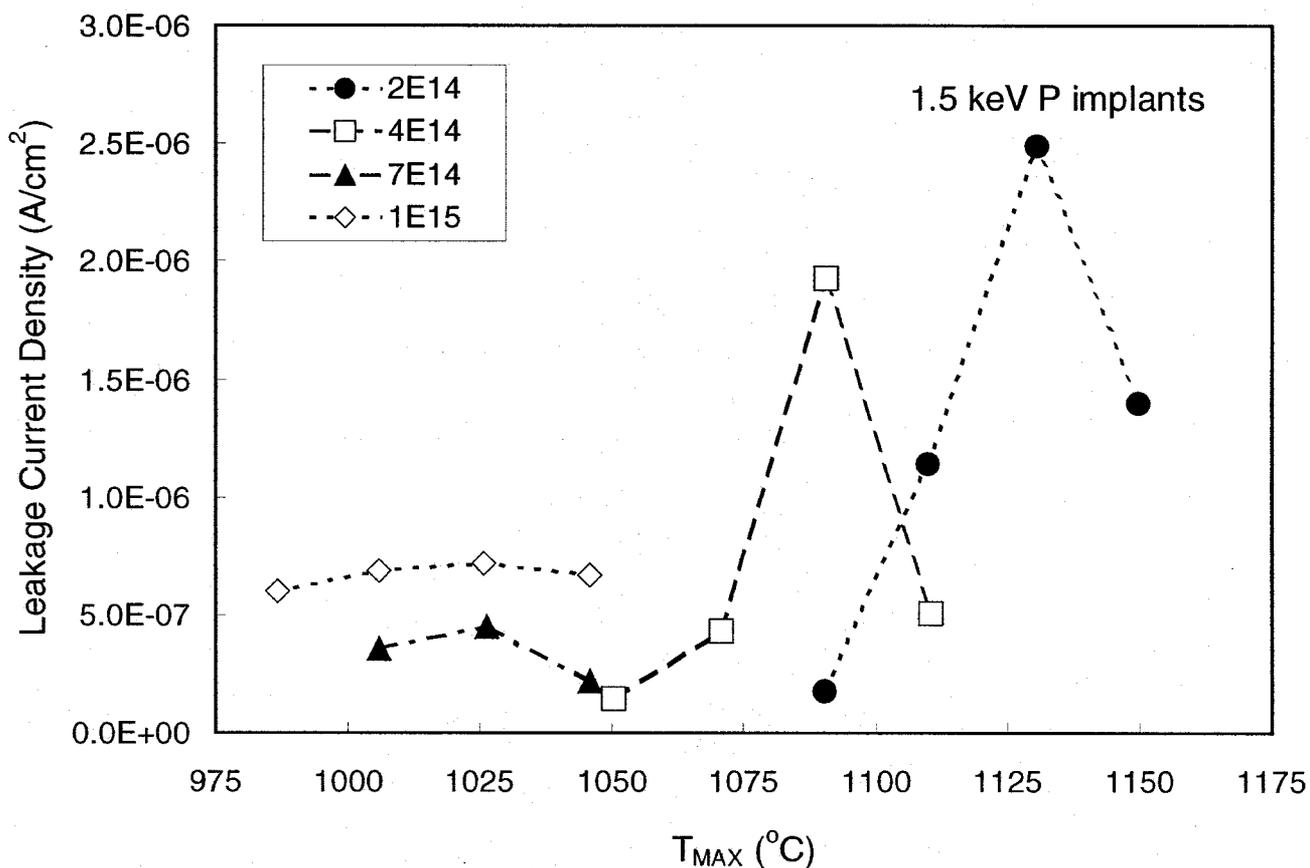


FIG. 9. Reverse bias diode leakage current density (at +1V bias) vs. arc-lamp spike anneal temperature for 1.5 keV P implants at four doses indicated (cm^{-2} units).

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INTRODUCTION

Hydrogen diffusion for impurity defect passivation has been traditionally done at low temperatures, in the range of 250 – 400 °C, using plasma or low-energy ion implantation. There is now considerable amount of information on the diffusion properties of hydrogen in silicon at such low temperatures. One of the interesting observations is that the low-temperature diffusivity, determined from the experimental diffusion profiles, is significantly lower than the values extrapolated from high-temperature data published by Van Weirengen and Warmohltz [1]. Figure 1 shows a compilation of diffusivity values published by different researchers [2]. The lower experimental values of diffusivity are attributed to a host of mechanisms that include field effects [3,4], H₂ formation [5], generation of H-related defects [6,7] and other trapping processes. To date trapping effects by the dopants present in Si wafer have been generally accepted [5, 8]. Many authors have attempted to quantify trapping effects. Early on, Corbett [9] proposed that trapping was also responsible for generation of kinks in the diffusion profile. Since then, there has been some quantitative modeling work done to estimate the influence of traps on the H diffusion [4,5,8,10]. Much of the previous work is based on bulk traps. Here we present results of our calculations that include several H-trapping mechanisms. Inclusion of these mechanisms leads to much better agreement between the theoretical and experimental H diffusion profiles.

D_H in Si in the Literature

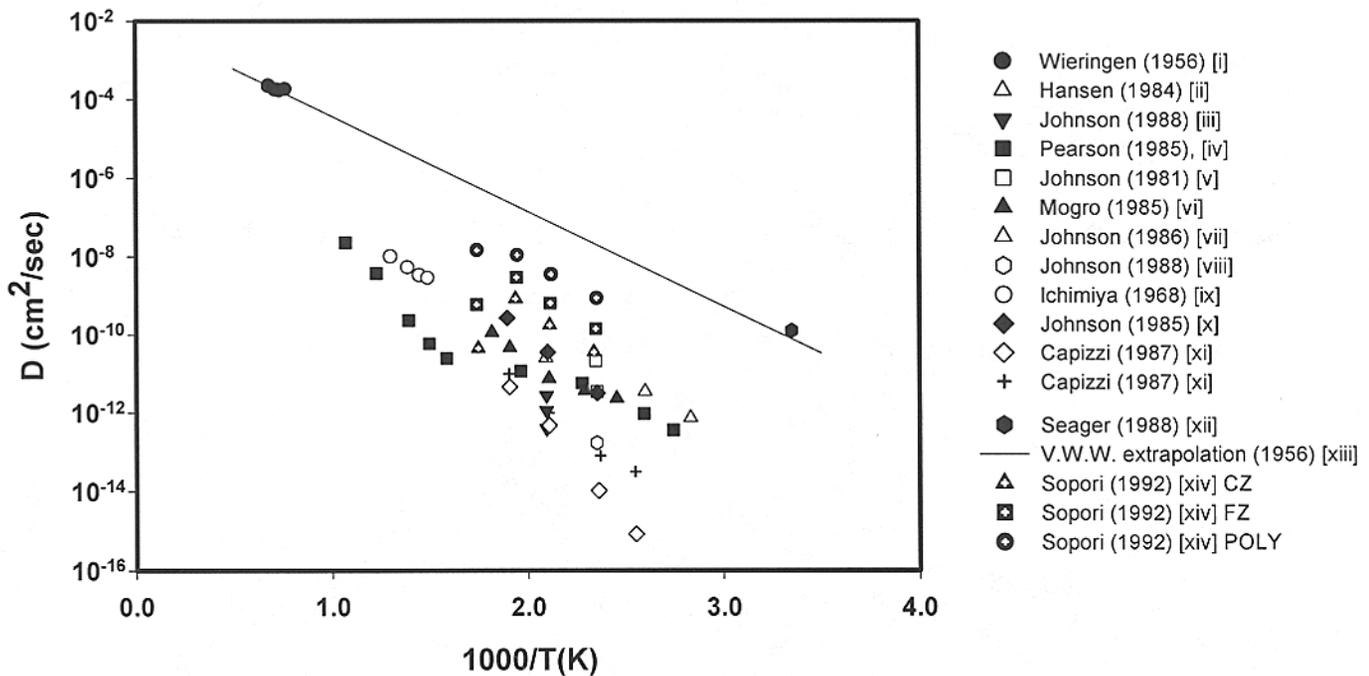


Figure 1. A summary of diffusivity values in the literature for hydrogen in silicon [2].

TRAPPING OF HYDROGEN IN SI

During a hydrogenation process, H was believed to diffuse into Si primarily as a monatomic species. However, H can interact with various impurities and defects in Si to form a variety of complexes [11,12,13]. Some of these complexes may be mobile and can indeed transport hydrogen within the wafer. For example, it is believed that hydrogen-vacancy may exhibit this behavior [14,15]. Other complexes may remain immobile under the processing conditions, leading to stagnation of hydrogen. A typical example is interaction of H with dopants. If hydrogenation is done at low temperatures, H can form B-H or P-H complex that can trap H [16,17]. The dissociation probability of these complexes is small at temperatures below 200 °C. Other impurities can also trap H.

The photovoltaic silicon (PV-Si), which has a preponderance of impurities and defects, is an excellent candidate to exhibit trapping effects. Unfortunately, we still do not have a good knowledge of the nature of all the defects in such materials. It is, however, known that there may be supersaturation of point defects. Presence of impurities like oxygen, carbon, and nitrogen can strongly influence the nature of point defects [15]. Likewise, extended defects (that are formed at high temperatures during cool-down of a Si crystal) can also compete as sinks for point defects. Extended defects can also become traps for H. Their trapping activity may depend on the history of the wafer. As a result, silicon substrates from different vendors can exhibit different behavior of H diffusion.

In general, trapped H can also be detrapped. The probability of detrapping is strongly temperature-dependant. During a hydrogenation process, once the H detrapped from an immobile trap it can diffuse before it is trapped again. It is interesting to relate this trapping process to enhanced solubility of H in Si. It is known that the solubility of H in a highly pure Si crystal should be extremely low. However, measured H concentrations in plasma treated wafers can reach $10^{21}/\text{cm}^3$. This mechanism is a manifestation of H trapping.

In addition to the bulk traps in a wafer, a hydrogenation process can introduce its own traps. For example, ion implantation and plasma processing can introduce surface damage (yet another form of trap) that fosters a very interesting behavior of H. It can trap atomic H, it can dissociate molecular hydrogen, and it can serve as a sink/source of H. Process-induced traps can play an important role on the diffusion behavior of H. One of these important features is that it can influence the flux of H or the surface concentration as discussed later in this paper.

Model for H diffusion

We have extended the trapping model, developed previously by a number of authors, to include process-induced trapping. As expected, the nature and distribution of process induced traps is a strong function of hydrogenation process itself and is, in general, time dependant. In this paper we will use this model to primarily illustrate effects of including various trapping processes on the profile of H.

Mathematically, we can include trapping in the diffusion equations and write it as:

$$\frac{\partial[H_{untrapped}]}{\partial t} = D_H \frac{\partial^2[H_{untrapped}]}{\partial x^2} - \frac{\partial[H_{trapped}]}{\partial t}$$

$$\frac{\partial[H_{trapped}]}{\partial t} = k[H_{untrapped}][T_{unoccupied}] - k'[H_{trapped}]$$

We can impose the following conditions describing interaction of H and traps:

$$[H_{tot}] = [H_{untrapped}] + [H_{trapped}]$$

$$[T_{unoccupied}] + [H_{trapped}] = [T_{tot}]$$

where,

$[H_{untrapped}]$ = Concentration of mobile H

$[H_{trapped}]$ = Concentration of trapped H

$[H_{tot}]$ = Total H concentration.

$[T_{tot}]$ = Total trap density

Here k' is the dissociation frequency and k is the association rate. In our calculations, we will assume a reasonable value of dissociation frequency (see results and discussion section). The association rate can be expressed in terms of the effective capture cross section (radius), R_c , as :
 $k = 4\pi R_c D_H$.

These equations need to be solved under boundary conditions imposed by the hydrogenation process. The boundary conditions (B.C.) used for the simulation are depicted as follows:

$$[H_{untrapped}] \Big|_{x=0} = C_s \quad \text{for a constant surface concentration, } C_s, \text{ of mobile H in plasma process.}$$

$$-D_H \frac{\partial[H_{untrapped}]}{\partial x} \Big|_{x=0} = J_s \quad \text{for a constant flux of mobile H for implantation process.}$$

Usually, the sample is thicker than the penetration depth of H. The following B.C. at $x = x_c$ was adopted, where x_c is a cutoff depth that is greater than the penetration depth of the H diffusion.

$$\frac{\partial[H_{untrapped}]}{\partial x} \Big|_{x=x_c} = 0$$

In the present paper, we will assume traps to be immobile, and apply this model to illustrate how the diffusion profile can change for different trapping mechanisms. It is instructive to start with typical experimental diffusion profiles and examine how they can be fitted by including different mechanisms. Figure 2 shows deuterium profiles (dotted data) of plasma-processed, n-type, FZ silicon wafers of different dopant concentrations [18]. Deuteration was done at 200 °C. The dopant material is identified in the figure.

We first try to fit the data by simply using a *erfc*. (no trapping) assuming a surface concentration of H that will give the best fit. Figure 2 shows the results of our best fits. The best-fit parameters are shown in the figure for all cases. It may be noticed that we have to assume very high surface concentration and a very low diffusivity to fit the data.

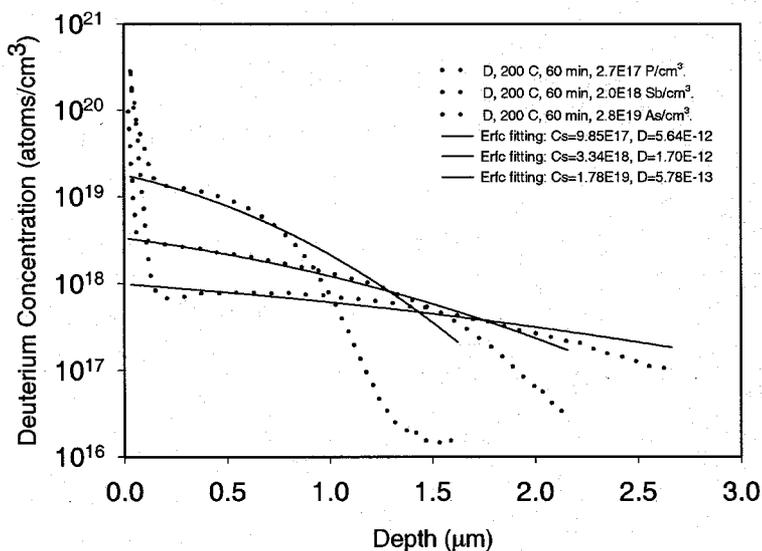


Figure 2. Experimental deuterium profiles (dotted lines) of a plasma-deuterated, n-type Si, at 200 °C, fitted with erfc.

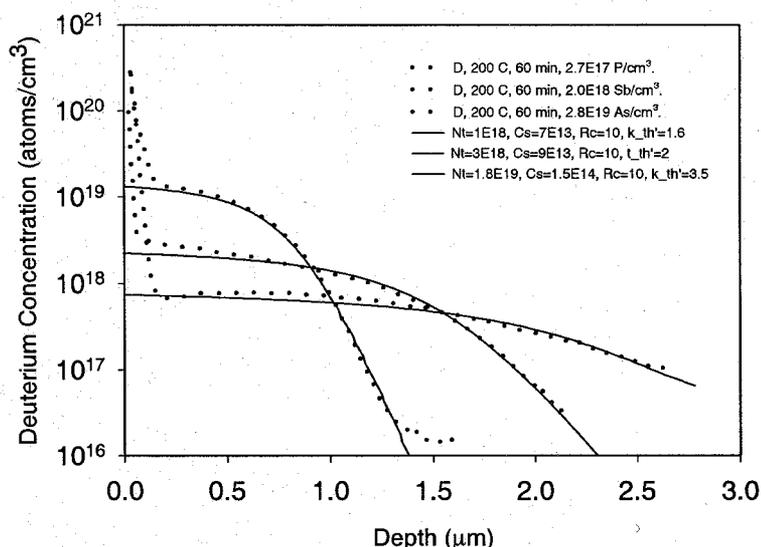


Figure 3. Experimental deuterium profiles (dotted lines) of a plasma-deuterated, n-type Si, at 200 °C, fitted with current model. $D = 5.27E-8 \text{ cm}^2\text{s}^{-1}$

Next we try to fit the same data, but now we incorporate a uniform bulk trap density. Figure 3 shows the profile for best-fit to the data (solid lines). The corresponding parameters (Rc , k' , and Cs) for the best fit are shown in the figure. Here we see that by introducing the trap densities between $10^{13} - 10^{14} \text{ cm}^{-3}$ we get excellent fit to the experimental profile away from the surface. This clearly demonstrates that presence of bulk traps can lower the effective diffusivity of H (or D). It may also be noted that bulk trap alone cannot generate a fit to the near-surface profile of deuterium.

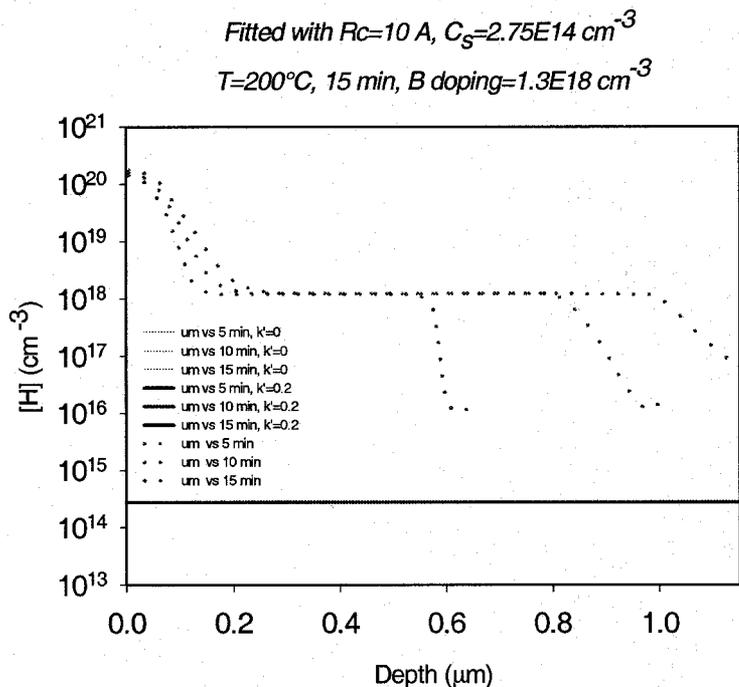


Figure 4. Experimental data of ref. [19] (dotted lines) and erfc. diffusion profile.

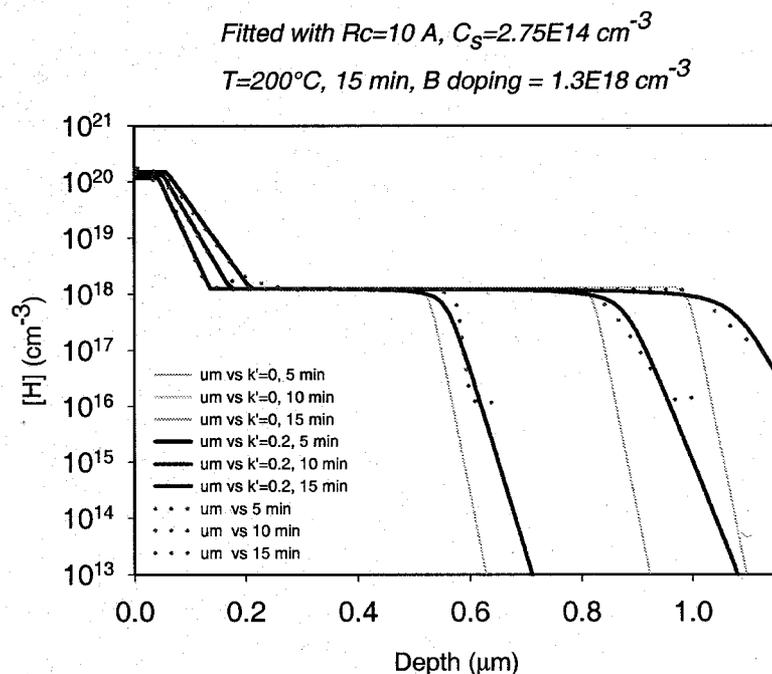


Figure 5. Experimental data of ref. [19] (dotted lines) and fitted results

To demonstrate the influence of process-induced traps, we use the experimental data from reference [19]. This data was also used by Kalejs et.al to examine the influence of bulk traps [8]. Figure 4 shows the experimental deuterium profiles [19] of a B-doped ($1.3E18 \text{ cm}^{-3}$) sample for plasma-processed at 200 °C for three different times (5, 10, and 15 minutes). As in the previous example, we first consider a case of zero bulk trap density. The calculated diffusion profile is shown by the solid line (three overlapping lines), all corresponding to very fast diffusion. Next, we include a uniform bulk trap density and process induced traps. For the plasma processing the form of process-induced trap distribution is expected to be exponential with a time-independent surface concentration. The total trap density has the following time dependence:

$$[T_{\text{tot}}] = T_0 \exp\left[-\frac{x}{a + bt}\right] + T_b$$

where the first time-dependent term is due to process damage and T_b is a constant bulk trap level. The best fits are obtained with $T_0 = 10^{21} \text{ cm}^{-3}$, $a = 0.1 \text{ }\mu\text{m}$, $b = 0.108 \text{ }\mu\text{m}$, and $T_b = 1.3 \times 10^{18} \text{ cm}^{-3}$. These results are shown in Figure 5. The solid lines show the fitted data. The best fits are obtained if we assume the dissociation frequency, $k' = 0.2$. It should be noted that same parameters give excellent fit for experimental profiles for different times.

The next example we consider case of low-energy implanted sample. Figure 6 shows a measured deuterium profile (thick, dotted line) of a FZ sample, implanted at 250 °C at approximately 1.5 keV, for 30 min. Because this is a case of ion implantation, we have tried to fit this data with various values of the flux density and a distribution function of :

$$[T_{\text{tot}}] = [T_0] \cdot \frac{t}{T} \cdot \exp\left(-\frac{(x - x_p)^2}{\Delta x_p}\right) + [T_b]$$

where $[T_0] = 4.454 \times 10^{20} \text{ cm}^{-3}$, $T = 1800 \text{ s}$, $x_p = 0.0367 \text{ }\mu\text{m}$, $\Delta x_p = 0.001596 \text{ }\mu\text{m}$, $[T_b] = 1.2 \times 10^{17} \text{ cm}^{-3}$.

$$Nt_b = 1.2E17, k_{th} = 0.1$$

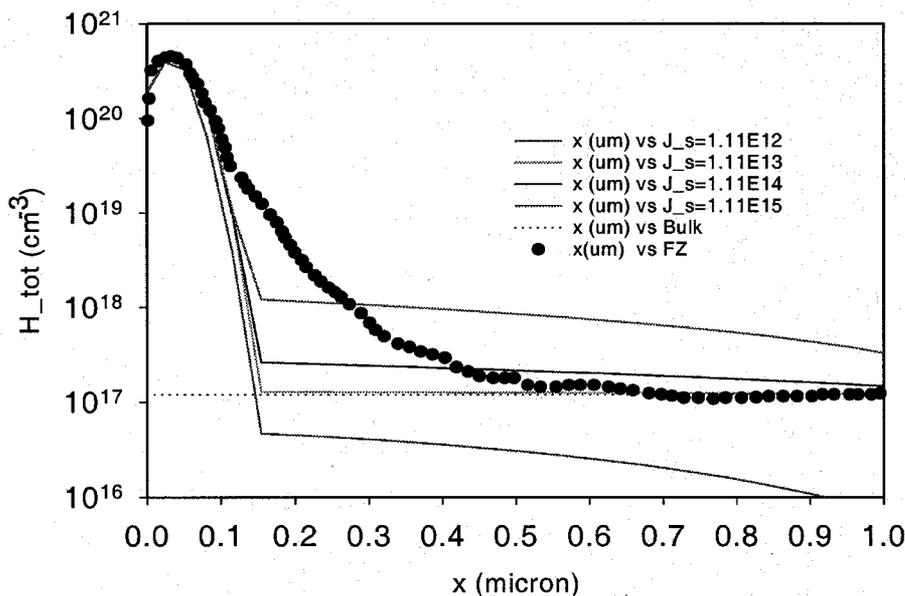


Figure 7. Experimental and calculated profiles of deuterium: deuterium was implanted at 1.5 KeV, at 250 °C for 30 min.

These calculations are performed for different values of deuterium flux – ranging from 1.1 E12 to 1.1 E15 cm^{-2}/s . It is interesting to note that the near-surface distribution of D does not change with flux (as expected). However, there is a strong dependence of bulk distribution on the flux

density. An important result is that it is difficult to fit the entire profile under the assumption of immobile traps.

CONCLUSIONS

An extended H-trapping model, that includes both bulk and process-induced traps, as well as detrapping processes, can yield excellent fit to the experimental H or D profiles. In most cases, it is sufficient to assume immobile traps. However, we have encountered situation where it is necessary to include mobile traps.

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Pilot Manufacturing of Dendritic Web Photovoltaic Products

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ABSTRACT

A new pilot manufacturing facility has been established for the commercial production of dendritic web photovoltaic modules. After several years of significant advances in dendritic web growth and low cost cell development, EBARA Solar, Inc.(ESI) initiated operations in this facility in May of 2001. The production processes will initially be based on the PhosTop cell design with a dendritic web substrate. Continuing development at the same facility will enable ESI to eventually produce and market high efficiency back contact and bifacial solar cells.

INTRODUCTION

After years of development of the dendritic web technology, Ebara Solar, Inc. (ESI) has established a pilot manufacturing line in Southwestern Pennsylvania. The pilot facility is based on the dendritic web crystal growth technology, a few unique cell designs, standard power modules, and a variety of unique module configurations. This new facility will be producing the first commercial dendritic web modules which will be sold internationally. In addition, R&D efforts to further improve the cost, reliability, and throughput of the involved processes will be continued at this facility. This new facility, designed to have an ultimate production capacity of up to 4 MW/yr, was started up in May of 2001 and will be ramping up production capability through the remainder of the year to an initial stage production level. Additional expansion of capacity is expected through 2002.

Very successful development progress over the last three years has led to a threefold increase in furnace productivity, significant automation advances, and low cost cell processes. Crystal growth throughput has been improved by changes in heat shield design, zoned heating, magnetic melt stabilization, and significant automation of crystal starting and steady state growth processes. These changes have resulted in a five fold increases in average crystal length, an 80% increase in ending crystal width, and a tripling of run length. Through automation, manpower requirements in the crystal growth process have been reduced by a factor of 3. A unique cell design based on the PhosTop process is being used for the production baseline process. Development efforts aimed at increasing efficiency of this cell design have focused on metallization optimization, self-doping contacts, surface passivation, and anti-reflective coating improvements. This low cost cell design has seen an improvement of 30% in efficiency over the last year. In addition, bifacial and interdigitated back contact cells are currently being optimized, and should be available for production at this facility within the next 2 years.

DENDRITIC WEB GROWTH TECHNOLOGY

Dendritic web growth is unique in the world of crystal growth technology in that dendritic web grows as a thin ribbon, yet still retains its single crystal structure. Thin means efficient silicon

material utilization, while single crystal translates to excellent electrical properties. The first description of silicon dendritic web growth appeared in 1964¹. Figure 1 illustrates what happens during web growth. The liquid surrounding a fine silicon dendrite seed is initially supercooled below its freezing temperature by a few degrees. As the melt temperature falls, the seed first spreads laterally to form a button. When the seed is then raised, two secondary dendrites propagate from each end of the button into the melt. The button and dendrites act as a frame supporting a liquid film which crystallizes to form a silicon web having a $\langle 111 \rangle$ surface. Web is typically 100 μm thick and 6 cm wide, but thickness below 80 μm and widths over 8 cm have been routinely achievable. Replenishing the shallow melt with silicon pellets provides the conditions needed for steady-state growth. Web crystals over 100 m in length have been produced. Solar cells fabricated from silicon web crystals have achieved light-to-electrical energy conversion efficiencies above 17%.

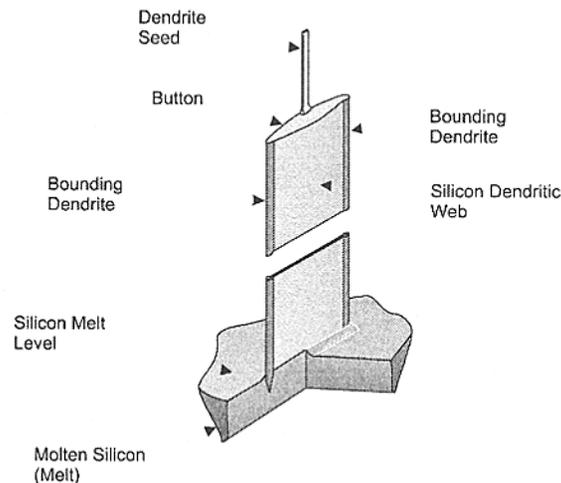


Figure 1. Schematic showing a dendritic web single crystal emerging from molten silicon supported by a frame of dendrites. web growth is initiated from a dendrite seed. Note all components shown are silicon.

Dendritic web silicon shares some common features with other forms of crystalline silicon used as solar cell substrates. In all cases, silicon is a stable semiconductor with a crystalline structure and an energy bandgap well-suited for converting sunlight into electricity. In web growth, as in Czochralski (CZ) ingot growth, molten silicon is contained in a quartz crucible and a single crystal of silicon is drawn from the melt. This means that both web and CZ silicon good structural and electrical properties, as well as high chemical purity since the growing crystal rejects impurities to the melt. However, a CZ silicon ingot must be sliced into wafers to make solar cells, and valuable silicon is lost in the sawdust. Silicon can also be cast into large polycrystalline blocks which must then be cut into wafers. Current technology limits the thickness of sawn wafers to approximately 300 μm . Some silicon ribbon technologies also exist which eliminate the need to saw wafers from ingots. These ribbons are polycrystalline, however, with typical thickness well above 200 μm . Only web and CZ silicon have the perfection associated with a single crystal. A major difference between web and all other forms of crystalline silicon used as substrates for solar cells is thickness. Web, with a typical thickness of 100 μm , is the thinnest form of crystalline silicon in production today. Unlike CZ and cast silicon, dendritic web grows as a sheet and so requires no sawing or etching of saw damage to produce a starting substrate. Unlike other forms of ribbon silicon, dendritic web is grown as a single crystal with flat surfaces. This combination of thin silicon with high material quality results in the most cost-effective use of silicon starting material for solar cells, as illustrated in Figure 2.

PHOSTOP CELL TECHNOLOGY

Dendritic web silicon calls for a unique solar cell structure to match. The structure developed by ESI and produced in quantity is shown in Figure 3. The p-n junction is formed by alloying aluminum with n-type silicon, and this p-n junction is located at the back (unilluminated) side of the cell. With a phosphorus front diffusion, the resultant n^+np^+ structure has been implemented using web substrates which are 100 μm thick and doped with antimony to 20 $\Omega\text{-cm}$. Such a structure eliminates shunting of the p-n junction, provides an effective front surface field, enables a high minority carrier lifetime in the base, and is immune to light-induced degradation. With a silicon nitride anti-reflective coating and solderable silver contacts as a grid on the front and as two stripes over the aluminum-silicon eutectic metal on the back, the cell is complete. This cell has been named “PhosTop”² because the top surface is doped with phosphorus rather than boron, as is usually the case for an n-base cell.

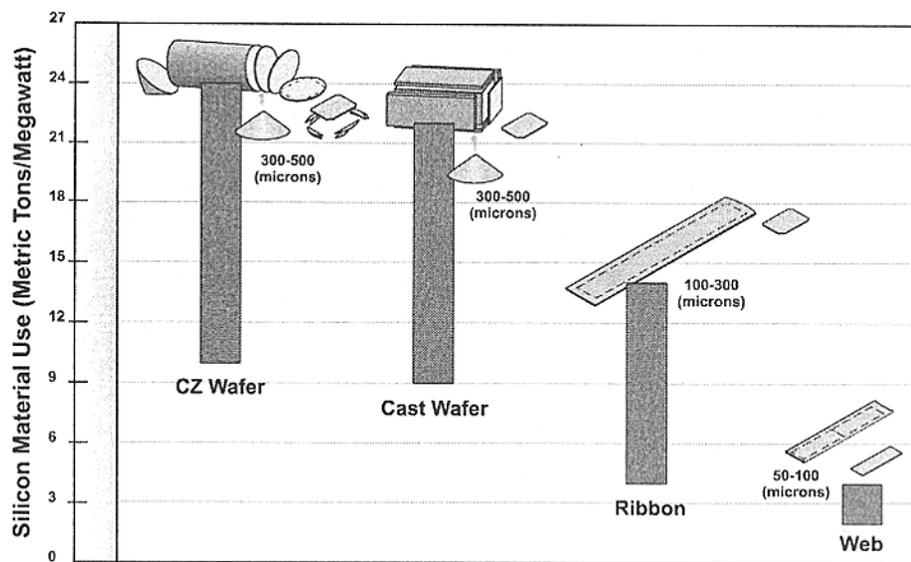


Figure 2. Comparison of material usage for various silicon solar cell substrates, showing that dendritic web utilizes silicon most effectively.

PHOSTOP Cell

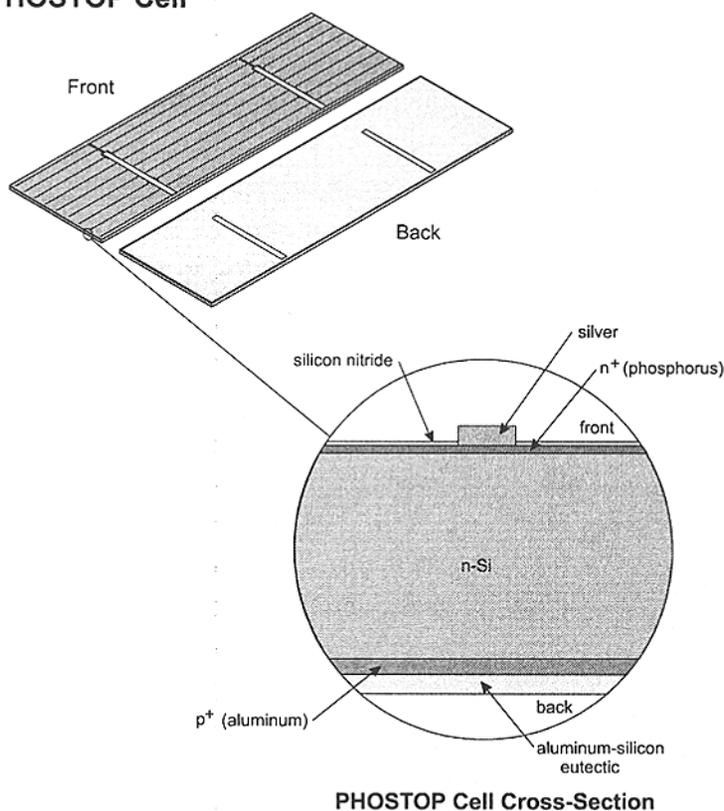


Figure 3. Structure of the aluminum alloy back junction

A comparison between conventional silicon solar cells, and the ESI “PhosTop” cell is given in Table 1. The PhosTop process utilizes high throughput screen-printing to deposit front phosphorus, back aluminum, back silver pads, and front silver grid. The printing steps are followed by equally rapid heat treatments in belt furnaces for phosphorus diffusion, aluminum alloying, and silver firing. A key feature of the PhosTop process is the use of a self-doping silver paste for the front grid. This eliminates the need for edge clean-up which is common in the silicon PV industry. The silicon nitride anti-reflective coating is deposited by plasma-enhanced chemical vapor deposition. ESI PhosTop cells made by the current production process typically have a light-to-electrical energy conversion efficiency in the range of 13 to 15%.

Table 1. Conventional silicon cell versus dendritic web silicon "PhosTop" cell.

Cell Feature	Conventional Cell	Dendritic Web "PhosTop" Cell
Substrate Thickness	300 μm	100 μm
Substrate Type (dopant)	p-type (B)	n-type (Sb)
Substrate Resistivity	1 $\Omega\text{-cm}$	20 $\Omega\text{-cm}$
Junction (dopants)	n^+p (P, B)	p^+n (Al, Sb)
Junction Location	Front (n^+pp^+)	Back (n^+np^+)

IBC and BIFACIAL CELL PROCESS TECHNOLOGIES

Because dendritic web silicon is thin (100 μm) and of high electrical quality (minority carrier diffusion length several times the thickness), it lends itself to more advanced solar cell structures. One such structure under development at ESI is the interdigitated back contact (IBC) cell. In the IBC cell, both positive and negative contacts are on the unilluminated side, thereby reducing shadowing losses to zero. Eliminating the front gridlines makes the cell aesthetically more pleasing for some applications, such as building-integrated photovoltaics. In addition, interconnecting cells into a series string is expected to be much simpler with both positive and negative contacts on the same side.

A "bifacial" cell is one in which both the front and back faces are designed to receive illumination.³ Since light energy can enter the cell from either side, the electrical output of a bifacial cell can be greater than the output from a conventional "monofacial" cell with only modest additional fabrication cost. If the resistivity of the web substrate is above 10 $\Omega\text{-cm}$, it is common for minority carrier diffusion length to be more than twice the nominal web thickness of 100 μm , meaning that the cell will respond to illumination on the p-n junction side or on the opposite (back) side. Web bifacial cells under back illumination typically produce more than 85% of the power produced under front illumination.

SUMMARY

After many years in development dendritic web is finally exhibiting throughput and performance characteristics that are enabling commercialization. A pilot facility for commercial production has been created to establish an initial market presence for web-based products. These products are based on unique, low cost cell designs. Standard power modules will be available, as well as unique designs taking advantage of the properties of the web substrate.

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Processing and Handling of Low Thickness Silicon Solar Cells

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1. Introduction

Near 80% of the world production of photovoltaic modules uses crystalline silicon as raw material. Cost of silicon wafers is responsible at least of 30% of the final cost of photovoltaic modules and competitiveness in PV cost will require to reduce the cost of raw material, either silicon or other different material. To lower the thickness of silicon wafers is an obvious way to reduce cost of PV solar energy [1,2] and figures lower than 1\$/Wp seem to be possible.

Besides being cheaper, low-thickness silicon substrates allow to manufacture a larger variety of efficient solar cell structures, like back-contact and bifacial cells, but even using low quality and low cost materials. The flexible behavior of thin silicon wafers could be also used in new applications, as for example over curved surfaces.

To lower the PV cost by reducing the thickness of Silicon wafers requires to keep an high value of conversion efficiency and to maintain a high mechanical yield over all the manufacture of solar modules: slicing of ingot, solar cell processing and module assembly.

In this paper we will present some results of processing thin solar cells, using industrial CZ silicon and a simple manufacturing process based in the boron deposition and diffusion by the screen-printing technique.

2. Cell processing and electrical results

Thin solar cells require an excellent passivation of their surfaces. High-low junctions, or low recombination emitters could be used instead. We use a conventional BSF structure, which is able to realize bifacial solar cells. The manufacturing process is extremely simple being similar, in number of steps, to those employed in mass production. This process is based in the formation of BSF (when used in p type wafers) by the screen-printing of boron and covers the following steps:

- a) Chemical cleaning and texturing of both surfaces of wafers
- b) Boron screen-printing over one face of the wafer and firing
- c) Phosphorus diffusion in POCl_3 ambient
- d) Spray deposition of TiO_2 antireflective layer
- e) Screen-printing and firing of metallization pastes

This process could be used with p and n type wafers giving to n^+pp^+ or p^+nn^+ structures.

CZ silicon wafers of industrial quality have been used. Two boron pastes, from different suppliers, and several Ag and Ag/Al pastes have been used. Best solar cells are 16.1% efficient with simetry (in bifacial cells) of 78% in p type wafers and 84% in n type wafers.

Firing conditions of the boron paste and of the metallization pastes, also, are very critical parameters, giving to high dependence of the minority carriers lifetime and to a strong dependence of the series resistance [3]. This last parameter shows a strong correlation of the thickness of the wafer and of the firing conditions.

The lifetime of minority carriers in the base of cells was checked after the most important thermal steps. High lifetime values in the fully finished BSF structure seem to evidence the correct operation of the gettering processes. These values can exceed 100 μ s in an appreciable number of cells but usually range from 40 to 60 μ s. Lower values are obtained only when an inappropriate function appears in the manufacturing process. Cells in the lower lifetime range, and with 80-100 μ m of base thickness, show bifaciality values of over 95% and V_{oc} , I_{sc} of 600 mV and 32 mA/cm² respectively. These values seem to be appropriate for an industrial manufacturing line. Numerical simulations, using the internal cell parameters obtained by MultIV software [4], showed a high level of agreement with experimental results. However, a large contact resistance of the screen printing metallization was been obtained. A dependence of firing conditions on the thickness of cells seems to be clear. Also, lifetime of p type wafers showed a strong dependence of firing conditions of the boron paste.

The optimization of firing of the boron paste led to an improved BSF effect on p type wafers and higher lifetime values in base. Solar cells of 27 cm² have been done in 103 x 103 mm wafers in quantity of 3 per wafer. The optimized process has been applied over carrier 2C, including 12 wafers. In order to diminish the series resistance and optimize the fill factor the firing process of the metallization pastes has been change each two wafers. The following table shows the results of a batch of solar cells, manufactured at different firing conditions.

Wafer	Front Isc (mA)	Rear Isc (mA)	Front Voc (mV)	Rear Voc (mV)	Bifaciality (%)	Eff. Front (%)	Eff. Rear (%)
2C4	920	702	595	587.5	76.3	13.3	10.0
2C6	938	719	599	592	76.7	14.6	11.4
2C8	895	695	596	589.5	77.7	12.6	10.2
2C10	948	685	605	596	72.3	14.8	10.6
2C14	939	645	606	598	68.7	15.7	11.0
2C16	955	673	606	598	70.5	16.1	11.6
2C18	972	660	595	587	67.9	13.1	8.4
2C20	922	685	603	594	74.3	13.2	10.4

Table 1. Electrical results of different solar cells with area of 27 cm².

Optimum firing point was obtained over 2C14 and 2C16 cells. In these cases 16% efficiency under 1 sun front illumination was obtained. Bifaciality ranges from 60 to 78%, being 70% a usual value.

An analysis of achievable efficiencies has been made by using PC-1D [5]. Lifetime values of only 40 μ s have been used. An external series resistance of 1 Ω -cm² simulates the usual value in screen-printed cells. Figure 1 shows some results. Both, theoretical and experimental results are in good agreement. The main conclusions are the necessity for a low base thickness to achieve high efficiencies under back illumination. Light trapping is essential to obtain high efficiencies in low thickness cells both under front and back illuminations. Efficiency is also a function of wafer resistivity. Front efficiency is highly dependent on that, however, back efficiency is almost independent. Optimum values to base resistivity seem to be within the 3 to 5 Ω -cm range. Greater improvement in efficiency requires severe changes in emitter profiles.

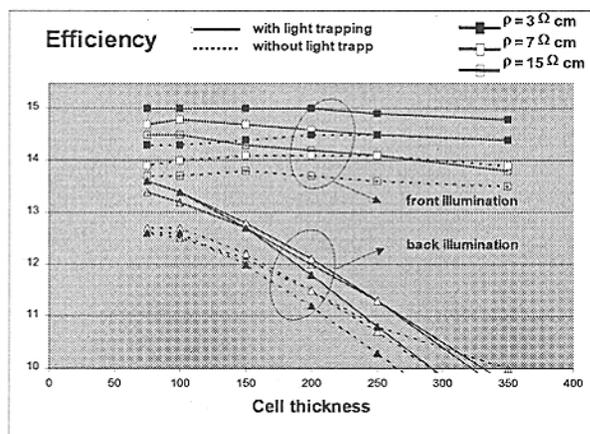


Figure 1. Front and back efficiency vs cell thickness and base resistivity

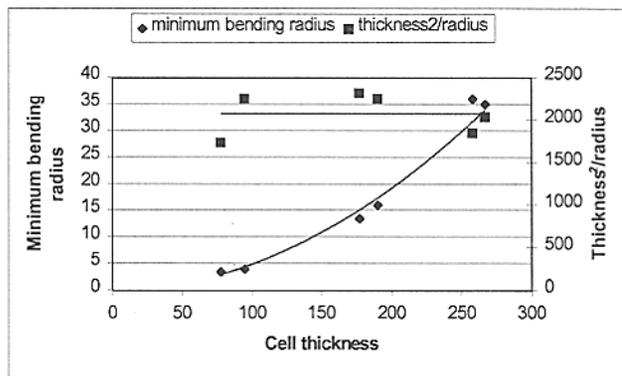


Figure 2. Minimum bending radius vs cell thickness

3. MECHANICAL ANALYSIS

Mechanical behavior of thin wafers is very different from conventional ones. Thinner wafers are highly flexibility and their breakage can be avoided if this is taken into account. To obtain the allowed maximum bending over wafers, we have carried out a systematic analysis. The minimum radius before wafer shatter has been obtained for a variety of thickness and processes. CZ silicon from two different manufacturers has been used. Several experiments have been made to analyze the dependence of surface properties, dopant additions and thermal processes. Polished and textured surfaces, with and without thermal processes, have been analyzed. Bending in two different crystallographic directions, $\langle 110 \rangle$ and $\langle 100 \rangle$, have been applied. No appreciable difference has been observed between these experiments. The only parameter controlling wafer bending seems to be their thickness, independently of surface finishing or thermal processing.

A simple expression links bending to thickness. According to this, the maximum bending is a linear function to the square of the thickness. A minimum radius of only 2 cm corresponds to a thickness of 95 μ m. Figure 2 shows several experimental values and good

agreement with this simple rule. Mechanical breakage could be avoided preventing a lower radius.

An analysis of the breaking mechanisms requires the knowledge of momentum and stress inside the wafer. We made this analysis previously [3] and the results suggests that breakage is caused by an intermediate effect between both behaviors, maximum tension and momentum, but in any case, it appears that this occurs inside the wafer, not on its surface. This conclusion would coincide with the fact that the breakage radius is irrespective of the surface treatment of the wafer.

Without a good understanding of what is the real mechanism that causes the wafer to break, although this might be linked to the transmission of the momentum across several crystallographic planes. We can say that the maximum momentum that the wafer can withstand is proportional to its thickness. Hence, it is easy to calculate the maximum admissible loads, as well as the deformations that can be expected. Depending upon the results, it is possible to adjust the parameters of the wafer handling equipment, ensuring high mechanical yield values.

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CONTACT RESISTANCE SCANNING FOR PROCESS OPTIMIZATION: THE CORESCANNER METHOD

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ABSTRACT

It is difficult to obtain screen printed grid lines on solar cells with a low contact resistance, since the contact formation is very sensitive to many parameters. To optimize the process, it is necessary to be able to measure the contact resistance for each grid line. Recently, we have introduced an instrument that can do this, called the Corescanner.

In this paper, the relation between process parameters and contact resistance is investigated using this instrument. The most important finding is that poor contacting results in large inhomogeneities in contact resistance. Even for cells with very low fill factors, regions of low contact resistance can be found. Low firing temperature settings lead to a large region of high contact resistance, and an uneven printing pressure results in large contact resistance differences across the cell, although no problems were visible by microscope. In this way, we will build a problem solving library of process issues and related contact resistance scans.

To conclude, the Corescanner provides us with a technique to monitor contact resistance. This instrument is a valuable tool for fault detection, error diagnosis and process optimisation.

INTRODUCTION

One of the key issues in industrial crystalline solar cell processing is to obtain a good contact below the screen printed metallisation. The print quality and the sintering determine the quality of the formed contact. For instance, cleaning of screens, screen quality, paste rheology and print pressure influence the print quality. The sintering of the metal paste can be influenced by emitter homogeneity and sheet resistance, coating homogeneity and thickness, temperature homogeneity and stability of the furnace. Although it is possible to achieve fill factors of 78% for screen printed cells in the laboratory, in industry 5-10% lower fill factors are common due to the sensitivity of contact formation.

Of course, it is important to determine which process parameter is responsible for the high contact resistances on the low fill factor cells. Recently, we have introduced a new patented technique [1,2,3] to scan the Contact Resistance over the entire surface of a solar cell, which is used by the Corescanner. With this instrument, a start is made to relate process problems and contact resistance scans.

THE CORESCANNER

The Corescanner can scan the contact resistance or locate shunts. The method for locating shunts is explained in [1,2], a comparison with lock-in thermography is presented at this workshop [4]. The Corescanner method for measuring contact resistance is shown in Figure 1. The principle is to measure the potential jump between a grid line and neighbouring silicon, which occurs due to a light beam induced current that flows through the metal-silicon interface. A potential probe is used for the measurement of the potential jump between grid line and neighbouring silicon. The probe is centred in the beam, moving together with it across the cell, while being in continuous contact with the surface.

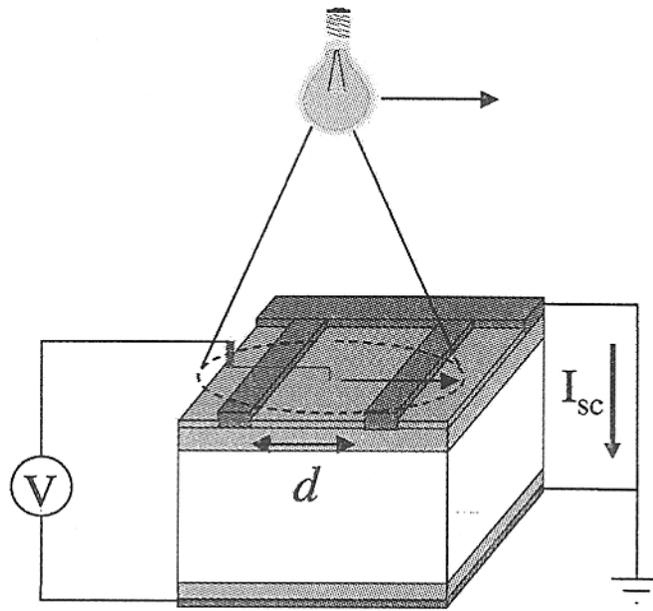


Figure 1: Working principle of the Corescanner

The contact resistance of the lines can now be determined from the measured potentials. The contacting properties of grid lines are traditionally characterized by the specific contact resistance ρ_c ; however, this approach has several disadvantages. In the first place, the local specific contact resistance below a screen printed line is not constant over the width of the line. Secondly, for low to medium ρ_c values it is necessary to know the sheet resistance below the line $\rho_{s,bl}$ for an accurate ρ_c calculation. Finally, for the performance of a region between grid lines it is only the combined influence of ρ_c and $\rho_{s,bl}$ that is important for the fill factor. Therefore, it is best to include the influence of $\rho_{s,bl}$ and inhomogeneous contacting in a useful definition of the contact resistance for grid lines, called the line contact resistance R_{cl} . In the following definition this is the case, since the potential difference V_{ce} between the edge of the contact (grid line) and the neighbouring silicon is determined by the combination of all resistance sources below the line:

$$R_{cl} = \frac{V_{ce}}{i_c} = \frac{V_{ce}}{J_{sc} d},$$

where i_c is the current entering the contact per unit length of contact, J_{sc} is the local short circuit current density generated in the illuminated area and d is the distance between the fingers. J_{sc} needs to be measured only once per cell: J_{sc} variations from point to point are typically less than 10%. J_{sc} should be kept at approximately 30 mA/cm², to minimize errors due to possible non-ohmic behaviour of the finger contact which occurs at high current densities. An example of a typical Corescanner line scan perpendicular to the fingers and performed at $J_{sc} = 30$ mA/cm² is shown in Figure 2:

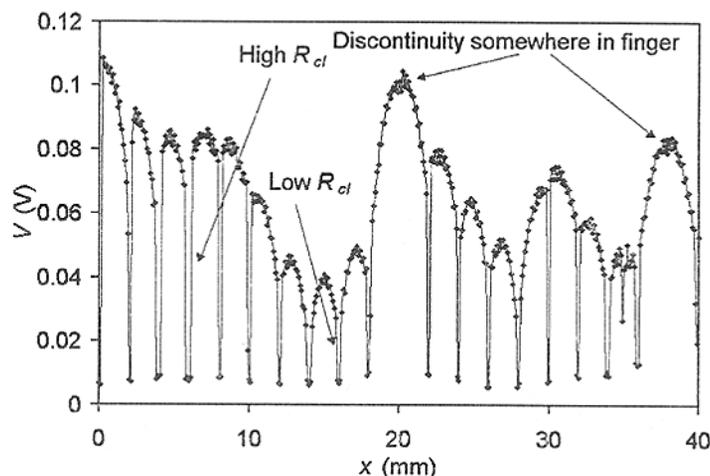


Figure 2: Corescanner line scan perpendicular to fingers

This line scan shows typical features of a Corescanner measurement:

1. Fingers are at the lowest potential because they are in contact with the grounded busbar,
2. Between the fingers the potential has a parabolic shape due to emitter sheet resistance,
3. Potential jumps are present at the fingers due to contact resistance,
4. Finger interruptions cause high parabolas due to a doubled finger spacing.

Cells can be studied best by scanning the entire surface in about 20 min time, and plotting potentials in 2D or 3D graphs, as shown for a typical example given in Figure 3:

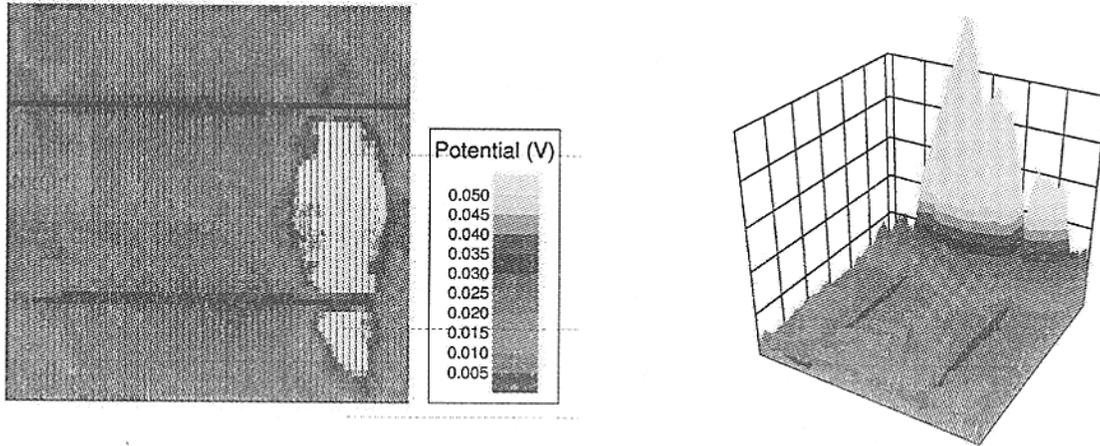


Figure 3: 2D and 3D representation of contact resistance measurement with the CoreScanner

In a 2D graph, large colour differences between finger and silicon indicate a high contact resistance. The cell was measured at a J_{sc} of about 30 mA/cm^2 , as for all the cells presented in this paper. Also the colour encoding of the above 2D picture is used throughout the paper. Potentials between fingers above 0.015 V indicate locations where the contact resistance is too high.

ANALYSING PROCESSING PROBLEMS

With the Corescanner, we now have an instrument to monitor the contact resistance over the complete solar cell surface. In this section, some process parameters are changed and contact resistance scans measured. These results will be used to set up a library of process problems and related scans. When low fill factors occur, this library can be used to determine the cause.

Influence of firing temperature

To investigate the influence of peak firing temperature on contact formation, multicrystalline silicon solar cells coated with SiN_x were fired in a belt furnace at different peak temperatures. The peak temperatures used were 855 , 870 , 885 and $900 \text{ }^\circ\text{C}$. The scans on these cells are shown in Figure 4:

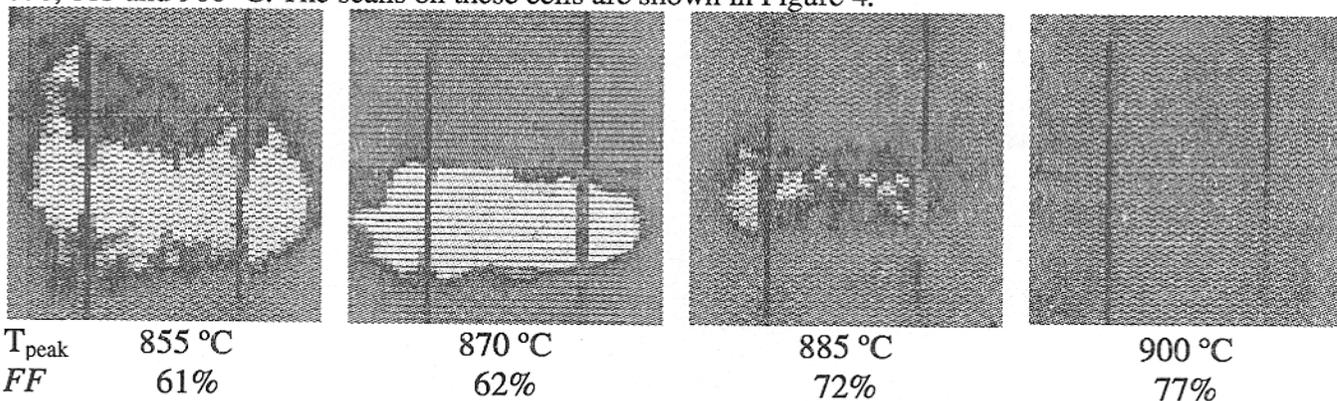


Figure 4: Contact resistance scans as a function of peak firing temperature

These pictures show for the first time the influence of firing temperature. Surprisingly, it is the homogeneity of the contact resistance that is influenced the most. Even for the cell with a very low fill factor, regions can be found

where the contact resistance is as good as for the high fill factor cells. Currently, we are investigating the cause of these inhomogeneities to increase the process window for firing.

Influence print pressure

A second factor influencing the contact formation is the print quality. Normally, this is monitored with a microscope. However, not all effects are visible by detecting the shape of the printed lines. For instance, when the print pressure is varied, the visible print quality stays the same. However, the contact resistance is strongly influenced, as can be seen in Figure 5:

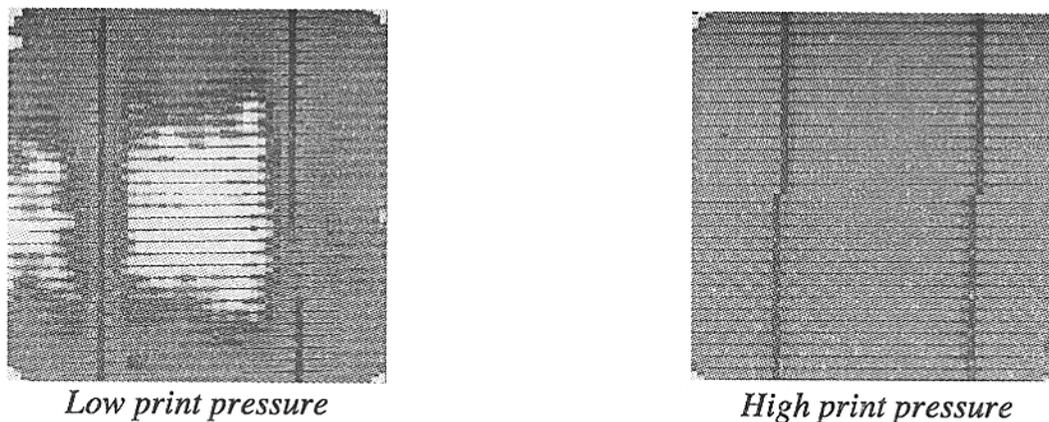


Figure 5: Influence of print pressure on contact resistance scan

Contact resistance is highest at the centre of the cell. It was determined that the vacuum chuck of the printer was not flat due to wear of placing cells. The non-flatness of the chuck becomes strongly visible for lower pressures.

CONCLUSIONS

In this paper, contact resistance is measured over the entire cell surface using the newly developed Corescanner in contact resistance mode. For the first time, it has been possible to investigate the relationship between processing parameters and the distribution of contact resistance over the solar cell. Peak firing temperature for example, is found to influence the contact resistance homogeneity drastically. This provides a means for diagnosing temperature settings during production. The method also forms a powerful aid in troubleshooting of other processing problems. For example, low fill factors during production could be allocated to the non-flatness of a worn vacuum chuck of a screen printer, whereby printing at a low squeegee pressure leads to high contact resistance at the centre of the cell.

Most importantly, poor contacting results in large inhomogeneities in contact resistance. However, even when low fill factors are obtained, areas of low contact resistance may still be present for a large region of the cell. This surprising result is a strong encouragement to improve the contacting process window by diagnosis with the Corescanner.

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Thin Film Silicon Solar Cells on Low Cost Glass and Glass-Ceramic Substrates: Recent Progress

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Introduction

The mass production of thin film solar cells requires the low cost deposition of silicon at high rates. As discussed in previous proceedings of this workshop, that requirement, in turn, necessitates the development of a low cost transparent substrate that can be processed at temperatures above 700°C, the minimum temperature to decompose dichlorosilane at an appreciable rate. Current glass substrates are not suitable, as even the most heat resistant commercial glass substrates soften at temperatures above 650°C. Fused silica, although transparent, is not a viable alternative either, because – besides being expensive - its thermal expansion is ~ 1/5 of that of silicon. A polysilicon film deposited at high temperature when cooled to room temperature therefore develops cracks, which, as shown previously, increase the leakage current of the cell. An attractive, low cost alternative is to use a glass-ceramic substrate. Glass ceramics are chemically very stable, can withstand high temperatures, and can be economically fabricated as large sheets as demonstrated by their commercial use to fabricate smooth black tops for electric ranges. By selecting a suitable composition, glass ceramics can be engineered to be transparent and to match the thermal expansion of silicon.

Glass-Ceramic Substrates

Under the contract, we investigated a glass ceramic in the SiO₂-Al₂O₃-ZnO-MgO-TiO₂-ZrO₂ system developed by Corning Inc. Its major ingredient is SiO₂ (about 70 vol%). After melting the ingredient, the material is a glass and can be shaped by standard glass forming methods, including e.g. “pressing” an anti-reflex, inverted pyramidal texture into the glass surface. The material is transformed by heat treatment into a glass ceramic, which consists of 10-15 nm-sized spinel crystals uniformly dispersed in a siliceous glass matrix [1]. The material is exceptionally transparent because the crystals (i) have a refractive index similar to the matrix and (ii) are too small to scatter light effectively. An additional benefit is that glass ceramics are much tougher than glass, as the spinel crystals impede the propagation of any crack present.

Barrier Layers

Barrier layers are required when these multi-component substrates are processed at high temperatures, typically 900 °C, since otherwise substrate components will migrate from the substrate into the polysilicon films. A major effort of the contract, discussed in earlier proceedings, was to develop a simple, low cost, and yet effective barrier layer. Eventually we settled on a system that consists of 1000 Å of SiN_x followed by 1000 Å of SiO₂. SIMS, as well as the analysis of test devices, shows this system to be an excellent diffusion barrier at temperatures up to 900 C [2].

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The p-i-n 'triple' poly-Si layer is the basic building block of the high efficiency, poly-silicon, thin film solar cell proposed by Martin Green. Multiple stacking of these layers permits to reach the necessary optical absorption to efficiently convert light. The i layer is designed to be depleted and, akin to the a-Si:H cell, separates the generated charge carriers by the built in electric field. As in the a-Si:H solar cell, this design minimizes sensitivity to recombination at structural defects. The properties of the intrinsic layer are crucial in optimizing cell efficiency. We reported in previous proceedings on how we measure the density of bandgap states in this layer, and how this density varies with substrate surface roughness and hydrogenation.

To characterize the p-i-n building block, we fabricate two kinds of test devices.

The *first* test device is fabricated entirely at Cornell. The p-i-n triple layers are deposited in a low pressure CVD system, from silane, at 620 °C, simultaneously on both (i) barrier layer coated glass-ceramic substrates and (ii) oxidized silicon control wafers. To facilitate the electrical analysis of cell operation and, in particular, depletion, the thickness of the i-layer was varied between 0 to 3000 nm. The films are then processed into vertical p-i-n diodes using photolithography and RIE etching.

Figure 1 shows typical I-V curves of devices fabricated on oxidized silicon 'control' wafers. Identical I-V data were measured on devices fabricated on glass-ceramics substrates. The fact that the data are independent of the substrate indicates (i) that surface roughness, which is higher on barrier coated glass ceramics, does not influence the electrical performance of p-i-n triple layer and (ii) that there is no impurity outmigration from glass ceramic substrates. To characterize the dependence of the junction characteristics on the thickness of the i layer, we inspected the ratio, R, of the forward and reverse current at 0.6 V. Figure 2 shows R, as a function of thickness, for diodes fabricated on both glass-ceramic and oxidized silicon wafers. It can be seen that R reaches its maximum value when the i-layer is about 1000 nm thick.

The *second* test device is fabricated partially at Cornell and partially at Purdue University. The reason for the split is that Purdue has an coldwall APCVD reactor, operated with dichlorosilane. This APCVD reactor is operated by Prof. Neudeck's group. This reactor can deposit thicker silicon films much faster than the Cornell reactor, which is a silane LPCVD system.

It is well known that polysilicon deposited from dichlorosilane tends not to nucleate well on SiO₂ surfaces². To promote nucleation, we therefore first deposit a thin polysilicon layer on our substrates (glass ceramic) and controls (oxidized silicon) at Cornell. Other approaches could be taken to deal with the nucleation problem (e.g. using SiN_x) but to keep continuity we decided not to change the barrier layer. One advantage

² Etching by, HCl, a reaction by-product, tends to dissolve nuclei forming on SiO₂.

of the present approach is that the “design” of the seed layer is very flexible as both its texture (which is highly temperature dependent) and grain size can be adjusted ³.

The use of two reactors to consecutively deposit polycrystalline silicon films immediately raises the question: Is the second deposition epitaxial on the first one? This is by no means self-evident, as the thinnest native oxide layer formed on the first layer will disrupt the epitaxial relationship.

To investigate this question, we deposited both doped and undoped seed layers of similar grain size (31 nm in n^+ and 29 nm in intrinsic films) on a variety of substrates. At Purdue, thick (around 2 microns) intrinsic poly-Si layers were deposited at 900 C onto these seed layers. In all cases, these thick APCVD films had a prominent {110} texture (see Table 1) which, as discussed by J. Werner at last year’s workshop, is the optimal texture for single layer polysilicon cells. The underlying reason is that most of the tilt boundaries formed are symmetric and hence do not contain dangling bonds, regardless of the tilt angle [3]. The {110} texture was more pronounced in the film deposited on an n^+ layer, which is favorable as in devices a doped layer is the bottom contact. The observation that the texture depends on the seed layer implies that APCVD deposited layer nucleate, at least partially, epitaxially on our seed films.

To investigate the relationship between seed layer and the APCVD deposited layer in more details, we inspected the interface between the LPCVD and APCVD layer by TEM. Figures 3 and 4 show examples of the cross-sectional TEM images obtained for samples using n^+ and undoped poly-Si seed layers. In both cases, the APCVD deposited poly-Si exhibited a columnar grain structure with increasing average lateral grain size toward the top surface. Near the top, the average lateral grain size APCVD poly-Si was measured to be about 150nm for an n^+ -seed layer, and about 210 nm on an undoped layer. However, it appeared that the variation in grain sizes were much larger for APCVD polysilicon grown on the n^+ -seed layer. Inspection of the figs. 3 and 4 shows that the APCVD poly-Si registers with seamlessly with the undoped seed layer but that a boundary can be seen in the case of the n^+ -seed layer. Possible reasons include the partial presence of native oxide on n^+ -seed layer ⁴, the influence of phosphorus atoms on nucleation, and the slightly different lattice constant of heavily phosphorous doped silicon.

The fabrication of vertical p-i-n solar cell test structures with thick layers poses a challenge in that the topography, after definition of the device, contains steps with a height equal to the sum of the thickness of the i layer plus the top p^+ layer, that is up to several microns in height. Therefore, a modified process was used. In addition, these thick intrinsic layers require a masks layout such that unavoidable alignment errors (which increase with i layer thickness) do not lead to shorts between the top p^+ and

³ A particular effective adjustment is to put down a thicker seed layer than needed, to oxidize partially the film, and to strip the oxide with HF. The injection of interstitials during oxidation both increases the grain size and coaxes the grain boundaries into configurations with less electrical activity.

⁴ It is known that n^+ doped poly-Si is more sensitive to oxygen, and in particular form forms oxidized grain boundaries which are never seen in undoped polysilicon films.

bottom n^+ contact layers. After the deposition and patterning of the n^+ layer, a thin (100 nm) layer of low temperature oxide (LTO) was deposited by LPCVD at 450 C and patterned. This layer served as an etch stop in areas of the device where the thick intrinsic APCVD layer was designed not to contact the n^+ layer (as, for example, in “point contact” type cells). Next, a thin, 100 nm thick intrinsic layer was blanked deposited. The purpose of this layer was to ensure laterally homogeneous deposition of the APCVD layer (without this layer, the APCVD layer will nucleate only in the LTO windows, leading to an even more irregular surface geometry). The top contact, a 100 nm thick layer of p^+ doped polysilicon was deposited at 620°C by LPCVD. This layer was covered with a (second) LTO layers, windows in which defined the device islands, which were formed by RIE dry-etching. To reduce edge leakage, the wafers then were annealed in nitrogen at 900°C for 4 hours. Aluminum contacts were thermally evaporated, patterned using lift-off technique and annealed in hydrogen at 400 C.

Preliminary electrical measurements on these devices show that they have a lower series resistance and larger forward current densities than those fabricated with the all 620°C. Further testing is being carried out.

Acknowledgements

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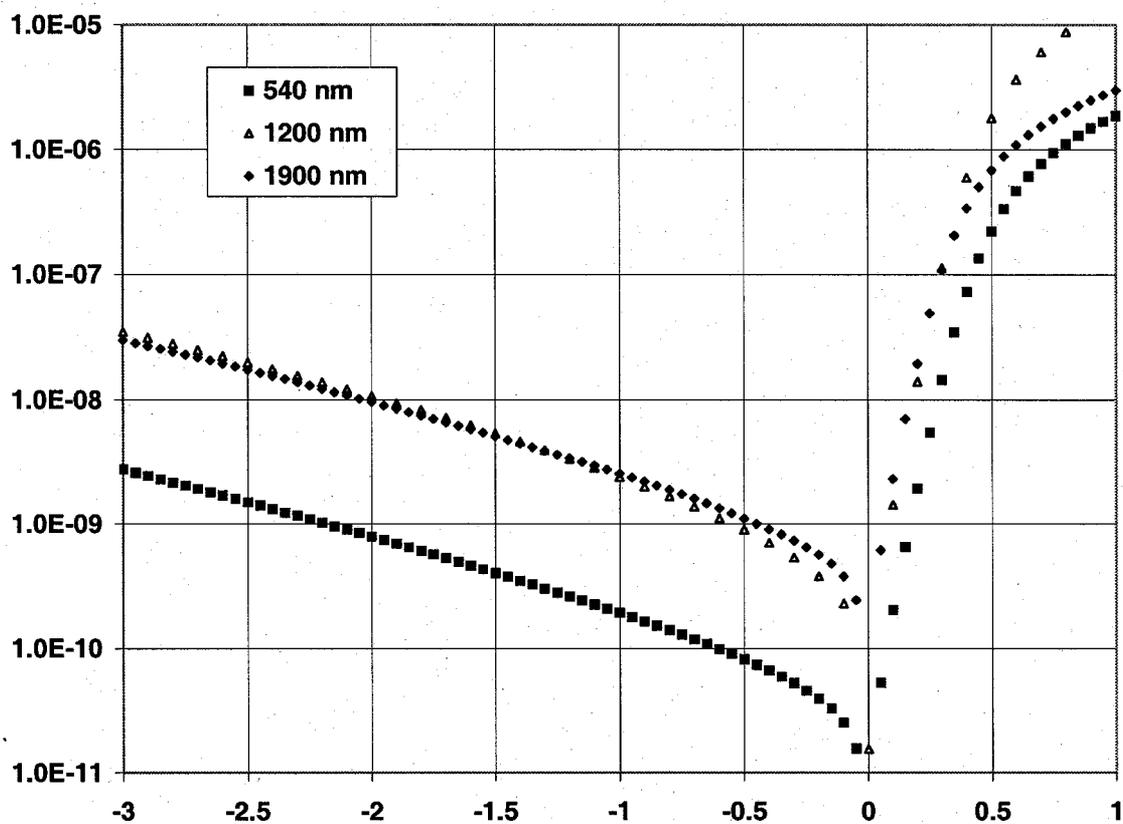


Figure 1. Dark current-voltage characteristics for p-i-n diodes made on barrier layer coated glass-ceramic substrates. The thickness of the i-layer is 540 nm, 1200 nm and 1900 nm.

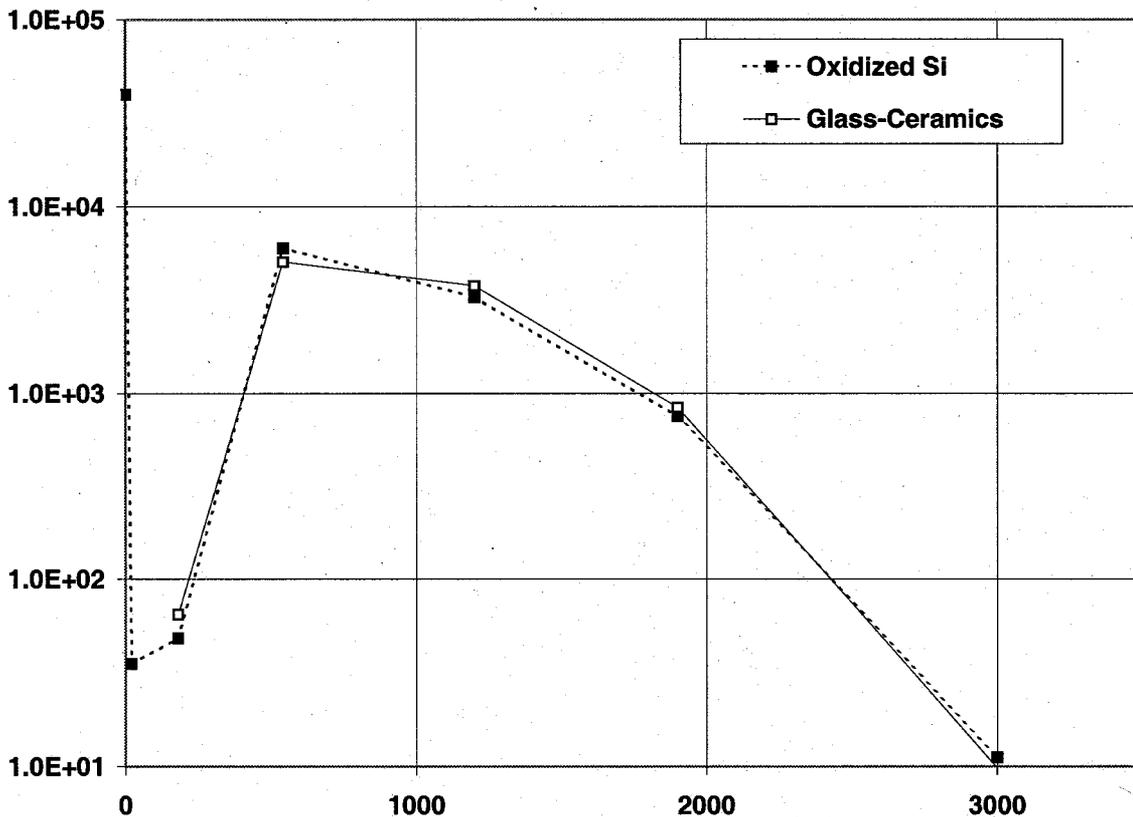
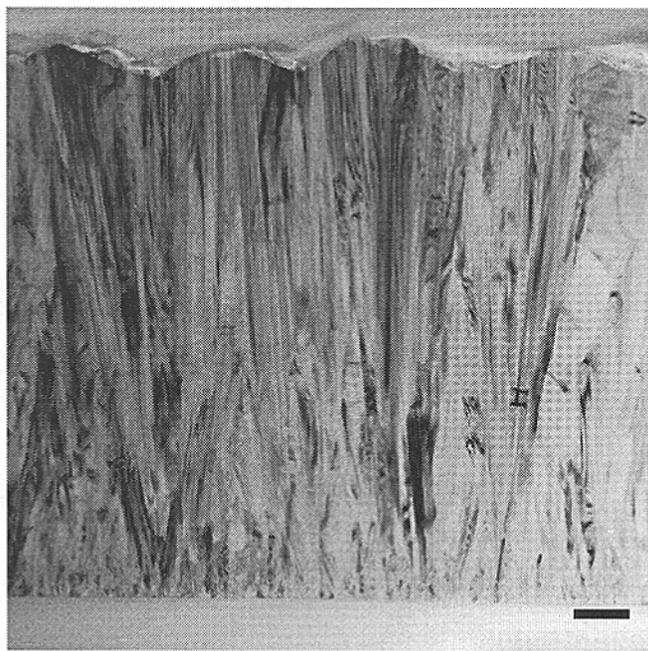


Figure 2. Diode rectifying ratio, measured at 0.6 V bias, versus thickness of the i-layer.



200 nm

Figure 3. TEM image of undoped APCVD poly-Si grown at 900 C on an undoped LPCVD poly-Si seed layer.

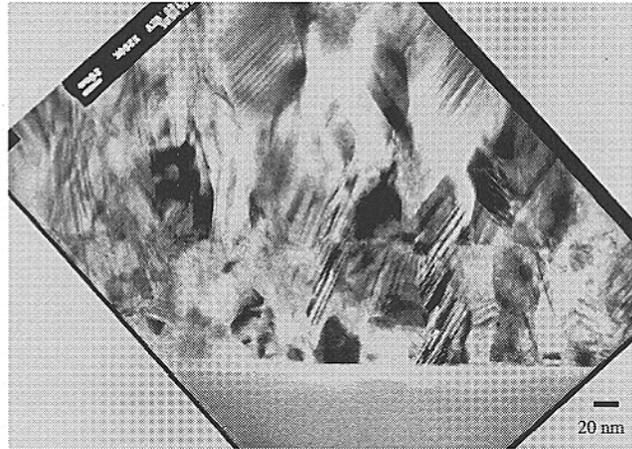


Figure 4. TEM image of undoped APCVD poly-Si grown at 900 °C on an n⁺ doped LPCVD poly-Si seed layer.

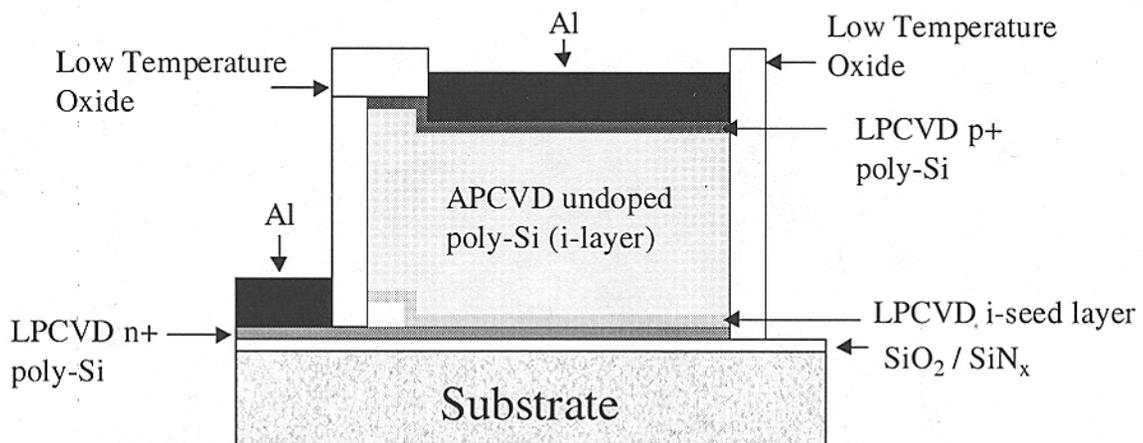


Fig. 5. Schematic layout of the solar cell test structure. See text for details.

Table 1. Texture of APCVD poly-Si films deposited on n+- and undoped LPCVD polysilicon seed layers deduced from X-ray diffraction measurements. Data took into account corrections for difference in structure factors and optical path length for different reflections. Intensity of (400) reflection in both cases could not be distinguished from the background.

Seed Layer	(111)	(220)	(311)	(331)	(422)
N+	5	2307	35	964	35
Undoped	54	1182	70	674	92

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13. ABSTRACT (<i>Maximum 200 words</i>): The 11 th Workshop will provide a forum for an informal exchange of technical and scientific information between international researchers in the photovoltaic and non-photovoltaic fields. Discussions will include the various aspects of impurities and defects in silicon – their properties, the dynamics during device processing, and their application for developing low-cost processes for manufacturing high-efficiency silicon solar cells. Sessions and panel discussions will review impurities and defects in crystalline-silicon PV, advanced cell structures, new processes and process characterization techniques, and future manufacturing demands. The workshop will emphasize some of the promising new technologies in Si solar cell fabrication that can lower PV energy costs and meet the throughput demands of the future. The three-day workshop will consist of presentations by invited speakers, followed by discussion sessions. Topics to be discussed are: Si Mechanical properties & Wafer Handling, Advanced Topics in PV Fundamentals, Gettering & Passivation, Impurities & Defects, Advanced Emitters, Crystalline Silicon Growth, and Solar Cell Processing. The workshop will also include presentations by NREL subcontractors who will review the highlights of their research during the current subcontract period. In addition, there will be two poster sessions presenting the latest research and development results. Some presentations will address recent technologies in the microelectronics field that may have a direct bearing on PV.				
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