Stability and Fidelity of Power-Hardware-in-the-Loop Using NREL’s CGI

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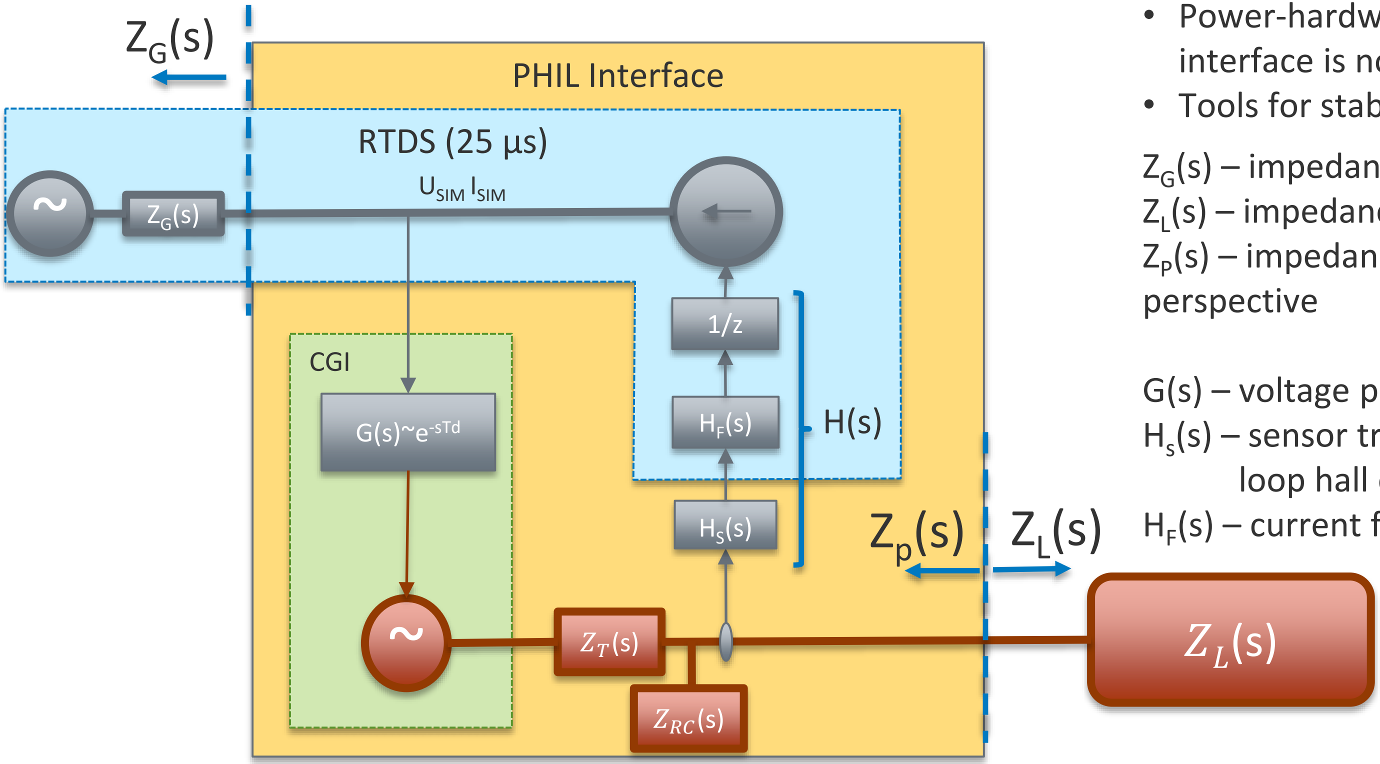
6th Annual International Workshop on
Grid Simulator Testing of Energy Systems and Wind Turbine
Power Trains and Other Renewable Technologies

Controllable Grid Interface (CGI) Control Diagram



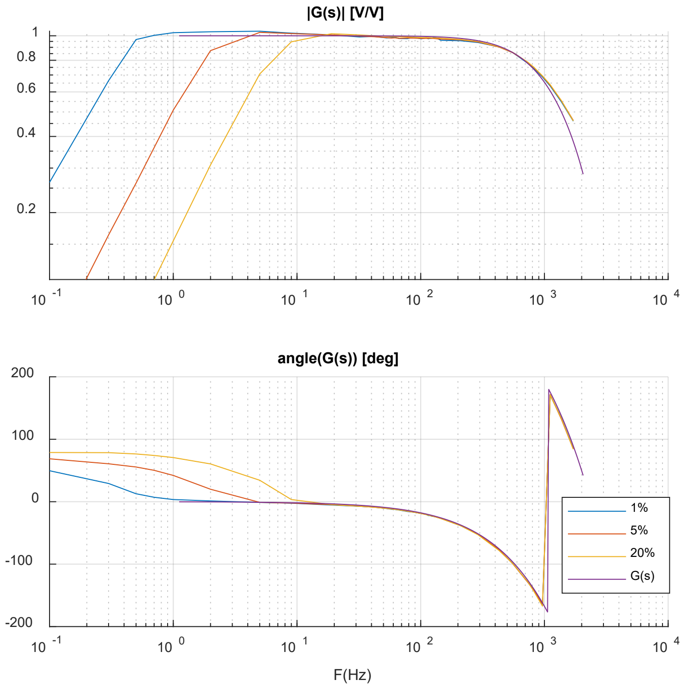
- Power-hardware-in-the-loop (PHIL) interface is now very well characterized
- Tools for stability analysis developed

$Z_G(s)$ – impedance of simulated grid
$Z_L(s)$ – impedance of load / DUT
$Z_P(s)$ – impedance of PHIL system from DUT perspective

$G(s)$ – voltage path ~ delay e^{-sTd}
$H_s(s)$ – sensor transfer function – closed loop hall effect current sensor
$H_F(s)$ – current filter

Acronyms:
DUT – Device Under Test
RTDS – Real-Time Digital Simulator

G(s) – Voltage Path Transfer Function



CGI#1 approximate transfer function:

$$G(s) = e^{-sT_d} \frac{1-e^{-sT_S}}{sT_S} \frac{1}{\frac{s}{\omega_C}+1}$$

Transport delay
T_d = 220 µs

Sampling
T_S = 250 µs

Low-pass
F_c = 1 kHz

CGI#2 – we expect significant improvement in all aspects.

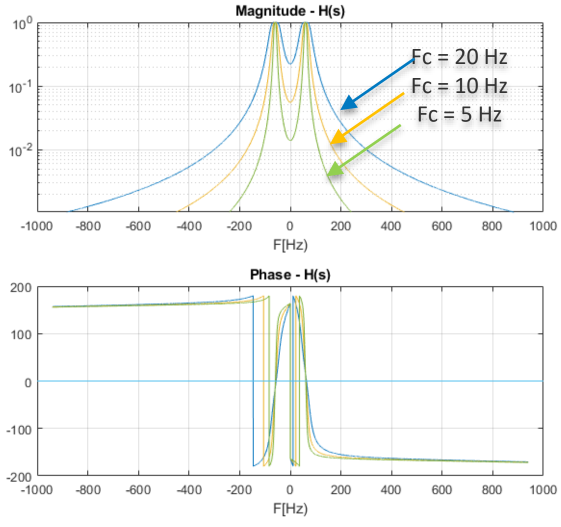
H(s) – Current Path

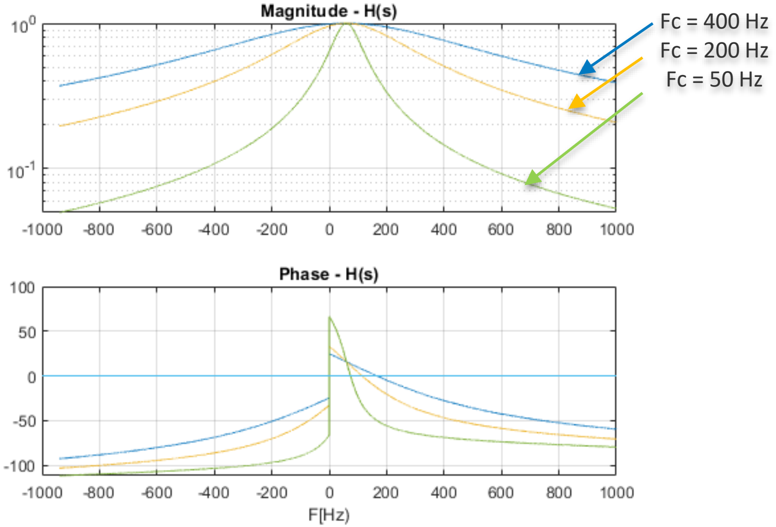
Option 1 (past)

- Decoupled pos/neg sequence measurements
- Independent delay compensation of pos/neg sequence
- 2nd-order filter
- Prone to instabilities due to transformer saturation.

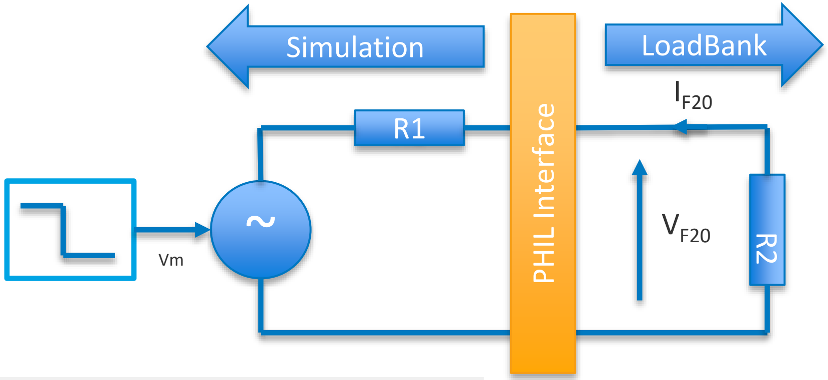
Option 2 (recent)

- 1st- or 2nd-order filter
- Delay compensation of positive sequence only
- Much higher bandwidth with proper stability design.





PHIL/Virtual Impedance – R-R Divider

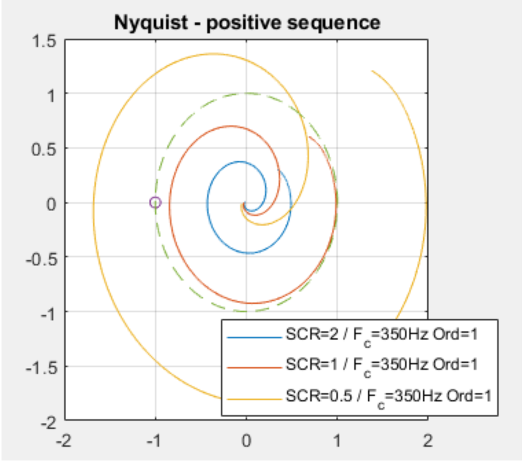


Using moderate filter H(s) with F_c = 350 Hz

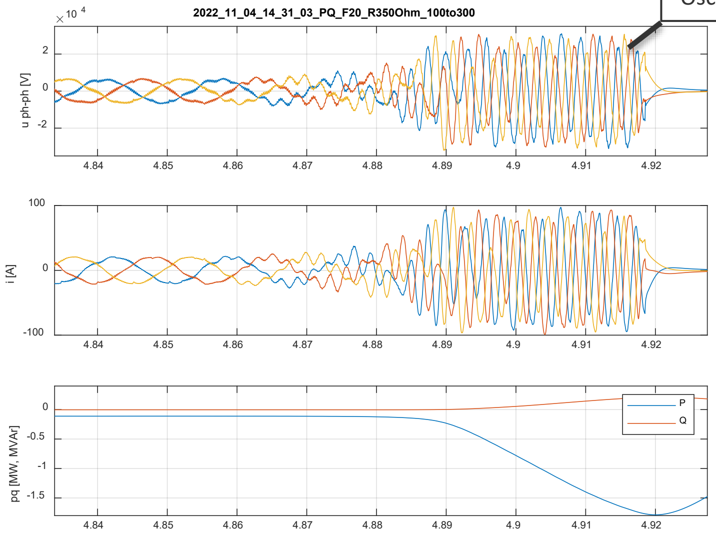
R2 > R1: SCR = 2 – stable

R2 = R1: SCR = 1 – stable

R2 < R1: SCR = 0.5 – unstable

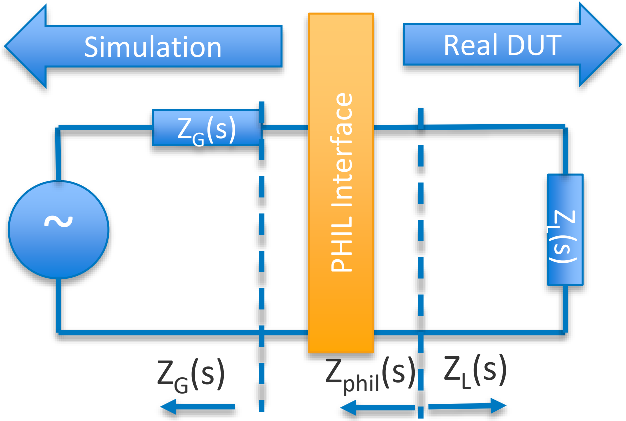


Oscillation at 370 Hz



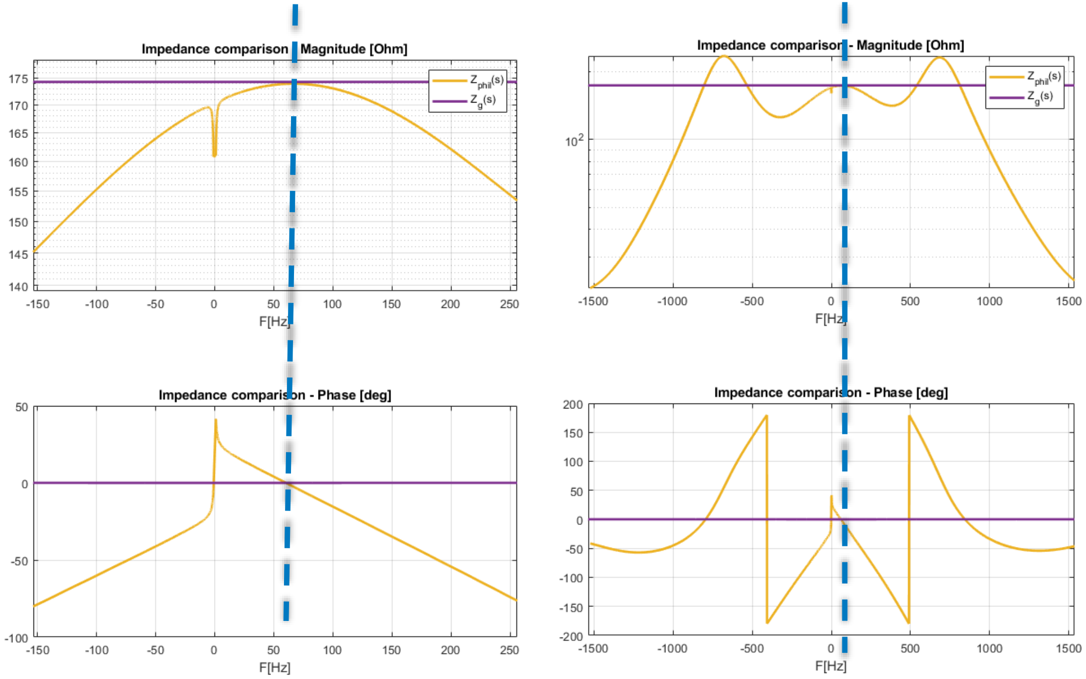
Acronyms:
SCR – short circuit ratio

PHIL Accuracy – Example Fc = 350 Hz/1st-Order

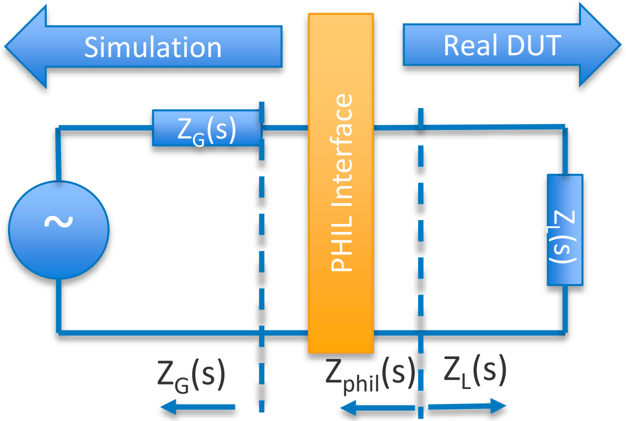


At 60 Hz – perfect matching of magnitude and phase

- Delay compensated
- Steady state: $PQ_G = PQ_L$

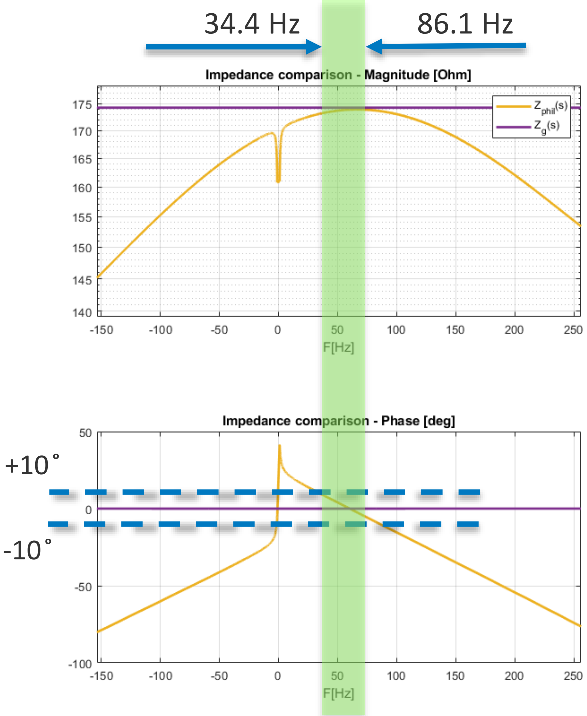


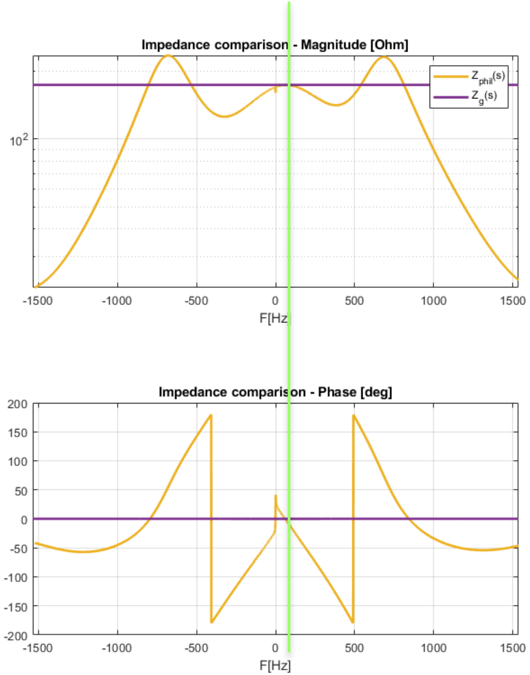
PHIL Accuracy – Example Fc = 350 Hz/1st-Order

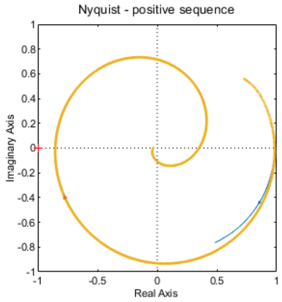


BW_{10deg} = 86.1 – 34.4 = 51.7 Hz

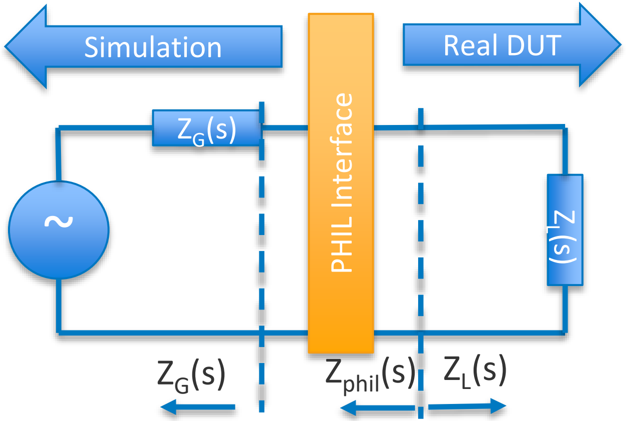
- Very high accuracy in this area





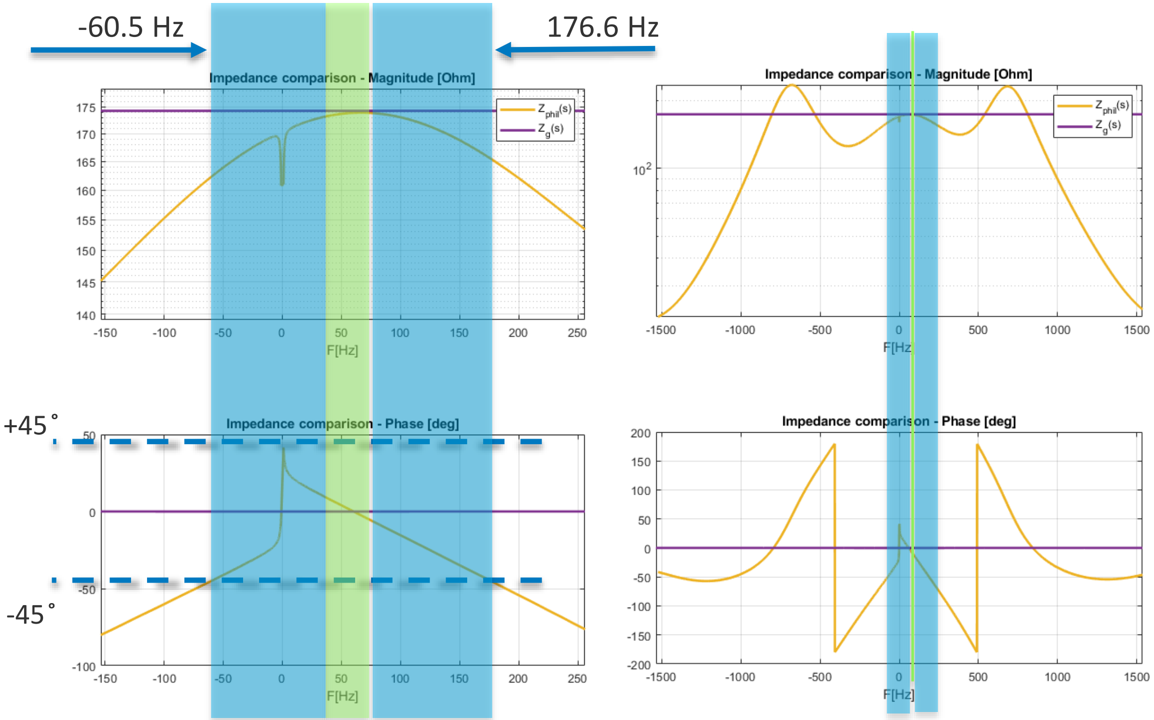


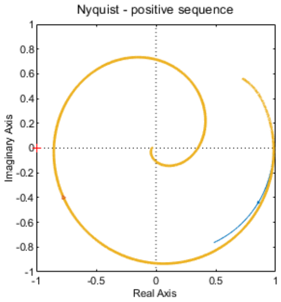
PHIL Accuracy – Example Fc = 350 Hz/1st-Order



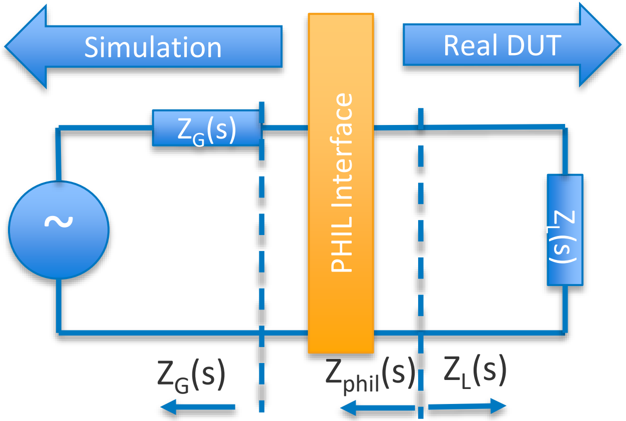
BW_{45deg} = 176.6 – (–60.5) = 237.1 Hz

- Impedance characteristics preserved

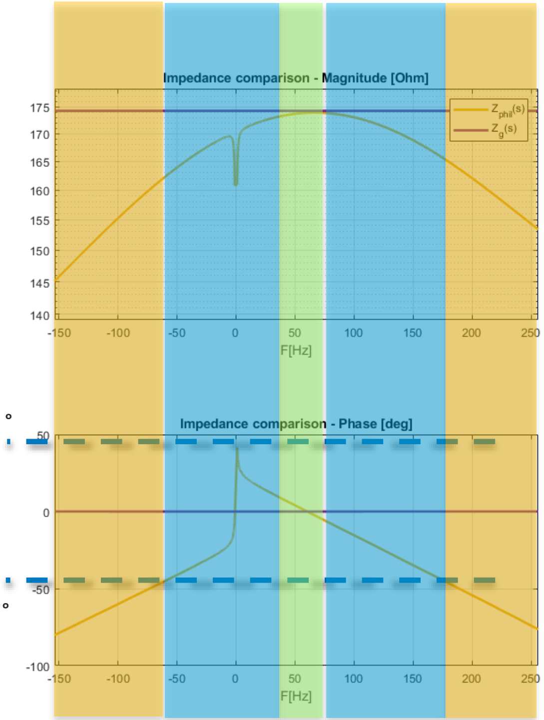




PHIL Accuracy – Example Fc = 350 Hz/1st-Order

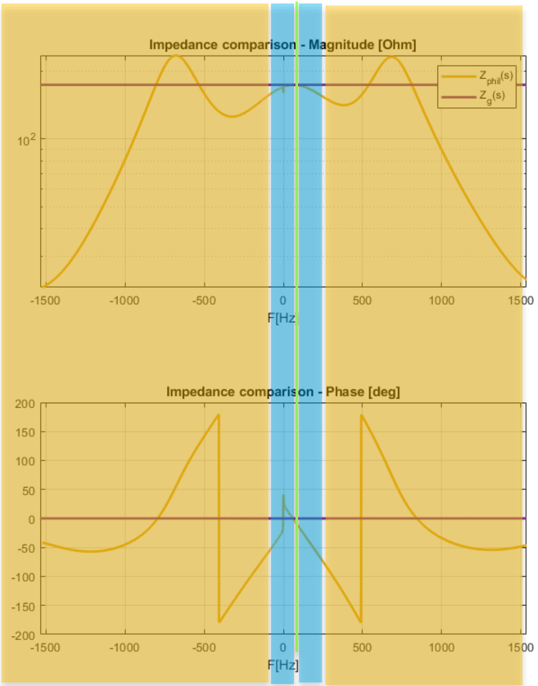


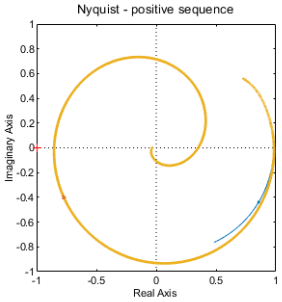
Outside BW$_{45deg}$ – filter out try to stay stable



+45˚

-45˚





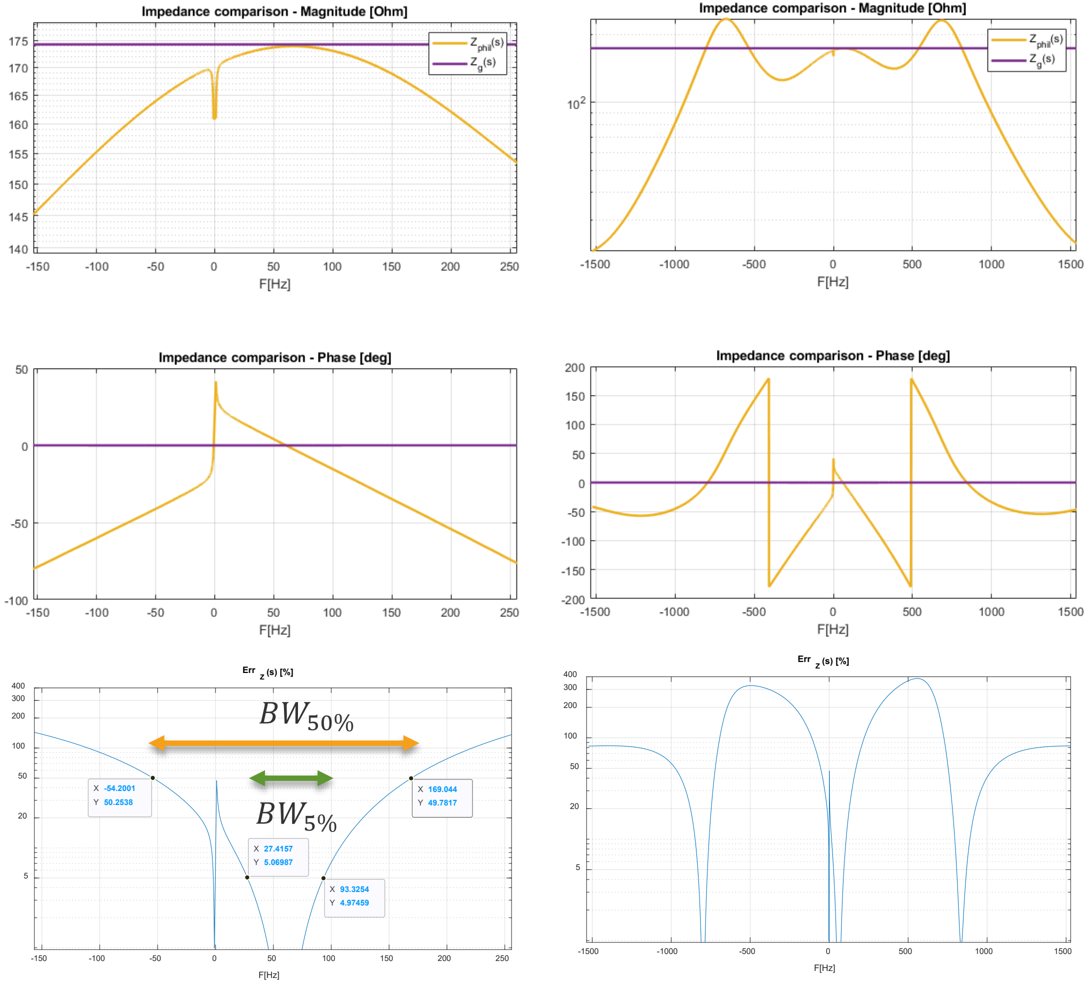
Przemyslaw Koralewicz, 5/9/202

PHIL Bandwidth Definition

- BW_{10deg} and BW_{45deg} do not take magnitude error into consideration
- Relative impedance error:

$$Err_Z(s) = \frac{\left(Z_{phil}(s) - Z_G(s)\right)^2}{Z_G(s)^2}$$

$$BW_{5\%} = 65.9\text{ Hz} \approx BW_{10deg}$$
$$BW_{50\%} = 223.2\text{ Hz} \approx BW_{45deg}$$

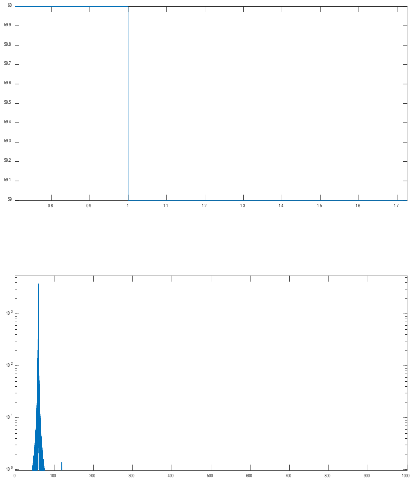


Signal Dynamics

60 to 59 Hz frequency step

e.g.:

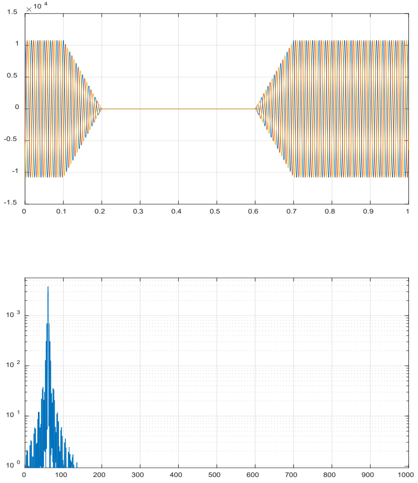
- Fault Ride-Through
- Load-gen balancing
- Inertia studies



100 ms voltage ramps (6 cycle)

e.g.:

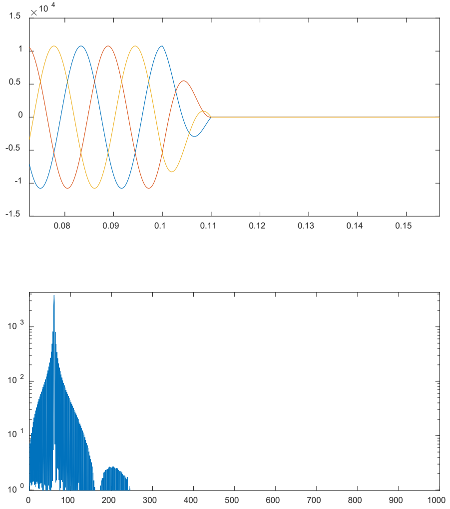
- V-Q droops slow support by Inverter Based Generation
- Soft black start



10 ms voltage ramps (sub-cycle)

e.g.:

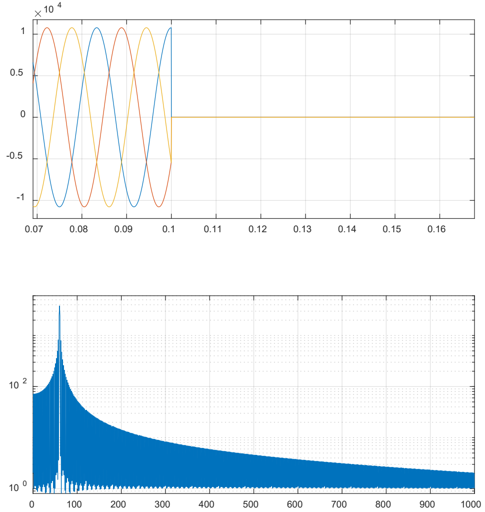
- Generators exciter control interactions
- Faster voltage control



0 ms - V step

e.g.:

- Fault near DUT terminals
- Breaker opening/closing



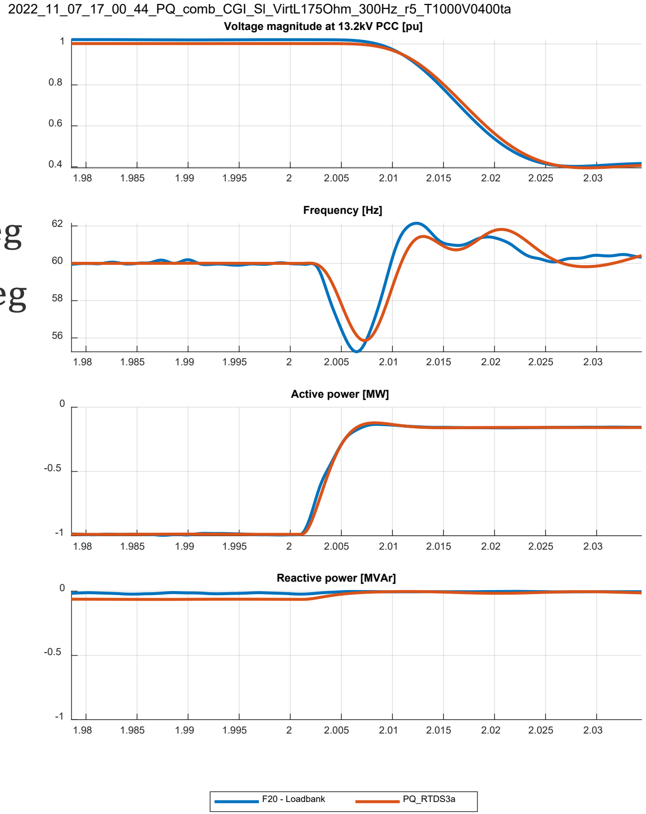
PHIL/Virtual Impedance – R-R Divider
SCR = 1, Fc = 300 Hz

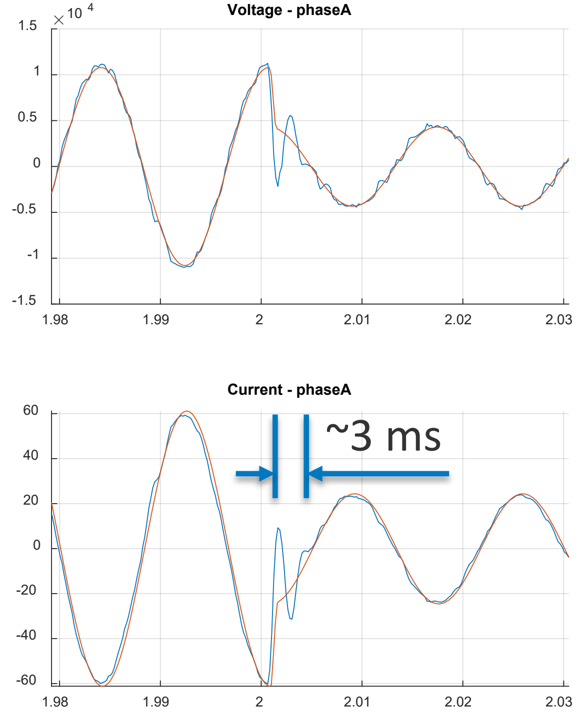
$$R_G = 174\ \Omega$$
$$R_L = 174\ \Omega$$

$$BW_{5\%} = 59.8\ \text{Hz} \approx BW_{10\text{deg}}$$
$$BW_{50\%} = 211\ \text{Hz} \approx BW_{45\text{deg}}$$

Time constant:

$$\tau \sim \frac{1}{\pi BW_{50\%}} = 1.5\ \text{ms}$$





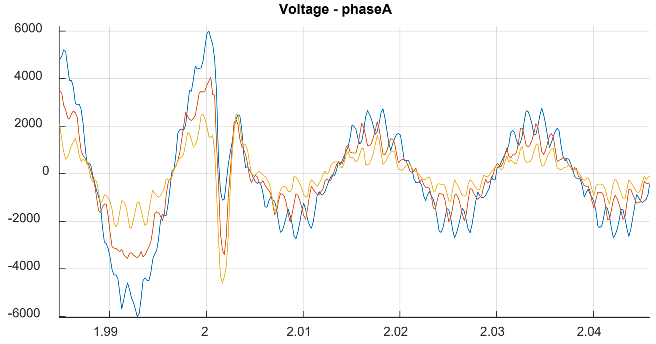
What Is Wrong With Bandwidth Definition?

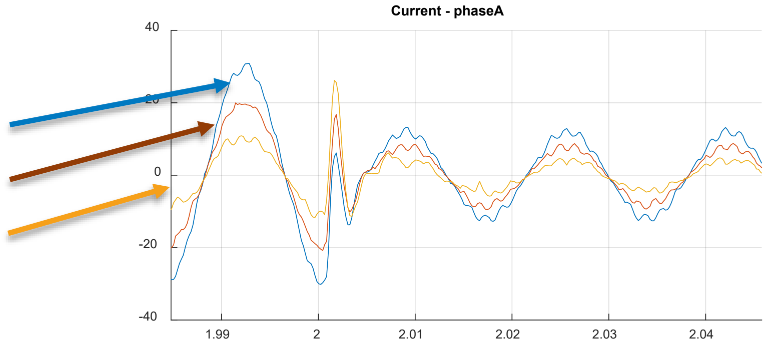
$BW_{50\%}$ does not give very good picture of what transient disturbance will look like.

Below – various bandwidth – same transient response.

Filter tuned to achieve same phase margin.

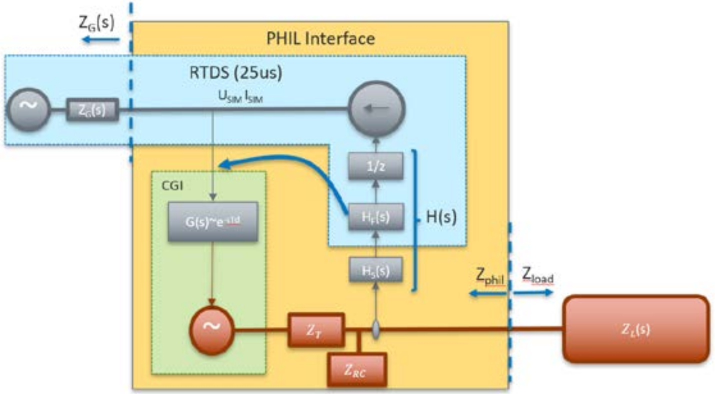
SCR = 1 $BW_{50\%} = 211\ \mathrm{Hz}$
SCR = 0.5 $BW_{50\%} = 123\ \mathrm{Hz}$
SCR = 0.2 $BW_{50\%} = 37\ \mathrm{Hz}$

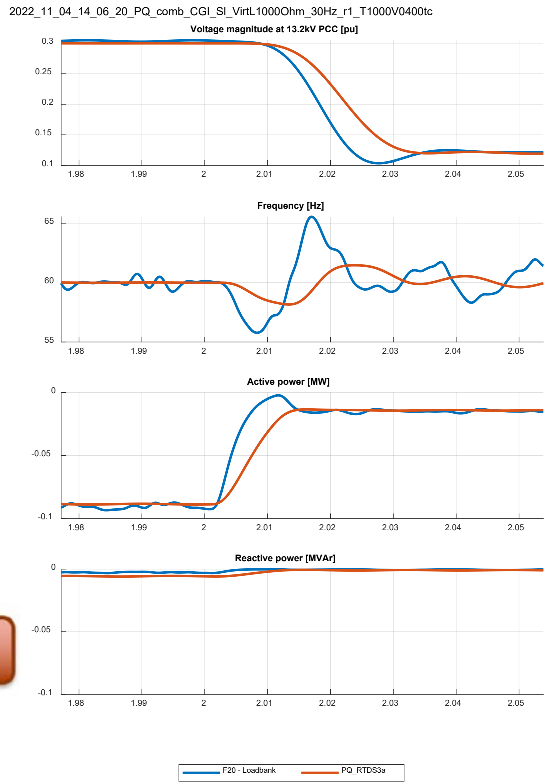


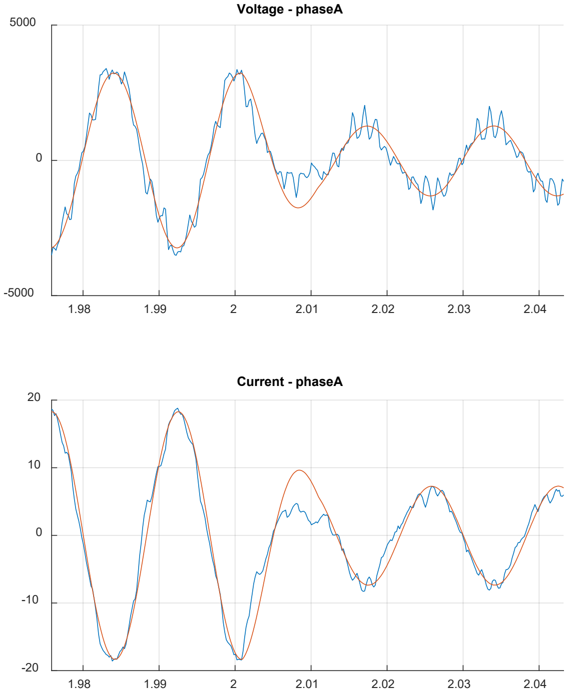


Mitigation of Transient Spikes

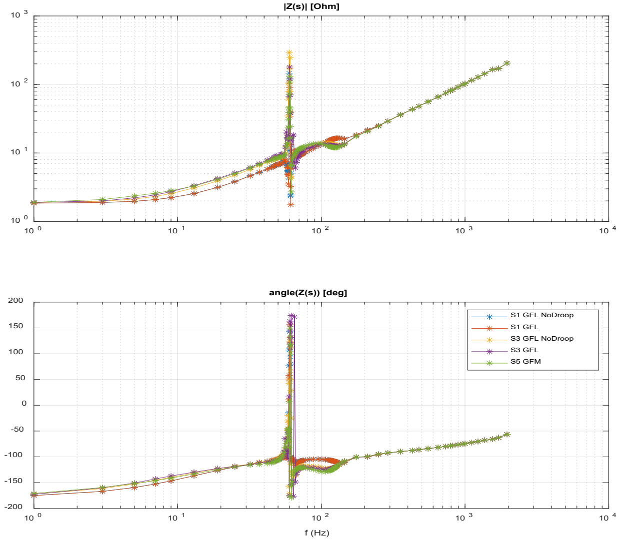
- Ramp rate limitation on perturbation signal
- Move H(s) filter onto voltage path

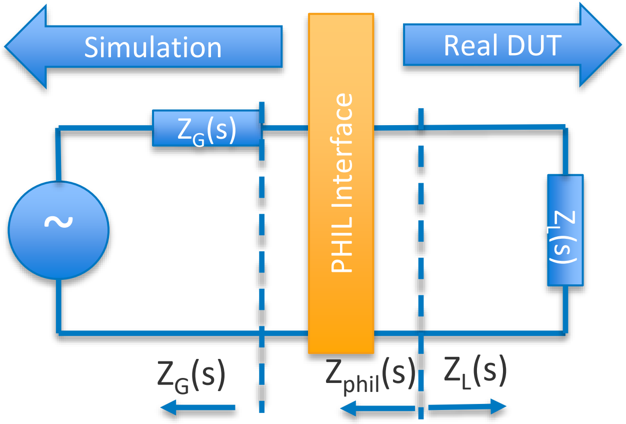


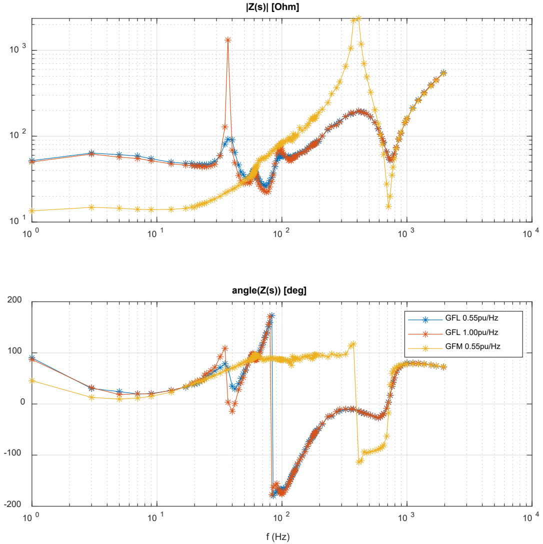




Maui – SAPPHIRE – PHIL



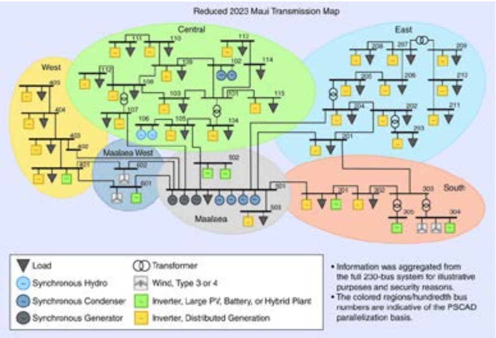




Dynamics of Maui model:

- Above 100 Hz – dominated by input transformer
- Inertia, frequency, and voltage droops information is carried in narrow bandwidth of ~20 Hz
- PHIL high frequency stability can be designed just by knowing input transformer impedance, and it is fixed for all cases.

Simulation bandwidth $BW_{50\%} = 137$ Hz



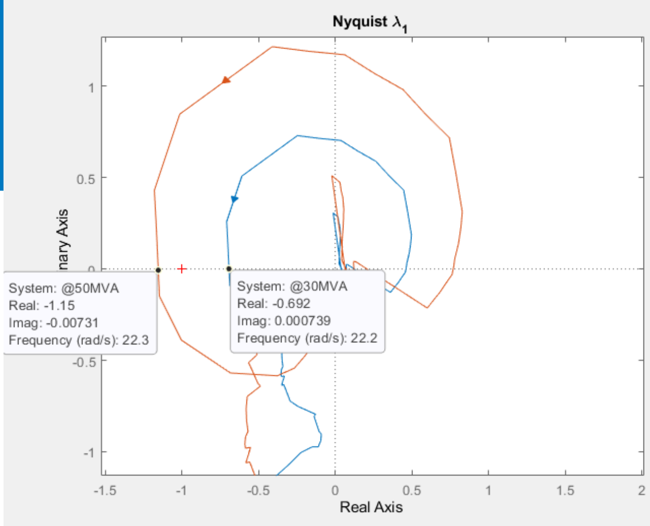
- Information was aggregated from the full 230-bus system for illustrative purposes and security reasons.
- The colored regions/hundredth bus numbers are indicative of the PSCAD parallelization basis.

Oscillation at 22 Hz

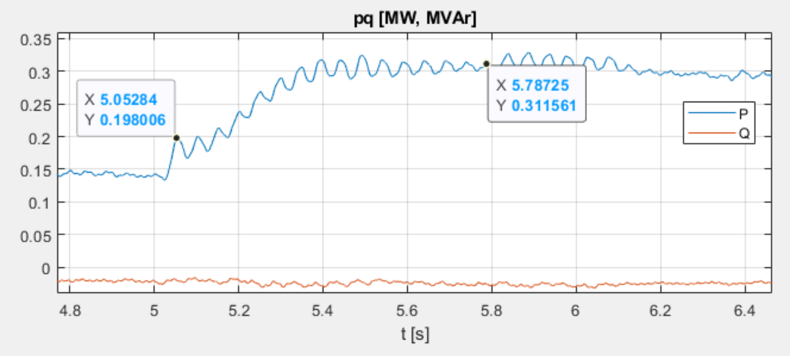
By comparing $Z_G(s)$ and $Z_L(s)$:
At nominal scaling of 30 MW, the plant is stable. Oscillation mode at 22.2 Hz is expected with no PHIL with 3 dB of damping.

In PHIL we measured 20.4 Hz damped oscillation.

Also, the prediction is that if plant was scaled to 50 MVA, the system will become unstable.



Ideal Nyquist plot – no impact of PHIL interface



$F_{osc} = 15/(5.787–5.052) = 20.4$ Hz

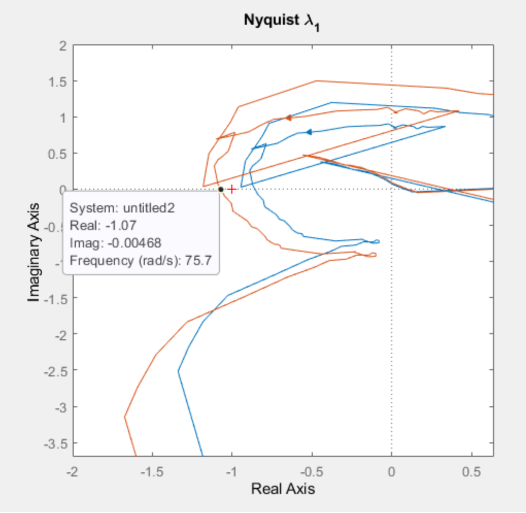
Oscillation at 135 Hz

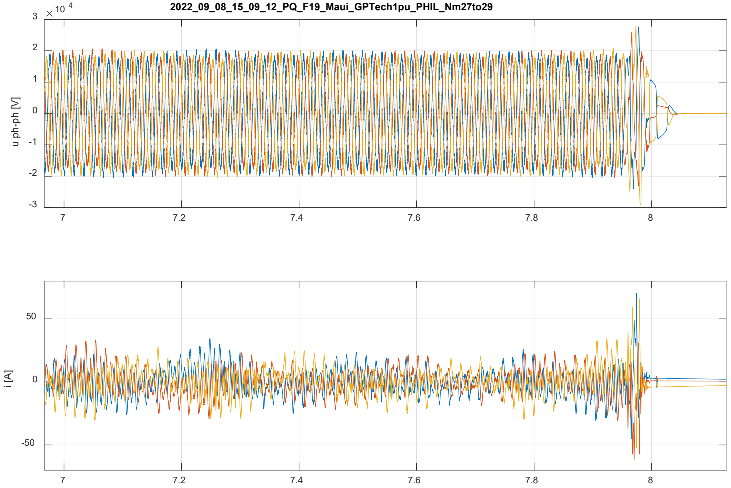
Oscillation mode 1: Aggressive voltage droop

- Inverter based resource operates with aggressive voltage droop – no issue on strong grid
- Ideal stability analysis shows that system will be stable when scaled to 20 MW
- Ideal stability analysis shows that system will be unstable when scaled to 25 MW, and oscillation frequency can be determined from eigenvalue analysis at 135.7 Hz (60 + 75.7).

- When running PHIL and scaling it up from 20 MW to 25 MW, the system went unstable. Fast Fourier Transformation analysis of data show 116 Hz instability.

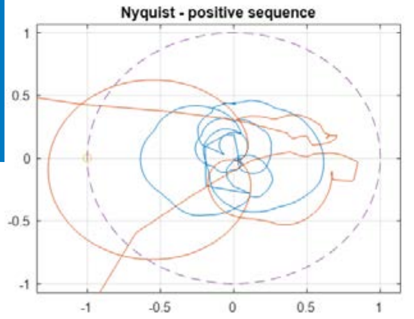
Ideal Nyquist plot – no impact of PHIL interface



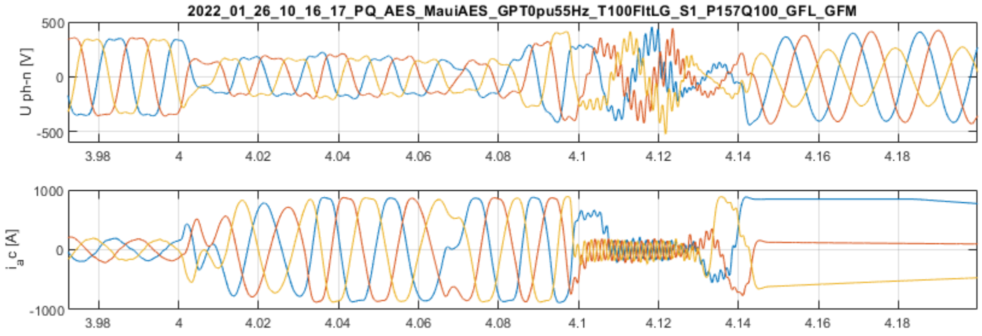


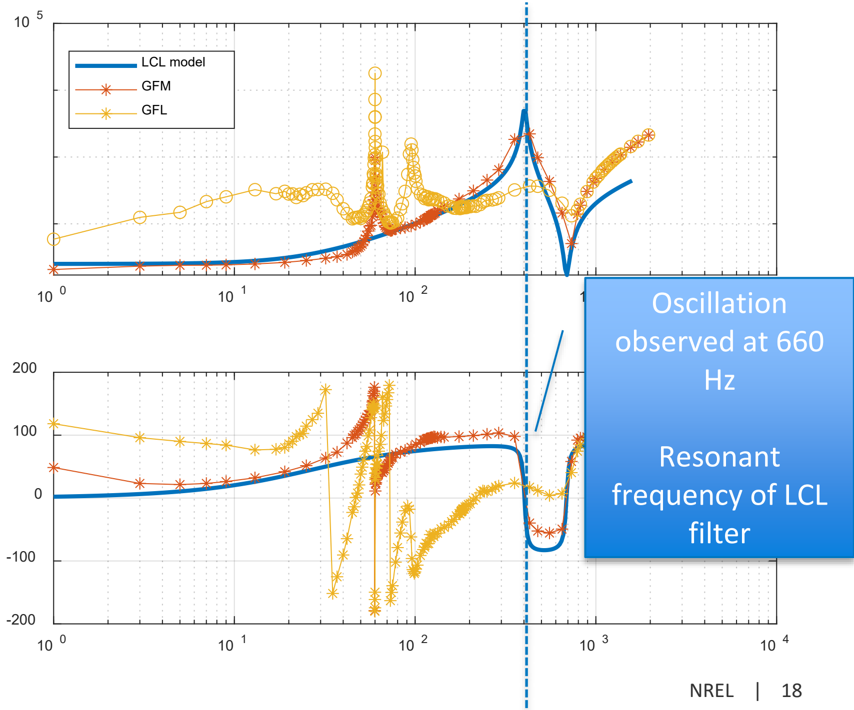
PHIL increasing the power scaling from 21 MVA to 23 MVA

Instability at 660 Hz



- Example of PHIL induced instability at high frequency.
- Filter was designed to be stable using inverter impedance scans – while modulating.
- As soon as inverter stopped modulating its impedance changed to LCL (Inductive-Capacitive-Inductive) filter only, and this was not stable, resulting in 660 Hz oscillation.
- Lesson learned – PHIL stability has to be designed for all possible cases, particularly when inverter is not modulating.





Oscillation observed at 660 Hz

Resonant frequency of LCL filter

Conclusions

- Many PHIL cases are viable, even with considerable delay if properly managed.
- Good understanding of dynamics of PHIL interface is a key to unlocking higher-bandwidth PHIL simulations.
- Bandwidth quantification is proposed using $BW_{5\%}$ and $BW_{50\%}$ measures.

Thank You

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