Impact of Accelerated Stress-Tests on SiC MOSFET Precursor Parameters

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Joseph P. Kozak and Khai D. T. Ngo
Virginia Polytechnic Institute and State University

Douglas DeVoto and Joshua Major
National Renewable Energy Laboratory

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Impact of Accelerated Stress-Tests on SiC MOSFET Precursor Parameters

Joseph P. Kozak* and Khai D.T. Ngo
Bradley Dept. of Electrical and Computer Engineering
Virginia Tech
Blacksburg, VA, USA
*jpkozak@vt.edu

Douglas J. DeVoto, Joshua J. Major
National Renewable Energy Laboratory (NREL)
Golden, CO, USA

***Abstract*— Incorporating SiC power MOSFETs is very attractive for advancing power electronic system performance, yet the system reliability with new devices remains in question. This work presents an overview of accelerated lifetime tests and the packaging and semiconductor failure mechanisms they excite. The experiments explained here includes High Temperature Gate Bias (HTGB), Switching Cycling, Power Cycling, and Thermal Cycling. These experiments stress different failure mechanisms, that show degradation in different device parameters including, but not limited to, threshold voltage and on-resistance. These four experiments help illustrate the spectrum between device and package degradation that can be used to design more reliable power electronic circuits.**

Keywords—Silicon Carbide, MOSFET, Accelerated Testing, Reliability

I. Introduction

The integration of wide-bandgap (WBG) materials into power semiconductor devices is a necessary step to progress power electronics systems to be lighter, smaller, and more efficient. Silicon carbide (SiC) power metal oxide semiconductor field effect transistors (MOSFETs), in comparison to silicon devices, have most notable advantages in electrical breakdown field, thermal conductivity, electron saturation drive velocity, and irradiation tolerance [1]-[3]. In addition, SiC transistors have been shown to be able to operate at higher temperatures (on average at a 25°C higher operating temperature to Si [2]). While the material's characteristics are well known, and significant research has been invested into characterizing SiC MOSFETs for circuit applications, the degradation of these new devices under various operating conditions is not fully understood [4].

This work investigates various accelerated lifetime test (ALT) procedures and discusses their impact on packaging and semiconductor degradation of SiC MOSFETs. Fig. 1 categorizes a spectrum of ALTs by the test's target failure mechanism – packaging-based failure or semiconductor-based failure. While there are other ALTs, the experiments shown here help illustrate the spectrum between device and package degradation under various accelerated test methods.

The left side of Fig. 1 shows experiments that traditionally stress the packaging (extrinsic) failure mechanisms. In this work the package is defined as all components outside of the SiC MOSFET, including die attach material, electrical interconnects, encapsulant, and heat sink. These components are composed of various materials with different coefficient of thermal expansion rates, which causes stresses to develop when the package undergoes thermal changes. Failures within, or between, these components typically occur under accelerated thermal aging, thermal cycling, and power cycling tests due to large temperature swings that permeate throughout the entire package.

The right side of Fig. 1 shows some experiments that are focused on stressing semiconductor (intrinsic) failure mechanisms. A major weakness within the semiconductor itself is the crystallographic mismatch at the interface of the SiC-SiO_2 layers in the MOSFET. This interface region consists of numerous trap charges including – interface traps, oxide traps, fixed charges, and mobile ions [5], [6]. Under various energy profiles, these charges can shift the threshold voltage (V_{th}) of the device. In addition to shifting V_{th}, time-dependent dielectric breakdown caused by Fowler-Nordheim tunneling can greatly weaken the oxide layer of the MOS structure degrading the semiconductor performance itself [7].

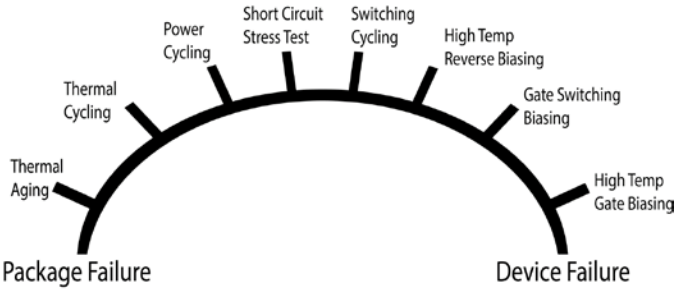

Fig. 1 Accelerated lifetime test spectrum.

This work surveys the effects of two semiconductor-based and two packaging-based lifetime experiments on SiC

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MOSFETs. Section II explores work focusing on high-temperature gate bias (HTGB) experiments [5]-[9] and Switching Cycling [10]. Section III inspects package level degradation from both Power Cycling experiments [11]-[15], and Thermal Cycling experiments [10], [16], [17]. The effects and changes of different device characteristics are discussed, with a focus on V_{th} and ON-resistance (R_{DSon}).

II. Semiconductor Focused Lifetime Tests

A. High Temperature Gate Bias

One of the most sensitive areas of the MOSFET structure is within the gate oxide layer. Significant research has gone into better processing techniques and reliability of the gate oxide, especially for SiC devices [18]. This is in part because of the greater crystallographic mismatch between SiC and the SiO_2 oxide in comparison to Si [19]; in addition, the wider bandgap of SiC allows for more Fowler-Nordheim tunneling current to take place [7]. To test the resilience of the oxide layer, a HTGB experiment can be conducted.

This HTGB experiment raises the temperature of the semiconductor device to a stressful state, generally between 125°C and 175°C for SiC [7]. Under these conditions, a high electric field is applied onto the gate of the MOSFET (with the upper limit near 3MV/cm) to stress the oxide layer within the device [5], [7], [9]. After a predetermined time, measurements of the device characteristics can be taken to observe the full effects of the electric field, which can most predominantly be seen by shifts in threshold voltage. Another experimental profile is shown in Fig. 2 where a device is stressed under both a positive and negative bias for set amounts of time (t_{soak}). A common technique when rotating between the two stress-bias voltages is to ramp the voltage up/down to the $+V_{GS}$ or $-V_{GS}$ values. This will minimize degradation and excessive trap charge states [5], [9]. Fig. 3-6 shows degradation effects from different HTGB experiments. The main degradation is trap movement at the oxide interface and can be observed in shifts within the threshold voltage and semiconductor related parameters and less on packaging related parameters.

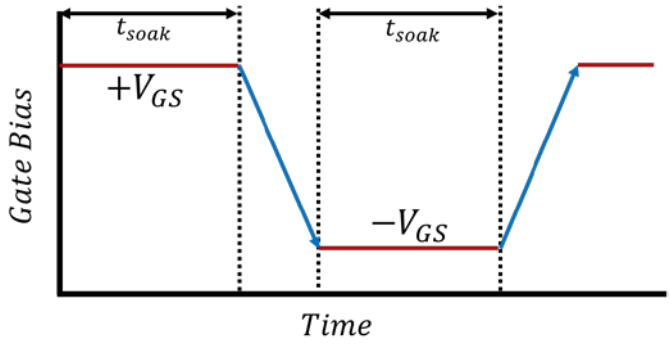

Fig. 2 HTGB experiment showing the soak times for both a $+V_{GS}$ and $-V_{GS}$ bias, with ramping voltages between the two bias values [6].

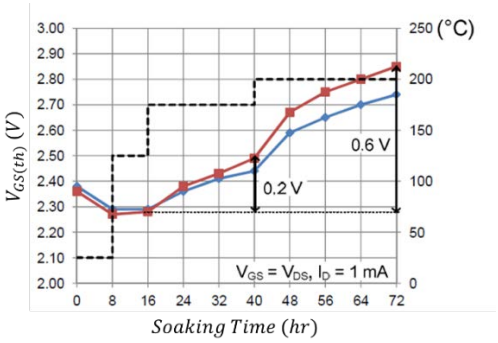

Fig. 3 Static V_{th} measurements after HTGB tests in [7].

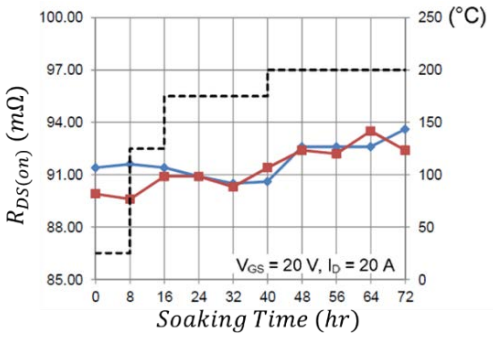

Fig. 4 Static R_{DSon} measurements after HTGB tests in [7].

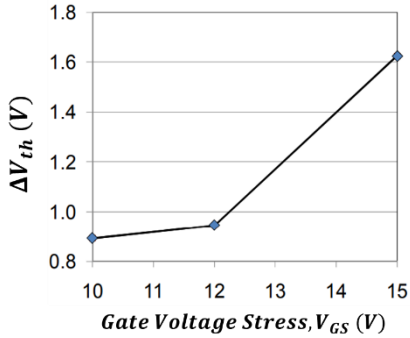

Fig. 5 Dependence of V_{th} shifts on stress bias for devices with T = 150°C and t = 1 hour [8].

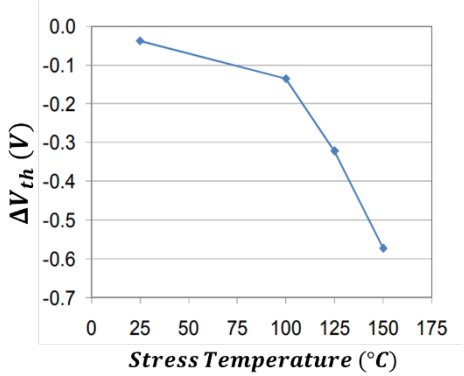

Fig. 6 Dependence of V_{th} shift on stress temperature for devices with V_{GS} = 15V, t = 1 hour [8].

B. Switching Cycling

The HTGB experiments are focused on stressing the gate oxide and semiconductor itself through a high electric field on the gate terminal. This high electric field is held at a steady state, DC-bias. Under normal converter-oriented, operating conditions, the electric field is transient through the switching events. To stress the oxide and semiconductor under parameters closer to normal operating conditions, Switching Cycling has been introduced [10]. A variation on HTGB and high-temperature reverse bias (HTRB) testing [20] (not detailed in this work), Switching Cycling applies a DC-bias across the drain-source of the device while switching the device on/off continuously.

The device under test (DUT) is placed in a clamped, inductive switching circuit and switched continuously. A high Drain-Source voltage (V_{DS}) equal to 90% of the breakdown voltage is applied onto the device generating a high electric field similar to HTRB experiments. The DUT is then switched on and off continuously stressing the device primarily through the transient electric field generated by switching events. The on-time is set to 150 nanoseconds to decrease conduction losses and self-heating effects in the device. Fig. 7 shows the continuous switching nature of the Switching Cycling experiment in [10].

The electrical parameters that have shown most changes from Switching Cycling includes output characteristics, transfer characteristics (including V_{th}), Drain-Source leakage current, and Gate-Source leakage. Fig. 8-11 show these changes over time. The primary degradation can be seen on the semiconductor with the large shift in V_{th}, Drain-Source leakage current, and Gate-Source leakage current. Packaging-based degradation is minimal, as can be seen in the small shift in R_{DSon}.

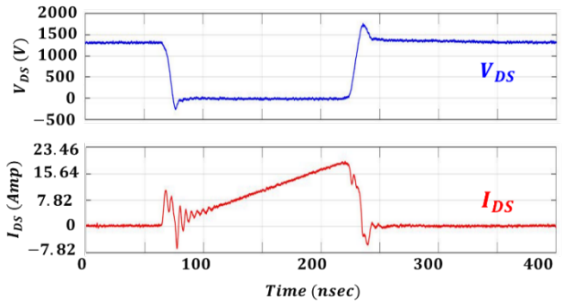

Fig. 7 V_{DS} (top) and I_{DS} (bottom) waveforms from Switching Cycling as explain in [10].

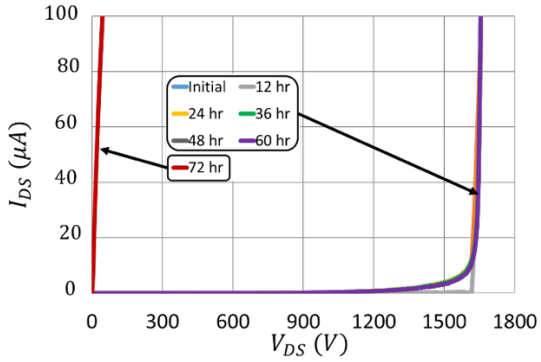

Fig. 8 Changes in Drain-Source leakage current over time as a result of Switching Cycling.

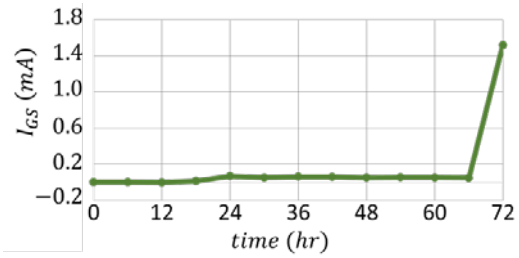

Fig. 9 Changes in Gate-Source leakage over time as a result of Switching Cycling.

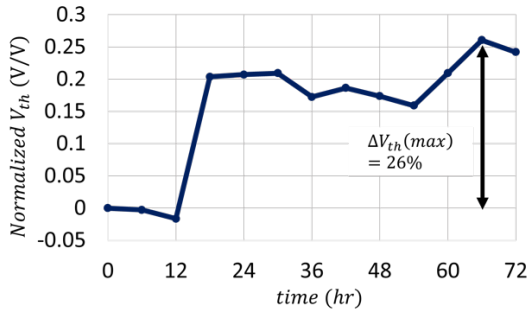

Fig. 10 Normalized V_{th} changes over time as a result of Switching Cycling.

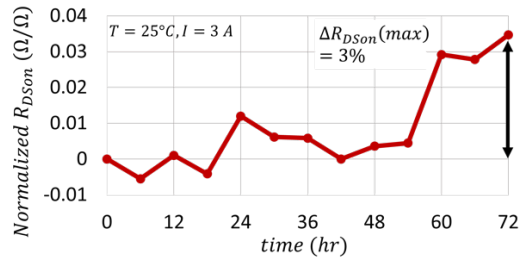

Fig. 11 Normalized R_{DSon} changes over time as a result of Switching Cycling.

III. Packaging Focused Lifetime Tests

A. Power Cycling

Power Cycling experiments focus on the package degradation of a device exploiting the different coefficients in thermal expansion of the packaging layers. A large change in temperature (ΔT) [21] causes these different layers to expand at different rates creating a mechanical stress throughout the packaged device [11], [12], [14], [15]. The ΔT is generated through the self-heating effects (conduction losses) from a Drain-Source current flowing through the DUT [14]. The case or device temperature is monitored and current flows through the device until a designated maximum temperature is reached. A constant current source and control device are used to turn the current on/off through the device and is described in more detail in [11]-[13], [22], [23]. In the off-state, the DUT operating temperature is monitored and the system is held off until the lower bounded temperature is reached. The experimental rate of the heating and cooling periods can be designed to match different industry applications [11], [12] through current magnitude, and cooling systems. A general power cycling temperature profile is shown in Fig. 12, where t_{on} represents the time the current conducts through the device, and t_{off} when the device is in the off-state.

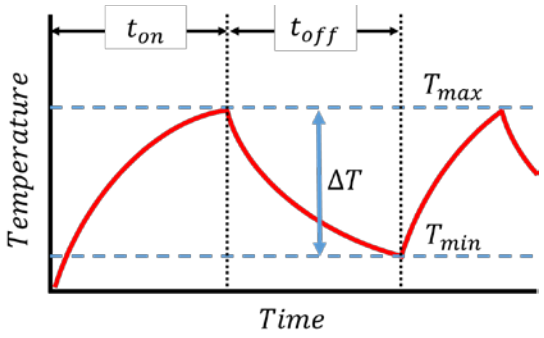

Fig. 12 General temperature stress profile for Power Cycling.

This thermal profile applies a mechanical stress throughout the packaged device. The most common degradation through Power Cycling includes wire-bond lift-off, and solder degradation. Wire-bond lift-off can be best seen through a large step change in R_{DSon}, [11]-[13], [22]. Solder degradation can be seen by incremental changes in R_{DSon} [12],[14], as well as changes in thermal resistance (Z_{th}) [11], [13], [14], [23]. While the temperature rise of the device is caused from the conduction losses through the device there is little degradation of the intrinsic nature of the semiconductor itself. Degradation depicting the changes in R_{DSon} from wire-bond lift-off and V_{DS} from wire bond lift-off and solder degradation are shown in Fig. 13 and Fig. 14.

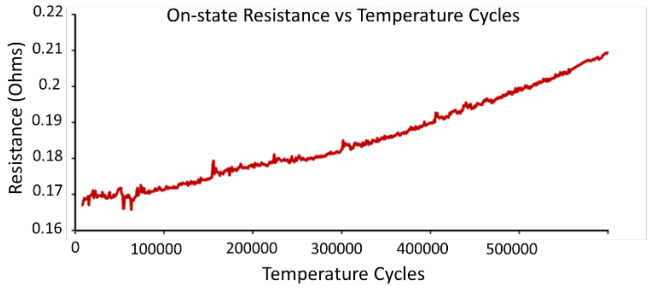

Fig. 13 On-resistance evolution through accelerated test in [15].

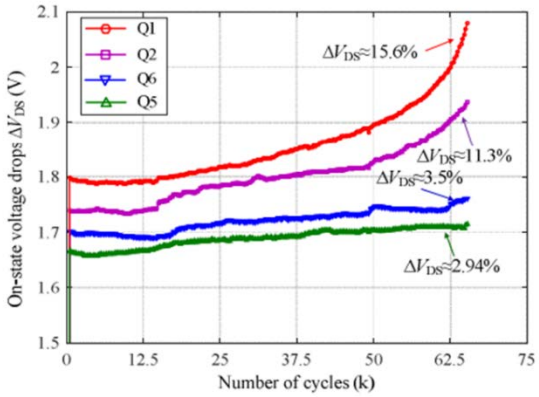

Fig. 14 Measured on-state voltage drop and fitting curves for devices during power cycling tests in [24].

B. *Thermal Cycling*

Similar to Power Cycling, Thermal Cycling stresses the interconnections of packaging layers (solder joints, wire bonds, etc.) through the mismatch in the coefficients of thermal expansion [17], [24]. Unlike Power Cycling however, the ΔT is generated completely through external means such as a hot plate or thermal shock chamber and not the conduction losses of the device [17]. As a result the T_{ave}, T_{min}, and T_{max} can be controlled with more precision and used to excite different failure mechanisms. It has been shown in [24] that the chosen ΔT range and Tave have a large effect on the degradation of the device. Fig. 15 shows a generic thermal cycling experimental profile including the rise and fall times, as well as the dwell/soak time at T_{max} and T_{min}.

The work conducted in [10] involved an experimental temperature profile that had a T_{min} of -40°C, T_{max} of 175°C and ΔT of 215°C. The rise and fall times were 10 minutes each with both the high and low temperature dwell times set to 10 minutes. Fig. 16 and Fig. 17 show changes in the R_{DSon} and V_{th} parameters. Fig. 17 shows that the changes in V_{th} are minimal and Fig. 16 [10] shows a 44% R_{DSon} change from its initial value after 2,000 cycles. These results, along with those shown in [17], depict that Thermal Cycling is set to degrade the device package as opposed to the semiconductor device itself.

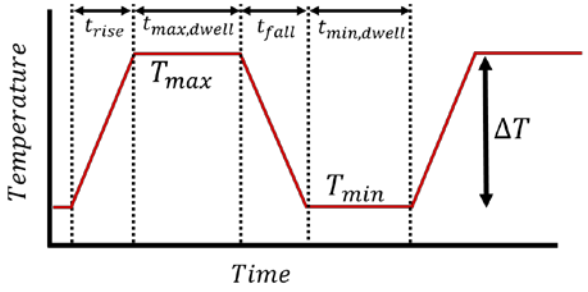

Fig. 15 General Thermal Cycling temperature profile.

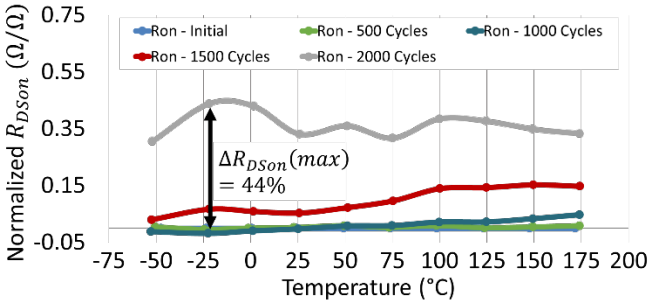

Fig. 16 Normalized changes of R_{DSon} over time from Thermal Cycling [10].

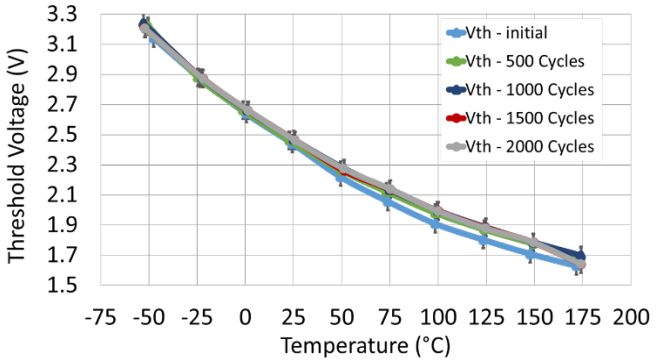

Fig. 17 Changes in V_{th} over time from Thermal Cycling [10].

IV. Conclusion

SiC power MOSFETs have demonstrated properties that can enhance power converter performance over traditional technologies. The reliability of SiC MOSFETs have remained in question and ALTs have only begun to show the results necessary to qualify the technology. Table I summarizes the four test methods described in this work. It also shows the ALT main stress mechanism (package or semiconductor), the system-level parameter in which changes are seen, and a general length for failure to mature. These tests all show how a packaged semiconductor survives under extreme conditions that are much harsher than industry-standard, operating conditions.

TABLE I
Accelerated Lifetime Experiments and Associated Stress Mechanisms

ALT	Stress Mechanism	System Level Parameter	Time to Failure
HTGB	Semiconductor	V_{th}	1000+ hours
Switching Cycling	Semiconductor	V_{th}	100 hours
Power Cycling	Package	R_{DSon}, Z_{th}	100-1000+ hours
Thermal Cycling	Package	R_{DSon}	1000+ hours

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