A Techno-economic Look at SiC WBG from Wafer to Motor Drive

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Presentation Outline

1. Techno-economic Analysis
2. SiC Project Overview
3. Current Global Supply Chain
4. Bottom-Up Cost Modeling
5. Wrap-up

Project funded by the DOE Advanced Manufacturing Office (AMO)

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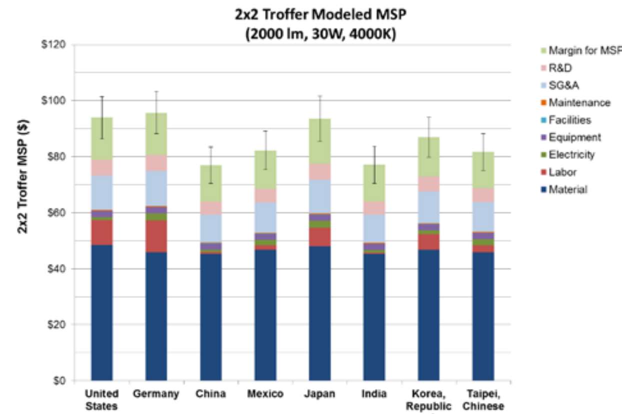
CEMAC Description

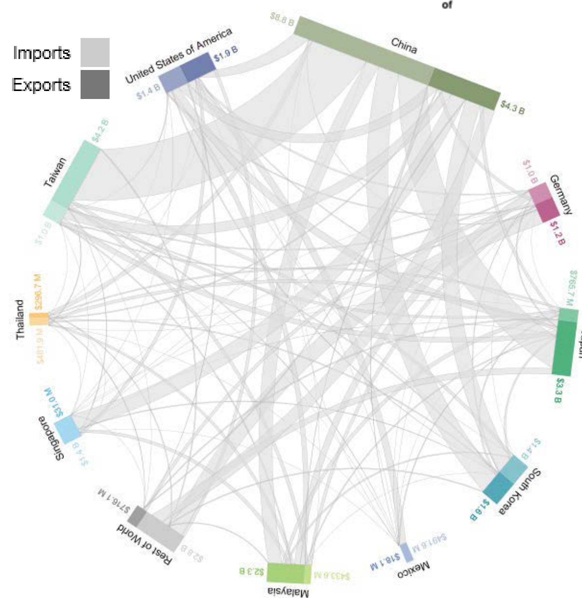
CEMAC
The Clean Energy Manufacturing Analysis Center

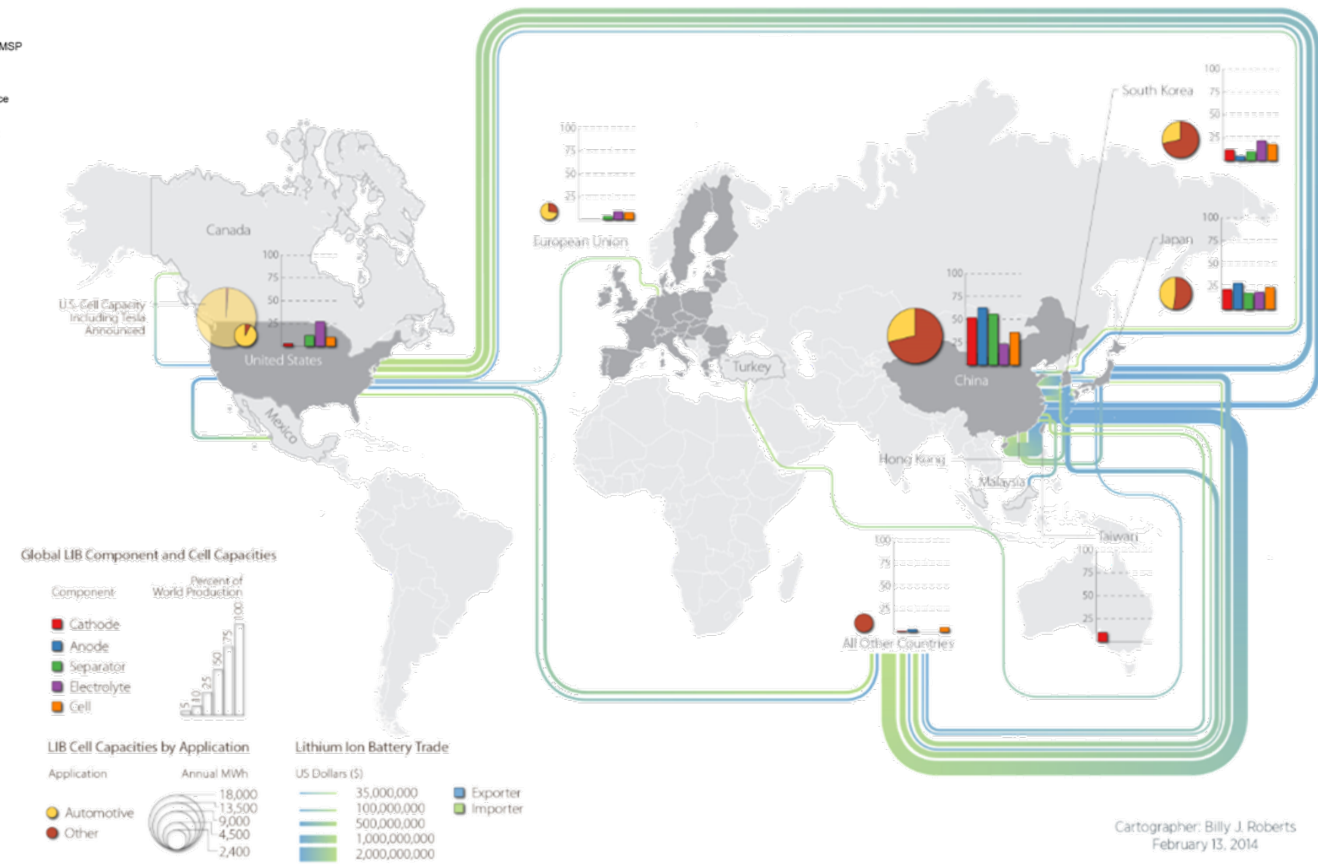
Clean Energy Manufacturing Analysis Center provides objective supply chain analysis to inform research and investment in the development of clean energy technologies

Types of analysis include:

1. Supply chain overview and analysis
2. Bottom-up manufacturing cost analysis
3. Technology analysis for manufacturing
4. Site selection support and dynamic modeling







Website: www.manufacturingcleanenergy.org

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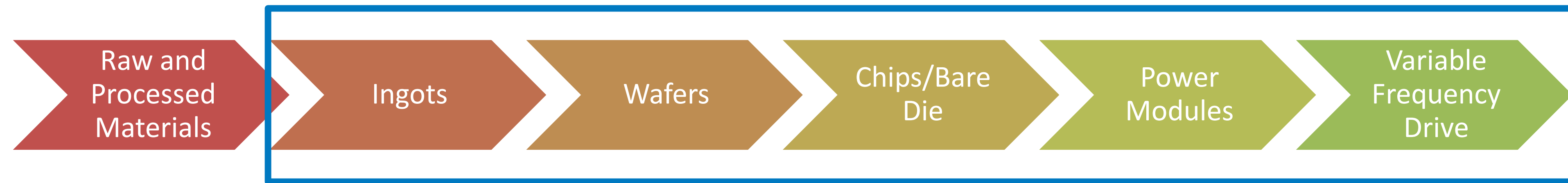
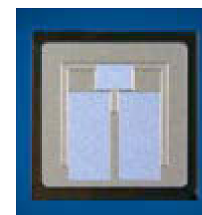
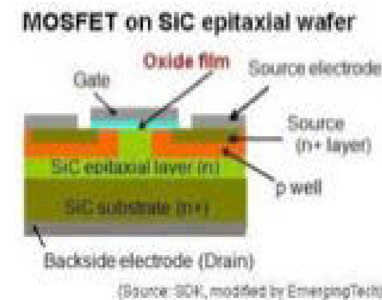
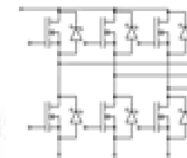
SiC Project Overview

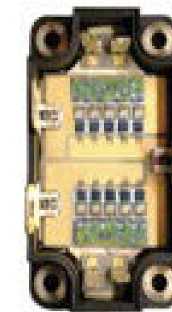
Simplified Value Chain for Variable Frequency Drive











- Focusing on the SiC value chain
- 3.3kV devices and power modules
- Applications to medium-voltage, industrial variable frequency drives (VFDs)
- Near-term designs

Wide Band-gap Project Takeaways

- WBG and specifically SiC adoption is growing

- The U.S. has a dominate position in wafer and device manufacturing
  - Power module manufacturing is done globally with a concentration in Asia regions
  - Medium voltage drive manufacturing tends to concentrate closer to the end user

- Material costs dominate bottoms-up cost models
  - SiC Wafer : >40% $1228-$1496/6’’ wafer
  - Devices>50%
    - SiC Diode -> $4.86-$5.03/unit
    - SiC Mosfet -> $1.67-$1.73/unit
  - SiC IGBT styled module : >60% $279-$291/module

- Multiple scenarios show the path to lower costs through the value chain

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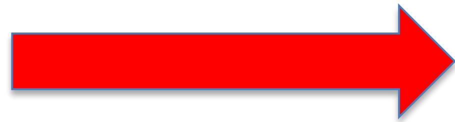

3. **Current Global Supply Chain**
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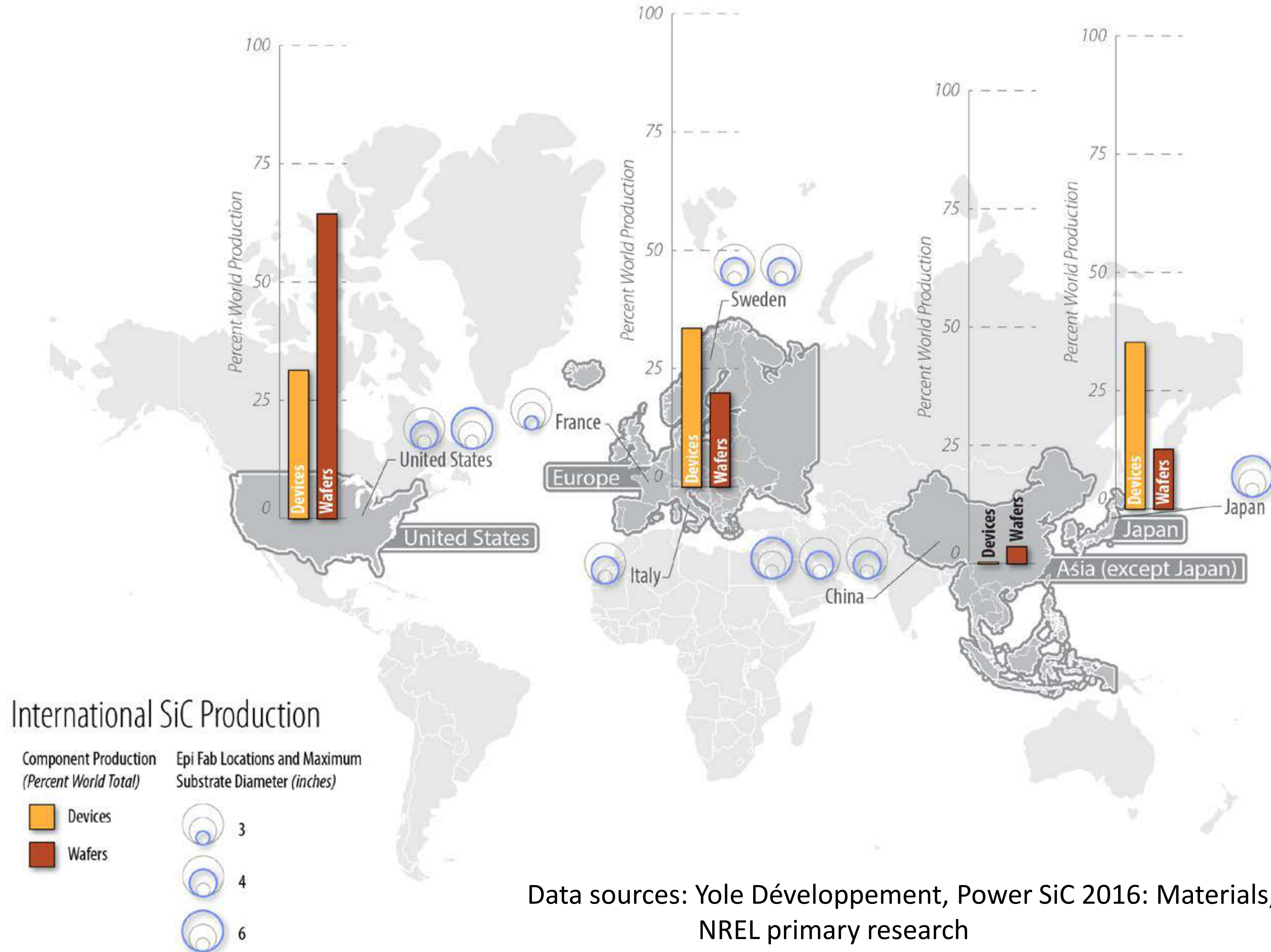
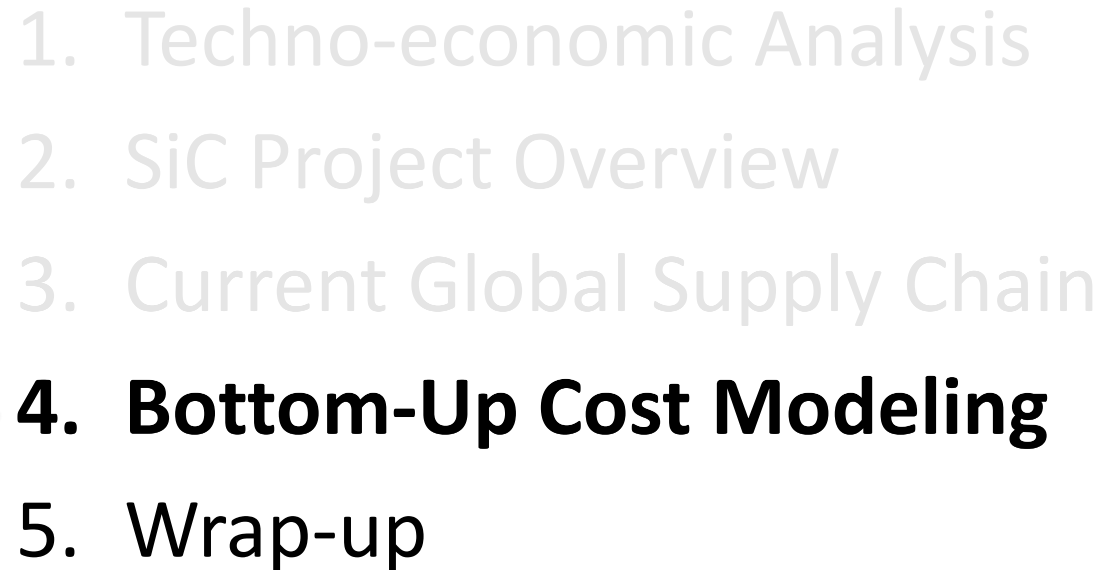
Current Global Supply Chain

Wafers, Epitaxy, and Chips



Data sources: Yole Développement, Power SiC 2016: Materials, Devices, and Applications; NREL primary research



Bottom-Up Cost Modeling

Regional Manufacturing Costs and Modeling Assumptions

- Manufacturing cost modeling base case
  - Models the effect of core country factors:
    - Labor rates
    - Electricity prices
    - Effective corporate tax rates
  - In this early-stage industry — particularly for upstream components — manufacturing competitiveness is less driven by core country factors, but this may change over time

- Economic modeling assumptions for all countries:
  - Same cost of debt and equity, D/E ratio
  - Same production volumes, yields, and wafer diameter
  - No subsidies
  - Assumes the same knowledge/capability of firms
  - Assigns the same risk associated with firms regardless of country
  - Wafer model assumes 100% capacity utilization

- MSP is the minimum sustainable price that a company must sell its product for in order to pay back the capital and operating expenses during the plant lifetime

SiC Epi-Wafers

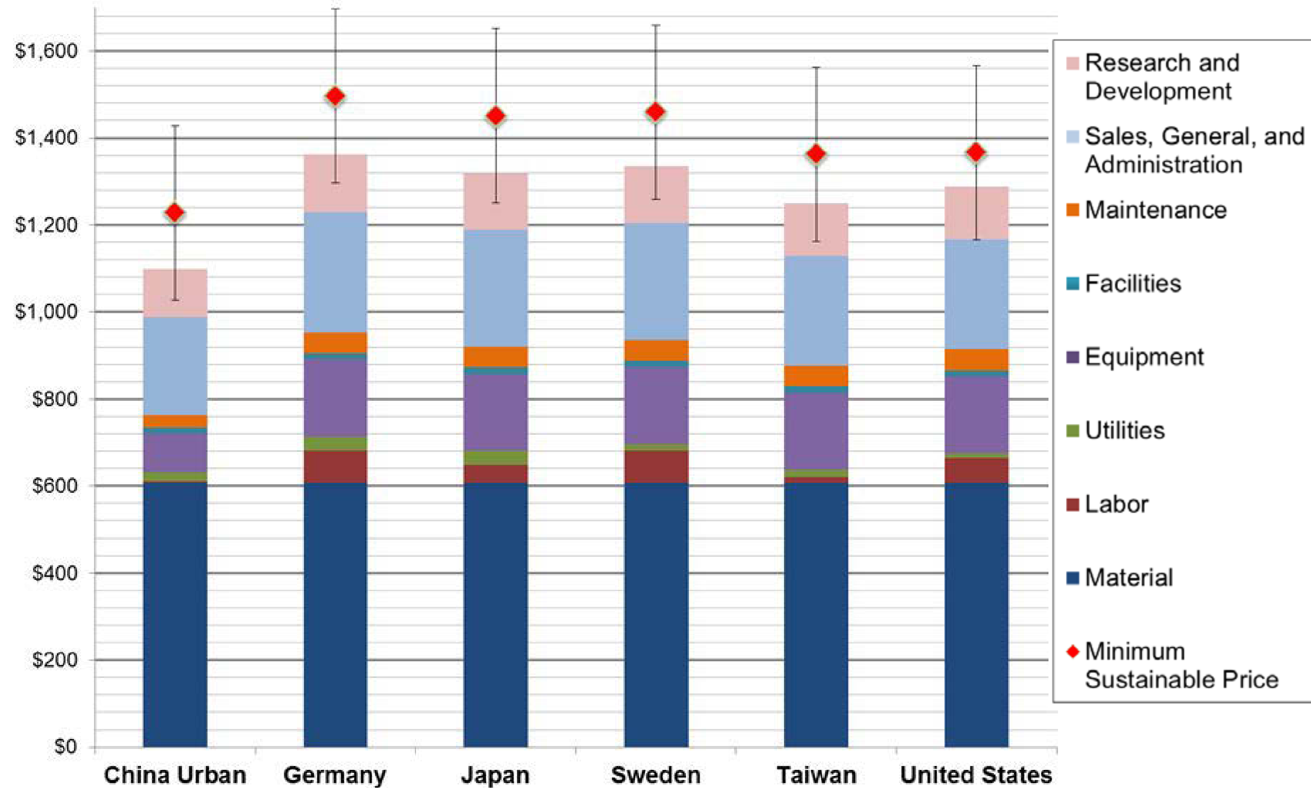
Substrates and Epi-Layer

For use in 3.3kV devices

5,000 6’’ wafers/month manufacturing capacity

Modeled SiC Epi-wafer

Base Case Results for SiC Wafers



MSP per wafer: $1228-$1496/unit

- Key cost drivers include:
  - Materials
    - High cost of high purity SiC powders for boule growth
    - High cost of consumables associated with wafering and polishing (diamond slurry, diamond wire, polishing pads)
  - Yield
  - Throughput of the boule (crystal) and epitaxial growth steps (key driver of equipment costs)
- Overhead costs will likely decrease as the industry scales and matures

- Regional differences in MSP are largely attributed to:
  - Labor cost differences, even for this highly automated scenario
  - Differences in overhead costs: SG&A, R&D, and taxes

SiC Chips

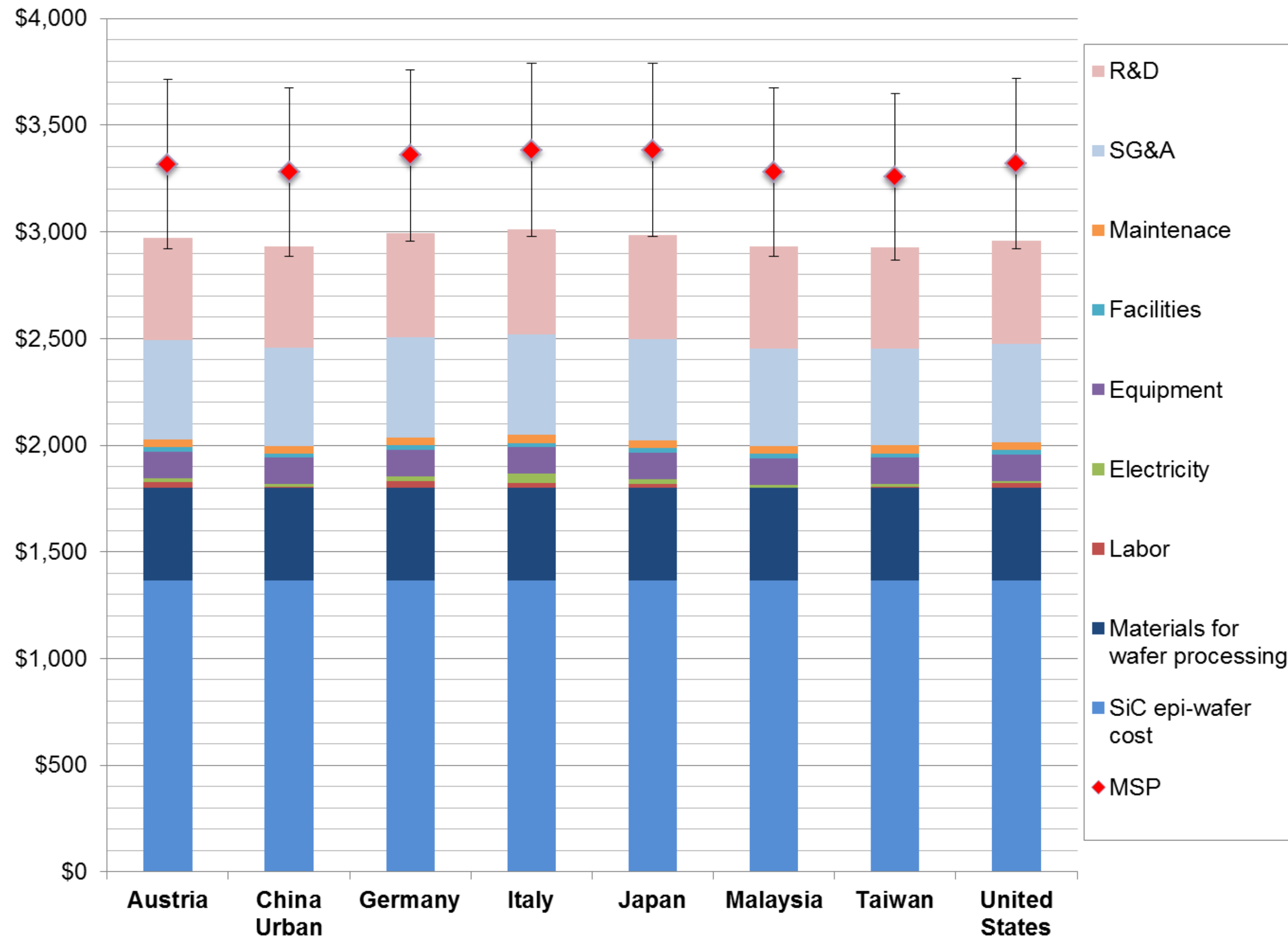
MOSFETs and SBDs

3.3kV devices

5,000 6’’ wafers/month manufacturing capacity

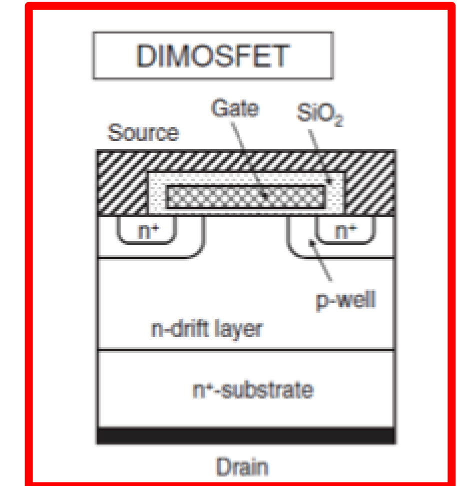
Base Case Results for SiC MOSFET Chips

- Labor has little impact on overall cost – wafer price constitutes the majority of manufacturing costs, process is highly automated, overhead costs are high
- Equipment and facilities costs dominate the wafer processing costs



8mm^2 chip area assumed

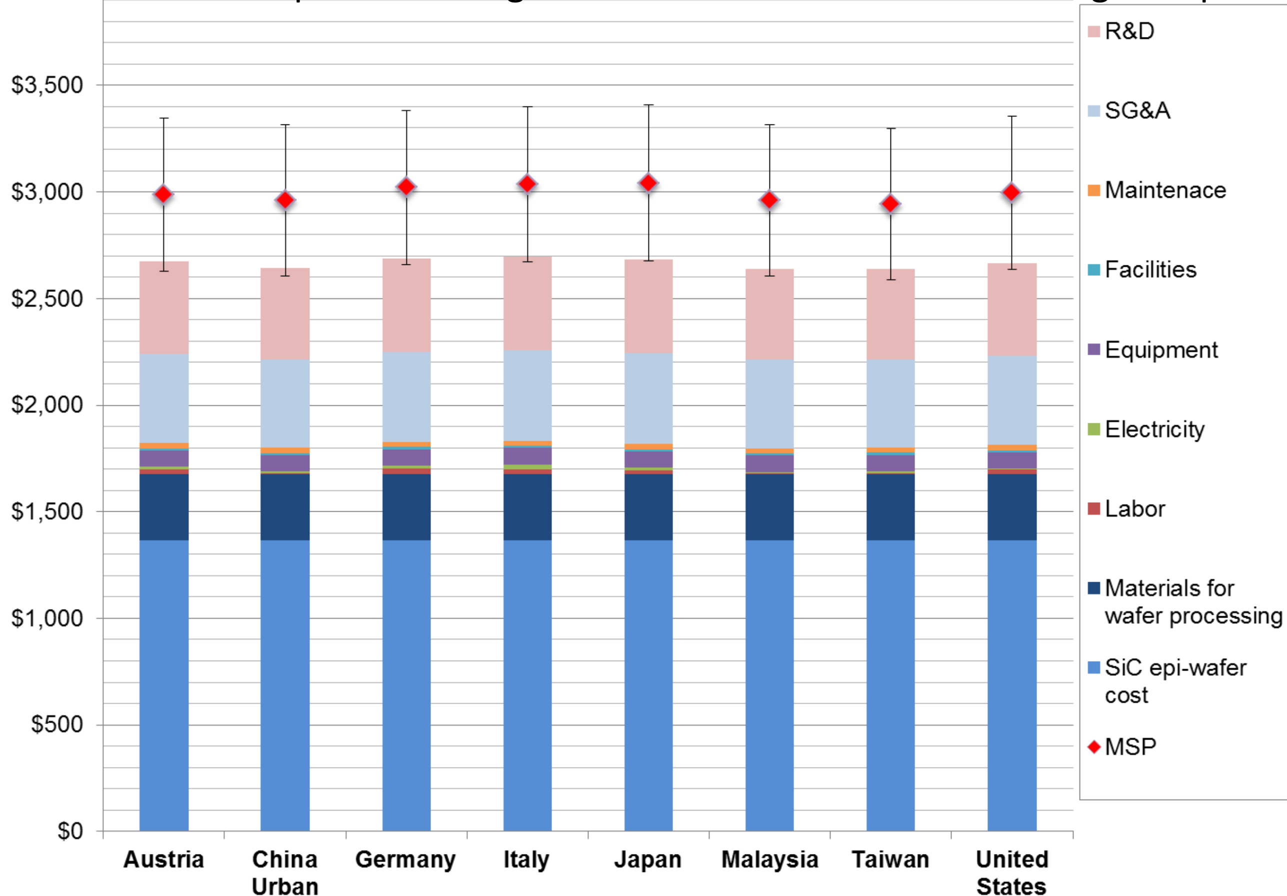
- MSP per chip: $1.67-$1.73/unit
- Calculated wafer processing cost for MOSFET chips: $320-$380/6" wafer

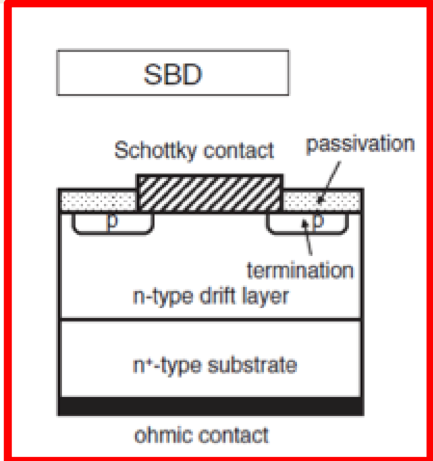


Source: Jpn. J. Appl. Phys 54, 040103 (2015)

Base Case Results for SiC SBD Chips

- Labor has little impact on overall cost – wafer price constitutes the majority of manufacturing costs, process is highly automated, overhead costs are high
- Equipment and facilities costs dominate the wafer processing costs
- Processing costs are lower per area for the SBD diode compared to the MOSFET — the device is simpler and there are fewer processing steps are required.
  - Per chip costs are higher because we assume a much larger chip size





Source: Jpn. J. Appl. Phys 54, 040103 (2015)

25mm² chip area assumed

- MSP per chip: $4.86-$5.03/unit
- Calculated wafer processing cost for SBD chips: $190-$230/6” wafer

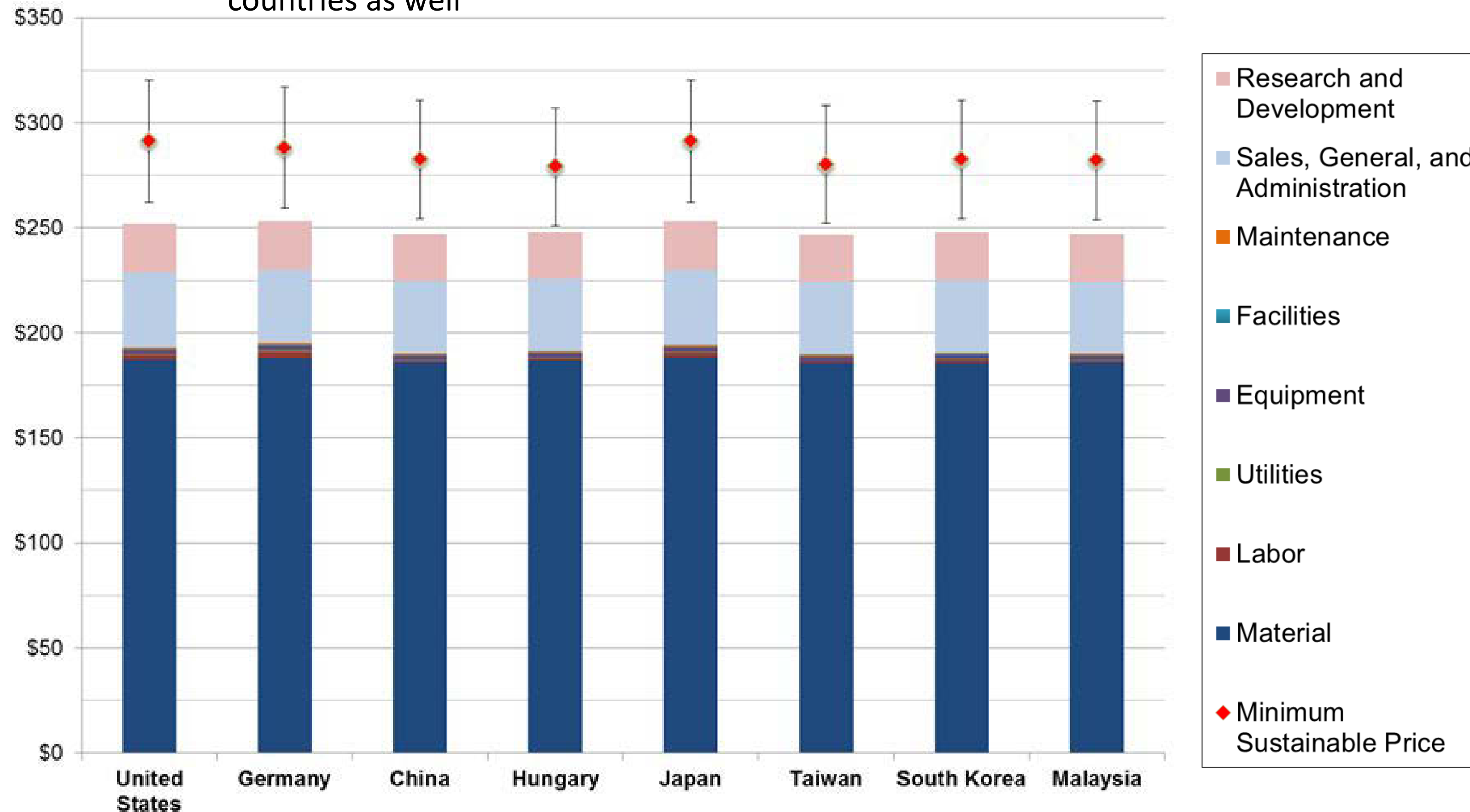
SiC Power Modules

3.3kV, based off a modified 1.7kV design, similar to IGBT module

1 million/year production volume

Base Case Results for SiC Power Modules

- Labor has little impact on overall cost, process is highly automated
- Equipment and facilities costs are also small at these production volumes
  - Specialized equipment is not required for near-term – can leverage existing packaging facilities/contract manufacturers
- SBD and MOSFET chip cost constitute a significant material cost- ~46%
  - Model used the model SBD and MOSFET chip MSP from the same region
    - i.e. If chips were made in the U.S., the model used U.S. chip prices for the module. However, in reality, the chips may be sourced from other countries as well

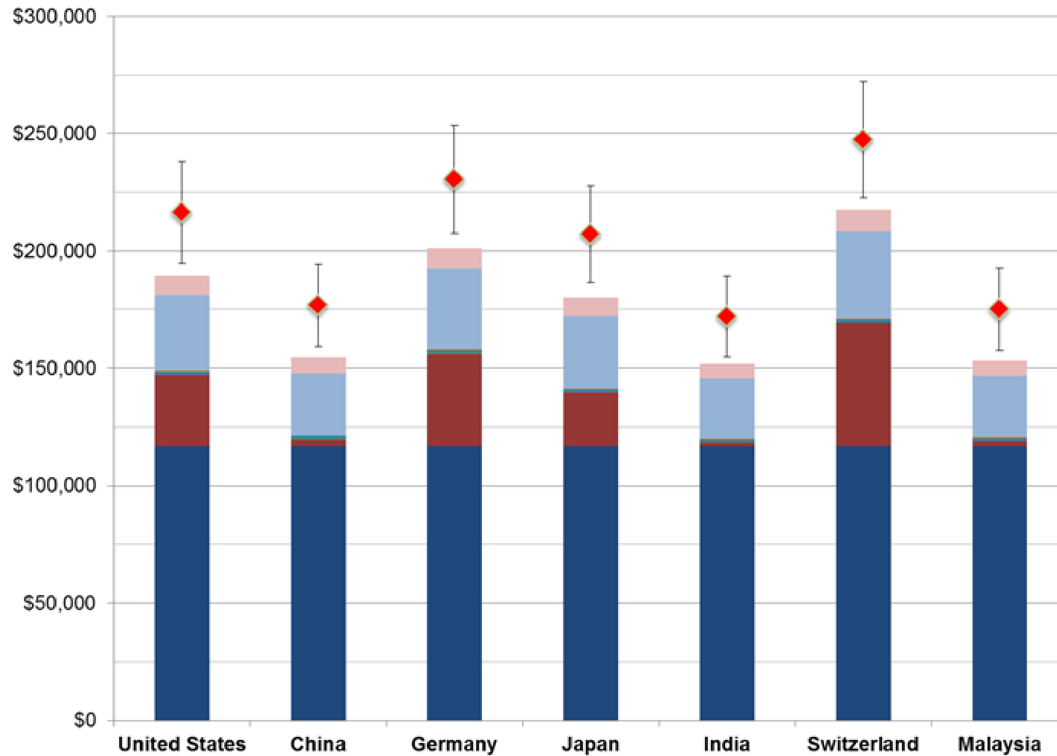


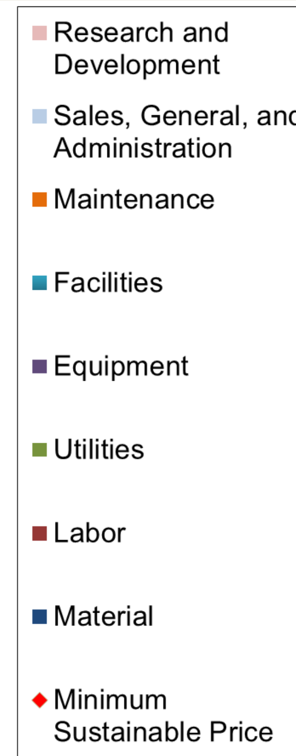
MSP per module: $279-$291/unit

SiC-Based VFD

1 MW drive, 45 3.3kV power modules

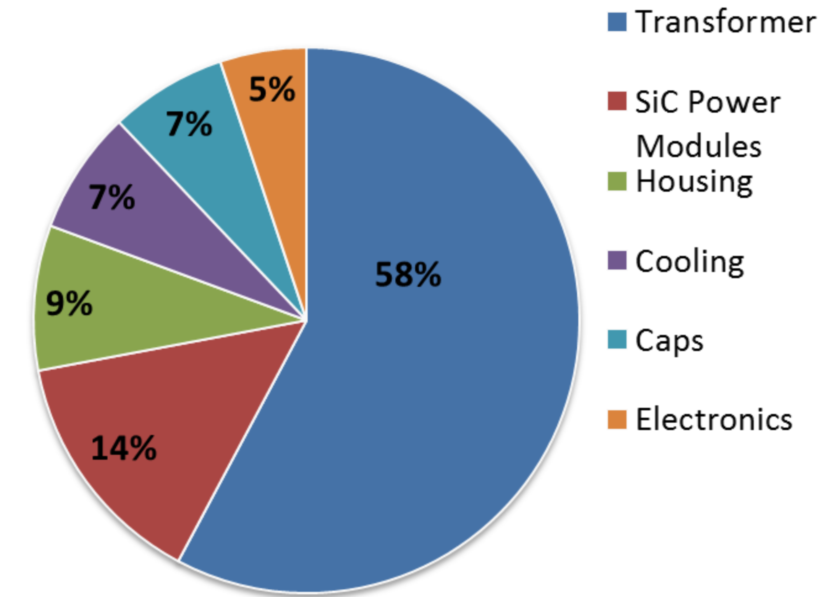
Base Case Results for SiC-based 1MW VFD*





*Hypothetical, no known products available on the market

MSP per drive:
$170K-$200K/unit



- Materials costs dominate overall manufacturing cost ~+70%
  - Dominated by transformer costs followed by power module costs
  - Model used the modeled power model MSP from the same region
    - i.e. If module s were made in the U.S., the model used the U.S. module MSP. However, in reality, the chips may be sourced from other countries as well
- Labor Costs ~17%
  - Assumes 8 weeks of construction with 3 labors (40 hours work week)
- Shipping costs for VFD devices are typically only 1-2% of the total cost
  - VFDs are manufactured closer to the end user to provide access to support and development without requiring intermediaries

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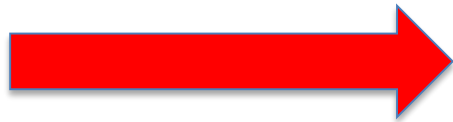


5. **Wrap-up**

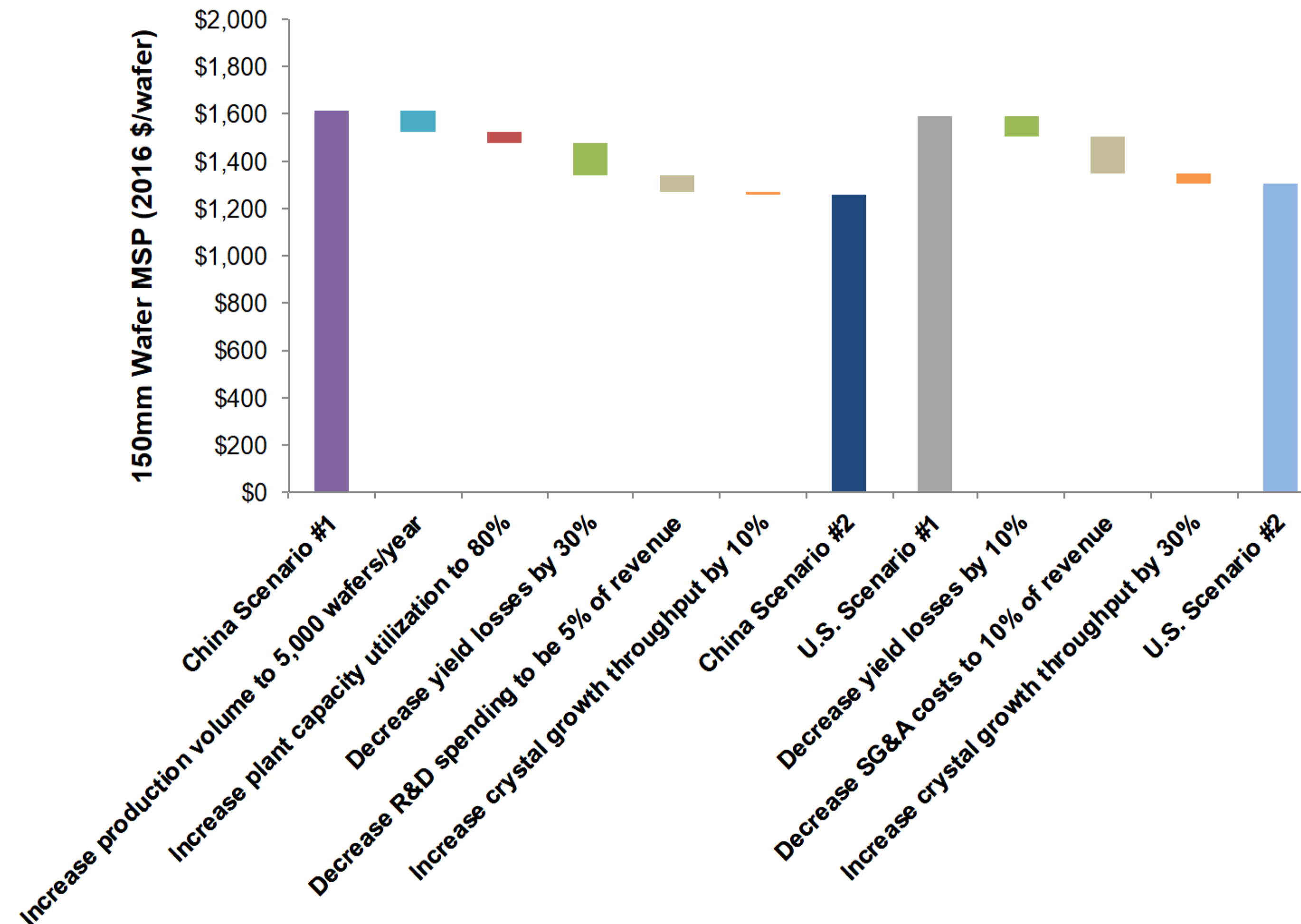
Scenario Analysis

Analysis Value

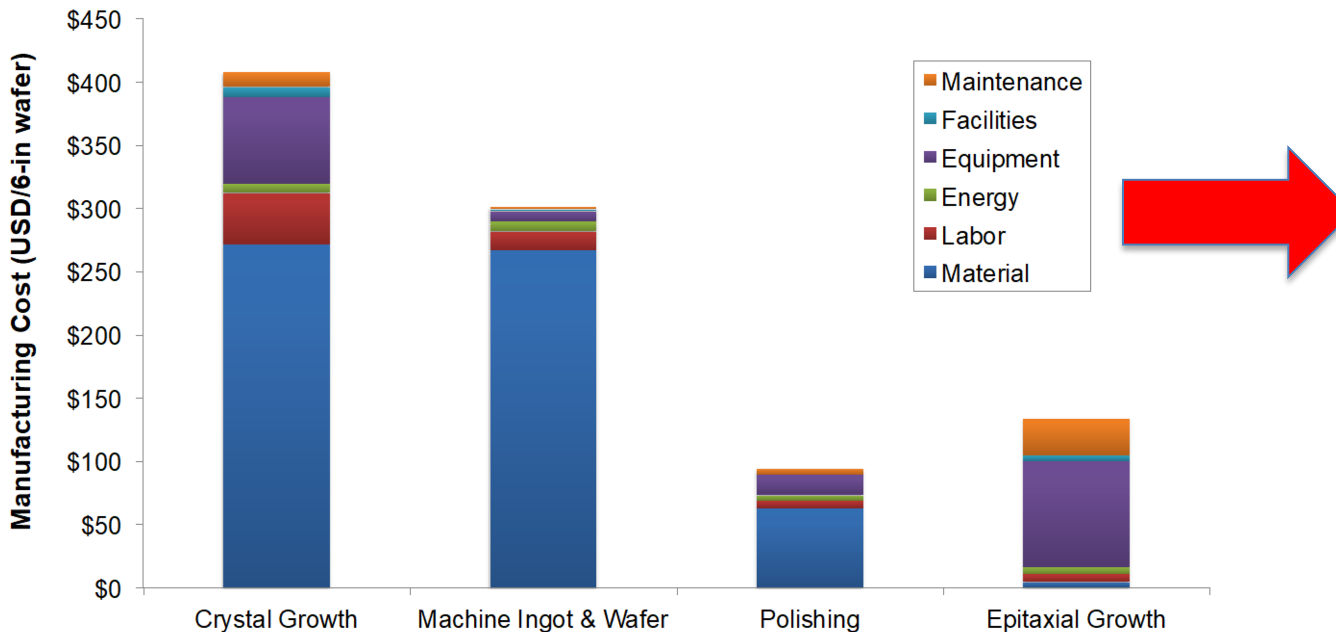
- Examine supply chain to identify potential material limitations before years of research leads to a non-sustainable breakthrough
- Identify areas of research interest based on cost
  – Run scenarios showing impact of research
- Provide support for proposals
  – Cost data showing how a research advancement could effect manufacturing costs
- Help companies understand the impact of change to their product on the overall value stream
- Explore scenarios showing paths to cost reduction

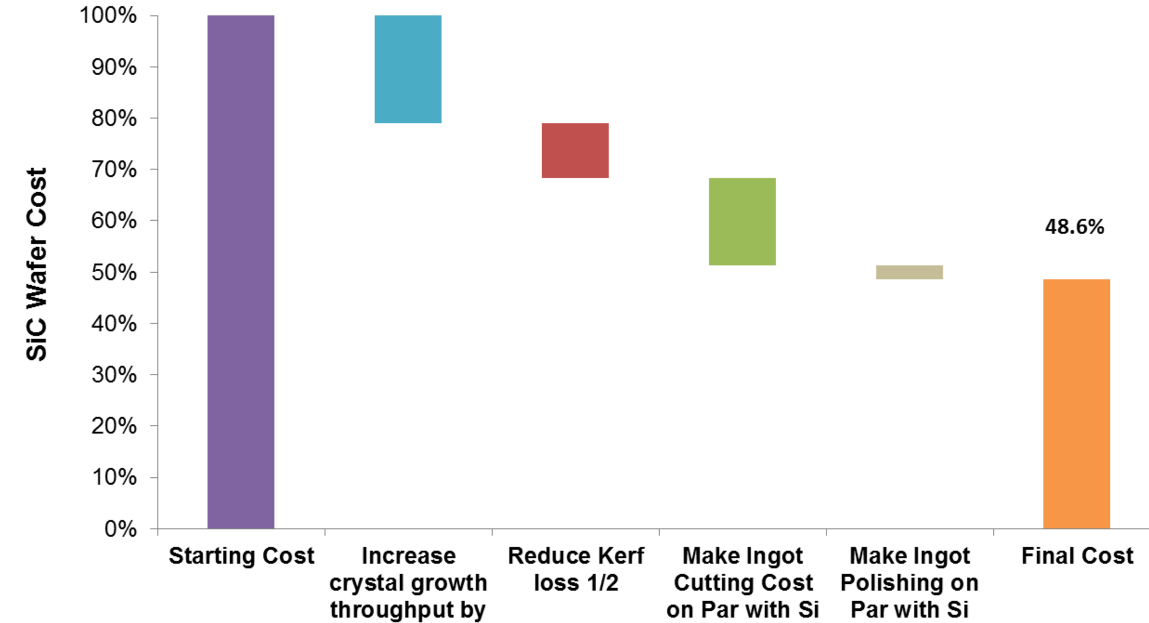
Regional Wafer Costs Reduction Scenario

- There are multiple pathways a country could pursue to achieve similar costs, including technical/engineering advancements, policy changes, and changes in business strategy
- An example scenario is shown below, although these changes could be implemented for either China or the United States



Potential Technical Paths to SiC Wafer Cost Reduction





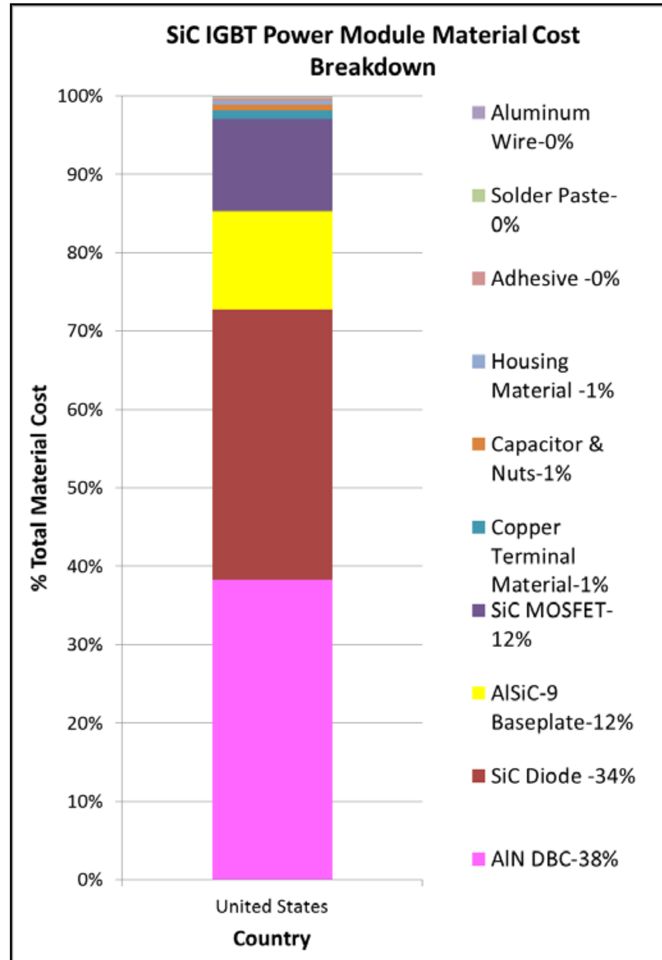
- Substrate costs account for >80% of chip costs at 5,000 6-inch wafers/year
- Yield is key to reducing costs, and quality is key for obtaining market penetration

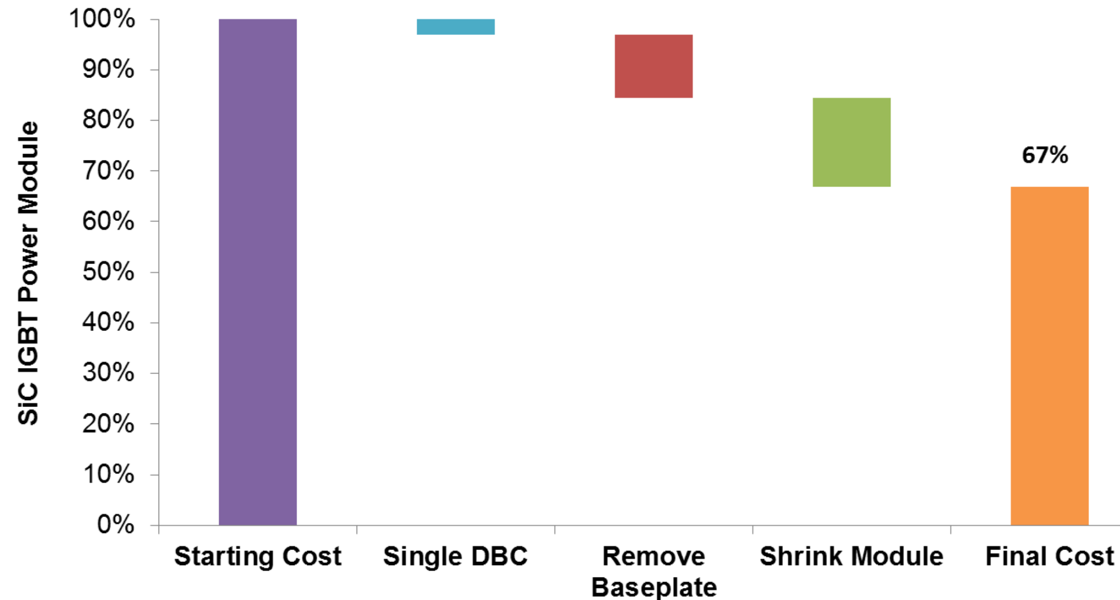
Greater than 50% Savings Potential

Power Module Cost Reduction Scenario

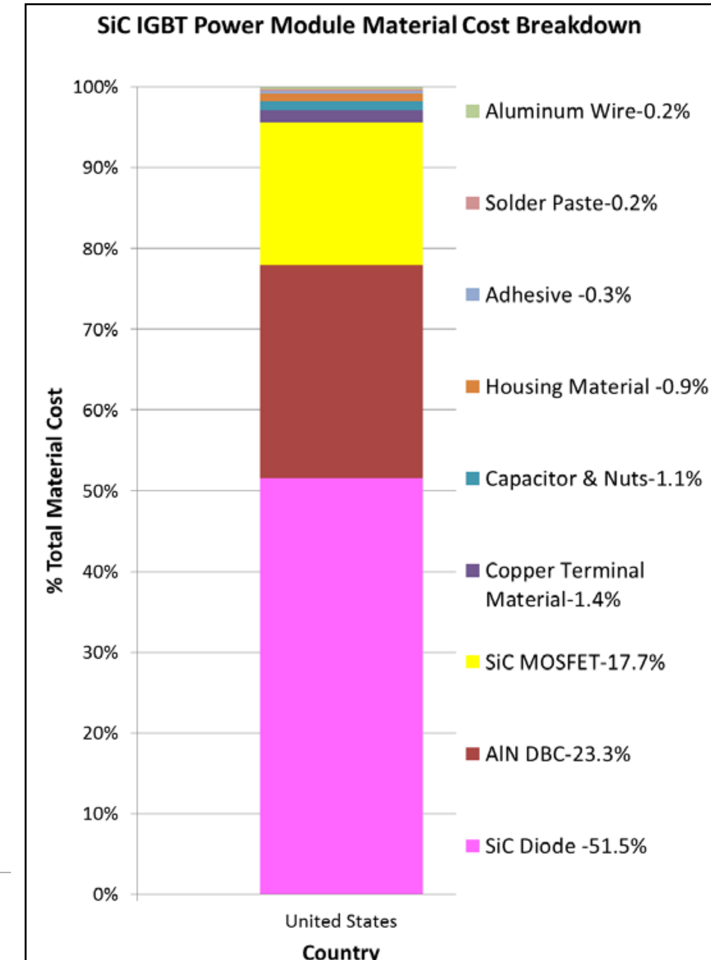
- Technical Path to Module Cost Reduction
  - Use only a single DBC
  - Remove having a baseplate
  - Shrink the module size ½
- Overall 33% cost reduction
  - SiC Devices now >69% of device cost

Current





Future



Thank You!

For more detailed information on our assumptions, see our accompanying technical report "Global Cost and Competitiveness Issues in Manufacturing SiC Power Electronics for Medium Voltage Motor Drives," NREL/TP-6A20-67694 (Feb. 2017)

http://www.nrel.gov/docs/fy17osti/67694.pdf

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