



A Techno-Economic Analysis and Cost Reduction Roadmap for III-V Solar Cells

Kelsey A. W. Horowitz, Timothy Remo, Brittany Smith,
and Aaron Ptak

National Renewable Energy Laboratory

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Contract No. DE-AC36-08GO28308

Technical Report
NREL/TP-6A20-72103
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Suggested Citation

Horowitz, Kelsey A. W., Timothy Remo, Brittany Smith, and Aaron Ptak. 2018. *Techno-Economic Analysis and Cost Reduction Roadmap for III-V Solar Cells*. Golden, CO: National Renewable Energy Laboratory. NREL/TP-6A20-72103. <https://www.nrel.gov/docs/fy19osti/72103.pdf>.

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National Renewable Energy Laboratory
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Golden, CO 80401
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Acknowledgments

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List of Acronyms

c-Si	crystalline silicon
CdTe	cadmium telluride
D-HVPE	dynamic hydride vapor phase epitaxy
DCF	discounted cash flow
GaAs	gallium arsenide
GaInAs	gallium indium arsenide
GaInP	gallium indium phosphide
GaN	gallium nitride
HVPE	hydride vapor phase epitaxy
kg	kilogram
LM	lattice-matched (LM)
LCOE	levelized cost of energy
MOCVD	metal-organic chemical vapor deposition
NREL	National Renewable Energy Laboratory
PV	photovoltaic
R&D	research and development
SG&A	sales, general, and administrative
Si	silicon
TMG	trimethylgallium
TMI	trimethylindium
UAV	unmanned aerial vehicle
W	Watts
WACC	weighted-average cost of capital
W _{DC}	Watts direct current

Executive Summary

III-V materials have achieved the highest efficiency of any solar cell technology. III-V solar cells have been commercially available for decades and have been widely used in space applications where high performance is required. However, prices of III-V solar cells are currently two to three orders of magnitude higher than other technologies, prohibiting their use in mainstream photovoltaic (PV) markets outside high-concentration photovoltaic systems.

In this report, we present a bottom-up cost model for III-V solar cell technology and use it to model current III-V costs and present a roadmap for potential future cost reductions. These include only the costs of the solar cells themselves, and not the cost of any packaging, or interconnects and cover glass. We estimate current III-V manufacturing costs from \$40/W_{DC} to over \$100/W_{DC}, with minimum sustainable prices of \$70/W_{DC} to over \$170/W_{DC}, depending on the cell type, process assumptions, and production volume. These do not reflect the costs or pricing of any specific company but rather benchmark a range of near-term costs. We show that manufacturing yields and the current low production volumes are key drivers of these high costs. Additionally, we identify three key components of III-V cell costs:

- The wafer or substrate the III-V solar cell is deposited on (GaAs or Ge)
- The epitaxial growth costs
- Other cell processing costs.

In addition to exploring the potential cost reductions that may result from increasing production volumes and yields, we examine advances that could be made in each of these three areas in an attempt to understand how low the costs of III-V solar cells might be able to go in the future, and whether these could be competitive in terrestrial solar markets. We find that cell manufacturing costs of \$0.40/W or below could be achieved in high-volume production, but that this would require commercialization and scale-up of a low-cost epitaxial growth technique; implementation of alternative, low-cost metallization schemes; and, critically, significant research and development to address the high cost of the substrate while achieving high (>90–95%) cumulative production yields.

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1 Introduction

The so-called “III-Vs” are a class of materials consisting of elements from group III (group 13) and group V (group 15) of the periodic table that have been used to create the world’s most-efficient solar photovoltaic (PV) cells.¹ In addition to having excellent optical and electronic properties, including a direct bandgap and high electron mobility, III-Vs can also be grown in multi-junction structures that allow for the reduction of thermalization losses and a resulting increase in efficiency. These solar cells have been used in space applications for decades due to their superior radiation resistance and ability to perform well in harsh environments, including extreme temperatures, compared to crystalline silicon (c-Si) solar cells (Andreev 2011). III-V solar cells themselves are thin-films, typically just a few microns thick, and they can be removed from their substrate to create flexible, lightweight devices. This characteristic is also valuable in aerospace applications, where weight drives total system cost and the ability to incorporate cells onto non-planar surfaces can be valuable. Additionally, the low temperature coefficient and good low-light performance of III-V cells can result in higher energy yield (kWh/kW) than c-Si in different locations (Silverman et al. 2013).

Despite these advantages, very few III-V solar cells are in use terrestrially because of their high cost: current III-V solar module prices often exceed \$150/W, which is roughly 400X the current prices for mainstream c-Si solar and cadmium telluride (CdTe) modules (\$0.30–\$0.50/W). Only applications that require the performance of III-V solar cells, including some unmanned aerial vehicle (UAV) and military applications, can tolerate these prices. These devices have been used in many high-concentration photovoltaic systems that concentrate incident sunlight onto a small area, such that much less solar cell material is required. However, concentrator photovoltaic installations have largely stopped in recent years (Wiesenfarth et al. 2017).

Some analysis is available on the cost of III-V solar cells and potential pathways to reduced costs. NREL published a slide deck containing some initial analysis of single and dual junction III-V solar cells cost structures and potential cost reductions in 2013 (Woodhouse and Goodrich 2013). Bottom-up cost modeling and road-mapping for III-Vs on Si tandem devices was published more recently (Essig et al. 2017). Estimated costs of III-V solar cells fabricated using hydride vapor phase epitaxy (HVPE) and epitaxial lift-off (ELO) with substrate reuse are included in (Simon, Schulte and Horowitz et al. forthcoming), along with a comparison of installed PV system costs for this technology and c-Si. Separate work outlining the pathways and challenges for reducing III-V substrate costs via different lift-off and reuse approaches has also been published (Ward et al. 2016).

However, a comprehensive picture of the potential for III-V solar cells to achieve one-sun costs compatible with larger-scale terrestrial deployment in rooftop, ground-mounted, or product-integrated markets has not yet emerged. In this report, we use bottom-up models to estimate the current costs of III-V cells. We highlight key cost drivers and map a path to a cost of \$0.50/W_{DC} or below, and we identify the research, development, manufacturing, and scaling challenges required to achieve these costs.

¹ See “Photovoltaic Research,” NREL, <https://www.nrel.gov/pv/>

This analysis is intended to inform research and development (R&D) directions, as well as to understand how III-V costs could evolve given potential cost reduction avenues that the authors are currently aware of. It is not intended as a projection of III-V costs, and how costs evolve over time will depend significantly on the investment in this area, pricing of input materials along the supply chain, and the outcomes of uncertain R&D and scaling efforts.

All cost analysis presented here includes only the costs of the solar cells themselves—and not the cost of any packaging, or interconnects and cover glass. The yield losses associated with these packaging steps are also not reflected in the cell costs presented here.

2 Methodology

This analysis utilizes NREL's established bottom-up cost analysis approach, which has been previously published in (Woodhouse and Goodrich 2013; Horowitz and Woodhouse 2015; Goodrich, et al. 2013; Woodhouse, Goodrich and Margolis et al. 2013; Horowitz, Fu and Woodhouse 2016). The general methodology is:

1. Determine a model device structure and manufacturing process flow based on academic literature, patents, and expert input, including interviews with current solar cell manufacturers.
 - A. In this case, three device structures are explored: triple junction (3J) GaInP/GaInAs/Ge, dual junction (2J) GaInP/GaAs, and single junction GaAs solar cells. The designs are intended to be representative of those produced commercially by the industry, but do not reflect the exact designs of a specific manufacturer, and in practice some design variability exists between different manufacturers.
 - B. Process flows are tailored to the production volume modeled and the intended markets. In some cases, this reflects current prevailing manufacturing practice (to the best of our knowledge), and in other cases, in particular when imagining what a process for III-V solar cells would look like for much higher production volumes than are observed today, this involves some informed speculation. This speculation is informed by current technology and comparable manufacturing processes in similar industries as well as interviews with industry members along the supply chain. Citations for specific assumptions for each case are described in Sections 3 and 4.
2. Create total cost-of-ownership models for each step in the process flow, which include all materials, direct labor, electricity, equipment, manufacturing facility, and maintenance costs.
3. Collect input data for the cost-of-ownership models for each process step, including, for example, deposition rates and other elements of process or cycle time, consumables usage, material utilization rates, and pricing. These data are collected from material and equipment suppliers, as well as solar cell manufacturers and other experts. Fully burdened costs (\$/hr) and electricity prices (\$/kWh) are taken from Bureau of Labor Statistics (Bureau of Labor Statistics 2017) and the U.S. Energy Information Administration (EIA 2018) respectively, for each manufacturing location modeled.

4. Sum the costs for all process steps to calculate the total manufacturing cost.
5. Input results from the manufacturing cost model into a *pro forma* discounted cash flow (DCF) model to calculate a minimum sustainable price (MSP) for the model device. MSP assumes all overhead costs (R&D, sales, general, and administrative (SG&A)) costs can be covered, and investors can be paid back at the weighted-average cost of capital (WACC). This DCF and the meaning of MSP have been described previously in (Horowitz and Woodhouse 2015; Powell et al. 2015). MSP, notably, does not represent the minimum possible price that can be observed in the market; it is not a market price

The model device structures and process flows, as well as details of input data or assumptions for each cell type and scenario are described in detail in Sections 3 and 4. All costs are modeled, and do not represent actual costs or prices of any particular company.

3 Cost Structure of Current III-V Solar Cells

In this section, we benchmark current costs of III-V solar cells, including single-junction, 2J, and 3J designs and discuss key cost drivers. All these solar cells are currently produced in low volumes, typically on the order of 100's of kW/year to low MW/year, although there have been announcements to expand single and/or 2J III-V solar cell production to 40MW/year in China (Osborne 2018). We assume a production volume of 3,800 6-inch wafers per month (45,600 wafers/year) for our base case models, equivalent to 200kW/year at 33% cell efficiency. We also make simplifying assumptions that capacity is fully utilized and that equipment and facilities are purchased new (i.e., are not yet depreciated).

3.1 Triple Junction Solar Cells

Multiple 3J solar cell designs exist in the market today. Most of these fall into the following general categories: lattice-matched (LM) GaInP/GaInAs/Ge cells, lattice-matched GaInP/Ga(In)As/GaInNAs dilute-nitride cells, inverted metamorphic solar cells, and upright metamorphic cells. For purposes of benchmarking in this report, we focus on a LM on Ge design, shown in Figure 1, with cell layers deposited via metal-organic chemical vapor deposition (MOCVD). We assume the metal contact layers are deposited using electron beam (e-beam) evaporation, with lithography used to define the front contacts. To the best of our knowledge, these represent the prevailing techniques used in industry today. In addition to the layers shown in Figure 1, we also assume an Al₂O₃/TiO₂ anti-reflective coating (ARC) is deposited via sputtering. The composition and fabrication approach of ARC for these solar cells varies by company and application, but the difference in costs between different ARC options are very low compared to other costs and uncertainties in our model. For the 3J cell, our model includes a total of 20 full time equivalent (FTE) direct laborers at 200 kW/year and five full-time equivalent (FTE) direct laborers at 50 kW/year. Overhead and other non-direct labor are captured in research and development (R&D) and selling, general, and administrative (SG&A) costs discussed below. The labor rates (\$/hour) assumed and other assumptions are summarized in Table 1.

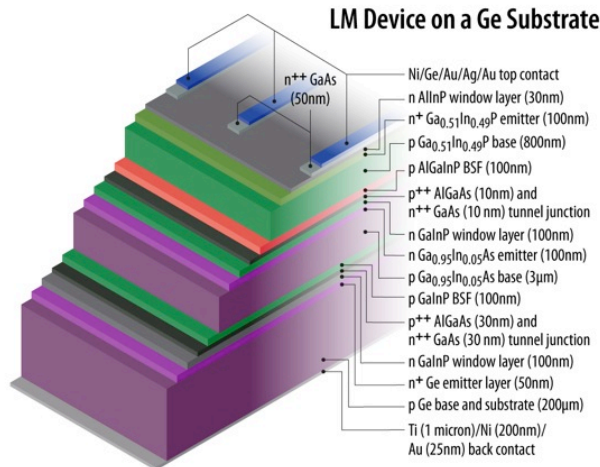


Figure 1. Schematic of the 3J device structure analyzed

Table 1. Key Input Assumptions for the III-V Solar Cell Base Cost Model

Parameter	Value	Notes
MOCVD tool cost	\$2.8million/tool	Includes installation and auxiliary costs
MOCVD batch size	8	6-inch wafers
MOCVD tool uptime	85%	
Heat/cool + pump/vent time for MOCVD	30 min	
GaAs deposition rate	15 µm/hour	
InGaP deposition rate	4 µm/hour	
Trimethylgallium (TMG) price	\$1/g	Prices can vary widely depending on the production location and company's leverage and supply chain. Prices as low as \$0.45/g for Chinese manufacturing (of LEDs and other devices) have been reported.
Trimethylindium (TMI) price	\$12/g	Prices can vary widely depending on the production location and company's leverage and supply chain.
TMG, TMI material utilization rate	30%	
Average V/III ratio	22	Used to calculate AsH ₃ and PH ₃ usage
Arsine (AsH ₃) price	\$0.44/g	
Phosphine (PH ₃) price	\$0.35/g	
Gold (Au) price	\$43/g	Assume recycling of Au that is utilized
Silver (Ag) price	\$0.55/g	
Ge substrate price	\$130/6-inch substrate	Prices can vary depending on the production location and company's leverage and supply chain, with prices

Parameter	Value	Notes
Cell area	133 cm ²	roughly between \$120/substrate and \$150/substrate Cropped 6-inch (150mm) wafer
Cumulative yield loss	20%	For the 3J cell on Ge only. Higher yield loss is assumed for later analysis on lift-off cells and is specified in Table 2.
Equipment depreciation	5-year straight-line	
Building depreciation	20-year straight-line	
Labor rates	\$14/hr for unskilled labor, \$25/hr for skilled labor	Will vary by location; these are meant to represent a mid-cost location in the United States.

Figure 2 shows the resulting step-by-step manufacturing cost breakdown for the 3J LM solar cell for two different production volumes—50kW/year and 200kW/year production. Total direct manufacturing costs (including depreciation) are estimated to be \$70/W_{DC} at 33% cell efficiency for 200kW/year production and \$100/W_{DC} for 50kW/year production. The significant difference in cost between these two volumes is due largely to the fact that fixed equipment and building costs are socialized over fewer watts produced; in other words, some of the tools are underutilized at 50kW/year, resulting in higher cost. There may also be some difference in material costs at these different scales; however, we did not have sufficient data to fully include this effect. Costs for each scenario will also depend on the level of automation employed.

As can be seen from the figure, the largest single cost is the Ge substrate, followed by MOCVD of the epi-stack. MOCVD costs are dominated by the equipment depreciation cost and the material costs. The high equipment depreciation cost is due both to the high price of each MOCVD tool and the long cycle time resulting both from significant heating and cooling time (30 min) and slow deposition (38 minutes total growth time), that is only amortized over a modest batch size (eight 6-inch wafers). Both the trimethyl- precursors and the arsine and phosphine contribute significantly to the material cost, and material costs are driven both by low utilization (particularly for the arsine and phosphine) and high material price per gram. The lithography equipment costs are also high due to high costs per tool set (\$1 million–\$2.5million installed for all required equipment) and low throughputs arising from to the use of single wafer processing on multiple toolsets (leading to a need for multiple tools). However, as previously mentioned, our analysis assumes this equipment (and all equipment) is purchased new and has not yet been depreciated. In cases where companies purchased used equipment and/or who have partially or fully depreciated these assets, these costs will lower.

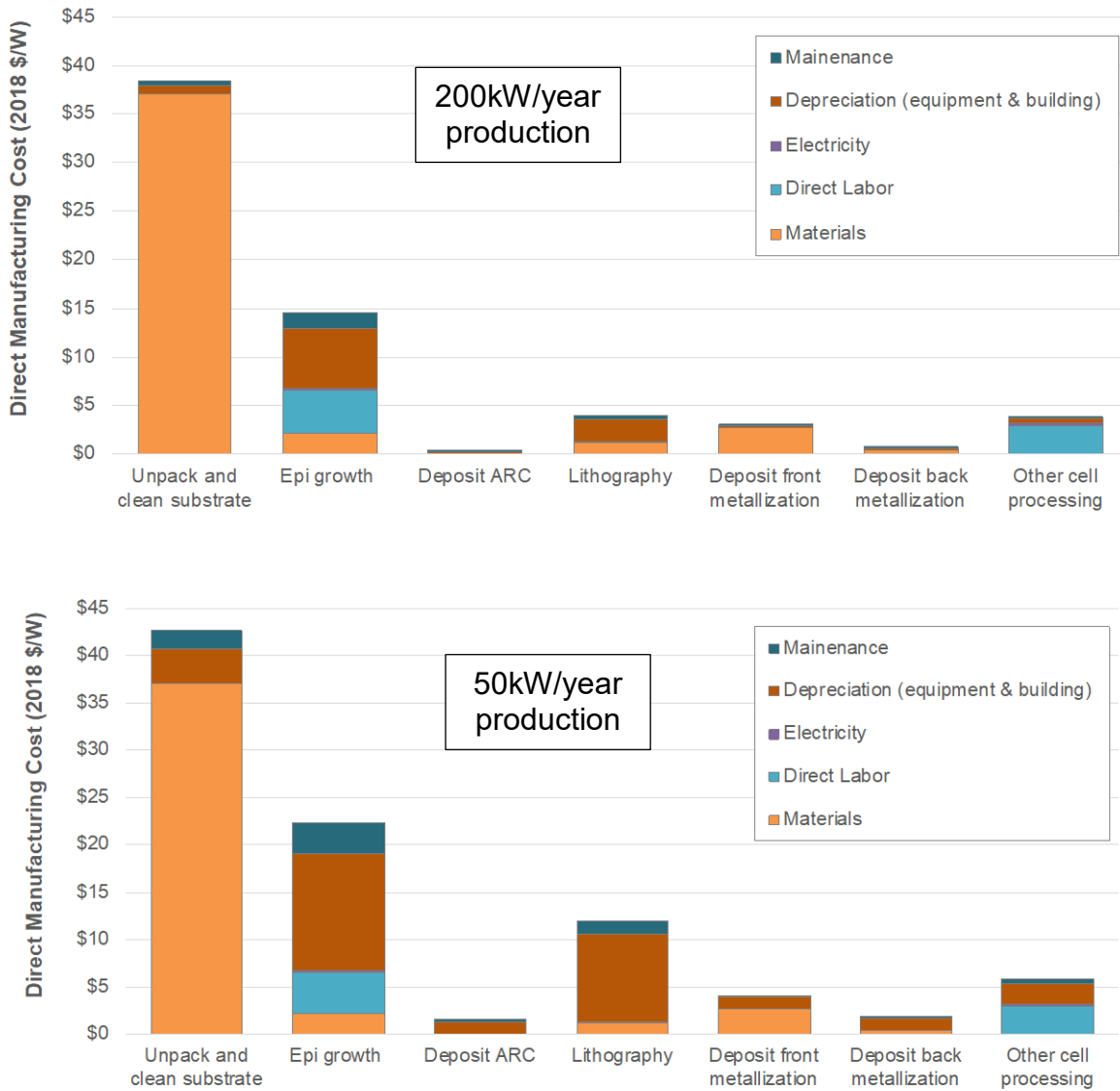


Figure 2. Step-by-step manufacturing cost breakdown for the 3J LM III-V solar cell shown in Figure 1

33% cell efficiency, U.S. manufacturing for (top) 200kW/year production volumes and (bottom) 50kW/year production volumes

The sensitivity of these manufacturing costs to $\pm 20\%$ changes in key input parameters is shown in Figure 3. As can be observed from the figure, the largest lever on cost is the Ge substrate price, followed by the manufacturing yield. Factors which affect the MOCVD process time, including deposition rates, base layer thicknesses, and the heating and cooling time, have a limited impact on costs at this production volume because at least one tool (and a minimum amount of staff and electricity to operate it) is required. If Au is not recycled (as assumed here), sensitivity to Au prices increases significantly. Similarly, if Ag is recycled (no Ag recycling is assumed in our base model), sensitivity to Ag prices decreases, although the decrease is less significant. Efficiency (not shown) also significantly influences manufacturing costs: decreasing efficiency to from 33% to 32% increases costs by $\$2.20/W_{DC}$, and increasing efficiency to 34% decreases costs by $\$2.07/W_{DC}$.



Figure 3. Sensitivity of direct manufacturing costs for the 3J LM III-V solar cell to changes in key input parameters

33% cell efficiency, U.S. manufacturing at 200 kW/year

Looking beyond direct manufacturing costs, overhead costs such as research and development (R&D) and selling, general, and administrative (SG&A) costs could contribute significantly to overall costs, particularly given the low volume of production and lack of standardization among projects/customers for III-V solar cells. Because there are no publicly traded III-V solar cell companies, we do not have data on actual R&D and SG&A costs in this industry. However, for purposes of illustration, we look at an example of what total costs and MSP may be if R&D and SG&A costs are 10% and 20% of revenue, respectively (Figure 4). We assume these same percentages for both the 50kW/year and 200kW/year cases, but in practice this will vary by company. The MSP in this example would be just under $\$120/W_{DC}$ at 200kW/year and approximately $\$170/W_{DC}$ at 50kW/year. This assumes a 14.8% weighted-average cost of capital (WACC), consistent with what has been estimated for other PV manufacturing companies (Powell et al. 2015) (again, no data on cost of capital for III-V solar cell companies are publicly available). A 20-year project life, 2% inflation rate, and a combined state and federal tax rate of 25.7%.

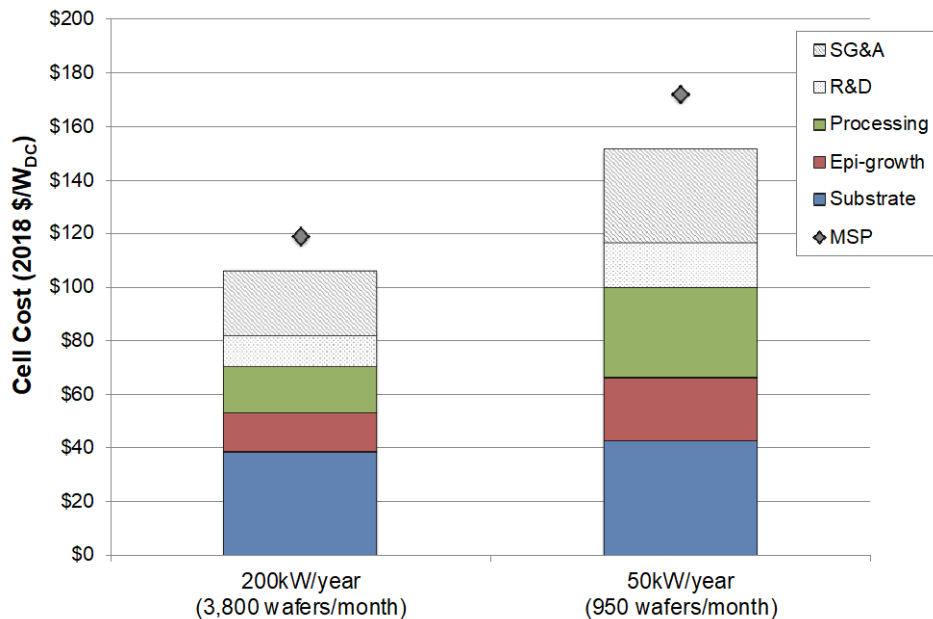


Figure 4. Example of a possible total cell cost breakdown by category and MSP for the 3J LM III-V solar cell shown in Figure 1

33% cell efficiency, U.S. manufacturing at 200 kW/year
 SG&A and R&D costs, as well as cost of capital (which influences MSP)
 vary by company and are not publicly available.

3.2 Single and Dual Junction Solar Cells

In this section, we explore costs associated with single and dual junction (2J) III-V solar cells. Figure 5 shows the reference cell designs used in our cost analysis. While these cells share many process steps with the typical 3J LM III-V solar cells on Ge analyzed in Section 3.1, there are several differences. First, Alta Devices is currently employing epitaxial lift-off (ELO) and substrate reuse for their single and 2J solar cells to mitigate the high cost of the GaAs substrate. ELO and reuse is also in use by MicroLink Devices for their 3J IMM cells, and this approach has also been explored at an R&D scale by a several other companies and research organizations (Adams et al. 2013). However, most 3J or 4J III-V solar cells on the market today (and used largely in space applications) do not employ ELO and reuse; instead, the substrate is thinned via etching as required by the application.

In our base case, we assume five substrate reuses as has been demonstrated in peer-review literature (Adams et al. 2013). Data on cell quality with 10 reuses has also been presented at a previous workshop (Li and Chaparala 2013), and we also explore the sensitivity of cell costs to number of substrate reuses in this section. Here, we assume chemo-mechanical polishing (CMP) is required after each lift-off step to re-prepare the surface for growth. However, there has been some literature suggesting that CMP may not be required during each lift-off step if a combination of buffer and protective etch layers are utilized (Lee et al. 2012). Because of this, we evaluate the impact of reduced CMP requirements on substrate and total cell costs in Section 4.3.

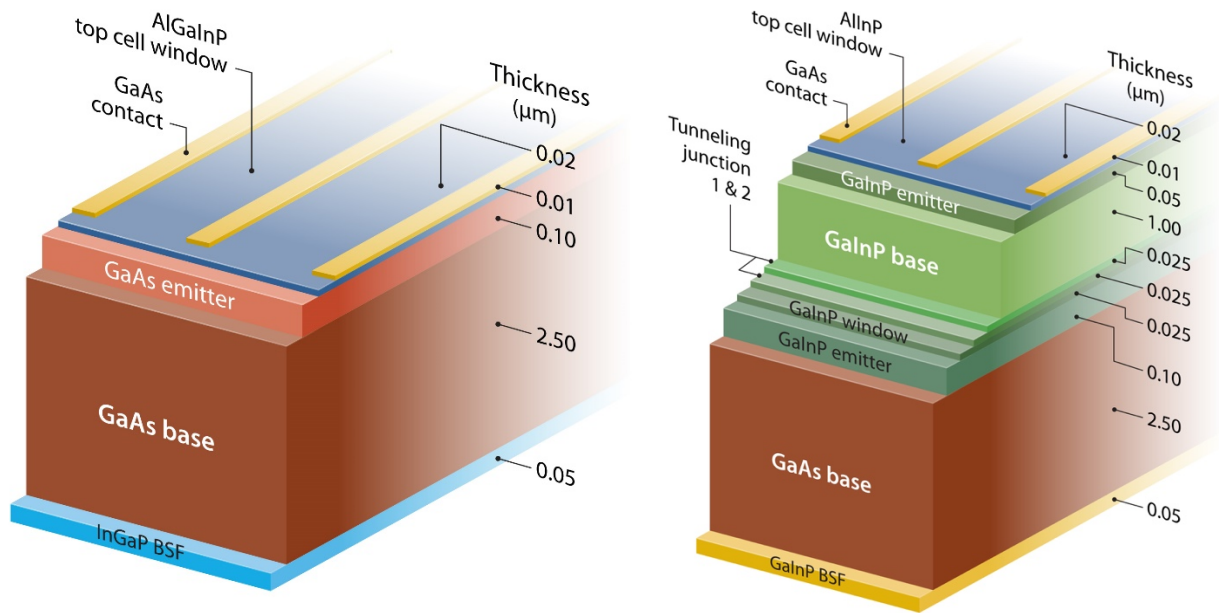


Figure 5. Diagram showing (left) single and (right) 2J III-V solar cell designs used in our cost model

While we assume the same production volume as for the 3J cells in our base case (3,800 6-inch wafers/month, equal to 170kW/year at 28% efficiency and 182kW/year at 30% efficiency), we also consider potential cost reductions associated with scaling up production to 20MW/year plants, consistent with the capacity Hanergy plans to install in China to produce single and/or 2J solar cells (Osborne 2018). However, we have significant uncertainty in the cost of epitaxial lift-off and reclaim/re-polishing processes at those production volumes because of the proprietary and firm-specific nature of these processes and associated difficulty in obtaining data. We make assumptions about the process scalability and cost, detailed below, and the sensitivity to different variables is also discussed in Section 4.3.

As with 3J cells, we assume the epitaxial layers are grown using MOCVD, the prevailing industry practice. For our base case, we assume the same growth rates for all layers as for the 3J case, but we also explore a high growth rate case, where GaAs is deposited at 60 $\mu\text{m}/\text{hour}$. Single junction GaAs solar cells have been grown at these rates in the literature with minimal degradation in cell performance (Schneider et al. 2017). The assumptions about labor intensity and level of automation are also the same as for the 3J cells.

We use a GaAs substrate price of \$100/6-inch wafer, and we assume a CMP cost of \$25/wafer. This CMP cost can vary by as much as 40%–50%, as there is significant variation in the quality of the reclaimed wafers. This leads to differences in the number and type of polishing steps required as well as the amount of material that needs to be removed to achieve a satisfactory surface for re-growth. For the ELO, we assume the same general process flow as in (Woodhouse and Goodrich 2013; Ward et al. 2016), which involves bonding the cell to a handle and then dissolving a lift-off layer using a wet process with a mechanism to apply stress to the substrate while etching as illustrated in Figure 6. We refer to the tool used to perform the first function as the bonding tool and that used to perform the second function as the ELO tool. As in (Ward et al.

2016), we use 10 hours for the etch step to dissolve the lift-off layer, and assume 80 cells per batch, which results in a requirement for one (fully utilized) ELO tool at this cycle time and our base production volume. Our assumptions about ELO and substrate costs are summarized in Table 2. As discussed above, these parameters contain significant uncertainty due to the lack of available data. In addition to uncertainty about the process parameters and tool costs (tools are currently customized and proprietary), companies may be lifting off smaller areas of cells (coupons, rather than full 6-inch wafers) that are later arrayed in packaging to create modules. This would affect etch times and influence overall throughput. Other assumptions for the single and 2J cost models (in the base case) are the same as those made for 3J solar cells (Table 1). We use the same financial assumptions (SG&A costs, R&D costs, cost of capital, and inflation rate) as for the 3J solar cells.

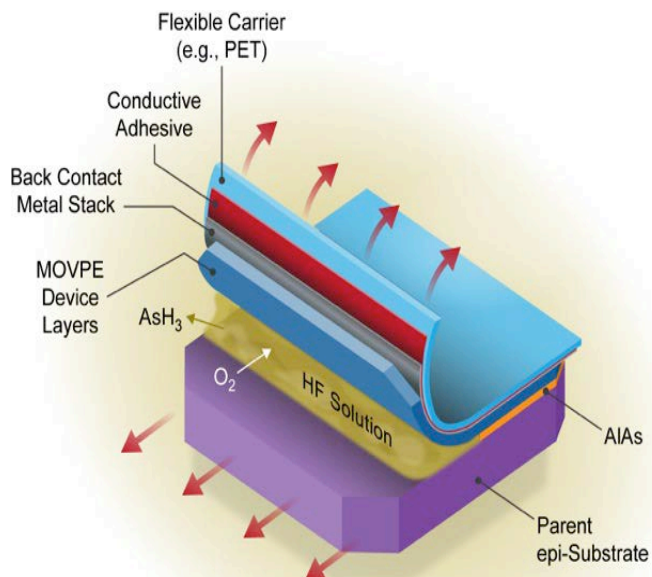


Figure 6. Illustration of the ELO process

The cell is bonded to a flexible carrier, and then stress is applied to peel the cell off of the parent epi-substrate (GaAs) while HF solution etches an aluminum arsenide (AlAs) lift-off layer.

Table 2. Key ELO and Substrate Assumptions for the Single and 2J Base Cases

Other input assumptions not specified here are the same as those in Table 1 (the assumptions used for the 3J solar cell).

Parameter	Value	Notes
GaAs substrate price	\$100/6-inch wafer	Prices can vary depending on the production location and company's leverage and supply chain, with prices roughly between \$90/substrate and \$150/substrate.
CMP cost	\$25/polish	May vary by up to 40%–50%
Number of substrate reuses	5	More may be possible in practice today, but limited data are available; see discussion above.

Parameter	Value	Notes
ELO tool installed price	\$400,000	
ELO tool uptime	90%	
ELO process yield	80%	
ELO tool throughput	8 cells/hour	10 hours of etch time, batch size of 80 cells
Bonding tool installed price	\$350,000	
Bonding throughput	20 cells per hour	Includes time for coating with adhesive and baking
Bonding tool uptime	90%	
Yield loss	10% additional yield loss introduced by ELO and reuse	Cumulative yield loss is then 30%. There is very little data available on yields currently achieved with reuse, or how this varies with the number of reuses.

Figure 7 (next page) shows the step-by-step cost breakdown for the single junction GaAs solar cells and dual-junction GaInP/GaAs solar cells under these assumptions with a production volume of 3,800 cells/month (roughly 200kW/year). The total manufacturing cost for the single-junction cell at 28% efficiency is calculated to be \$41W, with an MSP of \$69/W. For a dual-junction cell at 30% efficiency fabricated using the same process as the single-junction, we estimate a total manufacturing cost of \$41/W_{DC} and MSP of \$69/W_{DC}. While the epitaxial growth costs are higher for the dual-junction case, the increase in efficiency compared to the single-junction case drives reductions in the other cell costs resulting in a very similar cost per watt. Figure 8 compares the breakdown of costs for each of these cell types. At higher production volumes, equipment, material costs, direct labor, and overhead costs can be reduced significantly. We will discuss the potential impact of increased production volumes on cell costs in detail in Section 4.

As can be seen from Figure 7, the CMP costs are similar to the total cost of the substrate in this case, because the substrate cost is amortized over five reuses. The substrate and costs associated with reuses—CMP and ELO—are the largest contributor to overall cell costs. The high depreciation and labor costs associated with the ELO process are partly due to the low production volume, resulting in partially utilized tools and higher labor requirement, and partly due to the long cycle times associated with etching away the release layer.

While the epitaxial growth is the next most expensive step, the sum of steps involved in metallization exceed the cost of epitaxy. In particular, the high equipment cost associated with lithography equipment (due to the use of multi-step, single wafer processes as described above) is high and the cost of materials for the front contact fingers is high due to very low material utilization and the high per gram cost of the contact materials (the front contact includes gold in our reference design). Again, our analysis assumes the lithography equipment is purchased new and has not yet been depreciated. Some companies may also employ alternative, lower-cost metallization schemes for one sun applications (e.g., mobile PV and UAVs), but there is no publicly available information on these approaches or the extent to which they are utilized in practice.

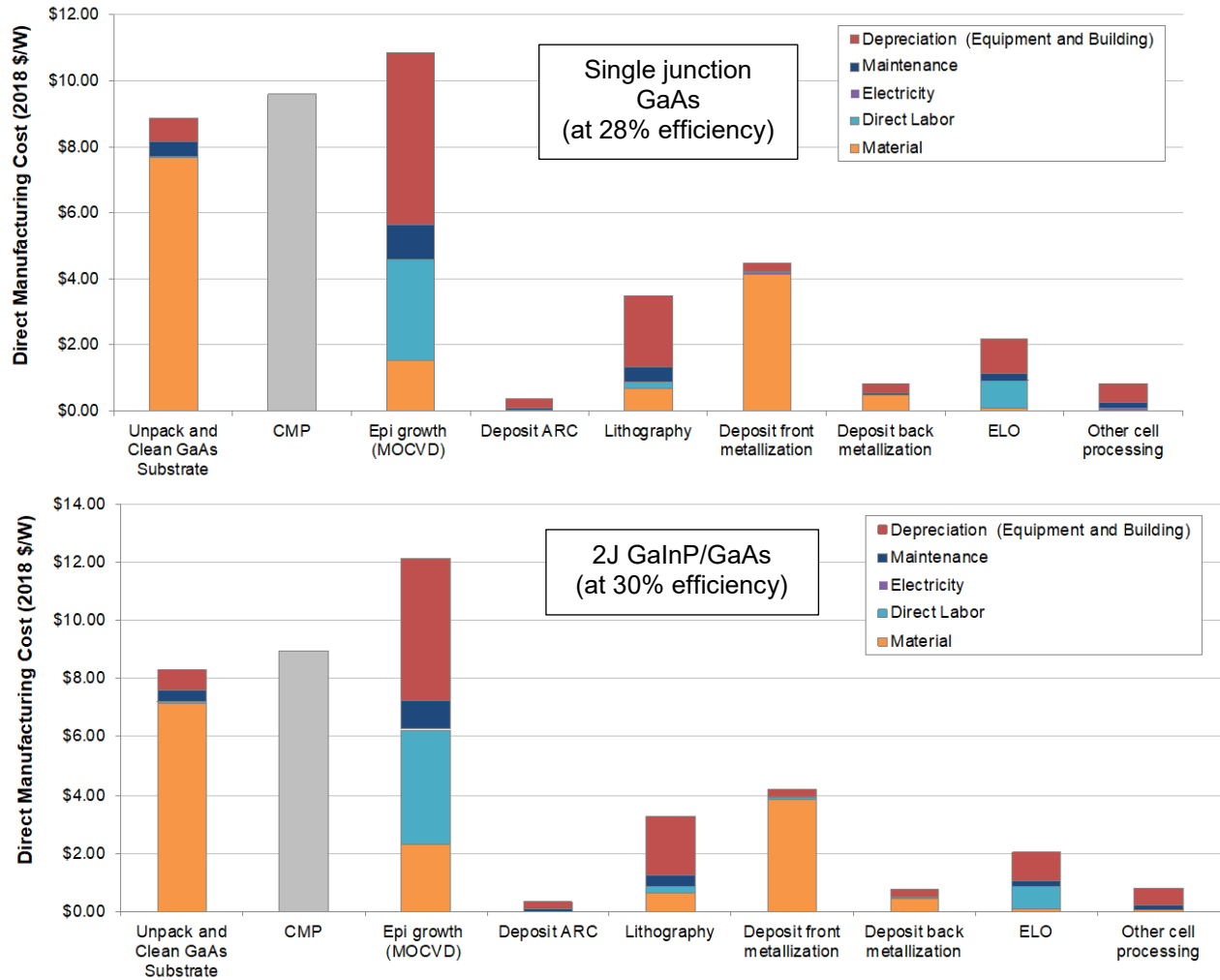


Figure 7. Step-by-step cost breakdown for (top) single junction GaAs solar cells at 28% efficiency and (bottom) 2J GaInP/GaAs solar cells at 30% fabricated via MOCVD in the base case

Assumes U.S. manufacturing at 3,800 cells/month (170kW/year - 182kW/year, depending on the efficiency); the CMP bar is gray because we do not have a bottom-up CMP cost model, but rather total costs obtained via industry interviews.

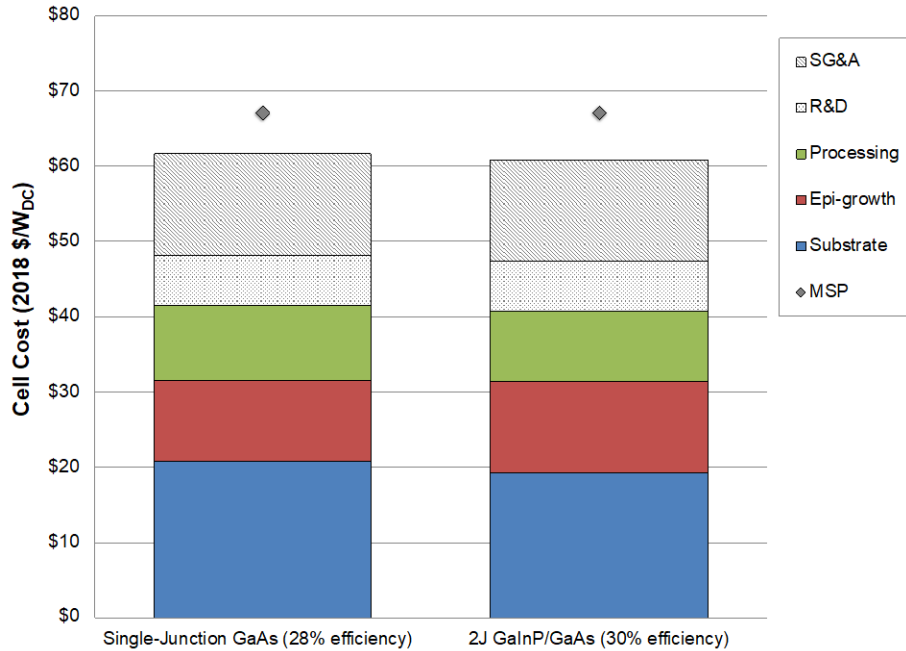


Figure 8. Comparison of cell cost breakdown for single- and dual-junction III-V solar cells grown via MOCVD

Assumes U.S. manufacturing; SG&A and R&D costs, as well as cost of capital (which influences MSP) vary by company and are not publicly available, so these are estimates.

Cell costs are also sensitive to a variety of factors that contain uncertain, either due real variability in processes and prices between companies and/or data limitations. Figure 9 shows how $\pm 20\%$ changes in key input variables influence total cell manufacturing costs. As with the 3J cells, manufacturing yield and substrate costs are a primary cost drivers. Changes in MOCVD tool price are also significant, at the same throughput (note that the sensitivity of cell costs to MOCVD tool price is roughly the same as for the 3J III-V cell in Figure 3, but the scale on the x-axis is different). The cost of CMP used to re-prepare the surface after lift-off, is another major cost driver.

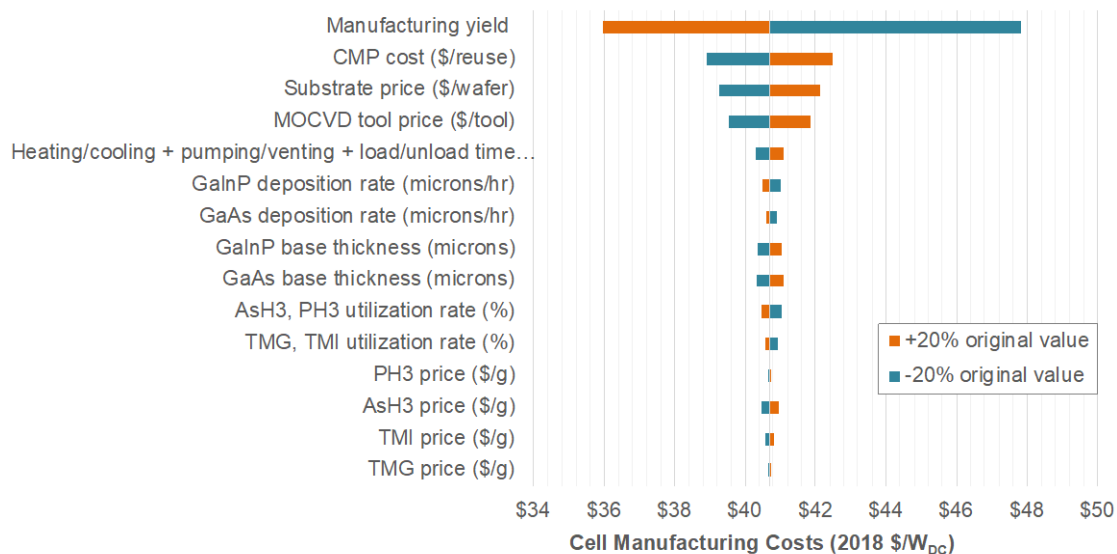


Figure 9. Sensitivity of 2J GaInP/GaAs cell costs to key input parameters

Assumes 30% cell efficiency and U.S. manufacturing and approximately 200kW/year production volume

The impact of increased deposition rates is limited by several factors. First, the non-linear influence on overall cycle time, which is split between growth and heating, cooling, pumping, venting, loading, and unloading time (30 minutes total in our model), and GaAs deposition rate only influences a portion of the epitaxial growth time (assuming constant GaInP deposition rates, which are approximately three times lower than GaAs in our reference case). Second, at these production volumes, only one MOCVD tool is required. Increasing the deposition rate, therefore, does drive some per Watt reductions in labor and electricity usage, but does not significantly affect depreciation costs, which are much more significant. Third, epitaxial growth costs only constitute a fraction of total cell manufacturing costs in this scenario. However, in certain future scenarios where III-Vs are produced at larger scale with modified manufacturing processes, deposition rate can have a more significant effect; additionally, in larger or more mainstream PV markets, the implications of \$1/W lower costs, or even a few cents a Watt lower costs, are the difference between a competitive and uncompetitive cell design. These scenarios are explored in detail in Section 4.

The sensitivity of 2J cell manufacturing cost to number of substrate reuses at different CMP costs is shown in Figure 10. \$25/CMP is the reference value (Table 2). \$8–\$10/CMP may be commensurate with scaling-up the current reclaim process to high volume. \$1/CMP has not been demonstrated yet, to our knowledge. This could be achieved in effect by either reducing the cost of CMP per polish to \$1, or by decreasing the frequency that CMP is required and lowering cost per polish (i.e., reducing CMP costs to \$10/reuse and then only performing CMP after 10 reuses, possibly by utilizing protective layers as described in Lee et al. (2012). Ward et al. (2016) provide further discussion on how the cost of the lift-off, reuse, and reclaim processes effect the total cost reductions that can be achieved as a function of reuses. We further discuss potential avenues to reduced substrate costs in Section 4.3. The degree to which moving to substrate reuses beyond 5–10 results in appreciably lower cost depends on the CMP, ELO processing, and other reclaim costs, as well as how the manufacturing yield loss changes with the number of reuses.

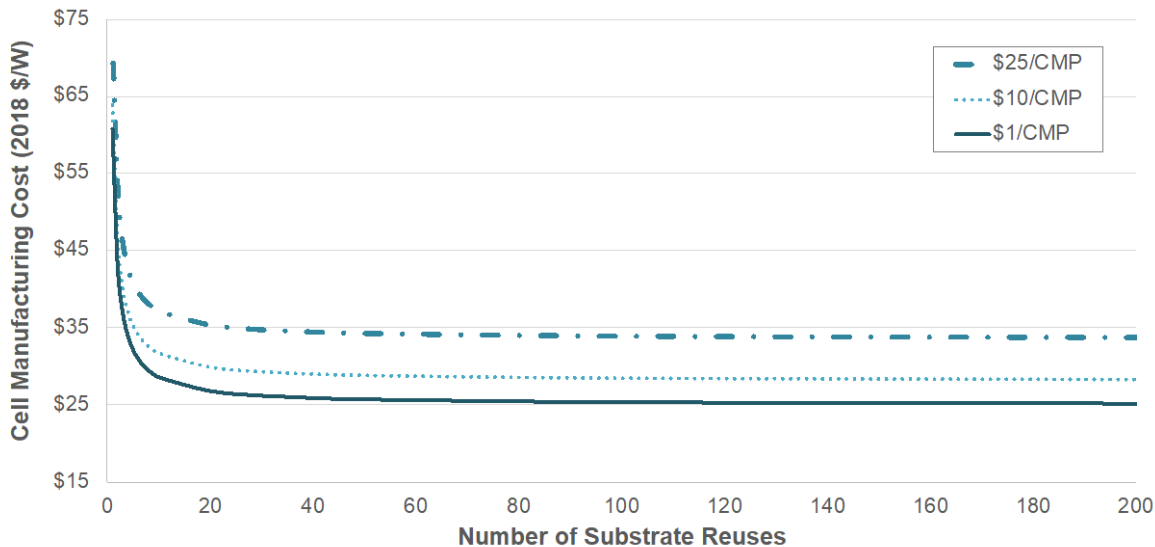


Figure 10. 2J GaInP/GaAs cell manufacturing costs as a function of the number of substrate reuses at different CMP costs

4 Pathways to Reduce III-V Solar Cell Costs

Based on our analysis of current III-V solar cell costs, we can find four key areas for cost reduction: scaling up production volume, reducing epitaxial growth costs, substrate costs, and metallization costs. Production yield improvements will also be critical across all these areas. In this section, we explore these pathways to lower cost, emphasizing R&D and manufacturing advancements required to achieve costs compatible with different PV markets. We focus on the case of the 2J GaInP/GaAs solar cell.

4.1 Production Volume and Yield Improvements

Increasing production volume can drive cost reductions via economies-of-scale and learning-by-doing. We do not have sufficient information to project potential savings associated with learning-by-doing in this report, so this phenomenon is not accounted for here. It is also of note that, because III-V solar cells are currently produced at such a small scale, other effects of scaling, including potential evolution in supply chains, can be difficult to predict. For example, other industries, including the display, c-Si solar, and other industries have seen massive reductions in cost with scale, not all of which were fully anticipated (Keshner and Arya 2004; Fraunhofer Institute for Solar Energy Systems 2018; Park, Lee and Kim 2003).

However, it is still illustrative to observe the potential cost reductions associated with simply scaling-up the reference process flow described in Section 3.2 without modification. The results for the 2J solar cell are shown in Figure 11. We assume progressive reductions in CMP costs (to \$8/CMP at 50MW/year), TMG and TMI precursor prices (to \$0.60/g and \$8/g, respectively, at 50MW/year), and substrate costs (to \$90/wafer at 50MW/year) as production volumes increase. We also assume MOCVD tool costs could be reduced by 10%–15% in high volumes. Other cost reductions result from improved tool utilization and increased automation and thus lower labor costs.

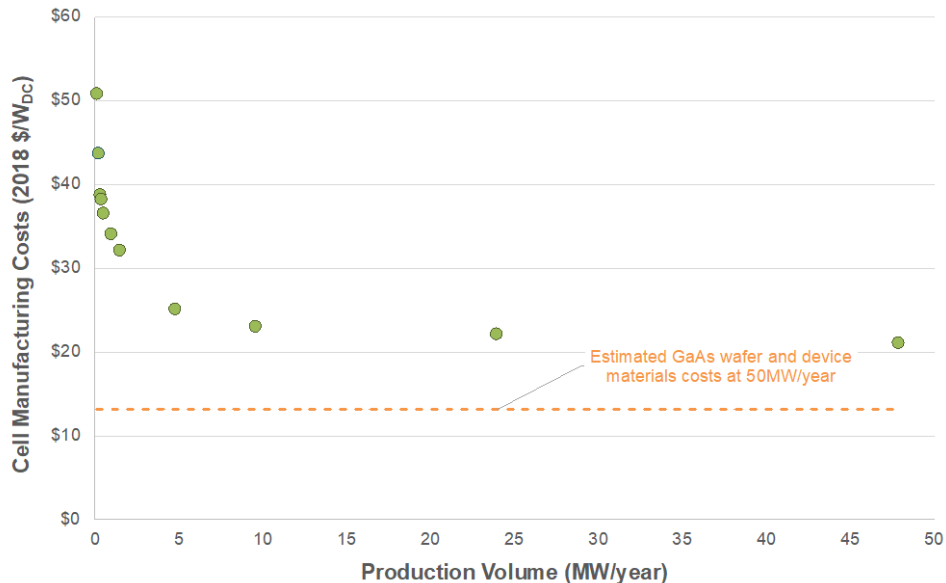


Figure 11. Estimated impact of increased production volume on 2J GaInP/GaAs solar cell costs fabricated with MOCVD

Assumes five substrate reuses, 30% efficiency, and U.S. manufacturing.

We can see that the potential cost reductions associated with simply increasing production volume are significant—approximately \$24/W going from 182 kW/year to 50 MW/year—but ultimately limited by the costs associated with the substrate, CMP, and device materials, including III-V precursors and metal costs. Additionally, MOCVD equipment costs are still high, due to the high price per tool and the relatively long cycle times. While additional economies-of-scale and learning-by-doing may occur at even high production volumes (these are difficult to predict, given the small scale of current production), without process or design improvements to address these issues, scaling up production can only get you so far.

Costs on the order of \$1/W to \$10/W have been tolerable in certain markets, including UAVs, man-portable power (e.g., in military or outdoor recreational applications), and other niche applications; however, these are not compatible with broad deployment in general PV markets. The remaining sections will review possible changes that could achieve further cost reductions.

4.2 Decreased Epitaxial Growth Costs

As discussed in Section 3, current MOCVD growth processes are expensive for several reasons: high cost per tool, low throughput, high cost precursors, and low material utilization. Significant reductions in epitaxy costs will involve improvements on all these fronts. Figure 12 illustrates the impact of different potential future improvements on the epitaxial growth costs for a 2J GaInP/GaAs solar cell at 50MW/year production volume. This assumes 95% yield for the epitaxial growth process in all scenarios (MOCVD and HVPE). The bar on the far left represents the reference case analyzed in Section 3.2. The second bar shows the cost reductions obtained when GaAs growth rates are increased from 15 μ m/hour to 60 μ m/hour, but it leaves the rest of the system and process the same, which is commensurate with publicly demonstrated growth rates as discussed above (Schmeider et al. 2017). It is of note that Fraunhofer has also publicly GaAs deposition rates of 145 μ m/hour with lower efficiency cells (Lang et al. 2018). It may be possible to eventually deposit GaAs with MOCVD at these higher rates with good quality,

increasing throughput. However, cost reductions achieved with these faster deposition rates are eventually limited by the fixed heating and cooling time per wafer in current deposition systems. To reach lower costs, additional throughput increases are required beyond which can be accomplished with current batch MOCVD systems for III-As/P materials. This could be achieved by significantly increasing batch sizes, as has been done with GaN MOCVD reactors for LED growth, which can have batch sizes of 48 six-inch wafers (Veeco 2017). Alternatively, a continuous, in-line MOCVD reactor could be constructed. There has not been any public demonstration of such a system to-date, and, to our knowledge, no such system is used in production today. However, this may be feasible in the future, and if such a reactor were constructed, it could enable significantly higher throughput, resulting in a reduction in total epi-growth costs by more than half, as shown in the third bar of Figure 12. The potential throughput and equipment prices for this scenario are estimated using a bottom-up reactor model described in (Simon, Schulte and Horowitz et al. forthcoming). Because of their higher capital cost per tool, these large in-line reactors (or large batch reactors) are only relevant to higher production volumes. We estimate that volumes of at least several MW/year are required for the capital cost of these tools to be justified.

Additional reductions would require lowering material costs. A major lever for doing so is increasing the material utilization, for the trimethyl precursors and the arsine and phosphine. As we saw in Section 3.2, costs are particularly sensitive to improvements in arsine utilization. The fourth and fifth bars in Figure 12 show the potential impact of significantly increased material utilization in an in-line type MOCVD tool. Again, to our knowledge, these utilization rates have not yet been demonstrated for MOCVD. 50% to 60% utilization of TMG and TMI could be possible in commercial MOCVD systems according to our industry interviews and recent reports (Lang et al. 2018). Re-design of the gas delivery systems and deposition chamber may enable improvements.

Dynamic hydride vapor phase epitaxy (D-HVPE) is one technique which has actually demonstrated very high growth rates—above to 195 $\mu\text{m}/\text{hour}$ for GaAs and 54 $\mu\text{m}/\text{hour}$ for GaInP—for full 2J solar cells in a pseudo-in-line reactor at the laboratory scale (Ptak 2018) (Schulte et al. 2017; Simon, Schulte and Young et al. 2016). D-HVPE is a variation on HVPE, which has been previously used for growth of III-V materials, in which the reaction chambers are spatially separated, enabling the creation of high-quality interfaces at high throughput. This lab reactor design could be extended to a scaled, fully-in-line tool, wherein one chamber is used to deposit each cell layer (Young et al. 2018). A concept drawing for this type of in-line system is illustrated in Figure 13 (no such reactor has actually been built or demonstrated to-date). If implemented, a D-HVPE tool could enable even greater cost reductions, as shown in the last bar of Figure 12. This is mostly due to the fact that input material costs are lower – D-HVPE uses lower-cost elemental Ga (\$0.21/g, 6N) and In (\$0.50/g, 6N) in place of TMG and TMI. Additionally, high performing GaAs and GaInP solar cells have been grown with V/III ratios of 2:4 using D-HVPE (Schulte et al. 2017; Simon, Schulte and Young, et al. 2016), resulting in much higher arsine and phosphine utilization. Additionally, TMG utilization rates of 70% have been estimated for the laboratory-scale tool. As with a very large, in-line MOCVD reactor, additional R&D is required to validate what utilization rates are possible. These utilization rates may not translate to a high-volume production tool, depending on the design, and significant uncertainty exists as to the final utilization rate. In this analyses, we deal with this by presenting parametric analyses showing costs with D-HVPE as a function of Ga and In utilization rates over

a wide range (Figure 14). Increasing the utilization of materials, or reducing the amount of material required by thinning the cell, also helps hedge against potential fluctuations in prices of the input materials. Ga and In prices have fluctuated significantly in the past.

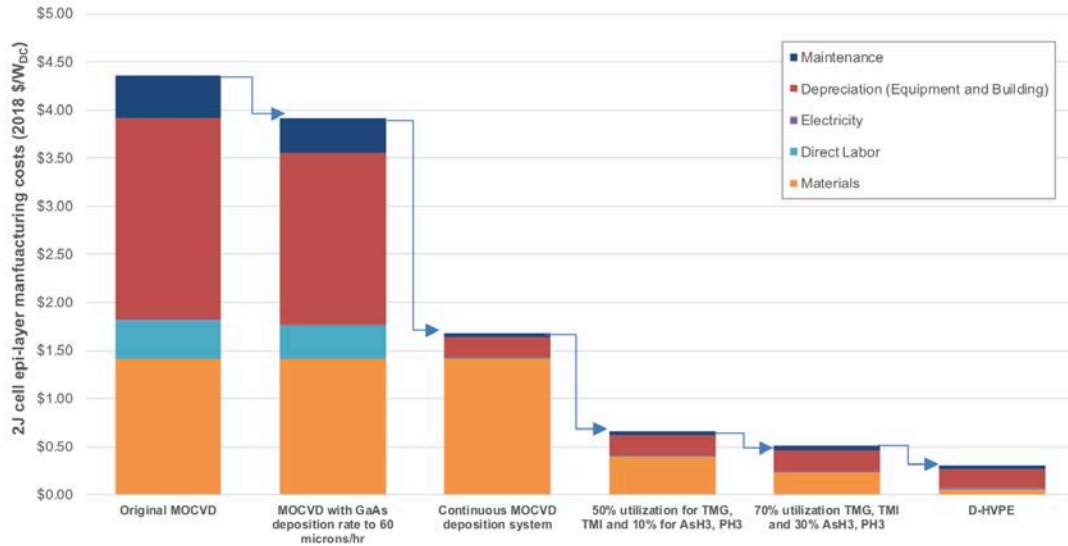


Figure 12. Impact of increased throughput and material utilization on 2J GaInP/GaAs epi-layer costs with MOCVD and D-HVPE

Assumes 30% efficiency and U.S. manufacturing at 50MW/year; the second from the left bar represents a near-term MOCVD scenario; bars 3–5 are MOCVD scenarios based on possible future developments that have not been proven in practice (in the laboratory or at scale); the D-HVPE bar assumes that the laboratory pseudo in-line D-HVPE process described above is successfully scaled-up to 6” wafer areas and achieve high yields, which has also not been demonstrated.

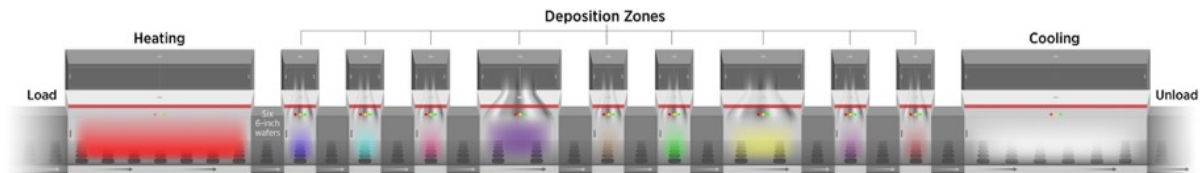


Figure 13. Concept drawing of a high-volume, in-line reactor for depositing III-V solar cells

Six 6-inch wafers move through the reactor in parallel. There is one deposition chamber for each layer of the solar cell, and then length of the chambers are scaled according to the layer thickness and deposition rate.

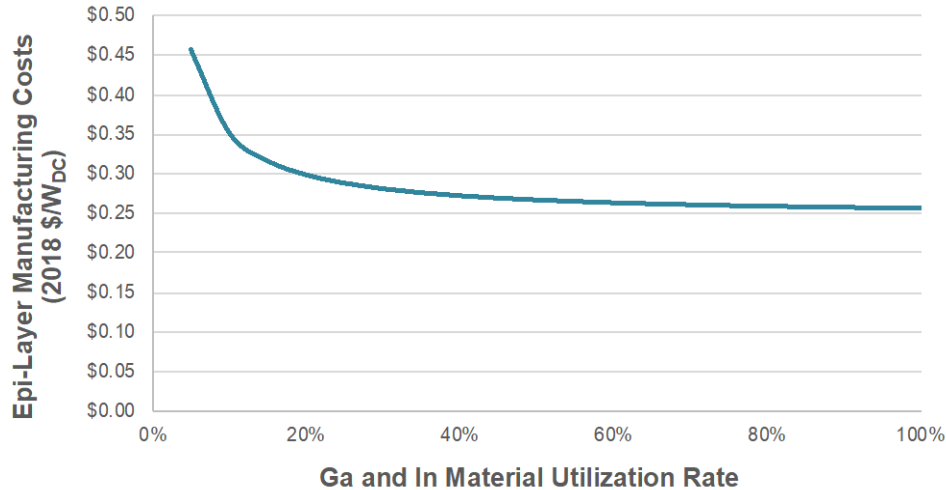


Figure 14. Sensitivity of epi-layer costs for a 2J GaInP/GaAs solar cell grown by D-HVPE to Ga and In material utilization rate

Figure 15 shows the sensitivity of growth costs for a 2J solar cell to additional key input parameters when D-HVPE is used. Figure 16 future illustrates the parametric dependence of epi-layer costs on GaAs deposition rate for a range of GaInP deposition rates.

As with MOCVD, the price of the HVPE tool is an important driver; this contains significant uncertainty at this point, as no commercial D-HVPE tool has been built. The -20% (low bar) value of the HVPE tool price shown in Figure 15 is \$7.4 million/tool (installed) and the +20% (high bar) value of the HVPE tool price is \$11 million/tool, with a reference modeled cost of \$9.2 million/tool.

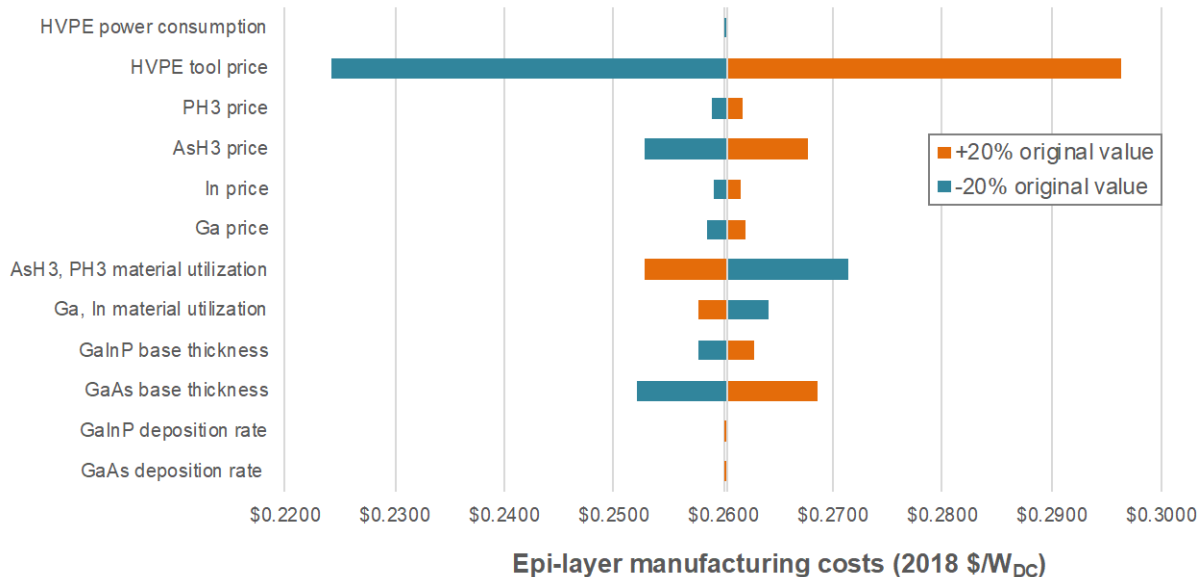


Figure 15. Sensitivity of epi-layer costs for a 2J GaInP/GaAs cell grown via D-HVPE to key input parameters

Assumes 30% cell efficiency and U.S. manufacturing at 50 MW/year

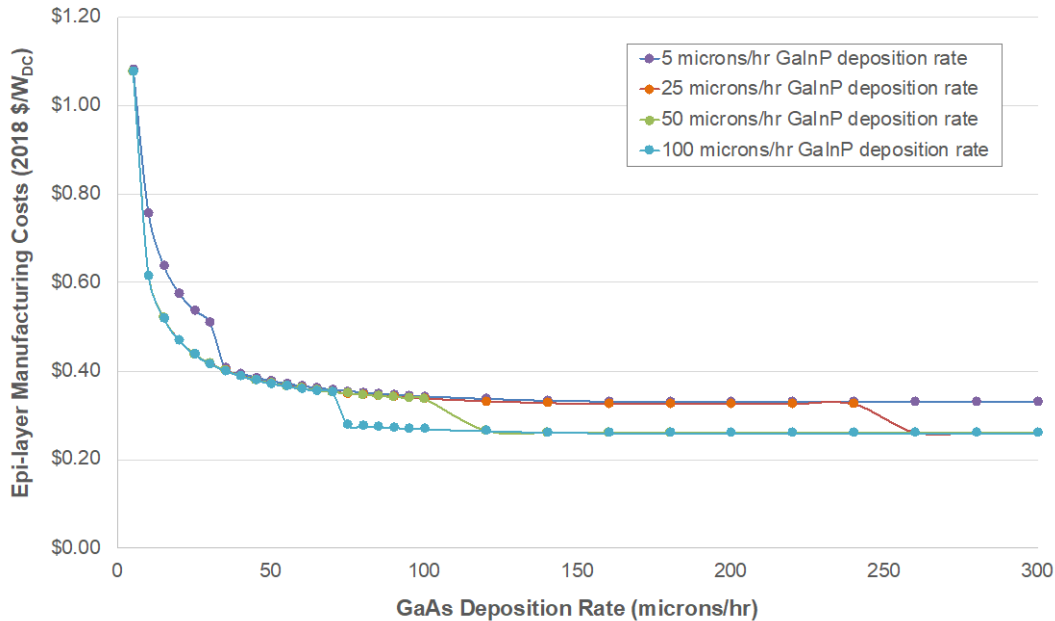


Figure 16. Sensitivity of epi-layer costs for a 2J GalnP/GaAs solar cell grown using D-HVPE to GaAs and GalnP deposition rates

The discontinuous behavior is due to the fact that tools are discrete units.

While per gram costs of precursor materials may decrease further in the future, they are already quite low, with TMG prices in particular having been reduced dramatically in recent years due to scaling and advancements in the LED industry. The TMG price assumed for U.S. manufacturing at 50MW/year is \$0.60/g. Prices as low as \$0.45/g have been reported for Chinese manufacturing as discussed above. This would result in an additional decrease of \$0.01/W to \$0.02/W in epi-costs compared to the fifth bar in Figure 12. Using elemental Ga and In instead of highly engineered trimethyl precursors also presents a fundamental advantage in cost. Any R&D to further reduce the cost per gram of input materials is of value to achieving low-cost III-Vs.

If the future, new growth techniques with similarly high throughputs and low materials costs (through a combination of increased utilization and lower input material prices) could also be developed.

4.3 Lowering Substrate Costs

As we saw in Section Figure 3, when substrate reuses is employed, substrate costs are driven by three primary factors: the substrate price, the number of reuses, and the cost of CMP and reclaim. There are different permutations of improvements in each of these areas that could be used to lower total substrate cost. Figure 17 shows the 2J solar cell manufacturing costs as a function of polishing cost per reuse and number of substrate reuses when ELO is used. For this case, we assume the ELO process has been improved, with additional parallelization in the process for bonding the cell to the handle as well as the use of a large wet etching tool the similar cost and batch size as HF wet processing tools used in the fabrication of c-Si solar cells (Woodhouse, Feldman et al. 2018). The result is a total ELO cost of approximately \$0.10/W. These are assumptions for purposes of illustrating potential costs under this scenario; as previously discussed, ELO costs in volume contain significant uncertainty and very little data are available.

Based on our interviews, we expect that reclaim, or polishing or CMP costs, could reach \$8–\$10/polish using the current process flows at higher volumes. However, these processes have not yet been fully optimized, given the small size of the current market and lack of a need for much lower costs given the overall cost structure of current III-V solar cells. Thus, there is potentially room to further reduce these costs in the future by modifying the polishing and reclaim processes and/or adapting deposition processes to enable epitaxially growth on somewhat rougher surfaces.

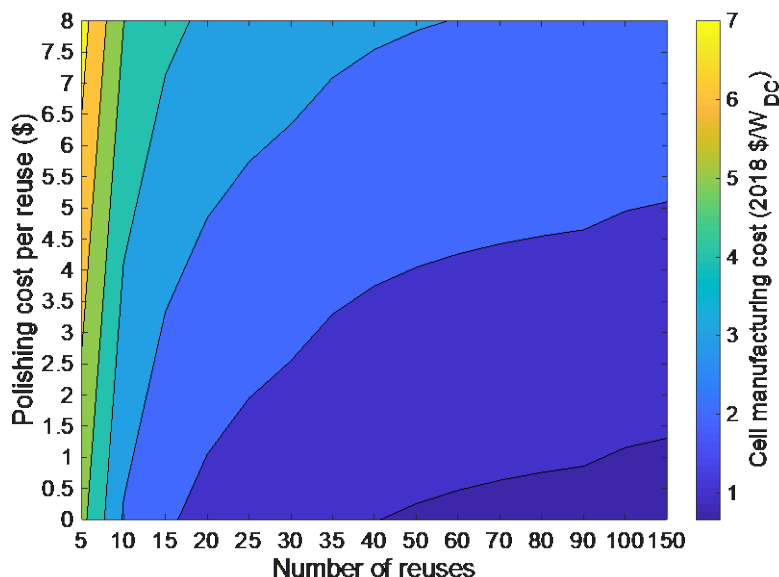


Figure 17. Manufacturing cost for a 2J GaInP/GaAs solar cell deposited using D-HVPE as a function of number of substrate reuses and polishing cost per reuse

\$90/6-inch GaAs substrate; assumes 30% efficiency and U.S. manufacturing at 50 MW/year
 Reductions in cost for the ELO process are assumed compared to our baseline case in Section 3.2.

It is important to note that the ability to achieve low-costs via substrate reuse depends critically on the yield of the lift-off and reuse process, on which there is no publicly available data. We have assumed a 10% additional yield loss associated with the lift-off and reuse process in this analysis. The optimal combination of lift-off, number of reuses, and polishing processes will likely be heavily influenced by yield issues.

An alternative path to lowering substrate costs is growing on a cheaper substrate than GaAs or Ge. This could be, for example, a virtual or engineered substrate, with a thin layer of lattice-matched material (e.g., GaAs and Ge) atop a lower-cost substrate. There has been some R&D in this area (e.g., Lee et al. 2016), but large-area virtual substrates appropriate for this application are not currently fully developed or commercially available. Another option could be to grow directly on a cheaper, lattice mismatched substrate. Direct growth of III-Vs on Si has been researched for both solar and non-solar applications for many years (Soga et al. 1997; Vaisman, et al. 2017; France, et al. 2016), but it has thus far proved challenging to achieve high material quality with this approach. However, this option is potentially appealing because Si wafers are so cheap (\$0.50 to \$1/wafer for a 244cm² wafer) that costs may be competitive in some markets without reuse, and the Si could be used to create a bottom cell in a tandem device. Cost-performance trade-offs and market needs must ultimately be considered for any process. As with reuse, high yield is also important for achieving very low costs. Any issues associated with

thermal mismatch of the substrates, either in manufacturing or after deployed in field (i.e., potential reliability issues) should also be considered. A reduction in the substrate price will result in a proportional reduction in the number of reuses required to achieve the same cost. For example, looking at Figure 17, if the substrate price is halved (to \$45/6-inch wafer), half the number of reuses are required to achieve the same cost for a given polishing cost.

4.4 Low-Cost Metallization

Prevailing metallization approaches for III-V solar cells have often prioritized performance over cost, commensurate with the needs of current markets. In some cases, for example with cells for high-concentration photovoltaic applications, lithographically-defined contacts and high-resolution metal deposition processes are necessary. However, lower cost metallization approaches are required for III-Vs to ever achieve low-cost compatible with more widespread deployment. Lower cost fabrication techniques could include electroplating and screen printing, which have been used for commercial c-Si solar cells. In addition to evaporation, electroplating is already widely used in the fabrication of III-V solar cells for R&D, but almost always a thick layer of gold is plated to maximize efficiency, and often photolithography is still used to define the contacts.

In this section, we explore the potential for using a gold-free electroplating approach to reduce metallization costs. Assumptions about the metal stack assumed are listed in Table 3. This results in a total metallization cost of \$0.06/W at 30% efficiency. This includes full area metallization on the back of the cell. Lower costs—below \$0.02/W at 30% efficiency—could be obtained if Cu-plated or Ag screen-printed contacts similar to those that have been considered for c-Si solar cells could be employed. However, these costs assume only partial coverage of the back of the cell, and thus the efficiency of III-V solar cells with this metallization would be lower. As with everything discussed in this Section, cost-performance trade-offs should be considered to determine the best approach. Additional research is required to fully understand how any type of modified contact affects efficiency and reliability of the device.

Table 3. Assumed Parameters of the Electroplated Contacts

Parameter	Value
Frontside metal stack	Ni (1 μ m)/Ag(500nm)
Backside metal stack	Ag(200nm)/Ni (8 μ m)
Frontside metal coverage ratio	15%
Backside metal coverage ratio	100%
Ag solution cost (\$/kg)	\$462
Ni solution cost (\$/kg)	\$49

It should be noted that metal prices also fluctuate significantly over time, and any fluctuations can affect the overall cost of solar cell contacts. However, for c-Si cells, increases in metal prices have tended to drive improvements that result in lower metal utilization or material substitution in the contacts that counteract some or all of these price increases.

4.5 Putting it Together: A Roadmap to Low-Cost III-Vs

Figure 18 includes an illustrative roadmap for how low-cost 2J III-V solar cells might be achieved. The first stage involves scaling up current production, implementing D-HVPE, increasing the number of substrate reuses, reducing CMP costs, and using low-cost metallization. We estimate that these measures would reduce cost from the baseline cost (Section 3.2) of \$42/W to \$2/W. There are multiple pathways, with different permutations of reductions in substrate, epitaxy, and metallization costs that can be used to reach similar cost levels.

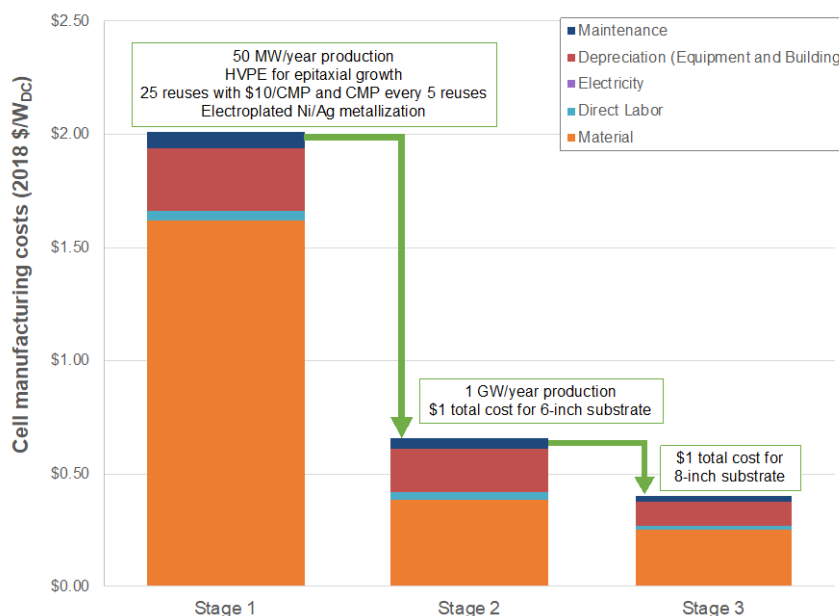


Figure 18. A roadmap to lower III-V solar cell costs

This illustrative example is for 2J GaInP/GaAs cells with 30% efficiency. It assumes U.S. manufacturing.

To reach even lower costs that could enable use of these solar cells in a broader set of markets, further reductions in substrate costs and increases in production volume would be required. We illustrate the potential impact of increasing production to one gigawatt (GW) per year and reducing all-in substrate costs (including substrate price and any lift-off, polishing, and reclaim costs) to \$1/6-inch wafer in Stage 2 of Figure 18. The majority of this cost reduction is achieved through lower substrate costs—using our model, we estimate that costs of \$0.70/W could be achieved at 50MW/year with \$1/substrate, \$0.04/W higher than the costs at 1GW/year. However, as discussed above, there is still significant uncertainty in how manufacturing processes and supply chains might evolve if III-Vs were produced at GW-scale, and our model does not account for any effects of learning-by-doing, which could further drive down costs as cumulative production increases.

A cost of \$1/substrate is equivalent approximately 100 reuses of a GaAs substrate (at today's volume prices) with low ELO costs and no CMP. As discussed in Section 4.3, this cost could also be obtained via the use of an alternative, low-cost substrate without lift-off, or a combination of reduced substrate and CMP costs and a lower number of reuses. Stage 3 in Figure 18 shows the additional savings if \$1 all-in costs for an 8-inch (244cm² when cropped to a pseudo-square) substrate could be obtained. While 8-inch GaAs substrates have been demonstrated (Compound Semiconductor 2002), they are not commercially available today.

There are also several additional avenues for further cost reduction, including thinning the cell layers, increasing manufacturing yield, improving efficiency, and decreasing metal utilization or using alternative, lower-cost metals. Additionally, optimization of the high-volume D-HVPE tool and process (e.g., belt speed and number of wafers in parallel) could result in further cost reductions.

5 Discussion

We find that there is significant opportunity to reduce III-V solar cell manufacturing costs from current levels of above \$50/W to below \$0.50/W. However, achieving the cost reductions would involve significant R&D as well as a scale-up of manufacturing. A cost of \$2/W may be achievable in the relatively near term if (1) increased substrate reuse can be implemented with high yields and reduced polishing or reclaim costs and (2) a commercial D-HVPE can be demonstrated and scaled-up. While a cost of \$2/W is too high to compete in mainstream PV markets, it may be sufficient for certain specialty markets, including portable power for military or outdoor recreation applications, PV on electric vehicles (cars, buses, RVs, trucks), and certain portable small-scale solar systems in developing countries. This would also represent a significant reduction of cost for III-Vs in markets where they are already used, including unmanned area vehicle (UAV) and space applications. These one-sun cell costs would also be tolerable in a low-concentration PV system.

To achieve costs below \$0.50/W, either (1) significant increases in number of substrate reuses above the current state-of-the-art or (2) the use of an alternative, low-cost substrate is required. Additional increases in production volume will also likely be needed. If 8-inch substrates can be used, costs of \$0.40/W may be possible. While \$0.40/W is still higher than c-Si cell manufacturing costs—typical prices for c-Si cells today are typically between \$0.15/W and \$0.25/W—this could enable III-Vs to compete in certain mainstream PV markets because of the advantages of III-V materials, which include their higher efficiency, light weight, and high energy yield.

High-efficiency c-Si cells currently command price premiums in certain markets, particularly residential rooftop markets. Analysis has shown that increasing efficiency can drive balance-of-system cost savings, with possible savings of \$0.26/W, compared to a 19% efficient cell in residential markets based on 2017 pricing (Fu et al. 2017). And, studies have estimated an 8% increase in energy yield for a GaAs solar cell compared to a Si solar cell in Boulder, Colorado (Silverman et al. 2013) because of the lower temperature coefficient and operating temperature of GaAs. These combined factors could allow for a III-V solar cell with a comparable or lower levelized cost of energy (LCOE) in certain markets. III-Vs at this cost could also enable deployment in areas that are weight- or space-constrained. Additional research is required to understand the economic potential for adoption of these solar cells at different costs.

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