CEMAC Clean Energy Manufacturing Analysis Center

A Manufacturing Cost and Supply Chain Analysis of SiC Power Electronics Applicable to Medium-Voltage Motor Drives

Kelsey Horowitz, Timothy Remo,
and Samantha Reese
National Renewable Energy Laboratory

CEMAC is operated by the Joint Institute for Strategic Energy Analysis for the U.S. Department of Energy's Clean Energy Manufacturing Initiative.

Technical Report
NREL/TP-6A20-67694
March 2017

Contract No. DE-AC36-08GO28308

CEMAC Clean Energy Manufacturing Analysis Center

A Manufacturing Cost and Supply Chain Analysis of SiC Power Electronics Applicable to Medium-Voltage Motor Drives

Kelsey Horowitz, Timothy Remo, and Samantha Reese
National Renewable Energy Laboratory

Prepared under Task No. AM05.5500

CEMAC is operated by the Joint Institute for Strategic Energy Analysis for the U.S. Department of Energy's Clean Energy Manufacturing Initiative.

Clean Energy Manufacturing Analysis Center
15013 Denver West Parkway
Golden, CO 80401
303-275-3000
www.manufacturingcleanenergy.org

Technical Report
NREL/TP-6A20-67694
March 2017

Contract No. DE-AC36-08GO28308

NOTICE

Available electronically at SciTech Connect: http:/www.osti.gov/scitech

Available for a processing fee to U.S. Department of Energy
and its contractors, in paper, from:
U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831-0062
OSTI http://www.osti.gov
Phone: 865.576.8401
Fax: 865.576.5728
Email: reports@osti.gov

Available for sale to the public, in paper, from:
U.S. Department of Commerce
National Technical Information Service
5301 Shawnee Road
Alexandria, VA 22312
NTIS http://www.ntis.gov
Phone: 800.553.6847 or 703.605.6000
Fax: 703.605.6900
Email: orders@ntis.gov

Cover Photos: (left to right) iStock 2225189; iStock 16687273; Oak Ridge National Laboratory; iStock 24304597; iStock 26005993; iStock 2069560

NREL prints on paper that contains recycled content.

Acknowledgments

This work was supported by the Advanced Manufacturing Office in the U.S. Department of Energy's Office of Energy Efficiency and Renewable Energy under contract number DE-AC36-08GO28308. We would also like to acknowledge Alfred Hicks (NREL), who created the chip process flow diagrams, and Billy Roberts (NREL), who made the SiC wafer and device map.

Nomenclature or List of Acronyms

DCF	discounted cash flow
kV	kilovolt
MOSFET	metal-oxide semiconductor field-effect transistor
MSP	minimum sustainable price
NREL	National Renewable Energy Laboratory
R&D	research and development
SBD	Schottky barrier diode
SG&A	sales, general, and administrative
Si	silicon
SiC	silicon carbide
VFD	variable frequency drive
WACC	weighted-average cost of capital

Abstract

Wide bandgap semiconductor devices are increasingly being considered for use in certain power electronics applications, where they can improve efficiency, performance, footprint, and, potentially, total system cost compared to systems using traditional silicon (Si) devices. Silicon carbide (SiC) devices in particular—which are currently more mature than other wide bandgap devices—are poised for growth in the coming years. Today, the manufacturing of SiC wafers is concentrated in the United States, and chip production is split roughly equally between the United States, Japan, and Europe. Established contract manufacturers located throughout Asia typically carry out manufacturing of wide bandgap power modules. By modeling regional cost drivers under different scenarios, we illustrate regional cost drives and provide an overview of global supply chain issues to help elucidate key factors that may influence manufacturing location investment decisions. We conduct this analysis for a particular case study where SiC devices are used in a medium-voltage motor drive.

Table of Contents

List of Figures

List of Tables

1 Introduction

Machine drives have historically constituted the single largest end use of electricity in the manufacturing sector (Unruh 2003). In cases where loads are variable, power electronics-based variable frequency drives (VFDs) are more efficient than the systems employing relatively inefficient gearboxes and mechanical throttles that typically used today. The use of wide bandgap (WBG) semiconductors can provide an additional boost to VFD efficiency, as well as allow them to operate efficiently at higher voltages, powers, temperatures, and switching frequencies. Because of reduced cooling requirements, lower part counts, and the possibility of using smaller passive components, WBG-based power electronics can also reduce the footprint and potentially the system cost of VFDs.

Silicon carbide (SiC) is a WBG semiconductor material that is available for use in commercial power electronics systems. While the current SiC market is small, comprising less than 2% of the total power semiconductor market, the market share is predicted to increase steadily over the next 5 years to comprise between 3 and 7 percent of the total market, with pronounced growth in motor drive applications; IHS also predicts continued growth through 2025 (Yole Développement 2016; IHS 2016). This presents an opportunity not only for energy savings, but also for manufacturing growth. This work aims to provide insights into 1) global manufacturing opportunities in this space, and 2) drivers of manufacturing plant location decisions, including the potential for specific policies, innovations, or other factors to influence where manufacturing plants are located. To achieve these aims, we provide an overview of the current state of global manufacturing as well a regional, bottom-up cost analysis of components along the value chain.

A simplified diagram of the value chain for manufacturing SiC power electronics in VFDs is shown in Figure 1. SiC boules (crystals) are grown, machined into ingots, and then sliced into substrates, which are subsequently polished. A thin SiC epitaxial layer is then grown on top of this substrate to create an epi-wafer. The epi-wafer is processed to make SiC semiconductor devices—transistors or diodes (individually referred to as die). The transistors and diodes are then either integrated into a power module[1] or discretely packaged. These power electronic components can then be integrated into the VFD, along with other low voltage circuitry (gate drivers, control circuit boards, etc.).

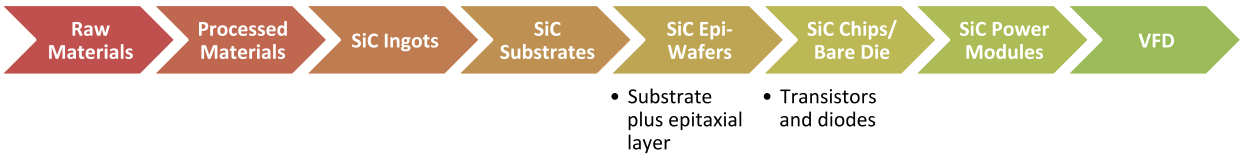

Figure 1. Simplified value chain diagram for SiC-based VFDs

[1]There are two ways to use SiC devices in VFDs. Bare dies may be integrated into power modules, which are then used in the VFD, as discussed here. Alternatively, bare dies may also be packaged into discrete SiC devices, which are then integrated onto a printed circuit board that goes into the VFD. Both of these approaches are used today. Several companies have proposed using hybrid Si/SiC or full-SiC power modules for medium-voltage motor drive applications in particular.

A significant fraction of the electricity is consumed by medium-voltage, high-power electric motor drives, which are used in chemical, oil, gas, mining, and manufacturing industries (Wolk 2014). Medium-voltage motor drives are usually defined as those with voltages between 2 kilovolts (kV) and 15 kV and powers between 0.2 megawatt and 40 megawatts. Today, SiC transistors and power modules are only commercially available for voltages up to 1.7 kV. However, 3.3-kV components have been developed by several companies, are available as engineering samples, and are expected to become more widely available in the coming years. There is also active research on higher-voltage SiC components, but these are currently at an earlier stage of development. For this analysis, we have chosen to focus on the case of 3.3-kV SiC chips and power modules used in a 1-megawatt VFD.

2 The Current Supply Chain for SiC-Based VFDs

2.1 Methodology for Selecting Materials for Supply Chain Analysis

In this section, we provide an overview of the current supply chain for most prevalent commercial designs and manufacturing processes associated with each link in the value chain for SiC-based VFDs (Figure 1). These designs and processes, as well as the materials associated with them, were determined via NREL primary interviews with members of industry and/or subject experts, literature and market reports (where available), and product datasheets. We then selected a sub-set of these materials for each value chain link for discussion based on the criteria outlined in (CEMAC 2017). Whether a given material meets these criteria was evaluated using NREL interviews with industry members and subject experts; data from the U.S. Geological Survey (USGS), the U.S. International Trade Commission (USITC), the International Trade Center, or literature/market reports (where available); and common knowledge (e.g. that carbon is not a fundamentally constrained material).

Because we focused on the designs and processes that are most prevalent in industry today, this analysis does not necessarily apply to all designs in the market or to emerging designs. Additionally, the SiC industry is relatively new and not widely tracked, and some of the supply chain data was available from only a limited number of sources. We attempted to mitigate any data limitations by having industry and other experts review the data and provide feedback, but some uncertainty in this information should be assumed.

2.2 Raw Materials

Silver and gold are often used as part of the metal contacts to SiC transistors or diodes. The supply of these materials is spread globally, reducing the risk associated with any import or export tariffs that may be placed on them. The largest producers of mined silver in 2014 and 2015 were China, Mexico, and Peru, but significant amounts were also produced in other countries around the world; gold was also mined globally during these years, with top producers being China, Russia, Australia, and the United States. The second exception is diamond, which is used in the wire used to slice SiC ingots into wafers, as well as in the slurry used for polishing wafers. Diamond is required for these processing steps because of the hardness of SiC. Both natural and synthetic diamond is used for industrial purposes, including cutting and polishing in other semiconductor applications. According to the USGS, 95% of the U.S. industrial diamond market now uses synthetic diamond (U.S. Geological Survey 2016). At

least 15 countries have the technology to produce synthetic diamond, including the United States, whose primary and secondary production in 2015 are estimated at 111 million carats and 38.3 million carats, respectively. China is currently the world's leading producer of synthetic industrial diamond, exceeding 4 billion carats of production in 2015 (U.S. Geological Survey 2016). Mine production of diamond is led by Australia, Botswana, Congo (Kinshasa), Russia, South Africa, and Zimbabwe.

Si and carbon (C) are the raw materials used in the greatest volume in SiC chips. These materials are earth-abundant, available globally, and do not pose a supply chain constraint.

2.3 Processed Materials

High-purity SiC powder, which can be used to grow SiC boules, is only available from a limited number of suppliers, and is relatively expensive. High purity silane (SiH_4) is a critical precursor for growing SiC layers in the chips and is typically produced by large, multinational industrial gas companies. Firms headquartered in the United States, Asia (China, Japan, Hong Kong, South Korea, and Taiwan), and Europe (Germany and France) currently produce silane.

2.4 SiC Substrates/Wafers

Figure 2 shows the percent of global wafer production by region/country. The locations shown correspond to where the wafers are manufactured, not the location of company headquarters. In Europe, wafer production facilities are located in Germany, Sweden, and Russia. In Asia (except for Japan), production is located in China and South Korea. In 2015, SiC wafer manufacturing capacity exceeded demand (Yole Développement 2016).

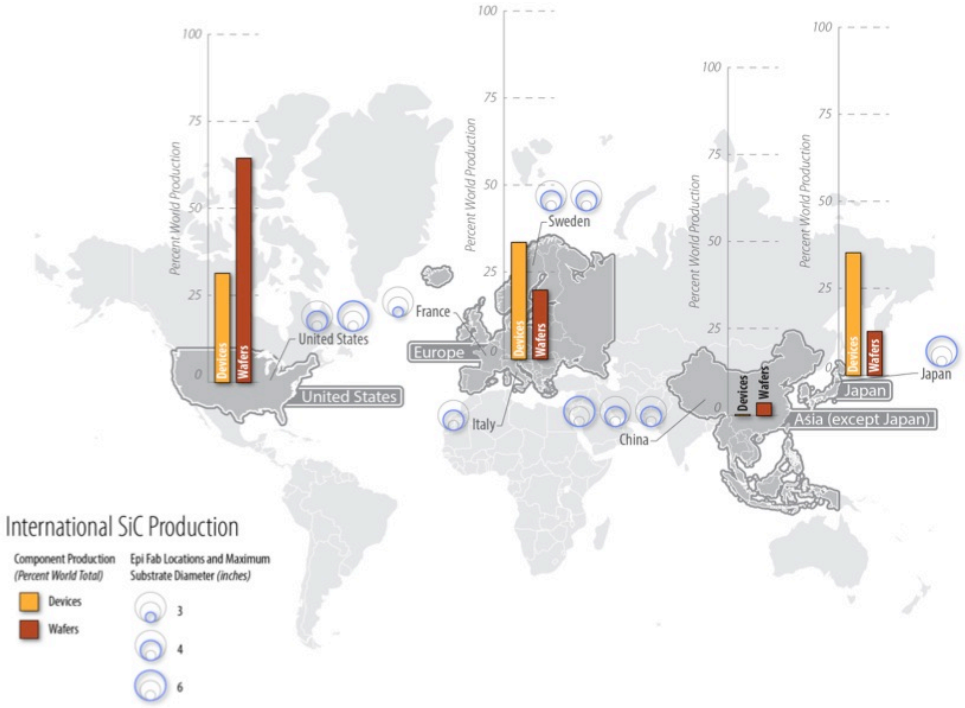

Figure 2. Map of global production of SiC wafers (substrates and epi-wafers) and devices with locations of SiC epi-fab facilities in 2016

Data source: Power SiC 2016: Materials, Devices, Modules, and Applications report, (Yole Développement 2016).

Typically, the companies that grow SiC boules also machine them into ingots and slice them to create substrates. A few of the companies that manufacture ingots and substrates also provide epi-layer growth and sell epi-wafers; these include Cree (United States), Dow Corning (United States), SiCrystal (Japanese-owned, German manufacturing), Nippon Steel (Japan), Norstel (Sweden), and SICC (China). The blue circles in Figure 2 indicate which countries have facilities for epitaxial growth and what wafer sizes can be produced by companies located within each country.

As can be seen from Figure 2, the United States is currently the global leader in production in terms of wafers/year of production of SiC substrates and wafers, followed by Europe and Japan. The quality of the SiC substrate is critical to achieving high-quality chips, and the SiC substrate constitutes a major portion of the chip cost. Thus, the distribution of SiC substrate and epi-wafer manufacturing has mostly been driven by where the companies that are able to achieve high-quality wafers with good yields are located. The choice to locate plants in certain locations has been driven largely by the existence of existing facilities and capabilities in that location. Some companies (like Dow Corning) have leveraged their own facility space, while others have acquired companies with existing SiC substrate manufacturing facilities and expertise (e.g., ROHM's acquisition of SiCrystal in 2010). Cree produces SiC substrates in relatively high volumes for the light-emitting diode market, allowing it to build expertise and realize additional economies of scale that would not be possible given the level of current demand for SiC power electronics.

The ownership and manufacturing locations for these firms can also be influenced by direct regulatory action. For example, Cree, a U.S. firm with much of its manufacturing in the United States, previously spun off the portions of its business related to power electronics and radio frequency electronics into Wolfspeed. German company Infineon planned to acquire Wolfspeed, but the deal was recently canceled because Cree could not sufficiently address national security concerns from the Committee on Foreign Investment in the U.S.[2]. The U.S. government has blocked other deals in the semiconductor space in the past over similar concerns.[3]

The cost of epi-growth and chips can also be reduced by the use of larger-area substrates (Agarwal, 2016; NREL cost analysis), so manufacturers that are able to successfully fabricate 6-inch (150-mm) diameter substrates with acceptable quality also have an advantage, which will be reinforced as 6-inch wafers gain market share in the coming years.[4] Cree, II-VI, and Dow Corning—all companies with U.S. manufacturing facilities—currently dominate the supply of 6-inch SiC wafers; however, SiC 6-inch wafers sales were estimated at only 6 to 7.5 percent of total wafer sales in 2016.

---

[2] Dylan McGrath. "Cree, Infineon nix Wolfspeed deal over U.S. government worries," *EE Times*, February 20, 2017, http://www.eetimes.com/document.asp?doc_id=1331375.
[3] Matthias Inverardi and Diane Bartz. "Obama bars China's Fujian from buying Aixtron's U.S. business," *Reuters*, December 2, 2016, http://www.reuters.com/article/us-aixtron-m-a-fujian-idUSKBN13R0DU.
[4] Four-inch (100-mm)-diameter wafers are currently used more commonly than 6-inch (150-mm) wafers.

While the share of Chinese firms in the SiC substrate market was only 3 to 4 percent in 2015, several Chinese firms have recently made significant investments in SiC substrate and epi-wafer manufacturing, nearly doubling global capacity, with additional expansions announced for coming years (Yole Développement 2016). Additionally, the Chinese government has supported the development of this industry by providing subsidies for equipment, and new plants have been financed with a combination of local government funding and private investment. Additionally, our interviews with industry members indicate that it may be possible for some firms to obtain certain materials used in manufacturing SiC wafers at lower cost in China. However, most of these firms have demonstrated only 4-inch-diameter wafers and are still developing the ability to produce high-quality substrates and/or epi-layers and are working to improve yields.

The global capacity utilization for SiC substrates in 2015 was estimated at 33 to 39 percent (Yole Développement 2016).

2.5 SiC Chips

SiC chip production is currently split roughly equally among the United States, Japan, and Europe (Figure 2). The top seven SiC chip manufacturers, which combined have over 95% of the market share, are large, multinational companies that were already established in the Si power electronic device space, and all have vertically integrated a significant portion of the value chain, including final systems integration/applications. If the announced acquisition of Wolfspeed by Infineon is carried out, Infineon may have nearly 50% of the SiC device market (Infineon 2016).

Many new entrants in SiC chip manufacturing are SiC pure-players, producing only SiC materials, and are focused on processing devices, a single piece of the value chain.

Over the last several years, China has made significant investments in developing a local semiconductor industry. SiC has been included in this, with the government providing significant funding for development of SiC chip manufacturing. Chinese SiC chip manufacturers have begun to enter the market and are looking to scale up production. Typically, Chinese SiC chip manufacturers (as well as Chinese manufacturers of SiC substrates, epi-wafers, and systems) are not vertically integrated.

2.6 SiC Power Modules

SiC power module manufacturing and manufacturing of power modules in general currently fall into two categories: 1) vertically integrated approaches, where companies have in-house manufacturing facilities, particularly in cases where highly customized modules are used; and 2) the use of contract manufacturers, which are overwhelmingly located in Asia. Our interviews with members of the industry indicate that contract manufacturing is more commonly used for higher volume production, where economies of scale can be realized by tapping existing facilities and supply chains for manufacturing Si power modules. SiC power modules are manufactured and shipped globally.

Quantitative data on SiC power module production volumes by country are not available. Additionally, existing trade codes do not provide specificity sufficient to map the global trade of these components. However, System Plus Consulting has assembled a database of locations where SiC and/or mid-to high-power Si power modules for manufacturing facilities owned and operated by several leading power electronics firms (System Plus Consulting 2015, NREL research), shown in Table 1. As can be seen from this table, these facilities are concentrated in China, Japan, Southeast Asia, and Europe, with one location within the United States. However, our interviews indicate that many of these companies are using contract manufacturing for producing their modules in volume. This allows companies to leverage existing facilities—avoiding the need for need capital investments—and take advantages of additional economies of scale. Contract manufacturing facilities used for Si-based mid- and high-power modules can also be used for SiC, and a similar approach could be followed for SiC power modules as the industry grows. Contract manufacturing of power modules takes place primarily in China and Southeast Asia.

Table 1. Manufacturing Locations for Medium-Voltage Power Modules (Mostly Used for Si Power Modules Today) for Several Leading Companies

Company	Country
Microsemi	France
Danfoss	Germany
Infineon	Germany, China
Semikron	Germany
Vincotech	Hungary
STMicro	Italy, Singapore
Hitachi	Japan
Mitsubishi	Japan
Renesas	Japan
Fuji Electric	Malaysia, Taiwan
Rohm	China
Fairchild	South Korea
ABB Semiconductor	Switzerland
Toshiba	Thailand
Cree/Wolfspeed/APEI	United States

2.7 SiC-Based VFDs

The total number of medium-voltage VFDs sold each year is very small: only 12,000 units were sold in 2015 (Zhou 2016). To our knowledge, there are no full-SiC VFDs produced commercially for use in industry today. Manufacturing production and capacity information for any medium-voltage VFDs is sparse, and trade codes are insufficient to determine how these specific types of drives are shipped globally. However, our interviews with members of industry indicate that medium-voltage VFDs in general (i.e., VFDs with Si or SiC power electronics) are primarily assembled close to the end customer. Many VFDs are semi-customized, and locating

manufacturing facilities close to the end customer allows for rapid response to customers, reduced lead times, and decreased uncertainty in lead times.

Many leading manufacturers of medium-voltage VFDs are large, multinational companies that have assembly plants throughout the globe and thus are able to respond to local markets. In 2015, the United States was the largest market for medium-voltage drives by revenue (30.0%), followed closely by China (28.6%). Europe, Middle East, and Africa regions; Japan; and the rest of Asia (excluding China and Japan) accounted for 24.7%, 4.7%, and 11.9% of the 2015 market respectively (Zhou 2016).

3 Regional Cost Analysis

Regional cost analysis of SiC ingots, substrates, epi-wafers, chips, power modules, and VFDs was performed using CEMAC's bottom-up cost modeling approach. Section 3.1 discusses the methodology used for analysis of each of these components. Results obtained using this approach are presented in Section 3.2.

The SiC industry is rapidly evolving, and costs are expected to decrease along the value chain. This work provides a snapshot of costs under a set of assumptions at the time of analysis, and these results do not reflect the potential cost reduction that may be achieved in the future. Rather, this cost analysis seeks to provide insights into current cost driver, and how these may vary by location of manufacturing, as part of the overall effort to understand drivers of manufacturing location decisions and the potential of the global supply chain to evolve as this industry develops.

3.1 Cost Analysis Methodology

For each component analyzed, a representative manufacturing process flow is developed based on a literature review, interviews with industry and subject experts, and other secondary sources (e.g., company websites, news articles, market reports). Where process flow information was obtained for each component is detailed in the following sections (Sections 3.1.1 – 3.1.4). A total-cost-of-ownership model is then created for each step in this process flow. The total-cost-of-ownership model includes the costs associated with materials, labor, utilities, facilities, equipment, and equipment maintenance. The costs assume that all equipment is purchased new at full price. Process-specific input data—e.g., labor requirements, throughputs/cycle times, material and electricity usage, material pricing—are collected from industry members, material suppliers, equipment manufacturers, and market reports. Most data from industry members and equipment manufacturers are collected via interview, and data from material suppliers are obtained via request for quotes or interviews. The ability of NREL to collect this input data relies on our ability to build trust with industry and protect proprietary or business-sensitive information from individual companies. Often, this can be achieved by collecting data from many different sources and providing only aggregated anonymized information. However, in cases where an only a small number of data points (or only one data point) can be obtained for a given input, and thus the data cannot be sufficiently anonymized, we are unable to publish specific input assumptions. Key input assumptions for the cost models that can be publicly disclosed are included in the appendix.

This bottom-up manufacturing cost modeling approach has been used by CEMAC/NREL in the past for a several of different technologies and has previously yielded results in line with reported data on costs and prices (Woodhouse et al. 2016; Chung and Elgqvist 2016).

Country-specific input data, including labor rates for different types of labor and electricity prices, are taken from the Clean Energy Manufacturing Analysis Center database of country costs. Labor and electricity costs are taken from the U.S. Bureau of Labor Statistics and Energy Information Administration, respectively; if data are unavailable from these sources, interviews, market reports, and other web sources are used to supplement. Table 2 details the country factors that are common across the components in this analysis; assumptions specific to different components are provided in Sections 3.1.1 through 3.1.4 and in the appendix. We assume the same labor count—the number of laborers required per step— regardless of the country of manufacturing. The corporate tax rates used for each country were taken from PwC (2011). These tax rates correspond to the average effective corporate tax rate for multiple firms in each country. A total of 1,820 companies were included in the analysis. More recent data on effective corporate tax rates are not available for all the countries covered in this analysis. Tax rates are used in calculating the minimum sustainable price, discussed below, and do not affect the manufacturing costs.

The China costs used in this analysis correspond to the costs associated with manufacturing in urban regions of China, where most manufacturing currently is located (e.g., Shanghai, Shenzhen, and Guangzhou). However, prior work has indicated that rural, western regions of China can have substantially lower labor and electricity costs if issues of severe weather, shortage of skilled labor, and transportation challenges could be mitigated to allow for large-scale manufacturing (Fu, James, and Woodhouse 2015).

Table 2. Country Factors for Countries Included in this Analysis

Country	Effective Corporate Tax Rate (%)	Industrial Electricity Price ($/kWh)
Austria	19.7%	$0.135
China (Urban)	21.5%	$0.110
Germany	27.9%	$0.179
Hungary	13.7%	$0.123
India	19.4%	$0.070
Italy	29.1%	$0.328
Malaysia	22.8%	$0.100
Japan	38.8%	$0.175
South Korea	24.3%	$0.100
Sweden	22.0%	$0.082
Switzerland	20.7%	$0.130
Taiwan	14.4%	$0.090
United States	27.7%	$0.060

In addition to computing manufacturing costs using the methodology described above, we also compute a minimum sustainable price (MSP). The MSP corresponds to the price at which the net present value of the investment in the manufacturing plant is equal to zero, and the internal rate of return is set equal to the weighted average cost of capital. The MSP represents the minimum price that, at a specific instance in time, would be required to cover all variable and fixed costs and repay investors at their expected rate of return. MSP is different from market price and does not reflect the effects of economic factors like supply and demand. The MSP may be above or below market prices.

The MSP is calculated using a *pro forma* discounted cash flow (DCF). Research and development (R&D) and sales, general, and administrative (SG&A) costs used in this model are typically input as a percent of revenue. For all cases and components, we use a 20-year cash flow analysis period. Specific assumptions about R&D, SG&A, and cost of capital for each component are discussed in Sections 3.1.1 through 3.1.4.

Observed differences in regional costs depend not only on "core" country factors—labor costs, electricity prices, and taxes—but also on the approach and capability of specific firms that are located in a given country, the availability and cost of capital, and on government policies and support. We present results associated with a base case, where only the core country factors are included, and then discuss the effects of different parameters that are not inherently related to manufacturing location on costs.

3.1.1 SiC Ingot, Substrate, and Epi-Wafer Cost Model

The manufacturing process flow used for calculating the costs associated with growing a SiC boule, creating SiC substrates from the boule, and epitaxially growing SiC on the substrate to create the epi-wafer is shown in Figure 3 (Müller 2000; Wijesundara 2011; NREL primary interviews). Some details are omitted to protect business-sensitive information. According to our interviews, the process flow is similar for different wafer diameters, although some parameters may be tweaked. Process flows may vary by company and polytype, or variations in the crystal structure. Currently, the crystal growth process is often semi-automated, with some manual loading and unloading or transport between stations. However, because of the long cycle time, only a small number of laborers are required per plant.

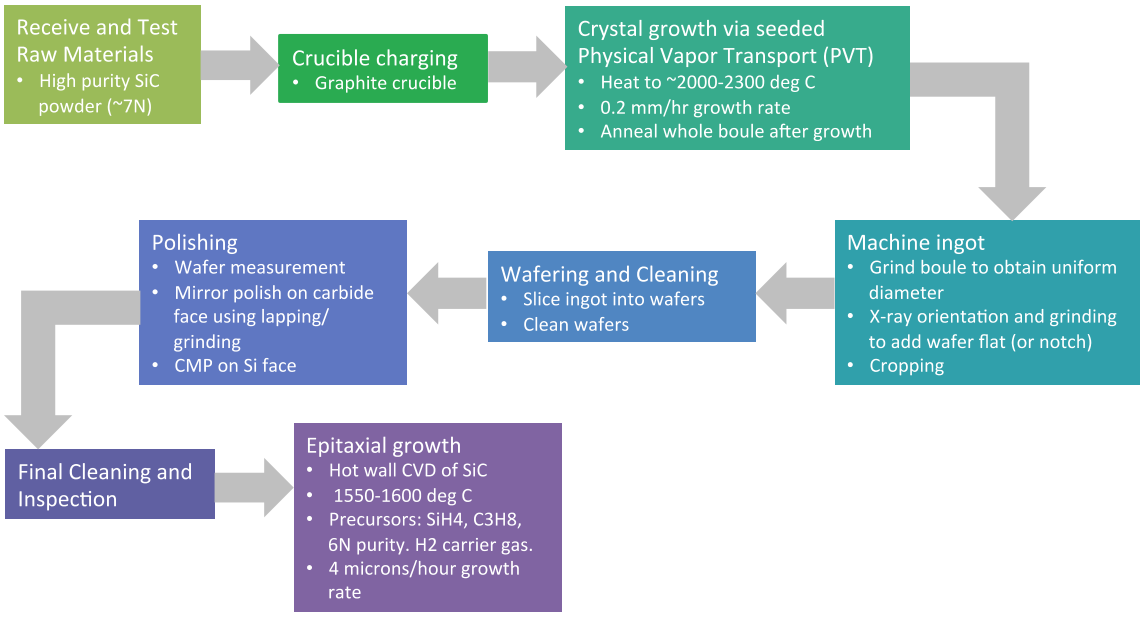

Figure 3. Manufacturing process flow used for calculating the costs associated with growing a SiC boule, creating SiC substrates from the boule, and epitaxially growing SiC on the substrate to create the epi-wafer

Key properties of the SiC wafer modeled are shown in Table 3. The thickness of the epi-layer (drift layer) was chosen based on literature (Agarwal et al. 2016; Hamada et al. 2015; Runhua et al. 2015; Sakai et al. 2015). While commercially available SiC wafers used for lower voltage (1.7 kV and below) are thinned using a backgrinding process, our interviews indicate that this step is not necessary for 3.3-kV devices; we assume the 350-µm substrate is used as is. The 4H polytype is currently the most prevalent and is expected to dominate the market in the coming years (Yole Développement 2016).

As mentioned above, 4-inch (100-mm) SiC wafers are currently the norm, with an estimated 6 to 7.5 percent of sample devices fabricated on 6-inch (150-mm) wafers. However, the share of 6-inch wafers is expected to increase in coming, and several SiC chip manufacturers either already have or are installing 6-inch manufacturing lines with the expectation that this will allow for lower costs (Yole Développement 2016; IHS 2016; Agarwal 2016; NREL primary interviews). For these reasons, we chose to focus on our cost analysis on the 6-inch case.

In 2015, II-VI exhibited the first 200-mm SiC substrates, but these substrates are not yet commercially available.

Table 3. Key Parameters of the SiC Wafer Modeled

Property	Value	Units
Wafer diameter	6 (150)	inches (mm)
Wafer thickness	350	µm
Epi-layer thickness	30	µm
Wafer doping	n+	
Polytype	4H	

For the base case, we assume that all countries have a production volume of 5,000 6-inch wafers per month and that manufacturing capacity is fully utilized. If capacity is underutilized for a given plant, costs per unit will increase; currently, there is an oversupply of SiC wafers in the market, and some capacity may indeed be underutilized.

Labor requirements were divided into two categories to calculate labor costs: semiconductor processes and first-line supervisors. The number of these types of laborers required per tool for each step in the manufacturing process is collected from industry members and equipment manufacturers, and then the total number of laborers in each category calculated as the labor requirement per tool multiplied by the number of tools required to meet 5,000 wafers per month. The hourly cost assumed for these types of workers by country is included in the appendix.

Table 4 lists the key financial assumptions used in the SiC wafer DCF model. These assumptions are common for all countries in our analysis. All data on the cost of debt, cost of equity, D/(D+E) ratios, SG&A, and R&D costs were taken from companies' publicly available financial reports. The fraction of financing from debt (D/(D+E)), SG&A, and R&D costs (as a percent of revenue) were assumed to be equal to the average of these values for Cree and II-VI (two leading manufacturers of SiC substrates) at the end of June 2016. Because these companies are public, these data are available in their financial statements; similar data could not be obtained for other manufacturers. The cost of equity was calculated for Cree and II-VI using the capital asset pricing model. The cost of debt was calculated based on an estimated average debt rating. If a debt rating was not provided in the financial statement, the company's interest expense ratio (earnings before interest and taxes/interest expense) was used to estimate it. At this early stage in the industry, it is likely that the cost of capital is more sensitive to firm-specific factors than the country (location) of manufacturing. For this reason, we applied the same cost of capital assumptions to all countries in the analysis.

Table 4. Key Financial Assumptions for the SiC Wafer DCF Model

Parameter	Value
Cost of debt	3.61%
Cost of equity	13.56%
D/(D+E)	35.98%
SG&A costs (% of revenue)	18.5%
R&D costs (% of revenue)	8.9%
Inflation	2%
Equipment depreciation period	7 years
Building depreciation period	20 years

3.1.2 SiC Chip Cost Models: MOSFETs and SBDs

Many steps in the process of fabricating SiC power chips are similar to those used for Si insulated gate bipolar transistor power chips; for these steps, the same general tool set can be used. However, there are several steps that must be added or modified for the case of SiC, including the addition of a high-temperature anneal, a backside laser anneal, and some modifications to the metallization and metal etching and ion-implant processes (X-FAB, n.d.).

The capital equipment requirements for these changes are relatively small compared to the total capital expenditure associated with a complete semiconductor fabrication.

Simplified diagrams of the process flows used for calculating the costs of SiC MOSFETs and SBDs are shown in Figure 4 (page 12).

X-FAB is currently modifying its Si chip line in Lubbock, Texas, to be able to produce 5,000 wafers (6-inch) per month ("X-FAB offers high-volume 6-inch SiC foundry production," 2016). Because of this, we have chosen to model metal-oxide semiconductor field-effect transistor (MOSFET) and Schottky barrier diode (SBD) costs at 5,000 (6-inch) wafers per month for our base case.

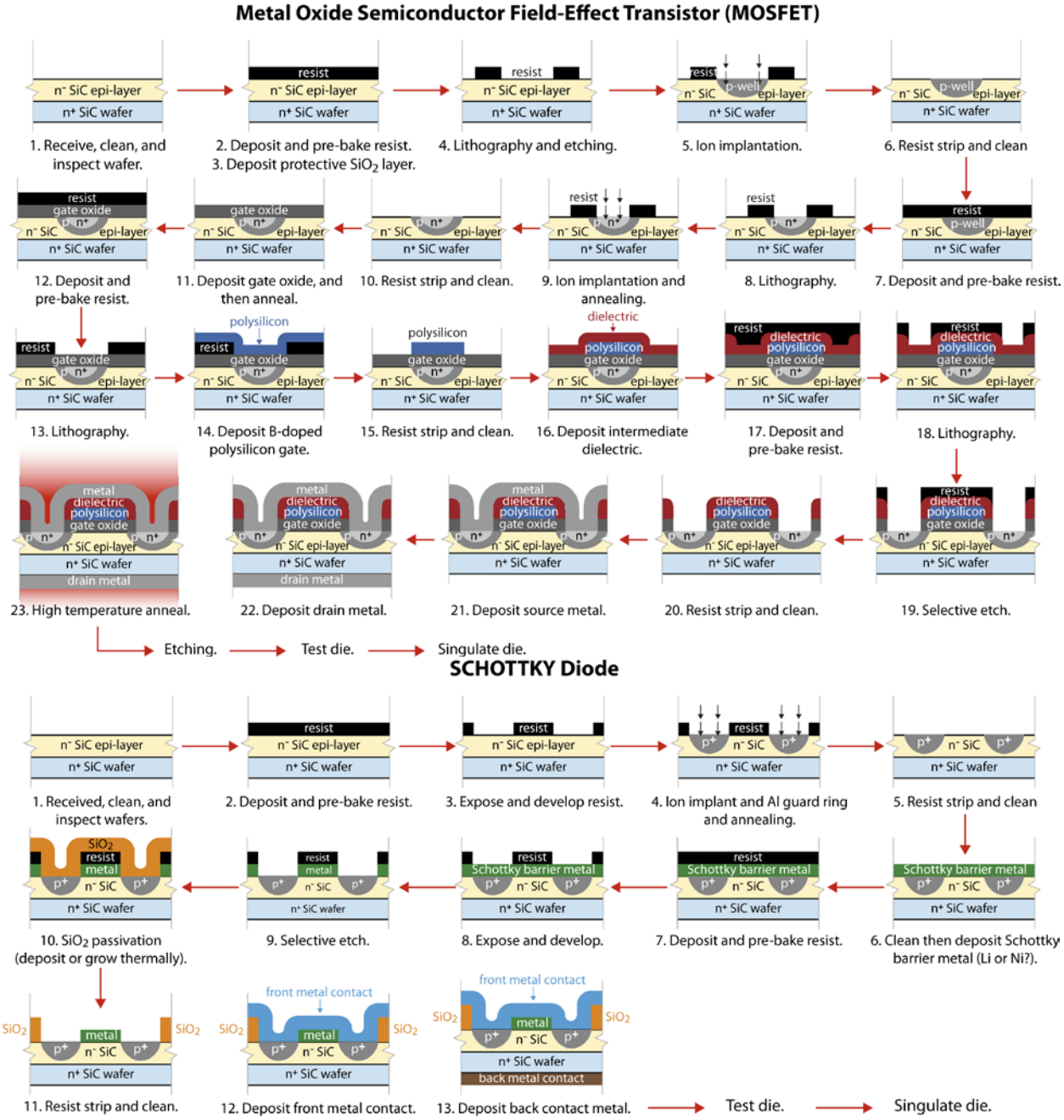

Figure 4. Manufacturing process flow used for calculating the costs associated with manufacturing SiC MOSFETs (top) and SBDs (bottom)

Table 5 lists the key design assumptions made for SiC MOSFETs and SBDs in our cost model. We use the U.S. base case MSP calculated using our model for the epi-wafer as the epi-wafer price. The die area for the MOSFET is taken from Agarwal et al. (2016) and assumes an on-resistance of 7.8 milliohms per square centimeter (mΩ-cm2) — this is low compared to leading production devices today, and so chip areas in the near term (and thus costs per chip) may be higher. The 25-mm2 SBD die area is based on a current rating of 20 amps. Sensitivity analysis was conducted over a range of die sizes given that there is some uncertainty in these sizes.

Table 5. SiC MOSFET and SBD Design Parameters

Parameter	SBD Value	MOSFET Value
MOSFET type	N/A	Planar, DIMOSFET
Die area	25 mm^2	8 mm^2 (Agarwal et al. 2016)
No. of dies per 6-inch wafer	605	1,951
6-inch epi-wafer price	$1,572	$1,572
Source metallization	N/A	Al (4 μm)
Drain metallization	N/A	Ni (0.8 μm) / Ag (0.6 μm)
Polysilicon gate thickness	N/A	500 nm
Gate oxide thickness	N/A	50 nm
Inter-metal dielectric thickness	N/A	1 μm
Schottky contact	Ni (150 nm) / Ti (30 nm)	N/A
Ohmic contact	Ti (5 nm) / Au (300 nm)	N/A

Table 6 lists the key financial input assumptions used for the SiC chip DCF models. These inputs are used for calculating the MSP of both MOSFETs and SBDs. The cost of debt and equity was calculated in the same way as for wafers (described in Section 3.1.1), and the D/(D+E) ratio was again taken from the companies' balance sheets. The average values of Cree and STMicroelectronics—two SiC chip manufacturers that are public in U.S. markets—were used. The reported spending on SG&A and R&D for Cree, STMicroelectronics, and Infineon (for the latest available date) was averaged to obtain the values used in our analysis. As for SiC substrates and wafers, all data is taken from publicly-available financial reports.

Table 6. Key Financial Assumptions for the SiC Chip DCF Model

Parameter	Value
Cost of debt	2.82%
Cost of equity	17.31%
D/(D+E)	33.20%
SG&A costs (% of revenue)	14.0%
R&D costs (% of revenue)	14.5%
Inflation	2%
Equipment depreciation period	7 years
Building depreciation period	20 years

3.1.3 SiC Power Module Cost Model

As mentioned in Section 1, 3, 3-kV full-SiC power modules have been developed, but are not commercially available today. We used a modified version of a 1.7-kV SiC half-bridge power module. This module consists of housing, connectors, and a direct-bonded copper substrate sintered to a baseplate. The SiC chips are direct soldered to the direct-bonded copper substrate and connected with aluminum wire bonds. Our model assumes that twelve 3.3-kV SiC MOSFETs and twelve 3.3-kV SiC SBDs are included in each power module. We assume that the price of these chips is equal to the modeled MOSFET and SiC MSPs for different countries, detailed in the appendix. The overall package dimensions are assumed to be 106 mm x 62 mm x 30 mm.

Currently, many companies use packaging very similar or identical to that used for Si-based power modules for the same voltage and power ranges. This allows firms to leverage existing capabilities when expanding their offerings to include SiC products. In the future, there is significant room for improving and tailoring power electronics packaging to SiC, including the use of new packaging materials, modifying the interconnects, using alternative architectures (e.g., stacked architectures), the use of integrated capacitors, or changes to the die attach process (Cole et al. 2015; Lee et al. 2008; Richmond et al. 2009; Khaja et al. 2013. These improvements are not explored here.

The manufacturing process flow used for our power module model is shown in Figure 5. This process flow is based on literature review (Lee et al. 2008; Sheng and Colino 2004; Stevanovic 2012) and information in the Power COSIM+ model (System Plus Consulting 2015). We assume a production volume of 1 million packages per year for all countries. Financial assumptions were the same as those made for chips, listed in Table 6. We assume that direct line workers are semiconductor processors supervised by first-line supervisors.

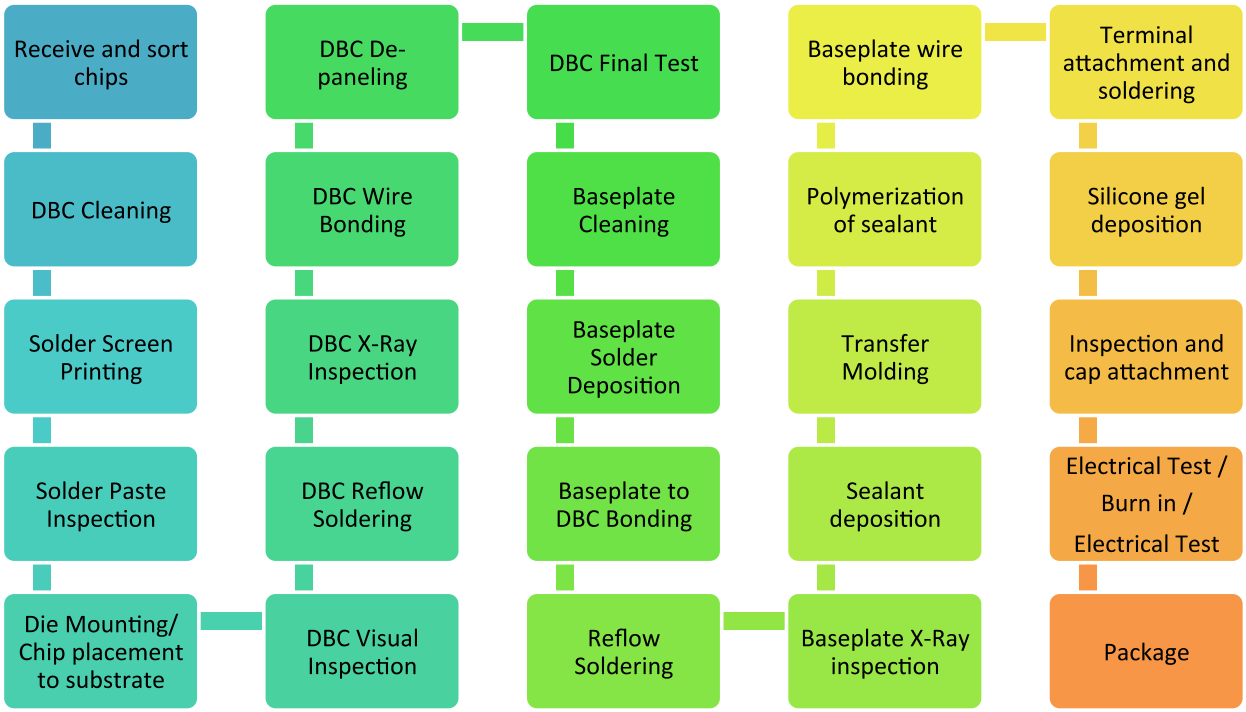

Figure 5. Manufacturing process flow used for calculating the costs associated with the SiC power module.

3.1.4 SiC-Based VFD Cost Model

The manufacture of medium-voltage VFDs consists of assembling purchased components into a final product. This is a largely manual process with multiple manual process steps. Some include wiring configurations, and some include moving heavy components like transformers and cabinet housing. On average, two to three workers carry out each assembly step. We assume that structural metal fabricators and fitters are used as the direct labor for the assembly process; the labor cost assumed for this type of employee by country is included in the appendix. For the modeled results, we assumed that three laborers are required to assemble each drive, and that the drive takes a total of eight weeks to assemble. A production volume of 1,000 VFDs per year was assumed in the cost model. Because this is a manual assembly process that would likely take place in a multi-use facility, there is not a clear definition of capacity utilization. The bill of materials for the VFD includes electrical components, the cooling system, the communications and controls system, and the cabinet. A detailed list of major components is shown in Table 7. Note that some VFDs are hermetically sealed while others are not; however, in this case the cost of hermetically sealing the cabinet was not a significant cost driver.

Table 7. Bill of Materials for the VFD

SiC power modules
Hermetically sealed cabinet
Fan
Liquid-cooled system
Transformers
Capacitors
Motor controller
Gate drivers
Human interface
Programmable logic controller
Wiring harness
DC power supply for gate drivers
Miscellaneous electrical components

The modeled scenario that was computed was based on inputs from current SiC research systems and on current VFD commercial-scale manufacturing. This 1-megawatt drive design consisted of 3 transformers and 45 SiC power modules. The specifications and prices for the transformers were modeled on commercially available three-phase components. The power module price was obtained from the bottom-up method in Section 3.1.3. The material prices for these components were held constant across all countries in the stated scenario. The rationale for these assumptions is that the main companies that are working in the VFD markets are large, multinational manufacturing companies. Much of the manufacturing of these drives is done near their end use application sites due in part customer ability to have better access to support and to reduce the need to go thru intermediaries (NREL primary interview). While there is the opportunity to obtain cheaper components outside of Europe and North America, the customers in the marketplace for VFDs are quite conservative, and therefore high quality and reliability are paramount in this industry. It is for those reasons the modeled scenario costs for materials were held constant across countries.

It is important to note that the SiC VFD was designed for the same switching frequency used in a similar Si-based VFD. The ability of SiC to attain higher switching frequencies could provide an opportunity for further system size reduction and cost savings in certain applications. However, many motors currently used in industrial applications are not able to handle higher switching frequencies, and our industry interviews indicate that, in the near-term, VFD firms are not moving to higher frequency designs.

Table 8 lists the key financial assumptions used for modeling the VFD. These assumptions were used across all counties. This was done primarily because many of the large-scale manufacturers of these drives are large, multinational corporations like GE, Siemens, and Mitsubishi. These companies' cost of debt and equity can be assumed to be the same for each of the counties where manufacturing can be located. Data for these key assumptions were obtained by analyzing the financial statements of these key corporations as well as for other competitors in the drive marketplace.

Table 8. Key Financial Assumptions for VFD DCF Model

Parameter	Value
Cost of debt	3.61%
Cost of equity	7.51%
SG&A costs (% of revenue)	15%
R&D costs (% of revenue)	3.75%
Inflation	2%
Equipment depreciation period	7 years
Building depreciation period	20 years

3.1.5 A Note on Production Volumes

Production volumes used in our models for each component described above are in units of each component per year. The assumption of 5,000 6-inch wafers/year used in our wafer cost model is consistent with module production volumes of approximately 1 million/year used in our power module cost model. These production volumes correspond to a VFD production of approximately 23,000 VFDs/year. If this volume were realized, it would represent a two-fold increase over the 2015 VFD market size; some growth the VFD market might be possible if SiC power electronics are used to improve their cost and performance. Additionally, SiC wafers, chips, and power modules are applicable to many end applications besides medium-voltage VFDS, and thus the production of these upstream components will exceed the demand from VFDs. We modeled the costs associated with a 1,000 VFD/year production, which would represent a fraction of the total market. Because the medium-voltage VFD manufacturing involves largely manual assembly of semi-customized designs, the effect of production volume on cost is expected to be small.

3.2 Regional Cost Model Results

3.2.1 Base Case Results for SiC Ingots, Substrates, and Epi-Wafers

Figure 6 shows the cost modeling results for SiC epi-wafers in the base case by country. For the case of U.S. manufacturing, the manufacturing costs and MSP associated with just the substrate (i.e., not including the epi-layer costs) were $758 per wafer and $1,290 per wafer, respectively. The manufacturing costs associated with epi-layer growth were calculated to be $130.08/wafer for the case of U.S. manufacturing.

Our bottom-up cost analysis showed that low yields (see Table A-1, in the Appendix) particularly in the crystal growth process, contribute significantly to the total manufacturing

cost. Materials constitute the single largest cost category. For the substrate, the primary material costs are the high-purity SiC materials used for crystal growth, as well as the expensive consumables associated with the wafering and polishing process (diamond slurry, diamond wire, polishing pads). For the epitaxial growth, silane is the most expensive material.

Equipment costs are also significant. The equipment costs for the crystal and epitaxial growth processes are high. For the crystal growth, the high cost stems not from the cost of each individual tool, but the fact that a large number of tools are required to meet the throughput requirements due to the low throughput of the growth process using current techniques. Increasing the throughput of the crystal growth process could enable reductions in this cost. For epitaxial growth, each tool is expensive, and the process is also relatively slow, so that multiple stations are required. High-voltage devices that are currently being brought to market—like 3.3-kV devices—require thicker epitaxial layers than are used for the lower-voltage devices typical today (Agarwal et al. 2016). The wafer polishing process may also need to be adapted to achieve low costs and sufficient yields at very high volumes of production.

The SG&A cost (as a percent of revenue) is also currently high. This may be related to the early stage of the industry, where overhead costs tend to be higher; these costs may decrease over time. However, because there are currently only few wafer manufacturers and even fewer that are public, we have only limited data on current overhead costs (see Section 3.1.1). These costs also fluctuate over time.

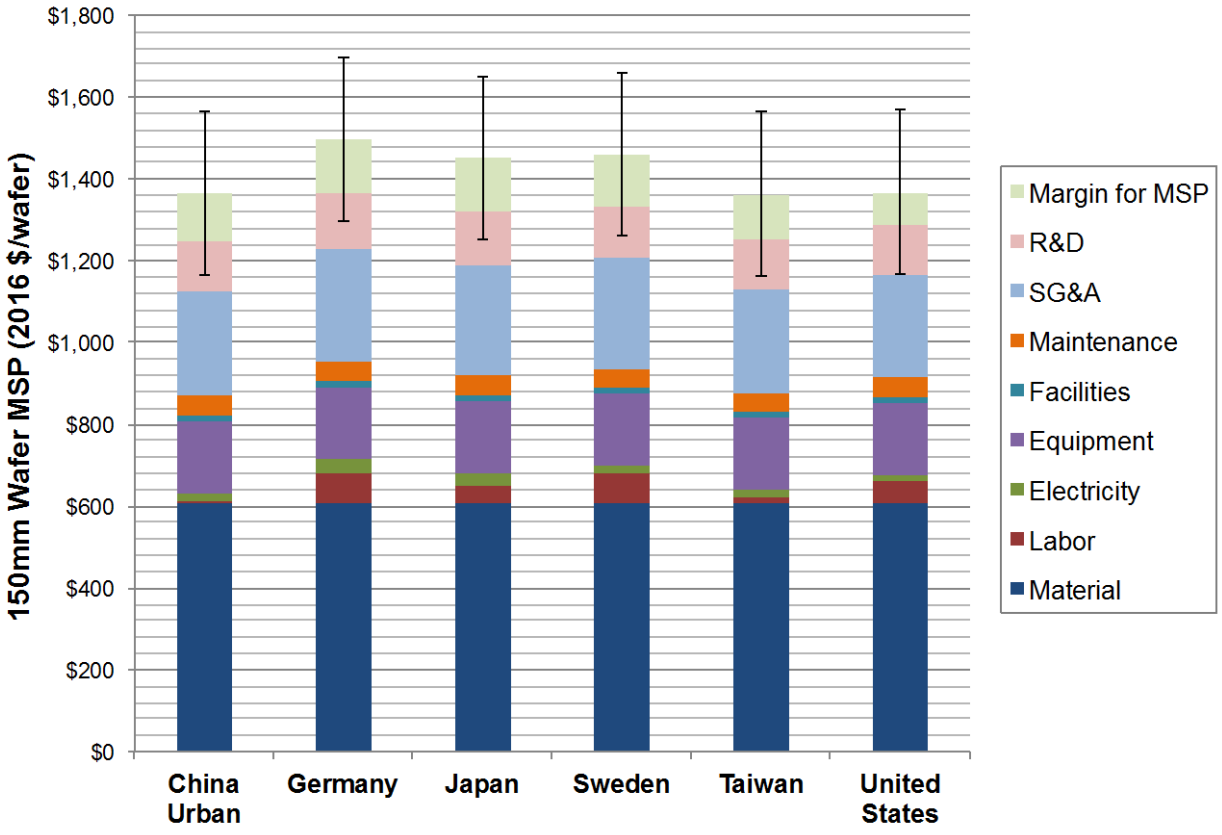

Figure 6. MSP breakdown by country for the SiC epi-wafers in the base case

As can be seen in Figure 6, labor costs are the primary driver of differences in regional manufacturing costs and MSPs for this base case. Smaller differences are attributable to differences in electricity costs, SG&A costs, R&D costs, and the margin for the MSP. In the base case, regional differences in the margin required for the MSP are caused by differences in the effective corporate tax rate by country. Because the SG&A and R&D costs are calculated as a fixed percentage of annual revenue, which is equal to the calculated MSP multiplied by the annual production volume,[5] countries with higher tax rates and high manufacturing costs have higher SG&A and R&D costs. However, in reality, these costs will likely vary by country on a dollar basis and differ by firm. Some firms manufacture in one country, but conduct the majority of their R&D and SG&A operations in other countries; many of the larger, vertically integrated multinational firms have manufacturing, R&D, and SG&A in multiple locations throughout the world with different cost structures. While there are insufficient data at this early stage in the SiC industry to see regional trends in R&D and SG&A spending as a percent of revenue by country, regional trends in R&D investments or the efficiency of overhead spending may develop over time.

3.2.2 Hypothetical, Regional Scenario Analysis on SiC Wafers

In the base case, the difference in MSP between countries as a percentage of total costs is small (Figure 6). As discussed in Section 2.3, we expect that current costs are more heavily influenced by the specific capabilities and strategies of firms who happened to be located in different countries, including the ability of certain firms to obtain higher yields and produce 6-inch wafers in higher volumes. Indeed, the United States, Japan, and Germany, which currently lead SiC wafer production globally, have higher costs in the base case than China or Taiwan.

In order to illustrate how these factors—both firm-specific characteristics and policy-related—could affect regional cost differences realized in practice, we provide analysis of two hypothetical scenarios roughly constructed to reflect scenarios that could be observed for certain in the United States and China in the present and near future (described below). The primary goal of this scenario analysis is to demonstrate to what degree regional costs could be affected by factors besides core country factors. This is important to understand because, as mentioned above, the base case does not fully reflect the factors that can lead to manufacturing cost-competitiveness. These scenarios correspond to just two possible examples of how relative differences in U.S. and Chinese costs could evolve. The relative impact of any of these variables as shown in Figure 7 will depend on the order of operations. It is of note that the particular circumstances—including the status of the industry, government policy, or a particular firm—is, of course, subject to change over time.

The two scenarios we modeled are also described below. Table A-2, in the Appendix includes details of the assumptions for each case. Figure 7 shows the modeled MSPs for these two hypothetical scenarios.

[5] Our financial model assumes that all product produced in a given year is sold to calculate revenues.

- Scenario #1: As discussed in Section 2.4, the U.S. currently produces a greater volume of SiC wafers than China. Because Chinese firms have recently installed more capacity in recent years, but still have only 3 to 4% of the market, we also expect that plant utilizations are currently low, although were not able to obtain numerical data on this. Additionally, because Chinese firms have only recently begun production of SiC wafers, while U.S firms are established in the market, it is possible that some Chinese firms currently have lower yields than U.S. firms. We again have not quantitative data on this relative yield difference; we examine the potential impact of a 30% relative yield difference on cost here as an example of how yield differences could affect cost; any gap in yield between firms in different countries could change over time. Finally, subsides and government support have played a significant role in development of semiconductor industries in China (Ernst 2015; Lu 2015; Yole Développement 2016; NREL primary interviews). There is good data available on the amount of subsidies received by individual SiC firms; in our scenario, we show the sensitivity of the modeled MSP to subsidizing 50% of the equipment.

- Scenario #2: This scenario builds off of Scenario 1 (rather than the base case), and illustrates one possible example of how two countries could take different pathways to obtain similar costs, including making changes in manufacturing process or business processes that result. China and the United States are modeled here, but this could apply to other countries as well. The exact values of the changes are chosen arbitrarily. The key take away from this plot is that regional cost differences result from a confluence of factors, including but in additional to technical differences and differences in core country factors. Variability of course also exists between firms within a country.

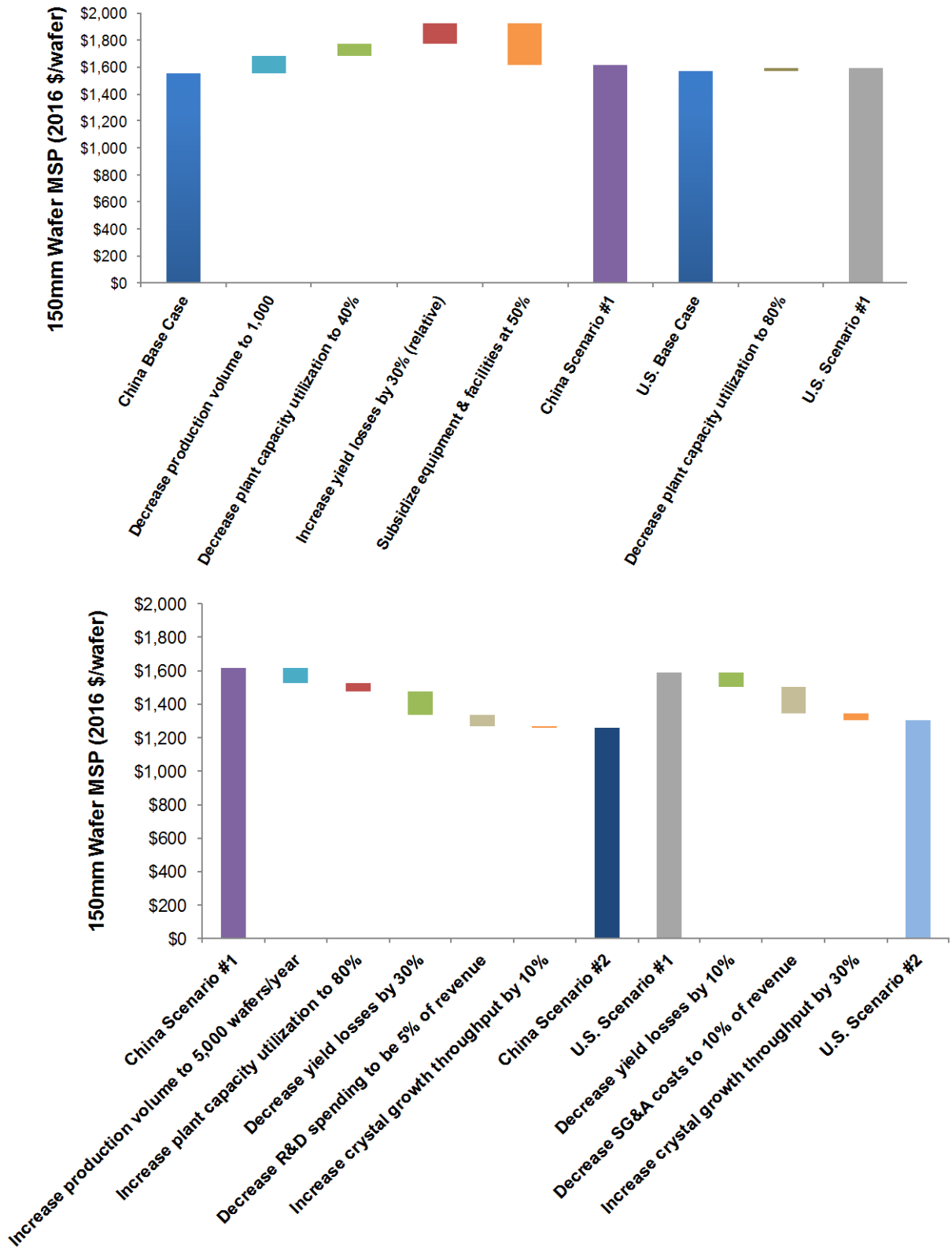

Figure 7. Comparison of China and U.S. modeled MSPs in our two hypothetical scenarios: (top) scenario #1 and (bottom) scenario #2. Details of the assumptions made in each scenario are included above.

3.2.3 Base Case Results for 3.3kV SiC Chips: MOSFETs and SBDs

Figure 8 shows the MSP breakdown for SiC MOSFETs (top) and SBDs (bottom) per 6-inch wafer. As can be seen from the figure, the processing costs per wafer for are substantially higher for the MOSFET than the SBD. This is because of the higher device complexity and larger number of steps involved for the MOSFETs. However, the much smaller MOSFET chip area in this case (see discussion in Section 3.1.2) results in a lower per-chip cost and MSP ($1.16/chip and $1.92/chip, respectively, for the case of U.S. manufacturing) compared to the SBD ($3.39/chip and $5.61/chip for U.S. manufacturing, respectively); per-chip costs for the MOSFET could be higher if there was a higher on-resistance (the resistance between terminals while in the on-state), which would translate to the need for larger chip areas. Chip area and thus per-chip costs depend on the current ratings and resistance of the devices, as well as the specific device designs selected (e.g., planar versus trench MOSFETs).

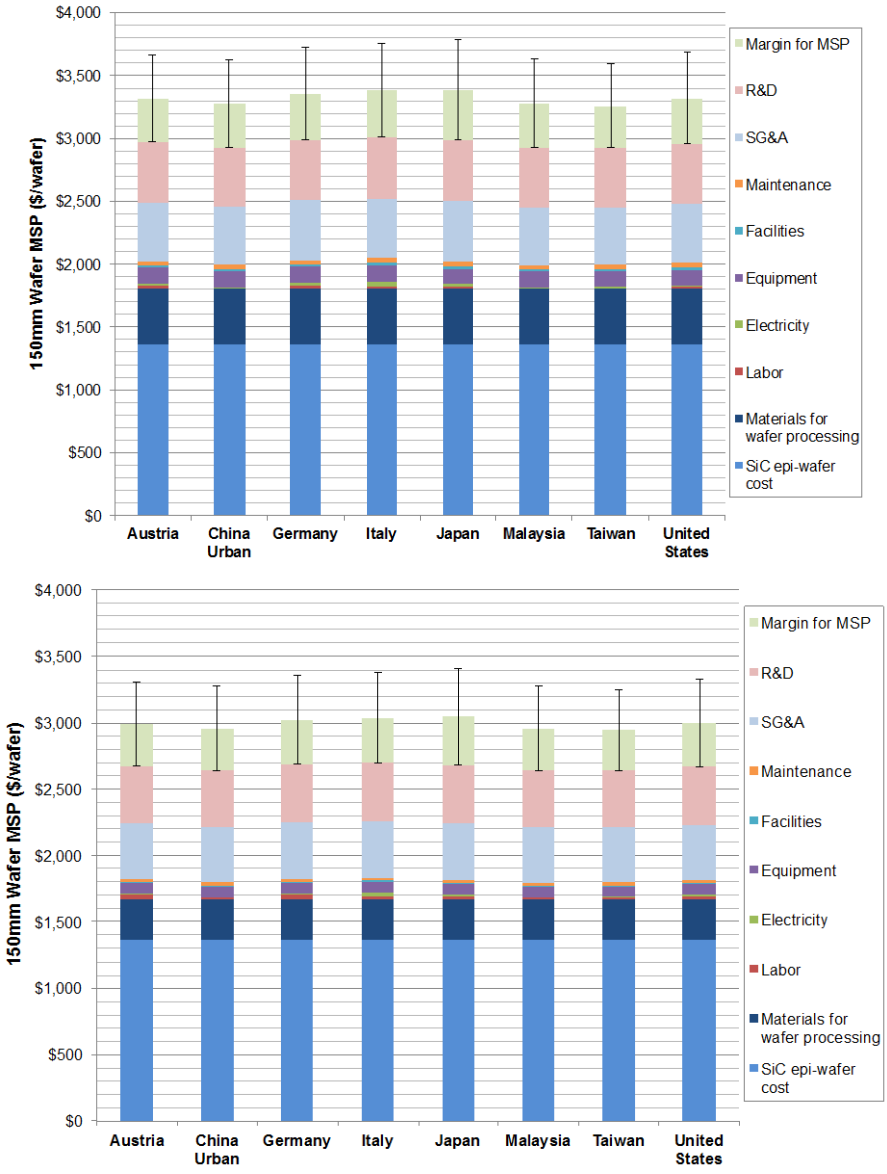

Figure 8. MSP breakdown by country for a 3.3-kV SiC MOSFET (top) and SBD (bottom) in the base case

The SiC epi-wafer is by far the larger contributor to cost for both types of devices. Decreasing the cost and/or price of the epi-wafers will enable significant reductions in the chip cost. Very large chip manufacturers may be able to pressure wafer suppliers to provide lower prices. The cost of other materials used in creating the chips is also a significant contributor to cost. This includes the cost of materials for the different device layers, the metallization, and materials used for processing (e.g., resists and developers used in lithography, wet chemicals for cleaning).

The equipment and facilities costs are also significant contributors to the manufacturing cost for the wafer processing. These costs are even higher per unit at lower production volumes. Subsidizing the equipment and facilities or leveraging existing Si facilities to take advantage of economies-of-scale for SiC devices (often referred to as the "foundry model") can significantly reduce these costs. The potential for different countries to successfully implement a high-volume foundry model is discussed in Section 4.

The SG&A and R&D costs are also high; the discussion of SG&A and R&D costs for wafers from Section 3.2.1 is relevant to chips as well. Labor, electricity, and tax costs contribute to the regional differences in MSP, but the effect is very small compared to the total MSP.

The yields associated with chip manufacturing are much higher than those for wafer manufacturing, and thus yield does not play as critical of a role in cost.

3.2.4 Base Case Results for 3.3-kV SiC Power Modules

Figure 9 shows the MSP breakdown by country for the SiC power module. The SiC chips (MOSFETs and SBDs) are the largest contributors to overall cost, making up 65%–75% of all materials costs. As discussed in Section 3.1.3, we assume that chips used in the power modules are sourced locally and assume the chip costs for each region are equal to our modeled MSPs for those countries. The difference in regional MSP for the power modules is primarily due to these differences in chip costs. However, in reality, chips can be sourced from other locations as well, and eventually, as the industry scales, a global chip price could emerge. Many companies use contract manufacturing for SiC module production; equipment and facilities that already exist for manufacturing Si power modules can be used for SiC production. This means that SiC module manufacturing firms can take advantage of the economies of scale enjoyed by Si module manufacturing firms, reducing overall equipment, facilities, and non-chip material costs.

Differences in effective corporate tax rates, labor costs, and electricity costs play a minor role in the regional cost differences as shown in Figure 9.

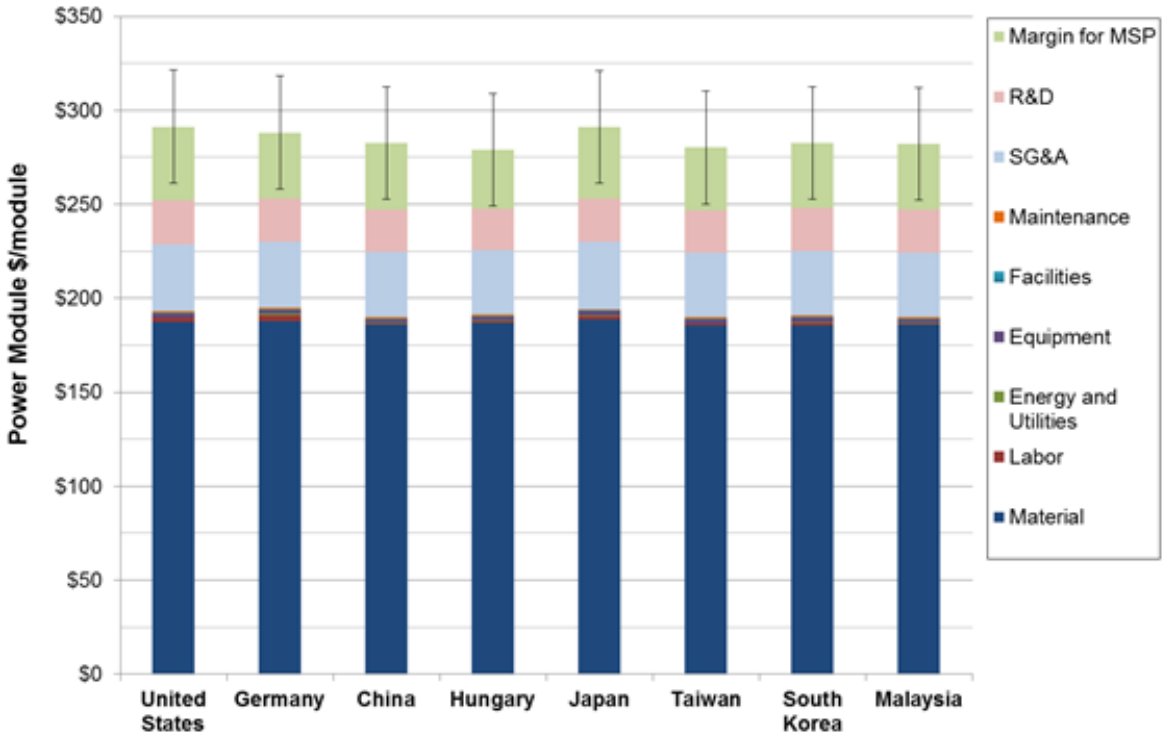

Figure 9. MSP breakdown by country for the SiC power module

3.2.5 Base Case Results for a 1-Megawatt SiC-based Medium-Voltage VFD

Figure 10 shows the MSP breakdown by country for the VFD. Material costs are the largest single cost category. Over half of the material costs are for the transformers; the SiC power modules also contribute significantly to total material costs. A breakdown of material costs by component is given in Figure 11. Transformer costs vary by design and depend on the voltage of the wall power. Transformers may be configured as multiple single-phase transformers or a single three-phase transformer. Each configuration has advantages and disadvantages based on size, material use, and final cost. We selected the configuration used here to be cost effective for the VFD modeled in this analysis. As discussed in Section 3.1.4, we do not assume a higher switching frequency than is typical for Si designs. While SiC can enable higher switching frequencies, this is not appropriate for all applications. If a higher frequency VFD is employed, this could reduce some of the materials costs, including those associated with the transformer.

Labor costs play a much larger role in regional cost differences for the VFD than the other components analyzed in this analysis. This is because the VFD manufacturing is largely a manual assembly process.

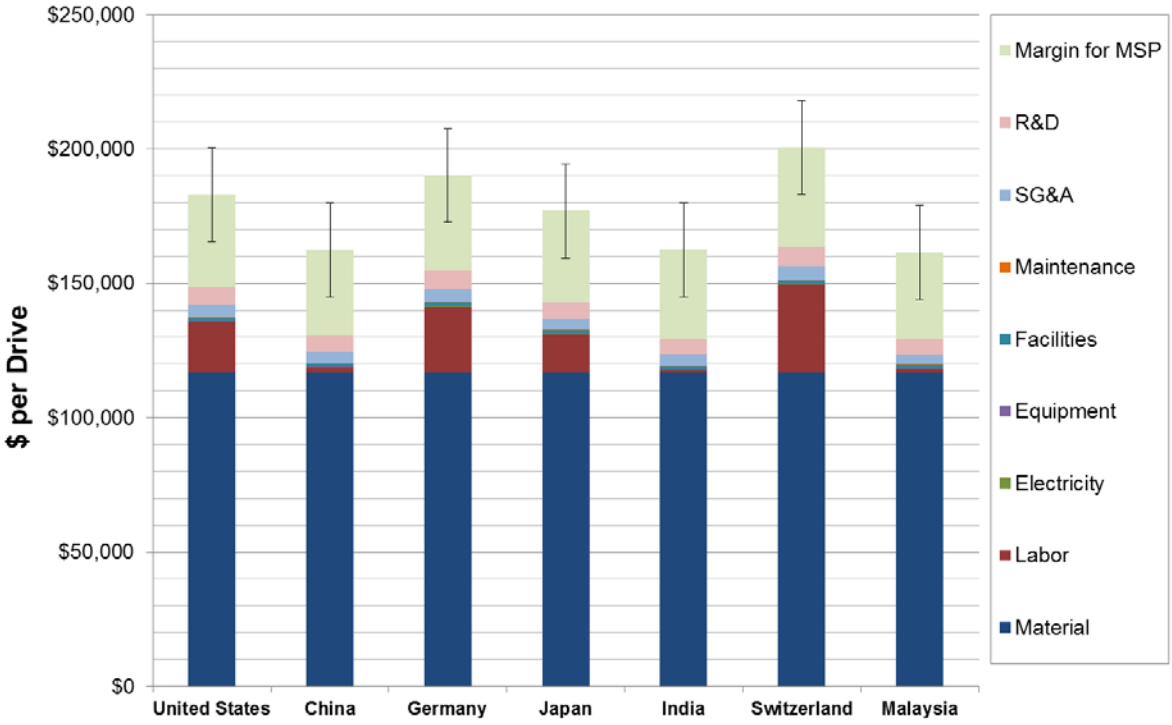

Figure 10. MSP breakdown by country for the SiC-based VFD

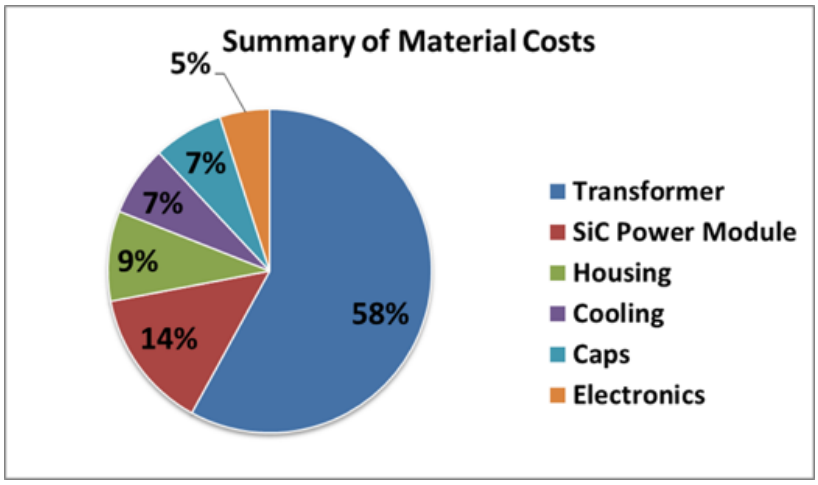

Figure 11. Breakdown of the material costs for the SiC-based VFD by category

4 Summary

Figure 12 shows the MSP of each component per VFD. In this case, we are using MSP as a proxy for the value of each component. The *value added* at each step is equal to the value at the step minus the costs for *all purchased input materials*, not just those included in this simplified value chain. As can be seen from this figure, the final assembly of the drive adds significant value. Some of this value will be captured by companies that assemble and sell the VFD, while some is captured by the manufacturers of other materials purchased for VFD assembly, including the transformer, housing, and other electronic components.

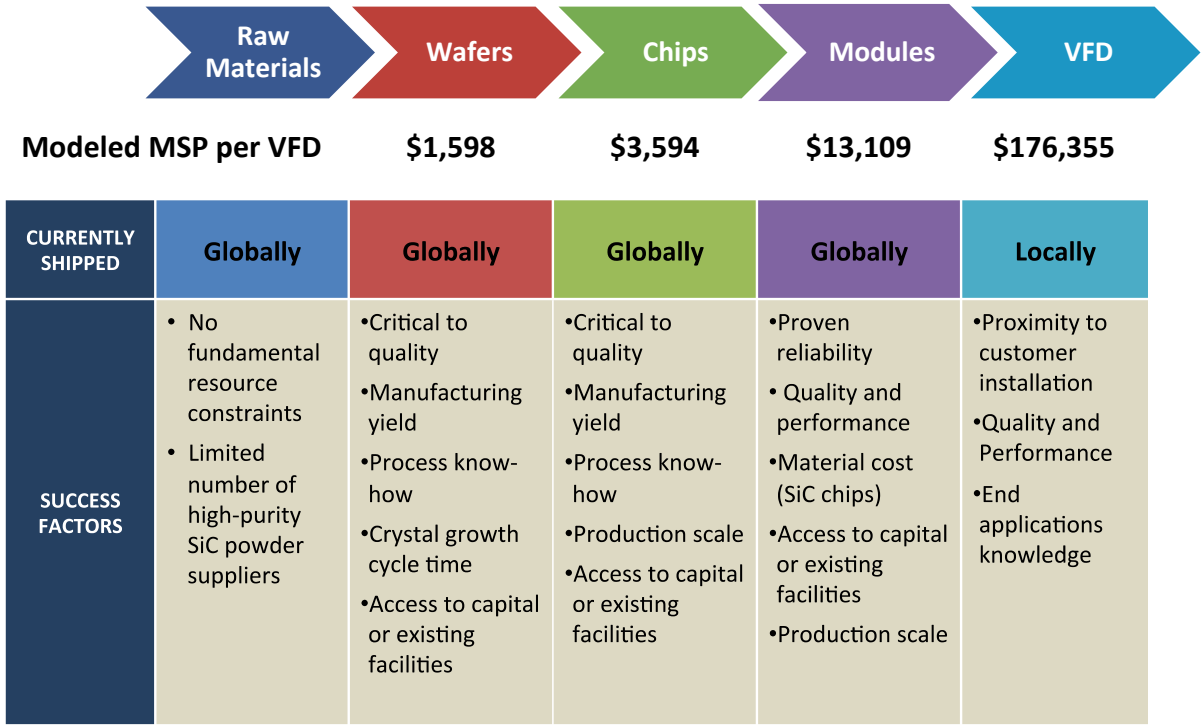

Figure 12. Summary of modeled MSP results and key factors across the value chain. The value and share for each element are shown for the case of U.S. manufacturing

Key factors that currently contributing to manufacturing location decisions along the value chain are also summarized in Figure 12. For VFDs, these factors relate to Si-based VFDs, not SiC-based VFDs, since these are not commercially available today. While cost is important (the cost of SiC devices and modules compared to Si still presents a barrier to adoption), quality and access to facilities and expertise are most critical for competing in the current environment and often drive the total cost. Manufacturers that are able to achieve high quality and leverage existing facilities and expertise— regardless of the location of their manufacturing—have been the most successful to-date. This is because downstream performance is critical to adoption of this technology. For example, yields during epitaxial growth can be low if substrate quality is poor, leading to high costs for epitaxial growth companies. Reliability and knowledge of the end application are particularly important for the manufacture of VFDs, which are often tailored to specific applications in industries where unreliable parts and associated downtime can mean millions of dollars of lost revenue. For these reasons, it is likely that quality will continue to play

a role in achieving low costs as well as market share for manufacturers along the value chain. This means that new entrants will need to achieve quality and reliability of their products even if they have cost advantages due to scale or inherent country factors to be competitive. Production volumes may play a larger role in regional manufacturing cost structures in the future as the industry scales up, depending on how global production patterns develop.

Differences in labor costs have not been primary drivers of the current distribution of manufacturing capacity for any components along the value chain to-date. Shipping time and costs issues play a role in where VFD assembly is sited, but have not influenced the location of manufacturing for the other components we explored.

References

Agarwal, A., Marlino, L., and Johnson, M. (2016). Wide BandGap Power Devices and Applications; the U.S. Initiative. In *46th European Solid-State Device Research Conference*. https://doi.org/10.1109/ESSDERC.2016.7599622

Cole, Z., B. McGee, J. Stabach, S. Storkov, B. Whitaker, D. Martin, G. Falling, R. Shaw, and B. Passmore. (2015).“High Temperature, Wide Bandgap Full-Bridge Power Modules for High Frequency Applications.” In *2015 IEEE International Workshop on Integrated Power Packaging (IWIPP)*, 119–22, 2015. doi:10.1109/IWIPP.2015.7295993.

CEMAC. (2017). Benchmarks of Global Clean Energy Manufacturing. NREL/ NREL/TP-6A50-65619. Retrieved from http://www.nrel.gov/docs/fy17osti/65619.pdf.

Chung, D., and Elgqvist, E. (2016, April). Automotive Lithium-ion Cell Manufacturing: Regional Cost Structures and Supply Chain Considerations. NREL/TP-6A20-66086. Retrieved from http://www.nrel.gov/docs/fy16osti/66086.pdf

Fu, R., James, T. L., and Woodhouse, M. (2015). Economic Measurements of Polysilicon for the Photovoltaic Industry: Market Competition and Manufacturing Competitiveness. *IEEE Journal of Photovoltaics*, *5*(2).

Hamada, K., Hino, S., and Kitani, T. (2015). Low On-Resistance SiC-MOSFET with a 3.3-kV Blocking Voltage. *Mitsubishi Electric ADVANCE*, *149*, 14–17.

IHS. (2016). *SiC & GaN Power Semiconductors Report - 2016*. https://technology.ihs.com/521146/sic-gan-power-semiconductors-2016

Infineon. (2016, July 14). Investor Presentation: Infineon to Acquire Wolfspeed. Retrieved from http://www.infineon.com/dgdl/2016-07-14_Infineon+to+acquire+Wolfspeed_Investor+Presentation.pdf?fileId=5546d46155dd90e10155e8859aae01d5

Khaja, A. Syed, C. Kaestle, and J. Franke. “Reliable Packaging Technologies for Power Electronics: Diffusion Soldering and Heavy Copper Wire Bonding.” In *Electric Drives Production Conference (EDPC), 2013 3rd International*, 1–6, 2013. doi:10.1109/EDPC.2013.6689763

Lee, K., Jeon, O., Lim, S., Park, S., Lee, B., and Lee, T. (2008). DBC Substrate Based EMC Transfer Molded Power Module. In *5th International Conference on Integrated Power Systems* (pp. 1–7).

Müller, St.G., Glass, R.C., Hobgood, H.M., Tsvetkov, V.F., Brady, M., Henshall, D., Jenny, J.R., Malta, D., and Carter Jr., C.H. (2000). The status of SiC bulk growth from an industrial point of view. *Journal of Crystal Growth*, 211, 325-332.

pwc. (2011, April). Global Effective Tax Rates. Retrieved from http://businessroundtable.org/sites/default/files/Effective_Tax_Rate_Study.pdf

Richmond, Jim, Scott Leslie, Brett Hull, Mrinal Das, Anant Agarwal, and John Palmour. "Roadmap for Megawatt Class Power Switch Modules Utilizing Large Area Silicon Carbide MOSFETs and JBS Diodes." In *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 106–11. IEEE, 2009. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5316038.

Runhua, H., Yonghong, T., Song, B., Gang, C., Ling, W., Ao, L., Zhifei, Z, et al. (2015). Design and fabrication of a 3.3 kV 4H-SiC MOSFET. *Journal of Semiconductors*, *36*(9). https://doi.org/10.1088/1674-4926/36/9/094002

Sakai, M., Toyoshima, S., Wada, K., Furumai, M., Tsuno, T., and Mikamura, Y. (2015). 3.3 KV SiC Power Module with Low Switching Loss. *Electronics, SEI Technical Review*, (81), 51–55.

Sheng, W. W., and Colino, R. P. (2004). *Power Electronic Modules: Design and Manufacture*. CRC Press.

Stevanovic, L. (2012). Packaging Challenges and Solutions for Silicon Carbide Power Electronics. In *Electronic Components and Technology Conference*. Retrieved from http://www.ectc.net/files/62/2_Stevanovic_GE.pdf

System Plus Consulting. (2015, July 7). POWER COSIM+: Semiconductor Manufacturing and Cost Simulation Tool. Retrieved from http://www.systemplus.fr/costing-tools/power-cosim/

U.S. Department of Energy. (2015). Wide Bandgap Semiconductors for Power Electronics. In *Quandrennial Technology Review 2016*. Retrieved from http://energy.gov/sites/prod/files/2015/09/f26/QTR2015-06-Manufacturing.pdf

U.S. Geological Survey. (2016, January). Report on Diamond (Industrial). Retrieved from http://minerals.usgs.gov/minerals/pubs/commodity/diamond/mcs-2016-diamo.pdf

Unruh, B. (2003). Machine Drive Electricity Use in the Industrial Sector. In *ACEEE Summer Study on Energy Efficiency in Industry* (pp. 241–252). Rye Brook, NY. Retrieved from http://www.eceee.org/library/conference_proceedings/ACEEE_industry/2003/Panel_6/p6_21/paper

Wijesundara, M.B.J. and R. Azevedo, *Silicon Carbide Microsystems for Harsh Environments. Chapter 2: SiC Materials and Processing Technology*, MEMS Reference Shelf 22, New York: Springer, 2011. DOI10.1007/978-1-4419-7121-0 2

Wolk, R. H. (2014). Proceedings of the NIST/DOE Workshop on High-Megawatt Direct-Drive Motors and Front-End Power Electronics.

Woodhouse, M., Feldman, D., Fu, R., Horowitz, K., Chung, D., Jordan, D., and Kurtz, S. (2016, May). On the Path to Sunshot: The Role of Advancements in Solar Photovoltaic Efficiency, Reliability, and Costs. NREL/TP-6A20-65872. Retrieved from http://www.nrel.gov/docs/fy16osti/65872.pdf

X-FAB. (n.d.). SiC Foundry at the Scale of Silicon: First 6-inch SiC Foundry Offering. Retrieved November 23, 2016, from http://www.xfab.com/fileadmin/X-FAB/Download_Center/Technology/SiC/Silicon_Carbide_Datasheet.pdf

X-FAB Offers High-Volume 6-Inch SiC Foundry Production. (2016, March 10). Retrieved from http://www.semiconductor-today.com/news_items/2016/mar/x-fab_100316.shtml

Yole Développement. (2016). *Power SiC 2016: Materials, Devices, and Applications*. http://www.i-micronews.com/category-listing/product/power-sic-2016-materials-devices-modules-and-applications.html

Zhou, W. (2016). Current and Future World Markets for Motors and Motor Controls. In *Motor & Drive Systems*. Jacksonville. Retrieved from http://www.e-driveonline.com/conferences/wp-content/uploads/2016/01/IHS.pdf

Appendix A. Detailed Input Assumptions

In this appendix, we provide further detail on input assumptions used in our models of wafers, chips, and VFDs. These include assumptions for both the manufacturing process parameters and pricing for key materials that may be of interest to the reader. Additionally, we provide information on the underlying assumptions the scenarios shown in Figure 8.

Table A-1. Key Input Assumptions used in the SiC Wafer Manufacturing Cost Model

Input Parameter	Value	Units
6N SiC powder price	$500	USD/kg
6N silane price	$184	USD/kg
High purity propane gas price	$0.31	USD/L
Raw boule height	35	mm
Wafers per ingot	44	
SiC crystal growth rate	0.22	mm/hr
SiC epitaxial growth rate	2.5	μm/hr
Silane flux (epitaxial growth)	0.45	L/min
Propane flux (epitaxial growth)	0.45	L/min
Cumulative yield loss (substrate manufacturing plus epitaxial growth)	40.41%	
Total direct labor count at 1,000 wafers/month	20	workers

Table A-2. Assumptions for the Hypothetical, Example Regional Cost Scenarios for SiC Wafers

	Scenario #1		Scenario #2	
Parameter	**United States**	**China**	**United States**	**China**
Production volume (6-inch wafers/year)	5,000	1,000	5,000	5,000
Plant capacity utilization (%)	80%	40%	80%	80%
Subsidy for equipment & facilities (% of costs subsidized)	0%	50%	0%	50%
Yield loss multiplier	1	1.3	0.8	1
SG&A costs (% of revenue)	18.5%	18.5%	10%	18.5%
R&D costs (% of revenue)	8.9%	8.9%	8.9%	5%
Crystal growth throughput multiplier	1	1	1.3	1.1

Table A-3. Key Input Assumptions Used in the SiC MOSFET Manufacturing Cost Model

Input Parameter	Value	Units
6N SiC powder price	$500	USD/kg
6N silane price	$184	USD/kg
High purity propane gas price	$0.31	USD/liter
Raw boule height	35	mm
Wafers per ingot	44	
SiC crystal growth rate	0.22	mm/hr
SiC epitaxial growth rate	2.5	μm/hr
Silane flux (epitaxial growth)	0.45	L/min
Propane flux (epitaxial growth)	0.45	L/min
Cumulative yield loss (substrate manufacturing plus epitaxial growth)	40.41%	
Total direct labor count at 1,000 wafers/month	20	workers

Table A-4. Key Input Assumptions for the VFD Cost Model

Input Parameter	Count	Units
SiC power modules	45	Units
Hermetically sealed cabinet	22	Surface area in sq. meter
Fan	6.5	Tonne
Liquid cooled system	70,000	Btu
Transformers	3	Units
Capacitors	108	Units
Motor controller	1	Units
Gate drivers	45	Units
Human interface	1	Units
Programmable logic controller	1	Units
Wiring harness	1	Units
DC power supply for gate drivers	1	Units
Miscellaneous electrical components		

Appendix B. Breakdown of Module Material Costs

Material costs dominated the cost of the SiC-based power modules. In this appendix, we provide a detailed breakdown of these materials costs by component for the interested reader.

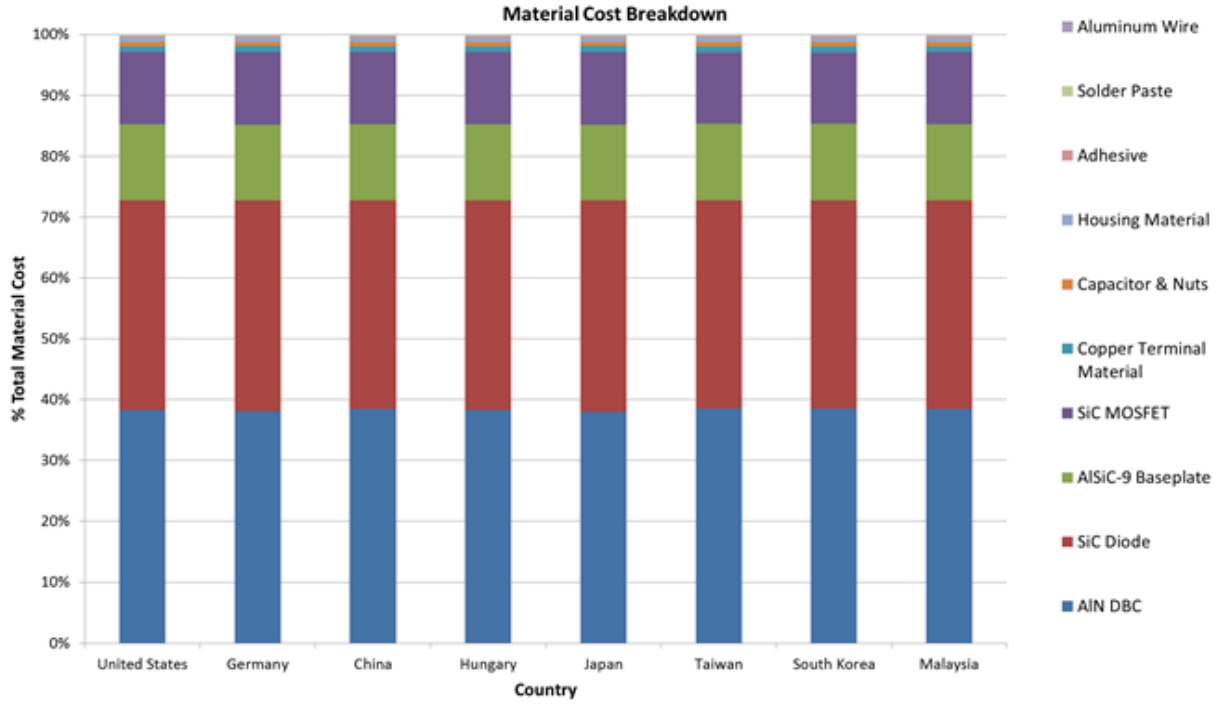

Figure B-1. Material cost breakdown for the SiC power modules