Fault Response of Distributed Energy Resources Considering the Requirements of IEEE 1547-2018

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Fault Response of Distributed Energy Resources Considering the Requirements of IEEE 1547-2018

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***Abstract*—Inverter-based DER responses to faults on the electric power system are different than those of conventional generators and are often poorly understood. Inverter fault responses are largely software-defined, within physics-based constraints. DERs are regulated by standards and grid codes that also constrain their responses. Though fault response of DERs will vary widely, for any DER following any particular standard, a pattern of fault response can be synthesized by observing that particular standard. In this paper, the recently published IEEE 1547-2018 is examined to explore the general fault response of any DER that follows IEEE 1547-2018. Additionally, an IEEE 1547-2018 compliant inverter model is developed and tested in simulation to find the fault response, and that response is compared with the fault response of a commercial off-the-shelf inverter.**

Keywords—IEEE 1547-2018, DER, fault current, inverter, inverter-interfaced distributed generation

I. Introduction

Traditional utility protection schemes are designed for networks with conventional synchronous generators as the main fault feeding sources. However, large scale integration of distributed energy resources (DERs) is likely to change the fault levels and characteristics. This is because DERs are expected to withstand and ride through faults to maintain stability of the network and to prevent further deterioration of the already faulted system [1]. For higher penetrations of DERs, modifications or additional protection schemes may be needed for reliable control and operation of power systems [2]. Updating the protection schemes to accommodate more DERs into the grid requires a better understanding of the DER fault responses. Though fault responses of induction and synchronous generators are well understood and documented, the same cannot be said for inverter interfaced distributed generators (IIDG) [3]. DERs based on synchronous or other types of rotary machines normally exhibit uncontrolled fault current, whereas IIDGs, independent of the energy sources, respond to fault according to the control method applied to the inverter [4]. Extensive electromagnetic time domain models [5] as well as simplified models [6] of IIDG have been proposed to investigate the IIDG fault response. The accuracy of these models will largely depend on the successful adoption of the control algorithms deployed by the IIDGs. Modeling the control algorithms of all the IIDGs available in the market will be unrealistic. An easier option would be to analyze the grid code or standards that the IIDGs conform to, while also considering inverter physical limits. For example, IEEE 1547-2018 [7] requires certain responses from DERs to different abnormal grid conditions. Analyzing these requirements, an expected range of fault response can be obtained for IEEE 1547-2018 compliant DERs. Nonetheless, the exact response of DERs will vary within that range, and experimental studies, such as shown in [8], are required to capture the exact response.

In this paper, an analysis of IEEE 1547-2018 is presented in regard to DER responses for abnormal voltage conditions. It was found that any DER compliant to IEEE 1547-2018 is expected to exhibit a fault response in a certain range, specifically the steady-state fault response. The fault current of IEEE 1547-2018 compliant DERs can be expected to be within specific ranges for different fault voltages.

II. IEEE 1547-2018 Requirements

IEEE 1547-2018 provides a detailed explanation on the procedure to find the reference point of applicability (RPA) where all the performance requirements have to be met by the DER. Depending on the voltage level (medium/low) and the connection configuration, the applicable voltage can be line-to-neutral and/or phase-to-phase and/or phase-to-ground. Also, the applicable voltage is recommended to be computed as the RMS value over the fundamental frequency if not otherwise reported. For multi-phase systems, advanced grid functions and ride-through requirements have different rules to calculate the applicable voltage. For voltage *trip* and ride-through requirements, relevant voltages can be calculated as (1) and (2) according to IEEE 1547-2018.

$$V_{lv}^{rv} = \min(V_i^{av}) \tag{1}$$

$$V_{hv}^{rv} = \max(V_i^{av}) \tag{2}$$

where V_{lv}^{rv} and V_{hv}^{rv} are the relevant voltages for low-voltage and high-voltage *trip* and ride through requirements respectively and V_i^{av} are the applicable voltages. V_i^{av} is the applicable voltage, where $i \in \{1, 2, 3\}$ for three-phase systems. DER *trip* time due to voltage disturbance and ride-through characteristics will be determined based on the relevant voltage calculated in (1) and (2). DERs are expected to have two types of responses with respect to any voltage disturbance *1)* mandatory voltage tripping and *2)* voltage ride through. Ride through defines a fundamental (non-adjustable) capability, whereas trip settings are adjustable. For mandatory voltage tripping requirements, two upper bound thresholds and lower bound thresholds of voltages are specified for three categories of DERs, i.e. Category I, II and III (as defined in IEEE 1547-2018). For each of the thresholds, a clearing time is also indicated. If the applicable voltage goes beyond the threshold, the DER has to first *cease to energize* and wait for the clearing time to *trip*.The voltage disturbance ride through requirement recognizes six modes of operations during voltage disturbances. The six modes are not all mutually exclusive,

as described below. A brief description of the modes of operation along with ranges of acceptable current magnitudes are discussed in the following section.

A. Continuous Operation (CO)

The CO mode of operation for DER is defined when the voltage is between 0.88 and 1.1 times the nominal voltage, V_N. Assuming DER output power remains constant, the range of current magnitude of the DER for continuous power delivery in CO will be in the range $[0.9091I_{pre}, 1.1364I_{pre}]$, where I_{pre} is the pre−disturbance current. In the condition where $I_{pre} = I_N$, I_N being the nominal current of the DER, the DER is permitted to prorate the active power for voltage fluctuations in the region below 1 p.u. This implies that the DER can operate as constant power source if the voltage at the RPA, V_{RPA}, is within 1.0 p.u. to 1.1 p.u. and within the voltage range of 0.88 p.u. to 1.0 p.u., the DER can operate either as constant power source or constant current source. In the case of constant current source mode of operation, the inverter output current is limited by I_{max}, where I_{max} is the maximum allowed current threshold of the DER.

B. Mandatory Operation (MO)

In MO mode of operation, Category II and Category III DERs (i.e. nearly all IIDGs) are not permitted to lower their apparent current below 80% of I_{pre}, unless input power is limited by the primary source. So the range of allowed current magnitude of the DER in MO will be $[0.8I_{pre}, I_{max}]$.

C. Permissive Operation (PO)

In PO mode of operation, the DER is permitted to either cease to energize (but not *trip*) or continue to exchange current with the grid. Thus, the DER is permitted to have any current in the range $[0, I_{max}]$ as IEEE 1547 does not specify any current range in PO.

D. Momentary Cessation (MC)

The allowed DER output current range in MC is $[0, I_{max}]$, for the first 83 ms (5 line cycles) and active current is required to be zero thereafter. When the voltage is in the MC region, the DER shall enter MC mode with no intentional delay. DERs are required to return to service from MC immediately after voltage returns to normal.

E. Cease to Energize (CE)

During CE mode of operation, DERs are permitted to generate only partial reactive power exclusively resulting from passive devices. DER output power is restricted in this region as defined by (3) and (4)

$$P = 0 \tag{3}$$

$$Q = \begin{cases} \leq 0.1 \times S_{rating} & S_{rating} \leq 500KVA \quad (4a) \\ \leq 0.03 \times S_{rating} & S_{rating} \geq 500KVA \quad (4b) \end{cases}$$

where P and Q are DER active and reactive power outputs, respectively, and S_{rating} is the apparent power rating of the DER. CE can mean either MC or *trip* as graphically shown Fig. 1(a). While in CE, whether the DER is in MC or *trip* mode depends on the fault voltage and duration of the fault. As

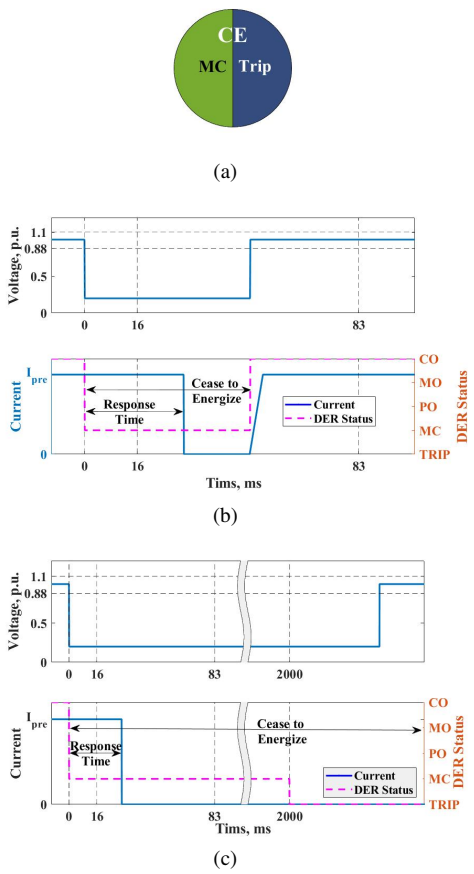

Fig. 1. Relationship of CE, MC and *trip*. This illustration was designed for for Category III DERs with default settings, but the general idea applies to other Categories and settings. a) CE can mean either MC or *trip* b) MC permits immediate return to service c) *Trip* inhibits immediate return to service.

shown in Fig. 1(b), if the voltage recovers before the clearing time setting, the DER can return to service once the fault is cleared. But, if the fault is not cleared within the clearing time setting, the DER will trip and will have to wait a certain time before entering service after the grid condition returns to normal. The relationship of CO, CE, MC and *trip* is illustrated in Fig. 1(b) and Fig. 1(c) for a Category-III DER with default settings.

F. Trip

Trip inhibits immediate return to service and might involve disconnection. *Trip* might follow subsequent to *cessation of energization* if the under- or over-voltage that triggered *cease to energize* lasts for more than the clearing time.

III. Other Considerations

A. Inverter physical limits

The output current of IIDG during grid faults is controlled to remain within a certain limit to avoid damaging the semi-conductor switches of the inverters [9]. Based on extensive testing and knowledge of power electronics design [8], [10], I_{max} of IIDG is typically limited to 1.0-1.2 pu.

B. Measurement accuracy

IEEE 1547-2018 sets minimum measurement and calculation accuracy criteria for DERs during both steady-state and transient events. Voltage has a minimum accuracy requirement of $\pm 1\% V_N$ in the range of 0.5 p.u. to 1.2 p.u. in steady-state and $\pm 2\% V_N$ in the range of 0.5 p.u. to 1.2 p.u. during transient conditions. For active and reactive power, the minimum accuracy applies only for steady-state in the range of 0.2 p.u. to 1.0 p.u.

C. Measuring disturbance duration time

The minimum disturbance ride-through time is cumulative across consecutive events and should be counted separately for under-voltage and over-voltage events. For consecutive voltage disturbances, minimum times for successive disturbance sets and minimum numbers of ride-through disturbance sets are provided for all three categories of DERs in IEEE 1547-2018.

D. Type of fault current supplied

Unlike some other standards, e.g. the German medium voltage network grid code [11], IEEE 1547-2018 does not mandate the DER to inject negative sequence current or provide *dynamic voltage support* for fault ride-through. The phase angle and sequential components of the current supplied during a fault are not specified in 1547-2018.

IV. Steady State Fault Current

For modes of operations other than CO, in addition to the actual fault response of the DER, it is important to consider the duration of the fault current for voltage disturbances. In this analysis, we have accounted for fault responses expected to last more than the RMS voltage detection time (e.g. one to two cycles) and those expected to last more than five cycles (83 ms). The minimum ride-through times in PO and MO for all three categories and voltage regions are at least 160 ms, long enough that the DER current should be considered in utility fault analysis. CE mode is an interesting case that requires the DER to cease energizing the grid. For all the categories of DERs, CE has a response time of 160 ms – long enough that DER current could still be considered in fault analysis. However, it is worth noting that no intentional delay is permitted in CE, so the fault current is expected to be near zero after a short detection time (e.g one to two cycles). But if the grid voltage exceeds $1.3V_N$, IEEE 1547-2018 requires the DER to CE within 16 ms (one cycle) to avoid contributing to transient over-voltage. So, above $1.3V_N$, it can be assumed for the purpose of fault analysis that the DER will contribute zero fault current. On the other hand, if voltage drops below 0.5 p.u. or rises above 1.1 p.u. due to abnormal grid conditions, Category III DERs will be in MC. In that case, the DER output current will reduce to zero before five line cycles for all values of I_{pre} if the fault is not cleared. However, there will be some uncertainties in actual DER response due to DER voltage measurement accuracy ($\pm 1\% V_{nom}$ as per IEEE 1547-2018). Fig. 2 graphically shows the allowable expected ranges of post-fault current shaded in green and yellow for different post-fault voltages if the pre-fault current is 1 p.u., assuming IEEE 1547-2018 default *trip* settings. The figure also assumes the maximum fault current the IIDG can produce is 1.2 p.u., which is on the high end of typical values seen in laboratory tests [8], [10]. In that figure, the green shaded areas show the allowable current range after five line cycles. Category III DERs might continue partial operation from one cycle to five cycles post fault in the voltage disturbance ranges of 0 p.u. to 0.5 p.u. and 1.1 p.u. to 1.3 p.u. This region is shaded in yellow in Fig. 2. Because the DER is required to cease to energize the grid with no intentional delay, the expected current for the purposes of protection is zero in this region.

The output current for all three categories of DERs in response to voltage disturbances can be summarized in two ways: *i)* constant power source, and *ii)* constant current source. The constant power source mode of operation can be defined as (5).

$$i^* = I_{PQ}\angle\theta = \frac{P^{ref} + jQ^{ref}}{V_{RPA}\angle\theta_{vRPA}} \tag{5}$$

where P^{ref} and Q^{ref} are reference active and reactive powers, respectively, i is DER output current, $*$ denotes complex conjugate, θ_{vRPA} is phase angle of the voltage at RPA, θ is the phase angle of DER output current, and I_{PQ} is current magnitude while the DER is in constant power source mode. For a three-phase system, V_{RPA} can be assumed as the positive sequence voltage magnitude. On the other hand, the current magnitude in constant current source mode of operation, I_{CC}, is restricted by the current ranges as discussed in section II. It should be noted here that there IEEE 1547-2018 places no requirements on θ, so Q_{ref} could have any value.

V. Experimental and Simulation Results

In order to evaluate DER responses to abnormal grid conditions with respect the requirements of IEEE 1547-2018, experimental and simulation studies were performed. Fig. 3 shows the experimental setup to test the response of an off-the-shelf (hardware) inverter when subjected to different faults. The grid simulator output voltage was varied to emulate the different fault levels at the terminals of the inverter. In these experiments, the equipment under test (EUT) was a 20 kW three-phase inverter. This inverter was manufactured before the publication of IEEE 1547-2018, hence is not expected to conform to the standard. To complement the experimental results, a simulation model similar to the test set-up shown in Fig. 3 was developed in Matlab/Simulink for time-domain simulation. The simulated inverter was designed to conform the IEEE 1547-2018 requirements. Because there are an infinite number of ways to implement the requirements of IEEE 1547-2018, the authors took liberty to set the restrictions as shown in (6).

$$I = \begin{cases} I_{PQ} & 1.0 \le V_{RPA} \le 1.1 & \text{(6a)} \\ I_{PQ} & I_{PQ} < I_{max} \text{ and } 0.88 \le V_{RPA} \le 1.0 & \text{(6b)} \\ I_{max} & I_{PQ} > I_{max} \text{ and } 0.88 \le V_{RPA} \le 1.0 & \text{(6c)} \\ 0.8 \times I_{pre} & 0.7 \le V_{RPA} \le 0.88 & \text{(6d)} \\ 0.2 \times I_{pre} & 0 \le V_{RPA} \le 0.7 & \text{(6e)} \end{cases}$$

where I is the inverter output current magnitude. I_{max} was set to 1.1 p.u. The fault current conditions in (6) are consistent

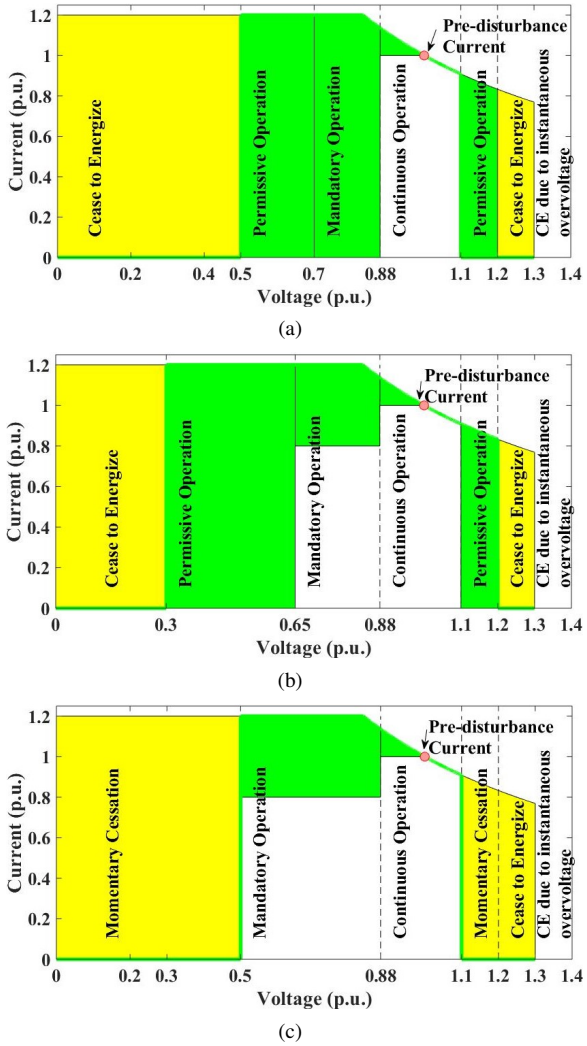

Fig. 2. Allowable current ranges after voltage disturbance according to IEEE 1547-2018 for pre-disturbance current = 1 p.u.; green and yellow shaded areas show allowable current range after RMS voltage detection time, while the green shaded area shows allowable current range after five line cycles. In MC and CE regions, the expected current is zero after the RMS voltage detection time (1-2 cycles). a) Category-I DERs b) Category-II DERs c) Category-III DERs

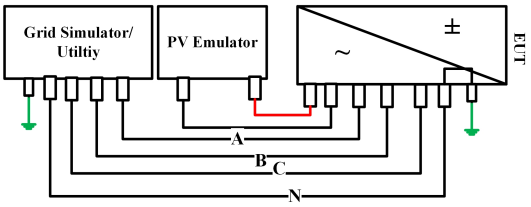

Fig. 3. Test setup to evaluate fault response of a commercial off-the-shelf inverter

with the requirements for Category II DERs. The inverters were tested for both symmetrical and asymmetrical faults. The test results are described in the following subsections.

A. Symmetrical Fault

Both the hardware inverter and the simulated inverter were subjected to various levels of three-phase symmetrical

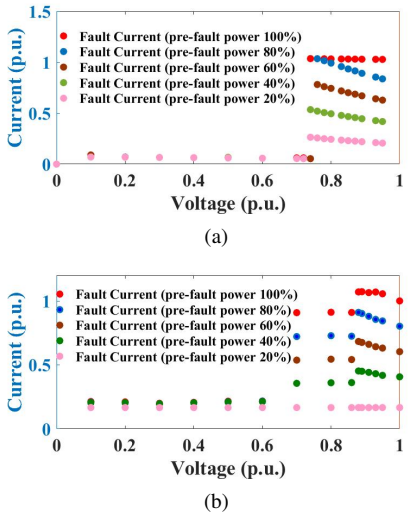

Fig. 4. Fault response for abnormal grid conditions a) commercial off-the-shelf inverter b) IEEE 1547-2018 compliant simulated inverter

TABLE I. DESCRIPTION OF THE SAG TYPES

Sag Type	Description
Sag Type A	Three-phase fault and three-phase-to-ground fault
Sag Type B	Single-phase-to-ground fault
Sag Type C	Phase-to-phase fault
Sag Type D	Propagation of a sag type C through transformer
Sag Type E	Two-phase to ground fault
Sag Type F	Propagation of a sag type E through transformer
Sag Type G	Propagation of a sag type E through two transformers

faults. Fig. 4(a) and Fig. 4(b) show the responses of the hardware and simulated inverters, respectively, for faults. The hardware inverter operates as a constant power source for voltage disturbances within the range of 0.74 p.u. to 1.0 p.u. unless the maximum current limit is reached. If the pre-fault current is 1.0 p.u., the hardware inverter maintains that current level in the voltage disturbance range of 0.74 p.u. to 1.0 p.u. If the voltage falls below 0.74 p.u., the hardware inverter operates as a constant current source with output current of about 0.07 p.u. for all pre-fault current levels. Other inverters tested exhibit different behavior (not shown). The simulated inverter was restricted in the fault response as defined in (6).

B. Asymmetrical Faults

Protection analysis using sequence components requires information on sequence components of the inverter fault current. The hardware inverter was tested for all seven types of sag listed in [12] to find its fault current sequence components. Brief descriptions of sag types A to G are shown in Table I. The sag types of Table I can be mathematically defined as (7), with further information (including transformer types where applicable) provided in [12].

$$[\overrightarrow{V}_a, \overrightarrow{V}_b, \overrightarrow{V}_c]^T = [M_a(\overrightarrow{D}), M_b(\overrightarrow{D}), M_c(\overrightarrow{D})]^T \overrightarrow{V_{sa}^+} \quad (7)$$

Here $\overrightarrow{V}_a$,$\overrightarrow{V}_b$,$\overrightarrow{V}_c$ are phase A, B, and C voltage phasors, respectively; $\overrightarrow{V_{sa}^+}$ is the nominal positive sequence voltage of phase A; and $\overrightarrow{D}$ is a fault-specific *characteristic phase angle jump*. T denotes the vector transpose and M_a, M_b, and M_c are $\overrightarrow{D}$ dependent functions whose value for different sag types can be found in [12]. $\overrightarrow{D}$ is a dimensionless complex number whose

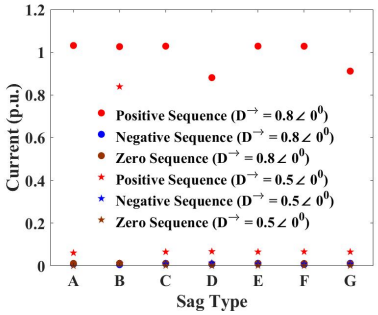

Fig. 5. Sequence components of fault current of the hardware inverter under different types of sag. (Negative and zero sequence currents are zero.)

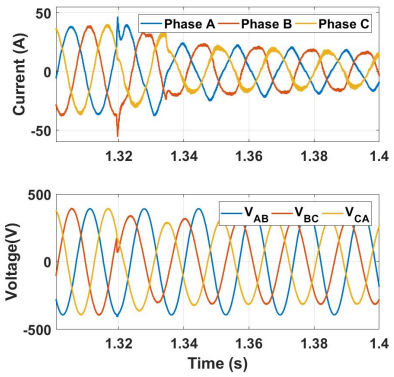

Fig. 6. Fault Current of the hardware inverter for an asymmetrical fault

value depends on source impedance, line impedance between PCC and fault, and fault impedance. The phase angle of $\overrightarrow{D}$ is the phase angle difference between the pre-fault voltage and the post-fault voltage. Fig. 5 summarizes the measured sequence components of the hardware inverter fault current under different types of sag for $\overrightarrow{D} = 0.8\angle 0°$ (denoting a high-impedance fault) and $\overrightarrow{D} = 0.5\angle 0°$ (denoting a low-impedance fault). The results shown in Fig. 5 indicate that the hardware inverter does not produce any negative or zero sequence current during unbalanced faults. This conforms to IEEE 1547-2018 as dynamic voltage support is not mandated. Fig. 6 shows the current waveform of the hardware inverter when the inverter is experiencing an unbalanced grid fault. It can be seen that even for an asymmetrical fault, the inverter output current is nearly symmetrical.

VI. Conclusion

The recently published IEEE 1547-2018 was analyzed in this paper to explore the potential responses of the standard-compliant DERs, specially IIDGs. It was found that IIDGs will behave as constant power sources in a narrow band of voltage excursion around the nominal voltage. Outside that narrow band, IIDGs can act like constant power sources or constant current sources for a wide range of voltage disturbances. Under the largest voltage excursions, IIDG fault current is limited by software-defined current limits. Though dynamic voltage support is mentioned in IEEE 1547-2018, it is not mandated or defined. So, IEEE 1547-2018 compliant IIDGs will most likely generate positive sequence current only for both symmetrical and asymmetrical faults. In addition, post-fault current magnitudes of IIDGs will be constrained to a narrower range (but not fully defined) by IEEE 1547-2018. For fault voltages in the 1547 momentary cessation and cease-to-energize regions, IIDG fault current is expected to be zero after a short RMS voltage detection time, potentially easing utility protection coordination.

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