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User Guide for PV Dynamic Model Simulation Written on PSCAD Platform

E. Muljadi, M. Singh, and V. Gevorgian
National Renewable Energy Laboratory

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Technical Report
NREL/TP-5D00-62053
November 2014

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National Renewable Energy Laboratory
15013 Denver West Parkway
Golden, CO 80401
303-275-3000 • www.nrel.gov

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List of Acronyms

AC	alternating current
CR-CSI	current-regulated current-source inverter
CR-VSI	current-regulated voltage-source inverter
CSI	current-source inverter
DC	direct current
HVRCM	high-voltage reactive-current management
IEEE	Institute of Electrical and Electronics Engineers
IGBT	insulated-gate bipolar transistor
LLG	line-to-line-to-ground
LVACM	low-voltage active-current management
LVPL	low-voltage power logic
PV	photovoltaic
REEC	renewable energy electrical controller
REGC	renewable energy generator controller
REMTF	Renewable Energy Modeling Task Force
REPC	renewable energy plant controller
SLG	single-line-to-ground
STATCOM	static compensation
SVC	static VAR compensator
VSI	voltage-source inverter
WECC	Western Electricity Coordinating Council

Executive Summary

This document describes the dynamic photovoltaic (PV) model developed by the National Renewable Energy Laboratory and is intended as a guide for users of these models. It is divided into five sections.

Section 1 presents the overview, and Section 2 presents different types of power converters. We begin with a discussion of the basic PV inverter and the control philosophy adapted for a power electronics-based generator, which we then contrast to the control philosophy for a conventional synchronous generator. A phasor diagram is used to represent the voltages and currents, including the magnitude and the phase angle; it is referred to throughout this application guide. Additional discussion is provided about the deployment of synchrophasors (phasor measurement units) throughout the power system network, which in the future will make controlling and implementing PV inverters and PV power plants easier. Because most PV inverters that are available in the market are based on a current-source inverter, we discuss this type of converter in detail to understand its operation and components.

Section 3 presents the control implementation of a PV inverter and a PV plant. The Renewable Energy Modeling Task Force (REMTF) of the Western Electricity Coordinating Council (WECC) developed an excellent document titled *Generic Solar Photovoltaic System Dynamic Simulation Model Specification*. The control diagrams presented in Section 3 are based on the PSCAD implementation of the WECC-REMTF control blocks derived from this document.

Section 4 gives examples of dynamic model validations using the data gathered from monitoring two PV plants. One of the two PV plants is a single-phase PV plant; the other is a three-phase PV power plant. When validating dynamic models, the input parameters are usually tuned and adjusted so that the output of the simulations matches the measured data. The tuned input parameters are documented and used to perform different simulations for the particular inverter and PV plant.

Finally, Section 5 presents the summary and conclusion, and the appendix presents the input parameters for the REMTF controllers. This input data is available from the WECC-REMTF document. Note that the PV inverter or PV plant is unique. The input parameters given in the appendix are generic typical input data. To ensure that the PV inverter and the PV plant dynamic models are well represented, the input data for the dynamic models provided by the PV inverter and PV plant owner/operator must be used.

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1 Introduction

The goal of the subtask on transient solar modeling (SS13-2020) is to develop and validate generic, open-source, flexible, three-phase, cycle-by-cycle models of photovoltaic (PV) inverters, PV plants, and their associated controls in PSCAD and disseminate these models to industry via an application guide and technical papers and reports.

The term *generic* is used to describe a model that is not specific to any manufacturer, which means that a dynamic model should be able to represent PV inverters from different manufacturers and not be specific to only one manufacturer. Different editions of PV inverters from the same manufacturer may implement similar control strategies but different ranges of settings. For example, various regional or market segments may have different grid codes, and a PV inverter may be set to accommodate local grid codes. The input parameters of the dynamic model to represent the PV plant at this location must be adapted accordingly. The dynamic model is also an open source; thus, it is easy to modify. Only the original file will be kept unchanged. The model also needs to be flexible so that changes can be made and/or added to the control block diagram to suit the specific design of a PV inverter or a specific PV plant. Also, this model is based on three phases; thus, the three phases—a, b, and c—are represented, instead of positive sequences only. This means that all the symmetrical components—positive sequence, negative sequence, and zero sequence—can be represented. This is important for a PV inverter, because many PV inverters are single phase, and many PV inverters are installed in the distribution network, which is susceptible to unbalanced conditions (from the network or voltages).

The completed PV generation dynamic model developed in this subtask is built on the PSCAD platform. The PV industry lacks such a model, and this project proposed to fill that gap down to the switch details via PSCAD. PSCAD allows for the analysis of unbalanced faults, such as single-line-to-ground (SLG) or line-to-line-to-ground (LLG), a key characteristic distinguishing PSCAD models from other dynamic models that focus on positive sequence behavior (e.g., PSLF and PSS/E). This program is intended as a cycle-by-cycle model of PV inverters, and it is built with detailed circuitry of the power converter (including the power semiconductor switches); thus, a detailed analysis of a PV inverter can be accomplished. For example, we can observe the dynamic of the voltage on the direct-current (DC) bus during the transmission faults, or we can observe the dynamic of the output currents and powers when one of the power semiconductor switches is damaged or misfired. The model is also intended to include the collector system of the PV plants and other plant-level controllers. The control architecture is based on the one developed by the Renewable Energy Modeling Task Force of the Western Electric Coordinating Council (WECC). There are three major blocks: the (1) renewable energy plant controller (REPC), (2) renewable energy electrical controller (REEC), and (3) renewable energy generator controller (REGC). The control block diagrams and their corresponding list of parameters are presented in the appendix.

In the previous report [1], we described the process of PV generation from the PV cell to the power converter, which includes the maximum power point tracker. In this report, we present different types of power converters (in Section 2), the control implementation (in Section 3), and the dynamic model validation (in Section 4). Finally, the summary and conclusion are presented in Section 5.

2 Basic Three-Phase PV Inverter

A three-phase PV inverter is usually designed for a three-phase system with a large rating (10 kW–2 MW and above). Most PV inverters are current controlled. To understand a basic PV inverter, it is important to understand the module and PV inverter hardware. In general, a PV inverter consists of a DC bus and three pairs of power semiconductors, also called power electronic switches or power switches. The most common power switches presently used are insulated-gate bipolar transistors (IGBT). An IGBT can be turned on and off very fast within microseconds (thus, the loss from power switching is low), and it has a low conduction loss.

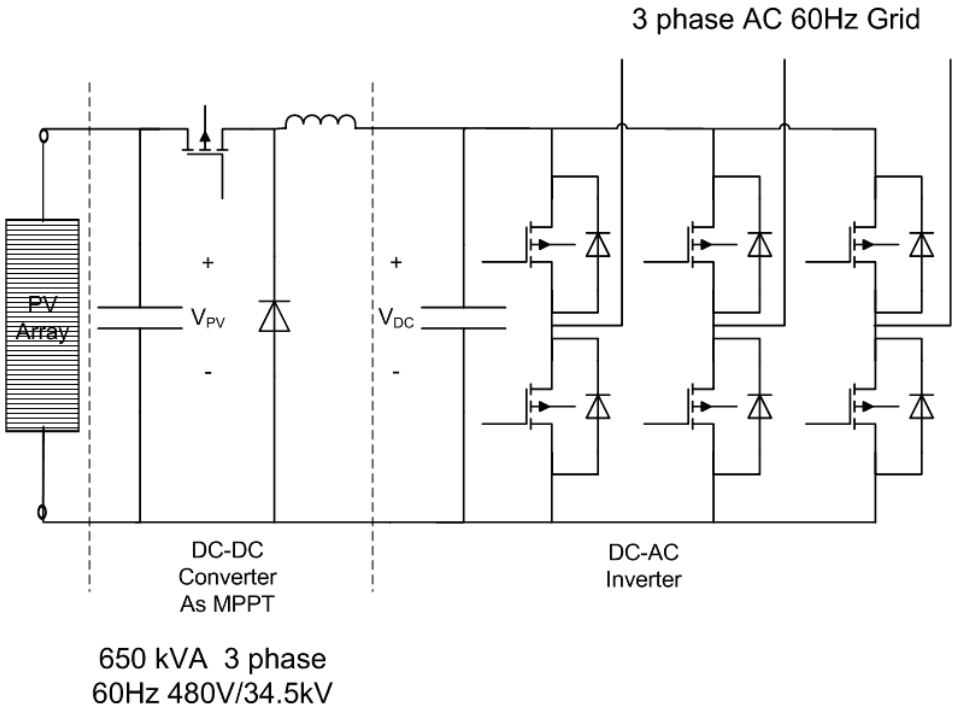


Figure 1. A typical three-phase PV inverter with IGBT power switches

2.1 Basic Control of Real and Reactive Power in a Two-Bus Power System

In this section, we use a two-bus system to illustrate real and reactive power for conventional generation and generation based on power converter based generation. We assume that the generator, $\mathbf{V_{pv}}$ (Bus 1), is connected to an infinite bus, $\mathbf{V_s}$ (Bus 2). In a conventional power plant with a synchronous generator, the following quantities are usually used to control the output of the generator:

- The voltage magnitude is used to control the reactive power (or reactive current component, $\mathbf{I_q}$ by controlling the excitation winding, thus increasing the voltage of $\mathbf{V_{pv}}$.
- The mechanical power is used to control the phase angle of the output voltage of the synchronous generator. The power angle, δ, of the output voltage mostly corresponds to the real current component, $\mathbf{I_p}$, of the output current, $\mathbf{I_s}$, of the voltage source.

A similar method can be used for a PV inverter, except we attempt to control the current directly.

2.1.1 Conventional Power System

2.1.1.1 Reactive Power Control

To understand a PV inverter and to simplify the analysis, let us consider an average model. Because the relationship of the reactive power to the terminal voltage is very tight, either the reactive power control or the voltage control is generally used. The phasor diagram concept is very useful to visualize the real power, reactive power, voltage, and current. It is also timely, as the synchrophasor measurements to monitor these quantities are available and have been installed massively in the modern power system network. The fundamental understanding of power systems in references [2, 3] and the concept and applications of synchrophasor measurement can be found in the references [4, 6].

To describe the relationship between the reactive power flow and the voltage level, refer to the phasor diagram shown in Figure 2. It is assumed that the PV inverter (terminal voltage, $\mathbf{V_{pv}}$) is connected to an infinite bus, $\mathbf{V_s}$, through a reactance, $\mathbf{X_s}$. The PV inverter ($\mathbf{V_{pv}}$) generates an output current, $\mathbf{I_s}$. The equation describing the relationship of the voltage at the two buses and the corresponding voltage drop across the reactance, $\mathbf{X_s}$, can be written as follows:

$$\boldsymbol{V_{pv} = V_s + j\, X_s\, I_s}$$

The reactive power losses ($\mathbf{Is^2\, X_s}$) in the transmission line can be supplied from Bus 1 ($\mathbf{V_{pv}}$) or Bus 2 ($\mathbf{V_s}$), or they can be shared by both sides. Parallel compensation (e.g., capacitor banks) can be implemented on both sides. Reactive compensation can be implemented by controlling the generator itself (internal control), or it can be provided externally, such as from adjustable capacitor banks, synchronous condensers, and static power compensation (a static VAR compensator, SVC; or static compensation, STATCOM).

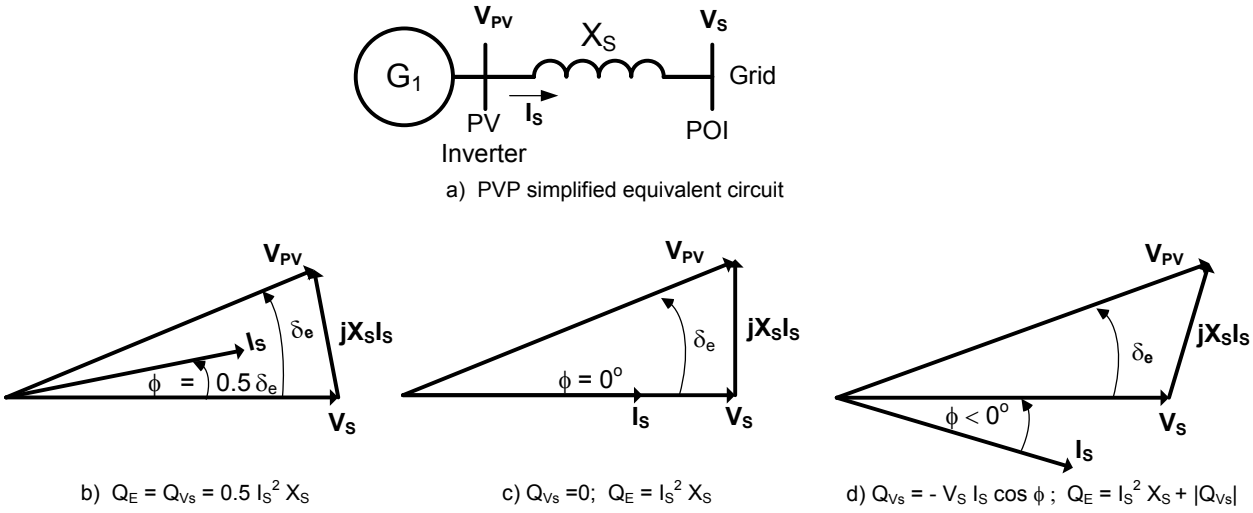


Figure 2. Illustration of a two-bus system demonstrating the voltage and reactive power flow in a synchronous generator

Consider Figure 2 (a), in which all the reactive power spent in the reactance, $\mathbf{X_s}$, is supplied by Bus 1. As shown, the voltage $\mathbf{V_{pv}} > V_s$, to make it possible for the reactive power to flow from Bus 1 to Bus 2. Similarly, as shown in Figure 2 (b), all the reactive power spent in the reactance, $\mathbf{X_s}$, is supplied by Bus 2. In this case, the relationship between the two voltages is $\mathbf{V_{pv}} < V_s$. Now consider Figure 2 (c), in which the voltages at Bus 1 and Bus 2 are maintained constant, and there is equal magnitude at 1.05 p.u. The reactive power is supplied equally by both Bus 1 and Bus 2. The voltage $\mathbf{V_{pv}} = V_s$ requires that the source of the reactive power comes from both sides. Thus, the larger the contribution of the reactive power, the higher the voltage of the source of the reactive power.

2.1.1.2 Real Power Control

The equation describing the relationship of the voltage at the two buses to the corresponding voltage drop across the reactance, $\mathbf{X_s}$, can be written as follows:

$$P = \frac{V_{PV} V_S}{X_S} \sin \delta$$

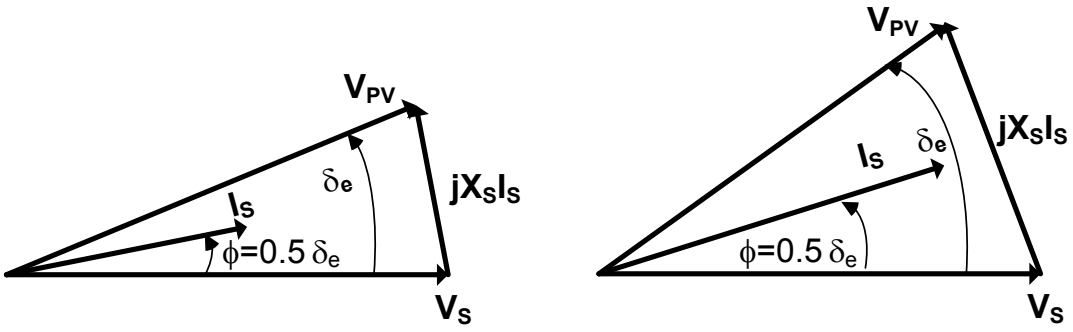


Figure 3. Illustration of a two-bus system demonstrating real power control in a conventional synchronous generator

Real power output can be increased in many ways. For example, increasing the real power output while maintaining equal voltage ($\mathbf{V_{pv}} = \mathbf{V_s}$) can be illustrated by the changes shown in the phasor diagrams in Figure 3. As mentioned above, in this equal-voltage condition both sides share the reactive power loss in the line reactance, $\mathbf{X_s}$, equally. As the current, $\mathbf{I_s}$, increases, the power angle, $\boldsymbol{\delta_e}$, also increases while equal voltage is maintained ($\mathbf{V_{pv}} = \mathbf{V_s}$).

2.1.2 Power-Converter-Based Power System

2.1.2.1 Reactive Power Control

Figure 4 illustrates the power converter based power system and its corresponding phasor diagram. The PV generator is connected to a grid through a reactance, $\mathbf{X_s}$. The current, $\mathbf{I_s}$, is decoupled into real and reactive components ($\mathbf{I_{p1}}$ and $\mathbf{I_{q1}}$). Assuming that the grid is an infinite bus, $\mathbf{V_s}$ is constant. The impact of reactive power's contribution on voltage regulation can be illustrated by the phasor diagrams shown in Figure 4 (b). As shown in Figure 4 (b), the phasor current, $\mathbf{I_s}$, is divided into the real current, $\mathbf{I_p}$, (in phase with the voltage $\mathbf{V_{pv}}$) and reactive current, $\mathbf{I_q}$, (in quadrature with respect to the voltage, $\mathbf{V_{pv}}$) components.

The voltage equation is rewritten as:

$$V_{PV} = V_s + j\,X_s\,(I_P + I_Q)$$

The real current component, $\mathbf{I_p}$, is proportional to the real power generated, and the reactive current, $\mathbf{I_q}$, is proportional to the reactive power generated. Doubling the reactive current, $\mathbf{I_q}$, will double the voltage drop, $\mathbf{I_q}\,\mathbf{X_s}$, and directly increase the terminal voltage, $\mathbf{V_{pv}}$, by an additional $\mathbf{I_q}\,\mathbf{X_s}$. Thus, to increase reactive current, we need to increase the voltage, $\mathbf{V_{pv}}$. The larger the value of $\mathbf{X_s}$, the higher the voltage, $\mathbf{V_{pv}}$, will increase as the same amount of the $\mathbf{I_q}$ current is increased. As can be expected, increasing the reactive component of the current, $\mathbf{I_q}$, will directly impact the terminal voltage magnitude, $\mathbf{V_{pv}}$, and increasing the real current component, $\mathbf{I_p}$, will more directly impact the power angle, δ, between $\mathbf{V_{pv}}$ and $\mathbf{V_s}$.

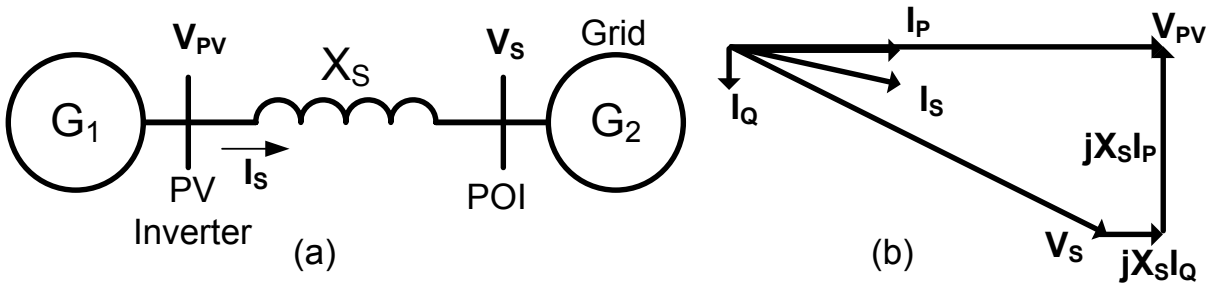


Figure 4. Illustration of a two-bus system in a PV inverter-based system with its corresponding phasor diagram

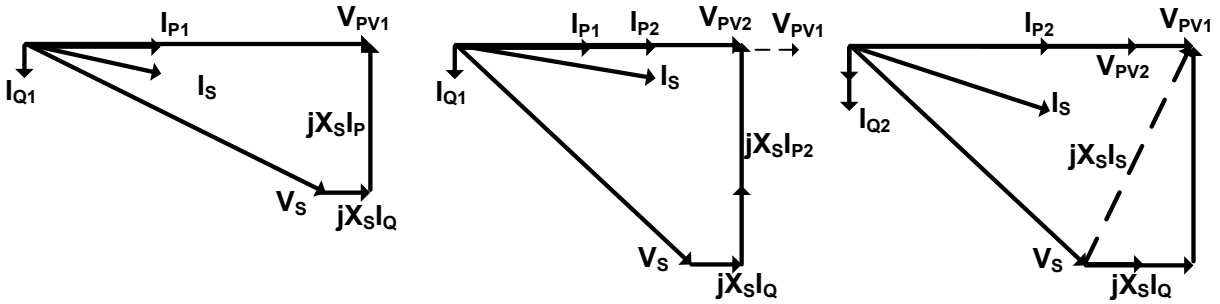
In PV generation, two limits must be observed:

- The total resultant current, $\mathbf{I_s}$, is limited by the maximum current-carrying capability of the power converter ($\mathbf{I_{max}}$). Thus, the power converter can increase its real or reactive current components (or both) only to a certain level, until the resultant current reaches its maximum ($\mathbf{I_s} = \mathbf{I_{max}}$ – current-carrying capability of the IGBT switches). At that point, the overcurrent protection will prevent the PV inverter from delivering more current.
- The maximum terminal voltage, $\mathbf{V_{pv}}$, must be limited to the maximum voltage of the power converter. Thus, the power converter can increase its reactive current component, $\mathbf{I_q}$, only so much, until the terminal voltage reaches its upper limit. At that point, the overvoltage protection will prevent the PV inverter unit from delivering more reactive current to the grid.

2.1.2.2 Real Power Control

Figure 5 (b) shows the size of the real current component increased to $\mathbf{I_{p2}}$, while the size of the reactive current component, $\mathbf{I_{q1}}$, is maintained. The additional voltage drop, $\mathbf{j}\mathbf{X_s}\,\mathbf{I_{p2}}$, is shown to increase by the same proportion. This affects the increase in the angle between $\mathbf{V_{pv1}}$ and $\mathbf{V_s}$. Because the size of the infinite bus, $\mathbf{V_s}$, is constant, the increase in $\mathbf{I_p}$ increases the voltage drop, but it decreases the voltage, $\mathbf{V_{pv2}}$. The size of the reactive current component stays the same, and the resulting voltage drop, $\mathbf{j}\,\mathbf{X_s}\,\mathbf{I_{q2}}$, also stays the same size. Note that the voltage, $\mathbf{V_{pv}}$, decreases from $\mathbf{V_{pv1}}$ to $\mathbf{V_{pv2}}$ (indicated by the dashed line in Figure 5 (b)). To return $\mathbf{V_{pv2}}$ to the same level as $\mathbf{V_{pv1}}$, the reactive current component, $\mathbf{I_q}$, is increased to $\mathbf{I_{q2}}$. This is shown in Figure 5 (c),

which indicates the size of the voltage, $\mathbf{V_{pv1}}$, and the size of the current, $\mathbf{I_{p2}}$. The increase in the output power is proportional to the change from $\mathbf{I_{p1}}$ to $\mathbf{I_{p2}}$, and the reactive current contribution to cover $\mathbf{I_s^2 X_s}$ loss are equally distributed between $\mathbf{V_{pv}}$ and $\mathbf{V_s}$.



(a). Baseline:, $I_p = I_{p1}$, $I_q = I_{q1}$ **(b). Increased: $I_p = I_{p2}$** **(c). $I_p = I_{p2}$, $I_q = I_{q2}$**

Figure 5. Illustration of a phasor diagram to demonstrate real and reactive power control in a PV inverter

2.2 Current-Source Inverter (CSI)—Average Model

Presently, most power converters are current-source inverters (CSIs). In the power drives, the current-control converter gives a very fast response to the torque required. In a grid-connected power converter, the current-control capability can give a quick response to the real and reactive power demand.

To understand a PV inverter, consider an average model, as shown in Figure 6. We consider an average model one of an ideal power converter that can generate a sinusoidal current (with no harmonics). Thus, we simulate a PV inverter as a sinusoidal-current source. The output current is synthesized to give a sinusoidal output current that has a controllable magnitude and phase angle. In a PV inverter, it is common to control the real ($\mathbf{I_p}$) and reactive ($\mathbf{I_q}$) components of the output currents.

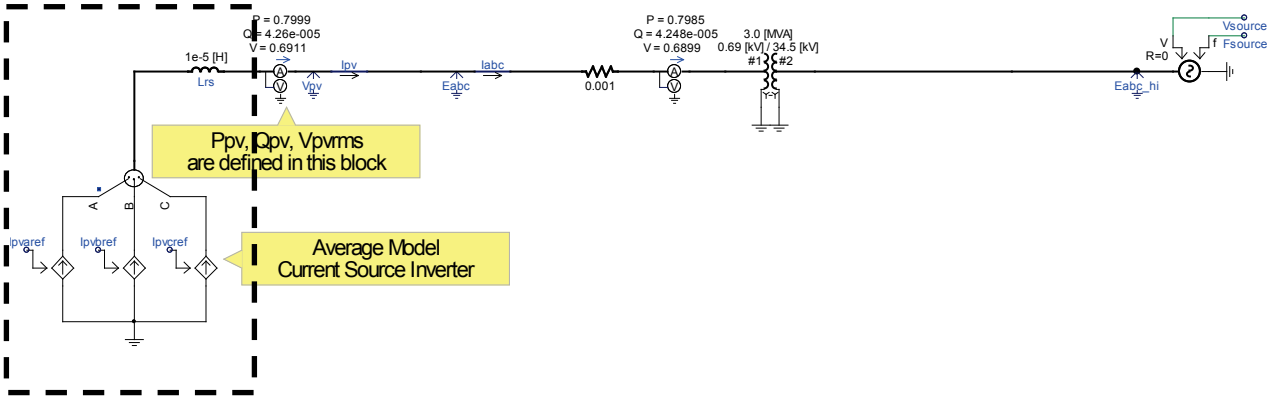


Figure 6. Illustration of an average model of a CSI synthesizing a PV inverter

The one-line diagram shown in Figure 6 above illustrates a three-phase PV inverter (an ideal model of a three-phase current source) connected to the grid. The DC-AC (alternating current) inverter has two major functions: (1) to control the real power output of the PV strings and (2) to control the reactive power output. In actual PV generation, the control of the real power is very simply implemented by maintaining a constant DC bus voltage while the controlling the DC-DC converter to maximize the output power of the PV module.

The CSI is the block inside the rectangle marked by the dashed black lines. The first thing to consider when controlling a CSI is to find the reference frame at the point of measurement to which it is connected. In this case, the reference is the terminal voltage of the PV inverter. The voltage sensor is placed at node $\mathbf{V_{pv}}$, as shown. Similarly, the real ($\mathbf{P_{pv}}$) and reactive power ($\mathbf{Q_{pv}}$) sensors are inside the multi-meter at the $\mathbf{V_{pv}}$ node.

Figure 7 below shows a simplified equivalent circuit of the current source producing the output current, $\mathbf{I_s}$. Using the d-q axis synchronized to the phasor voltage, $\mathbf{V_{pv}}$, we can decouple the current, $\mathbf{I_s}$, into its d-axis component (real current; $\mathbf{I_d} = \mathbf{I_p}$ component) and the q-axis, the reactive current component, $\mathbf{I_q}$. The real current component, $\mathbf{I_p}$, is used to control the output real power of the PV inverter. The control of the reactive current component, $\mathbf{I_q}$, is used to control the reactive power output of the PV inverter. PV inverter generates reactive power into a regular (non-infinite bus) grid. The terminal voltage increases as the reactive power output of the PV inverter increases. Consequently, controlling the reactive current component, $\mathbf{I_q}$, can be used to control the terminal voltage and vice versa.

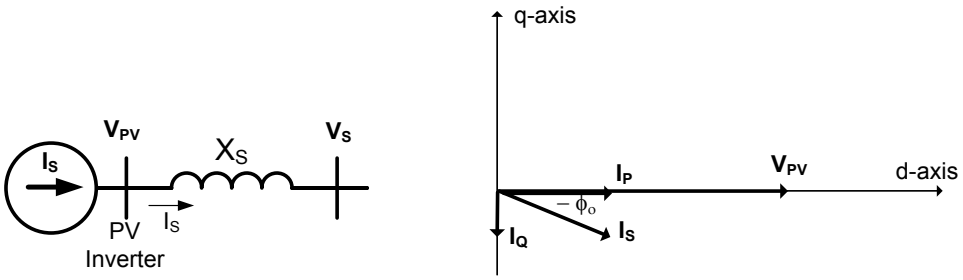


Figure 7. Illustration of a PV inverter equivalent circuit representing a three-phase current source connected to the grid and the corresponding terminal voltage phasor, V_{pv}, and the output current phasor, I_s, decoupled into I_p and I_q

The equation for the current can be expressed in a complex number.

$$\mathbf{V_{pv}} = V_{pv} \angle 0^o$$

$$\mathbf{I_s} = I_s \angle -\phi_o$$

Based on the arrow direction, by definition (generator convention), the apparent power generated by the PV inverter can be written as:

$$\mathbf{S_{pv}} = \mathbf{V_{pv}}\, \mathbf{I_s}^* = P + \mathbf{j}\, Q$$

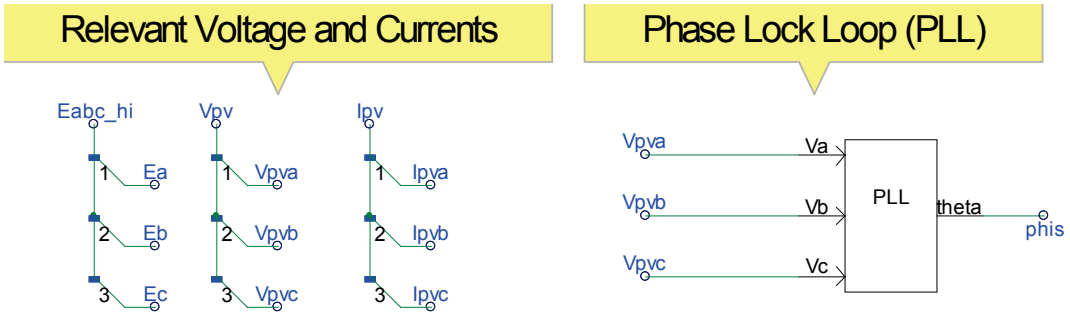
$$P = V_{pv}\, I_s \cos(\phi_o)$$

$$Q = V_{pv}\, I_s \sin(\phi_o)$$

The current conjugate of the output current is expressed as $\mathbf{I_s}^*$. Thus, both the real power and the reactive power have positive values (generated from the PV inverter).

The phase-locked loop shown in Figure 8 (b) is the synchronizer that will latch the reference frame to the synchronous reference frame attached to the voltage phasor, $\mathbf{V_{pv}}$, at the terminal of the PV inverter.

Note that after we found the reference frame of the terminal voltage, the real current component ($\mathbf{I_p}$) and the reactive current component ($\mathbf{I_q}$) can be oriented with respect to the "direct axis," which has the same phase angle of the the terminal voltage, $\mathbf{V_{pv}}$. Note that the subscript "p" indicates the real power component, and "q" indicates the reactive power component. The real power component, $\mathbf{I_p}$, is represented by the "direct" axis component (in phase with the synchronous reference frame, "d"); thus, it is sometimes used to indicate $\mathbf{I_p} = \mathbf{I_d}$; whereas the "q" also represents the "quadrature" axis component (in quadrature with respect to the direct axis, "d"), thus $\mathbf{I_q} = \mathbf{I_q}$.



(a) Monitored voltage and current

(b) Phase-locked loop to define the reference frame d-axis

Figure 8. Diagram illustrating the monitored voltage and current and the phase-locked loop to synchronize the reference frame to the terminal voltage

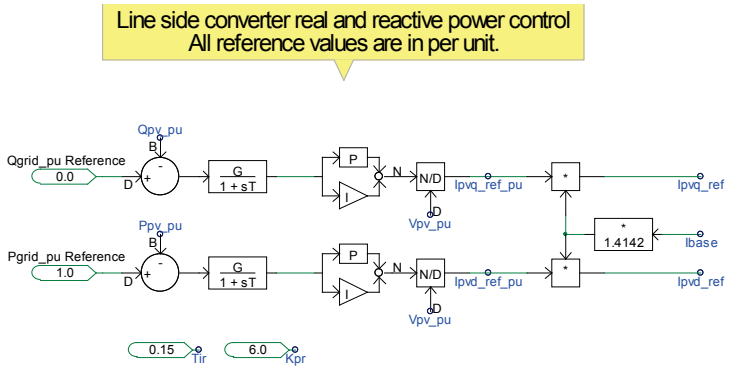


Figure 9. Diagram illustrating the real and reactive power reference per unit to compute the peak of the actual reference currents $\mathbf{I_q}$ and $\mathbf{I_d}$

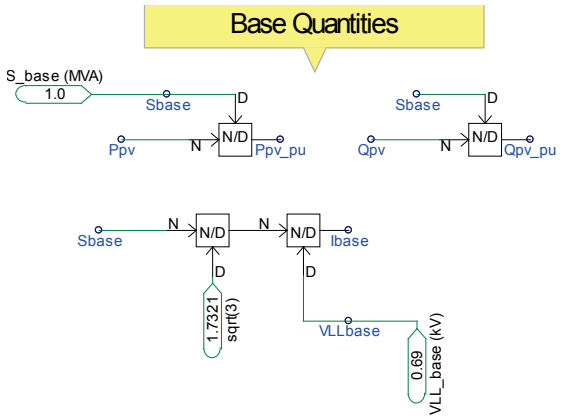


Figure 10. Diagram illustrating the base value calculations to be used in the control blocks

The diagram in Figure 9 shows a simple control to regulate the real and reactive power output of a PV inverter. The independent control is possible because the real and reactive currents are decoupled through the use of the synchronous reference frame calculation.

To use the same controller for differently sized power converters, and to avoid performing very complicated parameter tunings, it is common to use per-unit quantities. Figure 10 shows the base value calculations for the voltage, power, and current.

After the real ($\mathbf{I_{pvd\text{-}ref}}$) and reactive ($\mathbf{I_{pvq\text{-}ref}}$) current components in the synchronous reference frame have been computed, as shown in Figure 9 above, the quantities $\mathbf{I_{pvd\text{-}ref}}$ and $\mathbf{I_{pvq\text{-}ref}}$ can be transformed into the three-phase currents in the stationary reference frame (the time domain sinusoidal forms $\mathbf{I_{pvaref}}$, $\mathbf{I_{pvbref}}$, and $\mathbf{I_{pvcref}}$). These current signals are used to control the ideal current source to represent the CSI connected to the grid. Figure 12 and Figure 13 below show the reference current in the d-q axis using a synchronous reference frame and the three-phase reference currents in the time domain (the stationary reference frame), respectively.

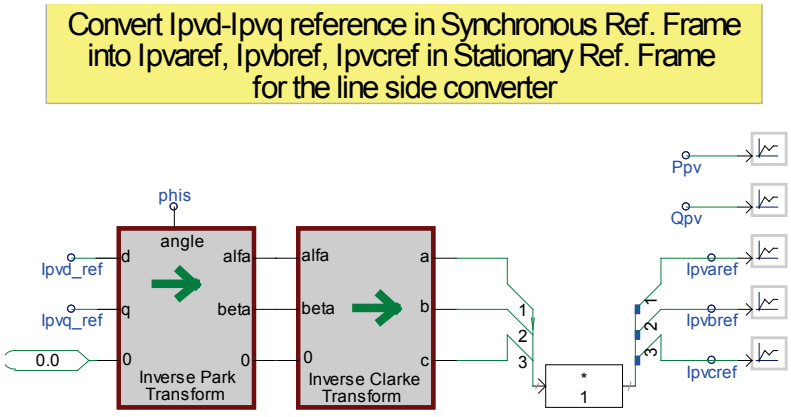


Figure 11. Diagram illustrating the reference currents to generate the specified real power reference, P_{grid_pu}, and the specified reactive power reference, Q_{grid_pu}

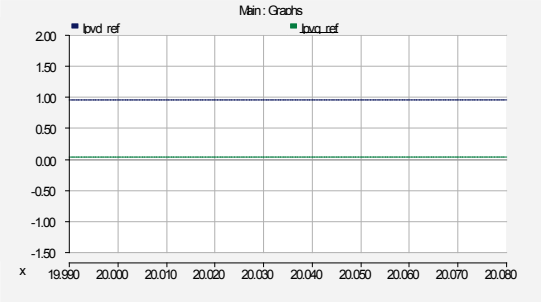


Figure 12. Real current, I_{pvd_ref}, and reactive reference current, I_{pvq_ref}, signals in the synchronous reference frame

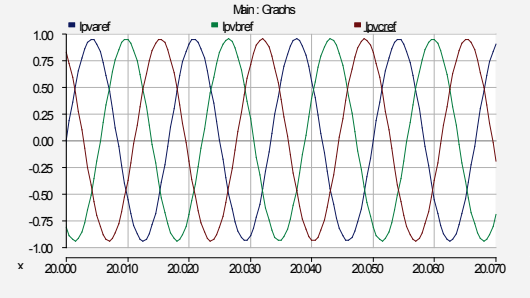


Figure 13. The three-phase reference signals—I_{pvaref}, I_{pvbref}, I_{pvcref}—in the stationary reference frame

Note that by using the average model, we can ignore the switching of the power switches, and we can assume that it has an infinite switching frequency—i.e., the resulting current is represented by the pure sinusoid generated by the controlled-current source to represent the practical CSI. One major advantage to this is that the simulations can be accomplished in a much shorter time, which allows us to perform many different types of dynamic simulations in power system studies.

2.3 CSI—Detail Model

A detailed model of a CSI is shown in Figure 14. The hardware of the power converter is represented by the real IGBT in parallel to its flywheel diode. The circuit driver is simulated by the real switching pattern commonly used in an actual power converter. The circuit is connected to the grid, as in the previous section. The only differences are that the ideal current source is replaced by an actual (hardware) power converter with six power switches and the firing control logic is implemented. The fundamental of power electronics converters, applications, and design can be found in reference [7]

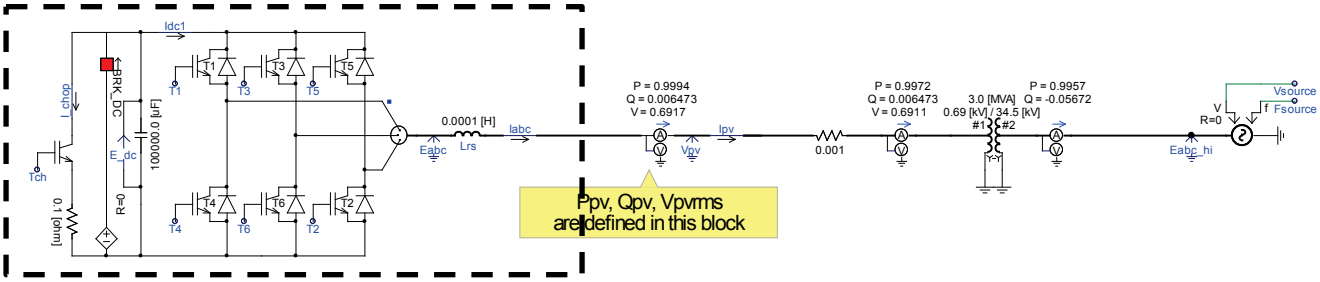


Figure 14. Diagram illustrating a three-phase CSI implementation with the actual six power switches (IGBTs)

2.3.1 Power-Switching Control

The commanded sinusoidal reference three-phase currents are compared to the actual three-phase currents (see Figure 15), and the errors are compared to a triangular waveform with a peak-to-peak value of ± 1. The currents are per-unitized by dividing the current errors by the base current. The outputs of the comparators are used as the firing signals to drive the base of the IGBTs; thus, they turn the IGBTs on and off.

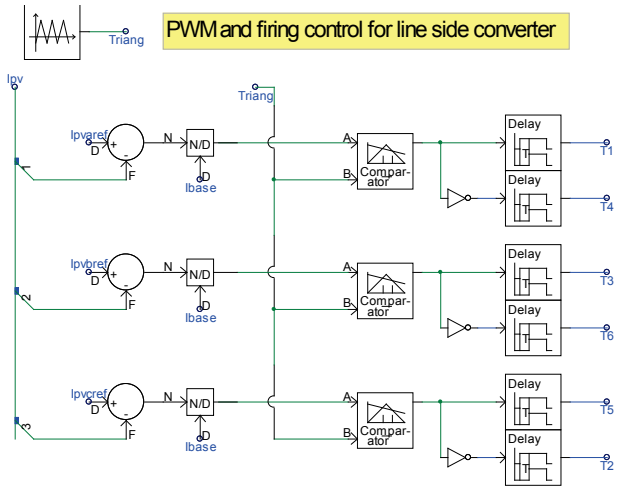


Figure 15. Diagram illustrating the logic circuits to turn the power switches in a CSI on and off in the correct order

The time delays are inserted in series with the firing signals to ensure that the top and bottom pairs of the IGBTs do not turn on at the same time to avoid short-circuiting the DC bus. This time delay is very small, in microseconds (modern IGBTs can turn on and off very fast). The detailed operation of the power converter is well-known technology that can be found in many power electronics textbooks.

2.3.2 Current-Regulated CSI

To regulate the real and reactive power output of the power converter, the same technique is used. The real ($\mathbf{I_{d\_ref}}$) and reactive current ($\mathbf{I_{q\_ref}}$) components are computed in the synchronous reference frame to obtain the phasor quantities, as shown in Figure 5 and Figure 7 above. The rotating reference frame is attached to the phasor voltage, $\mathbf{V_{pv}}$, and the rotating angle "phis" is found using the phase-locked loop.

The real and reactive current components ($\mathbf{I_{pvd\_ref}}$, $\mathbf{I_{pvq\_ref}}$) in the synchronous reference frame (see Figure 16) are then transformed back to the three-phase sinusoidal current references ($\mathbf{I_{pvaref}}$, $\mathbf{I_{pvbref}}$, $\mathbf{I_{pvcref}}$) in the stationary reference frame to drive the power switches of the IGBTs (see Figure 17).

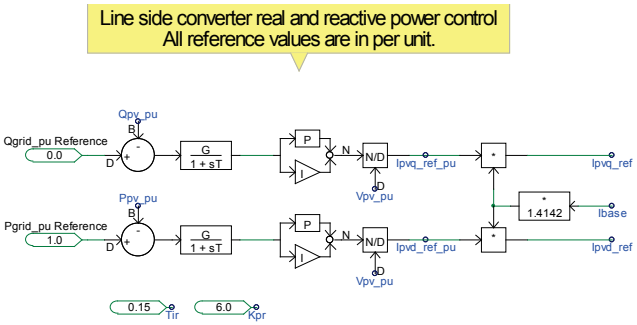


Figure 16. Diagram illustrating the real and reactive power references, per unit, to compute the peak of the reference currents, I_q and I_d

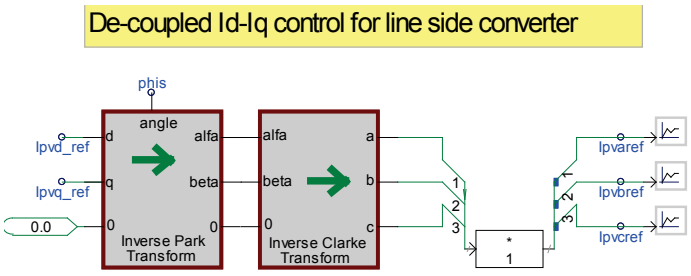


Figure 17. Diagram illustrating the inverse Park and inverse Clarke transformations to convert the synchronous referenced current signals, I_q and I_d, into the stationary reference frame current signals, I_a, I_b, and I_c

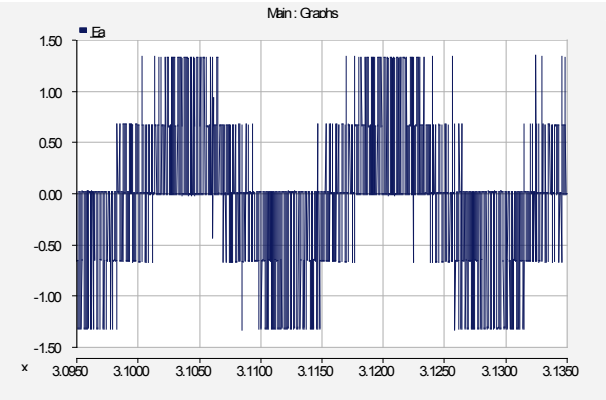


Figure 18. Phase voltage, V_{pva}, monitored at the terminal of the power converter

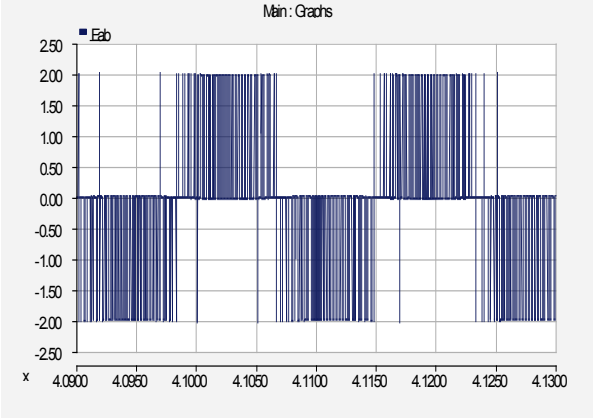


Figure 19. Line-to-line voltage, V_{pvab}, monitored at the terminal of the power converter

The per-phase voltage and the line-to-line voltage monitored at the terminal of the power converter are shown in Figure 18 and Figure 19 above. As can be expected, the output of the pulse-width modulation contains a lot of harmonics at the specified switching frequencies (900 Hz).

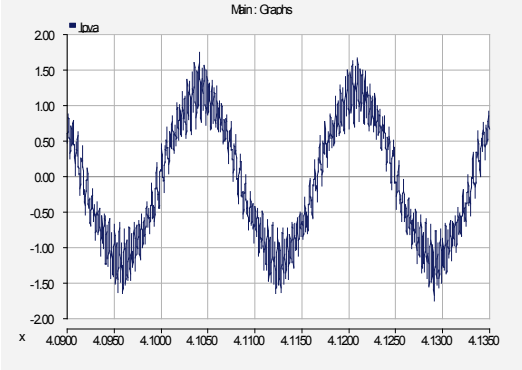


Figure 20. Line current output, I_a, of the power converter

As shown in Figure 20, the line current in Phase A is closer to the sinusoidal current, although the higher harmonic content is still visible. Note that the actual current is synthesized to follow the sinusoidal reference signal, $\mathbf{I_{pva\_ref}}$.

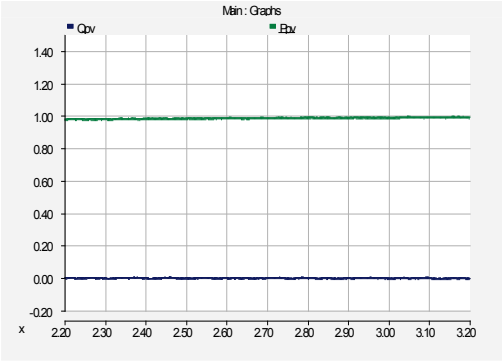


Figure 21. The real and reactive power measured at the output of the power converter

Figure 21 shows the measured real power and the reactive power at the terminal of the power converter. As the measurements are taken farther from the terminal of the PV inverter, the higher harmonic components of the currents are filtered out and the output voltage and currents look very sinusoidal.

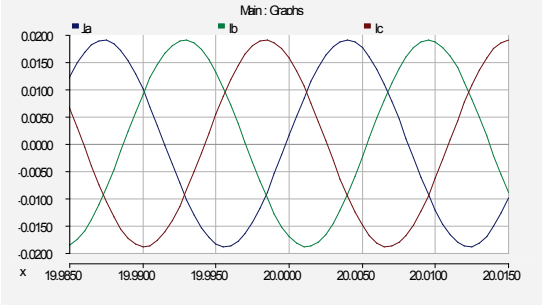


Figure 22. Three-phase line currents measured at the high side of the substation transformer

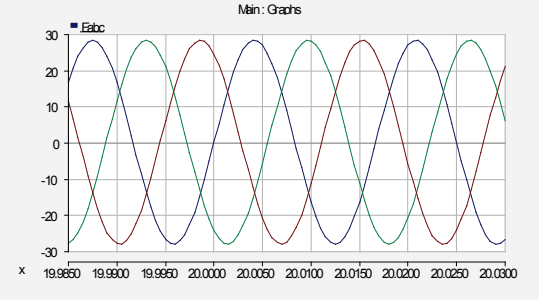


Figure 23. Three-phase voltage measured at the high side of the substation transformer

Figure 22 and Figure 23 show the measurements of the line currents and voltages taken at the high side of the substation transformer. As shown, the filtering of the line impedance very effectively cancelled most of the higher harmonics in both the currents and the voltages.

2.4 Voltage-Source Inverter (VSI)—Detail Model

A voltage-source inverter (VSI) synthesizes a voltage source connected to the grid. Because real and reactive power control is generally accomplished by controlling the reference currents, and controlling the voltage does not guarantee a direct response of the output currents, it is common practice to control the current indirectly by controlling the voltage output of the PV inverter. As shown below, the hardware for the VSI and the CSI are identical.

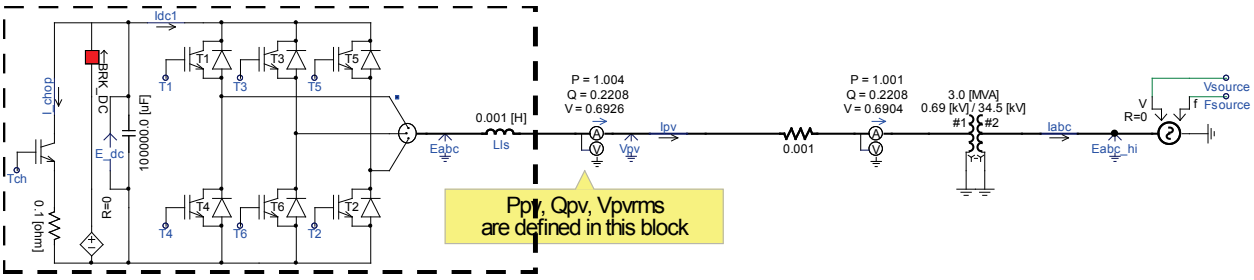


Figure 24. Diagram illustrating the three-phase VSI implementation with the actual six power-switches (IGBTs)

Figure 25 shows a comparison of the current-regulated current-source inverter (CR-CSI) to the current-regulated voltage source inverter (CR-VSI). The CR-CSI uses the reference current to generate a current signal to trigger the base drivers of the IGBTs and uses the current feedback to compare and correct the current errors to make accurate syntheses of the PV inverter output current. Thus, the filter inductance (represented by the reactance, $\mathbf{X_{ls}}$) does not have to be included in the equations used to generate the output currents.

The CR-VSI indirectly controls the output current. It uses the voltage feedback $\mathbf{V_{pv}}$ and the corresponding voltage drop across the filter inductance, $\mathbf{X_{ls}}$ $\mathbf{I_s}$, to synthesize the voltage feedback E that will produce the desired output currents ($\mathbf{I_{s\text{-}reference}}$). Thus, the filter inductance, $\mathbf{X_{ls}}$, must be included in the equations used to generate the voltage E.

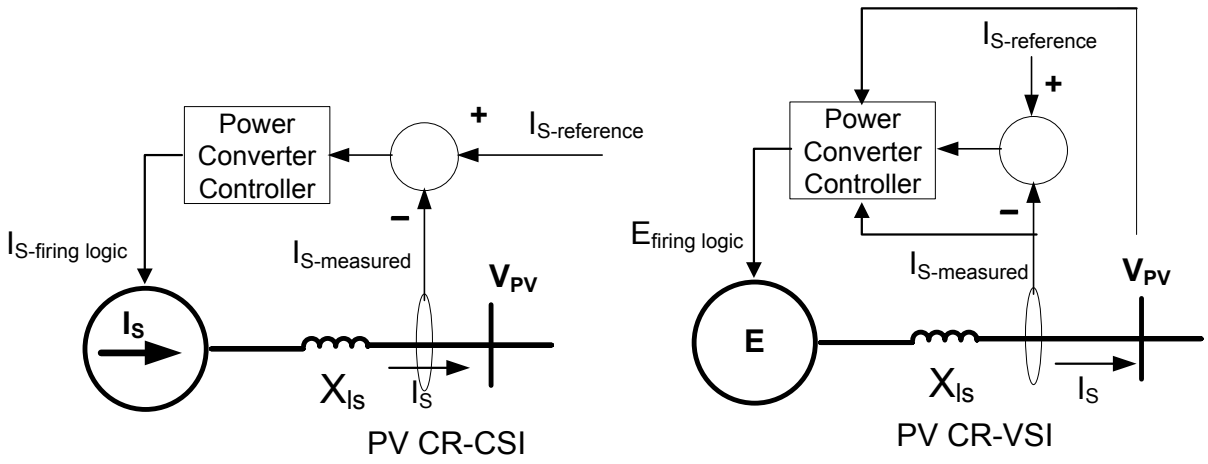
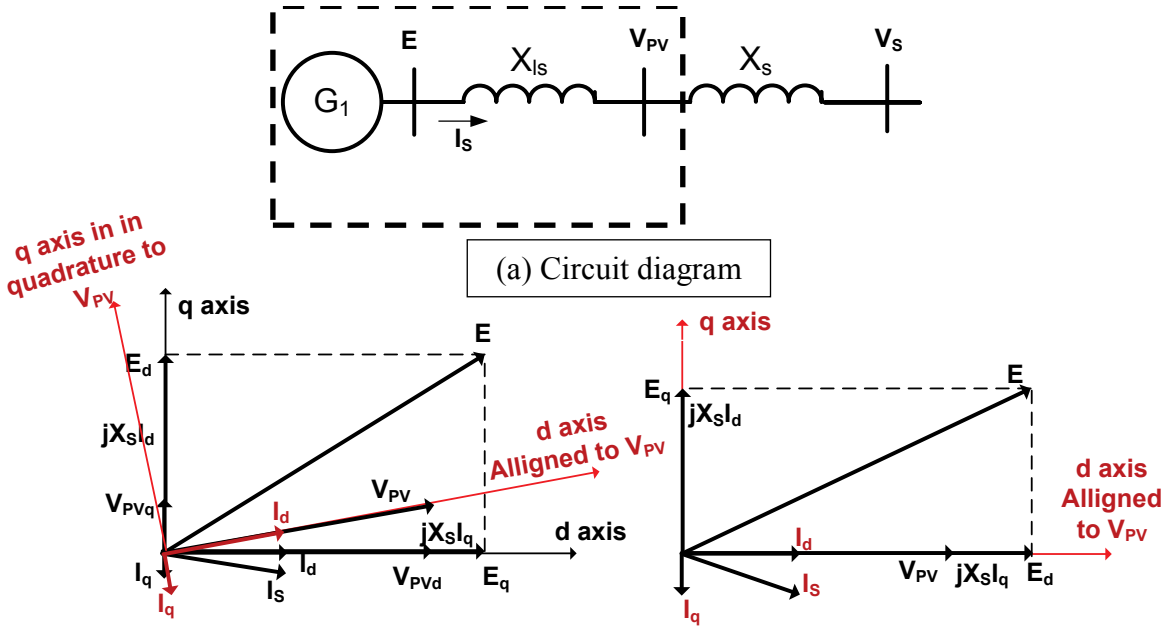


Figure 25. Diagram comparing the control philosophy of the CR-CSI to the CR-VSI

Consider Figure 26 (a), which shows the phasor diagram of the controller used to generate the voltage **E** in a CR-VSI. The single-line diagram of the power converter is enclosed in the dashed black lines. First, consider the voltage, $\mathbf{V_s}$, as an input to the phase-locked loop; thus, the d-axis is aligned to the voltage, $\mathbf{V_s}$. These phasor diagrams are shown in Figure 26 (b) and Figure 26 (c).



(b) Reference frame aligned to Eq **(c) Reference frame aligned to V_{pv}**

Figure 26. Diagram comparing the control philosophy of the CR-CSI to the CR-VSI

The equations governing the voltage can be written as:

$$\boldsymbol{E = V_{pv} + j\, X_{ls}\, I_s}$$

We can decouple the equation into its complex representation as:

$$\boldsymbol{E_d + jE_q = (V_{pvd} + jV_{pvq}) + j\,X_{ls}\,(I_d - jI_q)}$$

Or, this can be decoupled into two equations:

$$\boldsymbol{E_d = V_{pv} + X_{ls}\,I_q}$$

$$\boldsymbol{E_q = V_{pvq} + X_{ls}\,I_d}$$

As shown in Figure 26 (b), the Clarke and Park transformations can be used to transform the terminal voltages ($\mathbf{V_{pva}}$, $\mathbf{V_{pvb}}$, $\mathbf{V_{pvc}}$) in the stationary reference frame into the synchronous reference frame ($\mathbf{V_{pvd}}$ and $\mathbf{V_{pvq}}$). When the $\mathbf{V_{pv}}$ is used as the input to the phase-locked loop, the d-axis is aligned to the phasor voltage, $\mathbf{V_{pv}}$, and the phasor, $\mathbf{V_{pvq}} = \mathbf{0}$, as represented by the phasor diagrams shown in the Figure 26 (c). Description about Clark and Park transformations can be found in references [1] and [8, 9].

$$\boldsymbol{E_d = V_{pvd} + X_{ls}\,I_q}$$

$$\boldsymbol{V_{pvq} = 0}$$

The q-axis equation can be rewritten as:

$$\boldsymbol{E_q = X_{ls}\,I_d}$$

Figure 27 shows the implementation of the voltage reference signals $\mathbf{E_d}$ and $\mathbf{E_q}$. Additional input to make any corrections is also implemented using the PI controller to ensure that the reference real power and reactive power can be maintained.

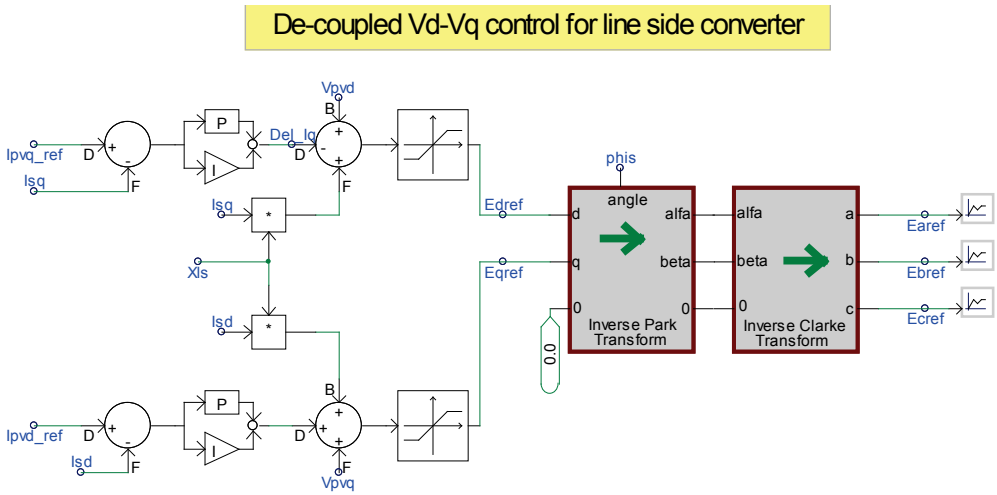


Figure 27. Diagram illustrating the three-phase voltage signal reference used to trigger the firing circuits of the VSI

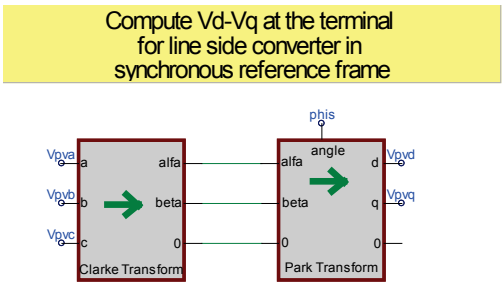


Figure 28. The transformation from V_{pv} (a,b,c) into V_{pvd} and V_{pvq} in the synchronous reference frame

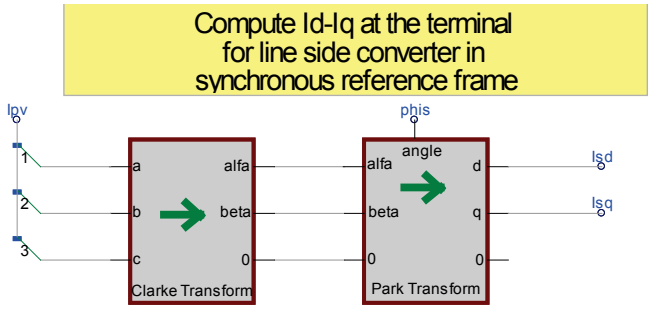


Figure 29. The transformation from I_{pv} (a,b,c) into I_{sd} and I_{sq} in the synchronous reference frame

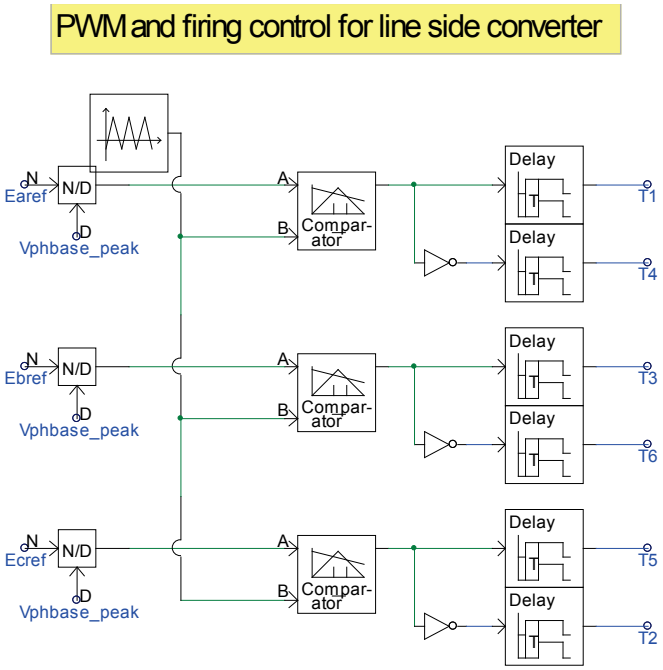


Figure 30. The logic circuits to turn the power switches in the CSI on and off in the correct order

After the voltage reference signals of the $\mathbf{E}_{\mathbf{qref}}$ and $\mathbf{E}_{\mathbf{dref}}$ have been computed in the synchronous reference frame, the three-phase voltage signals ($\mathbf{E}_{\mathbf{aref}}$, $\mathbf{E}_{\mathbf{bref}}$, $\mathbf{E}_{\mathbf{cref}}$) in the stationary reference frame can be generated and fed into the firing circuit board (shown in Figure 30) of the power converter to turn the IGBTs on and off in the correct sequence.

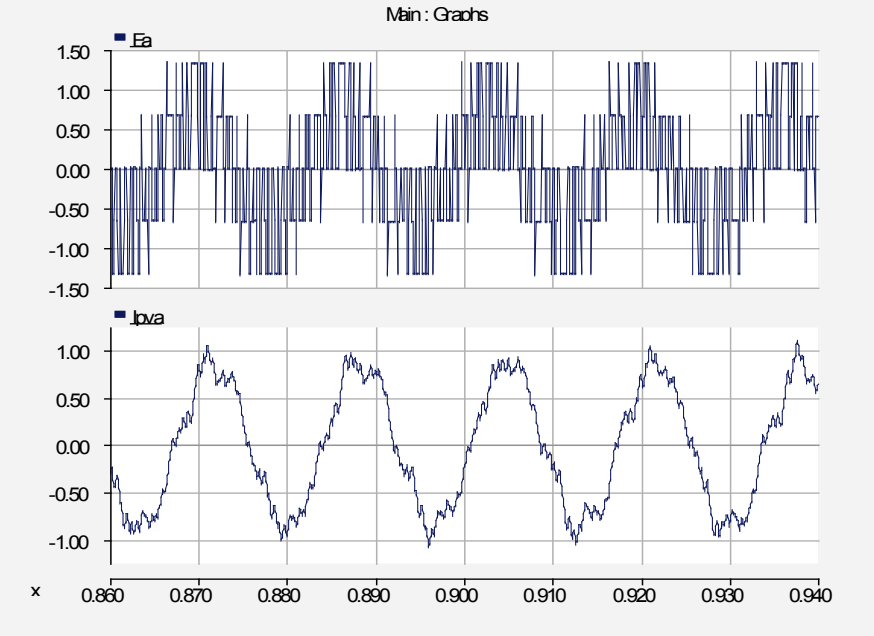


Figure 31. Per-phase voltage and line current of the CR-VSI

Figure 31 presents an example of the per-phase voltage and the line-current output of the CR-VSI. Note that the current waveform is less sinusoidal compared to that of the CR-CSI, because the power converter is not commanded to follow the reference currents; instead, it is commanded to synthesize the reference voltages, $\mathbf{E}_{\mathbf{aref}}$, $\mathbf{E}_{\mathbf{bref}}$, and $\mathbf{E}_{\mathbf{cref}}$.

3 Controlling the Grid-Side Inverter and Power Plant

The PV inverter is the point of conversion from DC to AC power. In small residential applications, the PV inverter is usually single phase, converting DC to single-phase AC (60 Hz). The PV array is connected to the PV inverter via a maximum power point tracker to optimize energy conversion from sunlight to electrical power. A detailed discussion about this process is not included in this report. A PV inverter for large-scale installation usually comes in three-phase arrangements. The PV inverter combines the output of rows of PV strings in DC and converts them to AC. For example, an inverter can processes the output of a PV array with 500 PV modules. Three-phase output rated at 208 V or 480 V is commonly found in commercial PV inverters. Again, it must be emphasized that the topology described here is a single-stage topology, and controls for multi-level and multi-stage converters will require significant modifications from the ones described here.

In this chapter, we implement a controller based on the controllers developed and recommended by the WECC Renewable Energy Modeling Task Force (REMTF) [10]. A block diagram illustrating an overview of PV power plant control is shown in Figure 32. From left to right, the highest level of control is implemented first, by the control block REPC; to the REEC, with a focus on the level of the PV inverter; then to the REGC, which is implemented to correct utility interface issues. The block diagrams and corresponding parameters are listed in the appendix.

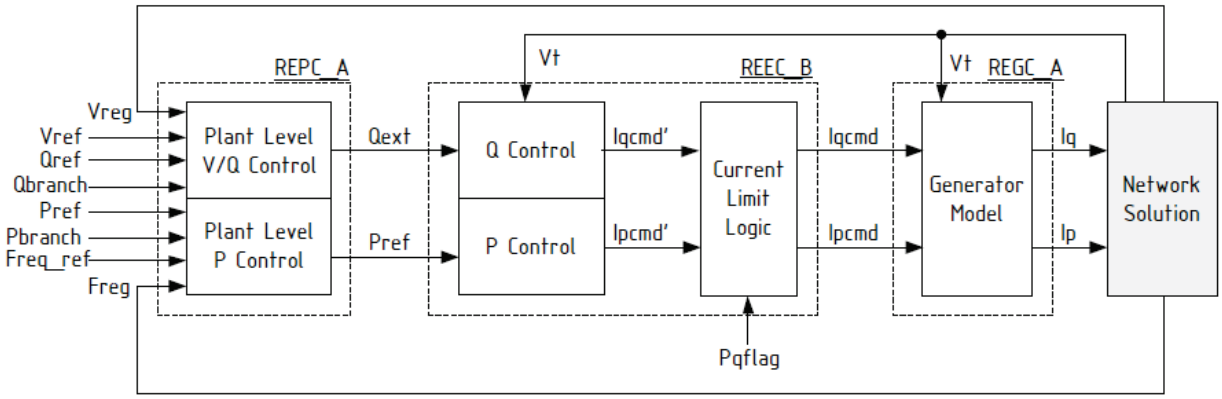


Figure 32. Block diagram representing a PV power plant

- REPC—This supervisory control is implemented to control the real and reactive power of an entire PV power plant. Inputs may include the reference voltage ($\mathbf{V_{ref}}$), reference reactive power ($\mathbf{Q_{ref}}$), reference real power ($\mathbf{P_{ref}}$), and reference frequency ($\mathbf{Freq_{ref}}$). Thus, the control block functions to control the real power output to respond to a frequency disturbance (and/or governor response) and to respond to a voltage regulation at a bus (at the point of interconnection or at the remote bus).
- REEC—This power-converter control is implemented to limit the currents based on the carrying capability of the power switches (i.e., IGBT and free-wheeling diode). Different types of reactive power control are implemented in this block as well.
- REGC—This generator control is implemented to the grid interface (under-/overvoltage scenarios) and enables nonlinear current control capability.

3.1 Device Level

A PV inverter is a mature technology developed early on by the power drive industry for adjustable-speed drives, also known as adjustable-frequency drives, used to control the variable-speed operation of electric machines (e.g., induction motors) with torque or speed-control capabilities. Later, grid-interface technology was also developed extensively by the industry to provide uninterruptible power supply for the computer industry. Thus, the basic operations have been developed based on the experiences gained by the various industries. The details of the design, analysis, and protection at the device level can be found in many power electronics textbooks.

3.2 Generator Level

At the generator level, the controller focuses on power-converter control and protection at the power-converter level. Two controllers to serve these functions have been developed by the WECC-REMTF. These controllers are meant to provide good grid integration to allow a PV converter to interface with the utility grid according to local standards and regulations. A PV controller can be set to provide fault ride-through capability, current limit protection, instantaneous and independent control of real and reactive power, and ancillary services to the grid.

3.2.1 REGC

The REGC is the first controller to be implemented and is directly connected to the power converter driver logic. As shown Figure 33, the inputs to this block are the commanded real power (P) current component ($\mathbf{I_{pcmd}}$) in phase with the voltage ($\mathbf{V_t}$), and the commanded reactive power (Q) current component ($\mathbf{I_{qcmd}}$), the current component in quadrature (perpendicular) to the voltage $\mathbf{V_t}$. The total current ($\mathbf{I_{cmd}}$) consists of the two components: $\mathbf{I_{pcmd}}$ and $\mathbf{I_{qcmd}}$. The REGC is intended to ensure that the power converter has ride-through capability when exposed to local disturbances or transmission line faults.

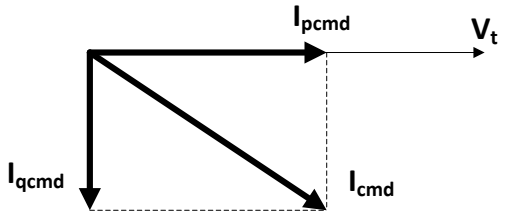


Figure 33. Phasor diagram illustrating commanded current and its real and reactive components

The outputs to this block are the commanded real power (P) current component ($\mathbf{I_{pord}}$), the current component in phase with the voltage $\mathbf{V_t}$, and the commanded reactive power (Q) current component ($\mathbf{I_{qord}}$), the current component in quadrature (perpendicular) to the voltage $\mathbf{V_t}$. Both of these quantities ($\mathbf{I_{pord}}$ and $\mathbf{I_{pord}}$) are the adjusted input values during high- or low-voltage operation.

The REPG uses per-unit quantities and the generator base (PV inverter base; e.g., MBASE = 1.5 MVA) instead of a system base or PV power plant base (e.g., SBASE = 60 MVA). However, if a single-generator representation is used, the REPG uses MBASE = SBASE.

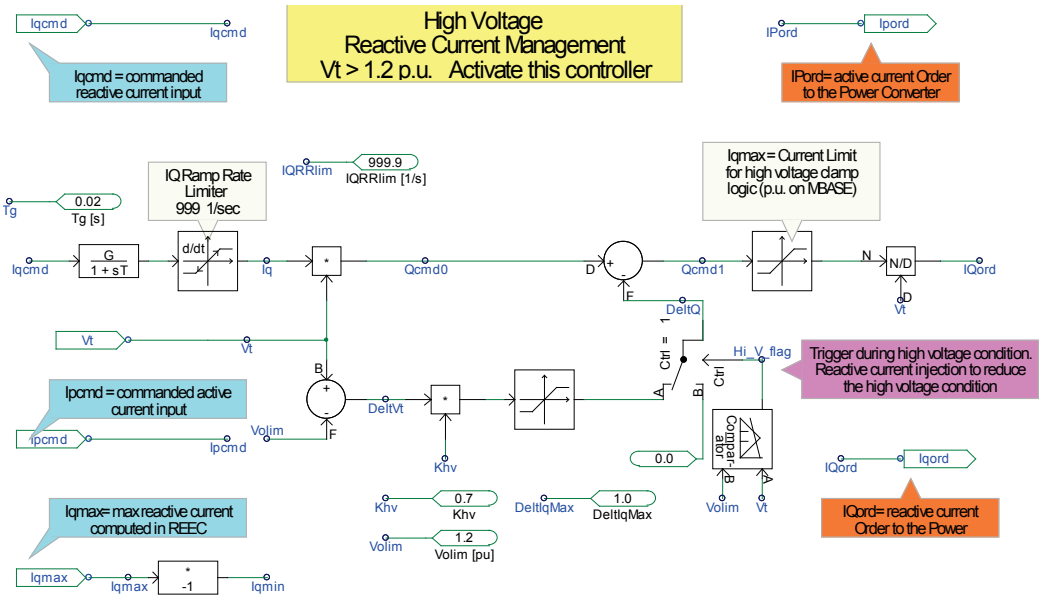


Figure 34. Block diagram illustrating the HVRCM controller to inject additional inductive current during a high-voltage event

As shown in the block diagram in Figure 34, the high-voltage reactive-current management (HVRCM) functions to alter the control behavior of the reactive power during high-voltage operation (e.g., higher than 1.2 p.u.), and the low-voltage active-current management (LVACM) functions to alter the control behavior of the active power during low-voltage operation (e.g., lower than 0.9 p.u.).

3.2.1.1 High-Voltage Region

The block diagram shown in Figure 35 below can be used to describe the control functions of the HVRCM. The term *reactive current* is used to describe both the inductive current and capacitive current. Inductive current is the current that causes a power converter to absorb reactive power, and the capacitive current is the current that causes a power converter to produce reactive power.

The HVRCM has the control property to change the output reactive current command (I_{qcmd}) by providing an additional inductive current injection to decrease the reactive power output of the power converter, thus indirectly reducing the terminal voltage of the power converter. It also has a ramp-rate limiter to limit the rate of change in the reactive current output.

In analogy to the droop, in a power plant governor this HVRCM also functions to increase the inductive current to draw more reactive current from the grid, thus, in effect, reducing the terminal voltage.

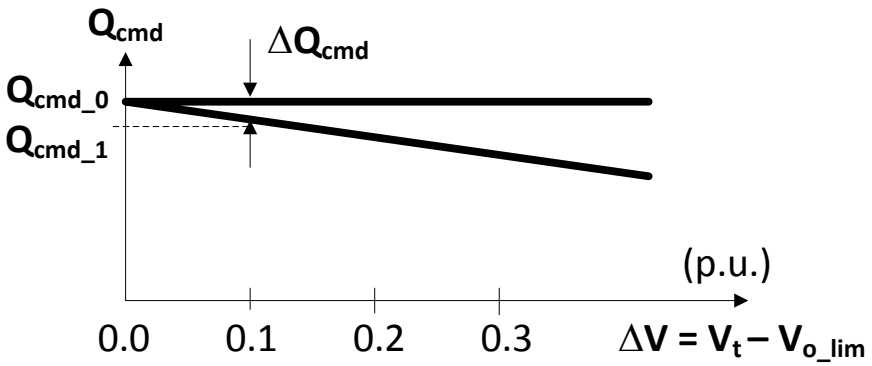


Figure 35. Block diagram illustrating the HVRCM controller to inject additional inductive current during a high-voltage event

Figure 35 describes the changes in reactive power command if the terminal voltage (V_t) exceeds the threshold voltage ($\mathbf{V_{olim}}$). The slope of the line is specified as the constant ($\mathbf{K_{hv}}$).

Note that the additional current injection is not activated until the level of the terminal voltage passes the overvoltage limit ($\mathbf{V_{olim}}$). The sensor used to activate this function is embedded in the comparator with the logic output Hi_V_flag = 1.

Under normal circumstances (the logic output Hi_V_flag = 0):

$$\Delta Q = 0$$

$$I_{qcmd1} = I_{qcmd0}$$

However, when the Hi_V_flag = 1, the inductive current injection is activated, and the following equations are used to govern the output of the inductive current injector:

$$\Delta V_t = V_{olim} - V_t$$

$$\Delta Q = Q_{cmd0} - Q_{cmd1}$$

$$\Delta Q = K_{hv}\, \Delta V$$

$$I_{qcmd1} = I_{qcmd0} - \frac{\Delta Q}{V_t}$$

Take, for example, V_{olim}= 1.2 p.u., K_{hv} = 0.7, the initial I_{qcmd} = 0.1 p.u. at the terminal voltage of V_t = 1.0 p.u. The terminal voltage suddenly increases to V_t = 1.3 p.u. because of an external disturbance. The reactive power, which was initially Q_{cmd_0} = 0.1 p.u. during the high-voltage event, decreases to Q_{cmd_1} = (0.1 - 0.07) p.u. = 0.03 p.u. Note that the current limiter is placed to ensure that the $\mathbf{I_{qmax}}$ (computed in the REEC block) is not exceeded.

The choice of $\mathbf{K_{hv}}$ is certainly determined by the local power system network. If the voltage in the local network varies a wide range above normal, the value of $\mathbf{K_{hv}}$ can be adjusted

accordingly. The impact from a single PV inverter to suddenly change the voltage level may not be significant; however, the collective impact of hundreds of PV inverters connected to the grid following the same command will definitely be very effective. Also note that the current limits must be set to the limit of the reactive power capability of the power converter. These currents are limited before the commanded currents are passed to the power switches via the variable $\mathbf{I_{qord}}$.

3.2.1.2 Low-Voltage Region

The block diagram shown in Figure 36 below can be used to describe the control functions of the LVACM. The term *active current* is used to describe the real or active power component (e.g., $\mathbf{I_{pcmd}}$ or $\mathbf{I_{pord}}$).

In summary, the LVACM allows two choices determined by the low-voltage power logic, or LVPL (the upper limit of $\mathbf{I_{pcmd}}$), switch. If LVPL = 1, the upper limit of the real power current component $\mathbf{I_{pcmd}}$ is governed by the nonlinear map LVPL compared to $\mathbf{V_t}$. If LVPL = 0, the upper limit of the real power current component $\mathbf{I_{pcmd}}$ is governed by $\mathbf{I_{pmax}}$ computed in another controller block called REEC (discussed below).

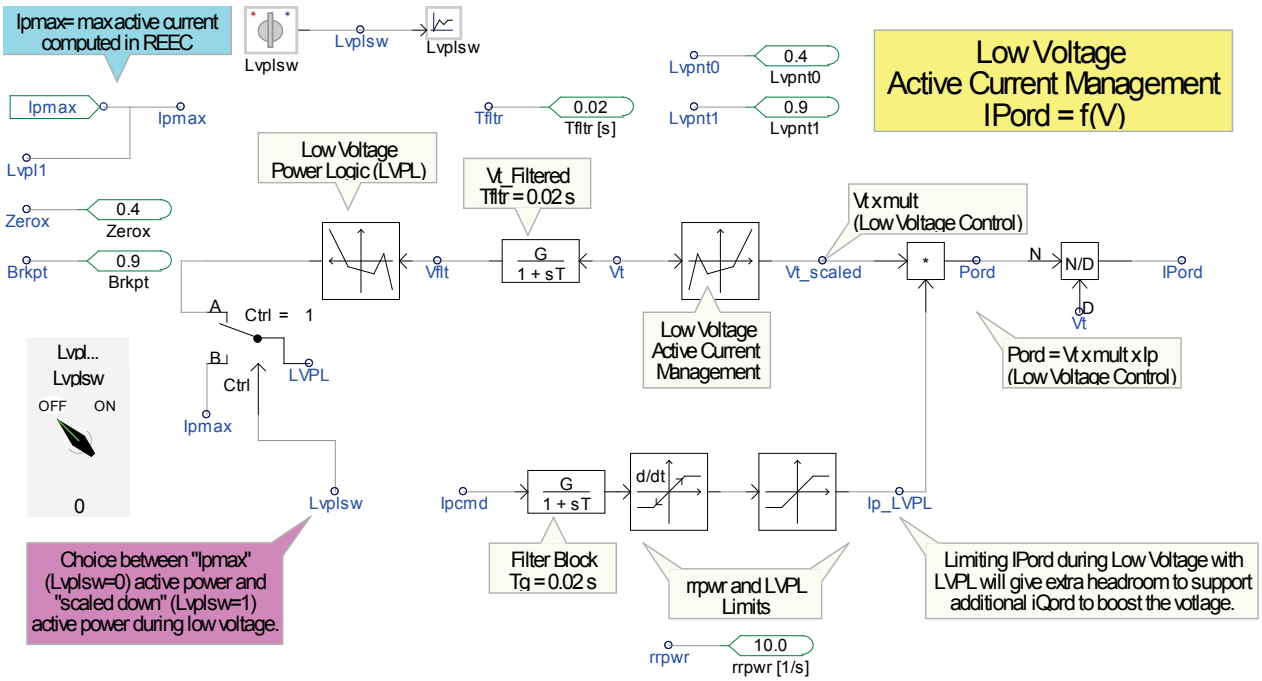


Figure 36. Block diagram illustrating the LVACM controller to adjust the real current component ($\mathbf{I_{pcmd}}$) during a low-voltage event

The block diagram in Figure 36 shows two quantities that should be computed. The first one is the scaled voltage ($\mathbf{V_{t\_scaled}}$), and the second one is the upper limit of the real current component (LVPL).

3.2.1.2.1 Computing $\mathbf{V_{t\_scaled}}$

Consider the $\mathbf{V_{t\_scaled}}$ computation. $\mathbf{V_{t\_scaled}}$ is computed from preprogrammed map shown in Figure 37. During a low-voltage event, the commanded power ($\mathbf{P_{ord}}$) must be scaled down to

accommodate the current-carrying capability of the power switches (IGBT and diodes). The $\mathbf{P_{ord}}$ should be scaled such that the resulting $\mathbf{I_{pord}}$ current will be within the allowable limit.

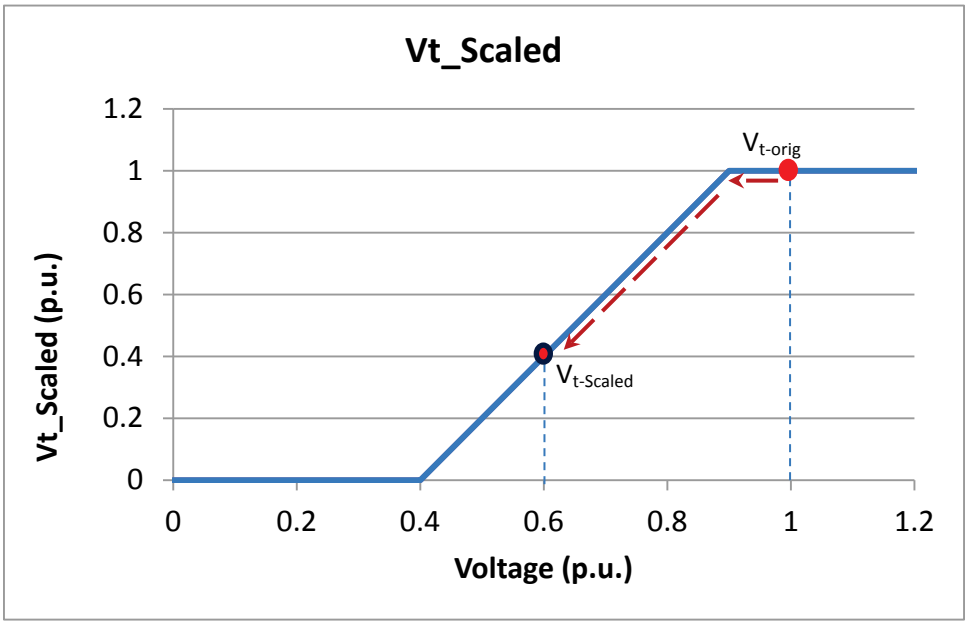


Figure 37. Scaled voltage to adjust the P_{ord} during a low-voltage event

For example, if the original commanded power P_{ord} = 1.0 p.u., under normal voltage (V_t = 1.0 p.u.), the commanded real power stays the same. Suppose during a grid disturbance the voltage drops to V_t = 0.6 p.u.; without scaling, the computed current command would be very high (I_{pcmd} = P_{ord}/V_t = 1.0/0.6 = 1.67 p.u.), which is much larger that the allowable current limit ($I_{pmax} \simeq$ 1.2 p.u.). Thus, by scaling the voltage accordingly, the new P_{ord} = V_{t_scaled} x 1.0 p.u. = 0.4 x 1.0, which gives the new P_{ord} = 0.4 p.u.

Note that when voltage is within the normal range (0.9 p.u.< V_t < 1.1 p.u.), the power converter must be capable of delivering P_{ord} = 1.0 p.u.; thus, the voltage is scaled to 1.0 for voltages V_t > 0.9 p.u. For example, at V_t = 0.9 p.u., the P_{ord} = 1.0 p.u. and I_{pcmd} = 1.11 p.u., which is within the maximum current limit

3.2.1.2.2 Computing LVPL

The second quantity of interest is the LVPL. This quantity is actually the upper limit of the real power component. There are two options based on the position of the logical switch, **LVPLsw**. If LVPLsw = 0, the value of LVPL is set to $\mathbf{I_{pmax}}$ (computed in the REEC block and indicated by the thick, bold, black line shown in Figure 38); on the other hand, if LVPLsw = 1, the value of LVPL is computed by using the nonlinear map shown above.

Unlike using the map for the scaled voltage presented previously, using the LVPL map may or may not affect the outcome of the commanded output power $\mathbf{P_{ord}}$; instead, this map is applicable only to the commanded current output, $\mathbf{I_{pcmd}}$. For example, under normal voltage (V_t = 1.0 p.u), I_{pcmd} = 0.2 p.u. If the voltage suddenly drops to 0.6 p.u., indicated by Point A on the map, the computed LVPL = 0.48 p.u.; thus, it does not affect the $\mathbf{I_{pcmd}}$ (i.e., at V_t = 0.6 p.u.) the $\mathbf{I_{pcmd}}$ is

not limited, and it is the same as the original value (I_{pcmd} = 0.2 p.u., indicated by Point A'). On the other hand, if the original I_{pcmd} = 0.8 p.u. (at V_t = 1.0 p.u., as indicated by Point B) and the voltage suddenly drops to V_t = 0.6 p.u., the commanded $\mathbf{I_{pcmd}}$ must be limited to I_{p_LVPL} = 0.48 p.u., as indicated by Point B' in the map. Note that within the normal voltage range, the current is limited to $\mathbf{I_{pmax}}$. ($\mathbf{I_{pmax}}$ is set to 1.2 p.u. in this particular map for 0.9 p.u. < V_t < 1.1 p.u.)

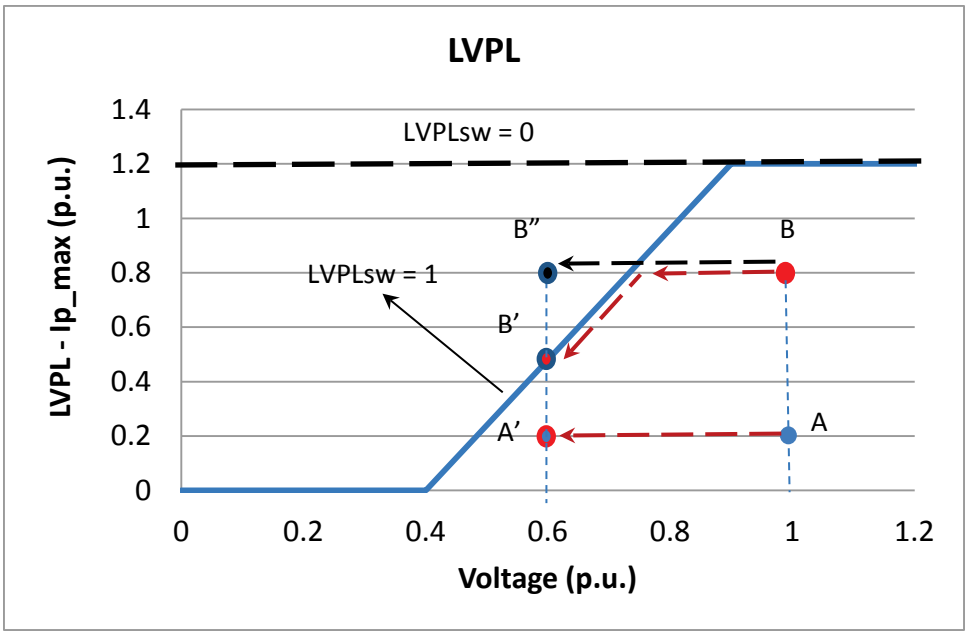


Figure 38. LVPL calculation to set the upper limit of I_{pcmd} during a low-voltage event

If LVPLsw = 0, the value of LVPL is set to $\mathbf{I_{pmax}}$. If the original I_{pcmd} = 0.8 p.u. (at V_t = 1.0 p.u., as indicated by Point B) and the voltage suddenly drops to V_t = 0.6 p.u.; the commanded $\mathbf{I_{pcmd}}$ will stay the same as the upper limit of the I_{p_LVPL} = 1.2 p.u. Thus, the operating point will move from Point B at V_t = 1.0 p.u. to the new operating point at V_t = 0.6 p.u., then to a new operating point as indicated by Point B" in the map.

3.2.1.2.3 Revised Commanded Power P_{ord} in the Low-Voltage Region

The revised commanded power $\mathbf{P_{ord}}$, computed based on the output of the $\mathbf{V_t}$ scaler and LVPL, can be different for different power levels and different settings of the **LVPLsw** logic switch.

3.2.1.2.3.1 Example 1

Normal condition P_{ord_orig} = 0.8 p.u.; V_t = 1.0 p.u.; and I_{pcmd} = *0.8 p.u*
LVPLsw = 1. The voltage drops to V_t = 0.6 p.u., $P_{ord\_new} = V_{t\_scaled}$ x $I_{pcmd\_limited}$ = 0.4 x 0.48 = 0.192 p.u., and the new $I_{pcmd} = I_{pord}$ = *0.192/0.6 = 0.32 p.u.*
LVPLsw = 0. The voltage drops to V_t = 0.6 p.u., $P_{ord\_new} = V_{t\_scaled}$ x $I_{pcmd\_limited}$ = 0.4 x 0.8 = 0.32 p.u., and the new $I_{pcmd} = I_{pord}$ = *0.32/0.6 = 0.533 p.u.*

3.2.1.2.3.2 Example 2

Normal condition P_{ord_orig} = 0.2 p.u.; V_t = 1.0 p.u.; and I_{pcmd} = *0.2 p.u*
LVPLsw = 1. The voltage drops to V_t = 0.6 p.u., $P_{ord\_new} = V_{t\_scaled}$ x $I_{pcmd\_limited}$ = 0.4 x 0.2 = 0.08 p.u., and the new $I_{pcmd} = I_{pord}$ = *0.08/0.6 = 0.133 p.u.*

LVPLsw = 0. The voltage drops to V_t = 0.6 p.u., $P_{ord\_new} = V_{t\_scaled}$ x $I_{pcmd\_limited}$ = 0.4 x 0.2 = 0.08 p.u., and the new $I_{pcmd} = I_{pord} = 0.08/0.6 = 0.133$ *p.u.*

Thus, the impact of the controller on the outcome of the commanded active power component is significant for medium to rated power when the **LVPLsw** is activated. However, when the active power command is low, it makes no difference whether the **LVPLsw** is activated or not.

3.2.2 REEC

The REEC is designed to control the real and reactive power (under normal and transient conditions). The REEC uses per-unit quantities and the generator base (PV inverter base; e.g., MBASE = 1.5 MVA) instead of a system base or PV power plant base (e.g., SBASE = 60 MVA). However, if a single-generator representation is used, the REPG uses MBASE = SBASE.

3.2.2.1 Control Implementation of Reactive Power and Voltage Control

The reactive power control block shown in Figure 39 illustrates the control mechanism of the reactive power control. Two stages are considered. This controller controls the reactive power to match the reactive power command, $\mathbf{Q_{in}}$. The $\mathbf{Q_{in}}$ is the input to the PI controller to regulate the reactive power or voltage, as shown in Figure 40 (enclosed in the solid black line). For now, ignore the blocks *NoFreeze* and *Freeze* and assume that these blocks are shorted.

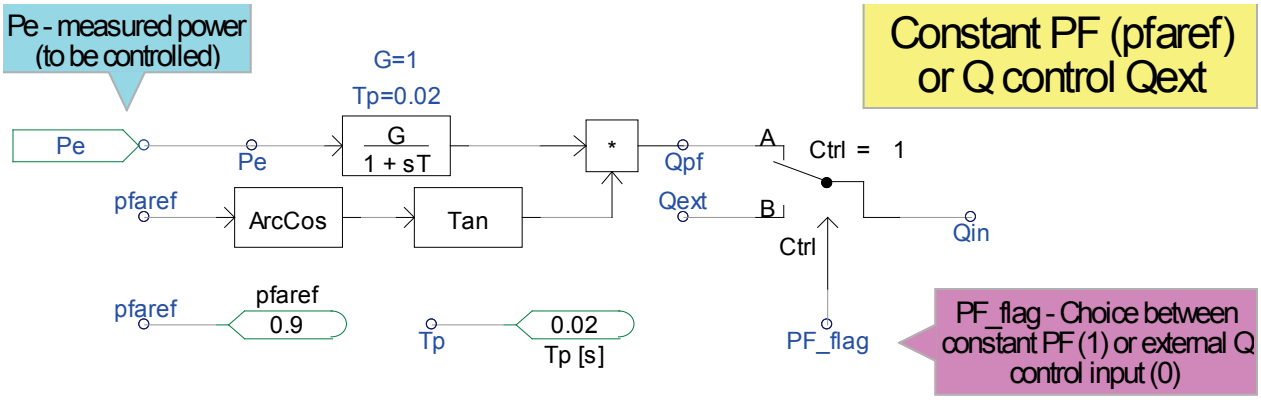


Figure 39. Block diagram illustrating the computation of the reactive power input command Q_{in}

3.2.2.1.1 Logical Switch PF_flag

If the controller is set to control the reactive power output of the power converter (Vflag = 1; see the description of Vflag below), two options are available to control the reactive power output.

- PF_flag = 1 sets the reactive power input command to follow $\boldsymbol{Q_{pf}}$ computed based on a constant power factor *pfaref*. The reactive power is commanded to be proportional to the actual real power Pe output; thus, it varies with the actual output power Pe as the output changes, except when the pfref = 1; however, in this case, the reactive power is commanded to be zero at all times. The $\boldsymbol{Q_{pf}}$ calculation can be shown as

$$Q_{pf} = Pe\ \tan(\cos^{-1}(pfaref))$$

- PF_flag = 0 sets the reactive power input command to follow the external reactive power command Q_{ext}. This input can be driven by supervisory control within the supervisory control domain (i.e., the REPC block diagram).

3.2.2.1.2 Logical Switch Vflag

The logical switch Vflag (shown in Figure 40) functions to control the reactive power output of the power converter. This block is inside the rectangle marked by the dashed red line. The input to this block is the output of the first block, and it may take two branches or directions, depending on the Vflag set. Focus on the circuit enclosed in the rectangle marked by the thin red line.

- Vflag = 1. The logical switch is set to A, then the reactive power control is chosen. The reactive power output will be controlled to match the reference Qin.
- Vflag = 0. The logical switch is set to B, then the voltage control is chosen. Note that the limiter placed before the $\mathbf{V_{star}}$ will limit the value of $\mathbf{V_{star}}$ (thus, the $\mathbf{V_{ref1}}$) within the acceptable voltage level ($V_{min} < V_{star} < V_{max}$). The terminal voltage $\mathbf{V_t}$ will be controlled to match the reference voltage $\mathbf{V_{ref1}}$.

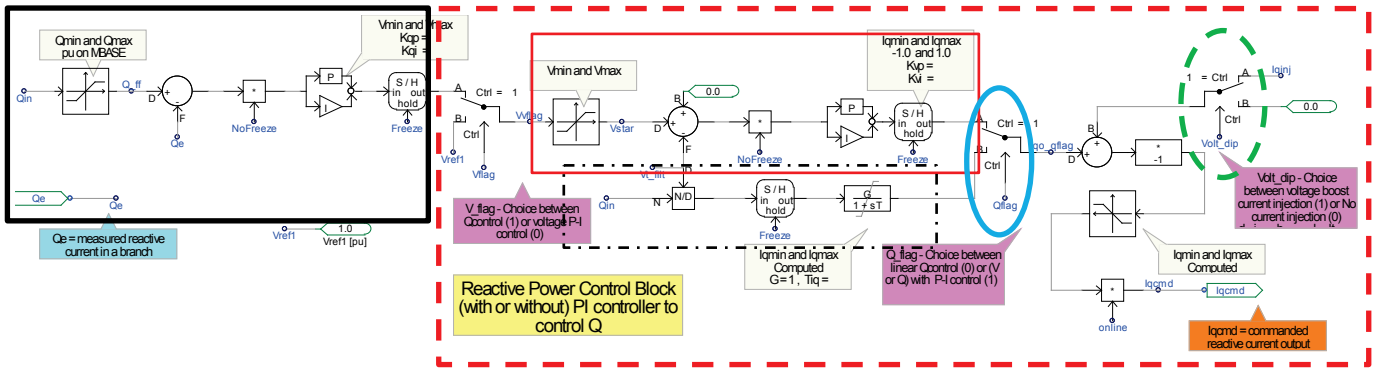


Figure 40. Reactive power and voltage control

3.2.2.1.3 Logical Switch Qflag

The output from the block enclosed in the red rectangle shown in Figure 40 will be the input A to the next logical switch (shown in the light blue ellipse) and to the next stage to calculate the commanded reactive current $\mathbf{I_{qcmd}}$. The logical switch is activated by the Qflag. The logical switch Qflag functions to determine if the reactive power output will be controlled via the two PI controllers (within the rectangles marked by the solid black line and the solid red line) or via the linear path (within the rectangle marked by the black dashes and dots).

- Qflag = 1 and Vflag = 1. The reactive power is accomplished via the PI controller inside the rectangle marked by the solid black line and the PI controller inside the rectangle marked by the dashed red line (two PI controllers in series).
- Qflag = 1 and Vflag = 0. The voltage is controlled by the PI controller shown inside the rectangle marked by the dashed red line (a single PI controller).

- Qflag = 0. The reactive power is controlled by a feed-forward linear loop without the PI controller (see the rectangle marked by the black dashes and dots). This loop will allow the reactive power to be controlled externally—for example, by supervisory control via the variable $\mathbf{Q_{ext}}$ to accomplish plant-level reactive control by paralleling the response of all the PV inverters within the PV plant (see the REPC block diagram).

3.2.2.1.4 Identifying Abnormal Voltage Range

Another logical switch is the one encircled within the dashed green ellipse shown in Figure 40. This logical switch enables the injection of additional reactive current, $\mathbf{I_{qinj}}$, during abnormal voltage (either in the overvoltage condition when the voltage $V_t > V_{up}$ or in the undervoltage condition when the voltage $V_t < V_{dip}$.

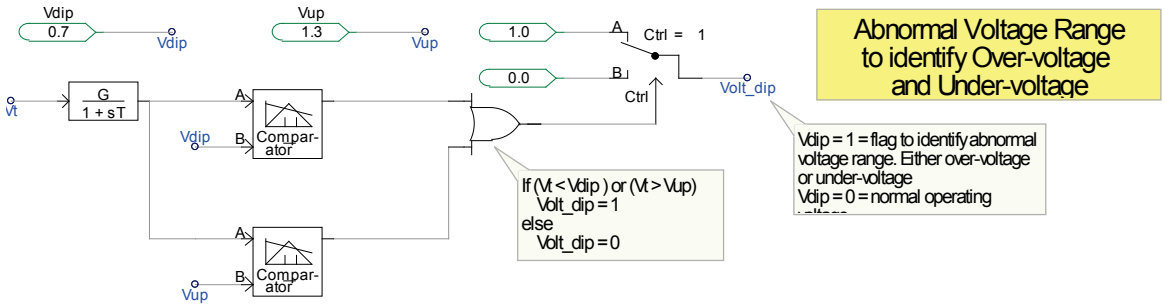


Figure 41. Identifying abnormal voltage to set Volt_dip

Figure 41 shows the logical switch Volt_dip. This logical switch will be operated based on the detection of the terminal voltage, $\mathbf{V_t}$, as shown in the diagram.

- Volt_dip = 0 is a normal condition, and the injection current $I_{qinj} = 0$.
- Volt_dip = 1 is an abnormal condition, and the injection current is used based on the droop characteristic.

The output commanded reactive current, $\mathbf{I_{qcmd}}$, is limited by its maximum, $\mathbf{I_{qmax}}$, and its minimum, $\mathbf{I_{qmin}}$. Calculating $\mathbf{I_{qmax}}$ and $\mathbf{I_{qmin}}$ will be shown in a later section.

3.2.2.1.5 Additional Reactive Current Injection, $\mathbf{I_{qinj}}$

The additional reactive current injection is computed based on the size of the voltage deviation of the terminal voltage, $\mathbf{V_t}$, from the reference voltage, $\mathbf{V_{ref0}}$.

Calculating an additional reactive current injection is done with the linear model shown in Figure 42. This controller block includes the deadband db1 and db2 to disable the control from injecting the additional reactive current, $\mathbf{I_{qinj}}$, when the voltage is within the normal range. In most cases, the reference voltage is assumed to be $V_{ref0} = 1.0$ p.u., and the normal voltage range 0.9 p.u. $< V_t < 1.1$ p.u.; thus, the deadbands db1 = db2 = 0.1 p.u. The constant value $\mathbf{K_{qv}}$ is the slope affecting the aggressiveness of the current injection, $\mathbf{I_{qinj}}$, to correct the voltage deviation. Note that the impact of the controller is dependent upon the stiffness of the grid, the availability of current-carrying capability of the power converter to pass this additional current, and the control setting of the PQflag. However, db_1, db_2, K_{qv}, and V_{ref0} can be adapted to the new values to follow specific regional and/or local rules and regulations.

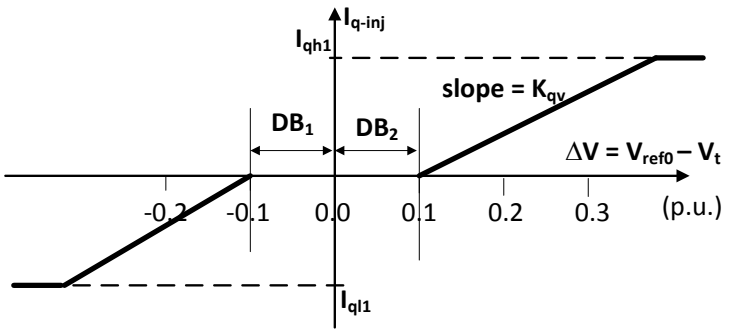


Figure 42. Diagram illustrating an additional reactive current injection during an abnormal voltage event (Volt_dip = 1)

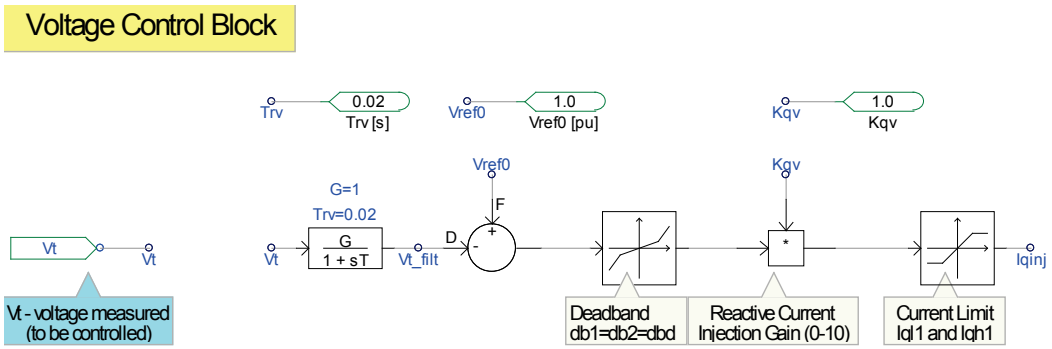


Figure 43. Block diagram illustrating a method to compute an additional reactive current injection during an abnormal voltage event (Volt_dip = 1)

Figure 43 above shows the control block diagram implementation of the additional current injection based on the voltage condition.

3.2.2.2 Real Power Control

Because the relationship of the reactive power to the terminal voltage is very tight, either the reactive power control or the voltage control is generally chosen. The reference real current component, $\mathbf{I_{pcmd}}$, can be computed by dividing the reference power, $\mathbf{P_{ref}}$, by the terminal voltage.

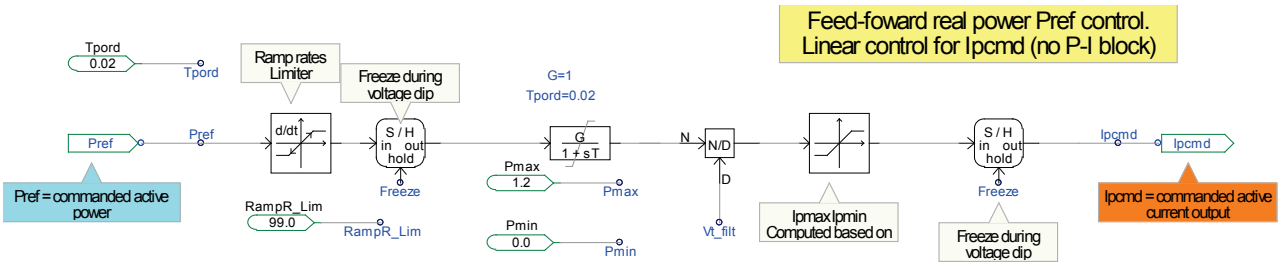


Figure 44. Block diagram illustrating a method to compute the real current component, I_{pcmd}

The block diagram shown in Figure 44 illustrates the following calculation.

$$I_{pcmd} = \frac{P_{ref}}{V_t}$$

The current limiter is used to limit the $\mathbf{I_{pcmd}}$ to the allowable $\mathbf{I_{pmax}}$ based on the setting of the PQflag (P-priority or Q-priority).

3.2.2.3 Calculating the Maximum and Minimum Current of I_{pcmd} and I_{qcmd}

To prevent the power switches (IGBTs and diodes) from conducting current higher than the current-carrying capability, the control block diagram shown in Figure 45 can be used to implement overcurrent protection.

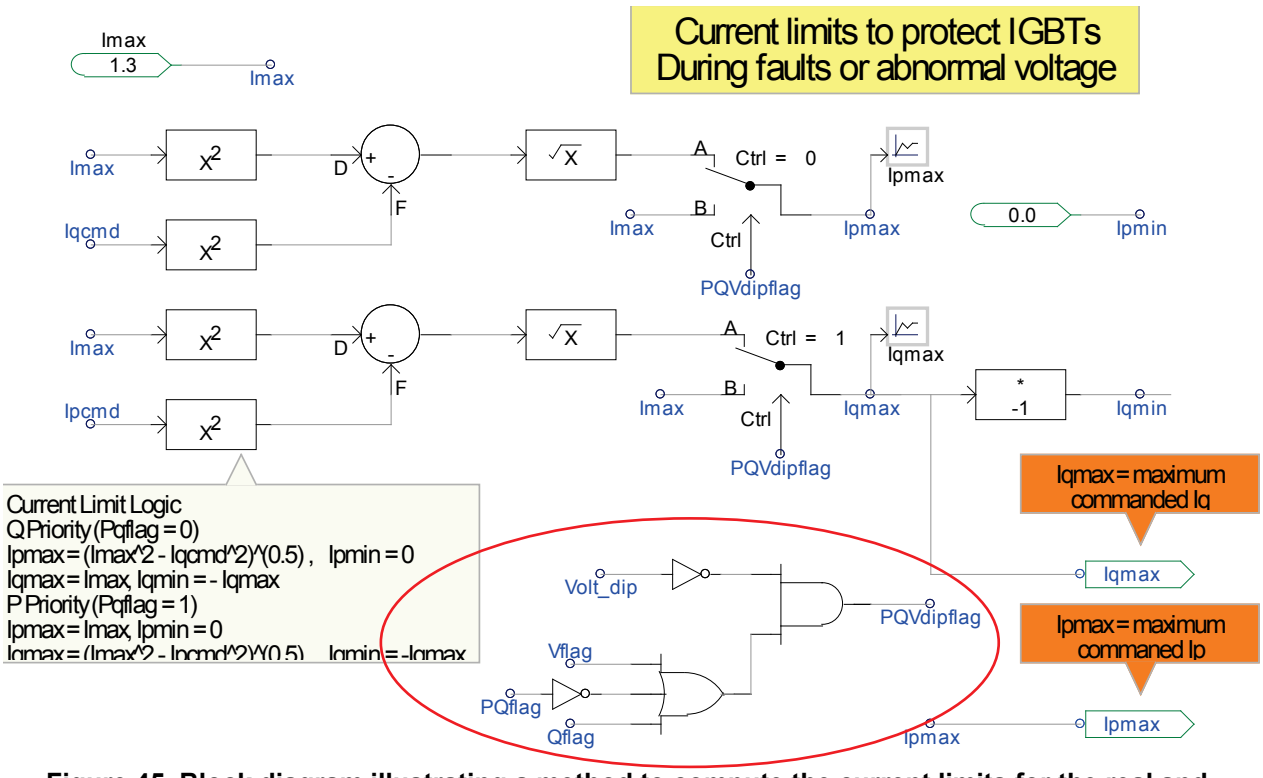


Figure 45. Block diagram illustrating a method to compute the current limits for the real and reactive current components

Two type of priorities can be set through the PQflag.

- PQflag = 1 is also known as P-priority. The controller's priority is to maximize the range of the real current component, $\mathbf{I_{pmax}}$, and use the remaining current capability for the reactive current component, $\mathbf{I_{qcmd}}$.

$$I_{pmax} = I_{max} \qquad I_{pmin} = 0$$

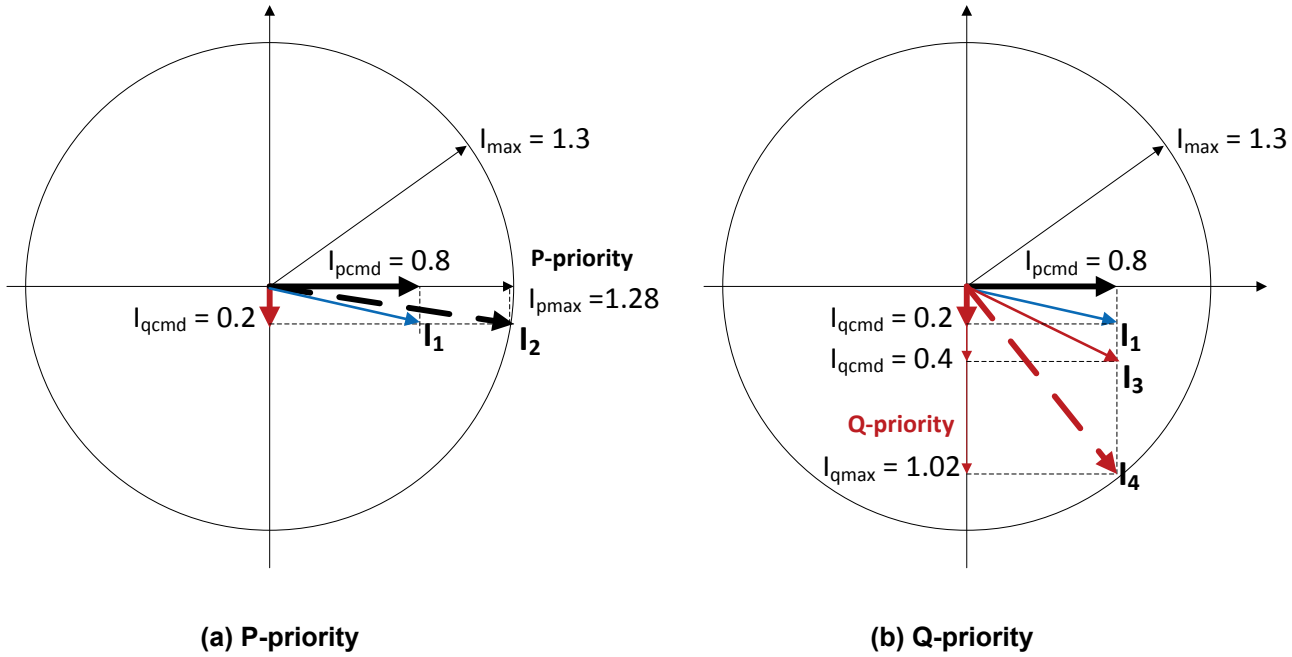
$$I_{qmax} = \sqrt{I_{max}^2 - I_{pcmd}^2} \qquad I_{qmin} = -I_{qmax}$$

- PQflag = 0 is also known as Q-priority. The controller's priority is to maximize the range of the reactive current component, $\mathbf{I_{qmax}}$, and use the remaining current capability for the real current component, $\mathbf{I_{pcmd}}$.

$$I_{pmax} = \sqrt{I_{max}^2 - I_{qcmd}^2} \qquad I_{pmin} = 0$$

$$I_{qmax} = I_{max} \qquad I_{qmin} = -I_{max}$$

Figure 46 illustrates the operation in P-priority and Q-priority. During a normal condition, the terminal voltage is assumed to be V_t = 1.0 p.u., and the maximum current allowed is I_{max} = 1.3 p.u. We assume initially that the output real power P = 0.8 p.u. I_{pcmd} = 0.8 p.u., and the reactive power Q = 0.2 p.u., I_{qcmd} = 0.2 p.u.; thus, the initial current is shown as the phasor $\mathbf{I_1}$.



(a) P-priority **(b) Q-priority**

Figure 46. Phasor diagrams illustrating the P-priority and Q-priority

The operation of P-Priority and Q-Priority is triggered by the logic diagram shown inside the red ellipse. Unless stated differently for different projects, during normal operation the P-Priority is set to maximize the energy yield of the renewable energy resources; thus, P-Priority is enabled (PQflag = 1) during normal operation (when the logic Volt_dip = 0). Even during abnormal voltage (V_dip = 1), the P-Priority can be activated (PQflag = 1) under certain circumstances.

3.2.2.3.1 Operation in P-priority

The phasor diagram shown in Figure 46 (a) illustrates the operation when P-priority option is selected. When a disturbance in the transmission line occurs, the voltage drops to V_t = 0.5 p.u. Using the P-priority, we can compute the maximum I_{pmax} = sqrt ($1.3^2 - 0.2^2$) = 1.28 p.u. Because the operation is set to P-priority, the controller tries to maintain output power constant at P = 0.8 p.u.; however, this requires I_{pcmd} = 0.8/0.5 = 1.6 p.u., which is higher than the allowable I_{pmax} =

1.28 p.u. Thus, we have to settle to I_{pcmd} = 1.28 p.u., and I_{qcmd} = 0.2 p.u. is frozen and must stay the same as the value before the voltage drop, and the output current changes from $\mathbf{I_1}$ to $\mathbf{I_2}$.

3.2.2.3.2 Operation in Q-priority

The phasor diagram shown in Figure 46 (b) illustrates the operation when the Q-priority option is selected. When a disturbance in the transmission line occurs, the voltage drops to V_t = 0.5 p.u. Using the Q-priority, we can compute the maximum I_{qmax} = sqrt ($1.3^2 - 0.8^2$) = 1.02 p.u. Because the operation is set to Q-priority, the controller tries to maintain the output reactive power constant at Q = 0.2 p.u. Thus, the required I_{qcmd} = 0.2/0.5 = 0.4 p.u. This value is the maximum range of allowable I_{qmax} = 1.02 p.u. The phasor current $\mathbf{I_1}$ moves to $\mathbf{I_3}$. Note that the magnitude of the phasor I_3 = 0.89 p.u., which is less than the maximum current limit I_{max} = 1.3 p.u.

Next, consider the additional current injection, $\mathbf{I_{qinj}}$, to support the voltage during the voltage dips. In this case, assume that K_{qv} = 2.0 and V_{ref0} = 1.0 p.u. When the voltage, V_t, drops to V_t = 0.5 p.u. The additional injection current is $I_{qinj} = K_{qv} (V_{ref0} - V_t)$ = 2 (1 - 0.5) = 1.0 p.u.; thus, including the current injection, $\mathbf{I_{qinj}}$, the total I_{qcmd} = 0.4 + 1.0 = 1.4 p.u. However, the I_{qmax} = 1.02 p.u. In this case, we have to settle with I_{qcmd} = 1.02 p.u. and I_{pcmd} = 0.8, and the total current I_4 = sqrt ($1.02^2 - 0.8^2$) = 1.3 p.u.

3.2.2.4 Controlling the Freeze During Abnormal Voltage Conditions

It is common in a PV inverter to freeze the states that control the output of the reactive power. This is done during the transients, so that the impact of the short disturbance does not exaggerate the situation and make the power system unstable when the disturbance is removed the grid. In some applications, the output current is frozen until the disturbance is over; however, this will only limit the output current contribution to the fault. The implementation is shown in Figure 47.

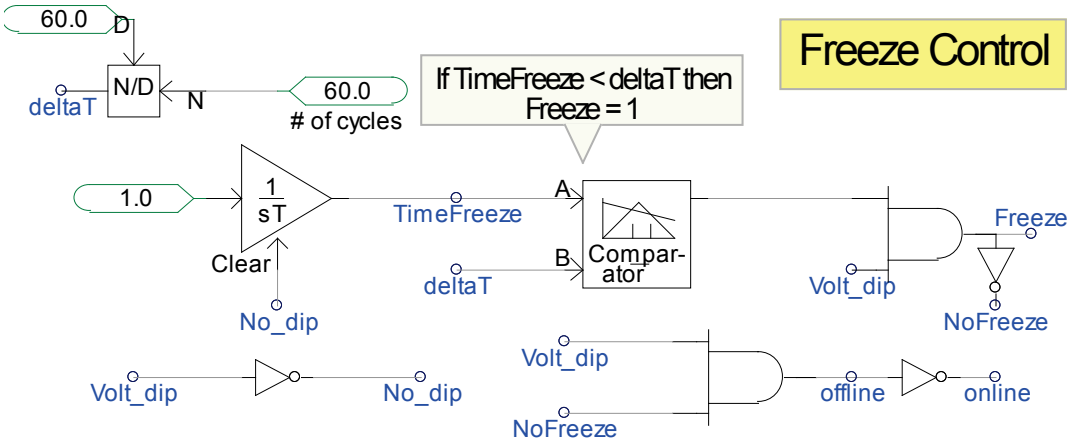


Figure 47. Block diagram illustrating a method to freeze the operating current during voltage dips

3.3 Plant Level

A PV plant consists of many large inverters connected in parallel by miles of AC cables (also known as a collector system). Supervisory control is implemented to the inverters within the power plant to achieve plant-level objectives. As the level of PV penetration increases, PV plants are required to provide low-voltage and high-voltage ride-through capabilities and different types of ancillary services (reactive power support, oscillation damping, inertial response, governor

control, spinning reserve, etc.) to the power system network. In large power system studies (such as WECC-wide studies), it is common to represent a wind power plant or PV plant as a single generator, as shown in Figure 48.

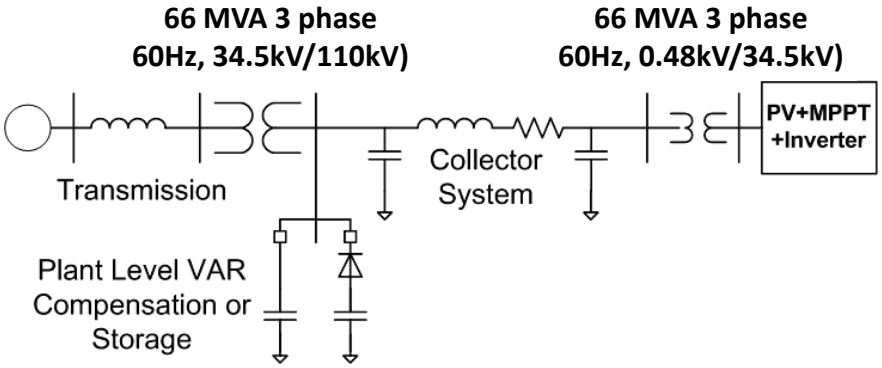


Figure 48. Single-line diagram illustrating a PV plant with a single generator

As shown, the output of a PV inverter is usually 208 V or 480 V. In the example presented above, the output voltage of the 165-kVA, three-phase PV inverter is 480 V; this is a parallel combination of many inverters representing a PV plant.

The transformers (480 V/34.5 kV) are connected to a substation transformer. Several of these nodes are connected in a daisy-chain fashion, which is then connected to the substation transformer (66 MVA, three-phase, 34.5 kV/110 kV). It is customary for the utility meters to be connected at the high side of the substation transformer to measure the revenue of a PV plant.

3.3.1 REPC

The REPC module shown in Figure 49 is a very useful way to implement the ancillary service capabilities of a renewable energy generator as required by the system operator. The REPC control block can be used to implement supervisory control to both the real and reactive power. Note the capability of the power converter to deliver the desired output and that the current-carrying capability of the power switches (IGBTs) takes precedence over the objective function specified in the REPC. For example, if the current/voltage limit of the IGBT has been reached, and the REPC objective function has not been accomplished, the final outcome will be determined by the IGBTs current/voltage limit.

Like REPG and REEC, the REPC uses per-unit quantities; however, in the REPC, the base quantity used is the system base (a PV power plant base) instead of the generator base (a PV inverter base).

3.3.1.1 Voltage Control at a Remote Bus

As shown in Figure 50, the remote bus is defined as the bus farther from the terminal voltage. The electrical distance from the terminal voltage is represented by the reactance $\mathbf{X_{br}}$, the current flowing through the branch is represented by $\mathbf{I_{branch}}$, and the reactive power flowing in the branch is represented by $\mathbf{Q_{branch}}$.

The regulated voltage is located in a remote bus from a monitored bus voltage $\mathbf{V_{reg}}$. Two types of voltage compensation can be activated in the REPC block diagram:

- VcompFlag = 1—The voltage to be controlled is measured from the Vreg, bus and it is compensated by using the computed voltage drop I X.
  A. Example 1—If you want to regulate $\mathbf{V_1}$ (high side of the transformer) and have access only to the voltage $\mathbf{V_t}$, then to control $\mathbf{V_1}$, the branch current $I_{branch} = I_{xfrmr}$ and $X_{br} = X_{xfrmr}$; voltage $V_{reg} = V_t$; and the voltage drop is computed from $\mathbf{I_{xfmr}}$ $\mathbf{X_{xfmr}}$.
  B. Example 2—If you want to regulate $\mathbf{V_2}$ and monitor only the voltage $\mathbf{V_1}$, then to control $\mathbf{V_2}$, the branch current $I_{branch} = I_{branch1}$ and $X_{br} = X_s$; the voltage $V_{reg} = V_1$; and voltage drop is computed from $\mathbf{I_{branch1}}$ $\mathbf{X_s}$.
- VcompFlag = 0—The voltage to be controlled is measured from the Vreg bus, and it is compensated by estimating the voltage drop by $\mathbf{K_c}$ $\mathbf{Q_{branch}}$.
  A. Example 1—If you want to regulate $\mathbf{V_3}$ and have access only to the voltage $\mathbf{V_2}$, then to control $\mathbf{V_3}$, the $Q_{branch} = Q_{branch1}$ and voltage $V_{reg} = V_2$, and the voltage drop is estimated by $\mathbf{K_{c1}}$ $\mathbf{Q_{branch1}}$.
  B. Example 2—If you want to regulate $\mathbf{V_1}$ and you have access only to the voltage $\mathbf{V_t}$, then to control $\mathbf{V_1}$, the $Q_{branch} = Q_{out}$ and voltage $V_{reg} = V_t$, and the voltage drop is estimated by $\mathbf{K_{cxfmr}}$ $\mathbf{Q_{out}}$.

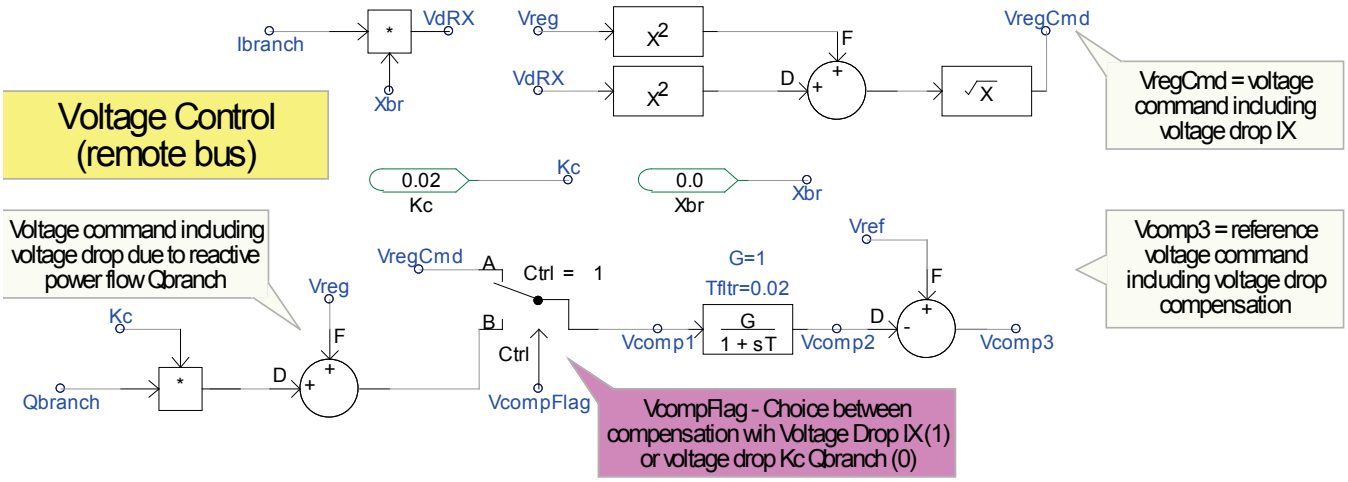


Figure 49. Control block diagram illustrating voltage regulation for a remote bus

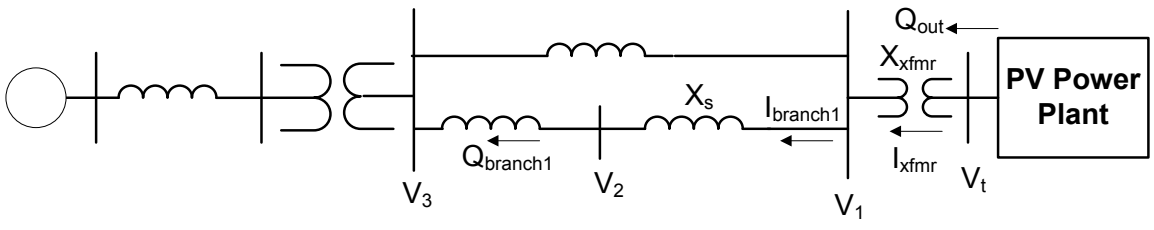


Figure 50. Single-line diagram illustrating a method to accomplish different remote voltage regulations

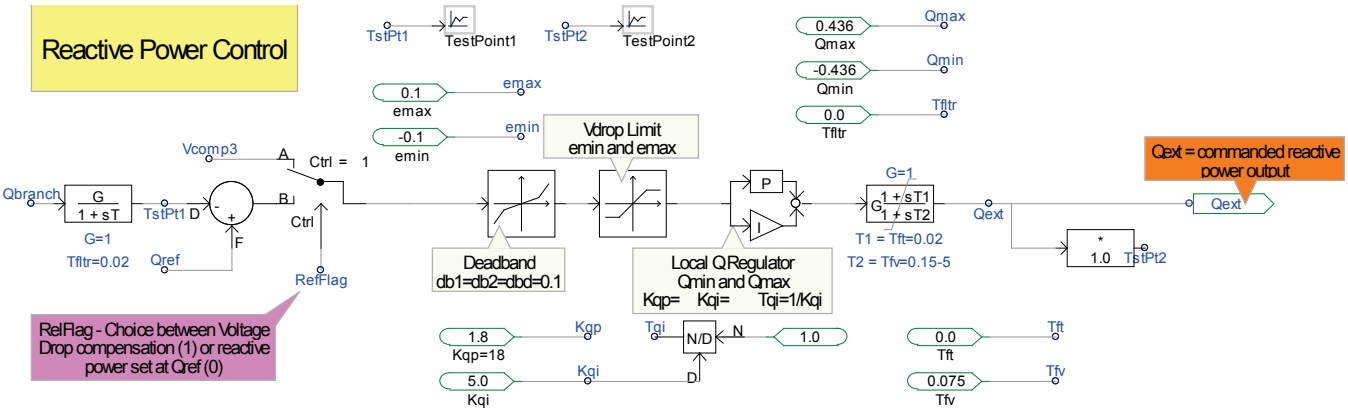


Figure 51. Control block diagram illustrating a method to regulate reactive power

3.3.1.2 Reactive Power Control

The reactive power control is illustrated by the control block diagram shown in Figure 51. In this control block diagram, there is a logical switch called **RefFlag** that must be set to make the following choices:

- RefFlag = 1—Configure the controller to regulate the voltage based on the measured voltage $\mathbf{V_{reg}}$.
- RefFlag = 0—Configure the controller to regulate the reactive power flow in a specified branch (for example, the $\mathbf{Q_{branch1}}$ in Branch 1 or Q_{out} measured at the output of bus $\mathbf{V_t}$) to follow the reference, $\mathbf{Q_{ref}}$. Caution must be taken when controlling a branch from a PV power plant when the output is split into multiple branches. For example, we can control the reactive power flow in a particular branch to follow a certain reference $Q_{branch} = Q_{branch1}$; however, the setup will let us control the reactive power flow only in a single branch, so if we control only the reactive power flow in Branch 1, we do not have any control over the power flow in Branch 2. Because the output of the power plant flows in both Branch 1 and Branch 2, the power plant may have reached its upper limit before $Q_{branch1} = Q_{ref}$ is reached.

The output of this controller is the $\mathbf{Q_{ext}}$, which is an input to the next block, REEC, and will be used to compute the reactive current component, $\mathbf{I_{qcmd}}$, that will generate the requested $\mathbf{Q_{ext}}$. Note that $\mathbf{Q_{ext}}$ is either the reference reactive power $\mathbf{Q_{ref}}$ (for RefFlag = 0) or the equivalent reactive power needed to regulate the voltage at a specified remote bus (for RefFlag = 1).

3.3.1.3 Real Power Control

The real power control is illustrated by the control block diagram shown in Figure 52. The reference power is set by the reference power Plant_Pref. The single-line diagram shown in Figure 53 is as an example of how to use reference power Plant_Pref. For example, if the output power of a PV power plant is to be controlled to follow the reference Plant_Pref, then we can set $P_{branch} = P_{out}$.

Caution must be taken when controlling a branch power flow from PV power plant when the output is split into multiple branches. For example, we can control the power flow in a particular branch to follow Plant_Pref by setting $P_{branch} = P_{branch23}$ or $P_{branch} = P_{branch1}$. However, the setup

will let us control the power flow only in a single branch; thus, if we control only the power flow in Branch 1, we do not have any control over the power flow in Branch 2. The power plant may have reached its upper limit before $P_{branch1}$ = Plant_Pref is reached.

This control block diagram shows a logical switch called **FreqFlag** that must be set to make the following choices:

- FregFlag =1—Configure the controller to regulate the real power flowing in the specified branch $\mathbf{P_{branch}}$ using the PI controller to include the reference Plant_Pref and the frequency response dP/dF. At this point, the only way to disable the frequency response dP/dF into the power command mix is to set the slope $D_{dn} = D_{up} = 0$.
- FreqFlag = 0—Configure the controller to regulate the reactive power flow in a specified branch $\mathbf{P_{branch}}$ to follow the reference real power command Plant_Pref using the feed-forward linear path (bypassing the PI controller) without the influence of frequency response.

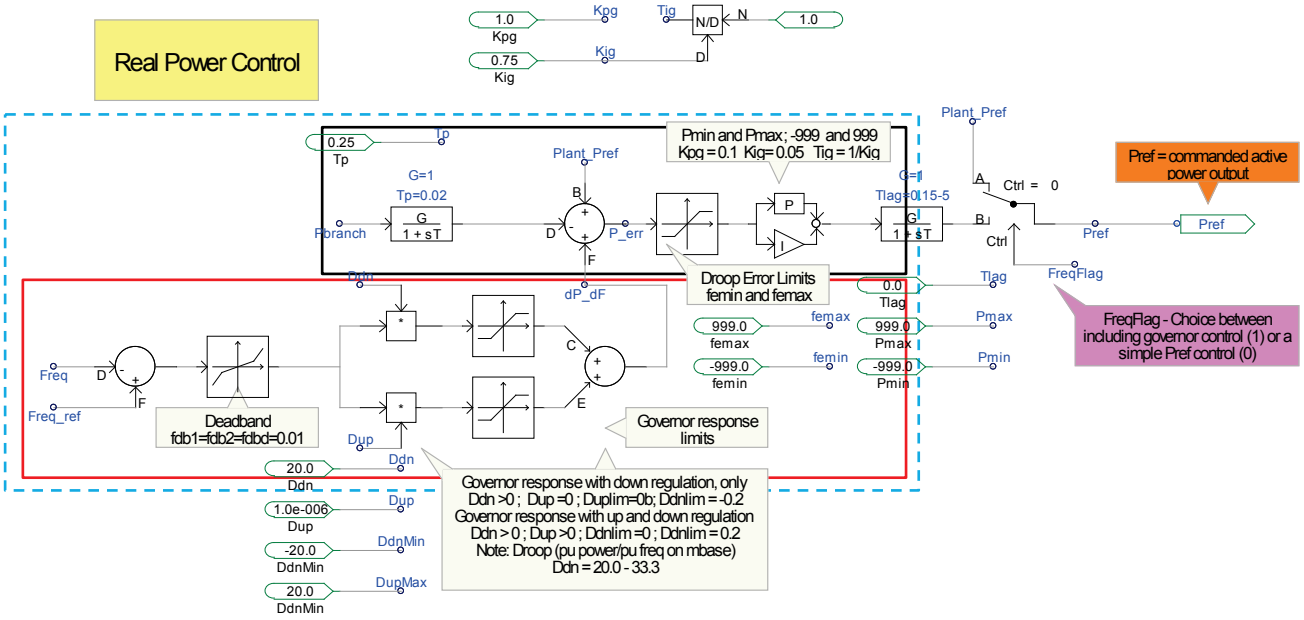


Figure 52. Control block diagram illustrating a method to regulate real power

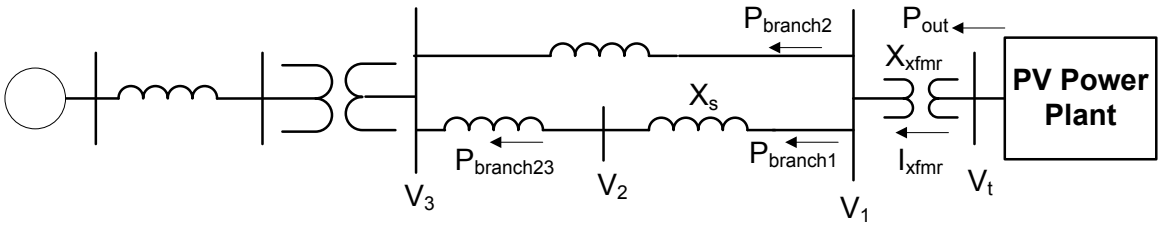


Figure 53. Single line diagram describing real power control in remote location

The output of this controller is the $\mathbf{P_{ref}}$, which will be used as an input to the next block, REEC, and to compute the real current component $\mathbf{I_{pcmd}}$ that will generate the requested **Plant_Pref**.

The real power control following the path with the PI loop lies within rectangle marked by the blue dashes. The diagram within the red rectangle is the frequency response control, and the diagram within the black rectangle is the total control of real power to match the real power flow within the branch to match the reference **Plant_Pref**.

3.3.1.4 Additional Real Power Boost to Respond to Frequency Changes

The additional real power control to support frequency regulation is illustrated by the control block diagram shown within the red rectangle in Figure 52. The reference frequency is set by **Freq_ref**. The measured frequency is the **Freq**. The error **ΔFreq** is passed through the deadband block, and the slope is controllable via the parameters $\mathbf{D_{dn}}$ and $\mathbf{D_{up}}$, and the output is limited by the limiter $\mathbf{D_{dn}Min}$ and $\mathbf{D_{up}Max}$. Figure 54 shows a graphical illustration of this concept. Note that the characteristics can be made nonsymmetrical to perform governor control and frequency response.

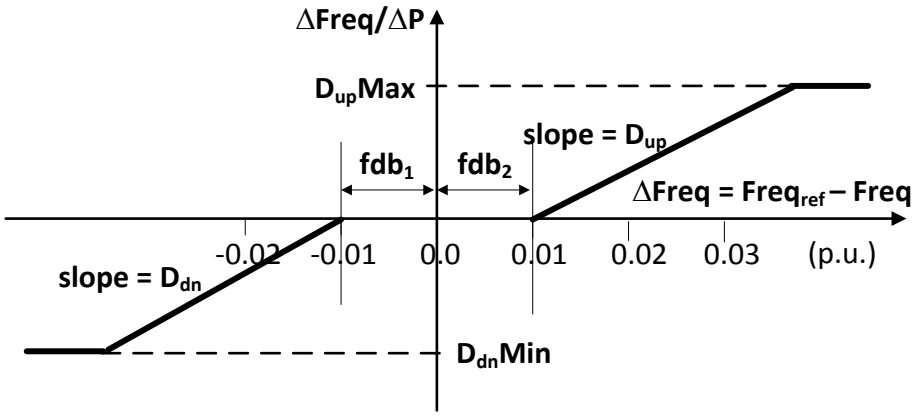


Figure 54. Graphical illustration of real power regulation during a frequency excursion

4 PV Dynamic Model Validation

Dynamic model validation is not an easy task to perform and includes many stages. Ideally, as much information as possible is needed. In a dynamic simulation, enough information may not be available to simulate an actual PV plant that we want to validate. In such a case, assumptions about the missing data have to be made; however, in some cases, the validation simply cannot be performed. On the other hand, having too much but inaccurate information may lead to a bad validation and an inaccurate representation of a PV inverter or PV plant.

A typical model validation will represent a PV plant as shown in Figure 55, in which a single PV inverter represents the total generation of an entire plant. The first step-up transformer connecting the PV inverter to the collector system is used to step up the voltage from low voltage to medium voltage (e.g., 480 V/34.5 kV). The collector system represents the lines or cables interconnecting the step-up transformer within the power plant to the substation transformer, where all the output of the PV inverters within the PV plant are stepped up to the transmission-level voltage (e.g., 34.5 kV/230 kV) to be transmitted over long distances. This collector system can be aggregated into a single impedance represented by $\mathbf{Z}_{\mathbf{collector}}$.

The recorded voltage measured at the point of interconnection is used to drive the simulation as the infinite voltage source at the point of interconnection. The simulation output of the real and reactive power as well as the output currents were compared to the measured data.

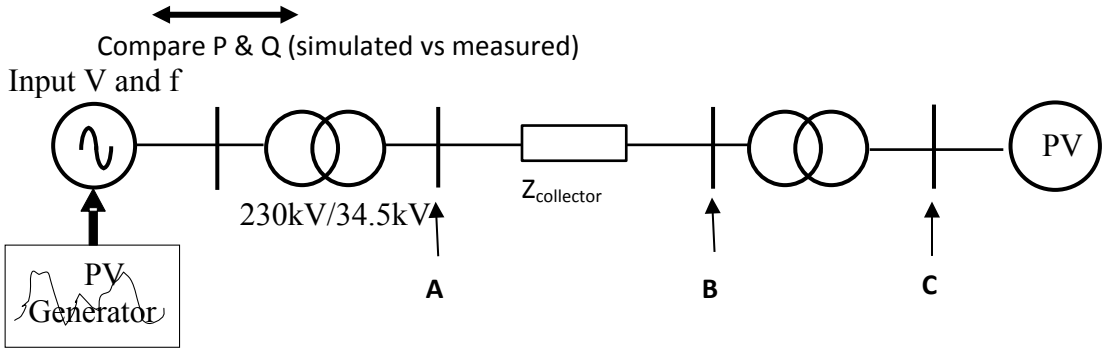


Figure 55. Single-line diagram illustrating the dynamic model validation

4.1 Three-Phase PV Plant Validation

4.1.1 Detailed Model Implementation

A detailed model of the circuit implementation is shown in Figure 56 below. To prepare for dynamic validation, the data measured at the point of interconnection is used as the input to the detailed model; these are usually three-phase voltages and currents. The real and reactive power output can be computed, or it can be obtained from the data recorder. Note that the real and reactive power from the calculation may contain high-frequency noise, whereas the output data obtained from the measurement is usually filtered. For the purpose of the validation, we use a moving average filter for the real and reactive power output computed from the measured three-phase voltages and currents.

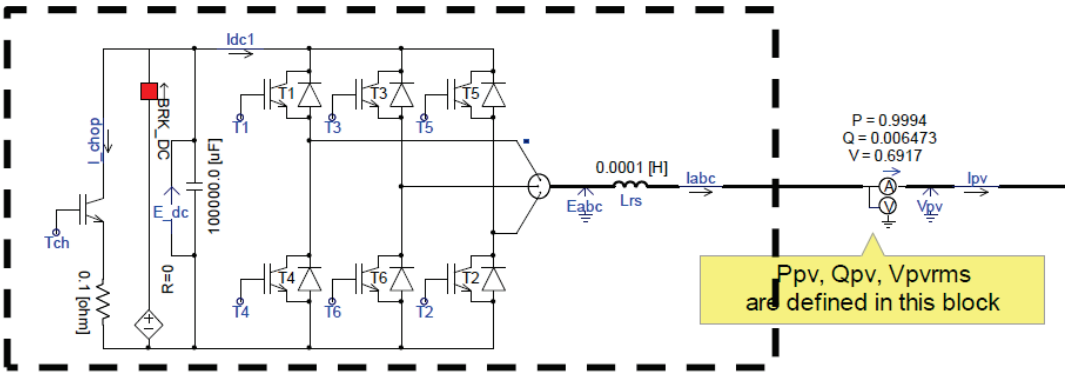


Figure 56. Circuit diagram illustrating the dynamic model validation for a detailed model

The initial condition (pre-fault) of the simulation is adjusted to match the pre-fault measured data. The measured values of the real and reactive power as shown in Figure 57 are used to adjust the commanded real and reactive power. The measured data is shown in blue, and the simulated results are shown in green. As shown, the simulation very closely follows the actual output measurement.

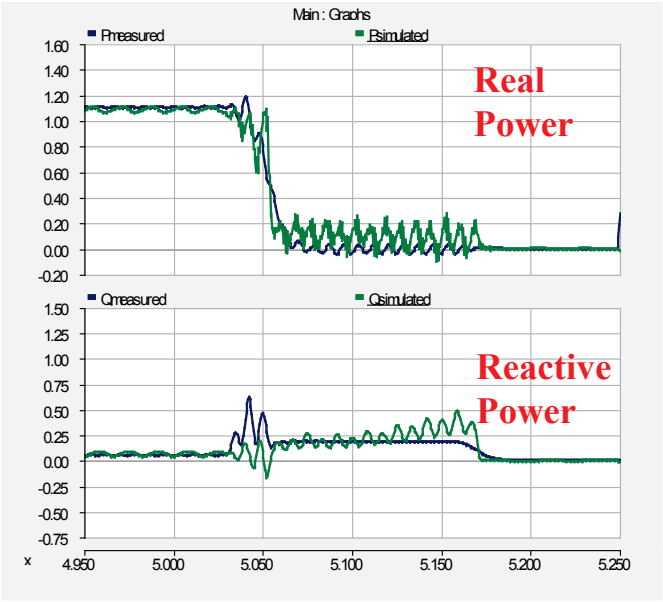


Figure 57. Real and reactive power output of the simulations

In a real set-up, ideally the solar irradiance should be the input; however, this information is seldom available, and—in addition to the transient model analysis, in which the duration of the observation is only a few seconds—this input is less important; thus, we assume that the solar irradiance is constant during the disturbance. The real and reactive power in the pre-fault condition is used to set the real and reactive power commands (reference real and reactive power). These reference values are considered to be constant for the duration of the fault. As shown in Figure 57, during the fault the result of the simulation indicates that the real and reactive power changes. That is a result of the control actions of the PV inverter, and it is not because of the reference values of the real and reactive power that are changing during the

disturbance. A comparison of the reference values to the measured values shows that the controller of the dynamic models functions properly, as indicated in Figure 57.

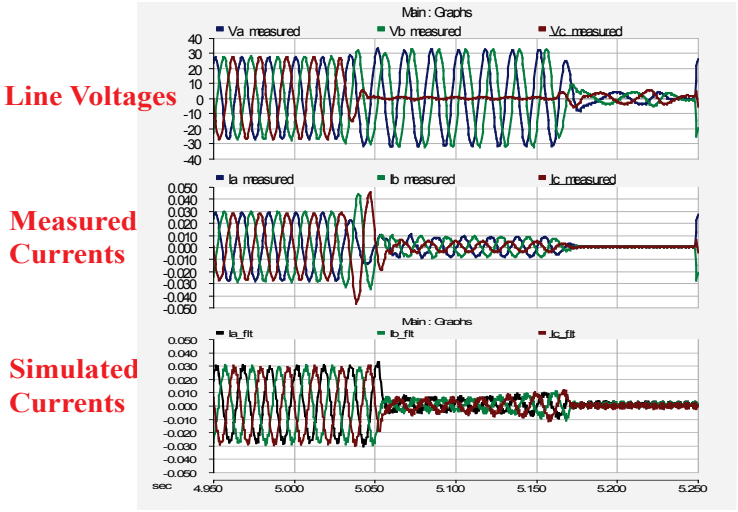


Figure 58. Voltage and current waveforms using a detailed model representation for (a) voltages measured, (b) currents measured, and (c) currents simulated

The voltage applied to drive the simulation is shown in the top row of Figure 58. The PV plant responded to this voltage, thus generating the current waveforms shown in the bottom row of Figure 58. A comparison of the measured current waveforms to the simulated waveforms indicates that the dynamic model and the controller represent the actual PV plant. Note that the output current, real power, and reactive power are determined by the voltage and the control parameter set for this particular PV plant or PV inverter. By comparing the output real and reactive power shown in Figure 57 to the output currents shown in Figure 58 (simulated versus measurement), we can conclude that the PV plant dynamic model very closely represents the actual plant.

4.1.2 Average Model Implementation

The average model of the circuit implementation is shown in Figure 59 below. The process to prepare for dynamic validation of the average model is the same as that described in the detailed model representation.

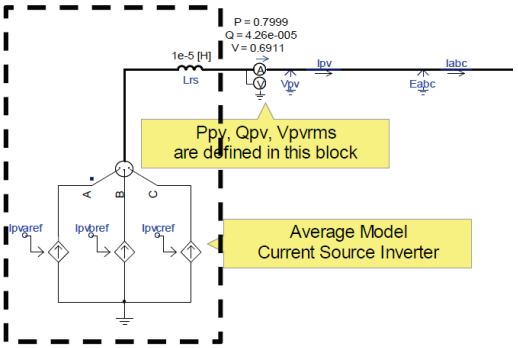
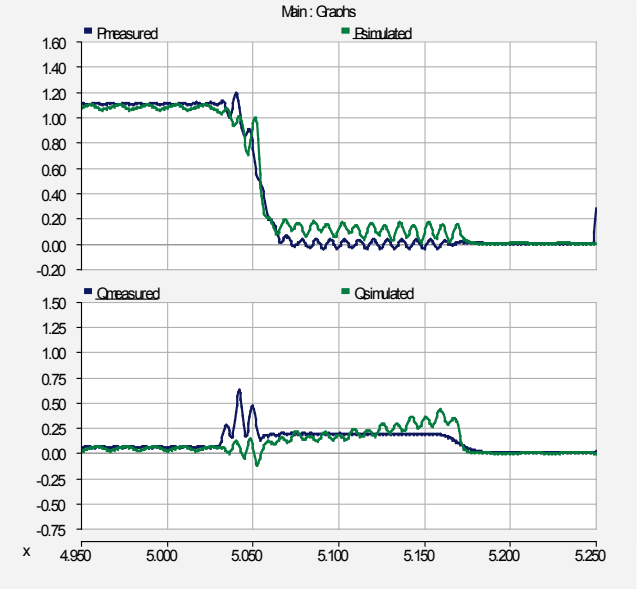
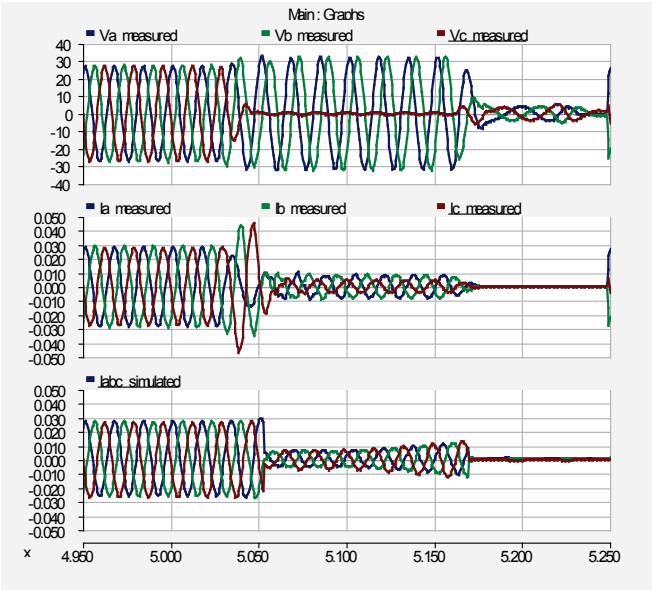


Figure 59. Circuit diagram illustrating the dynamic model validation of an average model



(a) Real and reactive power



(b) Three-phase voltages and currents

Figure 60. Comparison of the simulation output to the measured output for an average model

Figure 60 (a) shows the real power compared to the reactive power, and Figure 60 (b) shows the voltage and current waveforms measured at the point of interconnection. This is the voltage used to drive the simulation. A comparison of Figure 57 to Figure 60 (a) shows that there is almost no difference between the detailed model and the average model. Also, a comparison of Figure 58 to Figure 60 (b) shows that the current waveforms from the detailed model are very similar to the current waveforms from the average model. The only difference is the apparent harmonics shown in the output of the detailed model, but the fundamental components are very closely matched.

4.2 Single-Phase PV Plant Validation

In this section, a single-phase PV plant is validated against the measured data. This small-scale PV plant is illustrated in the circuit diagram presented in Figure 61.

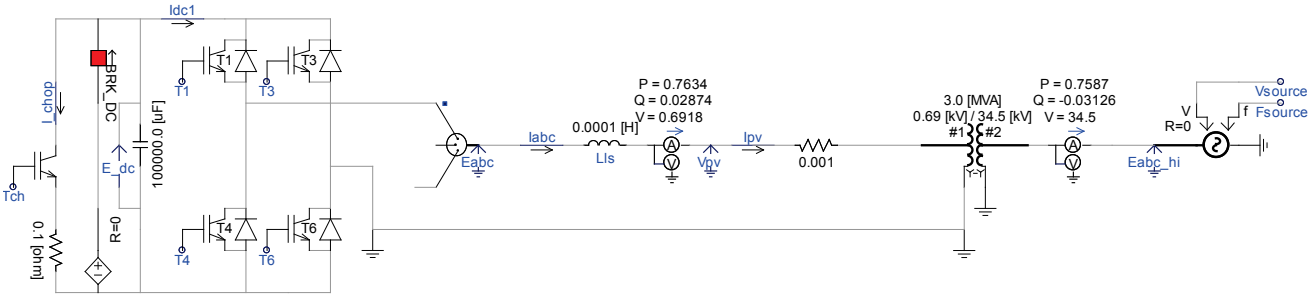
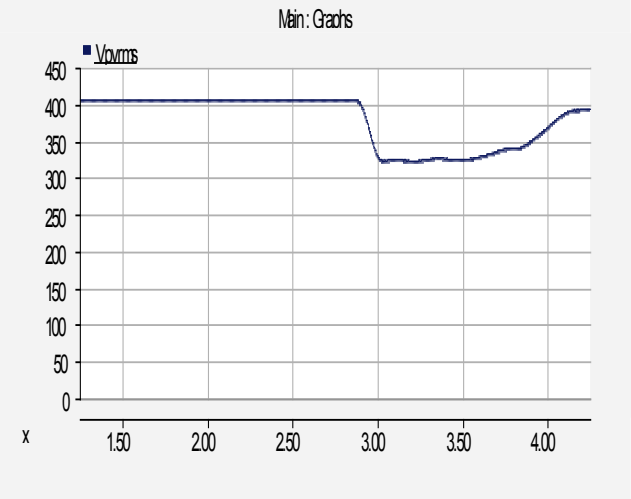
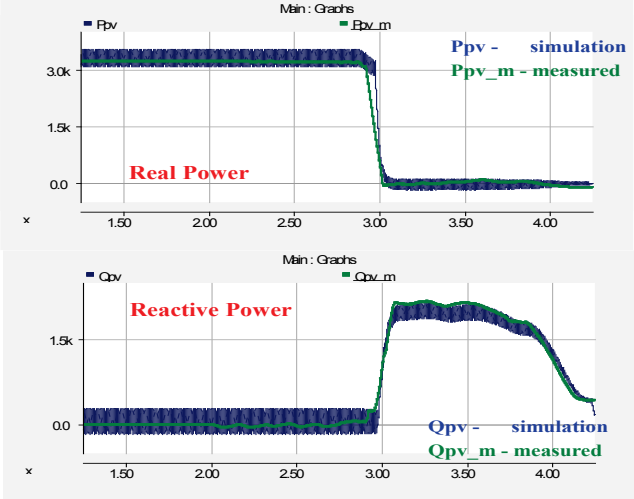


Figure 61. Diagram illustrating a single-phase PV plant circuit

Figure 62 (a) shows the voltage waveforms measured at the point of interconnection. This is the voltage used to drive the simulation. The voltage dip is caused by a fault occurring in the transmission far away from the PV plant.



(a) Voltage



(b) Real and reactive power

Figure 62. The voltage used to drive the simulation and the corresponding real and reactive power output

The real and reactive power output shown in Figure 62 (b) are the output of the simulation and the measured output. As mentioned previously, the measured data of the real power and the reactive power are filtered and the simulated output of the real and reactive power shows 120-Hz ripples, which is a typical characteristic of single-phase output power.

The output currents are shown in Figure 63. The simulation output current waveform is shown in Figure 63 (a), and the measured output current waveform is shown in Figure 63 (b). A comparison of the output current magnitude from the simulation result to the measured data is shown in Figure 63 (c).

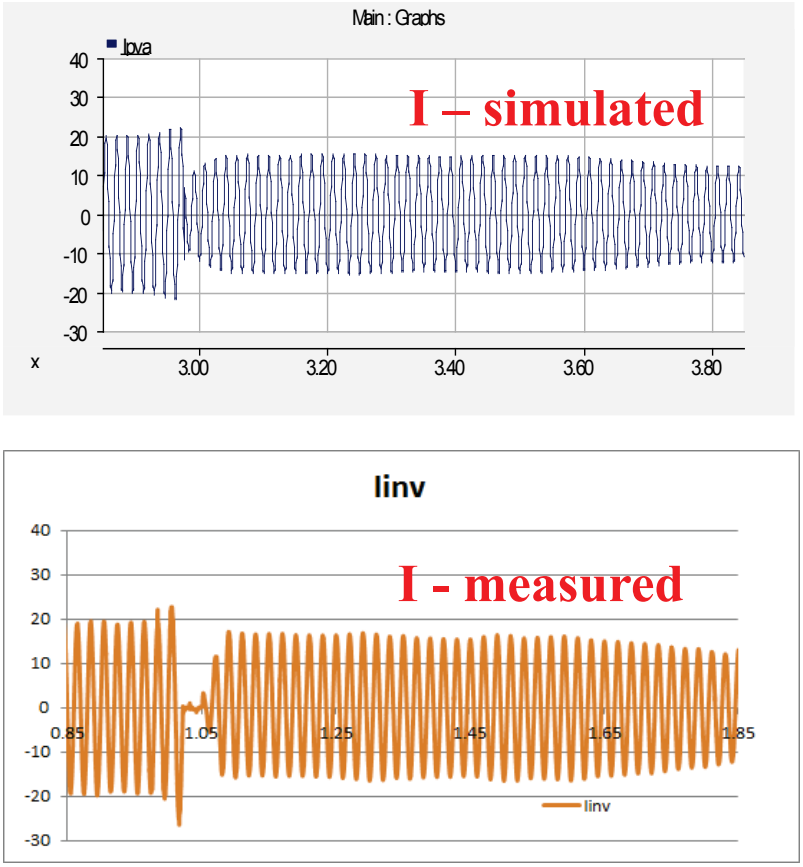


Figure 63. Output current waveforms and magnitude

5 Summary

We have developed PSCAD modules to simulate a (three-phase and single-phase) PV inverter at the equipment level and at the network level. Detailed and average dynamic models have been completed. The detailed model can be used to simulate the impact of a grid disturbance on the power semiconductor switches and other power converter components; similarly, it can be used to simulate failures in the power semiconductor and the impact on the output currents, real power, and reactive power delivered to the grid. The average model can be used to simulate power system dynamics for various control algorithms implemented on the power converter.

The dynamic models were developed in the PSCAD platform and designed to simulate both normal and unbalanced conditions. This capability is not available in the commonly used positive-sequence power system planning software.

The advantage of the average model compared to the detailed model is that the simulation integration time step can be shortened significantly, thus shortening the simulation time. On the other hand, in the average model we lose the detail of the power converter model and are unable to simulate the malfunction of the power semiconductors or different sizes of power converter components.

We also developed the WECC-REMTF controllers REEC, REGC, and REPC. With minor modifications, these controllers can be set to perform fault ride-through capability and ancillary service functions, such as frequency and inertial response, governor droop control, reserve, and others.

Finally, we performed dynamic model validations using recorded data from two PV plants. In both cases, the results of the simulations very closely followed the measured data; thus, this is a good indication that the simulated dynamic models represent real PV plants. Because of a confidentiality agreement, we are unable to disclose the location, size, and detail of the PV plants.

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Appendix: Control Blocks—REPC, REEC, and REGC

The information on the control blocks presented here is as described in the Western Electricity Coordinating Council's Renewable Energy Modeling Task Force report on *Generic Solar Photovoltaic System Dynamic Simulation Model Specification* (WECC 2012).

REPC

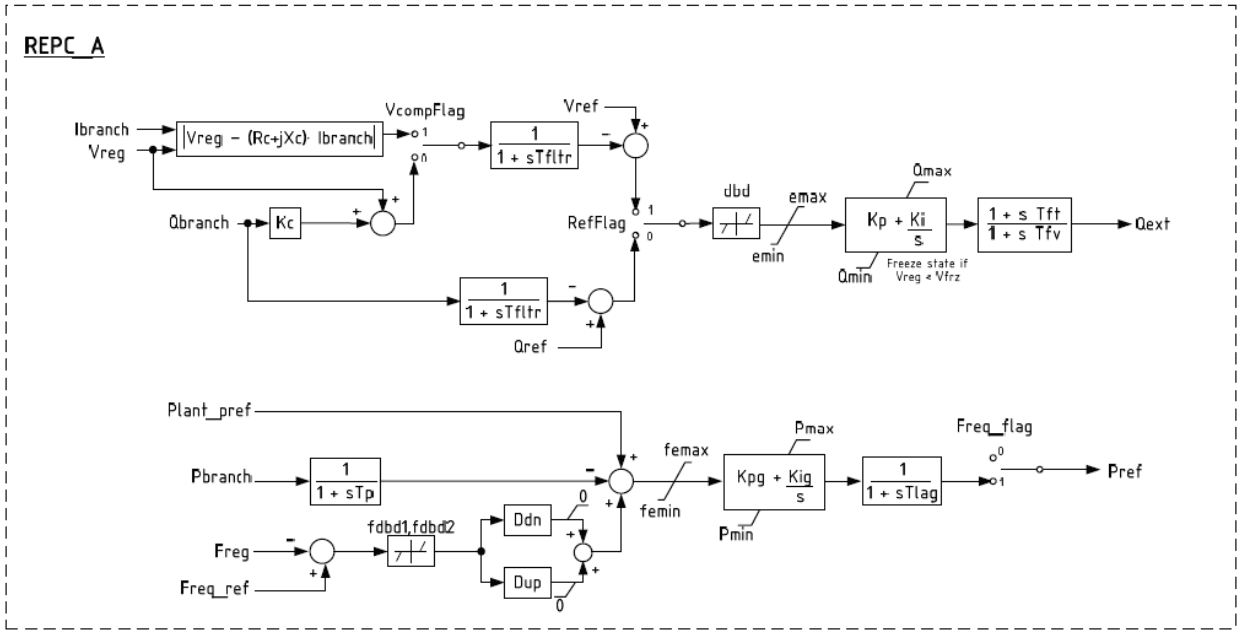

Table A-1. Parameters for the REPC

Parameter	Description	Typical Range of Values	Units
MBASE	Model MVA base	N/A	MVA
Tfltr	Voltage or reactive power measurement filter time constant	0.01 – 0.05	s
Kp	Proportional gain	N/A	pu/pu
Ki	Integral gain	N/A	pu/pu
Tft	Lead time constant	N/A	s
Tfv	Lag time constant	N/A	s
RefFlag	1 – for voltage control or 0 – for reactive power control	N/A	N/A
Vfrz	Voltage below which plant control integrator state (s2) is frozen	0 – 0.7	pu
Rc	Line drop compensation resistance	0	Pu
Xc	Current compensation constant (to emulate droop or line drop compensation)	-0.05 – 0.05	pu
Kc	Gain on reactive current compensation	N/A	pu
VcompFlag	Selection of droop (0) or line drop compensation (1)	N/A	N/A
emax	Maximum error limit		pu
emax	Minimum error limit		pu
dbd	Deadband in control	0	pu
Qmax	Maximum Q control output		pu
Qmin	Minimum Q control output		pu
Kpg	Proportional gain for power control		pu/pu
Kig	Integral gain for power control		pu/pu
Tp	Lag time constant on Pgen measurement		s
fdbd1	Deadband downside		pu
fdbd2	Deadband upside		pu
femax	Maximum error limit		pu
femin	Minimum error limit		pu
Pmax	Maximum Power		pu
Pmin	Minimum Power		pu
Tlag	Lag time constant on Pref feedback		s
Ddn	Downside droop	20	pu/pu
Dup	Upside droop	0	pu/pu
Pgen_ref	Initial power reference	From powerflow	pu
Freq_ref	Frequency reference	1.0	pu

Parameter	Description	Typical Range of Values	Units
vbus	The bus number in powerflow from which Vreg, Freq is picked up (i.e. the voltage being regulated and frequency being controlled; it can be the terminal of the aggregated WTG model or the point of interconnection)	N/A	N/A
branch	The branch (actual definition depends on software program) from which I_{branch}, Q_{branch} and P_{branch} is being measured.	N/A	N/A
Freq_flag	Flag to turn on (1) or off (0) the active power control loop within the plant controller	0	N/A

Note: Vref and Qref are initialized by the model based on Vreg and Qgen in the initial powerflow solution, and Qext is initialized based on the initialization of the initial Q reference from the down-stream aggregated WTG model.

REGC

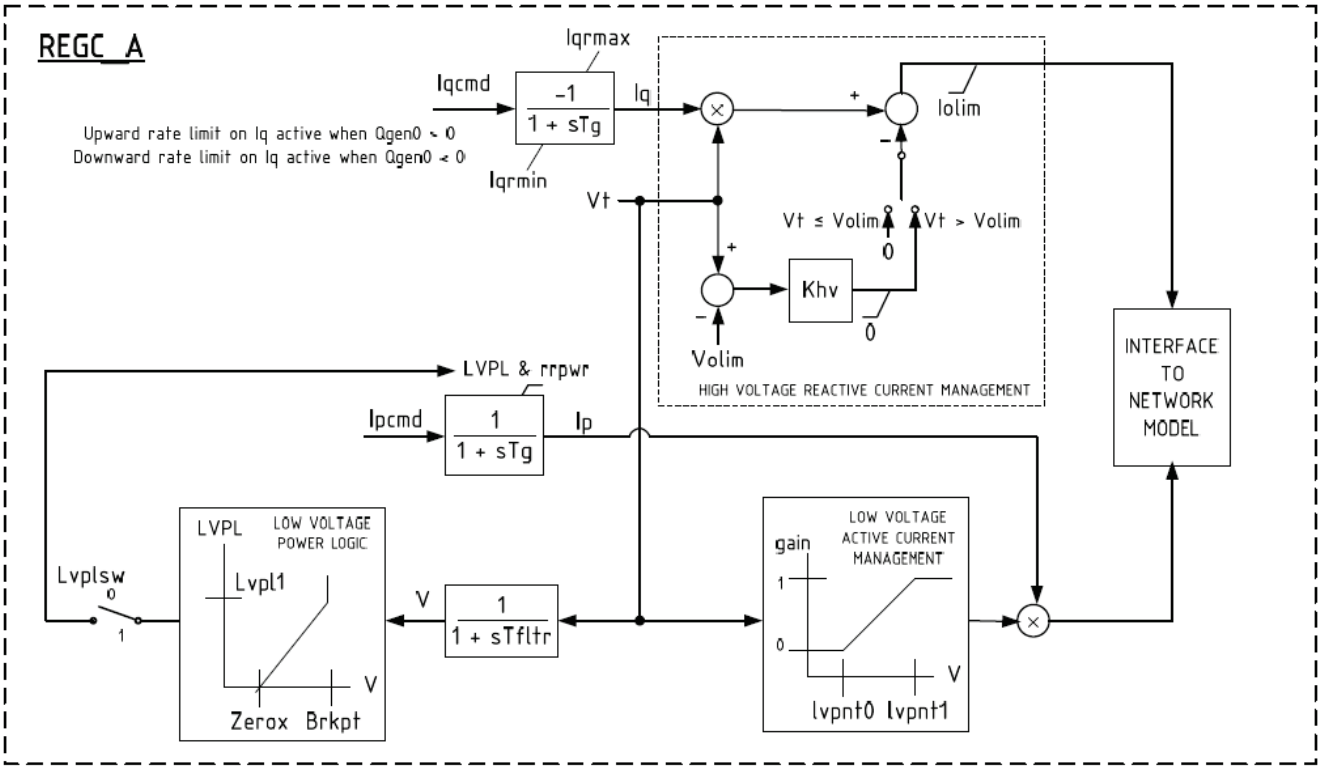

Table A-2. Parameters for the REGC

REGC_A Input Parameters		
Name	**Description**	**Typical Values**
Tfltr	Terminal voltage filter (for LVPL) time constant (s)	0.01 to 0.02
Lvpl1	LVPL gain breakpoint (pu current on mbase / pu voltage)	1.1 to 1.3
Zerox	LVPL zero crossing (pu voltage)	0.4
Brkpt	LVPL breakpoint (pu voltage)	0.9
Lvplsw	Enable (1) or disable (0) low voltage power logic	-
rrpwr	Active current up-ramp rate limit on voltage recovery (pu/s)	10.0
Tg	Inverter current regulator lag time constant (s)	0.02
Volim	Voltage limit for high voltage clamp logic (pu)	1.2
Iolim	Current limit for high voltage clamp logic (pu on mbase)	-1.0 to -1.5
Khv	High voltage clamp logic acceleration factor	0.7
lvpnt0	Low voltage active current management breakpoint (pu)	0.4
lvpnt1	Low voltage active current management breakpoint (pu)	0.8
Iqrmax	Maximum rate-of-change of reactive current (pu/s)	999.9
Iqrmin	Minimum rate-of-change of reactive current (pu/s)	-999.9

REGC_A Internal Variables	
Name	**Description**
Vt	Raw terminal voltage (pu, from network solution)
V	Filtered terminal voltage (pu)
LVPL	Active current limit from LVPL logic (pu on mbase)
Iqcmd	Desired reactive current (pu on mbase)
Ipcmd	Desired active current (pu on mbase)
Iq	Actual reactive current (pu on mbase)
REGC_A Output Channels	
Name	**Description**
Vt	Terminal voltage (pu)
Pgen	Electrical power (MW)
Qgen	Reactive Power (MVAR)
Ipcmd	Active current command (pu on mbase)
Iqcmd	Reactive current command (pu on mbase)
Ip	Active terminal current (pu on mbase)
Iq	Reactive terminal current (pu on mbase)

REEC

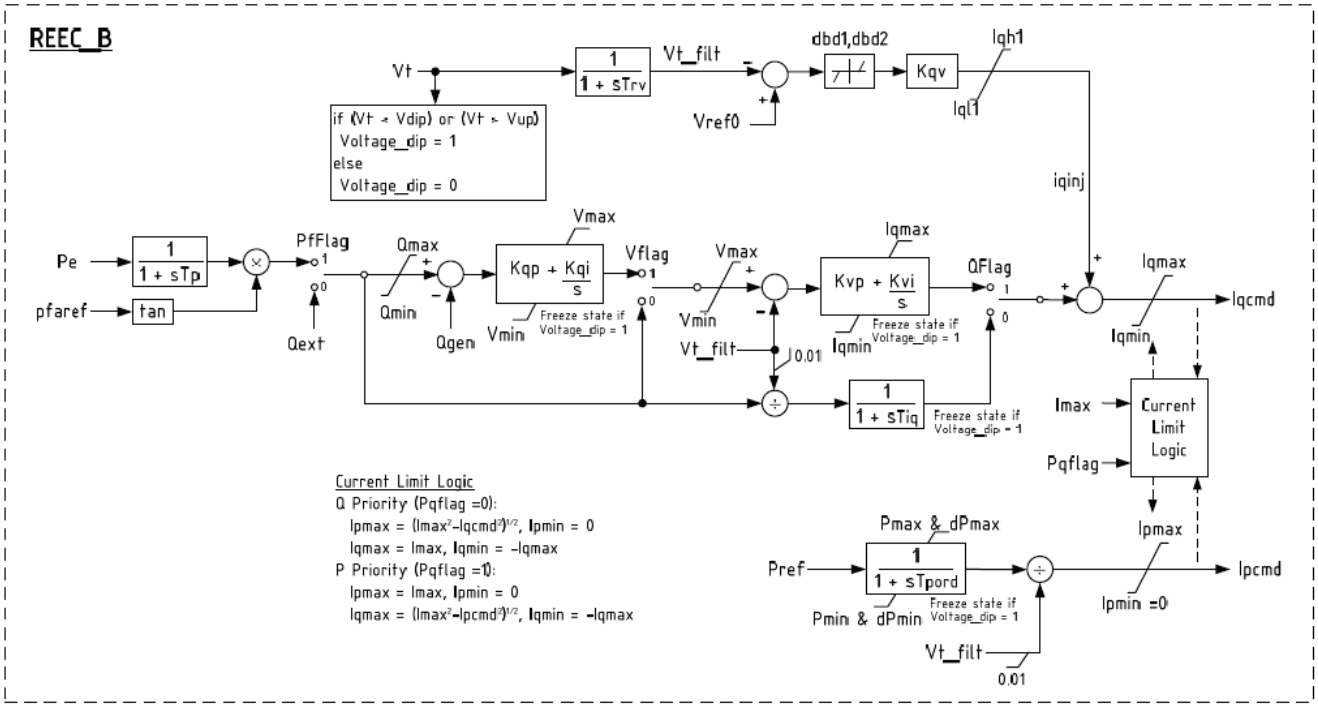

Table A-3. Parameters for the REEC

REEC_B Input Parameters		
Name	**Description**	**Typical Values**
PFflag	Constant Q (0) or PF (1) local control	-
Vflag	Local Q (0) or voltage control (1)	-
Qflag	Bypass (0) or engage (1) inner voltage regulator loop	-
Pqflag	Priority to reactive current (0) or active current (1)	-
Trv	Terminal bus voltage filter time constant (s)	0.01 to 0.02
Vdip	Low voltage condition trigger voltage (pu)	0.0 to 0.9
Vup	High voltage condition trigger voltage (pu)	1.1 to 1.3
Vref0	Reference voltage for reactive current injection (pu)	0.95 to 1.05
dbd1	Overvoltage deadband for reactive current injection (pu)	-0.1 to 0.0
dbd2	Undervoltage deadband for reactive current injection (pu)	0.0 to 0.1
Kqv	Reactive current injection gain (pu/pu)	0.0 to 10.0
Iqhl	Maximum reactive current injection (pu on mbase)	1.0 to 1.1
Iqll	Minimum reactive current injection (pu on mbase)	-1.1 to -1.0
Tp	Active power filter time constant (s)	0.01 to 0.02
Qmax	Maximum reactive power when Vflag = 1 (pu on mbase)	-
Qmin	Minimum reactive power when Vflag = 1 (pu on mbase)	-
Kqp	Local Q regulator proportional gain (pu/pu)	-
Kqi	Local Q regulator integral gain (pu/pu-s)	-
Vmax	Maximum voltage at inverter terminal bus (pu)	1.05 to 1.15
Vmin	Minimum voltage at inverter terminal bus (pu)	0.85 to 0.95
Kvp	Local voltage regulator proportional gain (pu/pu)	-
Kvi	Local voltage regulator integral gain (pu/pu-s)	-
Tiq	Reactive current regulator lag time constant (s)	0.01 to 0.02
Tpord	Inverter power order lag time constant (s)	-
Pmax	Maximum active power (pu on mbase)	1.0
Pmin	Minimum active power (pu on mbase)	0.0
dPmax	Active power up-ramp limit (pu/s on mbase)	-
dPmin	Active power down-ramp limit (pu/s on mbase)	-
Imax	Maximum apparent current (pu on mbase)	1.0 to 1.3

REEC_B Internal Variables	
Name	**Description**
Vt	Raw terminal voltage (pu, from network solution)
Vt_filt	Filtered terminal voltage (pu)
Voltage_dip	Low/high voltage ride-though condition (0 = normal, VRT = 1)
Pe	Inverter active power (pu on mbase)
Pref	Inverter active power reference (pu on mbase, from power flow solution or from plant controller model)
Pfaref	Inverter initial power factor angle (from power flow solution)
Qgen	Inverter reactive power (pu on mbase)
Qext	Inverter reactive power reference (pu on mbase, from power flow solution or from plant controller model)
Iqinj	Supplementary reactive current injection during VRT event (pu on mbase)
Ipmax	Maximum dynamic active current (pu on mbase)
Ipmin	Minimum active current (0)
Iqmax	Maximum dynamic reactive current (pu on mbase)
Iqmin	Minimum dynamic reactive current (pu on mbase, = -iqmax)
Ipcmd	Desired active current (pu on mbase)
Iqcmd	Desired reactive current (pu on mbase)

REEC_B Output Channels	
Name	**Description**
Pref	Reference active power (pu on mbase)
Qext	Reference reactive power (pu on mbase)
Vt_filt	Filtered terminal voltage (pu)
Iqinj	Reactive current from VRT logic (pu on mbase)
Ipcmd	Active current command (pu on mbase)
Iqcmd	Reactive current command (pu on mbase)